Fast Short Circuit Type I Detection Method based on V_{GE}-Monitoring

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Abstract

In this paper, a Short Circuit type I detection method based on the monitoring of the gate voltage is investigated. The proposed detection principle relies on an existing method, which was realized as an integrated solution before. A modified discrete circuit solution is introduced, developed and tested. Moreover, measurements and investigations on different packaging concepts and test conditions are performed. The overview of the functionality, reliability, and restraints of this method, as well as aspects of a supposed dynamic self-adaption feature, are discussed.

Keywords: IGBT, Short Circuit Detection, Gate Drive Unit

INTRODUCTION

A low inductive Short Circuit type I (SC I) event, also known as Hard Switching Fault (HSF), appears when a power transistor is turned on to an already shorted load. It is a critical situation that should be detected and turned off as fast as possible, especially for transistors with reduced short circuit capability, such as on-state-optimized IGBTs [1] [2].

The failure detection based on the desaturation of the power transistor is a well-known and reliable solution but lacks a fast detection time due to the necessity of a blanking time. It also requires space for the circuitry because of the use of high voltage blocking diodes or ohmic-capacitive dividers [3].

Several alternative approaches based on the monitoring of different quantities were proposed. They either interpret one quantity solely, e.g. the load current slope di/dt [4], the Gate-Emitter voltage V_{GE} [5] [6], or more than one quantity in combination. A 2-D detection presented and described in [1] [2] [7] is based on the simultaneous monitoring of both the load-current transient di_C/dt and the gate voltage V_{GE}. In addition, a detection combining a V_{GE} and V_{CE} evaluation was published in [8].

This paper provides an overview of an SC I detection method which is based solely on the monitoring of the gate voltage of the transistor. The SC detection principle was first introduced in [5], where it was realized via an integrated circuit. In this paper, a modified discrete circuit solution is developed and tested. Moreover, investigations on different packaging concepts and test conditions are shown, to provide a more complete overview of the functionality, reliability, restraints, and features of this method.

FUNCTIONAL PRINCIPLE

The detection circuit, which monitors the course of the Gate-Emitter voltage V_{GE} during the turn-on transition of the IGBT, is depicted in the bottom part of Fig. 1. For a normal turn-on process, the Miller-plateau can be observed in the V_{GE} course caused by the decreased Collector-Emitter voltage V_{CE}, which will not take place due to the permanently high V_{CE} voltage under low inductive SC type I conditions. This effect was already discovered and used for detection schemes in [9] and [10]. However, for a high inductive SC type I, a Miller-plateau would be observed due to the transient decrease of V_{CE}. Therefore, the proposed method would not work reliably for the latter case.

V_1 and V_2 describe the voltage level of the capacitors C_1 and C_2, respectively. When the IGBT receives the turn-on signal, C_1 and C_2 are individually charged by the currents I_1 and I_2. I_1 is adjusted higher than I_2, which results in a higher charging speed of V_1 for $C_1 \approx C_2$. Two reference levels V_{Ref1} and V_{Ref2} are defined to stop the charging process of V_1 and V_2, respectively. V_{Ref1} is set below the Miller-plateau level V_{Miller}. Meanwhile, V_{Ref2} is fixed slightly lower than the steady-state value of the positive gate voltage. V_1 stops rising at time t_1 when V_{GE} reaches the value of V_{Ref1}. Similarly, V_2 stops to increase at t_2, when V_{GE} reaches the value of V_{Ref2}. The values of V_{GE} and the reference voltages V_{Ref1} and V_{Ref2} are halved to become processible by the comparators. For V_{GE} this is enabled via an ohmic voltage divider. V_1 and V_2 can be held across C_1 and C_2 by employing two Schottky diodes D1 and D2. At t_2, V_1 and V_2 are compared by Comp3.

The working principle is depicted in the schematic drawings in Fig. 2 and Fig. 3 for a faultless and an SC I turn-on process under consideration of idealistic courses

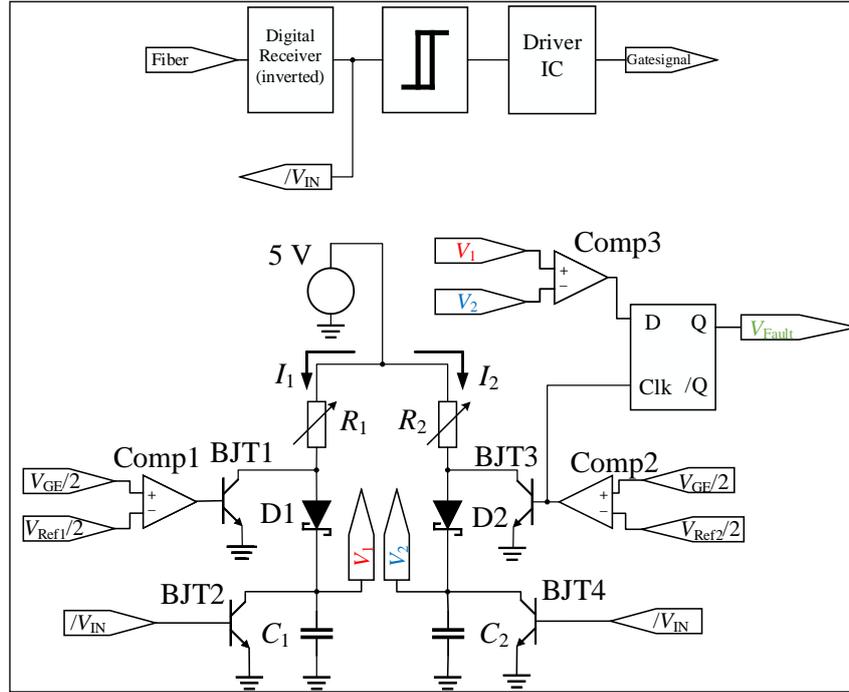for V_1, V_2, and the Fault-Signal V_{Fault} as well as typical courses of V_{GE}.

Fig. 1: Gate-signal-path (top) and detection circuit (bottom).

Under normal turn-on conditions, the relation (1) is applied due to a longer charging time t_2 of V_2, see Fig. 2:

$$V_1 < V_2|t = t_2 \qquad (1)$$

Therefore, (2) holds, see Fig. 3. This results in a fault signal V_{Fault} when the gate voltage reaches V_{Ref2}:
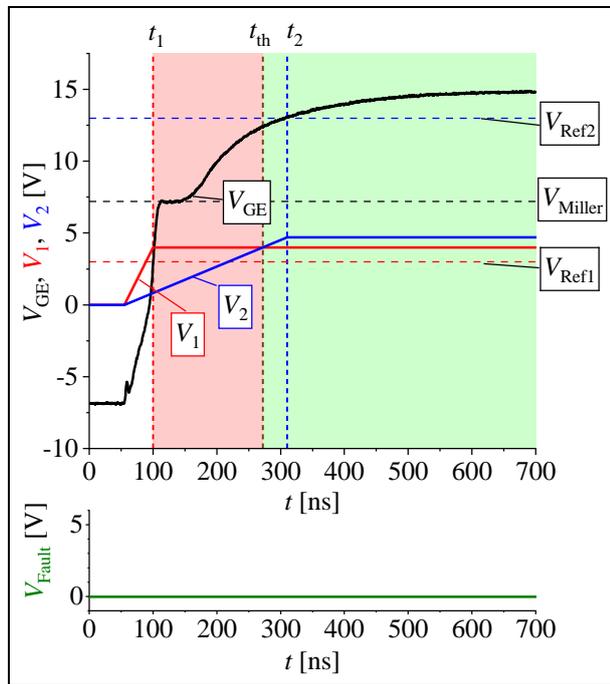
$$V_1 > V_2|t = t_2 \qquad (2)$$

Fig. 2: Working principle with idealistic courses for V_1, V_2 (top), and V_{Fault} (bottom) under normal switching operation.

On the contrary, under SC conditions V_2 does not have enough time to reach the value of V_1, because the rise of V_{GE} is faster without the Miller-plateau.
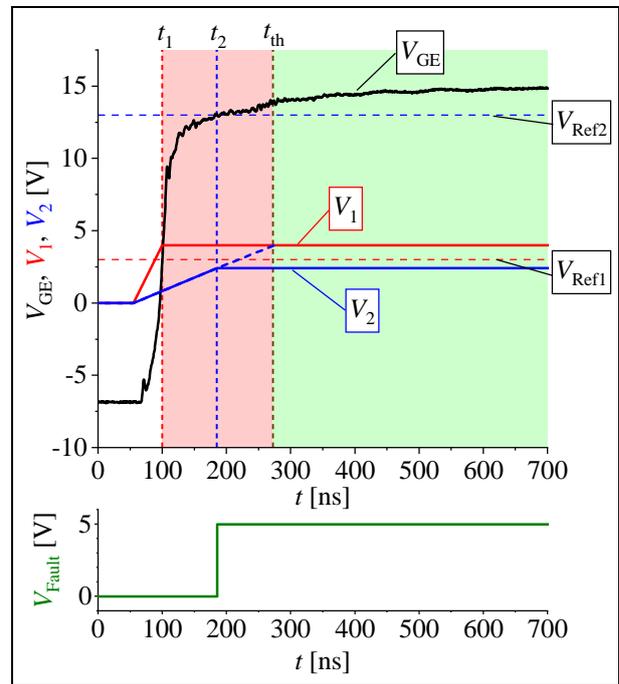

Fig. 3: Working principle with idealistic courses for V_1, V_2 (top), and V_{Fault} (bottom) under SC I turn-on conditions.

The threshold time t_{th} is the time when V_2 exceeds V_1. Since t_{th} is dependent on the rise time t_1 of V_1, t_{th} should automatically be adjusted to a certain value according to the slope of the V_{GE}-course during turn-on. This potentially enables a self-adaption which will be discussed in a later section.

MEASUREMENT SETUP

To prove the detection method´s working principle, application-conform measurements representing normal and SC I turn-on transitions are performed. The load circuit is depicted in Fig. 4. The low-side switch being protected is subjected to a normal turn-on process during the double pulse test. In this case, the high-side consists of a load inductivity L_{Load} and an antiparallel freewheeling diode FWD. For the SC I test, the high-side is shorted before the turn on. The gate voltage is reduced to half by an ohmic voltage divider consisting of two resistors R_{div}, to prevent the comparator input voltage from exceeding the allowable range.
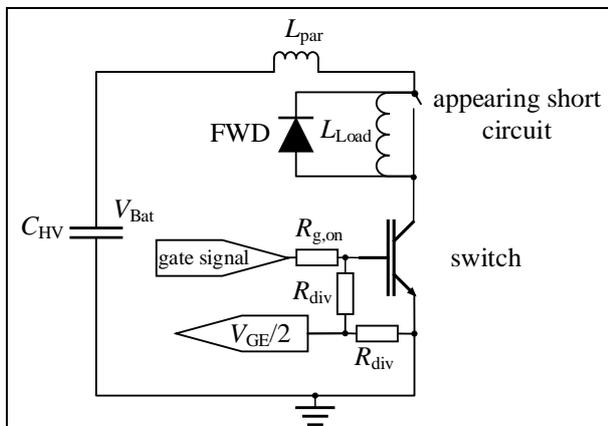

Fig. 4: Load circuit and parts of the gate signal loop for double pulse and SC I test.

The investigations have been carried out with IGBTs in TO-247-3 and EconoPACK-housing from Infineon. In Fig. 5, the proposed circuitry and the module are shown. The PCB on the lower left part of Fig. 5 represents the driver for the switch and its detection circuitry. It was used in this paper for testing IGBTs in both packages as mentioned before.
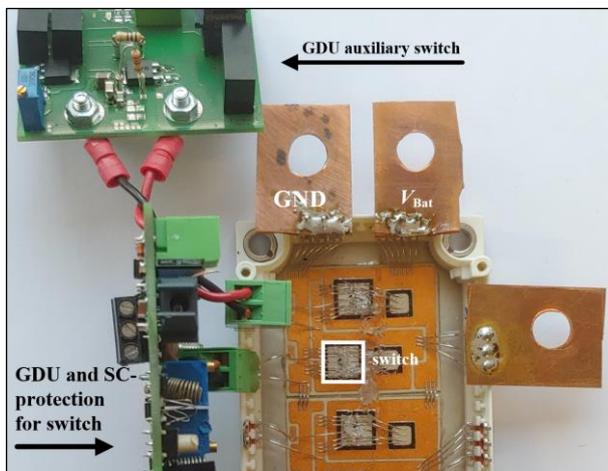

Fig. 5: Connection between EconoPACK-module with Gate Drive Unit (GDU) and detection circuit (bottom left).

MEASUREMENTS FOR GENERAL VALIDATION

In this section, the general working principle and detection accuracy of the method is demonstrated and proved. The following measurements have been generated using an IGBT-module FS75R17KE3 from Infineon in EconoPACK-housing under application-compliant conditions with reference voltages set to $V_{Ref1} = 3.8$ V and $V_{Ref2} = 13.8$ V.

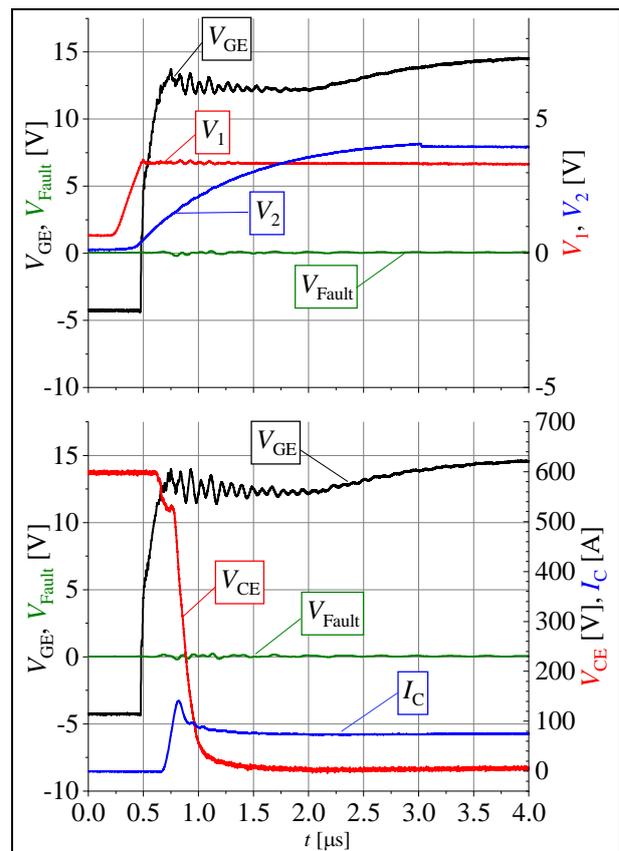For the non-fault case (1) see Fig. 6. There is no fault signal given.

Fig. 6: Courses of detection circuit V_1, V_2 (top), load circuit V_{CE}, I_C (bottom), V_{GE}, and V_{Fault} during normal turn-on process. $V_{Bat} = 600$ V, $I_C = 75$ A, $R_{g,on} = 6.4$ Ω, $L_{Load} = 500$ μH, $L_{par} = 70$ nH; EconoPACK-module.

For all the partial figures showing measurements, V_{GE} is always measured and depicted to demonstrate its relation to V_1 and V_2 or V_{CE} and I_C. V_{Fault} is always shown to prove its validity for each measurement.

At the beginning of the Miller-phase LC-oscillations are visible in the V_{GE} signal excited by the di_C/dt during the current rise and Reverse Recovery event of FWD. Regarding the stray inductance in the gate-loop, the connection between the GDU-detection board and the module is not realized ideally, as can be seen in Fig. 5. However, this does not affect the functionality of the detection circuit concerning the correct classification of a normal turn-on event. Nevertheless, an optimized gate loop design could mitigate this issue.

A successfully detected SC measurement under the same conditions as before is shown in Fig. 7. After turning on for around 300 ns, a short circuit is detected under given measurement conditions.
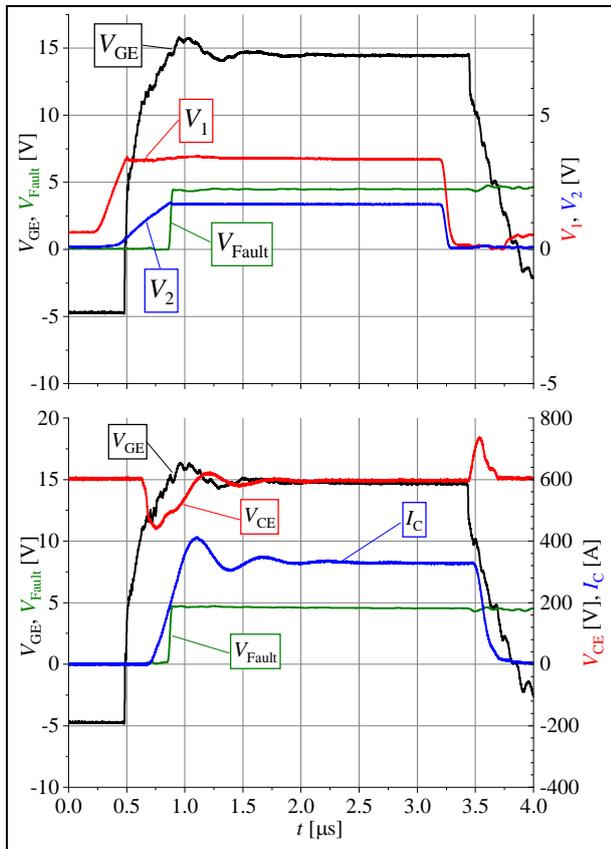

Fig. 7. Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom), and V_{GE} and V_{Fault} during SC I. $V_{Bat} = 600$ V, $I_C = 75$ A, $R_{g,on} = 6.4$ Ω, $L_{Load} = 500$ µH, $L_{par} = 70$ nH; EconoPACK-module.

The first measurements shown in Fig. 6 and Fig. 7 demonstrate that the proposed detection method can successfully distinguish between a normal and a failure turn-on. The detection offers a valid fault signal even before the static value of the positive gate voltage and short circuit current is attained. The detection mechanism can also be used within a 2-level turn-on procedure, where the full positive gate voltage is only released when no fault has been detected in the first turn-on step.

INVESTIGATION ON PACKAGES WITH AND WITHOUT A SENSE PIN

The evaluation of the behavior of the short circuit detection has not only been carried out on modules in EconoPACK-housing but also on devices in TO-247-3 package. Fig. 8 shows the behavior during a normal turn-on process using an IKW20N60T IGBT from Infineon under application relevant conditions. It is visible that, similarly to the EconoPACK-operation, oscillations occur from the appearance of the di_C/dt at turn on. Furthermore, the measured gate voltage V_{GE} is subjected

to a transient increase at the beginning of the Miller-phase between 300 and 350 ns.

Although the current slope di_C/dt for the TO-package is lower compared with the module, a more pronounced V_{GE} overshoot during normal turn-on can still be observed.
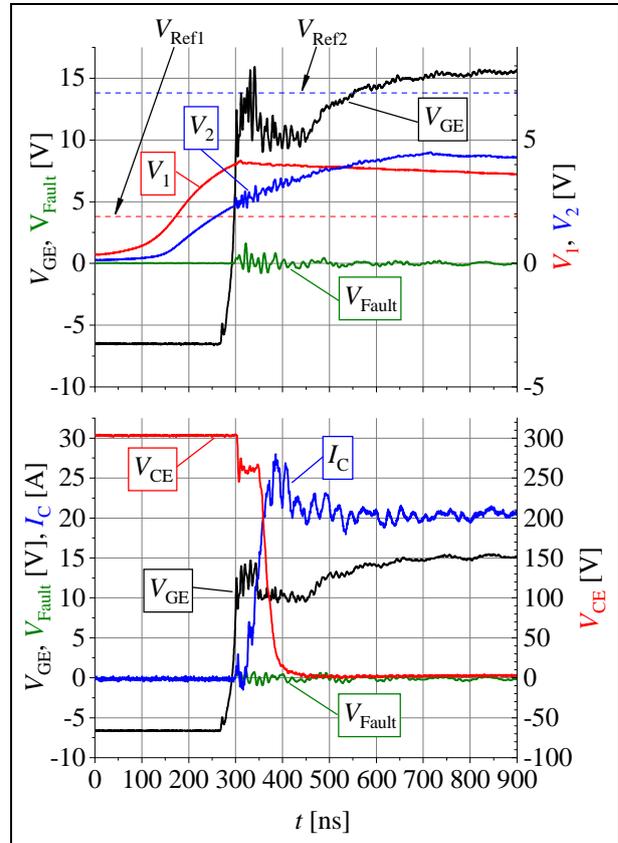

Fig. 8: Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom), and V_{GE}, V_{Fault} during normal turn-on process. $V_{Bat} = 300$ V, $I_C = 20$ A, $R_{g,on} = 6.2$ Ω, $L_{Load} = 500$ µH, $L_{par} = 80$ nH; TO-247-3-package.

The reason for this phenomenon can be found in the different structures of the two packages. Fig. 9 shows the gate loop of the module and how it is affected by a positive load current transient di_C/dt.
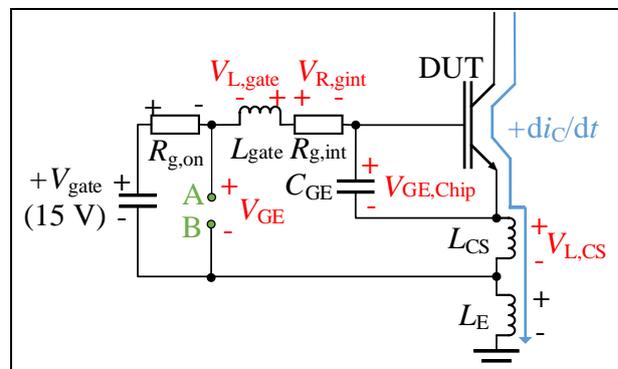

Fig. 9: Structure of the gate loop for a package or module offering a Kelvin sense contact.

The measured gate voltage V_{GE}, which also constitutes the voltage signal being monitored by the detection circuit before division, is picked off at terminals A and B.

4

During the occurrence of a collector current slope, V_{GE} does not correspond to the real chip-internal gate voltage $V_{GE,chip}$. Across the stray inductance in the gate loop L_{gate} and the common-source inductance L_{CS} affected by the gate current slope and the collector current slope respectively, additional voltages are induced:

$$V_{GE} = V_{R,gint} + V_{GE,chip} + V_{L,CS} - V_{L,gate}. \quad (3)$$

As

$$V_{L,CS} + V_{R,gint} > V_{L,gate} \quad (4)$$

applies, (5) holds.

$$V_{GE} > V_{GE,chip} \quad (5)$$

In contrast to the EconoPACK-module, a 3-pin TO-package is not provided with a separate Kelvin sense contact for the gate driver. For the TO-package, L_E in Fig. 9 is nonexistent, but there is a large L_{CS}. Hence, this measurement error produced by L_{CS} for a 3-pin TO-package becomes more pronounced compared to the used module offering a separate Kelvin sense connection.

Furthermore, the so-called self turn-on effect [11] can lead to a transient increase of V_{GE} additionally for both package concepts.

In the measurements shown in Fig. 8, V_{GE} exceeds the second reference V_{Ref2} before t_{th}, which normally would lead to a stopping of the charging process of C_2 and the end of the rise of V_2 accordingly, resulting in the output of a failure signal V_{Fault}. Since the ohmic voltage divider consisting of the two resistors R_{div}, dimensioned with each 2.7 kΩ, is not frequency compensated, $V_{GE}/2$ monitored by the detection logic is delayed to the original course of V_{GE}. To ensure fast and precise monitoring of the gate voltage, which this detection approach is aiming at, such a delay is generally considered as a disadvantage regarding the accuracy, especially for fast transitions. However, in the stated example this lack of precision turns into an advantage as it offers a certain level of robustness against the described transient gate voltage overshoot, oscillations, and noise. This results in a correctly detected normal turn-on process for the case depicted by Fig. 8. Nevertheless, when decreasing R_{div} to 1 kΩ, the divider proves fast enough to be sensitive to the disturbance resulting in the output of a fault signal constituting a wrongly detected SC I turn on (false positive). Due to this issue, a precise and reliable operation of the detection circuit cannot be ensured and proven under all conditions when applying this detection method to a package missing a Kelvin sense emitter. Instead, the usage of a device with a Kelvin sense emitter is required and recommended.

VARIATION OF TURN-ON RESISTANCE AND SELF-ADAPTION

Apart from the fast detection speed, the proposed method's capability to dynamically self-adapt should also be given. Specifically, a change of the V_{GE} slope without any readjustment via R_1 or R_2 in Fig. 1 or the reference voltages is highlighted. A change of the switching speed may occur due to a change of the gate turn-on resistor or the input capacitance. The functionality of this V_{GE}-based detection method under an expanded condition set and its claimed self-adaption feature under different V_{GE} slopes shall be investigated in this section. For this purpose an evaluation under a variation of the $R_{g,on}$-values is performed.

Functional capability under a variation of $R_{g,on}$

As the differences of the gate voltage courses get smaller with an increase in switching speed, distinguishing between normal and failure turn-on processes is considered to be more critical for low $R_{g,on}$-values.
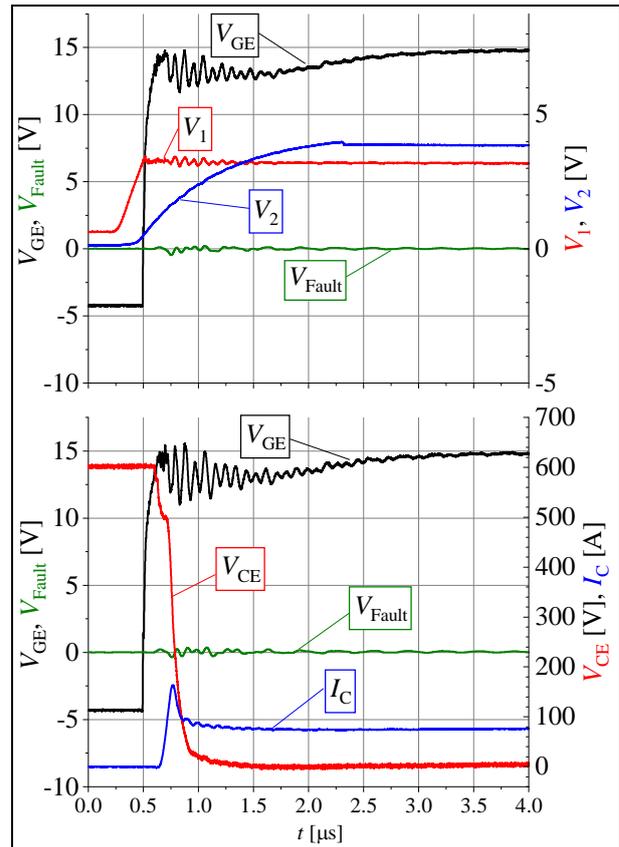
Fig. 10: Courses of detection circuit V_1, V_2 (top), load circuit V_{CE}, I_C (bottom), V_{GE}, V_{Fault} during normal turn-on process. $V_{Bat} = 600$ V, $I_C = 75$ A, $R_{g,on} = 1.7$ Ω, $L_{Load} = 500$ µH, $L_{par} = 70$ nH; EconoPACK-module.

According to the aforementioned results shown in Fig. 6 and Fig. 7, where a datasheet-$R_{g,on}$ of 6.4 Ω is used, measurements with an $R_{g,on}$ of 1.7 Ω and 3.5 Ω, respectively have been carried out. For both values, the separation of normal and failure cases is working reliably.

5

Fig. 10 and Fig. 11 show the measurement results for $R_{g,on} = 1{,}7\ \Omega$ representatively.
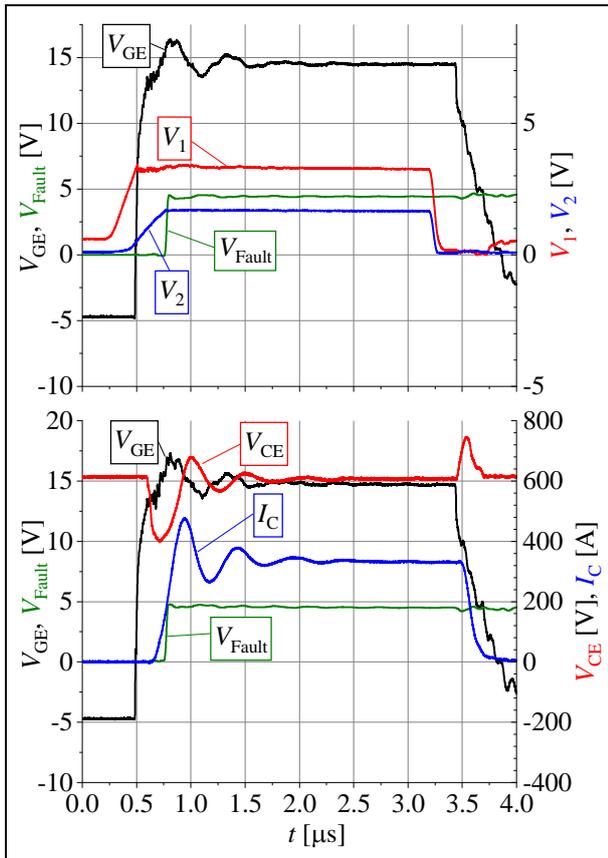

Fig. 11: Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom) and V_{GE}, V_{Fault} during SC I. $V_{Bat} = 600\ \text{V}$, $I_C = 75\ \text{A}$, $R_{g,on} = 1.7\ \Omega$, $L_{Load} = 500\ \mu\text{H}$, $L_{par} = 70\ \text{nH}$; EconoPACK-module.

Investigation on self-adaptive behavior

Conventional gate voltage-based SC I detections rely on attaining one reference voltage level within a certain time to detect a potential short. A big advantage of the proposed detection method is claimed to be the utilization of two reference voltages [5]. In theory, this allows the detection circuitry to dynamically self-adapt to different V_{GE} slopes, as the time t_{th} will automatically shift to certain values when t_1 is changed due to flatter or steeper V_{GE} slopes.

For a conventional gate voltage-based SC I detection the top of Fig. 12 depicts the V_{GE}-courses of normal and failure turn-on processes for a variety of V_{GE} slopes schematically. t_{th} is fixed to a constant value, represented by the constant V_1. V_2 is, similarly to the method discussed in this paper, used to assess the turn-on speed and to distinguish between a normal and a failure turn-on (see Fig. 12 bottom). As a result, the conventional approach would classify both a fast normal turn-on (Fig. 12: steep slope, normal), as well as a slow failure turn-on (Fig. 12: flat slope, SC I) incorrectly. Only the case for medium slopes is assessed correctly, as t_{th} fits to the proper separation of normal and SC I turn on.
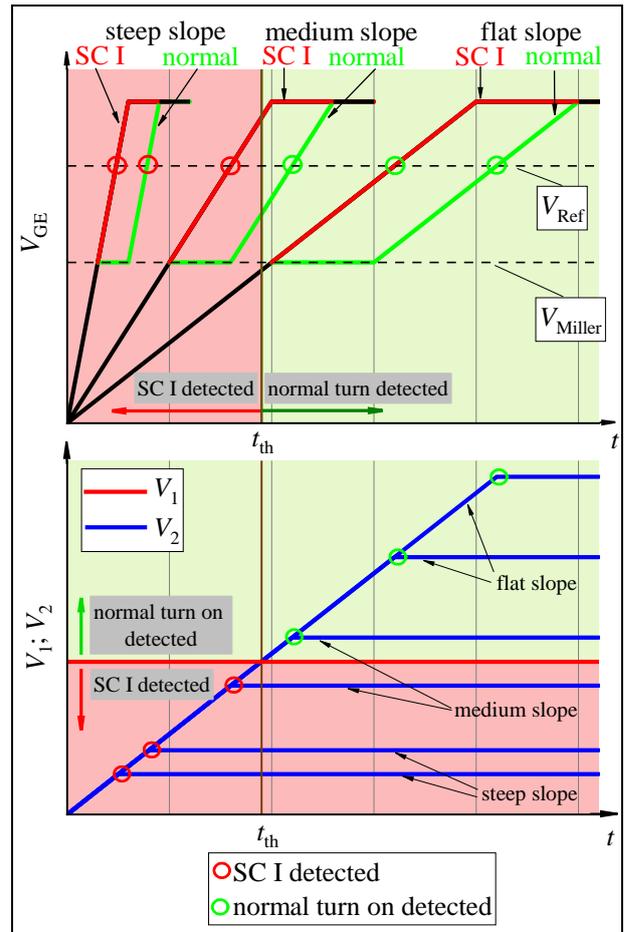

Fig. 12: Simplified schematic courses of V_{GE} for three different slopes under normal and low inductive SC I turn-on conditions for conventional gate voltage based method (top). Courses of the detection circuitry with only one voltage reference (V_{Ref}, top, represented by V_1, bottom). To provide comparability with the approach presented in this paper, V_1 is set to a constant value, representing the fixed threshold time t_{th} (see also [5]).

In contrast, the proposed principle relying on two voltage reference levels should categorize all switching events correctly. This can be achieved because t_{th} is correlated to the variable value of t_1. Therefore, t_1, describing the time within which V_{Ref1} is attained, acts as a determining factor and is used to adjust t_{th} and set it to a certain value according to the switching speed being present in the interval for $V_{GE} < V_{Ref1}$. Given this mechanism, also schematically depicted in Fig. 13 for the steep and flat slope case, a self-adaption to different switching speeds shall be enabled without the necessity to readjust the circuitry. The appropriate schematic courses of V_1 and V_2 are drawn in the lower part of Fig. 13.
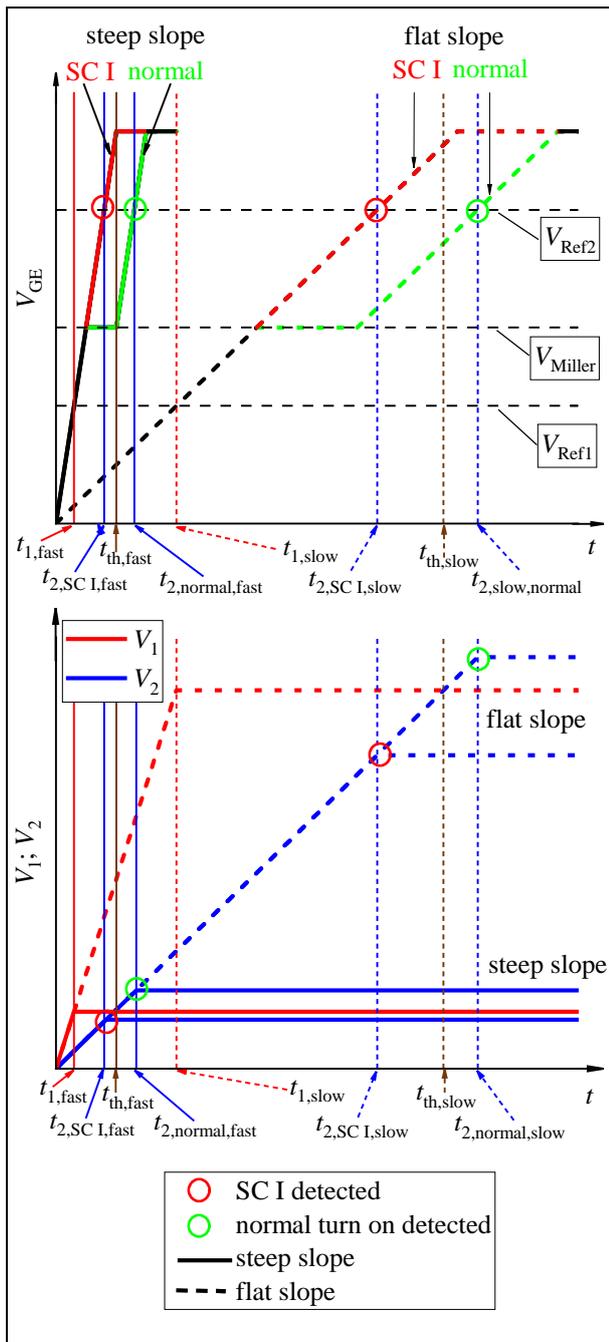
Fig. 13: Simplified schematic courses of V_{GE} for the steep and flat slope cases of Fig. 12 under normal turn-on and SC I conditions (top). Courses of the proposed detection circuitry using two voltage reference levels (bottom). t_{th} is set dynamically according to t_1, which adapts to the slope of V_{GE} (see also [5]).

Regarding the measurements shown in this paper for the EconoPACK-housing, the correct classification of the switching events for different $R_{g,on}$-values between 1.7 Ω and 6.4 Ω, shown in Fig. 6, Fig. 7, Fig. 10 and Fig. 11, could be obtained without a readjustment of the detection circuitry. Nevertheless, this achievement does not rely on dynamic self-adapting behavior. Fig. 14 displays the comparison of the V_{GE}-courses for the fastest normal turn-on at $R_{g,on} = 1.7$ Ω and the slowest SC I turn-on at $R_{g,on} = 6.4$ Ω.
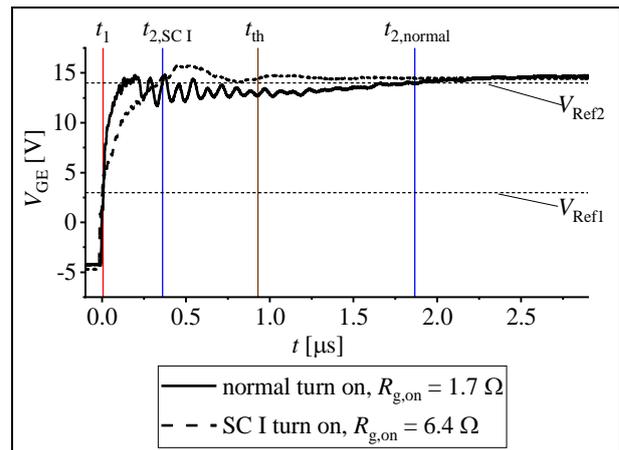

Fig. 14: V_{GE} for the fastest normal turn on at $R_{g,on} = 1.7$ Ω and the slowest SC I turn on at $R_{g,on} = 6.4$ Ω.

The slight exceedance of V_{Ref2} at the beginning of the Miller-phase is not taken into consideration by the detection circuitry because of the already explained smoothing behavior of the ohmic voltage divider. Despite the smaller $R_{g,on} = 1.7$ Ω, the normal turn-on process is still slower than the SC I turn on at higher $R_{g,on}$ (6.4 Ω) regarding the surpassing of the second reference V_{Ref2}. The correct categorization of both the cases shown in Fig. 14 without any readjustment is based on this fact instead of a dynamic self-adaption.

In contrast to the theoretic considerations of Fig. 12 (top) and Fig. 13 (top), the crossing of the first reference V_{Ref1} does not change significantly with a variation of $R_{g,on}$ within a certain range. As a result, a dynamic self-adaption would not happen in this case. The weak dependence of t_1 on $R_{g,on}$ is also due to the relatively high internal gate resistance $R_{g,int} = 8.5$ Ω present in the DUT, which attenuates changes of the external gate resistance. The self-adaptive behavior can only be proven, when the SC I turn-on is slower than the normal turn-on across the entire V_{GE}-course (see Fig. 13). In this case, a conventional gate voltage-based detection method would fail (see Fig. 12). Furthermore, a self-adaption could potentially only take place if the surpassing of V_{Ref1} occurred at considerably different times t_1 for both cases so that an adjustment of t_{th} could take place.

CONCLUSION

A discrete gate voltage-based SC I detection introduced in [5] has been presented and tested. The results show that the proposed method can detect a low inductive SC type I failure in a very fast and reliable way. The failure will be detected when V_{GE} attains the second voltage reference level. For the used 75 A EconoPACK-module, the SC I was detected 270 ns and 300 ns after turn-on for external gate turn-on resistances of 1.7 Ω and 6.4 Ω, respectively. Subsequently, for different gate resistors and input capacitances, the detection speed varies.

Furthermore, the reliability of the method highly depends on the package form of the DUT.

The reliability and functionality are applied for a package offering a sense emitter contact with a low L_{CS} design. The packages, which are not provided with a Kelvin sense, such as 3-pin TO-247 devices, as tested in this paper, are not recommended. Special attention should be paid to an operation at high load currents or turn-on transitions with low gate turn-on resistances since the voltage level of the Miller plateau depends on the level of load current and IRRM. This aspect can affect the detection method´s functionality when an overload current or a high IRRM is observed.

The expected self-adaptation of the detection for a varied V_{GE} slope highly depends on the DUT´s chip design, such as internal gate resistance and input capacitance C_{iss} (current rating).

However, the detection method demonstrated in this paper appears to be suitable also for bigger modules such as IHM (IGBT High Power Module), since the internal gate resistance is usually small and the common-source inductance L_{CS} is significantly optimized. Moreover, the high C_{iss}, due to a large number of chips in parallel, enables a wide detection time window for the varied V_{GE} slope. Finally, in comparison to the conventional V_{CE}-monitoring, the gate driver board is not exposed to high voltage, which provides more safety for the control unit and the driver itself.

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