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Singular Point Source MOS (S-MOS) Cell Concept

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Abstract

A Singular Point Source MOS (S-MOS) cell concept suitable for power semiconductor MOS based devices is presented. The S-MOS differs from a standard Planar or Trench MOS cell in the manner by which the total channel width per device area is determined. The S-MOS cell channel width is defined as the peripheral length of a line running approximately along the N++ source and P channel junction which is situated on a single gated trench side-wall. The length of the line can be established from a singular point source implant for forming the N++ source region which corresponds to the shape of the N++/P junction. The total channel width will therefore depend on the total number of gated trench side-walls per chip. Despite a relatively short channel width obtained on a single trench side-wall, narrow mesa dimensions between adjacent trenches will provide an adequate number of cells for adjusting the total channel width as required for a given device performance. The S-MOS can be realized by simple manufacturing processes and presents an alternative approach for MOS cell layouts by decoupling critical design parameters (e.g., channel width, trench dimension and NPN transistor area). This flexibility can lead to lower overall losses, lower gate charge levels, improved switching robustness and controllability for different MOS based devices.

Keywords: MOS devices, MOSFETs, Insulated gate bipolar transistors.

INTRODUCTION

MOS cell process/design platforms were developed over the years enabling advanced power devices such as the power MOSFET [1] and the Insulated Gate-Bipolar Transistor (IGBT) [2]. Both devices have been based on planar or trench MOS cells with a continuous development trend toward cell miniaturization which led to clear improvements in the overall performance over the years [3]. In particular, optimized trench gate designs target lower conduction losses and gate charge levels for optimum switching performance. Furthermore, special trench gate shielding features were also required for improving the device blocking, robustness and stability.

For IGBTs, modern structures employ Narrow Mesa trench designs for lowering the on-state losses. Typically, trench based IGBTs include non-active separation regions between active cells for lowering the channel width to achieve good short circuit capability [4][5]. However, trench IGBTs still require improvements in switching controllability especially for higher voltage devices [6][7].

On another development front with respect to wide bandgap semiconductors such as Silicon Carbide, the advances made on Silicon based MOS devices have provided a strong base for developing SiC power MOSFETs and IGBTs [8]. For SiC power MOSFETs, high cell packing densities are essential. In recent years, advanced 3D design concepts have been proposed [9] similar in a way to the low voltage lateral FINFET cell structure [10] as they rely on multi-dimensional channel width arrangements for increasing the cell density and reducing the on-state resistance R_{dson}.

In this paper, a new "Singular Point Source" MOS cell concept (S-MOS) is presented having improved design features for enabling higher performance levels when compared to standard MOS cell designs.

BACKGROUND AND NEW TECHNOLOGY

For a conventional CELLULAR type MOS cell layout design based on planar or trench gates, the channel width W_{ch} (also referred to as channel area) is defined as the total peripheral length along all the N++ source regions (or the total N++/P junction peripheral length). For LINEAR cell layouts as shown in FIG. 1 for both planar and trench MOS cells, W_{ch} is the longitudinal extension length of the N++ source in the third dimension [11]. For both cellular and linear designs, the total W_{ch} is defined by careful selection of certain mask dimensions when introducing the channel and source regions.

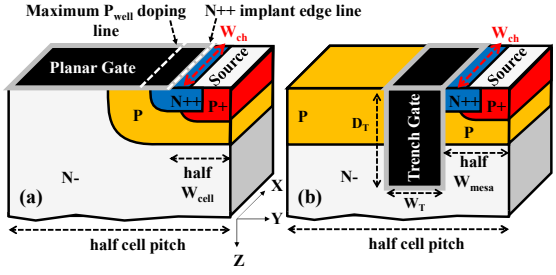

Fig. 1. Standard 3D linear Planar MOS cell (a) and Trench MOS cell (b).

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It is important to note that the channel electrical characteristics are mainly defined at the highest P doping concentration positions in the P channel region. Therefore, W_{ch} is more accurately defined as the peripheral length in the P channel region where the P doping is at maximum. For linear designs, W_{ch} is defined by either the N++/P junction or the highest P doping longitudinal extension lengths since they are geometrically the same. The same rule applies for a Trench cellular layout due to the vertical channel (i.e., no lateral difference between N++/P junction and the highest P doping peripheral lengths). However, for a planar cellular layout with rounded edges (e.g., circular or hex), there is a difference since the highest P doping peripheral length is larger than the N++/P junction peripheral length.

Typically, the distance from the N++ source implant edge to the maximum P channel doping point can range from 0.3 µm to 1 µm. The S-MOS concept described in this paper is in principle based on this design feature which presents a new approach for the MOS cell design. The 3D S-MOS structure is depicted in FIG. 2 along with the critical cell dimensions. The S-MOS 2D cross section at the trench side-wall is shown in FIG. 3 along the cutline A-A` outlined in FIG. 2.

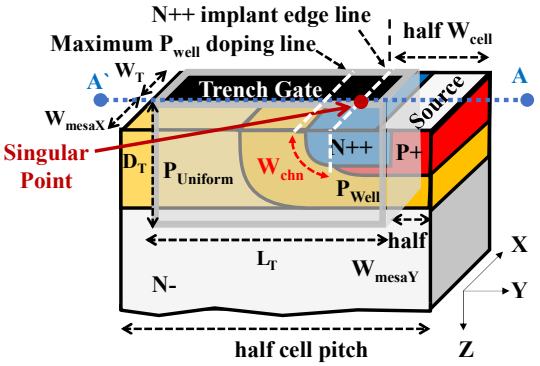

Fig. 2. Conceptional 3D S-MOS cell.

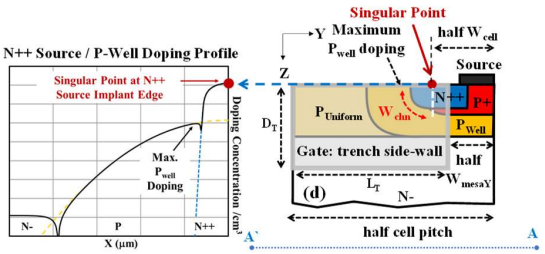

Fig. 3. S-MOS 2D cross section alone A-A` cutline in Fig.2 (at the trench side-wall) and doping concentration profile for the S-MOS P-Well version.

The key element for the S-MOS is the single unit channel width W_{chn} formed in the inversion layer of a gated trench side-wall. In this case, the channel width is not defined by a mask geometry (i.e., not an N++ extension line as in conventional designs), but is devised from a singular point source implant position which forms the N++ source and also the P-channel region (by implants through a mask and diffusion). The resulting doping profile will subsequently define W_{chn} on a single trench side-wall. The total device channel width W_{ch} becomes the sum of the W_{chn} formed on all trench side-walls. By implementing narrow mesa dimensions < 1 µm between active trench gates, the total W_{ch} is adequate for different power device design requirements.

There can be two types of P channel regions as shown in FIG. 2 and FIG. 3. This includes a P_{Well} profile similar to a P-type channel region employed in a planar design and a $P_{Uniform}$ profile similar to a P-type channel region employed in a trench design. Both P profiles can be formed by implantation and diffusion to resulting in gaussian profiles. While a P_{Well} forms a gaussian profile in both vertical and lateral dimensions from the singular point location, the $P_{Uniform}$ only forms a gaussian profile in the vertical dimension. For the later, a channel cannot form on the trench side-wall near the surface of the device as in the P_{Well} case. The S-MOS design also includes a key feature to prevent vertical trench channels from forming on the inner trench side-walls by extending the highly doped P+ base region under the N++ source. This ensures N++ protection during switching and potentially improved device robustness and stability. Furthermore, the length of the trench L_T can be adjusted to reduce the gate charge Q_G for improved switching behaviour and therefore, resulting a full or partial S-MOS trench design as described in the following section.

SIMULATION MODELS

The S-MOS concept was modelled using SILVACO 3D-TCAD software [12]. For the S-MOS proof of concept and to achieve efficient simulation time consumption, 150V MOSFET structures were modelled. On the other hand, for the reference planar and trench designs, 2D modelling was sufficient. We note that the 150V MOSFET investigation was not carried out to benchmark the structures with best-in-class equivalent devices, but as a qualitative exercise for comparing the new S-MOS with reference MOS cells concepts. For different type of MOS devices, the S-MOS will still require further optimization depending on the device type, rating and target performance.

Two S-MOS variants were investigated as shown in FIG. 4 having both a half-cell pitch of 5 µm. Design (A) employs a PARTIAL trench with a uniform type P channel doping region (L_T=1.5 µm) while Design (B) has a FULL extended trench and a P-well type channel region (L_T=4 µm). The total device thickness was 15 µm with a drift doping concentration of 1e15 /cm^3. The N++ drain had a maximum doping of 1e20 /cm^3 and depth of 1 µm. FIG. 5 shows the 3D S-MOS partial model doping concentration near the source from both sides of a half-cell unit with one trench side-wall. The P-channel region depth (main PN junction) was 3 µm deep while the

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maximum doping concentration was adjusted to obtain approximately the same saturation current levels for all devices. The maximum doping concentration for the N++ source and P+ contact was set at 1e20 /cm^3 and 5e19 /cm^3 respectively. The 2D planar design has a cell opening W_{cell} of 2 µm while the 2D trench design had a W_{mesa} of 1 µm. The S-MOS has a trench mesa W_{mesaX} around 0.5 µm (between orthogonal trenches) and a trench mesa W_{mesaY} around 1 µm (i.e., the half-cell in X dimension = 0.75 µm). The S-MOS W_{cell} was set at 2 µm (distance between two singular points) while the P+ region extended laterally below the N++ source to ensure channels are only formed on the trench side-walls. All trenches had a width W_T of 1 µm and depth D_T of 5 µm.

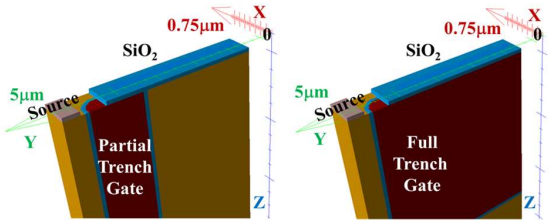

Fig. 4. 3D S-MOS models with partial (a) and full (b) trench.

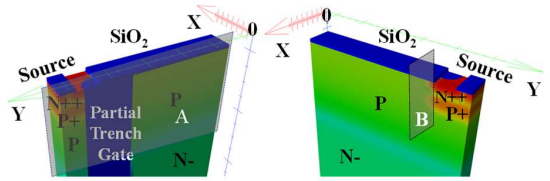

Fig. 5. 3D S-MOS Partial trench doping concentration (two sides of cell unit).

SIMULATION RESULTS AND DISCUSSION

For a 1 cm^2 scaled MOSFET, the linear planar and trench models had a total W_{ch} of 20 meters. For the S-MOS models, the W_{ch} per trench side-wall was approximately 0.75 µm leading to a similar total channel width W_{ch} per 1 cm^2 as for the reference devices. The channel parameters were adjusted to achieve similar saturation currents for all devices as shown in FIG. 6 for the IV output characteristics curves at 300K. At V_{gs}=10V. The S-MOS has an R_{dson} value similar to the trench device below 6 mohm/cm^2 when compared to the planar MOSFET which is around 8.6 mohm/cm^2. The full Trench S-MOS show the lowest levels below 5 mohm/cm^2. The S-MOS TCAD model for the patrial trench electron concentration at 2V is shown in FIG. 7. To better visualize the S-MOS during conduction, the cut planes A and B outlined in FIG. 5 are presented in FIG. 8 for the electron concentration. Cut A is at 0.5 µm in X direction (at the inversion layer of the trench side-wall) and cut B at 3.5 µm in Y direction (at the highest P channel doping). The figure show that the P+ base region placed under the N++ source region ensures no trench MOS channel is formed on the inner trench walls as explained earlier.

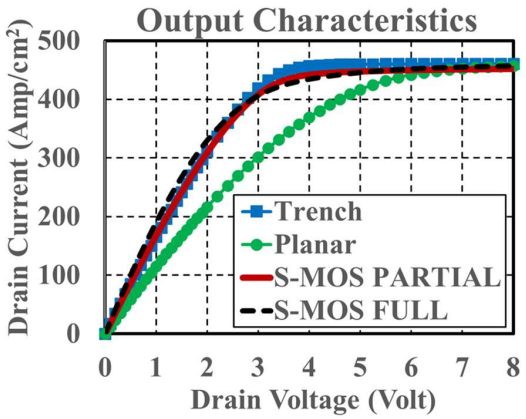

Fig. 6. 150V MOSFET IV output characteristics at 300K.

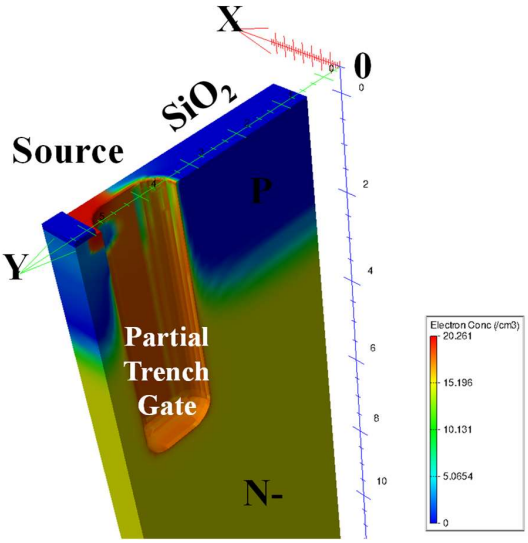

Fig. 7. 3D S-MOS partial trench electron concentration distribution at 2V, 300K.

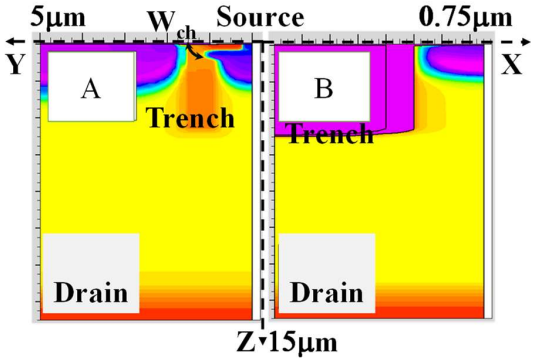

Fig. 8. S-MOS partial trench 2D cut sections cut A and B as shown in FIG. 5 for the electron concentration at 2V.

The IV transfer characteristics at 300K are shown in FIG. 9. All devices display normal behaviour with S-MOS devices exhibiting lower threshold voltage levels compared to reference devices due to higher current densities at the channel formed at trench gate oxide - planar gate oxide corner.

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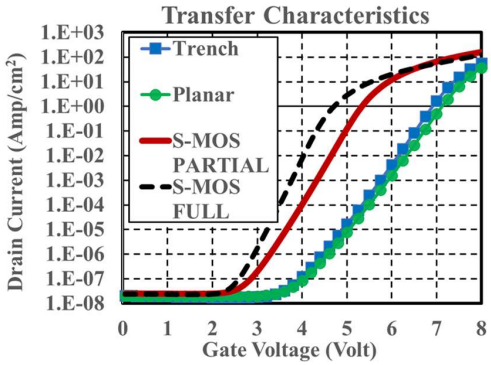

Fig. 9. 150V MOSFET IV transfer characteristics at 300K.

The IV blocking characteristics at 300K are shown in FIG. 10. The S-MOS shows higher blocking capability when compared to the trench MOSFET but still lower than the planar MOSFET. Trench devices typically show lower blocking due to the presence of the higher peak electric field associated with the trench bottom corner as shown in FIG. 11 for the Partial trench S-MOS at 150V.

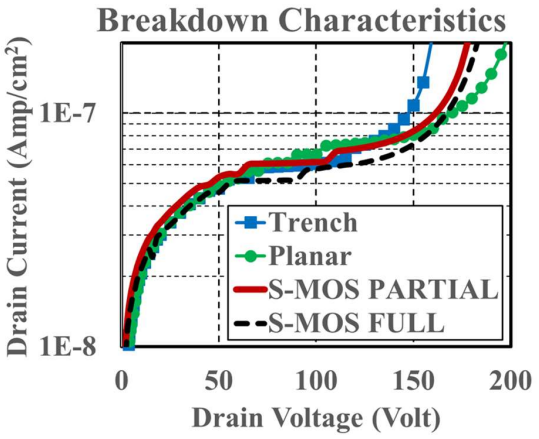

Fig. 10. 150V MOSFET IV breakdown characteristics at 300K.

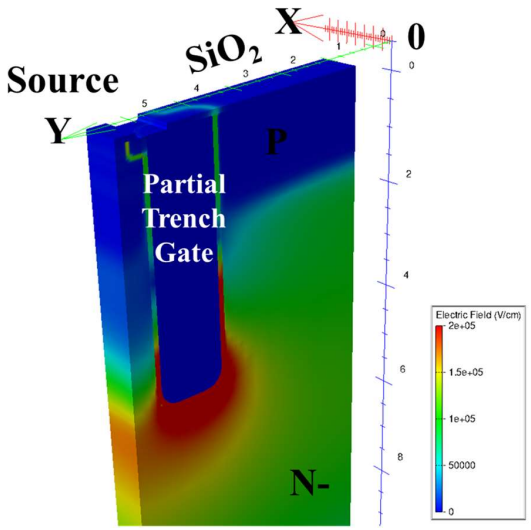

Fig. 11. 3D S-MOS partial trench electric field distribution at 150V, 300K.

Resistive switching results at 300K were obtained for all devices at V_{gs}=10V, DC voltage of 75V and a current of 100 A/cm^2. FIG. 12 and FIG. 13 show both the turn-off and turn-on current and voltage waveforms under such conditions respectively. For the same gate resistance R_G=1ohm, the devices show different switching behaviour which is dependent on the device input capacitance and gate charge levels. During turn-off, the much larger gate capacitance of the full trench S-MOS shows long delay times while the partial version matches that of the standard trench MOSFET. The planar device shows the shorter delay time as expected. During turn-on, the trench MOSFET deviates in the performance with slower di/dt and voltage fall times.

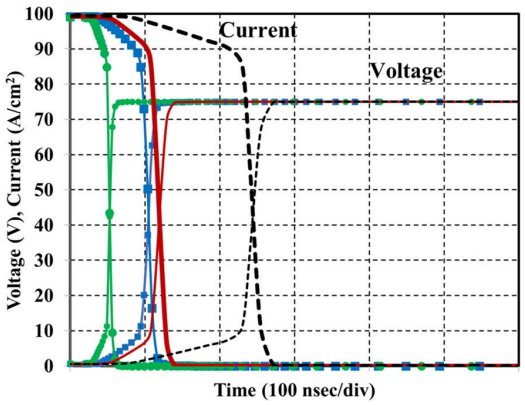

Fig. 12. 150V MOSFET turn-off resistive switching curves at 300K, 75V, 100A/cm^2 and R_G=1ohm.

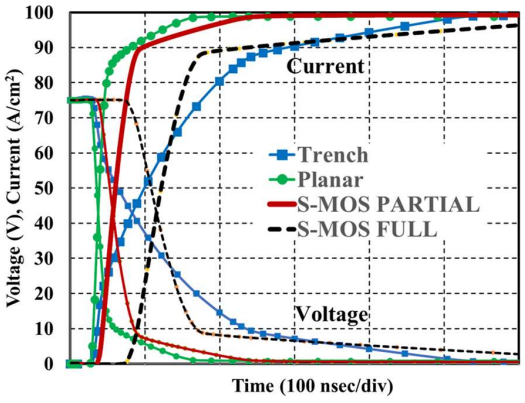

Fig. 13. 150V MOSFET turn-on resistive switching curves at 300K, 75V, 100A/cm^2 and R_G=1ohm.

To understand the switching behaviour obtained from the mixed mode simulations, the Gate Charge Q_G curves (V_{ge} versus Q_G) were extracted during the turn-on transient as shown in FIG. 14. The effect of L_T is clearly demonstrated showing that the S-MOS with partial trench can lead to low gate charge levels similar to those reach with trench gate designs. However, much lower turn-on losses can be achieved with the S-MOS concept due to the lower miller voltage plateau associated with this cell design as shown in FIG. 14.

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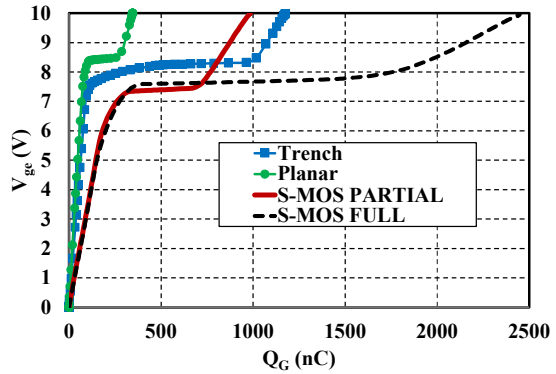

Fig. 14. 150V MOSFET turn-on resistvie switching associated Gate Charge curves at 300K.

A full summery of the static and dynamic parameters is provide in Table .1. It is clear that the switching losses of the partial S-MOS are much lower than the trench device while at the same time providing similar and low R_{dson} levels. Therefore, in principle, the S-MOS concept has the potential to provide benchmark performance after carful design optimisation and in relation to a given MOS based device concept.

Device	R_{dson}(ohm/cm^2)	V_{th}(V)	V_{bd}(V)	E_{on}(µJ)	E_{off}(µJ)	Q_G(nC)
Trench	0.00591	5.75	160	460	55	1175
Planar	0.00863	6	200	155	25	346
S-MOS PAR	0.00578	4.4	180	165	55	984
S-MOS FULL	0.00486	3.8	185	360	135	2308

Table 1. 150V MOSFET parameters under static and dynamic conditions at 300K (Switching: 75V, 100A/cm^2 and R_G=1ohm)
.

S-MOS OUTLOOK: Si IGBT and SIC MOSFET

To explore the potential of the S-MOS cell on high voltage devices, the new design was simulated for a 1200V IGBT 3D structure and compared to the latest Narrow Mesa Trench NM-IGBT designs having a W_{mesa} down to 1 µm [13]. For this case, the IGBT investigation provides an insight into the S-MOS behaviour for a bipolar device. A full and partial S-MOS trench design was implemented albeit with a P_{Well} doping profile as shown in FIG. 15. The S-MOS was capable of matching the NM-IGBT static performance in terms of conduction losses while also providing lower switching losses along with higher blocking capability. A full set of static and dynamic simulation results can be found in the referenced publication.

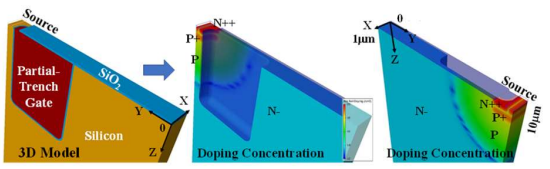

Fig. 15. 3D 1200V S-MOS IGBT model and net doping concentration.

The next step was to carry out the simulation study for a 1200V Silicon Carbide SiC MOSFET 3D structure as shown in FIG 17. Initial results show promising performance as shown in FIG. 18 for the IV output characteristics. The S-MOS is compared to a planar SiC MOSFET at 425K for a 1 cm^2 active area device. The S-MOS provides an R_{dson} around 3 mohm/ cm^2 compared to 5 mohm/cm^2 for the planar MOSFET. The full set of results will be published in a future article [14].

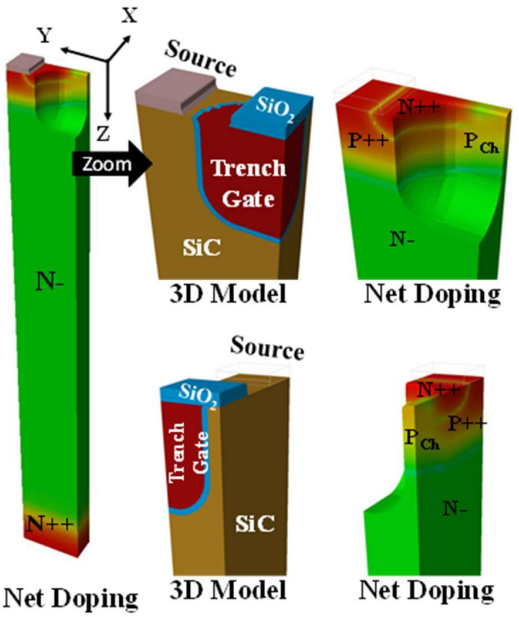

Fig. 17. 3D 1200V S-MOS SiC MOSFET model and net doping concentration.

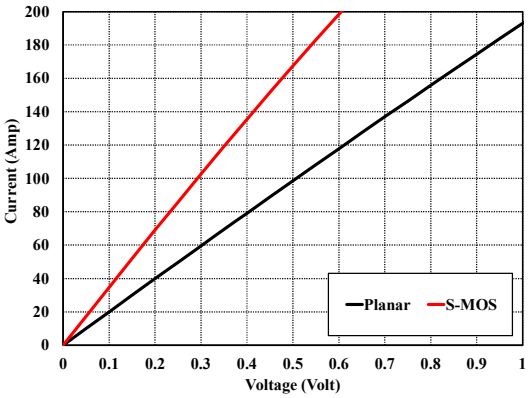

Fig. 18. 1200V SiC MOSFET IV output characteristics at 425K.

CONCLUSIONS

A new S-MOS cell concept was presented showing an alternative method to define and control the channel width in MOS based devices. The new approach can lead to simple manufacturing processes and improved overall performance. 3D simulation results confirm the

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functionality of the S-MOS concept for a 150V power MOSFET compared to standard planar and trench devices. An outlook towards the implementation of the S-MOS platform for silicon IGBTs and Silicon Carbide MOSFETs was also provided.

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