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Parylene as Coating for Power Semiconductor Devices

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Abstract

The introduction of wide band gap semiconductor devices leads to smaller package sizes, higher power densities and higher switching frequencies, which is advantageous compared to the power electronics based on the conventional silicon devices. However, due to the small insulation distances and the limited temperature range of available package materials, it is not possible to exploit these advantages completely. In this study, the properties of Parylene coatings as passivation layers in power semiconductor devices is investigated. The material would be particularly advantageous for double-side cooled power modules because it can fill the small gaps between different conductive layers, which is not possible with conventional packaging technologies. Parylene is promising to provide an excellent insulation performance even in these areas and exhibits a good temperature stability. Furthermore, this polymer acts as a barrier for humidity, dirt and corrosive gasses. Two types of Parylene were tested using the High-Voltage, High Humidity, High Temperature Reverse Bias (HV-H³TRB) test on substrate level and the better Parylene type also on automotive three-phase modules. The results are encouraging, although the performance strongly depends on the Parylene type and although a sensitivity to the respecive surface condition to be coated became apparent.

Keywords: Parylene, Coating, Encapsulation, Packaging, Power Electronics, Double-sided cooling, Power Module, Environmental Stress, Humidity Testing, THB, H³TRB, HV-H³TRB, Reliability.

INTRODUCTION

Replacing the conventional silicon (Si) by wide band gap (WBG) power semiconductor devices is particularly useful in applications asking for high power densities (e.g. SiC in electric vehicles) and high switching frequencies (e.g. GaN in inductive charging). But the advantages of WBG over silicon cannot be fully exploited yet due to the limitations imposed by the device packaging. Available packaging materials are limiting the maximum usable temperature range considerably and, in this way, retarding rapid market acceptance [1, 2]. In general, there are two basic trends to increase the temperature performance. One approach is to improve the temperature ratings of the plastics and composites applied next to the semiconductor chips. However, the mechanical characteristics tend to deteriorate with maximum allowed temperature and compromise the devices' integrity.

Another approach is maximising the cooling by adapting the double-side cooling principle [2–5]. However, this requires a coating, which is able to enter the smallest crevices, like Parylene does, which is also used for medical instruments and implants [6–9]. Figure 1 shows a simplified structure of such a double-side cooled module. Each substrate consists of two copper layers (a) with a ceramic insulation (b) placed in between. The die (c) is connected to the copper layers of the substrates via the die attach on both sides (d).

However, miniaturised power electronics structures become more and more challenging in terms of insulation requirements. The gaps (e) in between the two substrates have to be filled entirely to avoid partial discharges or even sparkovers. In conventional silicon power device packaging, silicone gel is the agent of choice acting as surface insulation. Unfortunately, silicone cannot be applied in this case due to its relatively high viscosity. The material just does not fill out the space properly in standard processing.

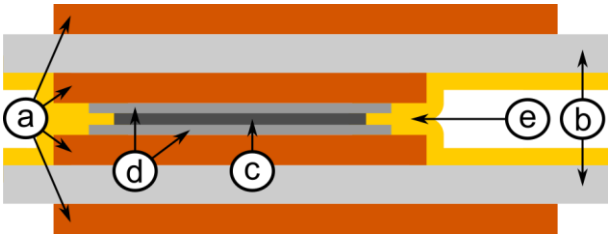

Fig. 1. Double-side cooled power module cf. [4]

In contrast, Parylene coatings provide excellent insulation properties [10] and the deposition process allows to fill the tightest gaps. Furthermore, a protective layer against dirt, humidity and corrosive gasses is provided [11]. As the diverse Parylene types offer these benefits to a different degree, two types were investigated in this work. Coated substrate samples were produced and tested under High Voltage, High Humidity, High Temperature Reverse Bias (HV-H³TRB) conditions.

Based on the results from the basic test, automotive three-phase modules, coated with the most performant Parylene variant were tested in HV-H³TRB, too.

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TEST SET-UP

Based on the power module structure in figure 1, test samples were produced consisting of only an Active Metal Brazing (AMB) substrate and bond interconnects. The substrates have a size of 20 mm × 20 mm. The top-side structure consists of two copper areas with a gap of 1 mm in between, as shown in figure 2. Both areas were connected with bond wires to establish an electrical connection. Each sample is coated with Parylene. In this study, two different Parylene types were used. Parylene 1 has a maximum temperature, which is similar to silicone gel, while Parylene 2 can withstand significantly higher temperatures. The processing steps are the same for both types, but the chemical structure is different.

Prior to the Parylene deposition, an advanced cleaning process is needed to ensure a proper adhesion of the polymer on the substrate, which is a crucial factor to improve humidity robustness. The preconditioning of the surface was performed using a wet chemical cleaning process. The Fourier-Transform Infrared (FTIR) spectroscopy results, obtained with the FTIR microscope Bruker LUMOS, show the differences before and after the wet chemical treatment of the copper AMB substrates. A significant reduction of organic contaminations on the substrate surface could be verified by FTIR spectroscopy results shown in figure 3.

After the cleaning process, the samples were coated at an evaporation temperature between 100 and 150 °C and a deposition pressure below 10 Pa.

Seven samples of each test group were mounted on a PTFE test board and six of them were connected in parallel to increase the number of samples in the test. The seventh sample remains without any electrical connection and acts as a chamber reference. Figure 4 shows an overview sketch of these test boards.

The HV-H³TRB test was performed to evaluate the performance of the two Parylene types. The samples were exposed to the climate conditions of 85 °C and 85 % relative humidity for at least 3 h to reach a climatic equilibrium. Then, the test voltage of 1000 V was applied for the entire duration of the respective test cycle. If one of the samples connected in parallel carried a too high leakage current, the measurement channel for the whole test group was switched off automatically. After the cycle time elapsed, the voltage was switched off and the drying period started for at least 3 h at 50 °C and 10 % relative humidity. After each cycle, failed samples were removed from the board. Then, the next cycle continued including the remaining samples only. Figure 5 shows the test procedure for each cycle in detail.

(a) (b) (c)

Fig. 2. Samples: (a) before HV-H³TRB, (b) after HV-H³TRB without bias (slight discolouration), (c) catastrophic failure during HV-H³TRB

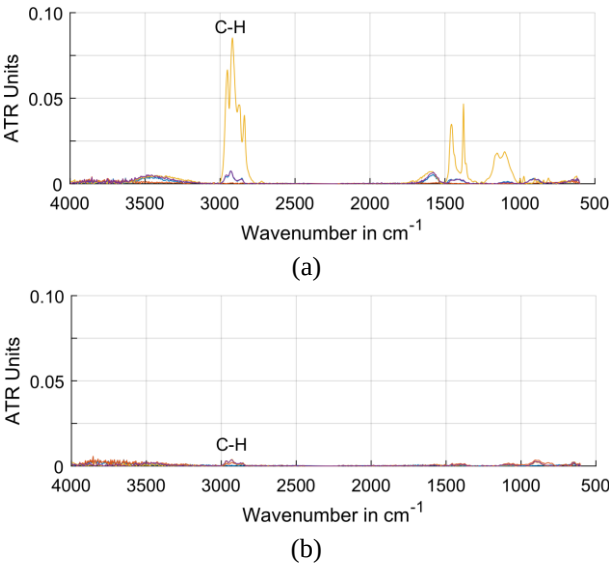

Fig. 3. FTIR results before (a) and after (b) the wet cleaning process at various positions

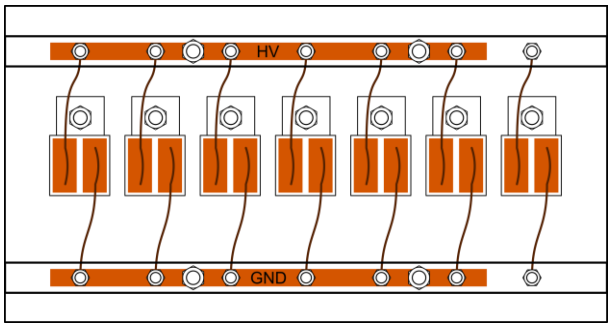

Fig. 4. Test board with six DUTs and an unbiased chamber reference (on the right).

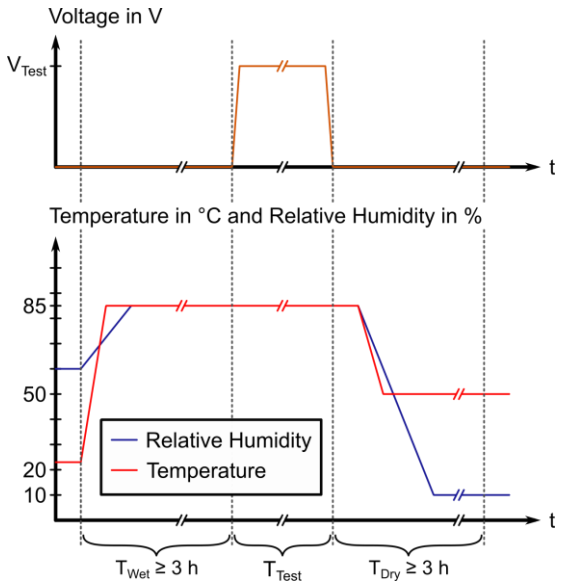

Fig. 5. Test procedure per cycle

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RESULTS AND ANALYSIS

Due to the rather large number of samples per test split, the HV-H³TRB test on the substrate samples allows a statistical evaluation. The Weibull plot in figure 6 reveals the differences between the two Parylene types and the impact of the cleaning process. The most obvious result is the much tighter distributions, which the Parylene 1 splits exhibit. As shown in table 1, the lifetime (scale parameter) of Parylene 1 is also significantly higher compared to Parylene 2. While the impact of the cleaning process is negligible for Parylene 2, it leads to a significantly higher performance for Parylene 1. The shape factor for Parylene 2 is below one, indicating early failures. In contrast, the shape parameter is significantly higher than one for Parylene 1, pointing out that the failures are due to wear-out.

During the HV-H³TRB, the failures were detected by an increase of the leakage current. All failures (cf. figure 2 (c)), come along with burn marks between both electrode pads. Further analysis of the failed test objects revealed a dendritic growth below the Parylene layer, which finally leads to a short circuit between the two electrodes. Figure 7 shows a dendritic structure on the left side and a catastrophic failure on the right side. The growth of the dendrite starts at the electrode with the applied high potential (anode) and propagates towards the low or ground potential. The underlying electrochemical process is called “Anodic Migration Phenomenon” (AMP) and is described in [12, 13]. Consequently, migration products under the Parylene coating could be observed in the area of the anode (figure 8).

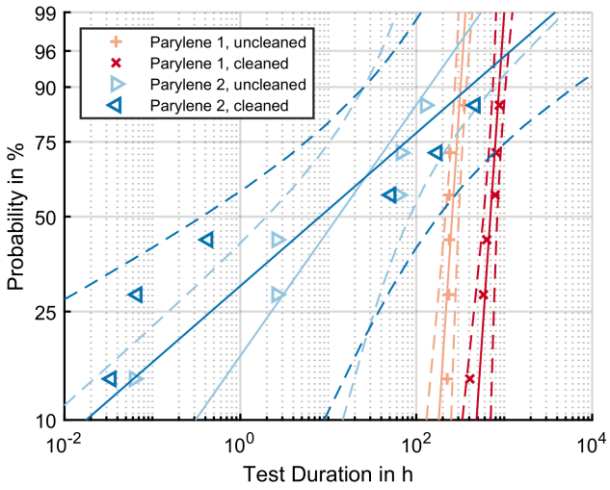

Fig. 6. Weibull plots of the substrate test campaign

Tab. 1 Weibull parameters for each test group

Name	Scale in h	Shape
Parylene 1, uncleaned	273	5.4
Parylene 1, cleaned	764	8.5
Parylene 2, uncleaned	26.6	0.5
Parylene 2, cleaned	26.5	0.3

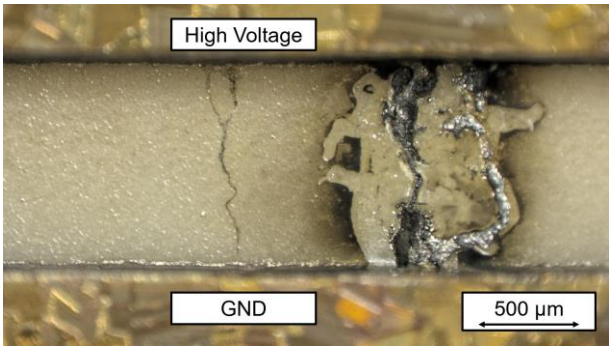

Fig. 7. Dendritic growth between the electrodes

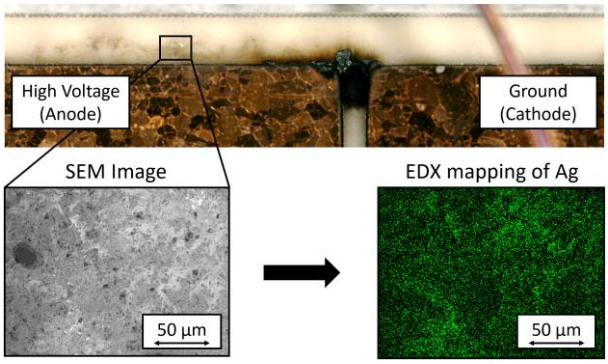

Fig. 8. EDX analysis of AMP residues

Since the copper area on the backside of the substrate is not connected, a capacitive voltage divider leads to a third potential in this test structure. The migration products of the AMP process can be observed on the edges of the substrate of the anode. The Parylene coating has been removed for the EDX analysis. The mapping of silver, as shown in figure 8, proves the migration products to be a chemical compound of silver, which originates from the AMB substrate.

One crucial factor during the AMP process is the delamination of the Parylene polymer from the surface. Using the Iodine Vapour Test (IVT) [14, 15], defects in the Parylene coating as well as adhesion weaknesses and delamination can be revealed optically. Delaminations as shown in figure 9, are visible after 4 h IVT at 80 °C. Mechanical stress, imposed e.g. by bent copper bond wires (see figure 9, left side) led to cracks and delamination. However, the delamination in this place is not a relevant failure mechanism. More important is the delamination visualised by the Iodine entrapped between the ceramic substrate and the Parylene layer. During the HV-H³TRB test, the delamination in this area leads to early failures due to the accumulation of water in the gaps and a faster degradation.

Fig. 9. Iodine Vapour Test results after 4 h at 80 °C

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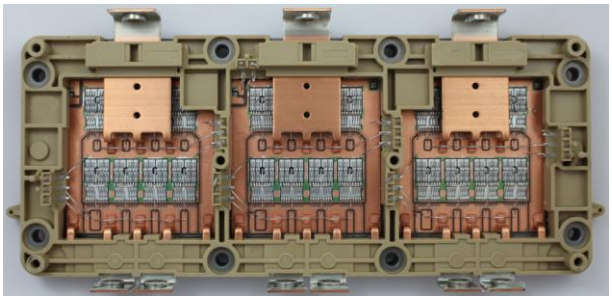

Fig. 10. 450 V three-phase automotive module coated with Parylene

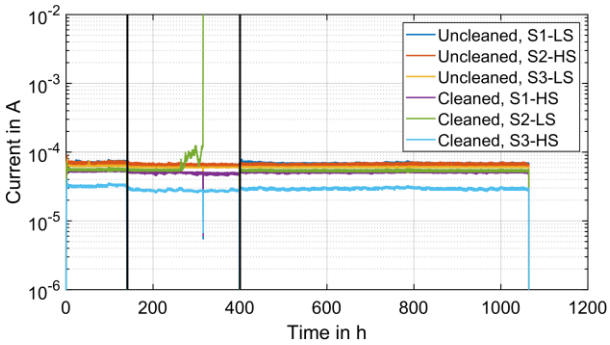

Fig. 11. Leakage logging during H³TRB Test of 450 V power modules at 85 °C, 85 % relative humidity and a test voltage of 405 V

CONFIRMATION ON POWER MODULE LEVEL

Based on the results of the substrate test, the Parylene 1 was selected to be tested on power modules for automotive applications. In this test, two three-phase modules were used. Each module consists of three half bridge systems and each half bridge has a high-side switch and a low-side switch. Every switch includes four IGBT chips and four diode chips. While one module remained uncleaned, the other module had been treated with the wet cleaning process. Both modules were coated with Parylene 1. Figure 10 shows a coated module before HV-H³TRB test. The voltage rating for these power modules is 450 V, although the chip voltage rating is higher. An HV-H³TRB test was carried out at 85 °C, 85 % relative humidity and 405 V, which is 90 % of the modules' voltage rating. The test duration was set to 1000 h according to AQG 324 [16].

Figure 11 shows the logging of the leakage currents of the respective switches under test. After 140 h and after 400 h the test was interrupted for intermediate measurements. During the whole test, only one semiconductor chip failed after 315 h in system 2, high side of the cleaned module. At the intermediate measurement after 400 h this DUT was inspected optically and the failed semiconductor has been disconnected from the other parts of the system. The blocking capability of the system regained the initial level. The same system was tested for the remaining test duration. The root cause of this failure is suspected to be an extrinsic defect, possibly due to processing the modules at different sites. No more failures occurred during the test of 1000 h.
The reason for the longer lifetime of the modules compared to the substrate samples is the much higher stress induced by the higher test voltage applied to the substrate samples.

SUMMARY AND OUTLOOK

In a first step, simplified structures of two copper pads with a distance of 1 mm on a ceramic substrate were produced and tested in HV-H³TRB. Each sample was coated with a layer of one of the two Parylene variants investigated. Some of the samples had been cleaned before the coating. During the HV-H³TRB test, the samples were exposed to 85 °C, 85 % relative humidity and 1000 V. Parylene 1 is clearly superior, showing a consistent wear-out behaviour, and cleaning the substrate before the coating increases its capability even further. The failure analysis indicated that the adhesion of the Parylene layer had been a crucial factor. Parylene 2 leads to an early-failure characteristic, with some very early failures due to delamination.
The superior Parylene 1 was then selected for a test on automotive power modules. In this second step of the investigation, two three-phase modules were tested in HV-H³TRB at 85 °C, 85 % relative humidity and 405 V for 1000 h. The three phases of the module were tested individually. There was one early failure, possibly due to an extrinsic root cause. Apart from that, the modules were completely stable.
These two experiments show that from a humidity capability point of view Parylene is indeed suited for standard power modules. The next step will be more challenging structures, e.g. required for double-side cooling, power cycling and thermal cycling experiments.

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