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Experimental Comparison of a New SAG-IGBT and Conventional DAG-IGBT Structures with LTO Design in terms of Turn-on Performance

S. T. Kong and L.Ngwendson
R&D Department Dynex Semiconductor Ltd.
Lincoln, LN6 3LF, UK

Abstract

In this paper, we compare a new Single Active Gate Trench IGBT(SAG-IGBT) with the conventional Double Active Trench Gate IGBT (DAG-IGBT) structures with the LTO (LOCOS Trench Oxide) technology. Both structures have been fabricated with the same design rules and process platform and test chips compared in terms of their Eon performance. The new proposed SAG-IGBT is created by connected one of the active trench to emitter potential which effectively halves the gate capacitance C_{GE} and C_{GD}. It is also shown that the proposed SAG-IGBT can achieve a further 50% reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% for identical Vce(on), with no degradation in the SCSOA.

Keywords: IGBTs, Trench, LOCOS

INTRODUCTION

Nowadays, IGBT devices are key components in power conversion circuitry and primarily used in electric power and energy systems[1-3]. The new generation of IGBT devices are based on a significant increased cell density in conjunction with striped trench gate structures[4-5]. The paralleled trench cell layout consists of active and passive/dummy trenches, which enable smaller cell pitches as well as high controllability of turn-on dI/dt. This cell design allows higher carrier storage at the emitter side, which leads to a significant increase in conductivity modulation in the drift region. At present, improving operational efficiencies and reducing switching losses are the fundamental concerns for engineers using these devices. Moreover, it is also a design challenge to achieve lower E_{ON} due to the presence of significant capacitances (C_{GC} + C_{GE}) leading to high gate charge (Q_G).

The LOCOS Trench Oxide IGBT (LTO-IGBT) (Fig.1a) was presented in ISPSD and PCIM 2019 and shown to achieve 30% Q_G and C_{GC} (C_{RES}) enabling 25% increased current density with competitive E_{ON} and E_{OFF} performance [6-8]. This device is known as the DAGIGBT in this work. The new proposed SAG-IGBT is created by connected one of the active trench to emitter potential which effectively halves the gate capacitance C_{GE}. In this paper, we show that the proposed SAG -IGBT can achieve a further 50% reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% for identical Vce(on), with no degradation in the SCSOA and RBSOA. In summary, lower capacitances, lower gate charge and reduced E_{ON} makes the SAG device structure a very strong candidate for more efficient high voltage trench IGBT designs as well as low voltage devices for automotive applications and other low loss power systems [1-3].

THE SAG/DAG STRUCTURES and DESIGNS

In the proposed SAG-IGBT design, one of the active trenches is connected to ground or emitter metallization by the contact mask as shown in Fig.1b. Other contact schems can also be used in the third dimension. For the same cell pitch, decreasing the number of active trenches within the SAG-IGBT device reduces the conductivity modulation. This is because of reduced MOS channel density for the same device active area. As a consequence, fewer electrons are injected per unit area causing a reduction base current of the PNP transistor hence lower saturation current and Vce(sat) due to lower conductivity modulation.

So a major challenges to solve with the SAG-IGBT device design where only one effective active trench is used, is to achieve identical MOS channel density in

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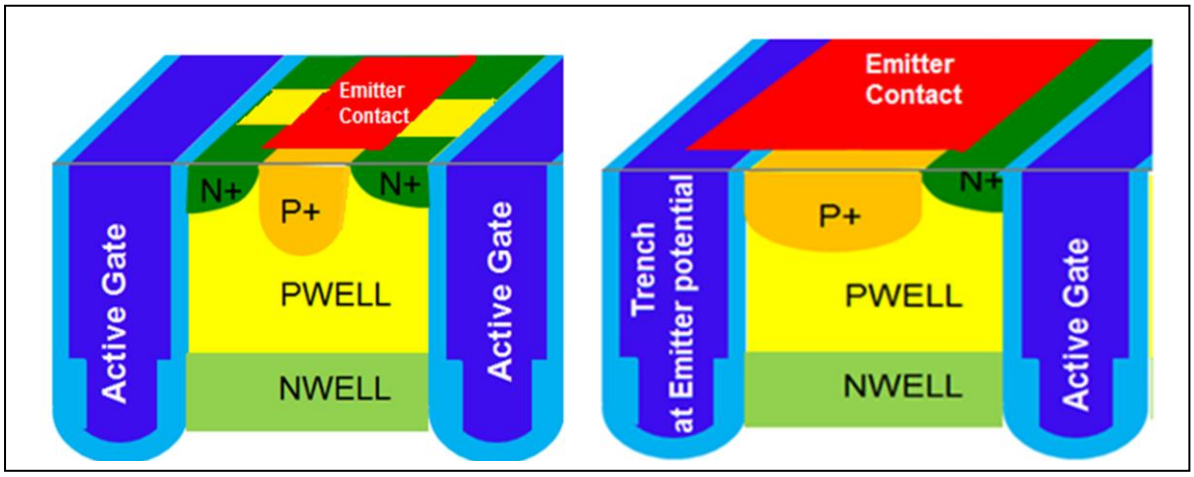

Fig. 1: The simplified top cell schematic of (a) DAG (Double Active Gate) structure with segmented N+/P in the emitter area (b) The SAG (Single-Active Gate) structure with continuous N+ along the single active gate trech

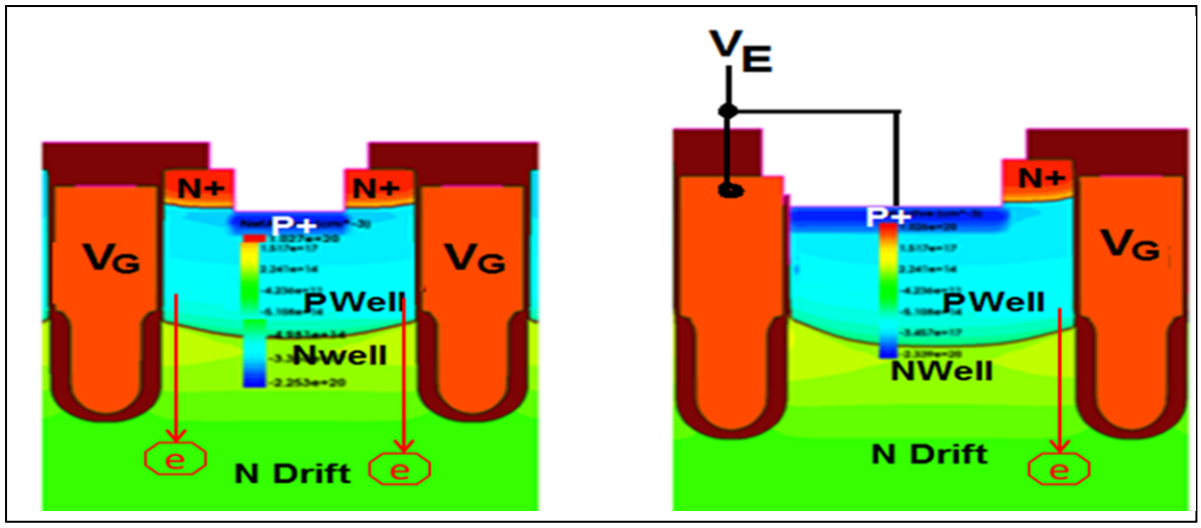

Fig. 2: Top cell of the simulated IGBT structures (a) DAG and (b) SAG device (only one trench is used for MOS channel conduction)

order to maintain Vce(sat), saturation current (I_{SAT}) and short-circuit current (I_{SC}). For identical Nwell(carrier stop layer) and threshold valtage Vth, two approaches are available: (i) reduce the cell pitch /width or (ii) increase emitter N+ area over the active gate trench. The later approach is used in this work which means the SAG device has continuous N+ along the active trench as shown in Fig.1b compared with segmented N+/P+ in the conventional DAG-IGBT device.

SIMULATION & EXPERIMENTAL RESULTS

As a first step, the design parameters of SAG-IGBT and conventional DAG-IGBT using the LOCOS Trench Oxide process [4-5] were studied numerically using Synopsys TCAD Simulator. Fig.2 shows the top cell of the two simulated device structures. These two structures were investigated using calibrated models in Synopsys TCAD tools. In 2D-simulation, the cell pitch/width of SAG-IGBT device is about a half-size of DAG-IGBT device. However, the effect of hole current on the channel inversion in DAG-IGBT/SAG-IGBT devices have also been considered but the study was limited to a 2D device model [9].

Fig.3 shows the simulated Q_G charateristics for DAG and SAG 6.5kV rated IGBT devices with the same simulation conditions. It is shown that the SAG-IGBT device can achieve at least 50% lower total gate charge Q_G and miller charge Q_{GC}. $V_{GE,TH}$ ($\sim 6V$) was matched in the both simulations. Lower miller charge and total gate charge improves the total switching losses (E_{ON} + E_{OFF}) of the device hence switching frequency and speed can be increased.

The simulation results comparing the input capacitance (C_{iss}), and reverse transfer capacitance (C_{res}) are shown in Fig.4. The simulation condition of the AC frequency was 100 kHz. It can be seen that the SAG device (black trace) has a 50% reduction in C_{iss} and C_{res} compared with the DAG device (red trace).

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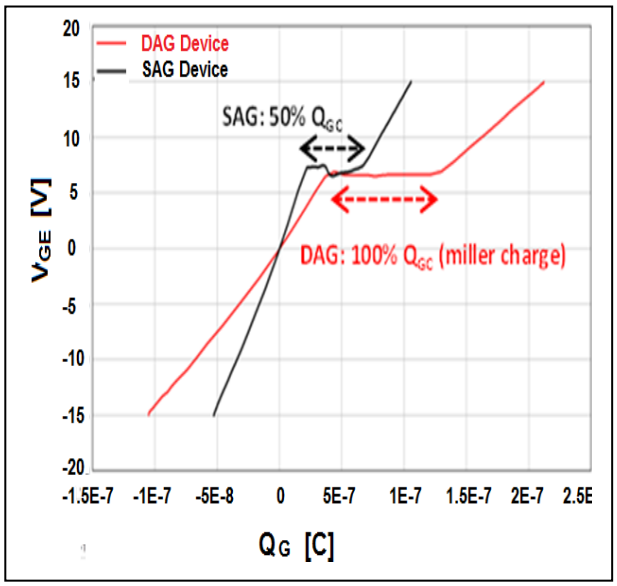

Fig. 3: Simulated gate charge (Q_G) for DAG and SAG 6.5kV rated IGBT devices [Vce=3.6kV, Ice=168A, Tj=25°C]

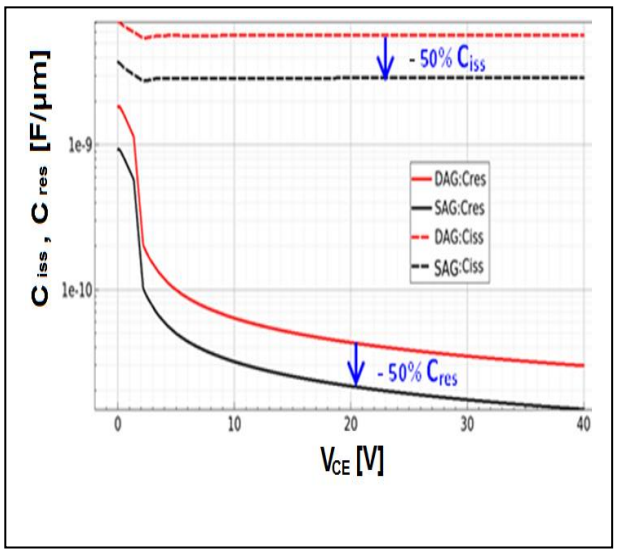

Fig. 4: Simulated C_{iss} and C_{res} of DAG and SAG devices for 6.5kV rated IGBT devices [Vge=0V, f=100 kHz, Tj=25°C]

Optimized engineering samples of both the SAG and DAG devices have been fabricated in silicon and electrical results are presented in this work. The SAG and DAG-IGBT devices are fabricated using the similar processes andthe chip size of 13.5mm x 13.5mm has been used

Fig.5 shows the image of the ceramic substrate, containing a parallel arrangement of 4 x IGBTs and 2x FRDs (Freewheeling Diodes) for testing. Each IGBT is a 6.5kV/42A rated SAG-LTO or DAG-LTO IGBT device which means total current per substrate is 168A.

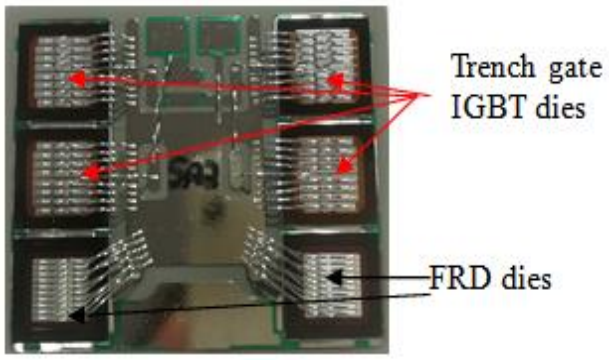

Fig.5: Image of a ceramic substrate, containing 4x trench gate IGBTs and 2x FRDs [rated voltage/current =6.5kV/168A]

Fig.6 shows the short-circuit Ice and Vce waveforms of SAG and DAG-IGBT at 125°C. It can be seen that both devices have a similar short circuit current level (i.e. Isc ~600A) due to matched MOS channel density a shown in fig.1. Therefore, the transconductance is also matched and we can compare E_{ON} and dI/dt of both structures using similar R_{GON} values.

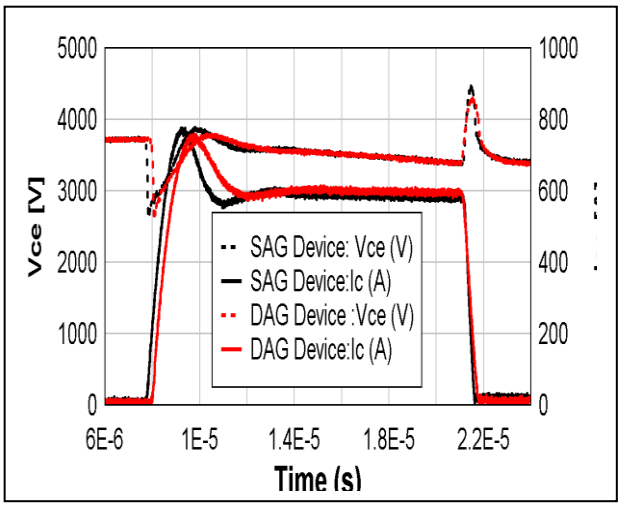

Fig. 6: Typical short circuit test Ice and Vce waveforms for 6.5kV DAG and SAG IGBT substrates. V_{CE}=3.6kV, T_J=125°C, V_{GE}=±15V. It can be seen that I_{SC} is well matched due to identical MOS channel density

Fig.7 shows the turn-on waveforms of SAG and DAG devices for identical R_{GON}/R_{GOFF} (16Ω/33Ω) values at T_J=125°C. It can be seen that reduced capacitance in the SAG structure especially C_{RES} results is faster turn-on in terms of shorter V_{CE} tail during turn-on which results in lower E_{ON}. In addition, reduced gate capacitance in the SAG structure results in small T_{don} values as shown in Fig.8.

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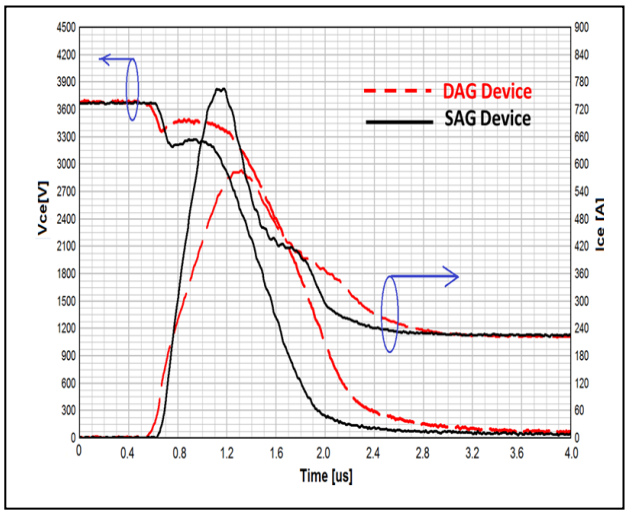

Fig. 7: Typical turn-on I_{CE} and V_{CE} waveforms for SAG and DAG 6.5kV IGBT devices for identical $R_{GON}/R_{G,OFF}$. [V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

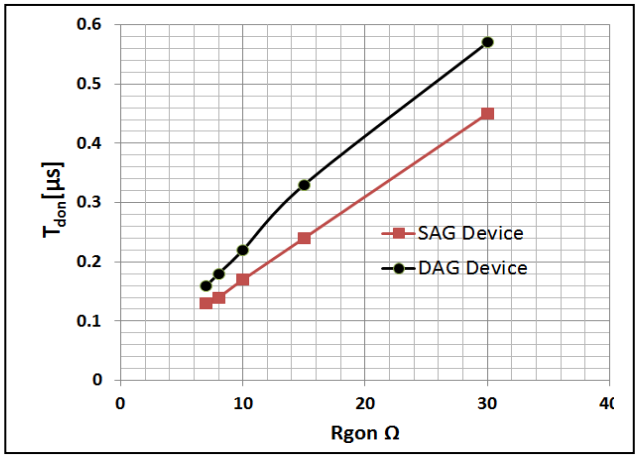

Fig.8: Typical influence of R_{GON} on Td_{on} for SAG and DAG 6.5kV IGBTs. [V_{CE}=3.6kV, I_{CE}~168A, T_J=125°C, V_{GE}=±15V]

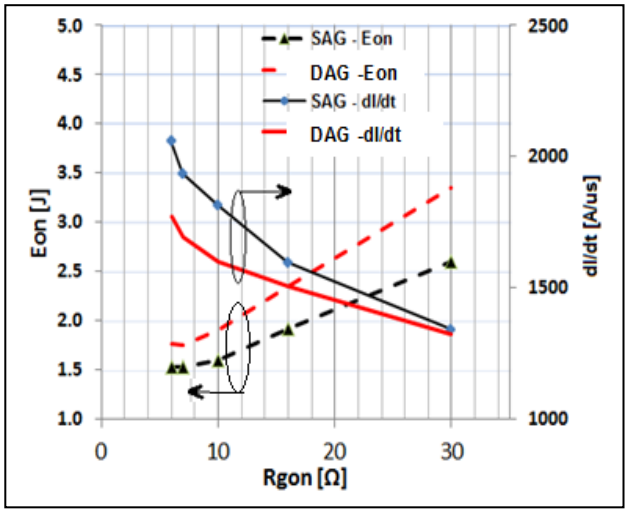

Fig. 9: Influence of R_{GON} on turn-on dI/dt for SAG and DAG 6.5kV IGBTs[V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

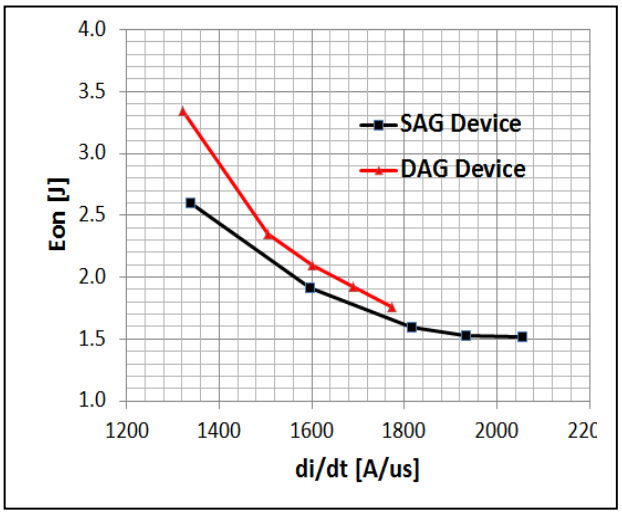

Fig. 10: Influence of turn-on dI/dt on E_{ON} for SAG and DAG 6.5kV IGBTs V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

Fig. 9 shows the influence of R_{GON} on Eon and dI/dt where it can be seen that both devices show good response to changing R_{GON}. In addition it can be seen that higher dI/dt and lower Eon is possible with SAG-IGBT compared to DAG-IGBT structure, for identical R_{GON}. Fig.10 shows that the SAG device structure can lower Eon by up to 25%. However, beyond dI/dt > 1600 A/µs the E_{ON} benefit of the SAG device becomes much less.

SWITCHING LOSSES COMPARISON OF SAG/DAG DEVICES

The benefit of this work can be summarized through Fig. 11, which shows the switching losses(E_{ON} + E_{OFF}) comparison of SAG and DAG devices under the same Vce(on) and dI/dt($\sim 1600 A/\mu s$) .

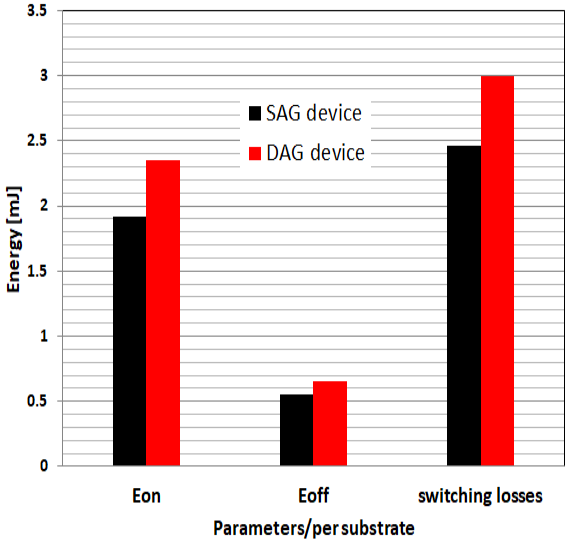

Fig. 11: Switching losses comparison of SAG and DAG devices under the same Vce(on) and dI/dt($\sim 1600 A/\mu s$)

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The E_{OFF} performance of IGBT is a function of (i) the turn-off speed of the gate (increases with C_{GE}) which determines turn-off dI/dt, (ii) V_{CE} rise or dV/dt (how fast the depletion moves towards the collector side) which is determined by the plasma density and (iii), the tail current which is determined by carrier lifetime and silicon thickness (hence device rating).

The SAG device shows the 11% lower E_{OFF} than DAG with the same Vce(on) value. For identical Vce(on), the SAG design will speed up only (i) above hence the influence on E_{OFF} is relatively small compared to Eon.

CONCLUSION

In this work we have shown simulation and experimental results comparing 6.5kV SAG and DAG IGBT device concepts using the LOCOS IGBT Trench structures. The LOCOS IGBT concept has been previously shown to reduce Q_G. Herein, it has been shown that the SAG-IGBT concept can achieve a further reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% and Eoff by 11%, for identical Vce(on) and dI/dt, with no degradation in the SCSOA.

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Addresses of the authors

S.T. Kong, 28, Tiber Road, Lincoln, UK, LN6 9TY, Chris.kong@dynexsemi.com

L. Ngwendson, Luther.Ngwendson@dynexsemi.com