DOI: https://doi.org/10.14311/ISPS.2021.012

TCAD Simulation of the Bipolar Degradation in SiC MOSFET Power Devices

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Abstract

Reliability and performance of SiC high power devices are still limited by inherent SiC material defects despite tremendous progress made to reduce the density of these defects. The bipolar degradation remains a major challenge for developing high voltage SiC power devices. It is mainly due to the presence of Shockley-type stacking sequence faults (SFs) within the hexagonal SiC structure lattice, creating 3C-like SiC regions embedded within the main 4H-SiC structure. In this paper, we present a two dimensional numerical model of 4H-SiC power MOSFET device in which the drift region of the device is formed by a 4H-3C-4H heterojunction to account for the bipolar degradation. TCAD simulation results showed that the 3C- nano-layer creates a high resistive layer, effectively preventing the current flows across it, hence reducing the total active area of the device.

Keywords: Bipolar degradation, stacking faults, heterojunction, 3C- SiC.

INTRODUCTION

Reliability assessment of SiC power devices rely on a wide range of tests that have been developed and established during more than 30 years of experience on power packages with implemented Si device technology [1]. These tests are mostly performed to assess the chip quality such as High Temperature Reverse bias (HTRB) and High Temperature Gate bias (HTGB) stress tests, to assess the stability of the package in specified operating conditions and under external and internal temperature swings such as power cycling tests, and to assess the mechanical integrity of the package such as vibration tests. However, additional reliability tests have been specifically developed to account for SiC materials defects that direct impact the performance of power devices.

SiC material defects are broadly classified into two groups and they differently affect power devices performances: point defects and extended defects. The former are identified as a major carrier lifetime killer while the latter lead to excessive leakage current and significantly decrease the breakdown voltage of power devices if they include carrot/comet defects or triangular defects for instance [2]. On the other hand, basal plane defects, which are classified as extended defects, trigger the so-called bipolar degradation and are considered as the major defects hindering the commercial development of high power discrete devices rated above 1.7kV despite tremendous technological progresses achieved in SiC power devices fabrication and epitaxial growth to reduce these defects.

The bipolar degradation phenomenon has been observed for the first time during the research and development of SiC PiN diodes in the early 2000s [3]. Extensive experimental results have been published to explain this degradation mechanism in power devices operating in bipolar mode as PiN diodes, IGBTs and BJTs as well in unipolar SiC MOSFET power devices which are similarly affected by such degradation if their inherent body diode, working as a bipolar device, is intentionally or accidentally turned on [4, 5]. It has been reported that basal plane defects easily glide under stress because the critical resolved sheer stress is relatively low in SiC, leading to the formation of Shockley-type stacking sequence faults within the hexagonal SiC structure lattice and creating 3C-SiC- regions embedded within the main 4H-SiC structure [6-9]. In term of electrical parameters, the bipolar degradation manifests itself as the increase of the forward voltage of the power device due to poor conductivity modulation in the affected regions occupied by the SFs.

The motivation of this work is to understand the correlation between these bipolar degradations and the change of SiC MOSFET power devices characteristics through simulation models. Several papers have been published on SiC MOSFETs modelling methods that are mainly categorized as behavioural models, semiphysics models, physics-based models, seminumerical models or numerical models [10]. In this paper, 2-D device simulation models have been developed to investigate the bipolar degradation in SiC MOSFET. The paper is

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organized as follows: section II presents a review of the bipolar degradation mechanism and explain how the defect is modelled within a 4H-SiC structure. In section III, the implementation of the power device in Silvaco-Atlas TCAD software is detailed and the main results are presented in section IV. A conclusion is given at the end of the paper.

REVIEW OF BIPOLAR DEGRADATION

Formation of partial dislocations

The cubic and hexagonal SiC structures known as 3C- and 4H- 6H- SiC are at present the main structures used for developing high power devices. However, deviation from their respective perfect stacking sequences is quite common during epitaxial growth processes as basal plane defects easily glide under stress because the critical resolved shear stress is relatively low in SiC at high temperature [2]. As a consequence, this deviation has been identified to create regions within the main structure that have the perfect stacking sequence of another polytype [6]. The structure is said to have stacking faults (SF) areas located between two partial dislocations (PD), namely the C-core and Si-core dislocation in which the latter is set into motion most likely due to electron-hole recombination enhanced dislocation glide (REDG) during the forward current conduction of bipolar devices as exemplified in figure 1 for the case of a 4H-SiC PiN diode.

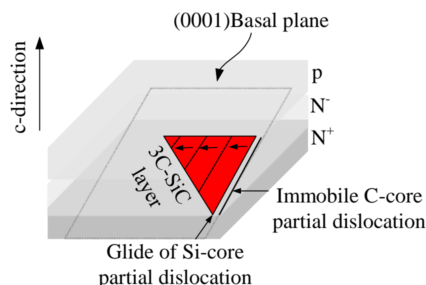

Figure 1. Schematic representation of Shockley stacking faults expansion within a *n-type* 4H-SiC PiN diode. A 3C-SiC layer area within the drift region is created by the glide of the Si-core partial dislocation while the C-core partial dislocation does not move.

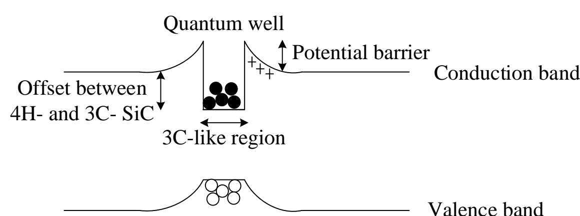

Figure 2. Conduction energy band split-off highlighting the inclusion of a 0.75nm 3C-SiC nano-layer into the 4H-SiC hexagonal structure which gives rise to a thin electron-attractive quantum well and creates a built-in potential barrier at both sides of the quantum well similar to a PN junction.

Electronic properties of SFs

The specification of the stacking patterns around stacking faults depend on the SiC polytype. We consider hereafter Shockley-type single SFs that are introduced by partial dislocations glide in the (0001) basal plane and are responsible for the so-called bipolar degradation in 4H-SiC power devices. In such structure, SFs in the neighbouring (0001) planes give rise to 3C-like cubic inclusion, i.e., a layer having a straight 3C-like stacking sequence [6]. Such structure's arrangement forms two heterojunctions of the type 4H-3C-4H SiC as schematically exemplified in figure 2. Experimental studies on *n-type* 4H-SiC samples, containing SFs regions, have indicated that this local thin planar 3C inclusion sequence is of the order of 0.75nm and lowers the conduction band by about 0.22eV - 0.31eV while the top of the valence band shows no such behaviour as illustrated in figure 2 [7]. For this reason, it was suggested that these SFs can be interpreted as a one-dimensional quantum well confinement effect with a strong electron localization in the c-direction (perpendicular to the (0001) basal plane, i.e., SF plane) [6-9]. Electrons trapped in the quantum well create a negative charge within the well and a positive charge within a depletion region from both sides of the well, until thermal equilibrium is established. As a consequence, a built-in electrostatic potential barrier appears in a similar way as in a PN junction. Under such condition, the overall energy properties of the 4H-SiC structure are fundamentally altered with the electron transport being practically obstructed in the c-direction whereas electrons are free to move in the SF plane [6].

MOSFET DEVICE MODELLING

To account for SFs effects in 4H-SiC MOSFET power devices, a thin 3C-SiC nano-layer is incorporated in the middle of the N^- drift layer of the device as shown in figure 3. Impact of such inclusion on the performance of the parasitic PiN body diode that initially triggers the bipolar degradation during the current conduction, and then the performance of the MOSFET in the first quadrant operation are examined using Silvaco-Atlas TCAD software.
The 2D cross-sectional view of the investigated 4H-SiC MOSFET structure is depicted in figure 3. Referring to literature data and design criteria for obtaining a threshold gate voltage between 4V and 6V [11], the doping and dimensions parameters are chosen as follows. A pitch cell of 8.5 μm has been considered throughout the analysis. The P^+ body region was designed with a thickness of 0.88 μm and an acceptor doping concentration of $1 \times 10^{17} cm^{-3}$. The N^+ source region was designed with a thickness of 0.32 μm and a donor doping

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concentration of $1x10^{19}$ cm^{-3}. The channel width was set to 1µm, and the thickness of the gate oxide was set to 50 nm giving an approximate threshold voltage of 5 V. The i-epilayer thickness was set to 12 µm to account for a breakdown voltage of 1.7kV. It was lightly doped with a uniform donor concentration profile of $1x10^{16}$ cm^{-3}. The N^- drain region was designed with a 2 µm thickness and a uniform doping concentration of $1x10^{19}$ cm^{-3}. A corrective factor was set within the algorithm to account for a MOSFET device with an approximate active area of $0.17cm^2$. It is worth noting that even though the design parameters may not be accurate with that of the commercial discrete power devices, it reflects the basic structure of the real device.

Note that the drain and the source electrodes were added to both sides of the structure. Shockley-type stacking faults regions are represented by the inclusion of a 3C-SiC nano-layer in the middle of the i-epilayer with a thickness of 0.75nm and a width varying between 25% and 100% of the total pitch cell width in order to get insights into the influence of the 3C-SiC inclusion on the carrier density and the I-V device characteristics. The simulated structure's parameters are summarized in Table I.

Material	Parameter	Value
	N^+ source doping concentration	1 x 10^{19} cm^{-3}
	P well doping concentration	1 x 10^{17} cm^{-3}
4H-SiC	N^- drift layer concentration	1 x 10^{16} cm^{-3}
	N^+ substrate doping concentration	1 x 10^{19} cm^{-3}
	Depth of N^+ source junction	0.32 µm
	Depth of P well junction	0.88 µm
	Thickness of the drift layer 12 µm	
SiO2	Thickness of the gate	50 nm
3C-SiC	Inclusive thickness layer 0.75 nm	

Table I. Summary of the simulated structure parameters

RESULTS AND DISCUSSION

Body diode degradation

The static I-V characteristics of the MOSFET body diode are depicted in figure 5 for different widths of the 3C-SiC nano-layer and at a temperature of 27°C and a gate voltage of -5V, assuring the MOSFET channel is fully pitched off (no synchronous rectification operation). Compared to the I-V characteristic of a healthy body diode, the maximum voltage shift ΔV_{max} due to the basal plane defect is estimated to be 0.7V at a current level of -3A. This represents the worst case scenario as it is assumed that the 3C- nano-layer, which is representative of the bipolar degradation, covers the whole width of the MOSFET pitch cell.

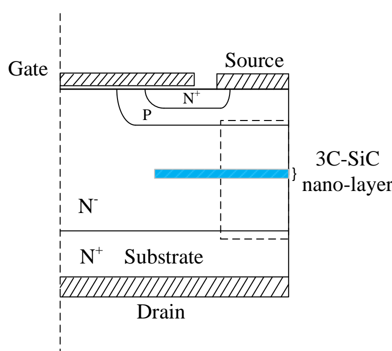

Figure 4. Cross-sectional view of the simulated 4H-SiC MOSFET power device with the inclusion of a 0.75nm 3C-SiC layer in the middle of the drift region.

However, the voltage shift does not drastically change with the 3C- nano layer width. This is due to the small active area the body diode occupies within the MOSFET pitch cell and hence it is suggested that SFs expansion will impact the performance of a MOSFET body diode at the early stage of the expansion.

In order to get insights into the behaviour of this drift configuration, the electrons and the holes carrier densities are presented in figure 6 at a voltage bias of -4V and a current of -3A. The electron/hole carrier densities within the defective 'i' region decrease when nearing the 3C-SiC nano-layer and a depletion layer of 0.1µm is formed at both sides of the 3C- layer. The density of the electrons is almost at its equilibrium value with a maximum excess carrier injection of only 1 x 10^{16} cm^{-3}. This is too low to assure high-level injection conditions. On the other hand, the minority carrier injection is approximately estimated to 4 x 10^{15} cm^{-3} which is still too low to assure the conductivity modulation effects necessary for PiN diodes to operate properly. The energy of the 4H-3C-4H- SiC structure at 27 °C is illustrated in figure 7. The energy gain due to the quantum well action of the 3C- nano-layer is estimated equal to $16mJ/m^2$ which exceeds the SFs energy formation γ of $14.7mJ/m^2$. This result is in accordance with the theoretical calculation obtained in [12] where it is predicted an energy gain of 15.5 mJ/m^2 with a doping concentration of 1 x 10^{16} cm^{-3} for the studied *n-type* 4H-SiC sample.

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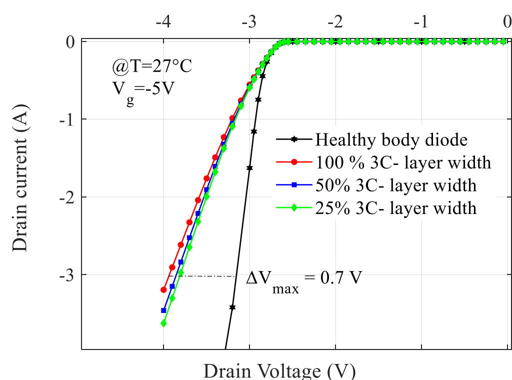

Figure 5. Static I-V characteristics of a healthy and a defective MOSFET body diodes where the width of the 3C-SiC nano-layer is varied between 25% and 100% of the total pitch cell width at a temperature of 27°C and a gate voltage of -5V.

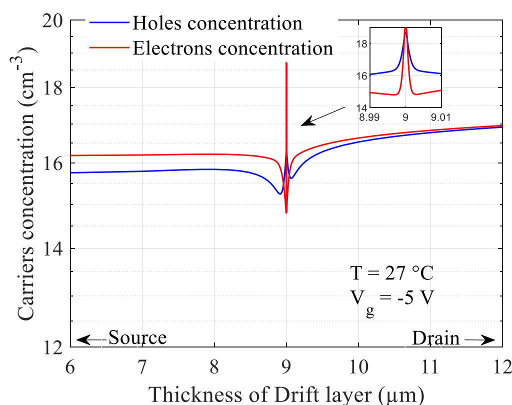

Figure 6. Defective MOSFET body diode Electrons/ holes carriers concentration. A depletion region is formed in the vicinity of the 3C-SiC nano-layer which causes the carriers concentration to lower.

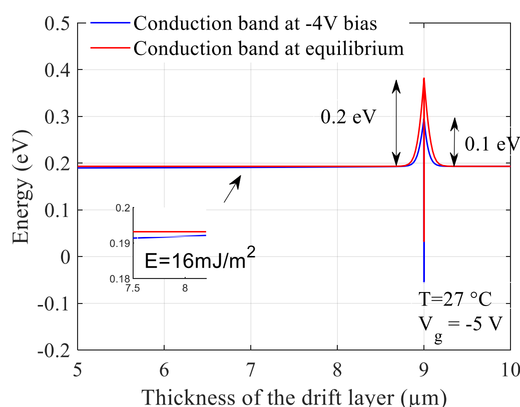

Figure 7. Defective MOSFET body diode energy at equilibrium (red) and at a bias voltage of -4V to illustrate the energy lowering due to the SFs. The energy formation is estimated equal to 16mJ/m^2.

MOSFET 1st quadrant operation

The unipolar MOSFET device operates under the majority carrier injection condition and as such, this mode of operation is not responsible for the expansion of the stacking faults (SFs). However, as previously mentioned, the voltage forward bias of the body diode triggers the basal plane dislocation glides, leading to the apparition of a 3C- polytype nano-layer within the 4H-SiC drift region. This obstructs as well the flow of the majority carriers.
Figure 8 shows the static I-V characteristics of the MOSFET operating in the 1st quadrant by varying the 3C-SiC layer width to cover 25%, 50% and 100% of the pitch cell, at a temperature of 27°C and a gate voltage of 20V. The voltage shift in this case is higher with a maximum voltage shift reaching 1 V at a current level of 4A. However, the size of the SFs had a more significant impact on the total active area of the device due to a larger depletion width appearing at both sides of the quantum well. At a voltage bias of 4V, the depletion width was estimated equal to 0.3 µm at 27°C, consuming space within the pitch cell and increasing the on-resistance by constricting the area through which the current can flow. The MOSFET on-resistance $R_{DS(on)}$ and its percentage variation with temperature are key performance indicators when considering the bipolar degradation and figure 9 illustrates the increase of the on-resistance of the simulated device at a temperature ranging from 300 K to 450 K. It is estimated an increase of 31% of the on-resistance at 300K. This suggests that the bipolar degradation is more detrimental to the operation of the MOSFET.

CONCLUSION

A two dimensional (2D) numerical model of a 4H-SiC power MOSFET device was build using Silvaco-Atlas simulator in order to gain insights into the performance degradation of the device when it is subject to a bipolar degradation due to the presence of stacking faults areas within the device. The defected area was represented by the inclusion of a 3C-layer in the middle of the drift layer of the device. This led to a heterojunction-like N^- region within the drift layer formed by a 4H-3C-4H- SiC arrangement. Regardless of the width of the 3C-SiC layer, it creates a high resistive area, preventing the current to flow through and hence reducing the total active area of the device. TCAD simulation results indicate that, during the operation of the MOSFET body diode, the electrons/holes carriers densities decrease within the vicinity of the 3C-SiC layer to a level that does not assure high level injection conditions for which the conductivity modulation is not possible. The forward voltage increase is due to the apparition of a depletion area at both sides of the 3C- nano-layer and is dependent on operating condition.

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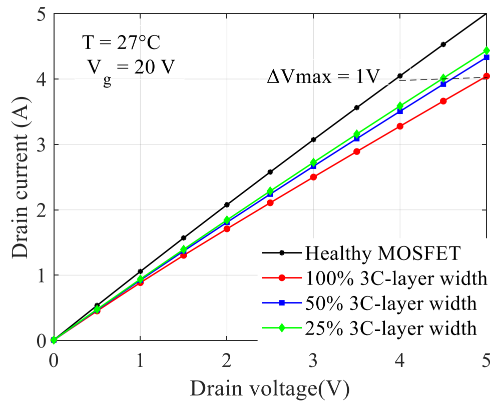

Fig 8. Static I-V characteristics of the MOSFET in the 1st quadrant obtained by varying the width of the 3C-SiC.

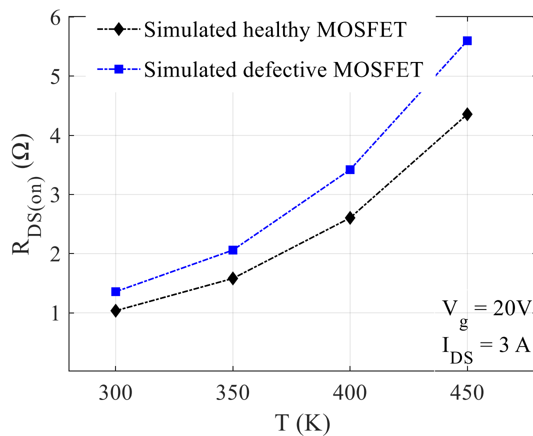

Figure 9. SiC MOSFET on-resistance variation in terms of the temperature. An increase of 31% is estimated at 300K.

Although the operation of the MOSFET in the 1st quadrant does not trigger any expansion of the stacking faults, it is still similarly affected by the presence of the 3C-SiC nano-layer.

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