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DEGRADATION OF POWER SIC MOSFET Under REPETITIVE UIS and SHORT CIRCUIT STRESS

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Abstract

This paper investigates the reliability of commercial planar and trench 1.2-kV 4H-SiC MOFSETs under repetitive unclamped inductive switching (UIS) and short circuit (SC) stresses. The degradation of device characteristics, including the transfer characteristics, drain leakage current Idss, and output characteristics, is observed. Repetitive SC stress was performed for 400 and 600 V bus voltages. Increased buss voltages during stress have higher impact on electrical performance of tested devices. The hot carriers injection and trapping into the gate oxide in the channel region may occur during the aging experiments and are believed to be responsible for the variation of electrical parameters.

Keywords: Reliability, degradation, SiC MOSFET, TrenchMOSFET, repetitive UIS, repetitive short circuit

INTRODUCTION

Silicon Carbide (SiC) power MOSFET fabrication technology has considerably matured over the recent years and therefore, they are now commercially available to buy in large quantities from various different manufacturers [1]. Because of their superior properties, SiC devices can be used for higher temperature, higher switching frequency, and higher power density applications [2-3]. Nevertheless, before they could completely replace silicon (Si) counterparts, robustness and reliability remain a main issue [3-4] for the devices under a number of extreme operational conditions, such as overcurrent, overtemperature, short circuit, and unclamped inductive switching (UIS) [5]. With trend of decreasing chip size for cost reduction purpose, the avalanche robustness and short circuit withstand capability became more critical, as they are strongly sensitive to the chip size design as the maximum energy density of the chip is fixed. In UIS test, the MOSFET is usually connected to an inductance without antiparallel free-wheeling diode to commutate the loop current when switching OFF the device. As a consequence of this, the device has to absorb all the energy previously stored in the inductance during the operation stage. The MOSFET, therefore, will be driven into the avalanche mode as long as the stored energy is sufficiently high, resulting in a gradual increase in the junction temperature of the device [6]. During avalanche operation at high currents, high concentrations of hot carriers are generated that may cause degradation of interfaces and insulation (oxide) layers.

Due to the smaller chip size and thinner gate oxide, the robustness of SiC MOSFETs regarding the SC condition is lower than their Si counterpart. When comparing Si IGBTs and SiC MOSFETs with similar current ratings, SiC MOSFETs have 5-10 times higher current density under short circuit conditions. Higher instantaneous power density and smaller thermal capacitance results in faster temperature rise and lower short circuit withstand time. Because an undesirable SC fault may occur in a variety of ways during the lifetime of the devices and at least 2 μs is needed for the commercial drivers to react. However, due to external effects and oscilations, SC event may occur many times during operational lifetime, therefore, the repetitive SC tests could reflect the impact of a single SC event and also provide more insights about the degradation process [7-8]. With the aid of repetitive SC tests, aging indicators can be explored comprehensively.

Therefore, this paper investigates the reliability of commercial 1.2-kV 4H-SiC MOFSETs under repetitive unclamped inductive switching (UIS) and short circuit (SC) stresses. The degradation of device characteristics, including the transfer characteristics, drain leakage current I_{dss}, and output characteristics, is observed.

EXPERIMENTAL SETUP

For all tests, two types of commercially available 1.2kV SiC MOSFET devices were used. The first samples were transistors with planar gate and on-resistance of 100mΩ. Second samples were devices with the trench gate

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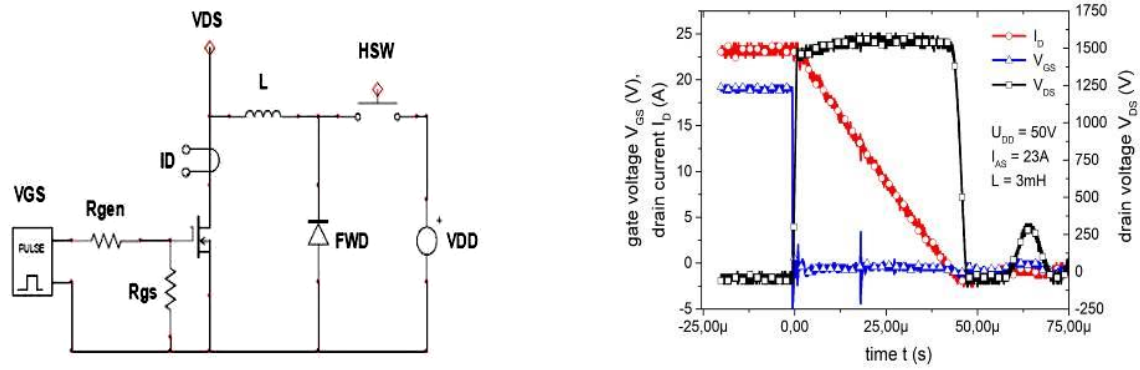


(a) (b)

Fig. 1a) Basic UIS test circuit. b) Typical current and voltage waveforms ***of*** *SiC MOSFET* under UIS test conditions.c) Typical current and voltage waveforms ***of*** *SiC MOSFET* under SC conditions

structure and 200 mΩ of on-resistance. Both devices were packaged in TO247. **UIS test** – Commercial UIS tester ITC55100 was used for UIS testing. The circuit diagram and typical voltage and current waveforms during the test for Si MOSFET are shown in Figure 1a-b. The device under test (DUT) is connected to the power supply through the inductor and high side switch HSW. When HSW is shorted and DUT is turned ON, the current limited by inductor starts to linearly rise. In the experiments, DUT and HSW are turned off when the current I_D reaches the required (pre-set) value. The magnetic field in the inductor L induces a counter electromagnetic force (EMF) that can build up surprisingly high potentials across the switch (DUT). If no protective circuits are added to the switch, all the energy accumulated in the inductor is dissipated directly in the device switch. [9] Conditions set for the repetitive UIS stress measurements were: inductance L = 1mH, supply voltage V_{DD} = 100V, switched current I_{AS} = 15A. The switching period between two pulses was set to 5ms and an additional time of 800ms was set after every 100 pulses. Current and switching period was set with accordance to minimize heat accumulation in samples and maximum non-destructive single pulse current for given inductive load.

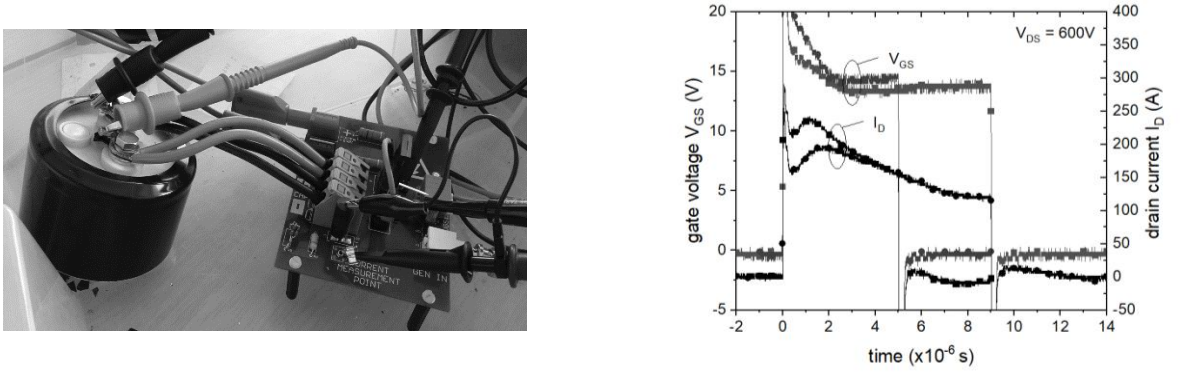
SC test – Short circuit measurements were done on the custom-built tester. Test parameters were defined for SC-I defined by JEDEC standards. Typical current and voltage waveforms during the short circuit test are shown in figure 2b. Test conditions were V_{DD}= 400/600V, SC pulse length t_P= 5us, time between pulses was set to t_T= 0.4s to prevent heat accumulation.

RESULTS - REPETITIVE UIS

First single pulse UIS capability of tested devices was verified. Obtained values of destructive currents of TrenchMOS and planar devices measured for different inductances are shown in Figure 3. Observed results are in good agreement with basic UIS theory where if the intrinsic temperature of the blocking PN junction is assumed as a critical value for the passive mode of destruction and tests start at a constant temperature, then the relation between the inductance L and the critical value of avalanche current I_{Avcrit} can be written as [8]:

$$\Delta T_M = \frac{\sqrt{2}}{3} C_{th0} . I_{AV} . V_{B\,Reff} . \sqrt[2.2]{\frac{LI_{AV}}{V_{B\,Reff}}} \rightarrow$$

$$I_{AVcrit} \sim \sqrt[3.2]{\frac{1}{L}} \quad .$$



(a) (b)

Fig. 2a) Custom built SC-I test board. b) Typical drain current and gate voltage waveforms of planar SiC MOSFET under SC conditions at 600V supply voltage, V_{GS} = 15 V and pulse lengths of t_p = 5 and 9 µs.

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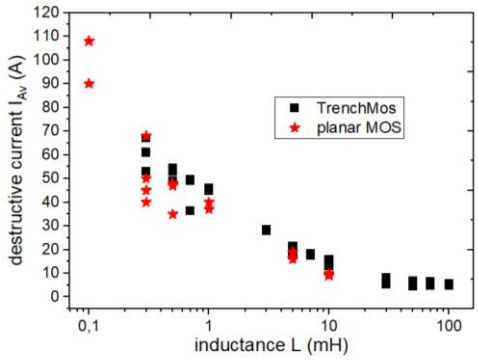
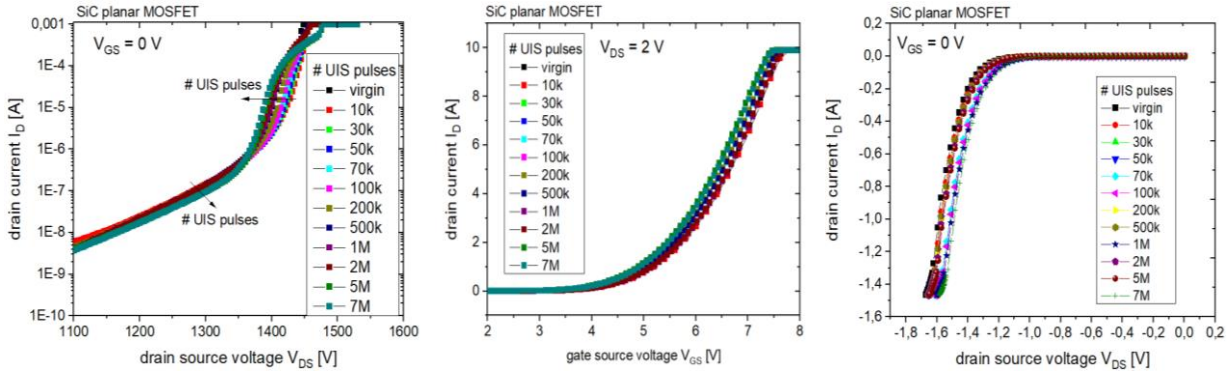


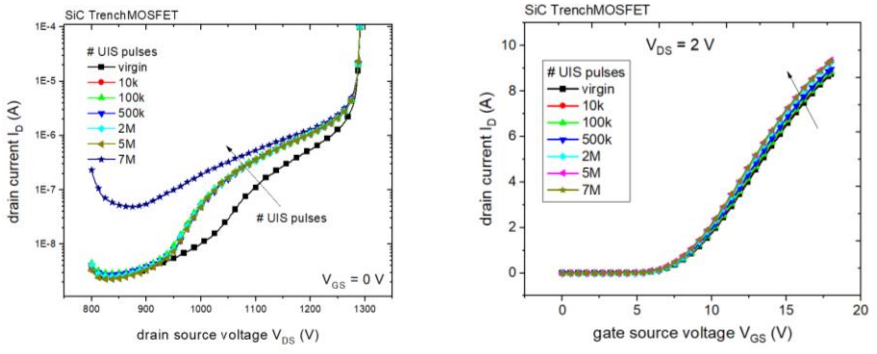
Fig. 3 Measured destructive currents of TrenchMOS samples for different inductive loads.

An interesting observation was that samples have very similar single pulse UIS capability, despite the fact that the active area of planar devices was more than 2 times larger than that of trench devices. Set conditions for the repetitive UIS stress measurements (L = 1mH, I_{AS} = 15A) were significantly lower than destructive currents for given inductance. Because during switching significant heat is generated in transistors, I-V measurements were performed after device cool down to prevent impact of temperature on device parameters shift. First, parameter shift induced by repetitive UIS was analysed on planar transistors. Measured I-V characteristics for virgin and stressed samples up to 7 million UIS pulses are shown in Figure 4. Observations were as follows: Repetitive UIS pulses induced shift all analyzed I-V curves. The shift in output, transfer, and diode characteristics was not uniform. However, after 7 million of stress pulses samples exhibit lower on-resistance RDSon than virgin samples, which can be attributed to change of threshold voltage VTH which decreased from a value of 3,13 V to a value of 2.87 V. It is a known fact that during the avalanching phase of UIS pulse, large concentrations of high energy carriers are generated close to blocking PN junction. The negative shift of threshold voltage, therefore, indicates the trapping of positive charge on the gate interface or in the gate dielectric. The origin of this positive charge can be attributed to high energy holes generated during UIS. The shift of diode characteristics indicates the presence of trapping effects also in the volume of the device on / close to blocking PN junction. Also, in this case, a decrease of diode threshold voltage indicates the trapping of the positive charge. Both effects, trapping on gate interfaces and in the volume, have a strong impact on the breakdown voltage of the device, which was most impacted. Due to repetitive UIS stress decrease of static breakdown voltage ΔBVDSS = -46 V was observed. Next, repetitive UIS was performed on samples with trench technology of the gate electrode. The impact of repetitive UIS on I-V characteristics is shown in Figure 5. Similar to a transistor with the planar gate electrode, the negative shift of threshold voltage was observed with the corresponding decrease of on-resistance. Indifference to the planar transistor, a significant increase of the drain



(a) (b) (c)

Fig. 4 planar SiC MOSFET - Measured impact of repetitive UIS on stability of electrical characteristics of planar SiC MOSFET. a) breakdown characteristic, b) Transfer characteristic, c) diode characteristics.



(a) (b)

Fig. 5 SiC TrenchMOSFET - Measured impact of repetitive UIS on stability of electrical characteristics. a) breakdown characteristic, b) Transfer characteristics.

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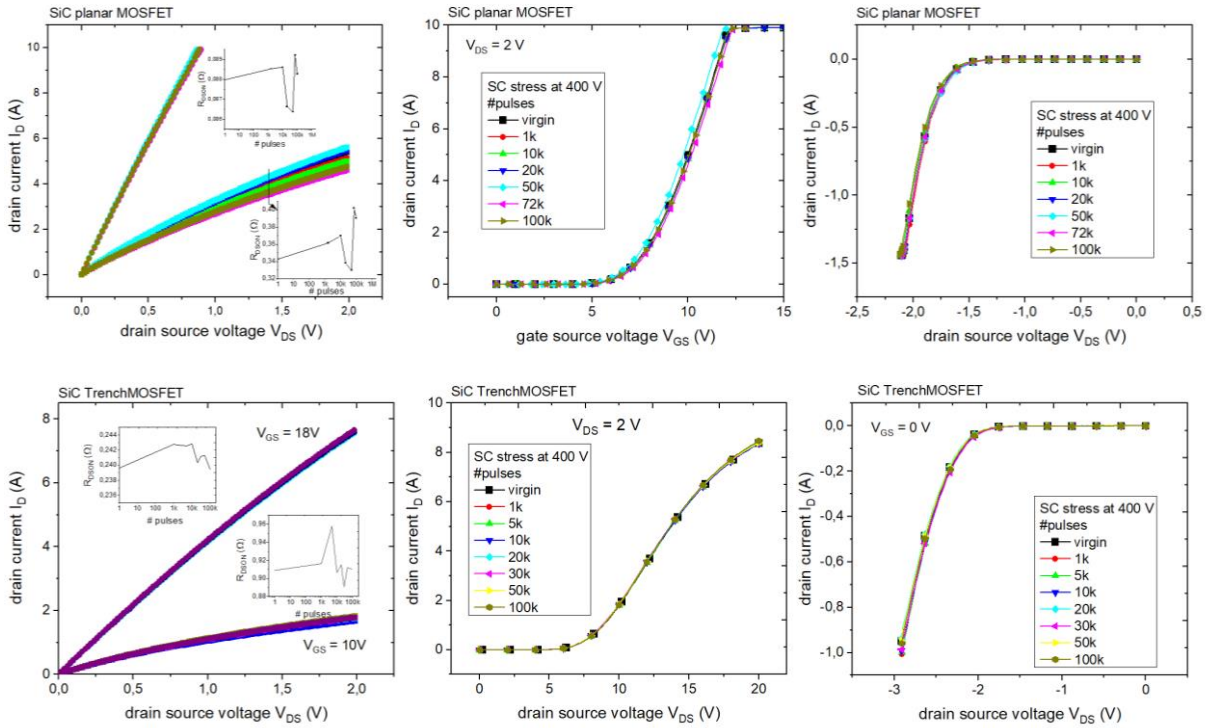

Fig. 6 Measured impact of repetitive SC stress on stability of electrical characteristics for buss voltage 400V for planar device (top) and TrenchMOSFET (bottom). Measured characteristics from left: output for V_{GS}= 10V and 18V, transfer characteristics for V_{DS} = 2V and antiparallel diode forward characteristics.

leakage current was observed (from 10 nA to 193 nA at V_{DS} = 1000V) and no impact on the breakdown voltage was observed.

RESULTS - REPETITIVE Short Circuit

Before repetitive SC experiments were performed it was necessary to determine maximum operating conditions for both trench and planar types of samples. TrenchMOS devices were capable to sustain short circuit pulses with pulse lengths of more than 20 µs at 600V bus voltage and VGS = 15 V. Planar devices performed worse. Most of the devices were able to sustain short circuit pulses in the range of 10 - 12 µs at 600V bus voltage. Therefore, the length of short circuit pulses was set to 5 µs for both types of samples. Repetitive short circuit experiments were performed at two buss voltages 400 V and 600 V. In Figure 6 are compared I-V characteristics for trench and planar MOSFET obtained from experiments performed at 400V bus voltage. The only very small impact of repetitive SC stress at 400V on output, transfer, and diode characteristics was observed for TrenchMOSFET. In the case of the planar device, a small shift of threshold voltage was observed and associated shift of on-resistance and shift of output characteristics. First, on-resistance was increasing for the first 10k pulses, the next a significant decrease down to 96% of the original value was observed after 50k of stress pulses. After the next 30k pulses on-resistance significantly raised to 114% of the original value.

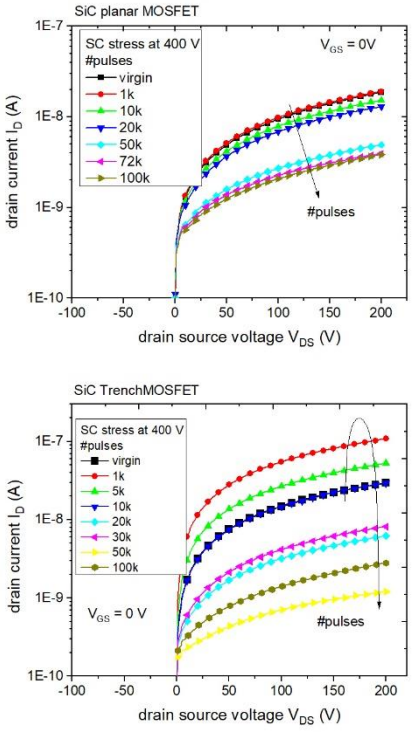

Fig. 7 Impact of repetitive SC stress at 400V on leakage current of planar and trench MOSFET device.

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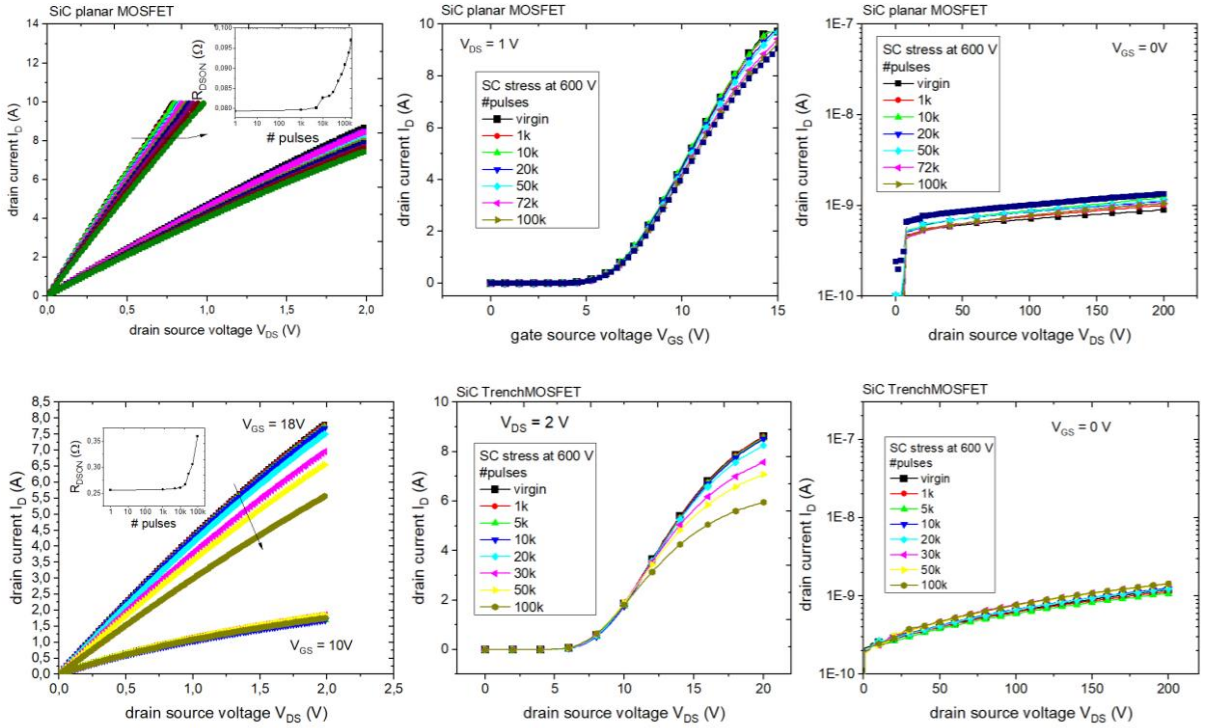

Fig. 8 Measured impact of repetitive SC stress on stability of electrical characteristics for buss voltage 600V for planar device (top) and TrenchMOSFET (bottom). Measured characteristics from left: output for V_{GS}= 10V and 18V, transfer characteristics for V_{DS} = 2V and drain leakage current characteristics.

This nonuniformity in changes indicates that at least two degradation mechanisms are present with the opposite effect on threshold voltage and on-resistance. Also, significant impact of SC stress was observed on leakage current (Fig. 7) in both devices. First, the leakage current was increasing with a number of stress pulses. For planar MOSFET this increase saturated after 1k of stress pulses and for devices with trench gate structure, increase saturated after 10k of stress pulses. After that leakage current was decreasing and after 100k of stress pulses its value was more than one magnitude lower than for virgin sample.

The next impact of repetitive SC stress at 600V was analyzed. Fresh devices were used for this analysis. Results are shown in Figure 8. At first glance, we can state that SC stress at 600V has a more significant impact on the performance of both devices especially on the threshold voltage and on the on-resistance of devices. A positive shift of threshold voltage ΔV_{TH} = +0.2 V was observed for planar devices. For TrenchMOSFETs threshold voltage was increasing for the first 10k pulses (ΔV_{TH} = +0.1 V) and then it was decreasing. After 30k it reached the initial value and next after 100k pulses it was 0,2 V lower than the initial value. A Uniform increase of on-resistance was observed for both devices. It was increasing first slowly for the first 10k pulses and the next dramatic increase was observed. After 100k pulses on resistance increased by 23,5% in the planar device and by 38,5% in TrenchMOS device. Surprisingly SC stress at 600 V had minimal impact on leakage current, and similar to stress at 400V small impact on diode characteristics was observed.

CONCLUSION

The degradation of commercial planar and trench gate 1,2 kV 4H-SiC MOSFETs subjected to the repetitive avalanche and short circuit pulses is investigated in this paper. ITC55100 UIS tester and custom-built SC tester are utilized to generate the stress. The strong impact of both stresses on the electrical performance of tested devices was observed. After repetitive UIS stress test devices show an almost consistent degradation tendency characterized by the decrease of Vth, an increase of RDSON, and leakage current. Moreover, a significant decrease in breakdown voltage was observed for planar devices. SC stress was performed at two bus voltages 400 and 600 volts. For SC stress performed at 400V, only a small impact on the electrical performance of TrenchMOSFET was observed, while a small increase of on-resistance was observed for planar devices. Stress at 400 V had a strong impact on drain leakage current. For SC tests performed at 600V significant increase of RDSon with the increase in the number of stress pulses was observed for both devices. TrenchMOSFET performs worst than the planar device at 600 V stress. A significant increase of on-resistance (38,5%) of TrenchMOSFET was measured after 100k stress pulses.

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This may be caused by the lower maturity of trench technology on SiC. It is believed that the main impact on the variation of the electrical characteristics and parameters have hot carriers injection and attributed trapping and traps generation in the gate oxide and/or at the channel interfaces.

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