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High-Voltage IGBT turn-off at transition from overcurrent to desaturation

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Abstract

The turn-off capability of a power semiconductor is normally given by the datasheet with test conditions. The RBSOA (Reverse Bias Safe Operation Area) diagram limits the collector-emitter peak voltage and maximum turn-off current [1]. As mentioned in the early literature and many datasheets of IGBT power modules, the current which can be turned off is limited to twice the nominal current, in the between this and short circuit it is forbidden to turn off the device [2]. In this paper, the turn-off behaviour of HV-IGBTs at the transition from overcurrent to desaturation is investigated with a 2D half-cell model in Synopsys TCAD as well as with single chip measurements. This article focuses on the classification of the turn-off process near the V_{CE} desaturation, with respect to the plasma- and electric field distribution, dynamic avalanche, as well as electric field peaks which occur during this process. It shows that the IGBT can be operated in this former forbidden region successfully, and a beginning desaturation releases dynamic avalanche.

Keywords: Overcurrent, IGBT turn-off behaviour, RBSOA, desaturation, dynamic avalanche, TCAD.

1 Introduction

In this paper, the overcurrent turn-off is investigated for three situations according to the initial state of the device, see Fig. 1. Turn-off situation I locates the voltage saturation region. The turn-off current is normally limited to two or three times of nominal current according to the RBSOA of the datasheet for situation I. At high current, dynamic avalanche can happen. Nowadays IGBTs can bear significant dynamic avalanche.
When the turn-off current is further increased, the device is turned off at the channel pinch-off region, normally four to five times nominal current. In this situation II, the device is close to the intersection of the voltage saturation and desaturation region.

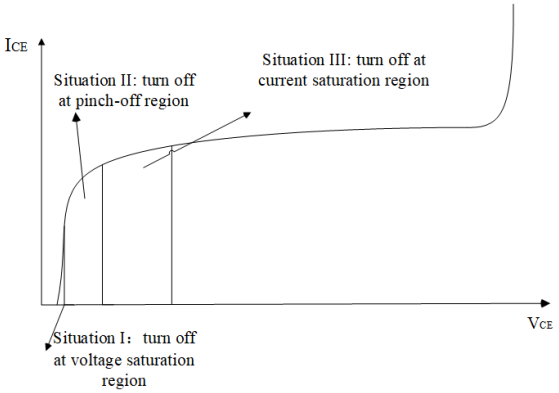

Fig. 1 Schematic diagram of different turn-off situations. Siutation II is forbidden for turn-off in [2]

In situation III, which locates close to the desaturation region, the initial value of the collector-emitter voltage V_{CE} is already much higher than the on-state voltage, the initial state of the device is similar to short circuit.
In the next chapters, these statements will be verified by experiments as well as TCAD simulation results.

2 Experimental results

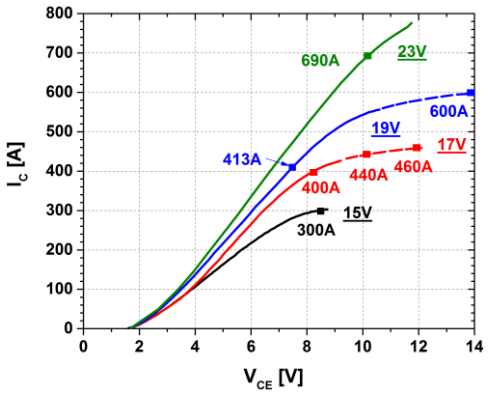

Fig. 2 Output characteristic of 4500 V IGBT, single chip. Points of turn-off measurements are marked. T = 25 °C

In the measurements, the device under test (DUT) is one single chip from a 4500 V press pack IGBT, rated for 50 A with a recommended gate emitter voltage V_{GE} 15 V. The output characteristic of this chip at room temperature at V_{GE} 15 V to 23 V is given in Fig. 2. At V_{GE} 15 V, the chip is in the voltage-saturated region up to 200 A (4 times rated current). With a further increased collector

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current I_C, the device approaches towards the desaturation region, the collector emitter voltage V_{CE} increases significantly.

All following turn-off measurements are executed at T = 25 °C. The measurement circuit for the overcurrent turn-off behavior is given in Fig. 3. The circuit includes the DC link voltage V_{DC}, a protection IGBT SIGBT, a stray inductance L_{stray}, a freewheeling diode FWD, a load inductance L_{load} and the DUT. The device is first ramped up with the load inductance to a desired value, it can be controlled by the pulse length, and then the device is turned off. The pulse length has to be rather short to prevent self-heating, but also not too short to ensure that the charge carrier distribution is close to a stationary situation. The protection IGBT will switch off within some micro seconds once a short circuit is detected in the circuit.

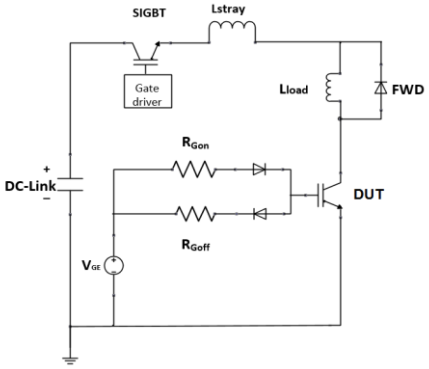

Fig. 3 Schematic diagram of measurement circuit

2.1 Turn-off as a single chip, medium L_{stray}

a) Turn-off with different R_{goff}.

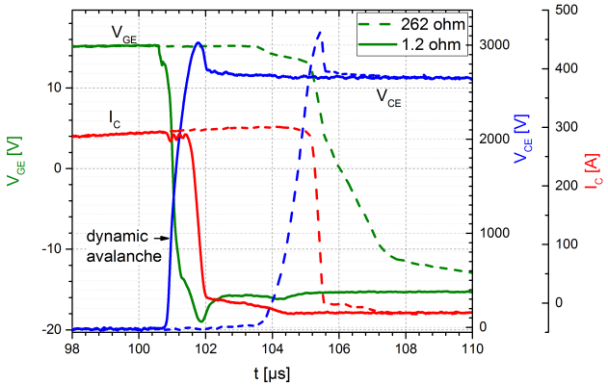

Fig. 4 Turn-off with different Rgoff, V_{GE} 15V

Test	1	2
V_{DC} [V]	2700	2700
I_{OFF} [A]	300	300
L_{stray} [nH]	430	430
L_{load} [µH]	1000	1000
t_{on} [µs]	100	100
R_{gon} [Ω]	1	1
R_{goff} [Ω]	**262**	**1.2**
V_{GE} [V]	-15/+15	-15/+15

Tab. 1 Test condition for turn-off with different R_{goff}, V_{GE} 15V

The measurements were first carried out with a medium L_{stray} of 430 nH with R_{goff} 262 Ω and 1.2 Ω at V_{GE} 15 V. The test conditions are given in Tab. 1. As shown in Fig. 4, after the gate voltage is switched to negative, the current continues to conduct until V_{CE} reaches the DC link value. The voltage peak of the single pulse measurement is determined by the stray inductance L_{stray} in the circuit multiplied by the slope of the current di_C/dt plus the turn-on voltage peak V_{FRM} of the diode. The changing of dv_{CE}/dt during the V_{CE} slope indicates the appearance of dynamic avalanche [3], but in this case it is only weakly pronounced. The device can be turned off at I_C 300 A near the desaturation region even with a very small gate resistance. As the gate resistance increases, the large gate resistance will slow down the discharge of the gate and keep the gate in the on-state for a longer time, so that more electrons are injected to compensate the holes which are injected from the collector side. In this case, a sign of dynamic avalanche by turn-off with 262 Ω is not observed. For 1.2 Ω, the IGBT is in the self-controlled region, which is determined by the plasma dynamics. The voltage peak is higher than the turn-off with a smaller R_{goff}.

b) Turn-off at different current, situation I, II, III

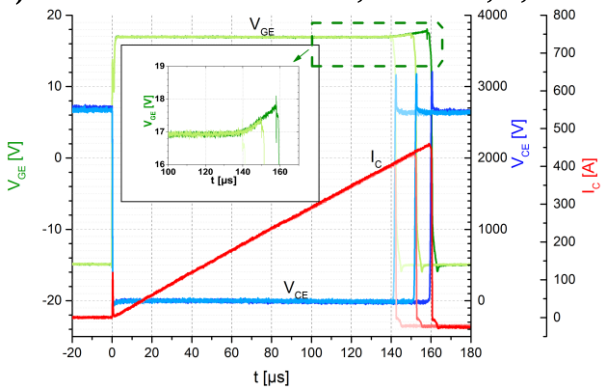

Fig. 5 Turn off at different current, situation I, II, III, V_{GE} 17 V

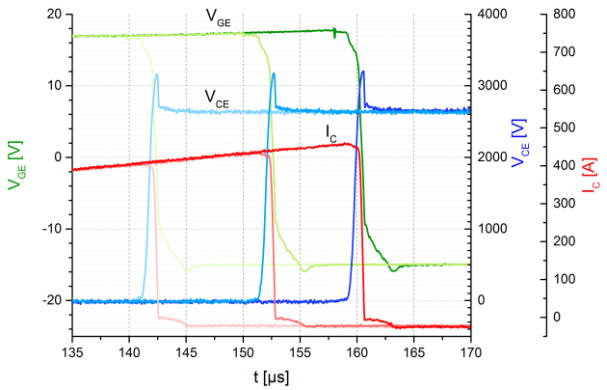

Fig. 6 From 140 µs to 170 µs of Fig. 5

Test	1	2	3
V_{DC} [V]	2700	2700	2700
I_{OFF} [A]	**400**	**440**	**460**
L_{stray} [nH]	430	430	430
L_{load} [µH]	1000	1000	1000
t_{on} [µs]	140	150	160

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R_{gon} [Ω]	1	1	1
R_{goff} [Ω]	100	100	100
V_{GE} [V]	-15/+17	-15/+17	-15/+17

Tab. 2 Test condition for turn-off at different current, situation I, II, III

After the devices turned off under V_{GE} 15 V without destruction, the gate voltage was increased to 17 V, so as to achieve a higher turn-off current. In this set of measurements, as the test condition is given in Tab. 2, the device turned off at 400 A, 440 A and 460 A by changing the pulse length. The three turn-off points are also marked in Fig. 2. The initial state of turn-off at 400 A is located just before desaturation. By a further increased turn-off current at 440 A and 460 A, the device is turning off in the region of situation II. The measurement results show an increase of V_{GE} starting from 400 A, see Fig. 5 and Fig. 6. This is due to the increased V_{CE} directly at the beginning of the turn-off process caused by the early desaturation. The gate capacitance is charged further by a feedback across the C_{GE} (Miller feedback). In other words, the turn-off process starts directly at the Miller plateau. Since the current is still rising until the DC-link voltage is reached, also the Miller plateau voltage has to rise. The rise of V_{GE} is the indication that the turn-off initial condition starts entering the desaturation region, which marks the start of the turn-off situation II. To further verify this statement, two turn-off measurements with comparable current values and different gate voltages were carried out.

c) Turn-off at comparable current, different gate voltage.

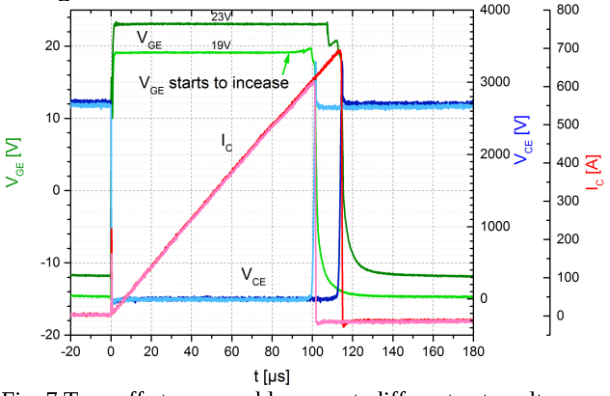

Fig. 7 Turn off at comparable current, different gate voltage

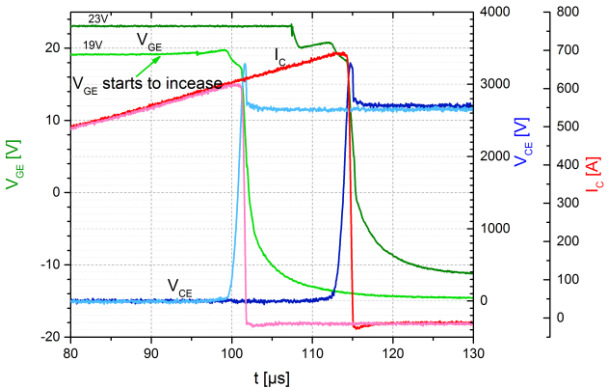

Fig. 8 From 80 µs to 130 µs of Fig. 7

Test	1	2
V_{DC} [V]	2700	2700
I_{OFF} [A]	**600**	**690**
L_{stray} [nH]	430	430
L_{load} [µH]	500	500
t_{on} [µs]	96	108
R_{gon} [Ω]	1	1
R_{goff} [Ω]	330	330
V_{GE} [V]	-15/+19	-12/+23

Tab. 3 Test condition for turn-off at comparable current, different gate voltage

As given in Tab. 3, the device was turned off at V_{GE} 19 V, 600 A, and V_{GE} 23 V, 690 A. From the output characteristic in Fig. 2, it is clear to see that for V_{GE} 19 V the initial state of the device before turning off is already in the region of situation II, however, this current value is still located in the region of situation I for V_{GE} 23 V, even at a higher current of 690 A. Fig. 7 and Fig. 8 show the turn-off behaviour for these two currents. For the measurement at V_{GE} 19 V, the gate voltage starts to increase before it starts the descent process. That means that the device is already in the desaturation region from the beginning of the turn-off process. Compared to the measurement at V_{GE} 23 V, no increase in the gate voltage is observed. This measurements proves the previous explanation.

2.2 Turn-off as a single chip with high L_{stray} and R_{goff}

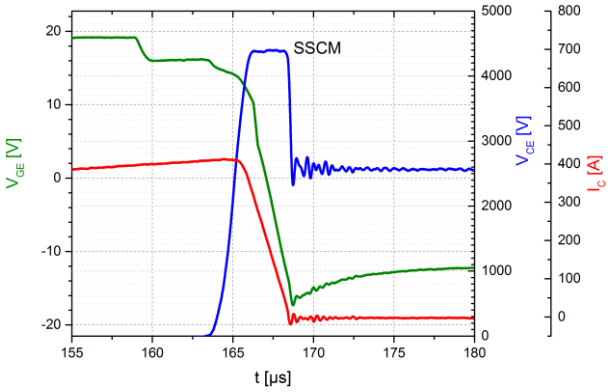

Fig. 9 Turn-off as a single chip with real-application scaled L_{stray} and R_{goff}

In order to achieve a comparable test condition to the measurement with press the pack IGBT, the stray inductance L_{stray} and the gate resistance R_{goff} were scaled according to the data sheet and the amount of chips. Due to the additional L_{stray}, the test condition becomes more critical, as the voltage peak is very close to the static breakdown voltage of 4500 V mentioned in the data sheet. This set of measurements first starts with a large gate resistance and gate voltage of 15 V to avoid too high di_C/dt and dv_{CE}/dt. Afterwards, the gate resistance is gradually reduced or the gate voltage is increased until the device is fails. The device can turn off at V_{GE} 15 V in the desaturation region with comparable test conditions as given in the data sheet. By further increasing the gate voltage and collector current, the chip failed. Fig. 9 and

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Tab. 4 show the penultimate pulse before destruction and the corresponding test conditions.

Test	1
V_{DC} [V]	2700
I_{OFF} [A]	**413**
L_{stray} [µH]	13
L_{load} [µH]	1000
t_{on} [µs]	135
R_{gon} [Ω]	1
R_{goff} [Ω]	270
V_{GE} [V]	-12/+19

Tab. 4 Test condition for turn-off as a single chip with real-application scaled L_{stray} and R_{goff}

As shown in Fig. 9, the device turned off at 413 A, V_{GE} 19 V, still located in the $V_{CE,sat}$ region. The chip was already undergoing a lot of stress because the large L_{stray} causes high overvoltage and triggers switching self-clamping-mode (SSCM) [4] [5]. The clamping voltage V_{SSCM} amounts 4400 V which is very close to the static V_{BR} value determined for this IGBT type in [6]. In SSCM holds according to [5]

$$\frac{\mathrm{d}i_C}{\mathrm{d}t} = \frac{V_{Clamp} - V_{DC}}{L_{stray}}.$$

The dissipated peak power is about 1.7 MW/cm². This shows an excellent overstress capability. By further increasing the turn-off current, the device failed by next pulse.

3 Simulation results

In this part, semiconductor simulations were carried out with Synopsys TCAD. A 2D half-cell model rated for 4500 V, 50 A was used. The turn-off behaviour for three turn-off situations is further explained, the internal characteristics, e.g. electric field, electron/hole density, etc. help to understand the different situations better.

3.1 Simulation of three turn off situations

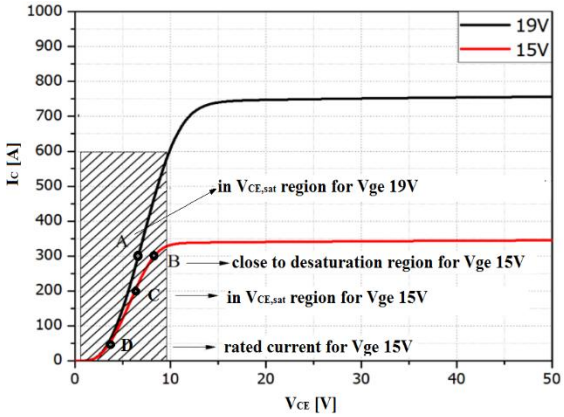

Fig. 10 Output characteristic for simulation model

First, the three turn-off situations were simulated. The turn-off initial states are marked in Fig. 10. In this figure, the point D stands for the nominal current (50 A) and represents the turn-off initial state for situation I. Point C describes a value of four times nominal current (200 A) and represents the turn-off initial state for situation II. Point B holds for six times the nominal current (300 A) and represents the turn-off initial state for situation III.

a) Turn-off at situation I, Fig. 10, point D

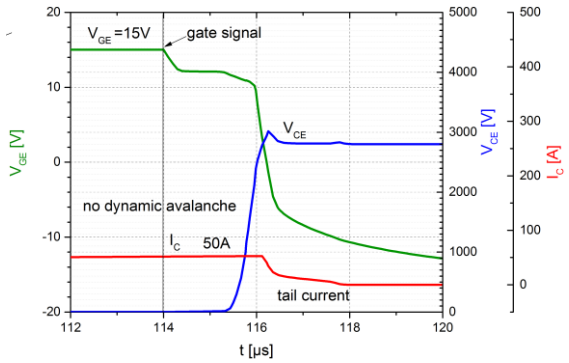

Fig. 11 TCAD simulation for turn-off at situation I, Fig. 10, point D, L_{stray} = 1200 nH, R_{goff} = 72 Ω

Situation I is shown in Fig. 11. No V_{GE} increase can be found. The IGBT is turned off in the normal operating region. At the end of the current slope, the tail current can be seen clearly. No dynamic avalanche was observed as there was no obvious changing of dv_{CE}/dt.

b) Turn-off at situation II, Fig. 10, point C

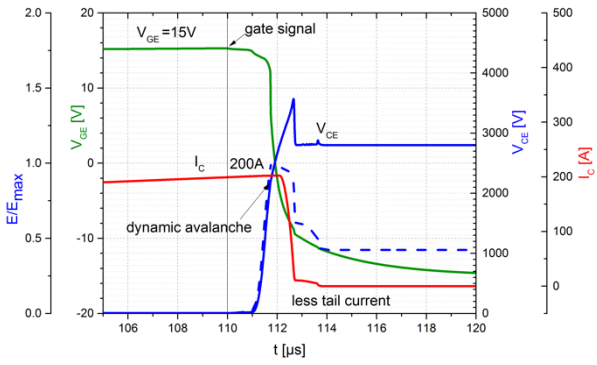

Fig. 12 TCAD simulation for turn-off at situation II, Fig. 10, point C, L_{stray} = 1200 nH, R_{goff} = 72 Ω

The second situation showing the process of turn-off under four times rated current is depicted in Fig. 12. The turn-off region is close to the boundary of the saturation region and desaturation region. At the moment of turn-off, marked as ‘‘gate signal’’ in Fig. 12, V_{CE} increases to 7 to 10 V. As the increase of V_{CE} cannot be ignored, the displacement current through the gate cannot be neglected anymore. The details will be explained in the following.

At the beginning of the inductance charging, the V_{GE} of 15 V stays constant with increasing collector current. When the load current increases to the boundary of the saturation region of the output characteristic, V_{CE} gets greater than the on-state voltage from that time onwards.

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The increasing V_{CE} influences the depletion capacitance, since the depletion region extends with the increasing collector-emitter voltage. Therefore, the whole capacitance between collector and gate C_{GC} decreases. The depletion capacitance part of C_{GC} starts to be charged in advance – a displacement current is flowing. This will raise the potential at the gate.

While the current is still increasing, V_{CE} also increases and quickly reaches the condition of pinch-off.

It has to be noted that the n-channel is pinched off at that moment but the electrons flow with a high velocity caused by a stronger electric field strength. Reducing electrons cannot compensate the increasing number of injected holes from the collector. In this case, dynamic avalanche is more prone to happen [3].

In Fig. 12, the dynamic avalanche happens when the maximum electric field reaches the peak value, around V_{CE} of 2500 V. At the same time, the channel is also closed. The dynamic avalanche generated electrons compensate a large number of holes from the collector and plasma. Compared to situation I, the duration of the Miller plateau is shorter. V_{GE} decreases quickly to the threshold voltage. This change in V_{GE} largely results from the fact that the depletion capacitance part of C_{GC} charges before the IGBT is turned off. With the passage of time, the electric field extends towards the n-buffer region, which removes already a large part of the plasma. The maximum electric field drops after the voltage spike.

c) Turn-off at situation III, Fig. 10, point B

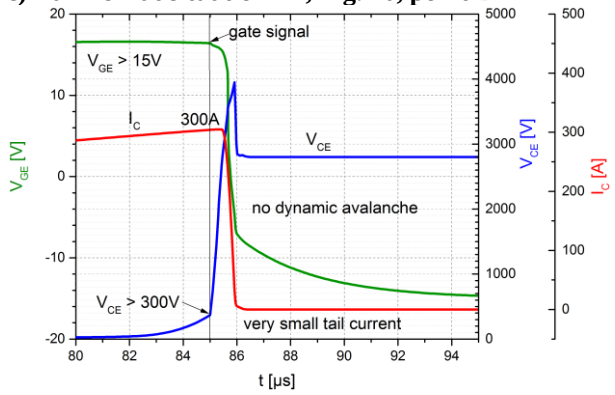

Fig. 13 TCAD simulation for turn-off at situation III, Fig. 10, point B, L_{stray} = 1200 nH, R_{goff} = 72 Ω

The last situation can be described as follows: at the end of the charging pulse, V_{CE} increases much more than the on-state voltage. It goes up along the output curve to the desaturation region and amounts to 300 V, see Fig. 13. In this case, the channel is pinched off early during the pulse and the junction-capacitance part of C_{GC} is charged already significantly. The displacement current through C_{GC} also causes the increase of V_{GE}. After starting the turn-off event at the gate driver there is no dynamic avalanche happening, even though the load current arrives at six times rated current. Furthermore, V_{CE} increases so quickly because there is no dynamic avalanche [7]. Besides, the duration of the Miller plateau is also short. Before V_{GE} has reached the threshold voltage V_{TH}, the electric field has been built up. Therefore, injected holes from the collector flow with high drift velocity through the base region. The current density drops a lot compared to the voltage saturation region. After V_{CE} reaches the DC link voltage, the decreasing I_C induces a high voltage spike in this case. The reason is that without dynamic avalanche, no avalanche generated electrons from the depletion region compensate the holes from the plasma or collector inside the device.

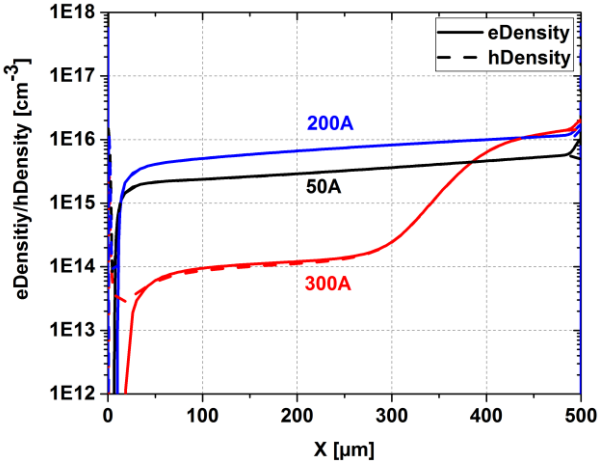

Fig. 14 Carrier density at turn-off moment of point B, C, D from Fig. 10, marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13

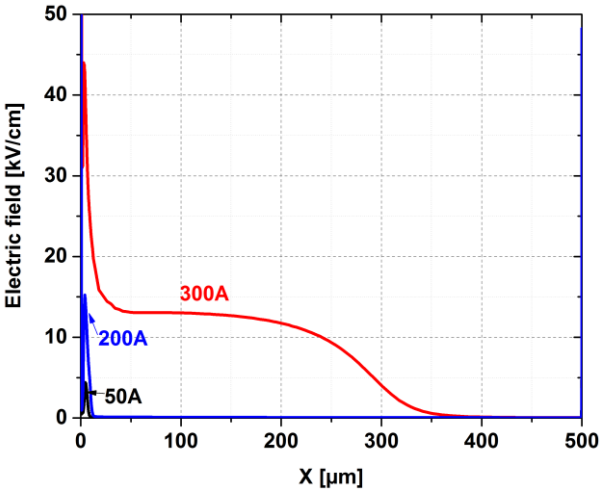

Fig. 15 Electric field at turn-off moment of point B, C, D from Fig. 10, marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13

To prove the explanation above for situation III, the comparison of the carrier densities and the electric field distribution between situation I, II and III is given in Fig. 14 and Fig. 15. At the moment of the gate signal turned off, which are marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13, the carrier density has dropped to 1E14 cm^{-3} for 300A, while the carrier density for 200A remains still at 7E15 cm^{-3}. The free carriers occupy the whole base region for 200A, and the electric field peak at that moment is not very high, because the IGBT is still at the boundary of the voltage saturation region. For 300 A, it is clear to see from Fig. 15 that the electric field already expands towards the collector side and occupies the most area of n^- region.

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3.2 Simulation of turn-off at different gate voltage

As already measured in the chapter 2.1c, the simulation in this part can also verify that explanation. The device was turned off at the same current but a different gate voltage, see Fig. 10, point A and B. According to the output characteristic at V_{GE} 19 V, the turn-off current 300 A is still in the voltage saturation region. Therefore, V_{CE} stays around the on-state voltage before turn-off. The displacement current can be neglected at the beginning of the turn-off event. With a high carrier density before the turn-off moment, the existence of the dynamic avalanche suppresses the voltage spike visible in Fig. 13. Although the two simulation projects are turned off at the same current 300 A, the behaviour of the turn-off process is quite different.

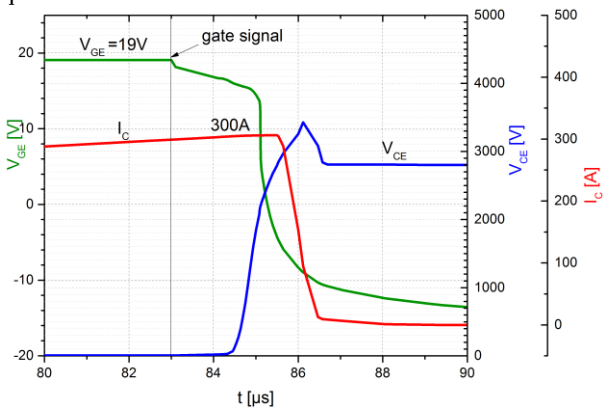

Fig. 16 TCAD simulation for turn-off for point A with V_{GE}=19V, Fig. 10, L_{stray} = 1200 nH, R_{goff} = 72 Ω

Comparing Fig. 16 with Fig. 13, the tail current is smaller at V_{GE} 15 V and the duration of the turn-off process is shorter. Because at V_{GE} 15 V a part of the charge-carrier plasma is already extracted in advance of the negative d*i*/d*t* phase (see Fig. 14 and Fig. 15). The formation of the electric field occurs earlier compared to V_{GE}=19V.

4 Conclusion

In this paper, it has been shown with experiment and simulation that IGBTs can be turned-off at high over-currents and even at the transition from overcurrent to voltage desaturation like in short circuit. The overcurrent turn-off is classified in situation I, II and III based on the simulation and measurement results of 4500 V IGBTs. The initial state of turn-off, e.g. expansion of the electric field and the electron/hole density, is the key to distinguish these three turn-off situations. Additionally, the rise of the gate voltage is an indication of the turn-off towards the desaturation region. The dynamic avalanche is influenced by the charging state of the gate and it can suppress high voltage spikes. The tail current is smaller, if the electric field is already partially established before the gate signal turns to negative. At the transition from voltage saturation to current saturation, the IGBT is released from dynamic avalanche. The simulation shows a stabilizing effect. However, high overvoltage peaks must then be withstood by the device.

There are still some points to be investigated in future work: the behaviour at high operation temperature, the overshoot of V_{CE} and the shape of it and the SSCM mode. Also, a turn-off at even higher gate voltages could be of interest. Further, a possible current filamentation process at multi-cell models should be investigated.

5 Acknowledgements

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