ČVUT
ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

REVIEWER'S OPINION OF FINAL THESIS

I. IDENTIFICATION DATA

Thesis name:	**FlexPRET real-time processor in heterogenous system**
Author's name:	**Dwivedi Prasoon**
Type of thesis:	bachelor
Faculty/Institute:	Faculty of Electrical Engineering (FEE)
Department:	Department of Cybernetics
Thesis reviewer:	Eduardo Augusto da Costa
Reviewer's department:	-

II. EVALUATION OF INDIVIDUAL CRITERIA

Assignment **ordinarily challenging**

Evaluation of thesis difficulty of assignment.

There are four major goals – still better steps – to fulfil this thesis:

- Understand the problem of time predictability on embedded systems;
- Learn a high-level synthesis language and the overall functioning of a microprocessor intellectual property (IP);
- Make use of this IP in a real platform, and show a technical solution for the problem;
- Compare the results with other works of softcore RISC-V IPs.

As the use of FPGA by itself is not an easy task, and as it goes from the theory to comparing a technical by-product with other solutions, I grade it ordinarily challenging.

Satisfaction of assignment **fulfilled with major objections**

Assess that handed thesis meets assignment. Present points of assignment that fell short or were extended. Try to assess importance, impact or cause of each shortcoming.

The problem of time predictability on embedded systems is defined in a rather good way, as are the theory related topics examined by the author.

However, the use of a CPU IP on an FPGA platform while generically presented in the text, it is not explored by the author in its results review or its conclusion. Some topics are not approached, such as what adjustments were made to the IP core so it could work on the FPGA platform? Or no adjustments were required at all?

Some sub-goals, such as creating a program to test the platform, which would be a rather spotless way to show the understanding and technical aptitude to do so, is not done.

Thus, from the understanding of the problem addressed in this work to the final product in a platform, only the understanding of the issue and its presentation are completed. The following stages lacked more extensive work, yet even imperfectly, they are done. Finally, I grade it fulfilled yet with major objections.

Method of conception **correct**

Assess that student has chosen correct approach or solution methods.

The procedure adopted by the author is coherent with the expectations of such problem. Once the problem was well understood:

- The overall framework is well chosen, yet it lacked explanation in some topics such as why FPGA and not something else;
- The processor IP as presented is adequate for embedded applications requiring time predictability – the author hit the spot;
- Some major simulation to see the platform working is done.

Yet it is short of a final validation of the platform as well as a stronger analysis of the results, the method is competent, thus correct, as I grade it.

Technical level **E - sufficient.**

Assess level of thesis specialty, use of knowledge gained by study and by expert literature, use of sources and data gained by experience.

Guided by the design flow procedures for FPGA, and theory about microprocessors, embedded electronics, the author aimed to produce a working model of softcore, and then to run benchmarks and a self-authored program, and then compare it with other authors or products.
The softcore was indeed generated, yet the text suggested it was not a fully functioning model on FPGA (if it is fully working on the FPGA, the author lacked expressivity).
The author then simulated the execution of benchmarks in the processor, which is a good realization, as the FPGAs are not the friendliest platform to work on.
This work lacks a comprehensive comparison and analysis of results, but still there is sufficient production for a bachelor thesis.

Formal and language level, scope of thesis **E - sufficient.**

Assess correctness of usage of formal notation. Assess typographical and language arrangement of thesis.

The text organisation is good overall. The progression of the themes is persistent and logic: the problem is presented, the many theories involved are presented, and so the technicality.
Following theories, the author goes to the implementation phase and presents it, but it is where it starts lacking data, organization, and presentation. The technical work is mostly shown, but as a reader I cannot know for sure what the author accomplished. Also, more technical comparations and analysis are expected to be seen in such a work, but it is barely done.
Finally, as it is shown in the next evaluation item, more than once information is presented without a proper citation, which makes it to resemble opinion, like in "*Hardware engineers are usually very proficient with C, but not with object-oriented programming, functional programming, or complex projects that use modern software engineering principles. This sets up biases against Chisel or similar languages."*.
So, summing up, I grade this work sufficient in this item of evaluation: while it is not perfectly done, the general expected structure, language and progression are present.

Selection of sources, citation correctness **E - sufficient.**

Present your opinion to student's activity when obtaining and using study materials for thesis creation. Characterize selection of sources. Assess that student used all relevant sources. Verify that all used elements are correctly distinguished from own results and thoughts. Assess that citation ethics has not been breached and that all bibliographic citations are complete and in accordance with citation convention and standards.

Although some major topics are covered with sources and references, it is not the norm in this thesis.
Entire topics – like "*Introduction to FPGA"* – are fully presented without referencing. For this FPGAs topic, for example, even the *datasheet* for the FPGA used would mostly suffice as source of information. Also, some numeral data presented "*20%"* and suggestion of scientific data "*This silicon inefficiency is the price to pay for programmability and is the reason why FPGAs have been more successful in high-end, low-volume applications"* is not backed by references. Moreover, in topics such as "*RISC",* "*Description of Processor*", or even "*Hardware Threads"* there are well-established and thus well-known authors like Ph.D. David Patterson and Ph.D. Andrew Tanenbaum, which ideally should be referenced in such themes.
The list goes on, on the topic *Chisel vs. classic HDLs*, the author presents an interesting comparison of *Classical* hardware description languages and high-level synthesis ones, while backing some data with reputable information, some hardly necessary information is on the text as well, like "*Hardware engineers are usually very proficient with C, but not with object-oriented programming, functional programming, or complex projects that use modern software engineering principles. This sets up biases against Chisel or similar languages"*, which is not, once again, assisted by sources.
As a side note, all figures presented have no source or authorship, so I presume the author created all them.
All in all, in spite of all issues, as the author chose reputable sources for critical areas in this work, some of them state of art, so I grade it sufficient.

Additional commentary and evaluation

Present your opinion to achieved primary goals of thesis, e.g. level of theoretical results, level and functionality of technical or software conception, publication performance, experimental dexterity etc.

The overall theoretical production is sufficient, yet it lacks academic traces such as more referencing. The author indeed creates a hardware design, which is at least simulation capable.

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REVIEWER'S OPINION OF FINAL THESIS

Overall, the author hit major requirements, as producing a logical text, at least with some reputable sources being referred to, with technical development of a digital circuit in an FPGA, yet the author did not crave to going beyond the ordinary expectation.

III. OVERALL EVALUATION, QUESTIONS FOR DEFENSE, CLASSIFICATION SUGGESTION

Summarize thesis aspects that swayed your final evaluation. Please present apt questions which student should answer during defense.

Guided by the technical knowledge regarding FPGA devices, adjacent theories of embedded electronics, and a working model of microprocessor IP for critically timed applications, the author aimed to have a working platform for it and then to run benchmarks and make analysis over it.
The softcore was indeed generated, and yet the text suggested it is not a fully functioning model on FPGA, the author simulated the execution of benchmarks in the processor, which is a good realization, as the FPGAs are not the friendliest platform to work on.
While it held technical accomplishments, and the text is quite logically ordered, the quality of this work is diminished by missing references of reputable sources in many sections, and it is rather the norm than the exception. This work is also devalued as a comprehensive discussion of the results is just missing.
As the author tackled imperative requirements, as producing a logical text, at least with some reputable sources being referred to, with technical development of a digital circuit in an FPGA, yet the author did not crave to go beyond the ordinary expectation, I evaluate this thesis as sufficient.
For the defence of this theses, it is suggested to ask the author (1) what were the adjustments made to the softcore so it could work on the FPGA; (2) what else the results of the benchmarks which were simulated in the softcore brings to this work, or were them only supposed to show that the softcore works and that there are different styles of benchmark with different time spans; (3) please elaborate on what programming language (assembly, C or even higher level languages) you would prefer to program this softcore, to achieve strict timing, and why?

I evaluate handed thesis with classification grade **E - sufficient.**

Date: **25.8.2021** Signature: