THESIS SUPERVISOR'S REPORT

I. IDENTIFICATION DATA

Thesis title:	**Graphical RISC-V Architecture Simulator – Instructions Decode and Execution and OS Emulation**
Author's name:	**Max Hollmann**
Type of thesis :	bachelor
Faculty/Institute:	Faculty of Electrical Engineering (FEE)
Department:	Department of Cybernetics – K13133
Thesis reviewer:	Ing. Pavel Píša, Ph.D.
Reviewer's department:	Department of Control Engineering - K13135

II. EVALUATION OF INDIVIDUAL CRITERIA

Assignment challenging

How demanding was the assigned project?

The stable and user-friendly processor simulator is crucial for Computer Architectures course students. The thesis goal was part of our aim to switch the QtMips simulator to RISC-V ISA, specially switch the instructions description, execution phases and pipeline stages, update mechanism for exception resolution and adapt system calls to match RISC-V Linux kernel subset. The original project is result of years of development and changes in the core part of it required to familiarize with 23 kLOC of the original code base, which involves understanding Qt5 used for graphics, C++ combined with user logic and low-level model and behavior of the simulated CPU.

Fulfilment of assignment fulfilled with major objections

How well does the thesis fulfil the assigned task? Have the primary goals been achieved? Which assigned tasks have been incompletely covered, and which parts of the thesis are overextended? Justify your answer.

1. *Familiarize with RISC-V processor architecture and respective standards and actual textbook.*
   Student presented ability to quickly understand even to complex topics. He has been well prepared for the task and has previously studied a number of books and articles based on his interest in computer architectures.
2. *Design and implement solution (utility program) to transform instruction set description in QEMU or other source into tables required to decode RISC-V instructions.*
   The step to implement tool which processes instructions specification and generates at least skeleton of the instruction decoding tables has been skipped. Manually filling in basic tables may be reasonable choice for initial minimal instruction subset implementation but tool will be missed when instruction set is extended. C-compress extension is necessary to execute GNU/Linux code of typical real RISC-V implementation, operations on CSR registers are missing. It is possible that floating point instructions will be implemented during some followup project, theses. It would be tedious and error prone work and that is why tool needs to be implemented anyway. There are reasonable sources of required information.
3. *Re-implement pipeline stages, ALU and other core components to match RISC-V architecture and referenced textbooks*
   MIPS influenced control signals has not been fully revised (i.e. IMF_REGD, IMF_PC_TO_R31) and are misleading in RISC-V case. At least analysis what needs to be implemented to support XLEN 32 is missing. Signaling between visualization and core has issues to highlight correct instructions in some cases. HI and LO registers are another leftovers, same as MIPS specific coprocessor 0. I cannot trace any attempt of the thesis author to update comprehensive test suite for the processor core. Even if all implementation is correct then missing tests are debt to prevent future inevitable regressions when some other students/developers start to contribute the project.
4. *Implement basic subset of machine control registers required for system calls and exceptions processing*
   Exceptions recognition and processing has been slightly updated to withstand pre-fetching of invalid instructions which do not reach memory stage due to flush. But it seems that no effort has been invested to update interrupt processing for requests incoming from peripherals.
5. *Implement subset of Linux kernel system calls emulation*
   System calls has been updated to match RISC-V calling convention. Previous author's work on unification of

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terminal and file accesses by QFile interface has not been integrated. There is reported some older Qt5 version as the blocker for the work but there is no analysis what are possible workarounds.

Activity and independence when creating final thesis — C - good.

Assess whether the student had a positive approach, whether the time limits were met, whether the conception was regularly consulted and whether the student was well prepared for the consultations. Assess the student's ability to work independently.

The student has showed interest in processor principles and design from the start of his bachelor studies. He has been active for years, visited with us processor designers in Brno, studied books and discussed the topics. But actual performance has been highly influenced by late starting of the preceding individual project, which can be partly excused by his stay abroad and general situation. But late work in the last semester has blocked his colleague working on visualization and result is that many parts received minimal testing and are unfinished.

Technical level — B - very good.

Is the thesis technically sound? How well did the student employ expertise in his/her field of study? Does the student explain clearly what he/she has done?

The student proved to have expected knowledge in computer systems area and programming. But postponing of the work and finishing it in a hurry has result in many leftovers, caused quite a lot of inefficiently spent time by his colleagues and delayed the project and lowered it chance to compete to other similar ongoing projects.

Formal level and language level, scope of thesis — A - excellent.

Are formalisms and notations used properly? Is the thesis organized in a logical way? Is the thesis sufficiently extensive? Is the thesis well-presented? Is the language clear and understandable? Is the English satisfactory?

The English language is at appropriate level for technical writing.

Selection of sources, citation correctness — A - excellent.

Does the thesis make adequate reference to earlier work on the topic? Was the selection of sources adequate? Is the student's original work clearly distinguished from earlier work in the field? Do the bibliographic citations meet the standards?

References (20 items) provide valuable list of pointers for documentation and projects required for start and continuation of work in the area.

Additional commentary and evaluation (optional)

Comment on the overall quality of the thesis, its novelty and its impact on the field, its strengths and weaknesses, the utility of the solution that is presented, the theoretical/formal level, the student's skillfulness, etc.

The project is step in a direction toward full switch of the simulator to RISC-V architecture but contributions of the author would require to be revised code to offer viable tool for wide range of computer architectures courses teaching.

III. OVERALL EVALUATION, QUESTIONS FOR THE PRESENTATION AND DEFENSE OF THE THESIS, SUGGESTED GRADE.

The thesis is a step to switch the currently used simulator QtMips to the RISC-V ISA (QtRvSim). The critical subset of assigned tasks to demonstrate RISC-V instructions processing have been fulfilled but is far to be complete.

The grade that I award for the thesis is C - good.

Date: **14.8.2021** Signature: