THESIS SUPERVISOR'S REPORT

I. IDENTIFICATION DATA

Thesis title:	**Graphical RISC-V Architecture Simulator - Memory Model and Project Management**
Author's name:	**Jakub Dupák**
Type of thesis :	bachelor
Faculty/Institute:	Faculty of Electrical Engineering (FEE)
Department:	Department of Cybernetics – K13133
Thesis reviewer:	Ing. Pavel Píša, Ph.D.
Reviewer's department:	Department of Control Engineering - K13135

II. EVALUATION OF INDIVIDUAL CRITERIA

Assignment — challenging

How demanding was the assigned project?

The stable and user-friendly processor simulator is crucial for Computer Architectures course students. The thesis goal was part of our aim to switch the QtMips simulator to RISC-V ISA, switch the memory model, adapt visualization, and update and enhance packaging. The project results from years of development and changes in the core part of it required to familiarize with 23 kLOC of the original base, which involves understanding Qt5 used for graphics, C++ combined with user logic and low-level model and behavior of the simulated CPU. Original memory model and emulated memory storage were insufficient for new host and target memory byte order combinations, and the requirement for unaligned accesses allowed by RISC-V ISA required a complete rewrite of this part. For visualization, the student has chosen a systematic approach and, instead of a minor adaptation of the original CPU core diagram, decided to switch to a completely new approach based on an external SVG-scene project, the task which has been planned only in long term perspective after this year projects. Project management, coordination work with another student was challenging as well. Instead of packaging update, the student decided to push the project forward and switch it to CMake build system.

Fulfilment of assignment — fulfilled

How well does the thesis fulfil the assigned task? Have the primary goals been achieved? Which assigned tasks have been incompletely covered, and which parts of the thesis are overextended? Justify your answer.

1. Familiarize with RISC-V processor architecture and respective standards and actual textbook.
   The student had read required books far before the start of the project and enrolled Advanced Computer Architectures course, where he implemented simple single cycle and simple pipelined RISC-V cores.
2. Redesign simulator memory model to allow its use for little-endian architecture, mapped filesystem files and 64-bit targets.
   The student has suggested and defended the redesign of the memory model architecture to separate front-end and back-end hierarchy. The designed solution allows to use memory model for both little and big-endian targets in all combinations of host and emulated devices byte ordering. It has been thoroughly tested by the test framework and even in the old MIPS simulator version, which has been extended for little-endian ELF binaries support.
3. Update visualization of the processor core.
   The visualization has been redesigned to a more flexible solution based on SVG. Connection to the core has been redesigned to lower a number of Qt signal-slot connections used and enhance performance.
4. Update documentation and packaging of the project.
   Basic documentation has been updated, and packaging has been overhaul and follows "quilt" packaging model for Debian, which was demanded by Debian developers. MAC OS, Windows, and many GNU/Linux distributions support has been updated, and some distributions support has been added. Update of some documentation waits for a companion project which is worked on by the second student.

Activity and independence when creating final thesis — A - excellent.

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Assess whether the student had a positive approach, whether the time limits were met, whether the conception was regularly consulted and whether the student was well prepared for the consultations. Assess the student's ability to work independently.
The student has interest in processor principles and design from the start of his bachelor studies. He has been active for years, visited with us processor designers in Brno, studied books and discussed the topics. He took active part in the project preparation and often suggested redesign far beyond my short and middle term plans so many solutions fulfill needs of long term project perspective.

Technical level	A - excellent.
Is the thesis technically sound? How well did the student employ expertise in his/her field of study? Does the student explain clearly what he/she has done?	
The student proved to have expected knowledge in computer systems area, programming, and code version control work. He proved an excellent level of analytical and programming skills, which is not only far above the expected level of the third-year Computer Sciences students but even specializations focusing on computer systems design.	

Formal level and language level, scope of thesis	A - excellent.
Are formalisms and notations used properly? Is the thesis organized in a logical way? Is the thesis sufficiently extensive? Is the thesis well-presented? Is the language clear and understandable? Is the English satisfactory?	
The English language is at an appropriate level for technical writing. The thesis provides a description of the original and student introduced solution of each area of his work.	

Selection of sources, citation correctness	A - excellent.
Does the thesis make adequate reference to earlier work on the topic? Was the selection of sources adequate? Is the student's original work clearly distinguished from earlier work in the field? Do the bibliographic citations meet the standards?	
References (23 items) provide valuable list of pointers for documentation and projects required for start and continuation of work in the area.	

Additional commentary and evaluation (optional)
Comment on the overall quality of the thesis, its novelty and its impact on the field, its strengths and weaknesses, the utility of the solution that is presented, the theoretical/formal level, the student's skillfulness, etc.
The project result is a sound base for the continuation of the project development and extension in a direction toward a not only crucial tool for Computer Architectures course but even Operating Systems education at our university and even worldwide.

III. OVERALL EVALUATION, QUESTIONS FOR THE PRESENTATION AND DEFENSE OF THE THESIS, SUGGESTED GRADE.

The thesis is a major step to witch the currently used simulator QtMips to the RISC-V ISA (QtRvSim). The assigned memory model, core visualization, and packaging tasks have been fully fulfilled with elegant solutions and the use and enhancement of appropriate techniques and libraries. Some of the achievements will be used even outside the project scope.

The grade that I award for the thesis is A - excellent.

Date: **31.5.2021** Signature: