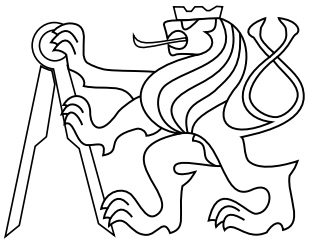
master's thesis

Design of High Power Converter with SiC MOSFETs

Jan Světlík



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MASTER'S THESIS ASSIGNMENT

I. Personal and study details

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Branch of study: **Sensors and Instrumentation**

II. Master's thesis details

Master's thesis title in English:

Design of High Power Converter with SiC MOSFETs

Master's thesis title in Czech:

Návrh výkonového měniče s SiC MOSFETy

Guidelines:

Design and implement a step-down converter controlled by a microcontroller with the use of high-voltage SiC transistors. The converter must operate at input voltage levels 400 V – 600 V DC and has to be able to deliver continuous output power up to 5 kW. Make analysis of the topic. Design simple control enabling the converter to operate in open loop as well as in closed loop with constant output voltage regulation. Propose simple communication with the microcontroller to allow configuration of basic parameters – switching frequency, dead time, output voltage. Test the dynamic behavior of the switching components under different input and output conditions.

Bibliography / sources:

[1] Erickson R., Dragon M.: Fundamentals of power electronic. 2nd eddition Norwell: Springer, 2001
[2] Abbateli L., Brusca C., Catalisano G.: AN4671 - How to fine tune your SiC MOSFET gate driver to minimize losses, STMicroelectronics, 2015
[3] Franklin G. F., Powell J. D., Emami-Naeini A.: Feedback Control of Dynamic Systems, Pearson Prentice Hall, 2003

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Date of master's thesis assignment: **12.02.2019** Deadline for master's thesis submission: _____

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III. Assignment receipt

The student acknowledges that the master's thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the master's thesis, the author must state the names of consultants and include a list of references.

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Date of assignment receipt	Student's signature

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Declaration

I declare that I worked out the presented thesis independently and I quoted all used sources of information in accord with Methodical instructions about ethical principles for writing academic thesis.

Abstract

Tato diplomová práce se zabývá návrhem výkonového měniče založeného na topologii typu synchronní buck. Měnič je zkonstruován s využitím MOSFET tranzistorů na bázi silikon karbidu. Tato práce se věnuje analýze měniče s cílem navrhnout a realizovat řídící jednotku umožňující jak zpětnovazební regulaci měniče, tak řízení v otevřené smyčce. Za tímto účelem je odvozen analytický model měniče coby dynamického systému, který je použit pro návrh a simulaci řízení. Kontrolní jednotka je implementována s využitím 32 bitového mikrořadiče založeného na architektuře ARM. V této práci je poskytnut popis a použití klíčových periférií mikrořadiče pro realizaci řízení. Na závěr jsou shrnuty výsledky měření dynamického chování výkonových tranzistorů při provozu měniče. Pozornost je především věnována měření proudu tekoucího jedním tranzistorem s využitím běžného rezistoru pro snímání proudu a kompenzaci frekvenční charakteristiky rezistoru.

Klíčová slova

Výkonový měnič, rozbor, návrh, řízení, SiC MOSFET

Abstract

This master degree thesis is concerned with the design of high power converter. The converter is based on synchronous buck topology and is realized using silicon carbide MOSFET transistors. This work deals with an analysis of such type of converter to design and realize a control unit providing feedback control of the converter. Therefore, a dynamic model of the converter is derived using a conventional technique of averaged state space modeling. The derived model is used for controller design and closed-loop control simulation. The control unit is implemented using a 32-bit ARM-based microcontroller. Hence, an insight into the microcontroller key peripherals is provided as well as a brief overview of the firmware architecture. This work concludes by a brief investigation of switching waveforms of SiC MOSFETs acquired during the converter operation. Attention is called to a transistor current measurement with a low-cost current sensing resistor and its frequency characteristic compensation.

Keywords

Power converter, analysis, design, control, SiC MOSFET

Contents

Abbreviations

List of abbreviations used within the text is here.

ADC	Analog to Digital Converter.
CCM	Continuous Conduction Mode or Core Coupled Memory, distinguished via context.
DAC	Digital to Analog Converter.
DCM	Discontinuous Conduction Mode.
DMA	Dirrect Memory Access.
DSP	Digital Signal Processing.
DTG	Dead Time Generator.
EMI	Electro-Magnetic Interference.
ESR	Equivalent Series Resistance.
FCCM	Forced Continuous conduction mode.
GPIO	General Purpose Input-Output.
HRTIM	High Resolution Timer, an STM32 peripheral dedicated for converter control and PWM generation.
IC	Integrated circuit.
IO	Input-Output of MCU or other IC.
LTI	Linear Time-Invariant, within the meaning of a dynamic system.
MCU	Microcontroller Unit.
MIMO	Multiple Input, Multiple Output, within the meaning of a dynamic system.
PCB	Printed Circuit board.
PLL	Phase Locked Loop.
PWM	Pulse-width Modulation.
SAR	Successive approximation analog to digital converter.
SISO	Single Input, Single Output, within the meaning of a dynamic system.
SMD	Surfave Mount Device.
SMT	Surfave Mount Technology.
TIM	General purpose timer, a hardware peripheral available in STM32 MCUs.
TUI	Terminal User Interface.
UART	Universal Asynchronous Receiver Transmitter.
USART	Universal Synchronus/Asynchronous Receiver Transmitter.
USB	Universal Serial Bus.

Symbols

Symbols used within the text are summarized here.

a_i	Coefficients of a continuous time transfer function denominator.
b_i	Coefficients of a continuous transfer function numerator.
s	Laplace transform operator.
z	Z-transform operator.
ω	Angular frequency in $rads^{-1}$.
j	Imaginary unit.
$\langle f(t) \rangle_T$	Cycle mean value of a periodic function of t over period T.
$\mathbf{x}(t)$	Vector of state variables of a dynamic system.
$\mathbf{u}(t)$	Vector of input variables of a dynamic system.
$\mathbf{y}(t)$	Vector of output variables of a dynamic system.
$C(s)$	Transfer function of a feedback compensator.
$G(s)$	Transfer function of a SISO dynamic system or a signal path.
$H(s)$	Transfer function matrix of a MIMO LTI dynamic system.
$L(s)$	Dot product of transfer functions of a feedback compensator and a dynamic system.
$T(s)$	Closed-loop transfer function.
$\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$	Main state matrix, input mapping matrix, output matrix and direct transfer matrix of a state space representation of LTI system.
$\mathbf{I}$	Identity matrix.
$e(t)$	Regulator error between a reference and regulated output quantity in the time domain.
$p(t)$	Output of the compensator in the time domain.
$E(s)$	Laplace image of regulator error between a reference and regulated output quantity in the time domain.
$P(s)$	Laplace image output of the compensator in the time domain.
$E(z)$	Z-Transform image of regulator error between a reference and regulated output quantity in the time domain.
$P(z)$	Z-Transform image output of the compensator in the time domain.
t	Symbol for time.
t_0	Symbol for time instant of initial conditions, i.e. $i_0 = i(t_0)$.
τ	Time constant $\tau = 1/\omega$ or alternative symbol for time used for integration.
$u(t), i(t)$	Time-varying voltage and current respectively.
U, I	Constant voltage and current respectively.
$\delta(t)$	Time-varying dutycle of a PWM signal.
δ	Constant dutycycle of a PWM signal.
$U(s), I(s)$	Laplace image of voltage and current respectively.
$U(z), I(z)$	Z-Transform image of voltage and current respectively.
R	Resistance.
r	Differential resistance.
L	Inductance.
C	Capacitance.
x	Arbitrary variable.
f	Frequency or a symbol for an arbitrary function, distinguished by a context.
$f(x)$	Arbitrary function of an arbitrary variable x.

T	Period of an arbitrary process, periodic or quasi-periodic signal.
T_S	Switching period of a converter operation.
$D_{CH(x)}$	ADC data word for an arbitrary channel x.
D_{CAL}	Calibration factor for the internal voltage reference of internal ADC.
D_{REF}	ADC data word for a channel monitoring internal voltage reference.
$U_{CH(x)}$	ADC input voltage at an arbitrary input channel x.
$U_{DA(x)}$	DAC output voltage of an arbitrary channel x.
f_{CLK}	Clock frequency.
f_{SYS}	System or core clock frequency.
f_{PLL}	Output frequency of a PLL.
f_{HTIM}	Clock frequency of HRTIM peripheral.
f_{ADC}	Clock frequency of ADC peripheral.
T_{SMP}	ADC sampling period of an input signal.
T_{SAR}	Time of a signal conversion by an ADC.
T_{ADC}	ADC conversion time.
$K_{X(Y)}$	Value of configuration register or bitfield X of an arbitrary peripheral Y, for example, value of period register of timing unit A of HRTIM is $K_{PER(A)}$.
K_P, K_I	Constants of a proportional and integral part respectively of a dynamic compensator.
$F(x)$	Static transfer function of an arbitrary quantity x.
S	Sensitivity of a static transfer function.
O	Offset of a static transfer function.
$\tan\delta$	Loss factor of the capacitor.
$\mathcal{R}_n$	Residue of a Taylor series of a function.
$\mathbb{W}$	Set of whole numbers.

1 Introduction

This diploma thesis aims to provide a design description of a high power converter. The converter is based on synchronous buck topology, and its primary purpose is to serve as a testing platform for a power MOSFETs on silicon carbide basis. The converter is intended to be used as a reference design for further developments as well as for performing several kinds of tests. One of the primary concerns is to make a platform for benchmarking and comparing SiC power MOSFETs. Another intention that gave rise to this project is to compare gate driving circuits and their performance in driving silicon-carbide MOSFETs.

The design of the power converter incorporates several levels of topics. This thesis is divided into the section to follow all the points met during the power converter design and development. The first topic is the design of the power stage of the converter. The power stage design includes the power magnetics, input and output filtering, transistor half-bridge and the disipated heat cooling mechanism. The other topic which is essential in term of this work is the open loop and closed loop control of the converter. For this purpose, a control unit based on an STM32 microcontroller is designed. The control unit is capable of sensing signals provided by the power stage prototype and needed for the closed loop regulation.

When speaking about a closed loop control of the converter, the problem of the control algorithm design and implementation comes forward. Concerning the closed-loop control design, an analysis of the converter has to be performed. The converter is modeled as a dynamic system using conventional techniques. The derived model of the converters dynamic behavior can be later used for the controller design as well as for simulation.

The last point of this work is performing specified tests with the use of the power converter. The necessary part is testing the functionality of the designed controller and the power stage itself. Moreover, special attention is put on switching characteristics of used power transistors as observing the switching performance of the power devices can be reflective of the converter design and mainly of its layout.

2 Synchronous buck based converter design

The power converter is based on the synchronous buck topology. The synchronous buck is one of the most basic topologies that is being used across different applications and different input and output conditions. It is a step-down converter. Hence it is capable of producing the output voltage only up to the input voltage level. Among other topologies, it is probably the most simple topology given the design as well as the control of the converter.

The synchronous buck or more generally the buck topology of power converters is applicable in a variety of applications. The usage of buck topologies starts from the low voltage and low power DC/DC converters used in different kinds of small electronics. The buck topology can also be seen in AC/DC converters or in auxiliary power supplies that do not require galvanic insulation. The buck topology can even be met in high power applications for instance in battery charging or industrial power supplies.

This chapter focuses on the buck converter analysis and design considerations. At the end of the chapter, the prototype of a high power synchronous buck converter is presented. The control unit, which design is the major part of this work, is designed based on the power stage design.

2.1 Analysis of the synchronous buck topology

The principle of operation of the synchronous buck converter is straightforward. The basic schematic of the converter is shown in Fig. 1. Two power switches T_1 and T_2 forms a half-bridge that is connected via an inductor to an output capacitor. The inductor and the output capacitor can be seen as a second order low pass filter that filters the switching harmonics of the half-bridge stage [1].

The basic buck converter is often used with one controlled power switch and a freewheeling diode. However, in low voltage application where high efficiency is targetted, the freewheeling diode is often accompanied by synchronous rectification. The synchronous rectification is commonly provided by a small on-state resistance field effect transistors to minimize the voltage drop when the low-side switch is conducting. In case of high power buck converters, a half-bridge of power switches may be used for lowering the conduction loses of the low-side switch, in case the forward voltage drop is significant.

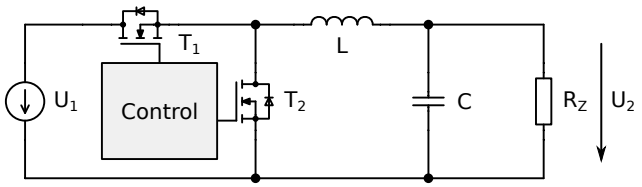
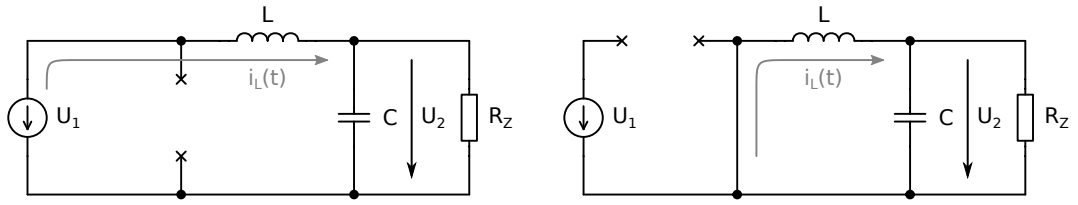


Figure 1 Basic schematic diagram of the synchronous buck topology



a) Equivalent circuit when the high-side switch is on

b) Equivalent circuit when the low-side switch is on

Figure 2 Equivalent circuits for both states of the synchronous buck converter

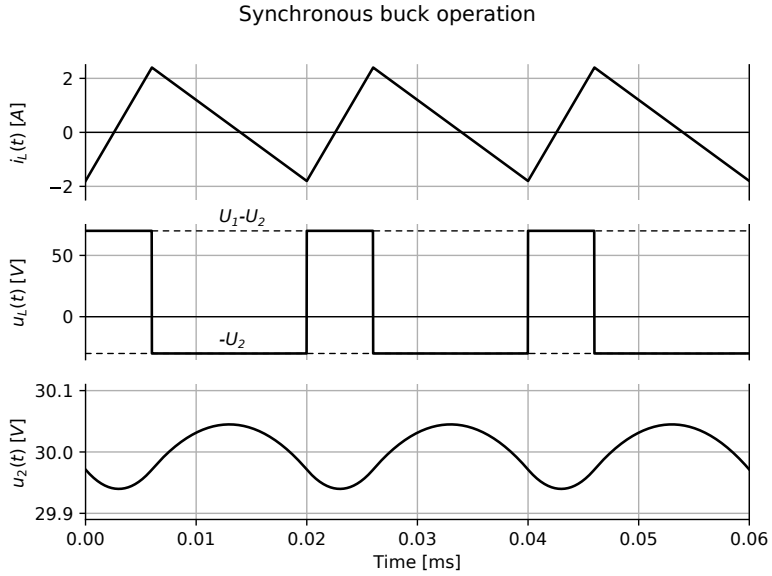


Figure 3 Waveforms of the inductor current, inductor voltage and the output voltage in steady state operation

2.1.1 Operation of the synchronous buck converter

The operation of the synchronous buck based converter can be divided into several time instants depending on the complexity of the final model. The simplest approach divides the converter operation into two subintervals. In each subinterval, one of the two transistors is switched on, and the other is switched off.

Fig. 2 shows the equivalent circuit during both states of the synchronous buck converter. Waveforms of the output capacitor voltage $u_C(t)$ and both, the inductor voltage $u_L(t)$ and inductor current $i_L(t)$ during the converter switching period are depicted in Fig. 3. The waveforms are reproduced at the converter steady-state operation for duty cycle $\delta = 0.3$.

The time interval $t \in (t_0, t_0 + \delta T_S)$, where t_0 denotes the time in which the high-side switch is turned on, T_S is the switching period and δ is duty cycle the converter operates with. It applies for the duty cycle $\delta \in \langle 0, 1 \rangle$. During the time instant when the high-side transistor is switched on, the inductor current starts flowing through the inductor into the output capacitor and to the output load as illustrated in Fig. 2a. Voltage $u_L(t) = u_1(t) - u_2(t)$ is applied to the inductor, which causes the inductor current to increase with approximately constant slope given by

$$\frac{di_L(T)}{dt} = \frac{u_L(t)}{L} = \frac{u_1(t) - u_2(t)}{L}. \tag{2.1}$$

The inductor current flows into the output load and simultaneously charges the output capacitor. The capacitor current can be expressed as follows

$$i_C(t) = C\frac{du_C(t)}{dt} = i_L(t) - \frac{u_C(t)}{R_Z}, \tag{2.2}$$

where R_Z is load resistance. This simple model neglects the capacitor series resistance R_C so it applies for the output voltage $u_2(t) = u_C(t)$. The symbol R_Z is used to annotate the load resistance instead of R_L as it could be confused with inductor series resistance used later in the text.

In a well-designed converter, the inductor and output capacitor values are proportional to the converter switching frequency to attenuate the switching harmonics. Thus the output voltage ripple is far lower than the output voltage in its mean value. Due to this assumption, the output voltage ripple can be neglected for the converter steady state evaluation [1].

During the second time interval $t \in (t_0 + dT_S, t_0 + T_S)$ the high-side transistor is switched off and the low-side switch starts conducting as depicted in Fig. 2b. During this time interval voltage $u_L(t) = -u_2(t)$ is applied to the inductor causing the inductor current to decrease with approximately constant slope

$$\frac{di_L(t)}{dt} = \frac{u_L(t)}{L} = -\frac{u_2(t)}{L}. \tag{2.3}$$

The capacitor current reamins the same as in (2.2).

At the beginning of the second time interval, the inductor current continues to flow into the output load and charges the output capacitor. MOSFET transistors can carry the drain current in both directions due to their body diode. This property makes the transistors behave as so-called two quadrant switches [1]. As a consequence, if the inductor current falls to the zero before the new switching period begins, it continues to decrease with a constant slope and becomes negative until the high-side switch is turned on again and a positive voltage is applied to the inductor.

This situation happens during the light load operation when the mean value of the inductor current $\langle i_L(t) \rangle$ is lower than the half of the inductor current ripple Δi_L. If the converter operates with inductor mean value higher than the half of the current ripple, the current remains positive until the next switching period begins. In both cases, the dynamic behavior of the converter remains the same. The operation of the synchronous buck is thus limited only to the so-called CCM (Continuous Conduction Mode). The state in which the inductor current ripple is higher than its mean value is sometimes referred to as an FCCM (Forced Continuous Conduction Mode) [2].

2.1.2 Continuous and Discontinuous Conduction Mode

If the converter is realized as a simple buck topology using a freewheeling diode, which behaves as one quadrant switch, the converter would be able of the DCM (Discontinuous Conduction Mode). The diode would allow the current flow only in the forward direction. In this case, at the moment in which the inductor is demagnetized, its current falls to the zero and the freewheeling diode stops conducting. At this moment the inductor current remains zero in its average value as the inductor voltage is zero as well. Considering the high-side MOSFET's drain-source capacitance C_{DS}, the inductor voltage and current starts oscillating as the current falls to zero. These decaying oscillations are caused by a series connection of the input capacitance, the drain-source capacitance and the inductor, which forms together with a series resonant circuit. The

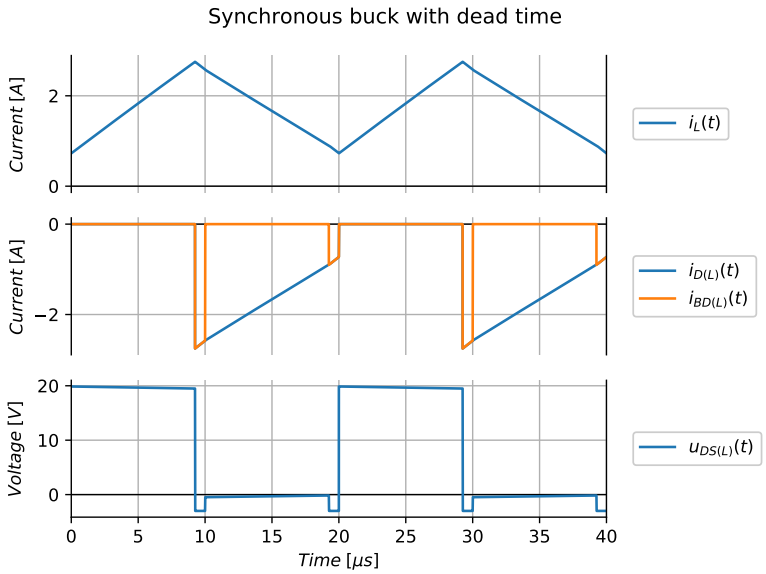


Figure 4 Schematic of the synchronous buck converter

DCM operation influences the converter behavior as it completely changes its static transfer function as well as its dynamic behavior. But this is not the case of the synchronous buck topology, so the modeling remains quite simple as described more in detail in section 4.2.

2.1.3 Extending the converter operation of a dead time

It is necessary to implement a deadtime before switching on the second transistor, while the first was switched off to prevent any cross-conduction between the transistors connected in a half-bridge configuration. The cross conduction could be caused by parasitic control signal overlapping. This overlapping can be induced for example by a pulse width distortion caused by a gate driver IC or by a phase distortion of the control signal path. The deadtime necessity is also caused by the fact that the transition from a conducting state to the closed state of the power transistor is not infinitely fast as discussed in chapter 7.

The waveforms of the converter operation with dead time are shown in Fig. 4. Note that the low-side transistor drain current $i_D(L)(t)$ is negative as per the two-port network convention. The $i_{BD(L)}(t)$ denotes the body diode current of the low-side MOSFET.

It can be seen from the waveforms that after the first time interval, when the high-side switch is turned off, a deadtime causes the inductor current commutation through the body diode of the low-side MOSFET transistor. During the second time interval, the situation is analogical, but it depends on the inductor current direction which of the two transistors body diode takes over the inductor current. If the current was positive, the low-side transistors body diode is conducting. Conversely, if the current was negative, which occurs when the half of the inductor current ripple is higher than its mean value, the body diode of the high-side transistor starts carrying the inductor current.

The body diode conduction during the dead time can significantly influence the converter efficiency as the SiC MOSFET body diode forward voltage is considerably higher compared to Si MOSFETs.

2.1.4 Steady State analysis of the synchronous buck topology

During the steady state operation of the converter, the total change in the inductor current between two neighbouring intervals, is zero [1]. It can be written for the inductor current $i_L(t_0) = i_L(t_0 + T_S)$. Solving the inductor current during first time interval $t \in (t_0, t_0 + \delta T_S)$ yields equation

$$i_L(t_0 + \delta T_S) = \frac{1}{L}\int_{t_0}^{t_0+\delta T_S} (u_1(t) - u_2(t))\, dt + i_L(t_0)\,. \tag{2.4}$$

Provided on the output voltage ripple is negligible compared to the mean value $\langle u_2(t)\rangle$ we can asume the output voltage to be constant $u_2(t) = U_2$. The input voltage can be supposed to be constant as well $u_1(t) = U_1$. In such case, we can write for the current in time $t = t_0 + \delta T_S$

$$i_L(t_0 + \delta T_S) = \frac{\delta T_S (U_1 - U_2)}{L} + i_L(t_0)\,. \tag{2.5}$$

Taking into account the solution of inductor current during the second time interval $t \in (t_0, t_0 + \delta T_S)$, when the low-side switch is conducting, we obtain for the current at the end of the second interval

$$i_L(t_0 + T_S) = \frac{1}{L}\int_{t_0+\delta T_S}^{t_0+T_S} -u_2(t)\, dt + i_L(t_0 + \delta T_S)\,. \tag{2.6}$$

Similarly, we assume both, the input and output voltages to be approximately constant. We get for the inductor current at the end of the second interval

$$i_L(t_0 + T_S) = \frac{-(1-\delta) T_S U_2}{L} + i_L(t_0 + \delta T_S)\,. \tag{2.7}$$

Since $i_L(t_0 + T_S) = i_L(t_0)$, we can substitute the inductor current at the beginning of the first interval by current at the end of the second interval. This yields equation

$$i_L(t_0 + \delta T_S) = \frac{\delta T_S (U_1 - U_2)}{L} + \frac{-(1-\delta) T_S U_2}{L} + i_L(t_0 + \delta T_S)\,. \tag{2.8}$$

Simplifying the equation and solving for δ gives the static transfer function for the buck converter

$$\delta = \frac{U_2}{U_1}. \tag{2.9}$$

For the converter design and component evaluation, it is essential to know ripple of the inductor current. In steady state, the current ripple can be expressed by

$$\Delta i_L = i_L(t_0 + \delta T_S) - i_L(t_0) = i_L(t_0 + \delta T_S) - i_L(t_0 + T_S)\,. \tag{2.10}$$

Replacing the inductor current values with particular solutions for steady state yields

$$\Delta i_L = \frac{(1-\delta) T_S U_2}{L} = \frac{\delta T_S (U_1 - U_2)}{L}. \tag{2.11}$$

Expressing U_2 from (2.9), we can rewrite the current ripple as follows

$$\Delta i_L = \frac{(1-\delta)\,\delta T_S U_1}{L}. \tag{2.12}$$

2.1.5 Estimating the converter parameters

The testing platform is supposed to be loaded by a resistive load of a constant value since there is no other type of electric load available in the laboratory, that would be able to dissipate such power. The maximum values of the inductor current, output voltage, and the current ripple can be specified according to the used type of load and for the boundary operating conditions.

The power converter is intended to be used across different conditions, including various values of the power inductor. Moreover, the power transistors can be exchanged. This versatility has led in specifying the boundary values of the testing platform fitted with one type of power transistors. This configuration was used as a reference design using it for determining the component values and operating ranges in conjunction with the control unit design.

Since the output load is a resistive load with a constant value, the maximum output voltage is limited by the value of the load resistance and the output power. The load resistance is $R_Z \approx 28\ \Omega$. The maximum output voltage at maximum output power is then given by $U_{2MAX} = \sqrt{P_{2MAX} R_Z}$. The maximum mean value of the output current is given by

$$I_{2MAX} = \sqrt{\frac{P_{2MAX}}{R_Z}}. \tag{2.13}$$

The mean value of inductor current is approximately the mean value of the output current in steady state operation of the converter. The absolute peak value of the inductor current is selected according to used power transistors. In the case of the reference design, SCT20N120 MOSFETs were used. These are SiC MOSFETs capable of 1200V drain-source voltage and 20A drain current. Based on the first quadrant characteristics provided by the devices datasheet, the maximum peak value of the inductor current was chosen to be approximately 19A. This value was evaluated as the maximum concerning the gate driving voltage $U_{GS_H} = 18\ V$ and taking into account the worst case operating conditions, i.e., the junction temperature $\vartheta_C \approx 150\ ^\circ C$.

Based on the chosen operating values, the maximum peak current, and the output current, the minimum inductor value for a given switching frequency can be evaluated. Since the switching frequency is going to be configurable as described in the control unit design description, the reference power stage design will focus on the minimum operating frequency that was chosen to be $f_{SW_{MIN}} = 45\ kHz$. Using the relationships derived in the previous section the minimum value of the power inductor is given by

$$L_{MIN} = \frac{(1 - \delta_{MAX})\, U_{1_{MAX}}}{\Delta i_{L_{MAX}} f_{MIN}}. \tag{2.14}$$

The converter parameters are sumarized in Tab. 1.

Parameter	Value	
Maximum output power	5	kW
Output load rezistance	≈ 28	Ω
Maximum peak current	19	A
Mean value of inductor current	$\doteq 13.4$	A
Maximum alowed current ripple	$\doteq 11.3$	A
Minimum inductor value	296	μH

Table 1 Summary of converter operating conditions

A high power inductor made up of two stacked E70 ferite cores of total inductance 300 μH was used. The key parameters of used inductor are sumarized in Tab. 2.

Parameter	Value	
Nominal inductance	300	μH
Number of turns	24	
Maximum peak current	30	A

Table 2 Key parameters of the power inductor

2.2 Prototype of the converter power stage

It has taken quite some time since the very first prototype of the testing platform. The actual power stage design was developed based on knowledge acquired during the development of the previous prototypes and experiments that have been made so far.

Since the converter is supposed to be used as a testing platform for SiC MOSFET transistors, it was a primary concern to design the converter taking into account a certain degree of versatility. The purpose of the converter unit is to provide a platform for comparing ST's solutions of SiC power MOSFETs with competitive products. It is then essential to make the design in such a form that will allow relatively easy and fast replacement of the discrete parts without the need of completely disassembling the whole converter. The converter also has to be easily accessible for the test equipment and probes in the purpose of data acquisition and performing different kinds of measurements. As a subject to this requirement, the design is only limited to the PCB without providing any covering box. The power module is alternatively placed in an outer cover or shield on a laboratory bench.

The second reason for developing this kind of testing platform is to make a comparative analysis of different types of gate driving circuits in the purpose of observing their capabilities in driving SiC MOSFETs. Since the SiC MOSFETs exhibit slightly different characteristics compared to ordinary Si power MOSFETs, it is needed to perform several tests before using regular gate drivers designed for driving Si MOSFETs or IGBTs for driving the SiC devices. The main interest is in identifying the switching characteristics and performance and transient immunity of the gate driver circuitry. Based on this requirement, it is desirable to make the gate drivers in forms of modules that can be easily replaced. However, speaking about the transient behavior of the SiC MOSFETs and their switching performance, it is essential to design the transistor gate-driving circuitry in a way that will not influence the converter's operation. As the transients in the SiC MOSFET based converter can be very fast producing high voltage and current slopes, the control logic and circuits can suffer a high level of EM interference, both the conductive and the radiated. The EM interference is even more significant in case the converter is operating with hard switching. In such a case, special care needs to be taken to optimize the design even in case the gate drivers are in the form of replaceable modules. Isolated power supplies for the gate drivers are designed in the way of replaceable modules as well.

The converter is based on synchronous buck topology, thus using two power switches in a half-bridge driving a power inductor. It was decided to design the PCB of the power module only for the transistor half-bridge, making it possible to test the power switches under various conditions including different types of power inductor. Hence, the power inductor is not included on the main board but is connected externally using

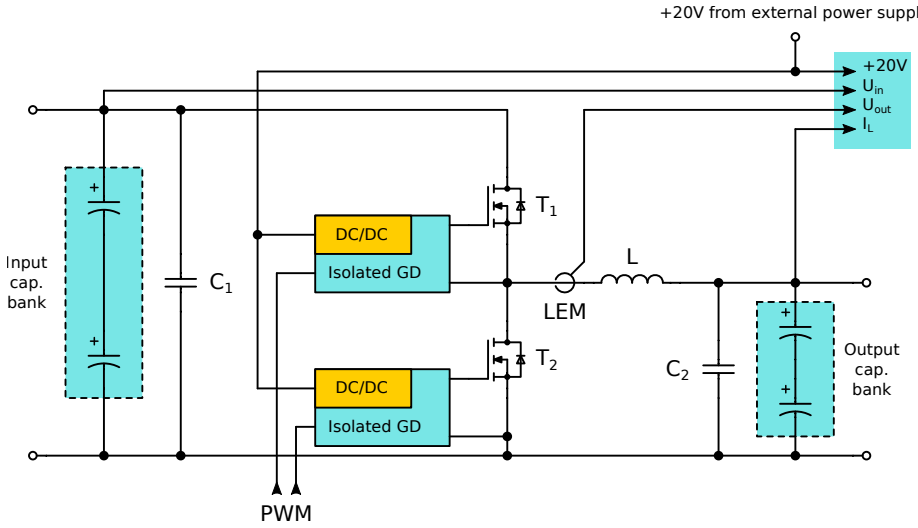


Figure 5 Block diagram of the converter power stage

high current terminals. The power module layout incorporates space for input and output capacitor bank, heatsink of the half-bridge, current transducers and a place for the gate driver modules.

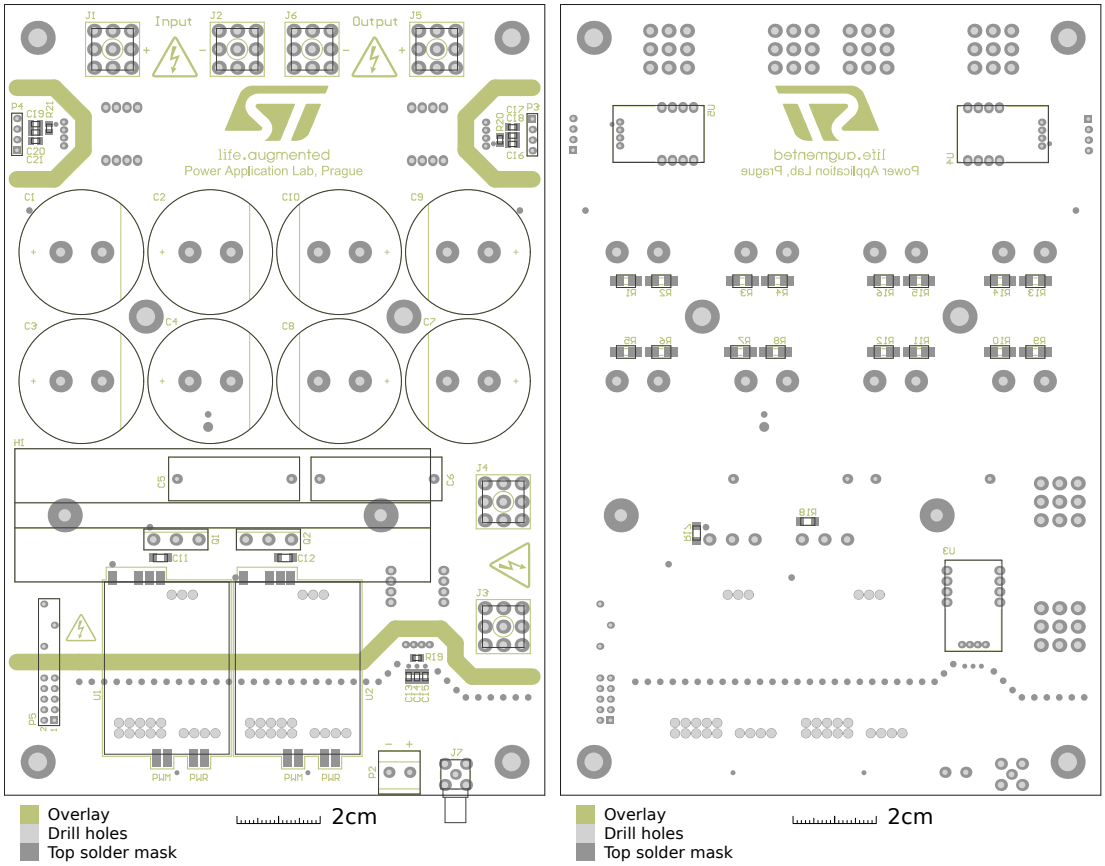
2.2.1 Power stage of the converter

The power stage consists of the output and input sections, the half-bridge with a heatsink and a primary side. The primary side is galvanically insulated from the power section and is mainly used for power distribution to the gate drivers and the control unit interface. The power stage also provides a current transducer used for measurement of the inductor current. Block diagram of the converter unit is shown in Fig. 5. The input voltage, output voltage and the signals from the inductor current sensor are provided on a connector that serves as an interface to the control unit.

Some place is reserved for input and output current sensors. However, their placement is optional since they are not used for the converter control as described in chapter 4. Hence, only the inductor current transducer signals are provided on the control unit connector. The design drawings of the power stage are shown in Fig. 6.

The input capacitor bank is made up of two in parallel connected sets of two aluminum electrolytic capacitors connected in series. The series connection is used to increase the maximum output and input voltage limits. However, the capacitors are not ideal and may suffer relatively high leakage currents that can vary significantly piece-to-piece, hence balancing resistors are added in parallel to each capacitor. The voltage balancers are placed on the bottom side of the power stage board as can be seen in Fig. 6b. The parallel connection of the capacitors is used for increasing the overall capacitor bank capacity and for reducing the equivalent series resistance of the filter. The same configuration is used for the output capacitor bank.

The foil capacitors C_5 and C_6 are placed on the top side of the power stage PCB under the heatsink as can be seen in Fig. 6a. Especially the input blocking capacitor C_5 is placed as close to the transistor half-bridge as possible. This capacitor is a part of the converter's critical loop as described more in detail in the following sections. A photo of the converter power stage together with the control unit can be seen in Fig. 106 in Appendix C.



a) Design drawing of the top side of the power stage

b) Design drawing of the bottom side of the power stage

Figure 6 Design drawings of the power stage of the converter

2.2.2 Hardware and layout considerations

The switching performance of high voltage SiC MOSFETs is far beyond the capabilities of IGBTs. Comparing the SiC devices rated below 1kV with ordinary Si MOSFETs, the transient dynamics can be much faster in case of SiC thanks to very fast current commutations through the SiC body diode as described more in detail and proved by measurements in chapter 7. These fast transients make the PCB layout more demanding than in case of slow devices. It is crucial to pay special attention to minimize stray inductances of any routes that are exposed to high di/dt. It is also mandatory to minimize inductances common for gate driver loop and the drain-source current.

Any conductor in the proximity of another conductor can be seen as an electrode of a parasitic capacitor. If the conductor is connected to a changing potential, its parasitic capacity to other conductors causes small current, depending on the relative area of the conductor, to flow between the neighboring conductors. Due to very high du/dt that can reach several tens of volts per nanosecond, the area of any floating conductor should be minimized. The amount of capacitive coupling can be high and can lead to malfunction of other devices operating at logic level voltages or parts sensitive to electromagnetic interference.

One of the most significant issues, when designing the converter, is the heatsink of the power transistors. It is practically impossible to operate the designed converter under its specified input voltage and output power while leaving the heatsink floating.

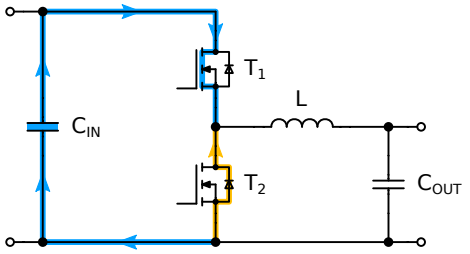
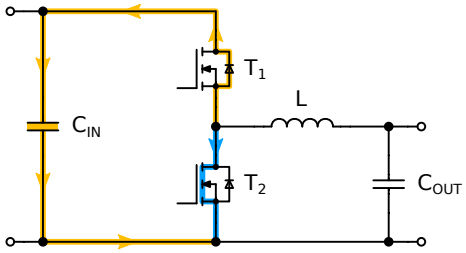
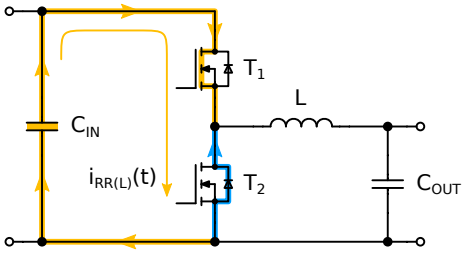


Figure 7 Schematic diagram of the current commutation during the high-side transistor switch off transient



a) Current commutation within the critical loop when $\Delta i_L/2 > \langle i_L(t) \rangle$



b) Current commutation within the critical loop when $\Delta i_L/2 < \langle i_L(t) \rangle$

Figure 8 Schematic diagram of the current commutation at the end of the second subinterval

The floating heatsink behaves like a floating electrode of a stray capacitor. Hence it is mandatory to couple the heatsink with any fixed potential either directly or capacitively for high frequencies only.

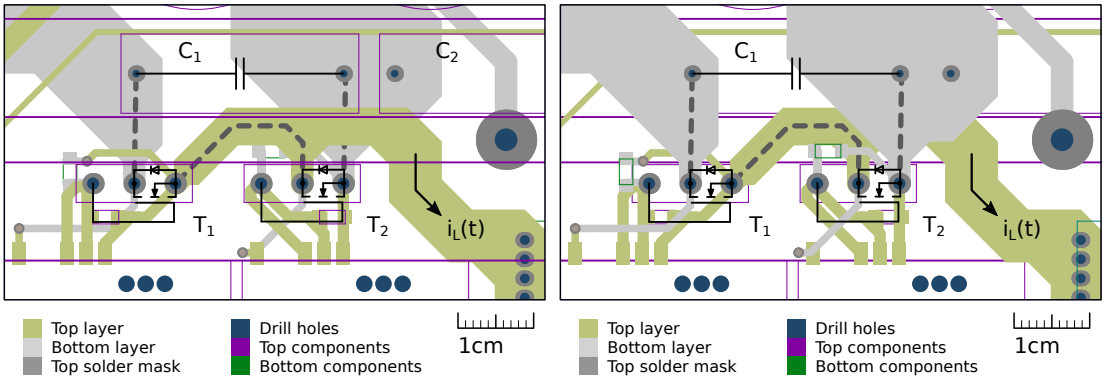
Besides the heatsink grounding, the total area of the half-bridge middle point should be minimized. Since the inductor is connected externally, this requirement is not fulfilled strictly. However, the external connection of inductor allowed significant reduction of critical loop inductance which is being discussed in the following section. At this point, at least the conductor length to the power inductor should be as short as possible. It is also preferable to connect the outer side of the inductor winding to the output, leaving the floating terminal deeper in the inductor winding.

Critical loop inductance

One of the most important things is to minimize parasitic inductances of conductors that are exposed to high di/dt. In case of the synchronous buck topology, the critical loop is formed by the input blocking capacitor, the transistor half bridge, and interconnecting paths. All the inductances distributed over the critical loop adds together and forms a voltage drop during switching transients.

Fig. 7 depicts the directions of currents distributed within the critical loop, and the inductor current commutation during the high-side transistor is switched off. The orange color highlights the conductor where no current has flown before the transient. After the switch-off, it started increasing and flowing in the direction of the arrows. Conversely, the blue color stands for a current that has flown through the conductor and dropped to zero.

In synchronous buck topology, after the first interval in which the high-side switch is conducting, the current is always positive during the steady state operation of the converter. As the high-side switch turns off, the body diode of the low-side switch takes over the inductor current.



a) Top view of the critical loop layout **b)** Bottom view of the critical loop layout

Figure 9 A cut-out of the critical loop layout

During the switch off transient of the low-side transistor, the situation is split into two cases. In the first case, if the inductor current has fallen to the zero and became negative, the current commutes through the body diode of the high-side switch when the low-side transistor is turned off. The process is roughly depicted in Fig. 8a.

If the inductor current at the end of the second subinterval is still positive, the inductor current continues to flow through the low-side transistor body diode until the high-side transistor is switched on. As soon as the high-side transistor is switched on, it takes over the inductor current as shown in Fig. 8b. In addition, a reverse recovery current of the low-side switch body diode $i_{RR(L)}(t)$ starts flowing through the half-bridge. This current has a nature of short spike that decays as soon as the recovery charge of the body diode is discharged. A more detailed description of the switching transients is provided in chapter 7.

The layout of the critical loop on the power stage is depicted in Fig. 9. The input blocking capacitor is high-voltage, low ESR foil capacitor. It is a double metalized polypropylene capacitor with a very low loss coefficient — $\tan\delta$. Key parameters of the capacitor are summarized in Tab. 3.

Parameter	Value	
Capacity	220	nF
Parasitic inductance	≈ 23	nH
Disipation factor	$\leq 6 \cdot 10^{-4}$	–
Equivalent Series Resistance	≤ 43	$m\Omega$
DC voltage rating	1000	V

Table 3 Key parameters for the critical loop blocking capacitor, data source [34]

The bold dashed line marks the critical loop in the power stage PCB layout cut-outs shown in Fig. 9. It can be seen, the input and output foil capacitors are placed as close as possible to the half-bridge to minimize the stray inductances. The most critical is the input blocking capacitor placement. The parameters of the critical loop inductance were estimated on the prototype of the power stage PCB as discussed more in detail in section 2.4.

The parasitic properties of the critical loop significantly influence the switching performace of the MOSFET transistors especially, by influencing the drain-surce voltage blocked by the transistors.

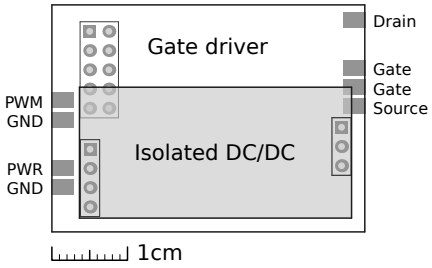


Figure 10 Design drawing of the gate driver module with isolated DC/DC

2.3 Gate drivers of the power transistors

The high-side transistor requires a floating gate driver as it is driven against the source that is connected to the middle point of the half-bridge. The transistors in the half-bridge are both provided with the same galvanically isolated gate driver. The low-side switch does not need the floating gate driver. However, it is good practice to include the same gate driver circuit in the high-side and the low-side transistor to make the transport delays equal. It also provides galvanic insulation of the control logic ground and ground of the power stage. As mentioned before, the gate drivers are made in the form of modules that are placed on the power stage PCB in front of the power transistors. These modules lie on the main PCB and are connected with dedicated solder pads to minimize the distance from the power transistors. Design drawing of the gate driver module with a DC/DC on top of it is shown in Fig. 10.

The gate signal is split into two paths. One path is used for driving the transistors in a standard way, with a series resistance provided to limit the peak current into the transistor gate. The other path provides a separate track for gate driving circuits featuring so-called Müller clamp functionality. This functionality is described more in detail in section 2.3.1. The Müller clamp track is routed separately directly to the transistor gate to minimize the shared stray inductance with the standard gate path. There is also a small capacitor connected between the gate and source of the transistor. The capacitor is placed as close as possible to provide a low impedance for high-frequency. The ceramic capacitor helps to suppress spikes at the transistor gate that could arise due to high du/dt and capacitive coupling. It also provides some limited improvement in case of current injected through the Müller capacity of the transistor.

At the primary side, the gate driver is equipped with two input ports. One port is used for power distribution to power up the gate drivers and their isolated DC/DC converters. The other port is input for the PWM signal. It is common for both, the high-side and the low-side transistor. The first gate driver modules implemented two configurable logic invertors for providing a complementary signal. This approach was used to drive the power converter with a single PWM from a signal generator at the beginnings of the converter development as there was no control unit to provide the complementary PWM signals.

The gate driver module provides header type connectors for connecting the DC/DC converter. The DC/DC module is placed on the top of the gate driver module as shown in Fig. 10.

2.3.1 Automotive grade, galvanically insulated gate driver STGAP1AS

The first gate driver module is based on STGAP1AS circuit. It is a galvanically isolated automotive grade gate driver IC [28]. STGAP1AS is a sophisticated gate driver imple-

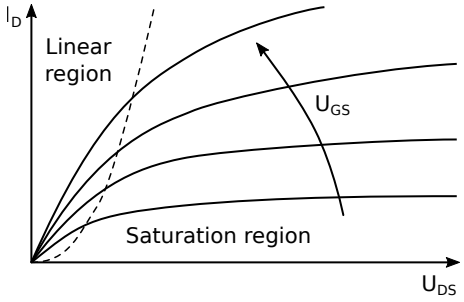


Figure 11 The output characteristic of the MOSFET transistor

menting a variety of functions and protections. The gate driver is equipped with an SPI interface used for the configuration of the gate driver functions. The STGAP1AS can be driven by two complementary signals, where the first is the active signal for the power switch driven by the gate driver IC, and the other is from a gate driver of the complementary power switch.

The gate driver circuit implements hardware interlocking. The interlocking feature is provided by a state machine that turns the gate driver output into a safe state in case the input signal overlapping is detected [28]. It also incorporates an internal deadtime generator. The deadtime generator is disabled by default and must be configured by the SPI interface. The deadtime generator provides three values of dead time duration. The deadtime length is set via writing a particular value into the device's configuration register.

Among the driving signal related protections, STGAP1AS also implements some secondary stage protections such as desaturation protection, the Müller clamp feature or overcurrent protection. The gate driving circuit also provides an under voltage lockout that turns off the gate driver in case the secondary side supply voltage drops below a certain threshold [28]. The threshold of the under voltage lockout can also be configured using the configuration registers of the device.

The desaturation protection

The desaturation protection is used to protect the power switch from damage due to a high current that could lead to the power switch saturation. In case the MOSFET transistor is entirely switched on and is operating in the linear area of its output characteristic, refer to Fig. 11[1], the drain-source voltage drop is given mainly by the on-state channel resistance. If the MOSFET transistor enters the saturation region, the drain current starts to be limited by the transistor transconductance, so the drain-source voltage starts to increase more rapidly as the output resistance is rising. This further voltage increase causes higher conduction losses, and due to increased power dissipation, the transistor can be damaged.

The STGAP1AS allows monitoring the drain-source voltage during the on-state of the power switch. As shown in a schematic diagram in Fig. 12, the *DESAT* pin of the gate driving circuit sources a small current into the power transistor drain. The voltage drop among the output of the *DESAT* pin is internally connected to a comparator. In case the power switch gets into the saturation region, the voltage drop among the *DESAT* pin increases and the comparator turns on the desaturation protection. The diode D_1 is used to block the off-state drain-source voltage.

[1]The output characteristic is only an illustration and may be disproportionate to a typical high voltage MOSFET output characteristic

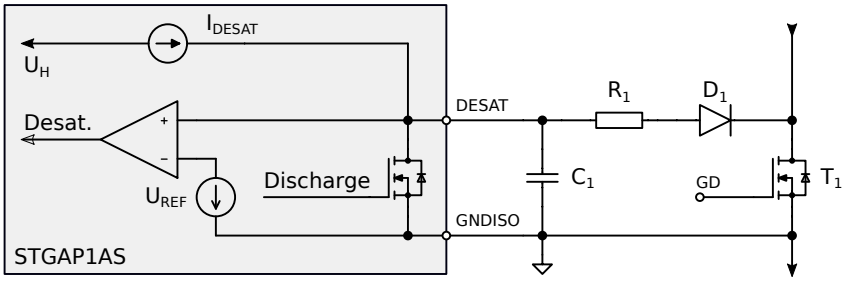


Figure 12 Schematic diagram of the desaturation protection usage [28]

Adding the RC low-pass filter helps to prevent false desaturation protection triggering during the switch-on or switch-off transients. The RC filter works as a simple blanking circuit. The blanking capacitor is discharged during the MOSFET off-state. If the MOSFET is switched on, the blanking capacitor is being charged with a slope given by the internal current source until it reaches the MOSFET on-state drain-source voltage. At this point, the current starts flowing through the diode D_1 and the voltage on the *DESAT* pin is given by the drain-source voltage of the power transistor.

Gate driver output stage and the Müller clamp protection

The gate driving circuit provides two separated outputs for sink and source. The split gate driving output allows for adding different impedances for the switch-on and switch-off transient of the power switch. This method can be used for instance in case of soft switching when there is no need for fast charging/discharging the transistor's gate-source capacity, which helps to reduce the current spikes within the gate-driving loop. There is also a third output for the Müller clamp feature. This output is used for connecting the gate of the power transistor to a lower driving voltage through a low impedance. This functionality helps to suppress voltage peaks between gate and source caused by current injection through the parasitic Müller capacity.

Fig. 13 shows the schematic diagram of the STGAP1AS driving stage. Note that it is only principal schematic that does not show the exact internal structure of the gate driver.

Fig. 13 also shows the possibility of using a split power supply for powering the STGAP1AS. It can be used to switch off the power MOSFET with a negative off-state voltage level. The negative driving voltage is applied to speed up the discharging of the gate-source capacitance when the gate-source voltage crosses the threshold level of

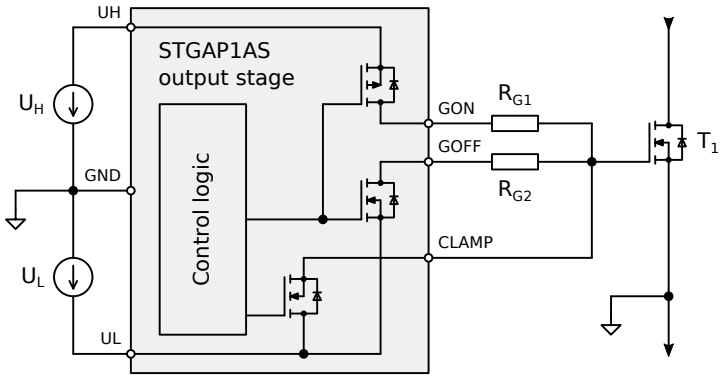
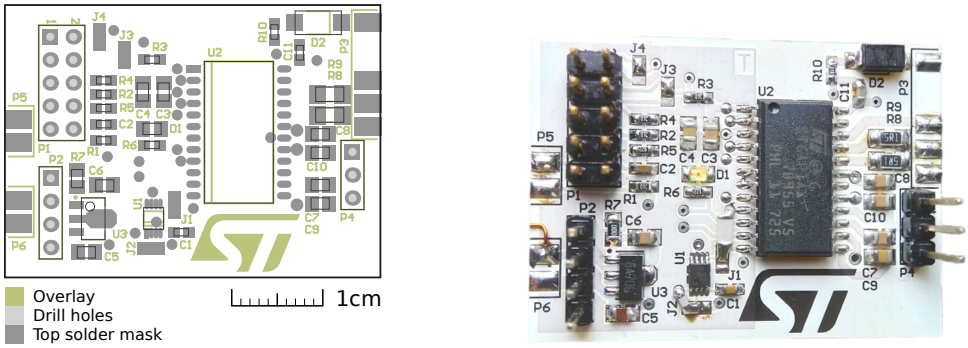


Figure 13 Schematic diagram of the Müller clamp feature [28]



a) Design drawing of the gate driver module **b)** Image of the assembled gate driver module

Figure 14 Design drawing and a photo of the STGAP1AS based gate driver module

the power transistor. The negative off-state voltage can also be profitable when using SiC-based MOSFET transistors since the negative gate-source voltage helps to decrease leakage current of the transistor significantly [9].

The STGAP1AS based gate driver module is used in the way that one PWM signal is fed into both the high and the low-side gate driver. A configurable signal inverter is added to the gate driver to create the complementary signals directly on the gate driver module. As stated earlier, this approach was used at the beginning of the converter development since there was no control unit. The gate drivers were driven by a standard PWM signal from a signal generator. The STGAP1AS driver was used to generate the dead time in this version.

Fig. 14a shows the design drawing of the STGAP1AS gate driver module. Note the connectors *P2* and *P4* serve for connecting the isolated DC/DC as mentioned earlier. The connectors *P3*, *P5*, and *P6* are the solder pads that are used to connect the gate driver module to the power stage. A photo of the assembled gate driver can be seen in Fig. 14b.

The gate driver is powered via a linear voltage regulator from an external power supply used for powering the converter driving circuits.

2.3.2 Galvanically insulated gate drivers based on STGAP2

The STGAP2 is a lightweight version of the previously described gate driver in a smaller package with fewer pins. The STGAP2 is not an automotive grade and lacks several functions compared to the previously described integrated circuit. It does not provide any communication interface. Moreover, there is no desaturation protection and no possibility of built-in overcurrent protection. The gate driver still uses two separate inputs, one for the active signal and one for the complementary signal and provides hardware level interlocking in case of erroneous driving signals [29]. But the STGAP2 does not implement an internal dead time generation; thus the dead time has to be guaranteed by the control signal.

The STGAP2 is available in two versions, the first version marked by S is with two separate driving outputs, one for sink and the other for source. This split output can be used when a different driving impedance for the switch-on and switch-off is needed. The other version marked by SC uses the previously described Müller clamp feature but only one driving output common for driving the gate-source to the high and the low level. In such a case, if the different switch-on and switch-off impedances are required, an external diode can be used as depicted in the schematic diagram shown in Fig. 15.

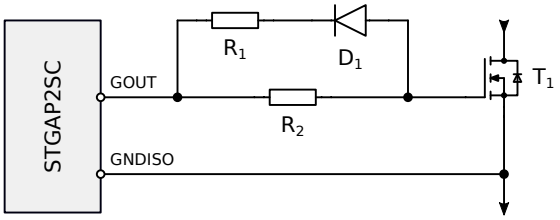
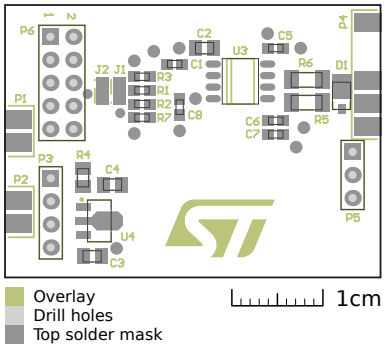
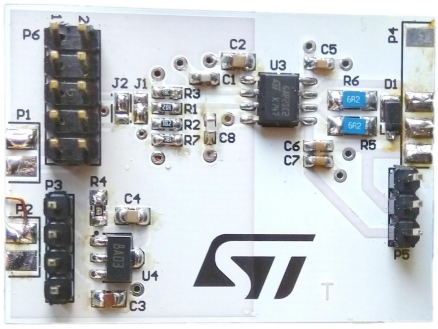


Figure 15 Schematic diagram of a diode bypass



a) Design drawing of the STGAP2SC based gate driver



b) Photo of the assembled gate driver module

Figure 16 Design drawing and photo of the STGAP2SC based gate driver module

The STGAP2 also does not explicitly support the split power supply. In case the off-state gate-source negative voltage level is required, the middle point of the split power supply is connected to the source of the power MOSFET only. Therefore it is mandatory to split the blocking capacitor as it was in case of the split power supply.

The realization of gate driver variant with Müller clamp feature is presented in Fig. 16. The mechanical rendition of the STGAP2SC gate driver module is shown in Fig. 16a. Only to the top side of the design drawing is included since the bottom side does not include any components. Fig. 16b shows the photo of the first prototype.

The design drawing of the gate driver variant with the split output is depicted in Fig. 17. The STGAP2S gate driver module has not been tested yet since the gate driver circuit is not available at this moment. Only the variant with the Müller clamp feature was tested in the application. The schematic diagrams of the STGAP2S and STGAP2SC based gate drivers are shown in Fig. 103, and Fig. 104 respectively, in Appendix B.

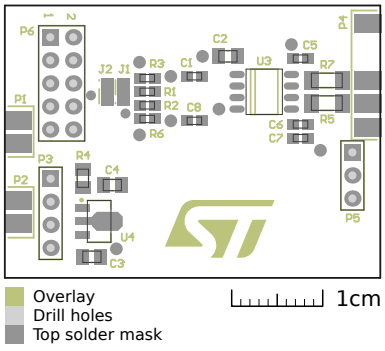
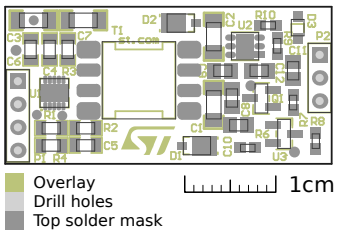
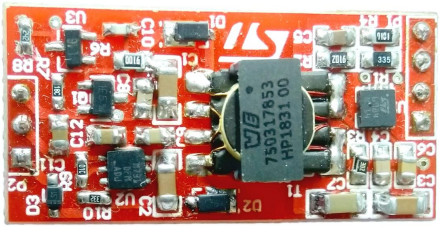


Figure 17 Design draving of the STGAP2S based gate driver



a) Design drawing of the isolated DC/DC converter



b) Photo of the isolated DC/DC converter

Figure 18 Design drawing and photo of the isolated DC/DC used for powering the gate driver modules

2.3.3 Isolated DC/DC converters for powering gate drivers

Since the gate drivers are isolated, they require a galvanically isolated power supply to provide powering of the secondary side of the gate driver circuit. The whole primary part of the power stage is supplied by a voltage of approximately 20V from an external power supply. The DC/DC is providing two separate branches at the secondary side to allow the positive and the negative voltage for the gate driver.

A complete schematic diagram of the isolated DC/DC can be seen in Fig. 101 in Appendix B. The converter is based on modified buck topology so-called flyback-buck. The principle of operation is similar as in case of a simple buck converter. The only difference is that instead of ordinary inductor a primary winding of a transformer is used. The operation of flyback-buck based DC/DC is explained more in detail in section 3.5, as the same type of converter, is used for powering the control unit.

Since the DC/DC is based on primary regulation, the secondary side voltage is defined by the regulation precision on the primary side and the primary to secondary winding ratio. The secondary voltage is then greatly influenced by the transformer leakage flux which can vary significantly piece-to-piece. Due to these variations, the secondary voltages are not given precisely. As one of the purposes of this testing platform is performing tests when driving the SiC MOSFETs with different voltage levels, it is needed to provide more precise secondary voltages for the gate driver circuit. Linear voltage regulators were added to the secondary side of the isolated DC/DC to meet the requirement of precisely defined voltage levels.

On-state voltage	$U_H = 18\ V$
Off-state voltage	$U_L = -3.3\ V$

Table 4 Driving voltages used in the reference design

The secondary side voltage levels that are used in case of the reference design are summarized in Tab. 4.

2.4 Estimation of the critical loop inductance of the prototype PCB

This section focuses on the estimation of the critical loop parameters of the power converter. There are several possible ways of estimating the loop parameters. The first method is based on observing the waveform of the drain-source voltage u_{DS} of the low-side switch during turn on and turn-off transients. The second method is measuring

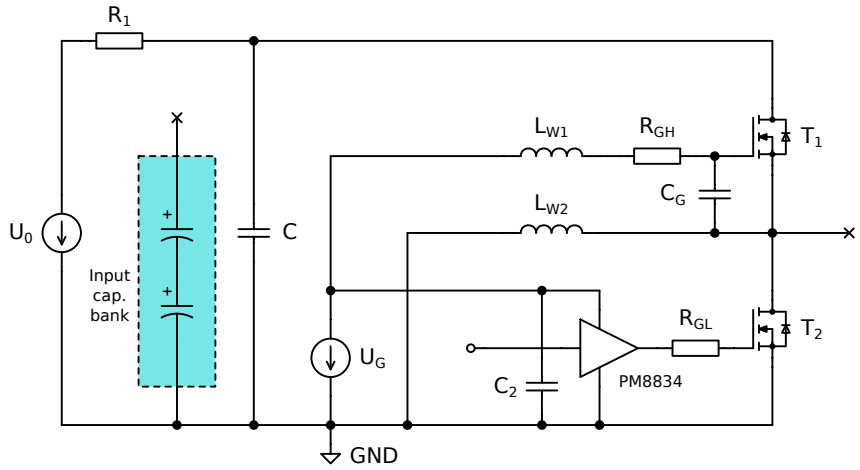


Figure 19 Probe connection for measuring the critical loop response

a small signal response of the critical loop over a wide band of frequencies and trying to estimate the parameters of the substitute circuit. As the critical loop is of very low impedance at low frequencies, it is rather challenging to get consistent data about the loop parameters using, for example, network analysis.

2.4.1 Critical loop identification using an initial condition response

Among the previously mentioned approaches, it is also possible to use an initial condition response to estimate the circuit parameters. Given the critical loop equivalent schematic, it is possible to use the input foil capacitor as charge storage and one of the MOSFET transistors in the half-bridge as an initiator of the transient response. If the precharged capacitor is connected to the critical loop impedance, it produces decaying oscillations. These oscillations are caused by the series connection of the parasitic inductances and the capacitor itself.

The decoupling foil capacitor was disconnected from the rest of the input capacitor bank, and precharged to a specified voltage to generate the response of the initial conditions. The high-side transistor was permanently driven on while keeping the low-side transistor turned off. The low-side switch was initially off and was used to start the initial condition response. For driving the low-side switch, an ordinary dual-channel gate driver PM8834 was used. Both gate drivers in the IC were connected in parallel to produce higher current to switch on the MOSFET as fast as possible.

The schematic diagram of the measurement setup and the probe placement for observing the loop response is illustrated in Fig. 19. A voltage probe was used to measure the voltage across the decoupling capacitor. For rough current measurement, a Rogowski coil with a transducer was used.

The Rogowski coil was clipped around the high-side transistor drain lead. The high-side switch was permanently switched on using an external power supply. The same power supply as for powering the low-side gate driver circuit was used. Using this simple setup can, however, influence the high-side transistor driving voltage. Since during the transient when the low-side MOSFET is turned on, a decaying oscillation appears. This oscillation produces a relatively high current in the critical loop generating a voltage drop over the low-side transistor.

The driving voltage of the high-side transistor is referenced to the source of the low-side MOSFET; it is thus mandatory to decouple the high-side gate for high frequencies

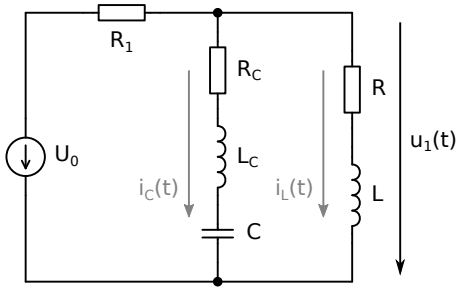


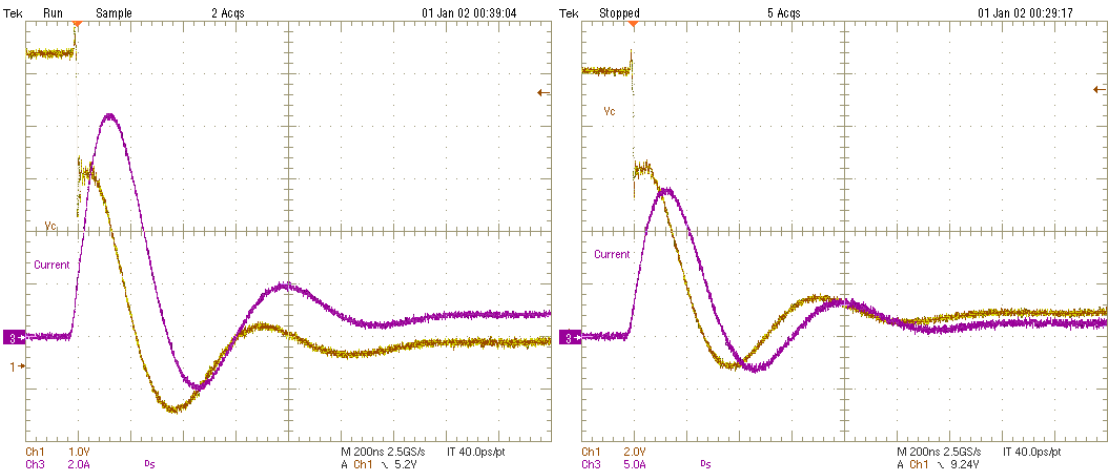
Figure 20 Equivalent circuit of the experiment

preventing the voltage drop across the low-side switch influencing the high-side gate driving voltage. A capacitor of significantly higher capacity than the input capacity of the transistor does the decoupling of the high-side gate-source voltage. The gate and source terminals are also separated from the shared power supply by a series inductance that is not physically present but is formed by long wires.

This decoupling was proved to be enough to provide such a simple test setup without the need for any floating gate driver with an isolated power supply. Since the initial condition response produces transient that takes only several hundreds of nanoseconds, this approach is valid, and the high-side transistor drain-source voltage should not fall significantly.

One could object that the isolated DC/DC could be used to drive both transistors as it is used during the regular operation of the converter. The reason for excluding the gate driver modules from this experiment is relatively high radiated and conductive EMI caused by the isolated DC/DC.

By considering the probe placement, an equivalent circuit of the critical loop can be created as shown in Fig. 20. The resistor R is a characterization of the on-state resistance of both transistors and the all stray resistances of tracks interconnecting the transistors and the active tip of the voltage probe. The inductance L includes all the parasitic inductances along the half-bridge path such as the stray inductances, inductances of transistor leads or wire bonding. A comparison of initial condition responses under different initial voltages is shown in Fig. 21. Fig. 21a shows the response with capacitor precharged to $U_0 = 6\ V$ and Fig. 21b shows the case with $U_0 = 10\ V$.



a) Initial conditions response at $U_0 = 6\ V$ **b)** Initial conditions response at $U_0 = 10\ V$

Figure 21 Captured waveforms of initial conditions response at different initial voltages

Initial conditions response analysis

It applies for the capacitor current

$$i_C(t) = C\frac{du_C(t)}{dt}, \tag{2.15}$$

where $u_C(t)$ is the capacitor voltage. Using third Kirchoff's law, it can be written for the voltage among the half-bridge stray inductance L

$$u_L(t) = L\frac{di_L(t)}{dt} = u_1 - Ri_L(t). \tag{2.16}$$

The measured voltage $u_1(t)$ can be expressed using the first Kirchoff's law applied to the $u_1(t)$ node as

$$u_1(t) = U_0 - R_1 i_L(t) - R_1 i_C(t), \tag{2.17}$$

Where U_0 is the voltage used to precharge the capacitor. Substituing the $u_1(t)$ in (2.16) yields equation

$$L\frac{di_L(t)}{dt} = U_0 - (R_1 + R)\, i_L(t) - R_1 i_C(t). \tag{2.18}$$

Using third Kirchoff's law, it can be written for the voltage across the parasitic inductance of the capacitor

$$u_{L_C}(t) = L_C\frac{di_C(t)}{dt} = u_1 - R_C i_C(t) - u_C(t), \tag{2.19}$$

where R_C is capacitor series resistance and L_C is capacitor series inductance. Substituting the $u_1(t)$ and rearranging the terms yields

$$L_C\frac{di_C(t)}{dt} = U_0 - (R_1 + R_C) - R_1 i_L(t) - u_C(t). \tag{2.20}$$

Putting the equations (2.18), (2.15) and (2.20) we have a state space representation of the simplified model for the critical loop inductance. Ussing these equations, the response to the initial conditions was simulated using Python programming language. Rearranging equations (2.18), (2.15) and (2.20) leads to a form that can be used for the system identification from the initial condition response from a measured waveforms. The equations are as follows

$$Ri_L(t) + L\frac{di_L(t)}{dt} = u_1, \tag{2.21}$$

$$-CR_C\frac{di_C(t)}{dt} - CL_C\frac{d^2 i_C(t)}{dt^2} = i_C(t) - C\frac{du_1(t)}{dt}. \tag{2.22}$$

The capacitor current $i_C(t)$ can be computed from the half-bridge current and capacitor voltage as follows

$$i_C(t) = \frac{U_0 - u_1(t)}{R_1} - i_L(t). \tag{2.23}$$

Taking the acquired data samples of the measured voltage and the half-bridge current as vectors of data points $\mathbf{u}_1$ and $\mathbf{i}_L$ respectively, we can write the above equations in the form of an overdetermined set of linear equations in the form

$$\mathbf{Ax} = \mathbf{b}. \tag{2.24}$$

Using this expression, we can solve for the loop parameters in terms of the least squares $\mathbf{x} = pinv\,(\mathbf{A})\,\mathbf{b}$. Rewriting the equations (2.21) and (2.22) in the matrix form for the acquired samples we obtain

$$\begin{pmatrix} i_L(t) & \frac{di_L(t)}{dt} \end{pmatrix} \begin{pmatrix} R & L \end{pmatrix}^T = \begin{pmatrix} u_1 \end{pmatrix}, \tag{2.25}$$

$$\begin{pmatrix} -\frac{di_C(t)}{dt} & -\frac{d^2 i_C(t)}{dt^2} & \frac{du_1(t)}{dt} \end{pmatrix} \begin{pmatrix} CR_C & CL_C & C \end{pmatrix}^T = \begin{pmatrix} i_C(t) \end{pmatrix}. \tag{2.26}$$

As can be seen, for the identification of all parameters, derivatives of the measured quantities are needed. One approach that comes forward is to use an approximation of the derivation by the forward difference

$$\frac{dx(t)}{dt} \approx \frac{x(k+1) - x(k)}{T_S}, \tag{2.27}$$

where T_S is the sampling period; however, this approach can not be used on the measured data since the data are noisy. Creating derivatives from the data this way would lead to incorrect results due to the derivatives would be heavily distorted by the signal noise as the signal differentiating amplifies the high frequencies. One possible approach would be to filter out the data before computing the difference. Nevertheless, this approach would require complicated filters of a high order to make the noise effectively reduced at such level that would allow differentiating the signal. The other possible way is to use a Savitzky-Golay filter.

This filter uses a sliding window of a given length to interpolate the data in the window by a polynomial function of a given order [15]. How the window moves over the data, it creates new data points based on the values given by the interpolating polynomial. Since the original data are interpolated by a polynomial, a derivative of the polynomial can be evaluated at each point. Taking the window length sufficiently long an approximation of a noisy signal derivative can be obtained. However, the order of fitting function must be selected based on the order of evaluated derivative of the original signal. It requires some prior experiments with the acquired data to obtain optimal parameters of the filter. The deeper explanation of the Savitzky-Golay filter is, however, beyond the scope of this document.

Result of critical loop parameters estimation

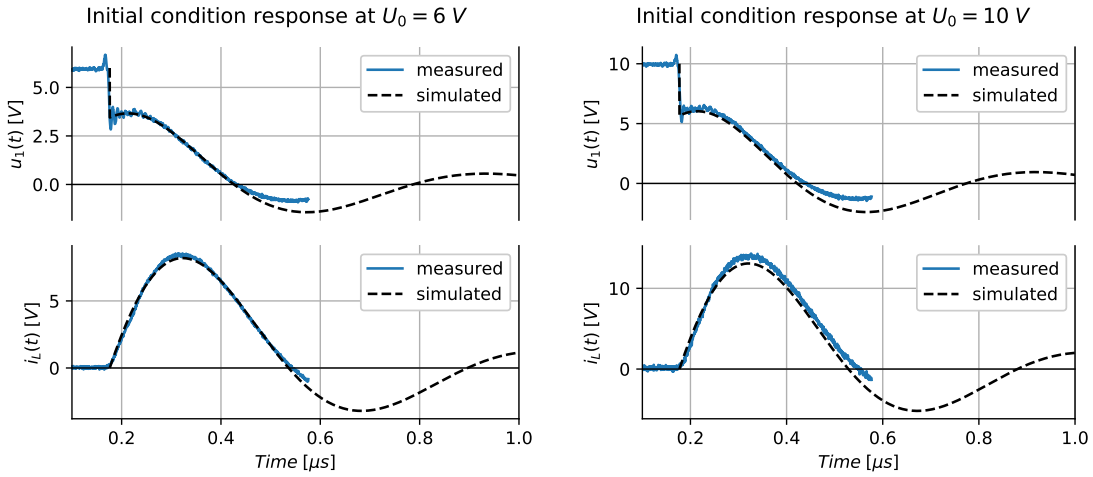
The experimental data were filtered using the filter as mentioned above. It was needed to find the optimal filter settings for each set of points to get the best results.

The inductance L and resistance R of the half-bridge was obtained using the equation (2.25). The solution is in form

$$\begin{pmatrix} R & L \end{pmatrix}^T = pinv\left\{ \begin{pmatrix} \mathbf{i}_L(t) & \frac{d}{dt}\mathbf{i}_L \end{pmatrix} \right\} \begin{pmatrix} \mathbf{u}_1 \end{pmatrix} \tag{2.28}$$

where $pinv\,\{\mathbf{A}\}$ denotes pseudo-inverse of the matrix $\mathbf{A}$. This method provided reliable results repeatable for data acquired under various conditions. However, in the case of the overdetermined set given in (2.26), the results showed to be inconsistent. It was observed by several experiments, that it is needed to provide the value of C apriori or the solution falls into incorrect values, and the results are not repeatable. Providing the value of C apriori yields equation

$$\begin{pmatrix} -\frac{d}{dt}\mathbf{i}_C & -\frac{d^2}{dt^2}\mathbf{i}_C \end{pmatrix} \begin{pmatrix} CR_C & CL_C \end{pmatrix}^T = \begin{pmatrix} \mathbf{i}_C(t) - \frac{d}{dt}\mathbf{u}_1 \end{pmatrix}. \tag{2.29}$$



a) Initial conditions response at $U_0 = 6\ V$ **b)** Initial conditions response at $U_0 = 10\ V$

Figure 22 Simulation of the initial response compared to measured waveforms

The solution of the unknown parameters can be expressed in the form

$$\begin{pmatrix} R_C & L_C \end{pmatrix}^T = \frac{1}{C} pinv\left\{ \begin{pmatrix} -\frac{d}{dt}\mathbf{i}_C & -\frac{d^2}{dt^2}\mathbf{i}_C \end{pmatrix} \right\} \begin{pmatrix} \mathbf{i}_C(t) - \frac{d}{dt}\mathbf{u}_1 \end{pmatrix}. \tag{2.30}$$

This method was experimentally fitted to the nature of measured data to provide the best results. Several experiments with acquire data processing were done to fine tune the parameters of the filters and the compensation of the waveform skewness. Hence, this approach suffers relatively high uncertainty caused by the noise of the experimental data. The derivatives used to form the overdetermined sets of equations are also approximations and are heavily dependent on parameters of used Savitzky-Golay filter. However, after finding the right conditions for data processing, the method provided results with some degree of repeatability. The results of the identification are summarized in Tab. 5.

U_0	$6V$	10	V
R	274.7	285.2	$m\Omega$
L	31.5	31.8	nH
R_C	11.5	10.6	$m\Omega$
L_C	23.3	24.4	nH
L_{CL}	54.8	56.2	nH

Table 5 Estimated parameters of the critical loop

The measured data are distorted by an offset that appears after the first half of the oscillation period. Due to this, only a part of the waveforms was found to be valid for the identification. The comparison of the initial response simulation with the measured data is shown in Fig. 22. Fig. 22a shows the simulation result compared to acquired data at the initial voltage $U_0 = 6\ V$ while Fig. 22b shows the responses at $U_0 = 10\ V$.

3 Design description of the control unit

This chapter aims to provide a design description of the control unit for the power converter. The main focus is on the overview of the hardware design, especially of the signal conditioning blocks.

Schematic diagrams of the control unit are split into small parts and are described separately. This approach prevents including large schematics in the text. The schematic diagrams included in the document are more likely block diagrams as some components are excluded and only those that are major for the circuit design are described. Moreover, the schematic diagrams described in the text always uses the component designators starting from the one rather than using numbers matching the original schematic sheet. It is done to prevent high numbers of component designators for the comprehensibility of the description and mathematic relationships. For the complete schematic diagrams of the control unit see Appendix A.

All blocks or quantities that share its notation across the document are summarized in the list of symbols and are mentioned in the text.

3.1 Design description

The converter control unit is provided with several input signals and is supposed to generate control outputs to the gate drivers. It is powered from an external voltage source the same way as the primary side of the gate drivers on the power stage board. The controller is used to sense input voltage, output voltage, and the inductor current. Measured signals are then conditioned to match the input specifications of an ADC used for the data acquisition. The control unit provides a communication interface for connecting a PC which can communicate with the control unit and perform several actions to configure the converter operation.

One of the most important functions of the control board is to provide the galvanic insulation of the input and output voltage measurement. It also provides insulation of the communication interface. A simplified block diagram of the control unit is shown in Fig. 23.

The control unit consists of three main parts. The first part is the communication interface. The communication interface provides a USB-mini type B port for connecting with a PC. It has a built-in USB to UART converter based on dedicated IC. The galvanic insulation is done on UART as the insulation of the UART is much more straightforward and cheaper than isolation of the USB.

The second part of the control unit is the signal conditioning and processing unit. It is based on STM32F mainstream MCU. This unit is galvanically connected with the primary side of the power stage and is powered from an external power supply.

The last part is the input and output voltage sensing. The voltage sensing is directly connected to the power stage input and output voltage. Thus galvanic insulation is essential to maintain a certain degree of safety. The galvanic insulation of the measured signal is provided by optoisolation amplifiers.

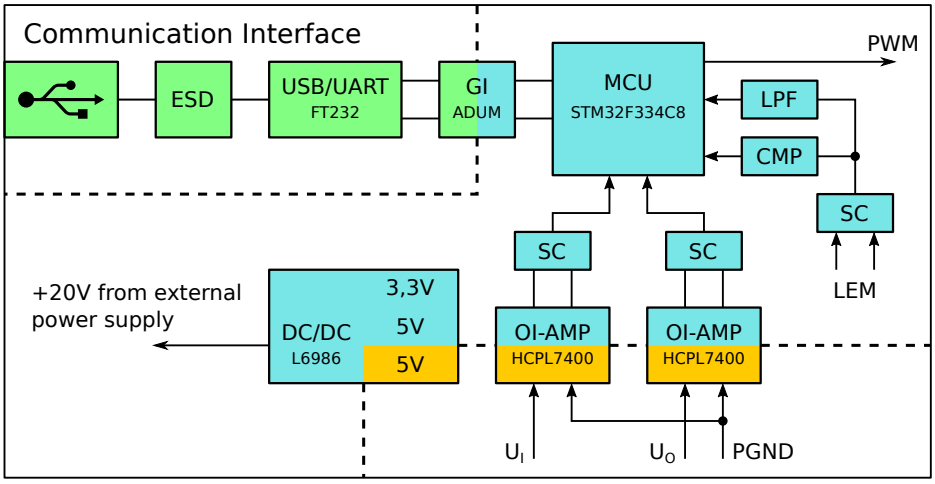


Figure 23 Simplified block diagram of the control board

3.2 Input and output voltage sensing

The input and the output voltages are pre-divided by voltage dividers to fit into the input voltage range of the optoisolation amplifiers. The divider also forms with an external capacitor first order low pass filter. The filter attenuates higher harmonics and spikes that could be added to the measured signal and helps to reduce potential conductive EMI. Notably, the input and output voltage sensing are exposed to relatively high interference from the converter half-bridge and isolated DC/DC converters powering the gate drivers. Signal filtering also reduces the bandwidth over which the noise is integrated.

The output of the optoisolation amplifiers is differential. To interface the amplifier output and adequately scale the voltage to the input voltage range of the ADC converter inside the MCU, differential amplifiers were added for both input and output voltage sensing. The differential amplifiers also provide some level of filtering mainly to suppress the conductive EMI with the other parts of the control board and to attenuate higher harmonics in the measured signal.

The outputs of the differential amplifiers are fed to the MCU pins that provide a mapping to the internal ADC. The input of the ADC is blocked with a small capacitor with a value of several tens of picofarads. This capacitor is added to provide some charge reserve for the input sampling capacitor of the ADC. The blocking capacitor is chosen sufficiently small to prevent instability of the preceding amplifier. If the capacitor value were too high, some techniques would be needed to avoid the operational amplifier from oscillating. At the minimum, an additional resistor in series with the blocking capacitor would be required.

A simplified schematic diagram of the output voltage measurement chain is shown in Fig. 24. The schematic diagram of the input voltage sensing is equivalent. Fig. 24 also presents the notation used to label all the important quantities. An either quantity that belongs to the output or input voltage sensing is marked by O or I respectively in brackets in the lower index.

The signal conditioning blocks of the control unit uses a single supply powering. It was chosen to simplify the design of a DC/DC converter used for the control unit powering as described in section 3.5. Hence, CMOS input and output rail-to-rail operation amplifiers were selected to maximize the output voltage swing.

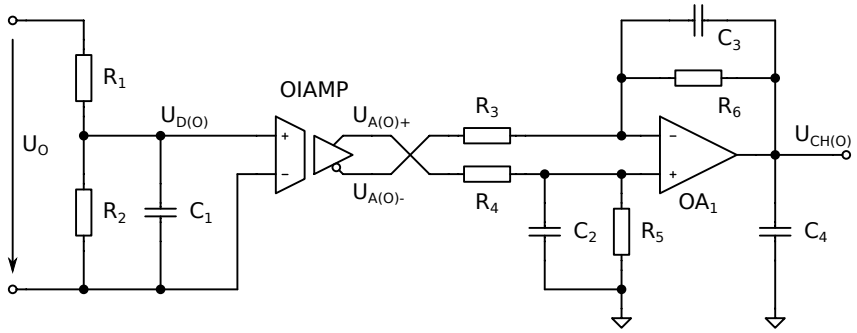


Figure 24 Simplified schematic diagram of measurement chain of the output voltage

3.2.1 Voltage sensing and signal conditioning design

The input and the output voltage sensing dividers are selected simply, based on the maximum input or output voltage ranges. The maximum input voltage before the output of the optoisolation amplifier is clipping is $U_{D(O)_{SAT}} = 308\ mV$ [35]. It is important to note that the resistor R_1 is realized by a series connection of four resistors. This is done in order to spread the output voltage across multiple physical parts. Since SMD resistors in package 1206 are used, the voltage across one resistor is limited.

Given the value of the resistor R_1 which represents the series cascade of resistors, the resistor R_2 can be simply calculated based on the selected input or output voltage range

$$R_2 = R_1 \frac{U_{D(O)_{SAT}}}{U_{O_{MAX}} - U_{D(O)_{SAT}}}. \tag{3.1}$$

A small capacitance decouples the input pins of the optoisolation amplifiers. The added capacity forms a first order low pass filter with the impedance of the voltage divider. This first order low-pass filter is used as an elementary anti-aliasing filter for the optoisolation amplifier input.

It applies for the parallel combination of R_2 and C_1

$$R_2 \parallel C_1 = \frac{R_2}{j\omega R_2 C_1 + 1}. \tag{3.2}$$

The input voltage of the optoisolation amplifier can be expressed using the sensed voltage as follows

$$U_{D(O)}(j\omega) = U_O(j\omega) \frac{\frac{R_2}{j\omega R_2 C_1 + 1}}{\frac{R_2}{j\omega R_2 C_1 + 1} + R_1}. \tag{3.3}$$

By simplifying the above expression, the small signal transfer function of the voltage sensing divider can be written in a form

$$G_{D(O)}(j\omega) = \frac{R_2}{R_2 + R_1} \frac{1}{1 + j\omega C_1 R_1 \parallel R_2}. \tag{3.4}$$

The capacitor can be then selected according to the required cut-off frequency $f_{D(O)}$ of the output voltage divider

$$C_1 = \frac{1}{2\pi f_{D(O)} R_1 \parallel R_2} \tag{3.5}$$

The differential amplifier is designed to match the output of the optoisolation amplifier to the input range of the microcontroller ADC. The key parameters of the optoisolation amplifier output are summarized in Tab. 6.

Parameter	Value
OPAMP low voltage level	$\approx 1.29\ V$
OPAMP high voltage level	$\approx 3.80\ V$
Maximum Output Swing	$\approx 2.51\ V$
Gain	$8\ VV^{-1}$

Table 6 Summary of key parameters of the optoisolation amplifier. Data source: [35].

Assuming $R_3 = R_6$ and $R_4 = R_5$, it applies for the output voltage of the differential amplifier

$$U_{CH(O)} = \frac{R_6}{R_3}\left(U_{A(O)+} - U_{A(O)-}\right). \tag{3.6}$$

The resistor ratio is selected to match the output voltage to the supply voltage of the microcontroller ADC if the output of the optoisolation amplifier is in its maximum voltage swing.

The differential amplifier is also used as a first-order low-pass filter by adding capacitors in parallel to the resistors R_6 and R_5. If the capacitors C_2 and C_3 are approximately the same value, the small signal transfer function of the differential amplifier can be approximated by

$$G_{A(O)}\left(j\omega\right) = \frac{R_6}{R_3}\frac{1}{1 + j\omega C_2 R_6}, \tag{3.7}$$

where $C_2 = C_3$. Given the cut-off frequency, the capacitor values are calculated according to

$$C_2 = \frac{1}{2\pi f_{A(O)} R_6}. \tag{3.8}$$

The cutoff frequency is chosen for the output voltage sensing to be slightly higher than the natural frequency of the converter dynamics. Hence, the higher voltage ripple will be observable at the input of the ADC, but it does not make a significant impact as the output voltage signal is sampled eight-times during the switching period, and a cycle mean value is evaluated. On the other hand, the input voltage measurement is taken only as an informative measurement and the control algorithm does not use it for regulation.

A control algorithm can use the input voltage for a feed-forward compensation, but even in this case, the input voltage is supposed to be constant and not varying significantly as it is provided by an external power supply. Based on this, the ADC is set to sample the input voltage at a lower rate than the output voltage. Also, the input voltage can suffer higher voltage ripple since the input current of the buck converter has a trapezoidal waveform when operating deep in CCM. Based on this, the cut-off frequency of the differential amplifier used for input voltage sensing is selected to be lower than the switching frequency of the converter.

Tab. 7 sumarizes parameters of signal conditioning circuits for the input and the output voltage sensing. The sensitivity of the output voltage measurement is set to a higher value. Hence the maximum measurable output voltage is lower compared to

Parameter	Iput	Output
Voltage sensing divider	$\doteq 406$	$\doteq 535\ \mu V V^{-1}$
Antialiasing filter cut-off frequency	$\doteq 97$	$\doteq 213\ kHz$
Differential amplifier gain	$\doteq 1.36$	$\doteq 1.36\ VV^{-1}$
Differential amplifier cut-off frequency	$\doteq 2.6$	$\doteq 39.3\ kHz$
Maximum measured voltage	$\doteq 745$	$\doteq 565\ V$

Table 7 Summary of the voltage sensing and signal conditioning circuit parameters

the maximum input voltage. This setting is done to provide better utilization of the ADC input dynamic range since the output voltage is not supposed to go too high and even close to the input voltage level. The closed-loop constant voltage regulation uses the measured value; it is essential to get the most upper possible dynamic range of the ADC for the output voltage measurement.

On the other hand, limiting the output voltage measurement range reduces the maximum voltage that can be set by the regulation. This limitation is not an issue in case of the under full load operation since the reference design output voltage under full load is limited to be below four hundred volts due to a resistive load. However, at light load operation, the maximum output voltage level achievable by the regulation is limited. Lowering the maximum output voltage is a compromise between the attainable output voltage and the ADC input dynamic range utilization for closed-loop control.

The maximum input differential voltage of the optoisolation amplifier before the output is clipping is much lower than the absolute maximum rating, there is substantial margin for the input voltage to exceed the linear range of the amplifier. Hence, in case of the open loop operation, the converter's output voltage can be safely set higher than the maximum measurable value. But the control unit will report a distorted value of the output voltage in such a case.

3.2.2 Voltage sensing transfer function

It is important to consider the transfer function of the output voltage measurement chain as it can influence the closed loop behavior of the converter. The voltage of the output voltage divider $U_{D(O)}$ is sensed by the optoisolation amplifier. Since the optoisolation amplifier has significantly higher input impedance than is the impedance of the voltage divider, which is given by the parrallel combination of resistors R_1 and R_2, we can negtlect the influence of the optoisolation amplifier to the divider voltage.

The input impedance of the differential amplifier used to interface the optoisolation amplifier output to the ADC input is given by the resistors R_3 and R_4. However, the output of the optoisoltaion amplifier is of low impedance which is many times lower than the input impedance of the differential amplifier. Hence, we can approximate the output of the optoisolation amplifier by a voltage source and neglect the influence of the optoisolation amplifier output impedance to the differential amplifier input.

Given the gain of the optoisolation amplifier G_{OA} which is the same for both, the input and the output voltage sensing, the overall transfer function of the output voltage sensing chain can be approximated as follows

$$G_{VS(O)}(j\omega) \approx G_{D(O)}(j\omega)\, G_{OA} G_{A(O)}(j\omega) = G_{OA} \frac{R_2 R_6}{(R_2 + R_1) R_3} \frac{1}{(1 + j\omega C_1 R_1 \parallel R_2)(1 + j\omega C_2 R_6)}. \quad (3.9)$$

3.3 Inductor current sensing

This section gives an overview of the inductor current sensing for current regulation and for providing over-current protection. A current transducer LEM CKSR-25R has been chosen for the inductor current measurement. The CKSR sensor series are based on a fluxgate sensor with favorable time and temperature stability of sensitivity, offset and voltage reference. It offers four conductors that can be connected either in parallel or in series in several configurations providing different settings of the sensor sensitivity. In case of this application, the parallel connection is used to get the maximum current range on the input and the lowest resistance inserted in the measured conductor.

This current transducer features a bandwidth of up to 300 kHz and good reaction and response times. It also has high du/dt immunity which makes it suitable for measuring the inductor current at the output of the transistor half-bridge. Tab. 8 shows a summary of the key parameter of the current transducer.

Parameter	Value
Bandwidth	300 kHz
Reaction time	300 ns
Response time	300 ns
Sensor sensitivity	25 mVA^{-1}
Reference voltage	2.5 V

Table 8 Summary of key parameters of the current transducer. Data source: [30].

Low values of reaction and response times make the current transducer also applicable for overcurrent protection. The current sensor is placed on the main power stage. It senses the inductor current at the output of the half-bridge. This placmemen is not optimal since the conductor where the current is sensed is floating with high du/dt [30]. Hence, a voltage spikes are injected to the current transducer output during switching of the half-bridge transistors. The amplitude of the spikes increases with increasing voltage slope and can reach values of several volts. It is therefore needed to load the output with a capacitor of sufficient capacity to absorb the energy injected due to the transients.

The current transducer could also be added at the output node of the power inductor before the capacitor bank. This placement would prevent the issues with the induced voltage spikes at the output as the other node of the inductor is fixed at the output voltage with negligible voltage changes during steady-state operation. However, in the prototype, the placement on the half-bridge output was chosen due to layout considerations and limited space. The output placement would be possible in case of PCB expansion for the optimal routing of the power and output signals of the current sensor.

3.3.1 Current transducer signal conditioning

Fig. 25 shows a simplified schematic diagram of the first part of the inductor current sensing and signal conditioning path.

The output of the current transducer is driving a low-pass filter made up of a simple RC network. The low-pass filter is placed directly at the output of the current sensor to attenuate spikes injected to the transducer output due to high $du\ dt$ of the measured conductor. The output driving capability of the sensor is however limited to 100 pF, so it is necessary to add a series resistor. Also, the reference output and the supply

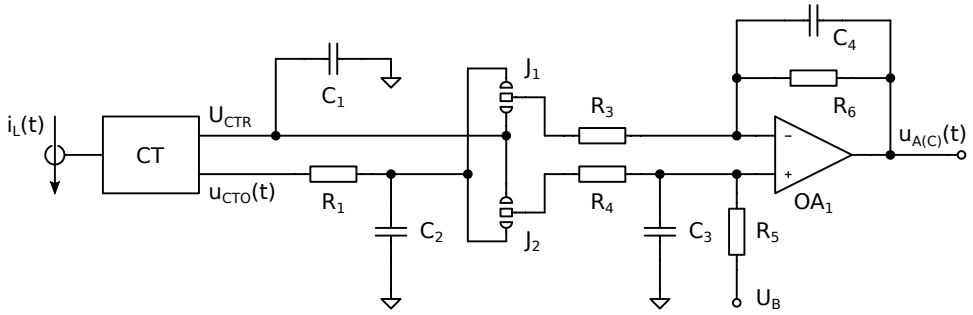


Figure 25 Schematic diagram of the current transducer output conditioning

voltage decoupling is essential. It is important to note that the RC network is present on the power stage PCB.

The signal from the current sensor is routed relatively long distance on the bottom side of the power stage PCB. Even the signal path is surrounded by grounded copper planes; it receives a certain degree of interference from both the switching SiC MOSFETs and from the DC/DC converters used for powering the transistor gate drivers. However, this situation could not be overcome by a different layout since the current transducer placement is optimized in term of the power stage layout and routing of the high current carrying conductors. To limit the amount of the noise present in the current transducer signal, another small value capacitor as added in the control unit as close to the signal conditioning as possible. Hence, the capacitor C_2 is made up of two physical components connected in parallel. One of them is a part of the RC filter tightly coupled to the current sensor output, and the other one is present on the control unit PCB as close to the signal conditioning as possible.

The output of the selected current transducer is relative to its internal reference voltage. The reference voltage is in the middle of the transducer supply voltage $U_{CTR} = 2.5\ V$, thus providing the bipolar information of the sensed current. The reference output is high impedance, so the measurement range can be biased by applying an external voltage to the transducer reference output [30]. It is needed to interface the current transducer's output to the input voltage range of the internal ADC to measure the voltage by the MCU.

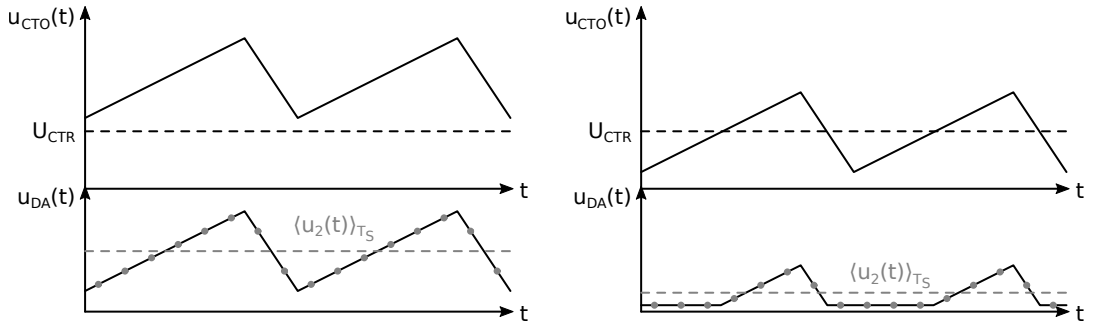
A differential amplifier is used to amplify a positive difference of the current transducer output voltage $u_{CTO}(t)$ and its reference voltage $u_{CTR}(t)$. The jumpers at the input of the differential amplifier are used to switch the polarity of the output signal. It is useful as the converter can be used as a synchronous boost. In such a case, the inductor current flows in the opposite direction compared to the synchronous buck. A more detailed description of the control unit abilities is provided in chapter 5.

If the differential amplifier resistors are selected in way that $R_3 = R_6$ and $R_4 = R_5$, the output voltage can be expressed as

$$u_{A(C)}(t) = \frac{R_6}{R_3}\left(u_{CTO}(t) - U_{CTR}\right) + U_B, \tag{3.10}$$

where U_B is a bias voltage. Since the signal conditioning uses a single supply, the amplifier is biased to prevent clipping in case the measured current is negative. The small signal transfer function of the differential amplifier can be approximated by

$$G_{A(C)}\left(j\omega\right) \approx \frac{R_6}{R_3}\frac{1}{1 + j\omega R_6 C_4}. \tag{3.11}$$



a) Differential amplifier output voltage and cycle mean evaluation at $\langle i_L(t)\rangle_{T_S} > \Delta i_L/2$

b) Differential amplifier output voltage and cycle mean evaluation at $\langle i_L(t)\rangle_{T_S} < \Delta i_L/2$

Figure 26 Example of current mean value distortion caused by the output clipping

Given the gain and the cut-off frequency of the amplifier the capacitor value can be selected using the same approach as described in the previous section.

Biasing the differential amplifier

In steady state operation of the converter, the cycle mean value of the inductor current $\langle i_L(t)\rangle\, T_S$ is always positive or zero in the synchronous buck topology. The level of the mean value of inductor current increases with output power. Conversely, it goes down towards zero with decreasing load. However, during transients, the mean value of the inductor current can go under the zero, and under the light load operation, the current ripple causes the current go to negative values as well.

Clipping the output to the zero can influence the behavior of the compensator during the transients and can induce stability issues of the current regulation. It also disallows to precisely regulate to the zero mean value of the current as the inductor current ripple is not negligible when the mean value goes close to the zero. Fig. 26a shows the evaluated cycle mean value of the current if $\langle i_L(t)\rangle_{T_S} > \Delta i_L/2$, while Fig. 26b shows the distorted cycle mean value evaluation in case the $\langle i_L(t)\rangle_{T_S} < \Delta i_L/2$.

One of the solutions that come forward is to use a fully differential operational amplifier. It would be possible to monitor the output of the differential amplifier by configuring the ADC in differential mode. However, the input range of the ADC would be split for both current polarities equally. As the current ripple depends on the selection of the inductor value, the current ripple can be small compared to the mean value during steady-state operation. In this case, halving the ADC range for both inductor current polarities is wasting of the dynamic range of the ADC.

To make better use of the ADC input range, we can suppose the inductor current will not fall to a negative value deeper than a half of the maximum inductor current ripple Δi_L plus some margin for the transients. The response during transients is a function of the current control quality. In the case of decent closed-loop behavior of the current control, one can assume the current will no go too deep into the negative values.

The applied solution uses a biased differential amplifier. The bias voltage is high enough to make some reserve on the ADC input for the current below zero. In this case, the reserve can be adjusted according to the power stage configuration to get the maximum utilization of the ADC input dynamic range. Several approaches can be used to apply the bias voltage to the amplifier. One method is to use a fixed bias voltage provided by a voltage divider. However, due to the requirement of control unit versatility, the bias voltage should be easily configurable.

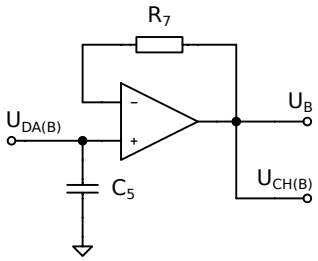


Figure 27 Schematic of the voltage follower used for the bias voltage decoupling

In this case, the bias voltage is provided by a DAC which is a part of the MCU. This approach can be used to maximize the versatility of the measuring chain. Fig. 27 shows a voltage follower that is used to decouple the DAC output voltage $U_{DA(B)}$ from the differential amplifier as the output impedance of the internal DAC converter is very high and has significant uncertainty. If an internal buffer for the DAC output is used, the output impedance decreases [18] but is still high enough to interfere with the resistor network of the differential amplifier. The output impedance of the voltage follower is negligible compared to the rest of the feedback network of the differential amplifier. In this case, the bias voltage is simply added to the output voltage assuming $R_2 = R_4$ and $R_1 = R_3$ as per equation (3.10).

The bias voltage is back-sensed by the ADC to provide a more precise correction of the bias of the amplifier as marked by the $U_{CH(B)}$ node in the schematic. The back-sensing of the bias voltage helps to suppress an influence of the operational amplifier input offset and input bias currents and their temperature drifts. The bias voltage is corrected using a technique described in section 3.4.

Bias voltage evaluation based on operating conditions

The output of the differential amplifier is fed to the Sallen-Key filter as described in section 3.3.2. The Sallen-Key filter amplifies the output of the differential amplifier by its gain G_{SK}. This gain is given by selecting a filter transfer function approximation. Taking into account the Sallen-Key filter gain, the output of the differential amplifier must fit in the range

$$U_{A(C)_{MAX}} = \frac{U_{DDA}}{G_{SK}}, \tag{3.12}$$

where U_{DDA} is the supply voltage of the ADC, which is equal to the maximum input voltage. The transducer U_{CTO} output voltage is given by

$$U_{CTO} = G_{CT} I_{CT} + U_{CTR}, \tag{3.13}$$

where U_{CTR} is the reference voltage of the current transducer and I_{CT} is the measured current. The maximum inductor current is given by the maximum load and the current ripple at the maximum output power, while the minimum of the inductor current occurs at light load operation. In this case, the minimum is produced only by half of the current ripple. As it was derived in chapter 2, the maximum peak inductor current is given by

$$i_{L_{MAX}} = \langle i_L(t) \rangle + \frac{\Delta i_L}{2}. \tag{3.14}$$

The inductor current ripple is given by

$$\Delta i_L = \frac{(1-\delta)\,\delta T_S U_I}{L}. \tag{3.15}$$

The maximum of the current appears at the maximum output power and the maximum input voltage. Assuming the fixed resistive load R_L that is available for the testing platform, the duty cycle at the maximum output power can be roughly estimated

$$\delta_{P_{MAX}} = \frac{U_{O_{MAX}}}{U_{I_{MAX}}} = \frac{\sqrt{P_{MAX} R_L}}{U_I}. \tag{3.16}$$

In the opposite case, the minimum peak current is the negative peak current during the light load operation. The duty cycle at which the maximum inductor current ripple occurs can be obtained by differentiating (3.15) by the duty cycle. It yields the equation

$$\frac{d\Delta i_L}{d\delta} = \frac{T_S U_I}{L} - \frac{\delta T_S U_I}{2L}. \tag{3.17}$$

Making the derivative equal to zero yields an equation which solution is

$$\tilde{\delta} = \frac{1}{2}. \tag{3.18}$$

It is obvious that if the $\delta = \tilde{\delta} = 0.5$ a maximum of the current ripple appears. The current ripple also increases with the input voltage, so the minimum peak current through the inductor can be expressed as

$$i_{LPK_{MIN}} = \frac{T_S U_{I_{MAX}}}{4L}. \tag{3.19}$$

Considering the power converter reference design described in chapter 2, the marginal values of the inductor current were estimated and are summarized in Tab. 9.

Parameter	Value
Output power	5 kW
Output voltage at full power	375 V
Duty cycle	0.625 $-$
Maximum input voltage	600 V
Minimum switchin frequency	40 kHz
Maximum peak current	$\doteq$ 20 A
Minimum peak current	$\doteq -6.5$ A

Table 9 Marginal values of the inductor current for the reference design

The above-evaluated values of the maximum and the minimum peak value of inductor current implies the maximum swing of the current transducer voltage. By considering the differential amplifier, the output swing at the amplifier output is given by

$$\Delta U_{A(C)} = \frac{R_2}{R_1}\left(\Delta U_{CT_O} - U_{CT_R}\right) = \frac{R_2}{R_1} G_{CT}\left(i_{L_{MAX}} - i_{L_{MIN}}\right). \tag{3.20}$$

Referring to the maximum allowed voltage swing of the differential amplifier given by (3.12), the required gain of the differential amplifier can be evaluated as

$$G_{A(C)} = \frac{R_2}{R_1} = \frac{U_{ADC_{MAX}}}{G_{SK}} \frac{1}{G_{CT}\left(i_{L_{MAX}} - i_{L_{MIN}}\right)}. \tag{3.21}$$

The differential amplifier with the addition of the Sallen-Key filter appropriately scales the current transducer output voltage for the given inductor current range. However, the voltage swing is shifted as it starts from a negative value for the current sensor output voltage. The bias applied to the differential amplifier can be evaluated as[1].

$$U_B = -\frac{R_2}{R_1} G_{CT} i_{L_M IN}. \tag{3.22}$$

The full-scale values of particular measurement stages and the evaluated value of the amplifier bias voltage are summarized in Tab. 10.

Parameter	Value
Minimum peak current	$-8\ A$
Maximum peak current	$20\ A$
Bias voltage	$0.7\ V$

Table 10 Current measurement parameters

3.3.2 Current transducer signal filtering

The amplified current transducer signal passes into a third order low pass filter that is made up of second order Sallen-Key filter and an RC low-pass filter. The signal is filtered to provide a more precise estimation of the cycle mean value of the inductor current. The inductor current is sampled at rate "only" eight times higher than the operating frequency of the converter. At marginal operating conditions when the duty cycle is close to one or zero, the influence of higher harmonics of the inductor current can be more significant. In this case, the low-pass filter helps for more accurate cycle mean value estimation as the higher harmonics that are above the Nyquist frequency of the sampling are attenuated. When designing the filter, its influence on the CL regulation of the converter must be taken into account. Therefore the filter cut-off frequency must not be chosen too low to be close to the dominant dynamics of the controlled system.

The schematic diagram of the Sallen-Key low-pass filter with an RC network at its output is shown in Fig. 28. An SMD solder jumper can optionally bypass the second-order Sallen-Key filter. The bypassing can be used in case of peak current control as in that case the more precise reproduction of the inductor current including higher harmonics is of primary concern. The more detailed description of the control unit possibilities is provided in chapter 5.

The values of the C_1, C_2, R_1 and R_2 were chosen to be $C_1 = C_2 = C$ and $R_1 = R_2 = R$ for symplifying the filter design. It applies for the Cut-off frequency [5]

$$RC = \frac{\sqrt{a_2}}{\omega_0}, \tag{3.23}$$

where $\omega_0 = 2\pi f_0$ is the angular cut-off frequency of the filter and a_2 is a second-order coefficient of the filter transfer function. It applies for an arbitrary second-order low-pass filter transfer function

$$G_{SK}(j\omega) = \frac{A_0}{1 + a_1 j\frac{\omega}{\omega_0} - a_2\frac{\omega^2}{\omega_0^2}}. \tag{3.24}$$

[1] Note that the absolute minimum inductor current is negative, thus the minus sign

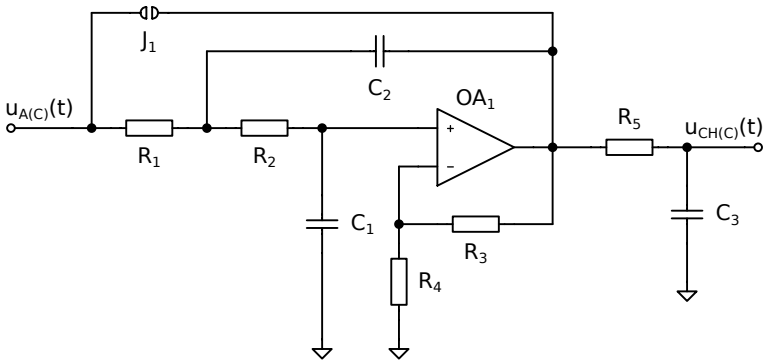


Figure 28 Schematic diagram of the current transducer signal filtering

The filter denominator coefficients are selected based on the desired type of transfer function approximation. Tab. 11 shows the values of second-order low-pass filter denominator coefficients.

Approximation	a_1	a_2
Critical dumping	1.287	0.414
Bessel	1.361	0.618
Butterworth	1.414	1.000
Chebyshev	1.065	1.931

Table 11 Example of second order low-pass filter denominator coefficients. Data source: [5].

In the case of inductor current filter, a Bessel approximation was used as it provides a faster step response without significant overshoot. The amplifier DC gain can be calculated using the filter denominator coefficients as follows [5].

$$G_{SK} = 1 + \frac{R_3}{R_4} = 3 - \frac{a_1}{\sqrt{a_2}}. \tag{3.25}$$

It holds for the small signal transfer function of the Sallen-Key filter [5]

$$G_{SK}\left(j\omega\right) = \frac{1 + \frac{R_3}{R_4}}{1 + j\omega RC\left(2 - \frac{R_3}{R_4}\right) - \omega^2}. \tag{3.26}$$

The output of the Sallen-Key filter continues to a first order low-pass filter formed by a simple RC network. The RC low-pass filter is connected to the input of the ADC. The filtering capacitor is made up of two capacitors in parallel. One of them is of several hundreds of picofarads and is placed as close to the ADC input as possible to compensate stray inductances of the PCB.

The low-pass filter also helps to attenuate the conductive EMI and attenuate high-frequency harmonics. The tightly connected capacitor to the ADC input also serves as a charge bank for the sampling circuitry inside the ADC, which helps in case of short sampling times. Despite this, the output impedance of the ADC driving circuit should be kept as low as possible due to the sampling rate at the ADC input [24, 18].

The maximum value of the impedance of a voltage source driving the ADC can be evaluated according to the shortest used sampling time of the ADC. This comes from the fact that charging of the ADC sampling capacitor is limited by the source impedance and the sampling time [18]. Thus, if the impedance of the voltage source is too high, it can cause an amplitude error of the sampled voltage.

The small signal transfer function of the RC filter is given by

$$G_{LP}(j\omega) = \frac{1}{1 + j\omega R_5 C_3}. \tag{3.27}$$

Value of the resistor in the RC low-pass filter is relatively small so the internal impedance of the preceding operational amplifier output cannot be neglected compared to the value of resistor R_5. Assuming that a resistive part of the output impedance of the operational amplifier driving the RC network dominates at low frequencies, this resistance can be added to the value of the resistor in the RC network. As a result, the transfer function for small signals of the filtering stage can be approximated as follows

$$G_{F(C)}(j\omega) \approx G_{SK}(j\omega)\,\tilde{G}_{LP}(j\omega), \tag{3.28}$$

where $\tilde{G}_{LP}(j\omega)$ is the transfer function of the RC network while considering the output resistance of the operational amplifier R_{OA}. Key parameters of the filtering stage are summarized in Tab. 12.

$$\tilde{G}_{LP}(j\omega) = \frac{1}{1 + j\omega\,(R_5 + R_{OA})\,C_3}. \tag{3.29}$$

Parameter	Value
Sallen-Key filter gain	$\doteq 1.273\ VV^{-1}$
Sallen-Key filter cut-off frequency	$\doteq 42\ kHz$
RC low-pass filter cut-off frequency	$\doteq 100\ kHz$

Table 12 Summary of the filtering stage parameters

3.3.3 Current measurement and signal conditioning transfer function

Since the inductor current $i_L(t)$ is measured using a current transducer and passes through several stages of signal conditioning, the resulting transfer function that includes the measurement path is essential for the controller design as well as it was for the output voltage sensing.

The current transducer bandwidth is up to 300 kHz for gain change $G_{CT}(j\omega) \pm 3\ dB$, which is far beyond the sampling rate at the lowest operating frequency $f_{S_{min}} = 40\ kHz$ and is much higher than the frequency of the dominant dynamics of the converter. In such a case, the current transducer frequency characteristic can be approximated as it was a constant gain G_{CT} over the control loop bandwidth. Moreover, there is no frequency characteristic specification in the sensor datasheet above the 300 kHz, so the behavior of the current transducer above this frequency is unknown.

The current transducer output drives a low-pass RC filter as described earlier. The cut-off frequency of the filter is higher than the bandwidth of the current transducer. Hence its frequency characteristic can be neglected as well.

Given the fact that the output impedance of the differential amplifier stage is significantly smaller compared to the input impedance of the Sallen-Key filter, the small signal transfer function of both, the amplifier and the filtering stage can be approximated by multiplication of both transfer functions. The complete transfer function of the current measurement chain can be estimated as follows

$$C_{CS}(j\omega) \approx G_{CT} G_{A(C)}(j\omega)\, G_{F(C)}(j\omega), \tag{3.30}$$

where $G_{A(C)}(j\omega)$ is the transfer function of the differential amplifier and $G_{F(C)}(j\omega)$ is the transfer function of the filtering stage. The $C_{CS}(j\omega)$ is the transfer function that is going to be used later for simulations of the closed-loop control behavior.

3.3.4 Overcurrent protection

The control unit is equipped with a fast comparator connected to the output voltage of the current transducer to provide overcurrent protection. The comparator is used to give a signalization whether the output of the current sensor goes too far from the reference value. Since the output of the transducer is bipolar relative to its reference, a window comparator is used to protect against positive and negative overcurrent event.

The overcurrent event can occur during the open loop operation or if the closed loop regulation fails or under other failure condition. It is mandatory to check the positive limit as well as the negative one. The positive limit can be reached for example during the short circuit on the output of the converter. The risky situation can also happen in case the output capacitor bank is discharged, and a fast increase in the duty cycle occurs or if the high-side switch is unintentionally switched on for a longer time interval. Conversely, in case the output capacitor bank is charged, and the low-side transistor is accidentally turned on, a negative current limit can be exceeded. In both cases, due to the high capacity of the input and the output capacitor banks, the current can be very high and can lead to the damage of the power transistors.

The window comparator is merely a connection of two comparators to the same signal and multiplying their outputs using logical AND. One of the comparators checks for a lower threshold level, the other one is checking for an upper threshold. For a fast and straightforward solution, the comparators are complementary. The one checking for the lower limit provides a high level on its output when the threshold is exceeded. Conversely, the higher threshold comparator produces a low level on its output when the higher threshold is exceeded. In such a case, the outputs of comparators can be easily joined together using diode AND function as depicted in the schematic diagram in Fig. 29. The AND function is realized using fast, small signal Schottky diodes.

Positive feedback is added to insert a small hysteresis into both comparators to prevent any spurious edges at the output when the input signal occurs near to any of

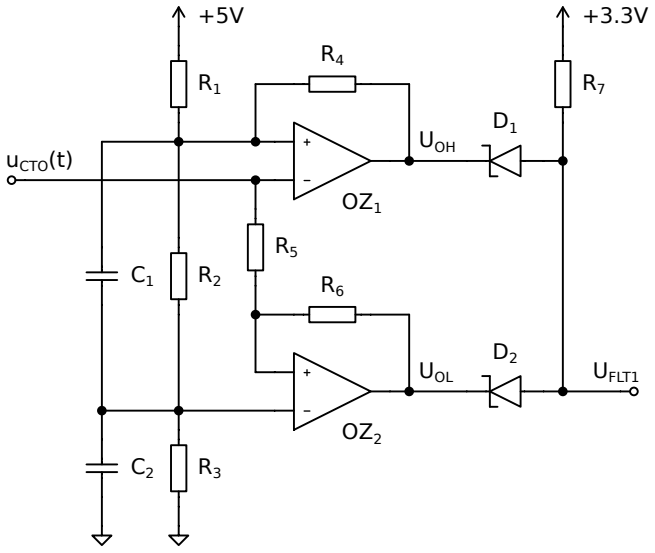


Figure 29 Schematic diagram of the window comparator

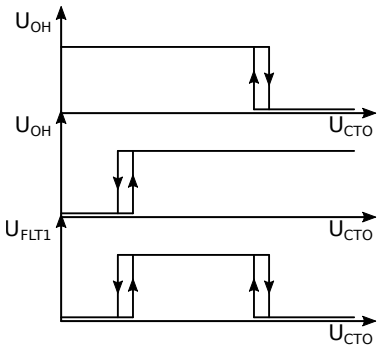


Figure 30 Ilustration of the window comparator operation

the threshold values.

The higher threshold comparator shares the feedback path with the resistor network that provides the threshold setting. Hence the output transition from a high state into a low state of the upper comparator moves the reference threshold of the lower comparator. It is therefore needed to keep the threshold levels of both comparators far enough from each other. Otherwise, the window comparator could not work correctly. The operation of the window comparator is illustrated in Fig. 30.

The lower threshold comparator is the noninverting comparator. Hence the lower comparator hysteresis U_{HL} is given by

$$U_{HL} = U_{CC}\frac{R_5}{R_6}. \tag{3.31}$$

The upper threshold comparator is the inverting comparator. The upper comparator hysteresis U_{HU} can be derived using linear superposition as

$$U_{HU} = U_{CC}\frac{(R_2 + R_3) \parallel R_1}{(R_2 + R_3) \parallel R_1 + R_4}, \tag{3.32}$$

If the hysteresis of each comparator is selected sufficiently low, i.e., several tens of millivolts, and if the difference between the lower and upper threshold voltage is several times higher than the hysteresis of both comparators, then the influence of the hysteresis can be neglected. Hence, it is sufficient to evaluate the divider resistors R_1, R_2 and R_3 in a way as there was no hysteresis present. It applies for the lower threshold voltage U_{TL}

$$U_{TL} = U_{CC}\frac{R_3}{R_1 + R_2 + R_3}. \tag{3.33}$$

The upper threshold voltage is given by

$$U_{TH} = U_{CC}\frac{R_3 + R_2}{R_1 + R_2 + R_3}. \tag{3.34}$$

Fixing the value of the resistor R_3, the other resistors can be found by solving equation (3.33) and (3.34) for unknowns R_1 and R_2. The resistor values are given by

$$R_1 = R_3\frac{U_{CC} - U_{TH} - U_{TL}}{U_{TL}}, \tag{3.35}$$

$$R_2 = R_3\frac{U_{TH}}{U_{TL}}. \tag{3.36}$$

The threshold voltages and hysteresis of both comparators were set according to the needs of the power converter reference design. According to the specifications of the used MOSFET transistors, the overcurrent protection was set to values summarized in Tab. 13.

Parameter	Value
Maximum peak current	35 A
Minimum peak current	-35 A
Hysteresis of maximum peak current	1 A
Hysteresis of minimum peak current	1 A

Table 13 Summary of the overcurrent protection settings

The overcurrent protection is set by hardware components but can be adjusted to needs of any other power transistors just by replacing one resistor while keeping the thresholds of the overcurrent protection symmetric.

3.4 Measurement calibration

All the measurement chains consist of several signal conditioning parts. Their static transfers can be easily obtained analytically and put together. It is needed to include the static transfers of the measurement chains in the control unit firmware to get the correct values of input and output voltages and inductor current. However, the analytically obtained transfer functions suffer from several sources of uncertainties. At the first point, the passive components and their uncertainties create the multiplicative or additive errors that can expand into the overall uncertainty of several percents from the measurement range of a particular quantity. Also, the active components add their offsets and gain error.

This problem has led to the implementation of calibration characteristics in the control unit firmware. The calibration constants are configured before the control unit usage. The calibration data are stored in the device firmware or can be configured online. Only the first order approximation of the transfer function is made for the calibration.

The input voltage on an arbitrary ADC input channel y is given

$$u_{CH(y)} = F(x) = Sx + O, \tag{3.37}$$

where S is the sensitivity, O output offset and the term x denotes the original input quantity. In this case, it can be the output voltage $x \equiv u_O(t)$, $y \equiv O$ or the input voltage $x \equiv u_I(t)$, $y \equiv C$.

3.4.1 Current transducer signal measurement calibration

In the case of the current measurement, the measurement chain is split into two parts as the stage after the offset injection may not be a unity gain. Fig. 31 shows the block diagram of the measurement chain of the inductor current.

The voltage at the ADC input that senses the inductor current can be expressed in the form

$$U_{CH(C)} = F_{C2}\left(F_{C1}\left(I_L\right) + U_{CH(B)}\right) = S_{C2}\left(S_{C1}I_L + O_{C1} + U_{CH(B)}\right) + O_{C2}, \tag{3.38}$$

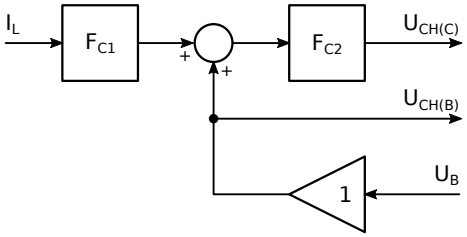


Figure 31 Block diagram of the current measurement correction

where F_{C2} denotes the first order static transfer function from the inductor current to the output voltage of the differential amplifier $U_{A(C)}$ and F_{C1} is the static transfer function of the signal filtering stage. The term $U_{CH(B)}$ denotes the voltage measured by the ADC channel used for scanning the actual value of the bias voltage. By collecting terms and expressing i_L from the (3.38) we obtain for the inductor current

$$i_L = \frac{1}{S_{C2}S_{C1}} \left(U_{CH(C)} - \tilde{U}_B - \tilde{O}_{C2} \right), \tag{3.39}$$

where $\tilde{U}_B = S_{C2}U_{CH(B)}$ is the bias voltage correction and $\tilde{O}_{C2} = S_{C2}O_{C1} + O_{C2}$ is the total output offset of the linear approximation of the transfer. Each static transfer function coefficients are stored in the control unit firmware and can be configured on the fly.

Since the control unit measures the exact value of the bias voltage, it implements an automatic calibration procedure of the current transducer output offset O_{C1} and both, the sensitivity S_{C2} and offset O_{C2}. The control unit performs the calibration procedure in two steps applying two levels of bias voltage. The calibration is done during the control unit startup. It must be ensured that there is no current flowing through the current transducer. Otherwise, the value of the offset would be distorted. If the inductor current is zero, the voltage at the current monitoring input of the ADC can be expressed as

$$U_{CH(C)} = S_{C2}U_B + \tilde{O}_{C2}. \tag{3.40}$$

During the calibration, two levels of bias voltage are applied, and both, the exact values of bias voltage, $U_{CH(B)_1}$ and $U_{CH(B)_2}$, and the resulting voltages, $U_{CH(C)_1}$ and $U_{CH(C)_2}$, are measured. The control unit performs the acquisition of the test sample continuously and filtering both voltages by a first order IIR filter. The control unit keeps acquiring the samples as long as the filtered signal is not considered stable. This procedure helps to improve the accuracy of the calibration in the presence of noise.

The result of the calibration is the sensitivity of the current transducer signal filter, and both, the filter and the current transducer output offsets. The DC gain of the current signal filter is given by

$$S_2 = \frac{U_{CH(C)_2} - U_{CH(C)_1}}{U_{CH(B)_2} - U_{CH(B)_1}}. \tag{3.41}$$

The value of the overall offset $\tilde{O}_2$ is given by

$$\tilde{O}_2 = \frac{1}{2} \left(U_{CH(C)_1} + U_{CH(C)_2} - S_2 \left(U_{CH(B)_1} + U_{CH(B)_2} \right) \right). \tag{3.42}$$

Note, that the overall offset $\tilde{O}_2$ includes the output offset of the current transducer and the offset of the current signal filter that is mainly caused by the Sallen-Key filter.

Thanks to this approach, only the sensitivity of the current sensor and the differential amplifier needs to be provided to the control unit.

3.4.2 Calibration of the reference control unit

The calibration constants for the voltage sensing were measured using a constant voltage power supply with adjustable output voltage in a range from zero to six hundred volts. The power supply was connected to the input and the output power ports of the power stage and the output voltage of the differential amplifier $U_{A(I)}$ and $U_{A(O)}$ respectively were measured. Both output voltages correspond to the voltages at the ADC channels monitoring the input and the output voltage. The transfer characteristic was measured while the power stage was inactive.

Fig. 32 shows the output and input voltage sensing transfer characteristic. The upper part of the graphs shows the measured transfer function of the input and output voltage sensing circuitry and the lower part depicts the residue of the linear interpolation.

In the case of the current sensing circuitry, high-current low-voltage power supply was used to draw current through the current transducer. The output voltage of differential amplifier U_{DA} used for conditioning the signal from the current sensor was measured as the output quantity.

The measured current sensing transfer characteristic is shown in the upper graph in Fig. 33. Residue from its linear interpolation is depicted in the lower part of the figure. The targetted parameter in case of the current sensing is only the transfer function sensitivity as described in the previous section.

Parameter	Sensitivity	Output offset
Input voltage sensing	4.41 $mV\,V^{-1}$	1.36 mV
Output voltage sensing	5.83 $mV\,V^{-1}$	5.93 mV
Inductor current sensing	92.56 $mV\,A^{-1}$	

Table 14 Summary of the signal conditioning parameters acquired by calibration

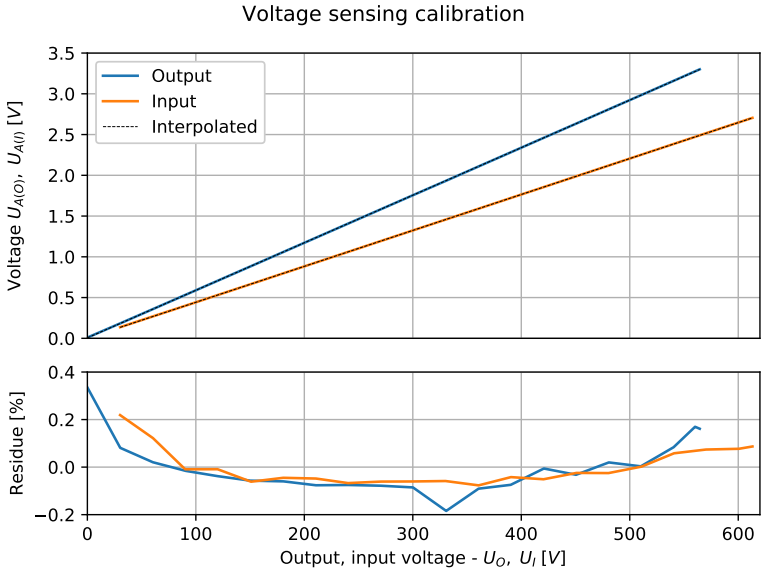


Figure 32 Transfer characteristics of input and output voltage sensing

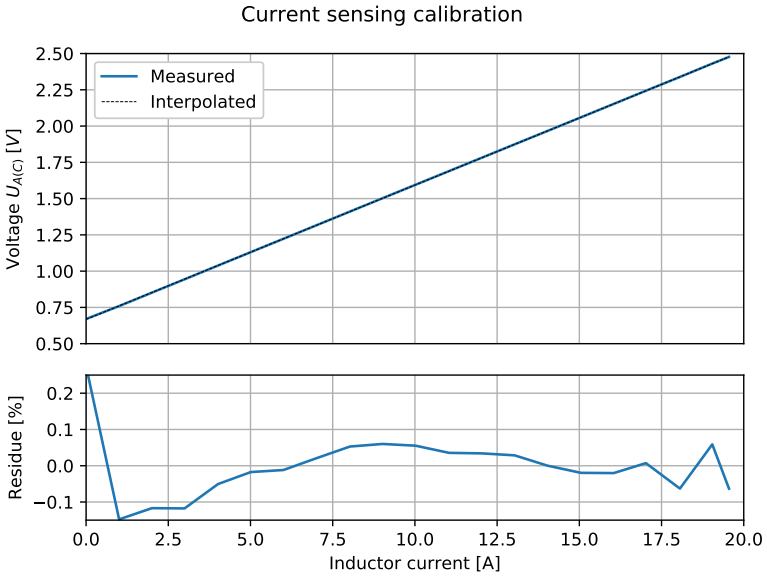


Figure 33 Transfer characteristics of inductor current sensing circuitry

The parameters of the signal conditioning are summarized in Tab. 14.

3.5 Control unit powering

A galvanic isolated power supply powers the secondary part of the optoisolation amplifiers. The power supply is based on an isolated DC/DC converter that also provides non-isolated powering for the control unit signal conditioning and the MCU. It produces a stabilized voltages from the supply rail common for the control unit and the primary side of the power stage.

The DC/DC converter is based on a modified buck topology, so-called flyback-buck. The principle schematic of the converter is shown in Fig. 34. The flyback-buck is a simple modification of the buck topology when instead of ordinary inductor a primary winding of a transformer is used.

3.5.1 Flyback-Buck operation

The primary side of the converter can be driven as in case of an ordinary buck converter with a freewheeling diode or with a half-bridge providing synchronous rectification.

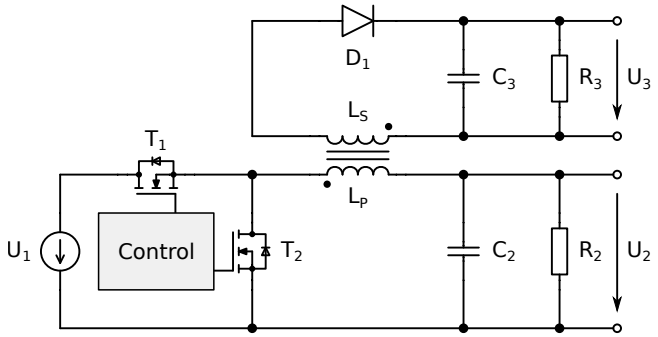


Figure 34 Basic schematic of flyback-buck DC/DC converter

The secondary winding is connected to a one-way rectifier. The rectifier is connected in a direction, so when a high-side switch is switched on, and the transformer primary winding is being magnetized, the diode blocks the secondary voltage. Given the primary side, the operation is identical with the standard buck converter.

If the synchronous rectification is used as in the case of the control unit powering, the operation of the converter can be divided into two subintervals. At the first time instance when $t \in (t_0, t_0 + \delta T_S)$, the high-side transistor T_1 is switched on. A current starts flowing through the primary winding of the transformer, causing the magnetization of the transformer core. The primary current splits into the primary load R_2 and into the primary output capacitor C_2 as depicted by the schematic diagram of the equivalent circuit in Fig. 35a. The current $i_P(t)$ rises with a slope

$$\frac{di_P(t)}{dt} = \frac{U_1 - u_2(t)}{L}. \tag{3.43}$$

If the primary capacitor is high enough to filter the current harmonics, the output voltage can be assumed to be constant with a negligible switching ripple, thus $u_2(t) \approx U_2$. In such a case, the primary current rises with an approximately constant slope.

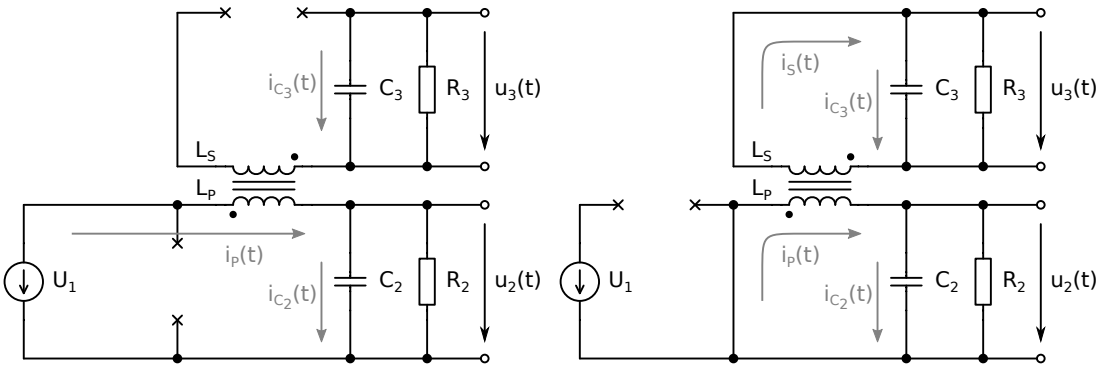
At this point, the secondary winding reflects the primary voltage, which is negative relative to the output diode. The output rectifier is not conducting. Hence, the secondary load consumes energy from the secondary capacitor C_3.

During the second time interval when $t \in (t_0 + \delta T_S, t_0 + T_S)$, the high-side switch is blocking and the low-side switch is conducting. At this point, a negative voltage is connected to the transformer primary winding, causing the secondary winding voltage is positive relative to the secondary side rectifier. Thus the secondary side diode is forward biased and current recharging the secondary side capacitor C_3 is drawn from the transformer. The schematic diagram of the equivalent circuit is shown in Fig. 35b.

The secondary current $i_S(t)$ transforms to the primary side and causes a further decrease of the primary current. The primary winding current can be expressed as [16]

$$i_P(t) = i_\mu(t) + \hat{i_S}(t) = i_\mu(t_0) + \frac{1}{L_P}\int_{t_0}^{t_0+t} u_P(\tau)\, d\tau + \frac{1}{k}\sqrt{\frac{L_P}{L_S}}\, i_S(t), \tag{3.44}$$

where $i_\mu(t_0)$ is the initial magnetization current, k is the transformer coupling ratio, and $\hat{i_S}(t)$ is the secondary side current transformed to the primary.



a) Equivalent circuit when high-side switch is on

b) Equivalent circuit when low-side switch is on

Figure 35 Equivalent circuits of each subinterval of flyback-buck operation

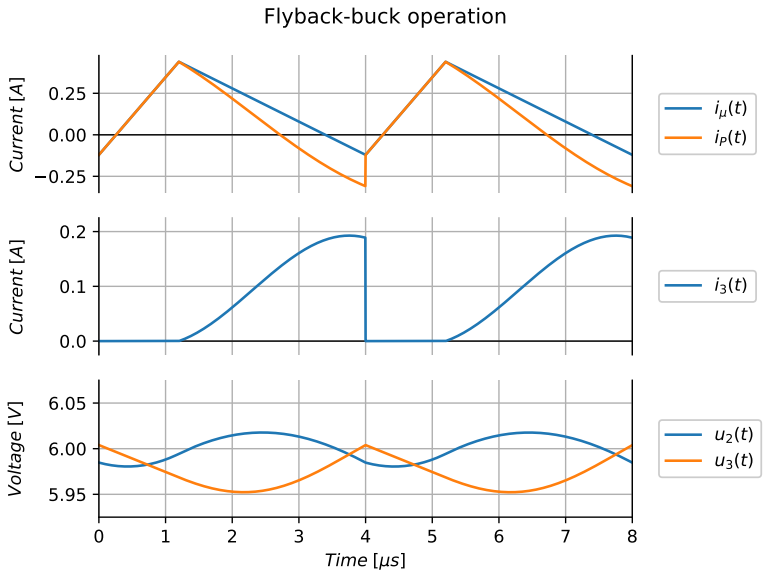


Figure 36 Waveforms of the primary current $i_P(t)$, magnetization current $i_\mu(t)$, secondary and primary voltages $u_2(t)$ and $u_3(t)$

Fig. 36 shows simplified waveforms of the primary winding current $i_P(t)$, primary magnetizing current $i_\mu(t)$, primary winding voltage $u_P(t)$ and the secondary winding current $i_S(t)$. The waveforms are depicted for a transformer with primary to secondary ratio close to one.

The waveform of the current during the on-time of the low-side switch is greatly influenced by the value of the capacitor C_3 and the leakage inductance of the transformer. The leakage inductance is caused by the non-ideal coupling between the primary and the secondary winding. The value of leakage inductance referenced to the secondary winding can be obtained by

$$L_{SL} = L_S \left(1 - k^2\right), \tag{3.45}$$

where L_S is the inductance of the secondary winding. The leakage inductance forms a series resonant circuit with the capacitor C_3. This resonant circuit is coupled through the transformer to the primary side. If the resonant frequency of the leakage inductance and the capacitor C_3 series connection is comparable with the converters switching frequency or is even higher, unwanted oscillations may appear on the primary current as well as on the secondary side.

3.5.2 The flyback-buck realization

The flyback-buck converter is realized with the use of L6984. The L6986 is a synchronous step-down converter that is able of the output current up to 1.5 A [37]. The L6986 converter includes both, the high-side and the low-side transistors of the synchronous buck half-bridge. The L6986 can operate in two modes, a low consumption mode, and a low noise mode.

In case of the low consumption mode, switching of the converter can be postponed as a consequence of a light load [37]. In such a case the device enters the so-called burst mode to minimize the switching loses and retain as high efficiency as possible. However, this mode of operation cannot be used in case of the flyback-buck topology since the

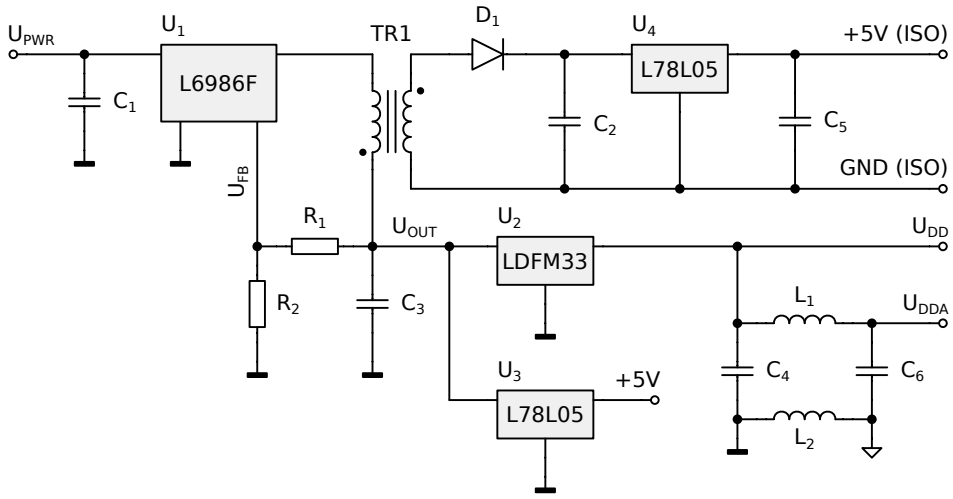


Figure 37 Simplified schematic diagram of control unit powering

converter terminates the switching of the low-side switch under the light load condition. Hence, only the low-side MOSFET body diode is conducting, and the converter operates in DCM during the burst mode.

In the case of the flyback-buck topology, the converter is set to operate in low noise mode. During the low noise mode operation, the converter switches with a fixed PWM frequency. This PWM frequency remains unchanged at any output load, and the principle of operation described in the previous section remains valid. The voltage regulation is derived from the primary output voltage. A voltage divider is used to sense the output voltage.

A simplified schematic diagram of the control unit powering is shown in Fig. 37. Note that it is rather block diagram showing the basic principle and power distribution of all signal conditioning blocks. For the complete schematic diagram of the control unit powering see Fig. 94 in Appendix A.

A commercial transformer from Würth has been used to speed up the control unit design and development instead of manufacturing a custom one. The transformer details are summarized in Tab. 15. The transformer has two secondary windings. The one with the lower secondary to primary winding ratio is used for the isolated power supply of the optoisolation amplifiers. The other winding is not used and is only connected via a rectifier diode to a capacitor.

Parameter	Value
Primary inductance	28 μH
Secondary one inductance	15.8 μH
Primary to secondary one ratio	$1.33 \div 1$ –
Primary to secondary twp ratio	$2 \div 1$ –

Table 15 Summary of key parameters of the transformer used for the DC/DC realization

The primary side of the DC/DC converter is used to power the MCU and the signal conditioning blocks. The flyback-buck primary voltage that is being regulated by the L6986 controller is set to a value higher than five volts. An LDO L78L05 is used to produce fixed voltage for the analog circuitry. Another 3.3 V LDO connected to the U_{OUT} is used for powering the MCU. The analog supply voltage for the MCU that is primarily used for the internal ADC and DAC is derived from the U_{DD} voltage. A

Ferrite Bead decouples the analog voltage. Similarly, the analog ground as marked by the triangular sign in the schematic is decoupled as well.

Since the DC/DC controller does not directly regulate the secondary side voltage, it is worthwhile to account with some voltage margin above the output voltage provided by the five volts LDO regulator L78L05 that is used for powering the isolated side of optoisolation amplifiers.

The parameters of the DC/DC powering the control unit are summarized in Tab. 16.

Parameter	Value
External power supply voltage U_{PWR}	20 V
Primary voltage U_{OUT}	6.52 V
Secondary one no-load voltage	8.7 V
Operating frequency	250 kHz
Primary side current ripple at no-load	615 mA

Table 16 Summary of DC/DC operating conditions

3.6 Control unit communication interface

The communication interface of the control unit is equipped with a USB-Mini Type B connector. In fact that the used MCU does not include a USB interface, an external USB to UART converter is made by use of dedicated IC. For this purpose, FT230X from FTDI Chip was used. The FT230X is a basic USB to UART converter without any other special functionalities [38]. This particular device was chosen as it needs a minimum of external components compared to other converters.

The block diagram of the communication interface is a part of the block diagram of the entire control unit presented at the beginning of this chapter in Fig. 23. The complete schematic diagram of the communication interface can be seen in Fig. 98 in Appendix A.

The communication interface uses USB-Mini Type B connector as it is a compromise between a robust and compact connector. The USB interface includes an ESD protection close to the connector. The communication interface was designed according to the design recommendations mentioned in the FT230X device datasheet.

A digital isolator ADUM1412 provides the galvanic insulation of the UART. It is a quad channel digital isolator providing two independent channels in both directions. The ADUM1412 can be powered by either 3.3 V or 5 V power supply. It offers relatively high data rates, up to 10 $Mbps$ which is far enough for running UART communication at baud rate 115.2 $kBdps$.

3.7 Realization of the control unit

This section gives a brief overview of the control unit development process starting from the prototype until the latest working version.

The very first prototype of the control unit was made on a piece of prototyping PCB. An externally connected development kit Nucleo-64 with STM32F334R8 microcontroller was connected to the signal conditioning blocks on the prototyping board. This module was only used initially to test the configuration of the MCU and test the signal conditioning blocks. However, this prototype did not perform well so a new prototype, referred to as the first working prototype, was created.

3.7.1 Control unit prototype

The prototype of the control unit was created on a single-sided home-made PCB. This prototype was assembled with STM32F334C8 microcontroller. It is a 48-pin version of the same microcontroller used in the very first experiment. The prototype was already powered by the flyback-buck based DC/DC as described in section 3.5.

The image of the prototype is shown in Fig. 38. Externally connected ST-Link-V2 module from Nucleo-64 development kit provided the UART to USB converter for communication with host PC since there was no integrated communication interface. The ST-Link module does not come with galvanic insulation, so the connection was often broken by conductive EMI when the power converter was active. Unstable communication was the primary motivation to include a galvanically insulated communication interface in the final version of the control unit.

The prototype was equipped with nearly the same signal conditioning blocks, except the fast window comparator employed for the overcurrent protection. This version of the control unit was used primarily for debugging.

3.7.2 Final version of the control unit

The second prototype, or rather the final version in term of this work, was made based on the knowledge from constructing the previous prototypes. This version is made according to the latest specification and includes all the functionalities described in previous sections.

The control unit is made on a two-sided PCB. The core of the control unit that contains the microcontroller and all the signal conditioning blocks are concentrated in a rectangular area that is covered by an SMD type metal shielding cover. The shielding box is used to reduce the level of EMI from the converter power stage that could disturb the inductor current and input and output voltage signal conditioning.

Since the shielding cover is of thin metal plate approximately 0.2 mm thin, it is not efficient in shielding relatively low frequencies produced by the converter. However, its primary purpose is to minimize the level of the capacitive coupling from the half-bridge and reduce interference with DC/DC converters of gate driver modules.

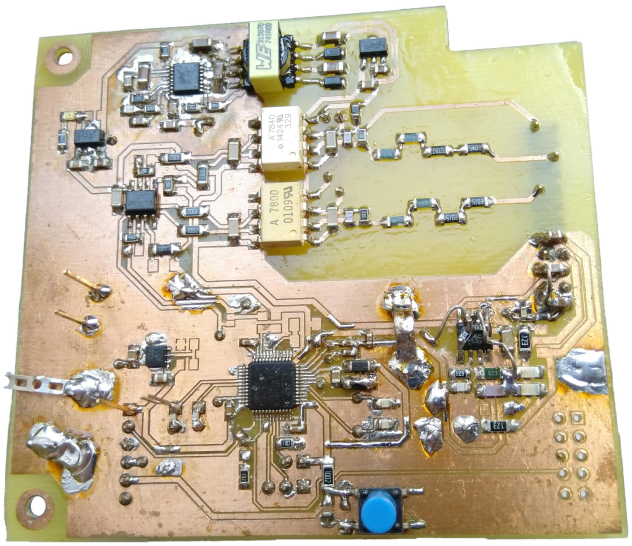


Figure 38 Photo of the prototype of the control unit made on single-sided PCB

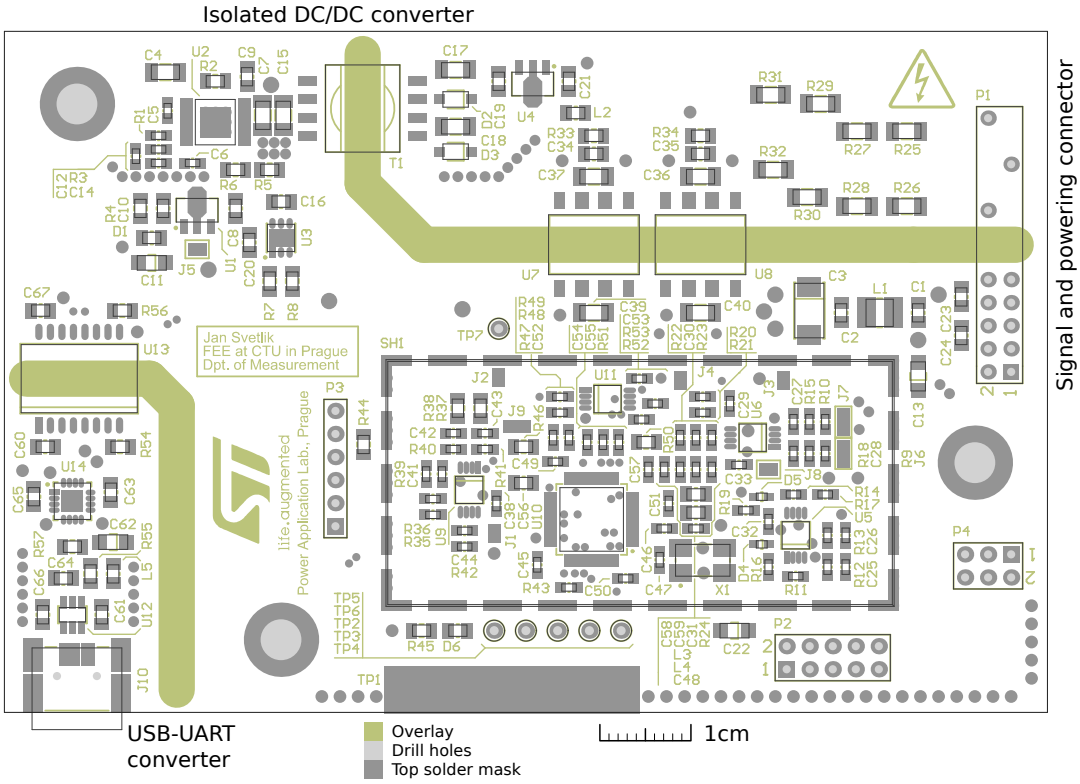


Figure 39 Design drawing of the final version of the control unit

A design drawing of the control unit is shown in Fig. 39. The metal shielding box footprint is marked by the double line bounding rectangle marked by the *SH1* designator. The connector on the top right side of the PCB is the powering and signal connector used to connect the control unit to the power stage. This connector provides the input and output voltage of the converter and with a current transducer signal. The devices *U7* and *U8* above the shielding box are the optoisolation amplifiers. The ara above the optoisolation amplifiers is galvanically connected with the power stage and is exposed to relatively high voltage.

The isolated DC/DC can be seen on the left upper corner, and the communication interface is loaded on the left lower corner. It is located as far from the power stage as possible. The thick lines around the communication interface and under the optoisolation amplifiers and the DC/DC transformer *T1* marks the galvanic insulation creepage. The control unit is also equipped with test points that can be used for debugging.

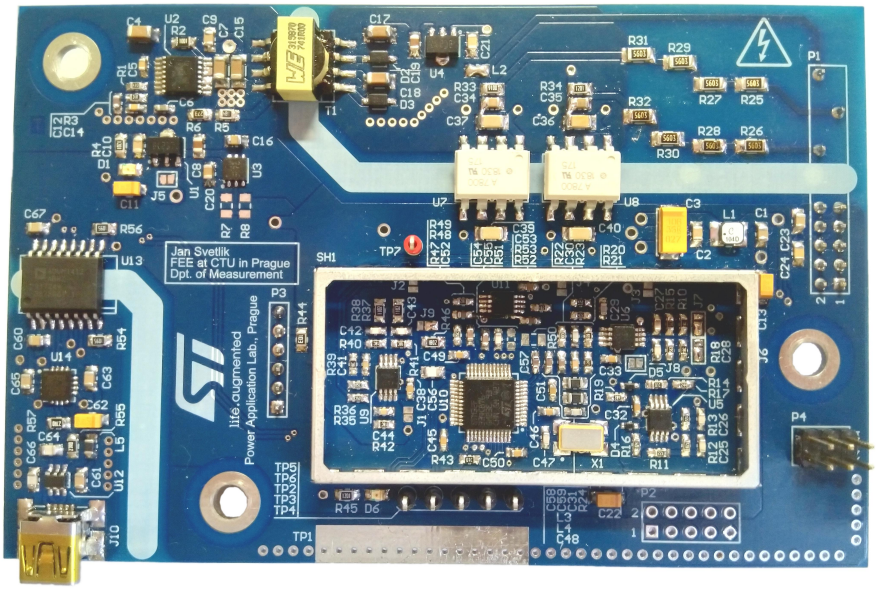


Figure 40 Photo of the control unit prototype

A photo of the control unit with uncovered signal signal processing part is shown in Fig. 40.

4 Analysis and modeling of the converter

This chapter focuses on deriving the converter model as of the dynamic system. The obtained mathematical model is used for further analysis of the system behavior under various conditions. The derived model was used for creating simulations in Python programming language for testing the open loop and closed loop behavior of the converter.

4.1 Modeling the dynamic behavior of the converter

It is desirable to neglect all the dynamics and transients that are faster than the converter operating frequency in order to get the approximation of the converters dynamic behavior. It is evident that the switching transients will not significantly influence the behavior of the converter at frequencies much lower than the operating frequency [1].

However, the switching losses can add to the other conductive losses in the converter and commonly can influence the overall dynamic behavior. At this point, for simplicity, we neglect the switching loses and perform the analysis for the conductive states of the converter ignoring the switching transients.

Now let us suppose the dominant converter behavior is significantly slower than the converters operating frequency. Then we can assume that the state of the converter will not change dramatically between two neighboring converter cycles. To express this small change of the converter state between two switching periods, we define the cycle mean value $\langle x(t) \rangle_{T_S}$ of all observed quantities.

4.1.1 High-side transistor switched on subinterval analysis

During the time interval $t \in (t_0 + T_s, t_0 + \delta T_s)$, the high-side transistor is switched on. The converter equivalent curcuit schematic diagram during this time instant is shown in Fig. 41.

We can express the inductor voltage using the second Kirchhoff's law as

$$u_L(t) = u_1(t) - R_1 i_L(t) - u_2(t), \tag{4.1}$$

where $R_1 = R_{DS} + R_L$. It applies for the inductor voltage

$$L\frac{di_L(t)}{dt} = u_1(t) - R_1 i_L(t) - u_2(t). \tag{4.2}$$

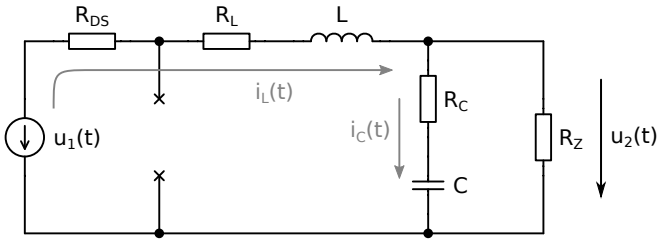


Figure 41 The synchronous buck equivalent circuit diagram in case the high-side switch is turned on

In this time instant, the output node's equation can be expressed using the first Kirchhoff's law

$$i_C(t) = i_L(t) - \frac{u_2(t)}{R_Z}. \tag{4.3}$$

It yields for the capacitor current

$$C\frac{du_C(t)}{dt} = i_L(t) - \frac{u_2(t)}{R_Z}. \tag{4.4}$$

To get the state representation of the system, it is worthwhile to express the output voltage $u_2(t)$ in terms of the state variables, that are in this case $i_L(t)$ and $u_C(t)$. The state vector is then $\mathbf{x}(t) = \begin{pmatrix} i_L(t) & u_C(t) \end{pmatrix}$. For this we can use the output node equation. According to the first Kirchhoff's law, it stands for the output node

$$i_L(t) - \frac{u_2(t) - u_C(t)}{R_C} - \frac{u_2}{R_Z} = 0. \tag{4.5}$$

By solving the equation for $u_2(t)$ we obtain

$$u_2(t) = \frac{R_Z R_C}{R_Z + R_C} i_L(t) + \frac{R_Z}{R_Z + R_C} u_C(t) = R_{out} i_L(t) + k_Z u_C(t), \tag{4.6}$$

Replacing the $u_2(t)$ and putting the equations together yields the state space representation of the converter when the high-side transistor is conducting.

$$L\frac{di_L(t)}{dt} = u_1(t) - i_L(t)\,(R_1 + R_{out}) - k_Z u_C(t), \tag{4.7}$$

$$C\frac{du_c(t)}{dt} = k_Z i_L(t) - \frac{k_Z}{R_Z} u_C(t). \tag{4.8}$$

The output equation is identical to (4.6).

4.1.2 Low-side transistor switched on subinterval analysis

When the time interval $t \in (t_0 + \delta T_s, t_0 + T_s)$ starts, the high-side switch is turned off and the low-side switch starts conducting. In this case, the converter is described by a different set of equations as the sub-circuit changes. The schematic diagram of the equivalent circuit of the converter is shown in Fig. 42.

For now, the deadtime insertion between the high-side transistor is switched off, and the low-side is driven on, is neglected as it makes the modeling much more complicated. The influence of the dead time is going to be discussed in section 4.2.3.

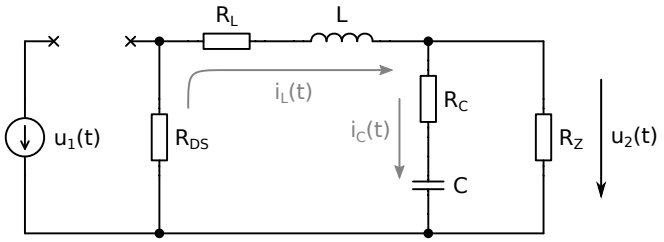


Figure 42 The synchronous buck equivalent circuit diagram in case the low-side switch is turned on

For the inductor voltage during the second time interval, we get an equation

$$u_L(t) = L\frac{di_L(t)}{dt} = -u_2(t) - R_1 i_L(t). \tag{4.9}$$

Proceeding the same way as in the previous case, we can express the capacitor current in a way

$$i_C(t) = C\frac{du_C(t)}{dt} = i_L(t) - \frac{u_2(t)}{R_Z}. \tag{4.10}$$

The output node equation remains the same as (4.5). The output voltage expressed in terms of the state variables remains the same. By replacing the output voltage given by (4.6) in both state equations and performing simplification, we are finished with the state representation of the converter during the second subinterval. The state equations are as follows

$$L\frac{di_L(t)}{dt} = -i_L(t)\left(R_1 + R_{out}\right) - k_Z u_C(t), \tag{4.11}$$

$$C\frac{du_C(t)}{dt} = k_Z i_L(t) - \frac{k_Z}{R_Z}u_C(t). \tag{4.12}$$

The output equation remains the same as it was in the case of the previous subinterval

$$u_2(t) = R_{out} i_L(t) + k_Z u_C(t). \tag{4.13}$$

4.2 Obtaining the averaged converter model

The converter is described by two sets of two ordinary differential equations. Each set of the equations describes the converter in the corresponding time interval when one of the power transistors is conducting, and the other one is closed. Following the approach described in [1] we can get the averaged state space model by merely evaluating the cycle mean value of the converter quantities over the switching period. By this, we obtain the cycle mean value of the converter state space representation

$$\langle \mathbf{x}(t) \rangle_{T_S} = \frac{1}{T}\int_t^{t+T_S} \mathbf{x}(\tau)\, d\tau. \tag{4.14}$$

4.2.1 Inductor cycle mean current

The inductor current during the first interval $t \in (t_0, t_0 + \delta T_S)$ is given by the solution of the ordinary differential equation

$$L\frac{i_L(t)}{dt} = u_L(t), \tag{4.15}$$

with initial condition $i_L(t_0)$. Solving the equation to obtain the inductor current at the end of the first subinterval $t = t_0 + \delta T_s$ we get

$$i_L\left(t_0 + \delta T_S\right) = \int_{t_0}^{t_0+\delta T_S} u_L(t)\, dt + i_L\left(t_0\right). \tag{4.16}$$

For the second time interval, we solve the inductor current equation the same way to get the inductor current at time $t = t_0 + T_S$ considering the initial condition the current at time $t = t_0 + \delta T_S$ — the inductor current at the end of the previous interval.

$$i_L\left(t_0 + T\right) = \frac{1}{L}\int_{t_0+\delta T_s}^{t_0+T_S} u_L(t)\,dt + i_L\left(t_0 + \delta T\right). \tag{4.17}$$

By substituing the term $i_L\left(t_0 + \delta T_S\right)$ in (4.17) by (4.16) we get the equation for the current at the end of the switching interval.

$$i_L\left(t_0 + T\right) = \frac{1}{L}\int_{t_0+\delta T_s}^{t_0+T_S} u_L(t)\,dt + \frac{1}{L}\int_{t_0}^{t_0+\delta T_S} u_L(t)\,dt + i_L\left(t_0\right). \tag{4.18}$$

The integrals can be combined as they integrate the same function over neighboring intervals. Rearranging the equation we obtain

$$i_L\left(t_0 + T\right) - i_L\left(t_0\right) = \frac{1}{L}\int_{t_0}^{t_0+T_S} u_L(t)\,dt \tag{4.19}$$

The cycle mean value of any quasi-periodic function $f(t)$ over period T is given by

$$\langle f(t)\rangle_T = \frac{1}{T}\int_{t}^{t+T} f(\tau)\,d\tau. \tag{4.20}$$

Comparing (4.19) with (4.20) we can modify the inductor current change into the form

$$i_L\left(t_0 + T\right) - i_L\left(t_0\right) = \frac{T_S}{L}\left\langle u_L(t)\right\rangle_{T_S}. \tag{4.21}$$

Dividing the (4.21) by the switching period, we get the derivative of cycle mean value of the inductor current. It applies for an arbitrary function $f(t)$ which is continuous and restricted on the interval $t \in (t_0, t_0 + T_S)$

$$\frac{d\left\langle f(t_0)\right\rangle_{T_S}}{dt} = \frac{f\left(t_0\right) - f\left(t_0 + T_S\right)}{T_S}. \tag{4.22}$$

Modifying (4.21) we get the expression for the inductor current slope between two neighbouring switching intervals [1].

$$L\frac{i_L\left(t_0 + T_S\right) - i_L\left(t_0\right)}{T_S} = L\frac{d\left\langle i_L(t_0)\right\rangle_{T_S}}{dt} = \left\langle u_L(t_0)\right\rangle_{T_S}. \tag{4.23}$$

At this point, we only need to express the cycle mean of the inductor voltage, which is given by

$$\left\langle u_L\left(t_0\right)\right\rangle_{T_S} = \frac{1}{T_S}\left(\int_{t_0}^{t_0+\delta T_S} u_L(t)\,dt + \int_{t_0+\delta T_s}^{t_0+T_S} u_L(t)\,dt\right). \tag{4.24}$$

Substituting the integrals by inductor voltages at the given sub-intervals yields the equation

$$\begin{aligned}\left\langle u_L(t_0)\right\rangle_{T_S} = \frac{1}{T_S}\Bigg(&\int_{t_0}^{t_0+\delta T_S}\left(u_1(t) - \left(R_1 + R_{out}\right)i_L(t) - k_Z u_C(t)\right)\,dt \\ &+ \int_{t_0+dT_s}^{t_0+T_S}\left(-\left(R_1 + R_{out}\right)i_L(t) - k_Z u_C(t)\right)\,dt\Bigg).\end{aligned} \tag{4.25}$$

Adding the integral terms together we obtain

$$\langle u_L(t_0)\rangle_{T_S} = \frac{1}{T_S}\left(\int_{t_0}^{t_0+\delta T_S} u_1(t)\,dt - (R_1+R_{out})\int_{t_0}^{t_0+T_S} i_L(t)\,dt - k_Z\int_{t_0}^{t_0+T_S} u_C(t)\right). \quad (4.26)$$

If we compare the result with the equation of the cycle mean value, we can rewrite the cycle mean inductor voltage in the form

$$\langle u_L(t_0)\rangle_{T_S} = \frac{1}{T_S}\left(\delta T_S \langle u_1(t)\rangle_{T_S} - T_S (R_1+R_{out}) \langle i_L(t)\rangle_{T_S} - T_S k_Z \langle u_C(t)\rangle_{T_S}\right). \quad (4.27)$$

Finally, the first state equation of the converter for cycle mean value of the inductor current is in form

$$\frac{d\langle i_L(t)\rangle_{T_S}}{dt} = \frac{1}{L}\left(\delta \langle u_1(t)\rangle_{T_S} - (R_1+R_{out})\langle i_L(t)\rangle_{T_S} - k_Z \langle u_C(t)\rangle_{T_S}\right). \quad (4.28)$$

Note that the cycle mean value of the inductor voltage can be evaluated at any time. Hence, the symbol t_0, used previously to fix the computation to the beginning of the switching interval, can be replaced by t as the cycle mean value computing window can slide over the waveform continuously. The derived relationships remain valid.

4.2.2 Capacitor cycle mean voltage

Following the same procedure for the capacitor current, we obtain the equation for the total change of the capacitor voltage between two surrounding intervals

$$\frac{u_C(t_0+T_S) - u_C(t_0)}{T_S} = \frac{d\langle u_C(t_0)\rangle_{T_S}}{dt} = \frac{\langle i_C(t_0)\rangle_{T_S}}{C}. \quad (4.29)$$

It applies for the cycle mean value of the capacitor current

$$\langle i_C(t_0)\rangle_{T_S} = \frac{1}{T_S}\left(\int_{t_0}^{t_0+\delta T_S}\left(k_Z i_L(t) - \frac{k_Z}{R_Z}u_C(t)\right)dt + \int_{t_0+\delta T_S}^{t_0+T_S}\left(k_Z i_L(t) - \frac{k_Z}{R_Z}u_C(t)\right)dt\right) \quad (4.30)$$

Simplifying the equation yields

$$\langle i_C(t_0)\rangle_{T_S} = \frac{1}{T_S}\left(k_Z\int_{t_0}^{t_0+T_S} i_L(t)\,dt - \frac{k_Z}{R_Z}\int_{t_0}^{t_0+T_S} u_C(t)\,dt\right). \quad (4.31)$$

By comparing the result with the equation for the cycle mean value, we get

$$\langle i_C(t_0)\rangle_{T_S} = \frac{1}{T_S}\left(T_S k_Z \langle i_L(t_0)\rangle_{T_S} - T_S\frac{k_Z}{R_Z}\langle u_C(t_0)\rangle_{T_S}\right). \quad (4.32)$$

Finally, we can write the equation for the capacitor voltage

$$\frac{d\left\langle u_C(t_0)\right\rangle_{T_S}}{dt} = \frac{1}{C}\left(k_Z\left\langle i_L(t_0)\right\rangle_{T_S} - \frac{k_Z}{R_Z}\left\langle u_C(t_0)\right\rangle_{T_S}\right). \tag{4.33}$$

Now we are finished with the averaged state space representation of the converter dynamics. The set of the equations describing the time evolution of the cycle mean values of state variables is

$$L\frac{d\left\langle i_L(t)\right\rangle_{T_S}}{dt} = \delta(t)\left\langle u_1(t)\right\rangle_{T_S} - (R_1 + R_{out})\left\langle i_L(t)\right\rangle_{T_S} - k_Z\left\langle u_C(t)\right\rangle_{T_S}, \tag{4.34}$$

$$C\frac{d\left\langle u_C(t)\right\rangle_{T_S}}{dt} = k_Z\left\langle i_L(t)\right\rangle_{T_S} - \frac{k_Z}{R_Z}\left\langle u_C(t)\right\rangle_{T_S}. \tag{4.35}$$

The output voltage equation remains the same during both intervals so the cycle means value can be easily deduced

$$\left\langle u_2(t)\right\rangle_{T_S} = R_{out}\left\langle i_L(t)\right\rangle_{T_S} + k_Z\left\langle u_C(t)\right\rangle_{T_S}. \tag{4.36}$$

The cycle mean of the state vector was denoted earlier. In case of the cycle mean of the input vector $\langle \mathbf{u}(t)\rangle_{T_S}$, we need to define the inputs to the system first. Naturally, we define the duty cycle as one of the system inputs. Suppose the duty cycle is a time-varying, thus $\delta = \delta(t)$, we can see from (4.34) that the system is non-linear if taking the voltage $\langle u_1(t)\rangle_{T_S}$ as the other input. However, since we are not able to influence the input voltage, I will refer the input voltage as a disturbance factor. If the input voltage is constant, the system is in its linear form.

4.2.3 Deadtime influence on the converter modeling

The deadtime insertion causes, in this particular case, the current commutation through the transistor body diode. Which body diode conducts during the dead time depends on which subinterval we are interested in, and also on the converter operating point. Hence two cases need to be analyzed. The first case is when the low-side transistor body diode is conducting. The equivalent schematic of the converter in that state is shown in Fig. 43.

The transistor body diode can be approximated by a forward voltage drop U_{BD} and a differential resistance r_{BD} that is given by

$$r_{BD} = \frac{d\tilde{U}_{BD}}{d\tilde{I}_{BD}} \approx \frac{\Delta\tilde{U}_{BD}}{\Delta\tilde{I}_{BD}}, \tag{4.37}$$

where $\tilde{U}_{BD}$ is the body diode forward voltage at a particular operating current $\tilde{I}_{BD}$.

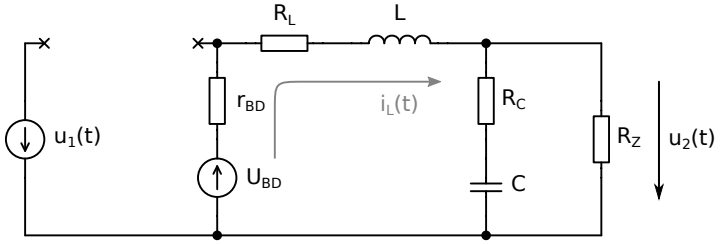


Figure 43 Equivalent circuit schematic diagram in case the low-side transistor body diode is conducting

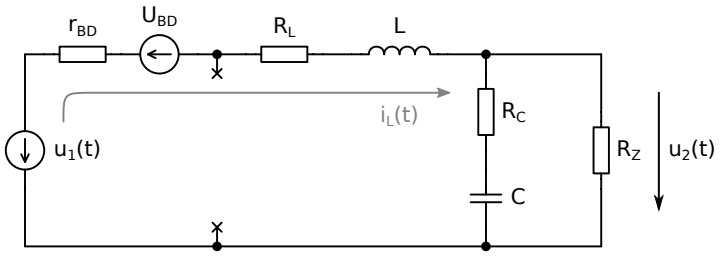


Figure 44 Equivalent circuit schematic diagram in case the high-side transistor body diode is conducting

The low-side MOSFET body diode conducts in case of the high-side switch was conducting and was switched off. During the steady state operation of the converter, this causes the inductor current reaches its positive peak value. Also, it conducts at the switch off of the low-side switch in case the converter is operating under the load, and the cycle mean value of the inductor current is higher than the half of the current ripple. In both cases, the equivalent circuit is shown in Fig. 43. The equation for the inductor voltage is in form

$$L\frac{di_L(t)}{dt} = -i_l(t)\left(R_{out} + R_L + r_{BD}\right) - U_F - k_Z u_C(t). \tag{4.38}$$

The second case is when a high-side MOSFET body diode is conducting. The equivalent schematic diagram of this state is shown in Fig. 44. Note the same notation for the body diode, as we assume that same transistor are used, so the body diode properties are similar.

In such a case, the inductor voltage is given by

$$L\frac{di_L(t)}{dt} = -i_L(t)\left(R_{out} + R_L + r_{BD}\right) + U_F - k_Z u_C(t) + u_1(t). \tag{4.39}$$

The high-side transistor body diode conducts in case the cycle mean value of the inductor current is lower than half of the current ripple. It is important to note that the capacitor current equation and the output equation remains the same.

It can be seen that the body diode conductivity during the dead time would add some additional loses to the averaged model caused by body-diode forward voltage and it's differential resistance r_{BD}. Especially the forward voltage of the SiC MOSFET body-diode can be very high and can be more significant in the case when estimating the converter efficiency. Hence, it is desirable to make the deadtime as short as possible.

The equations for the inductor current during the dead time differs. Moreover, which body diode is conducting at the end of the second subinterval depends on the converter operation. Thus, incorporating the body diode model into the averaged state space model would be complicated. But as stated before, it desirable to have the dead time as short as possible so in such a case, we can neglect the influence if the deadtime duration is many times shorter than the switching period — $2t_{DT} \ll T_S$. The body diode conduction can, however, be easily incorporated in numerical simulations.

4.2.4 Linear approximation of the converter model

The state space model can be easily solved by numerical methods, creating a simulation of the converter behavior. Nevertheless, for the compensator design, it is useful to have a linearized state space model. From the linearized model, we can get the transfer

functions at different conditions at a particular operating point. It holds for the state space representation of the converter

$$\frac{d}{dt}\left\langle \mathbf{x}(t)\right\rangle_{T_S} = \mathbf{F}\left(\left\langle \mathbf{x}(t)\right\rangle_{T_S}, \left\langle \mathbf{u}(t)\right\rangle_{T_S}\right). \tag{4.40}$$

To find the linear approximation of the state space model around a particular operating point $P_0 = \begin{pmatrix} \mathbf{x}_0 & \mathbf{u}_0 \end{pmatrix}$ we convert the state equations into the Taylor series

$$\mathbf{F}\left(\mathbf{x},\mathbf{u}\right) = \mathbf{F}\left(\mathbf{x}_0,\mathbf{u}_0\right) + \sum_{k=1}^{n} \frac{\left(\left(\mathbf{x}-\mathbf{x}_0\right) grad\right)^k \mathbf{F}\left(\mathbf{x}_0,\mathbf{u}_0\right)}{n!} + \sum_{k=1}^{n} \frac{\left(\left(\mathbf{u}-\mathbf{u}_0\right) grad\right)^k \mathbf{F}\left(\mathbf{x}_0,\mathbf{u}_0\right)}{n!} + \mathcal{R}_n, \tag{4.41}$$

where $\mathcal{R}_n$ is a residue. Taking into account only the first order term and expanding the gradient operator we can write

$$\mathbf{F}\left(\mathbf{x},\mathbf{u}\right) \approx \mathbf{F}\left(\mathbf{x}_0,\mathbf{u}_0\right) + \sum_{i=1}^{m} \frac{\partial \mathbf{F}}{\partial x_i}\Delta x_i + \sum_{i=1}^{p} \frac{\partial \mathbf{F}}{\partial x_i}\Delta u_i, \tag{4.42}$$

where m is the number of the state variables, and p is the number of inputs to the system. It applies for the derivation of the state vector around the operating point

$$\frac{d\mathbf{x}}{dt} = \frac{d\mathbf{x}_0}{dt} + \frac{d\Delta\mathbf{x}}{dt} = \mathbf{F}\left(\mathbf{x},\mathbf{u}\right). \tag{4.43}$$

Since

$$\frac{d\mathbf{x}_0}{dt} = \mathbf{F}\left(\mathbf{x}_0,\mathbf{u}_0\right), \tag{4.44}$$

we can subtract both terms from corresponding sides of the equation (4.43). Doing this we get the linear approximation of the state space model for small signals

$$\frac{d\Delta\mathbf{x}}{dt} = \sum_{i=1}^{m} \frac{\partial \mathbf{F}}{\partial x_i}\Delta x_i + \sum_{i=1}^{p} \frac{\partial \mathbf{F}}{\partial x_i}\Delta u_i. \tag{4.45}$$

Similarly, we can perform a linear approximation of the output equation

$$\Delta\mathbf{y} = \sum_{i=1}^{m} \frac{\partial \mathbf{G}}{\partial x_i}\Delta x_i + \sum_{i=1}^{p} \frac{\partial \mathbf{G}}{\partial x_i}\Delta u_i, \tag{4.46}$$

where $\mathbf{y}$ is a vector of output variables. The output vector, in the case of the synchronous buck converter, is in form

$$\mathbf{y}(t) = \begin{pmatrix} \left\langle u_2(t)\right\rangle_{T_S} & \left\langle i_L(t)\right\rangle_{T_S} \end{pmatrix}^T. \tag{4.47}$$

Hopefully, the output equation of the state space model is already in its linear form, so it is not needed to perform the derivatives of the output mapping function. However, this may not be the case of other topologies. For example, in the case of synchronous boost, both, the state equations and the output equations are highly non-linear. In such a case, proceeding with the linear approximation around the operating point will simplify the compensator design, but even with a linearized system, special care has to be taken to examine the regulation performance and CL stability outside, or far from the operating point.

Having the linear approximation of the system the converter state equations can be written in the well-known matrix form

$$\frac{d\Delta\mathbf{x}}{dt} = \mathbf{A}\Delta\mathbf{x}(t) + \mathbf{B}\Delta\mathbf{u}(t), \tag{4.48}$$

$$\Delta\mathbf{y} = \mathbf{C}\Delta\mathbf{x}(t) + \mathbf{D}\Delta\mathbf{u}(t). \tag{4.49}$$

In case of the synchronous buck converter, the linearized state-space model is as follows

$$\frac{d\Delta\mathbf{x}}{dt} = \begin{pmatrix} -\dfrac{(R_1 + R_{out})}{L} & -\dfrac{k_Z}{L} \\ \dfrac{k_Z}{C} & -\dfrac{k_Z}{CR_Z} \end{pmatrix} \Delta\mathbf{x}(t) + \begin{pmatrix} \dfrac{\langle u_1(t)\rangle_{T_S}}{L} & \dfrac{\delta(t)}{L} \\ 0 & 0 \end{pmatrix} \Delta\mathbf{u}(t), \tag{4.50}$$

$$\Delta\mathbf{y}(t) = \begin{pmatrix} R_C \parallel R_Z & k_Z \\ 1 & 0 \end{pmatrix} \Delta\mathbf{x}(t) + \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \Delta\mathbf{u}(t), \tag{4.51}$$

where k_Z is a substitution for

$$k_Z = \frac{R_Z}{R_Z + R_C}, \tag{4.52}$$

and R_{out} is a parallel combination of R_C and R_Z.

4.2.5 Getting transfer function matrix of the converter model

Since we have the linear approximation of the state space model of the converter, we can get the transfer function matrix. We can also analyze the system poles and zeros to get the necessary information for the controller design. The transfer function matrix can be obtained from the linear state space representation using Laplace transform in a way

$$\mathbf{H}(s) = \mathbf{C}\left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{B} + \mathbf{D}, \tag{4.53}$$

where $\mathbf{I}$ is the identity matrix. Following the state vector, input vector and output vector definitions from the previous section, the transfer function matrix is in form

$$\mathbf{H}(s) = \begin{pmatrix} \dfrac{U_2(s)}{\delta(s)} \\ \dfrac{I_L(s)}{\delta(s)} \end{pmatrix} = \begin{pmatrix} H_1(s) \\ H_2(s) \end{pmatrix}. \tag{4.54}$$

The element $H_1(s)$ is the transfer from the duty cycle of the PWM signal to the output voltage, while the term $H_2(s)$ denotes the transfer function from the duty cycle to the inductor current. It holds for the $H_1(s)$ transfer

$$H_1(s) = \frac{U_1(s)R_Z}{R_1 + R_Z} \frac{1 + sCR_C}{1 + s\left(C\left(R_C + R_1 \parallel R_Z\right) + \dfrac{L}{R_1 + R_Z}\right) + s^2CL\dfrac{R_C + R_Z}{R_1 + R_Z}}. \tag{4.55}$$

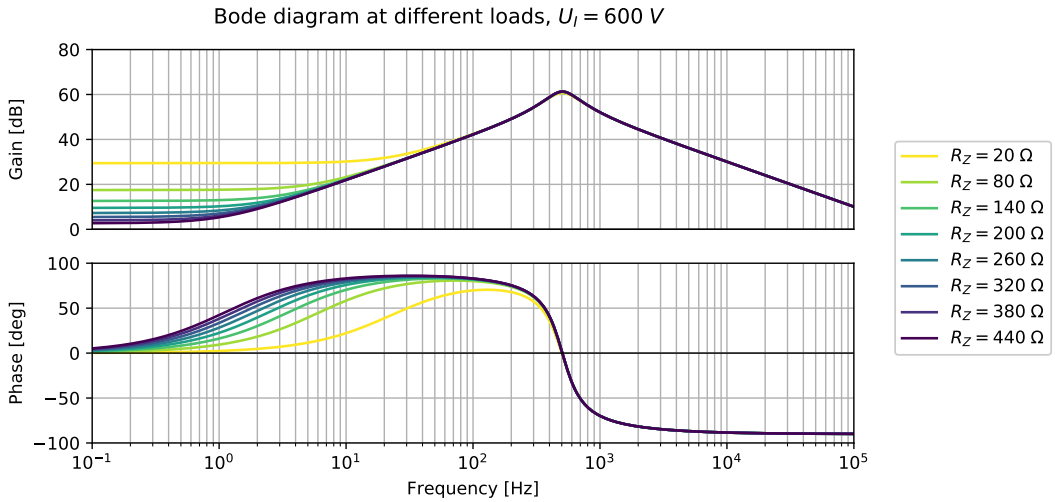


Figure 45 Bode diagram of the duty cycle to the inductor current transfer function

The transfer function $H_2(s)$ is given by

$$H_2(s) = \frac{U_1(s)}{R_1 + R_Z} \frac{1 + sC\left(R_C + R_Z\right)}{1 + s\left(C\left(R_C + R_1 \parallel R_Z\right) + \dfrac{L}{R_1 + R_Z}\right) + s^2 CL \dfrac{R_C + R_Z}{R_1 + R_Z}}. \tag{4.56}$$

Performing the linearization and proceeding with transfer function matrix evaluation under various conditions, a sweep analysis was done for observing the behavior of the converter under different loads or different input voltage levels.

4.2.6 Transfer function analysis for different conditions

Fig. 45 shows the Bode diagram of the duty cycle to inductor current transfer function. The transfer characteristic is evaluated at constant input voltage $U_1 = 600\ V$ for different values of the output load resistance. The load rezistance is swept in a linear range. With decreasing load resistance, the angular frequency of a zero present in the transfer function increases. The zero moves more to the left in the complex plane. Conversely, under the light load operation, the load resistance goes to high values. As a result, the zero of the transfer function moves to the right and limits to the origin of the complex plane for $R_Z \to \infty$. In such a case, the zero becomes more dominant at light load operation as its angular frequency ω_{Z1} decreases.

The angular frequency of the zero in the transfer function $H_2(s)$ is given by

$$\omega_{Z1} = \frac{1}{C\left(R_C + R_Z\right)}. \tag{4.57}$$

The DC gain of the transfer function $H_2(s)$ can be obtained by solving the limit

$$H_{20} = \lim_{s \to 0} H_2(s) = \frac{U_1}{R_1 + R_Z}. \tag{4.58}$$

This relationship implies that the load resistance change influences both, the dynamic behavior and the DC gain of the investigated transfer function.

On the other side, if the load resistance is kept constant, and the influence of the input voltage variation at a large scale is observed, only the DC gain of the transfer function

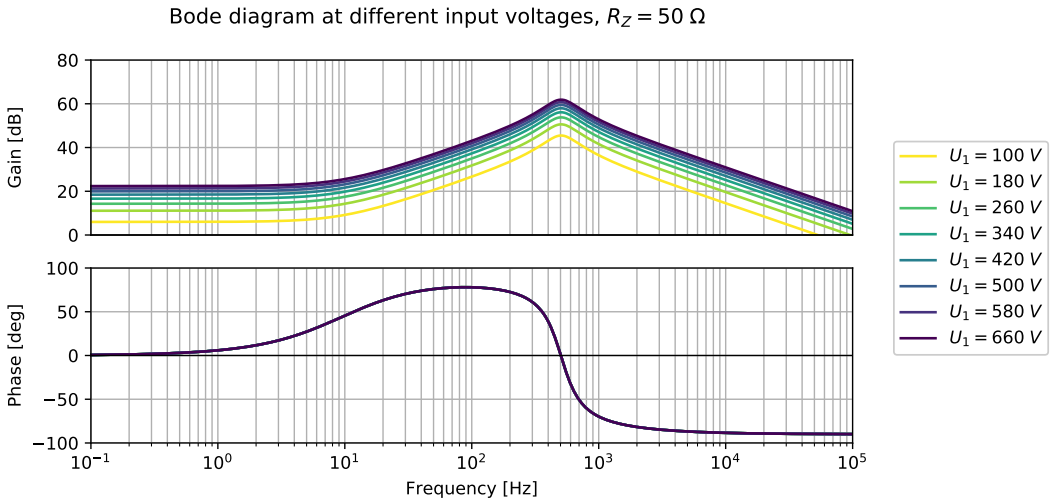


Figure 46 Bode diagram of the duty cycle to the inductor current transfer function

changes. This fact is proven by Bode diagram shown in Fig. 46. The load resistance is fixed to the value $R_Z = 50\ \Omega$ and the input voltage is swept with a constant step.

The behavior of the transfer function from the duty cycle to the output voltage is investigated the same way. Fixing the input voltage to be constant value $U_1 = 600\ V$ and performing the analysis for varius output loads with constant step, we get the set of transfer function characteristics. They are shown in Fig. 47.

It can be seen that under different loads that are in a range of reasonable values, the transfer function does not change significantly. Only for very high output loads, that are far above the maximum specified output power, the damping ratio is increasing, and the DC gain is decreasing. It applies for the DC gain of the $H_1(s)$ transfer function

$$H_{10} = \lim_{s \to 0} H_1(s) = U_1(s) \frac{R_Z}{R_Z + R_1}. \tag{4.59}$$

Since the R_1, which is a series connection of the drain-source on-state resistance of any MOSFET in the half-bridge and the inductor resistance R_L, is considerably lower than the resistance of the load R_Z, the DC gain does not vary substantially under different

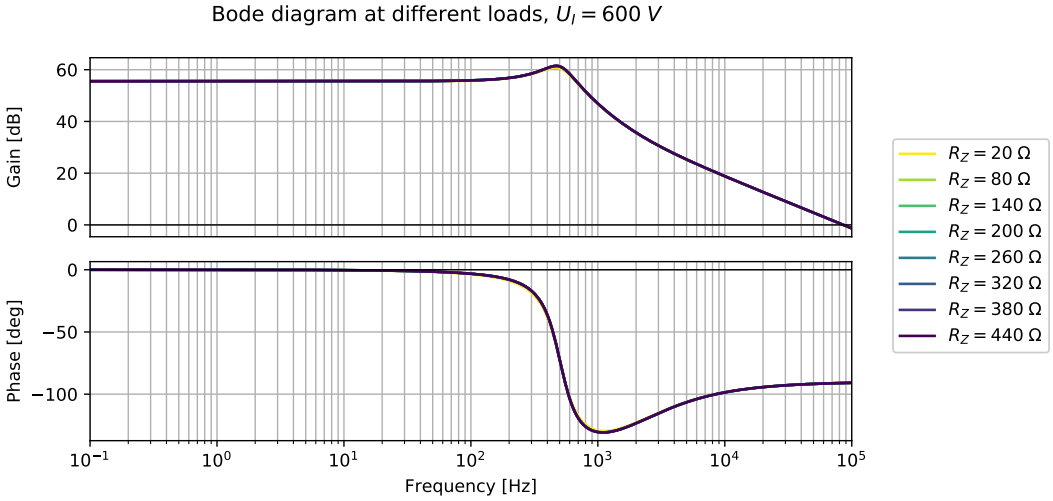


Figure 47 Bode diagram of the duty cycle to the output voltage transfer function

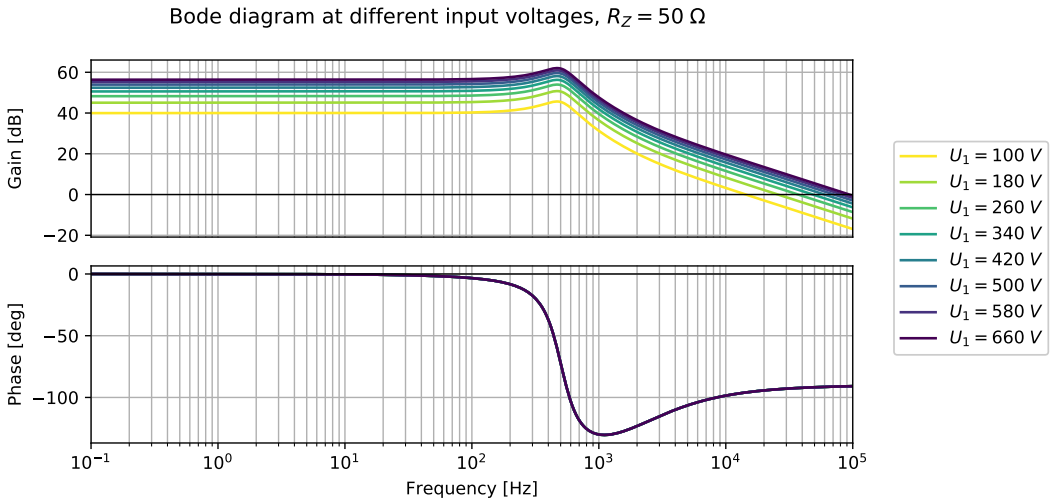


Figure 48 Bode diagram of the duty cycle to the output voltage transfer function

loads. The DC gain is influenced only when the resistance of the load is comparable with the R_1.

The DC gain of the transfer function is significantly influenced only by the input voltage. Bode plot of the transfer function for different input voltages, while the output load resistance is fixed to $R_L = 50\ \Omega$, is shown in Fig. 48. It is important to note that the input voltages are equally spaced.

5 Control unit core architecture

The control unit is implemented with the use of an STM32 microcontroller, more specifically an STM32F334C8 microcontroller was chosen. The microcontroller is used for measuring the converter signals and for the control outputs generation. The microcontroller also provides several kinds of protections.

The STM32F3 is a mainstream class of ARM Cortex-M4 based microcontrollers. The ARM Cortex-M4 is a high-end, 32-bit processor architecture well suited for the microcontrollers [3]. The ARM Cortex-M4 processors include a hardware floating point unit and a set of digital signal processing — DSP instructions, such as saturating arithmetic or packing and unpacking instructions [3]. These qualities in conjunction with relatively high performance make the ARM Cortex-M4 based microcontrollers capable of some tasks related to fast digital signal processing or for running control algorithms.

The STM32 microcontrollers are equipped with a variety of hardware peripherals. These peripherals are not part of the ARM Cortex-M4 core. However, they are interconnected with the core by a system bus. This interconnection allows fast and straightforward access to the peripherals from the application code. The STM32F3 family offers several types of timers, analog to digital or digital to analog converters, various types of communication interfaces, internal comparators and many other peripherals.

The STM32F334 series comes with a so-called High-Resolution Timer. It is a hardware peripheral specially designed to provide control for different classes of switching mode power supplies. It is a timer that can be used to generate PWM signals with very high time resolution even at higher frequencies. It is thus suitable for converter control as it preserves the high dynamic range of the 16-bit counter even at high output signal rates. The high-resolution timer is also equipped with a variety of protection mechanisms and external events that can be used to alter the timer operation without any software action. Moreover, it offers a high degree of interconnection with other on-chip peripherals and thus can be used for creating complex control schemes using different kinds of synchronization between analog to digital converters and other peripherals.

The control unit firmware uses the internal interconnection of the hardware peripherals of the MCU such as analog to digital converters, timers, digital to analog converters or DMA. The proper configuration and interconnection of the hardware peripherals allow to move some tasks to the hardware level and save the CPU software time.

The generation of the control signals for the converter or handling external fault events is done by hardware without any software intervention. The control loop algorithm and any other critical tasks such as communication to the host PC over the UART are done either by the device or by software executed in interrupt service routines. The interrupt service routines are managed by their configurable priorities. Hence the critical code such as the control algorithm is always run at the highest priority. This approach allows keeping the essential tasks running even the software in the main program loop is stuck at more sophisticated algorithms that are not time critical.

5.1 Control signal generation

The synchronous buck converter is driven by two complementary signals, each of them for one of the transistors in the half-bridge. For the control signal generation, the high-resolution timer peripheral is used. This section aims to provide an overview of the high-resolution timer operation and its usage for generating the control signals and handling fault events and states.

5.1.1 High-Resolution Timer overview

The high-resolution timer is equipped with a pseudo multiplier that allows the timer to be clocked at rates up to 32 times higher than the frequency of the system clock. The High-Resolution Timer can be clocked by either the system clock of the microcontroller or by internal PLL. In the later case, the timer clock frequency can be up to 4.608 GHz [17]. This configuration allows generating a PWM at frequencies of thousands of kilohertz or units of megahertz, still with enough resolution to provide a high dynamic range of the PWM output for the converter control.

The HRTIM peripheral also offers a very high degree of connectivity with other on-chip peripherals such as analog-digital converters, digital-analog converters, generating DMA requests, on-chip comparators, etc. This interconnection allows, in collaboration with sophisticated HRTIM output management system, implementation of several kinds of software independent protection mechanisms. The HRTIM also offers interconnection with external peripherals or can react on external events for instance from external comparators.

The HRTIM consists of six 16-bit timing units, one Master timer, and five Slave timers. The slave timing units can be synchronized with the master timing unit using internal signals and events. Each slave timing unit features two outputs that can be configured to operate independently, being driven by different events, or they can act as one output providing complementary signals. The outputs can be controlled by several events from the timing unit that the outputs belong to, from other timing units or even by events from external sources. The output crossbar unit provides all the mentioned output functionalities. Each output can be configured to be driven by one or more events from different sources into its active or inactive state. The polarity configuration allows defining the logic levels of the active and inactive state of the timing unit output [17].

The timing unit also allows generating of two complementary output signals with hardware implemented deadtime. In such case, the output waveforms are generated from a waveform defined for the first output channel [17]. The deadtime generator uses the timer clock prescaled by a configurable prescaler fed into the 9-bit deadtime counter. The deadtime generator allows configuring the deadtime duration from a fraction of nanosecond up to tens of microseconds.

5.1.2 Control signal generation

Each timing unit consists of a pseudo-prescaler that can be configured to multiply or to divide the high-resolution timer clock f_{HTIM}. The clock from the prescaler is then fed to the 16-bit counter. The counter can be configured to count in several different ways and can be triggered either by software or by an event from internal or an external source [18]. The maximum value of the counter is configurable, allowing in conjunction with configurable prescaler, generating signals with arbitrary frequency.

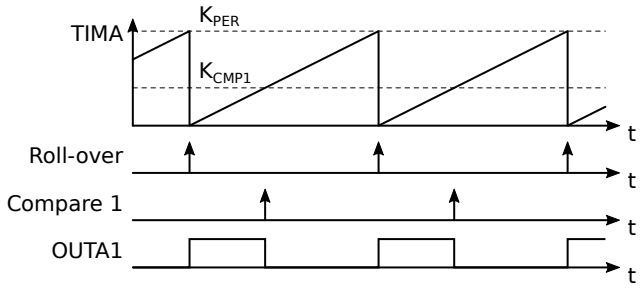


Figure 49 Principle of PWM generation using a high-resolution timer timing unit

The timing unit contains a set of four compare units, and in the case of slave timers, two capture units are available. The capture unit serves for transferring the actual value of the counter to its capture register when a particular event occurs. The event to be captured can be configured as well as the behavior of the timer in case the capture event occurs. This feature allows, for example, measurement of a time delay between two external events.

The compare unit is a digital comparator that compares a value held in its compare register against an immediate state of the counter. The compare unit can be configured to send a signal when the counter value matches the compare value. This signal can be handled in various ways. For instance, the compare event can be used to trigger other timing units or conversion on the analog-digital converter or to generate an interrupt request and many others. It can also be used by the output crossbar unit to change a state of an output pin, which is the case of generating a PWM with a fixed frequency.

Fig. 49 shows the principle of generating the PWM using a high-resolution timer. The K_{CMP1} denotes the value of the compare one register and the K_{PER} denotes the maximum value of the counter. The Roll-over event is generated by the counter when it reaches the maximum value and resets to zero. The compare one event is sent by the compare one unit as described before. The $OUTA1$ denotes the output one of the timing unit A — it is the signal produced by the output crossbar unit. It stands for the signal duty cycle

$$\delta = \frac{K_{PER(A)}}{K_{CMP1(A)}}, \tag{5.1}$$

where $K_{PER(A)}$ is a period register value of timer A and $K_{CMP1(A)}$ is a value of compare register one used to generate a compare event. Any of the compare units of the timing unit can be used to produce a compare event. However, a compare one was chosen for this particular case.

The clock frequency of the timing unit $f_{CLK(A)}$ is derived from the internal prescaler driven by the high-resolution timer clock f_{HTIM}. The clock frequency $f_{CLK(A)}$ is given by [17]

$$f_{CLK(A)} = 2^5 \frac{f_{HTIM}}{2^{K_{PCK(A)}}}, \tag{5.2}$$

where $K_{PCK(A)} \in \langle 0, 7 \rangle \subset \mathbb{W}$ is a prescaler exponent of the timing unit A. The constant 2^5 is the ratio of the pseudo multiplier used by the high-resolution timer to produce the clock frequency higher than the system clock or clock from the PLL. The

frequency of the output signal is given by [17]

$$f_{PWM} = \frac{f_{CLK(A)}}{K_{PER(A)} + 1} = 2^5 \frac{f_{HTIM}}{2^{K_{PCK(A)}} \left(K_{PER(A)} + 1 \right)}, \tag{5.3}$$

5.1.3 Frequency configuration of the control signal

The control unit firmware allows for the configurable switching frequency of the converter. The frequency is configured before the timer activation when the converter is not operating. The firmware computes the values of prescaler ratio $K_{PCK(A)}$ and the period value $K_{PER(A)}$ based on preset frequency. It is desirable to get the maximum possible value of $K_{PCK(A)}$, to optimize the dynamic range of the output signal. The prescaler ratio is then evaluated first using

$$2^{\tilde{K}_{PCK(A)}} = \left\lfloor 2^5 \frac{f_{HTIM}}{f_P \max\left(K_{PER(A)} \right)} \right\rfloor, \tag{5.4}$$

where $\max\left(K_{PER(A)} \right) = 2^{16} - 1$ is the maximum value of the period register. Taking the floor value of the result comes from the fact, that the prescaling value is an integer number. The prescaler exponent can be obtained by

$$\tilde{K}_{PCK(A)} = \max\left(\left\lceil \log_2 2^{\tilde{K}_{PCK(A)}} \right\rceil, 0 \right) = \max\left(\left\lceil log_2 \left\lfloor 2^5 \frac{f_{HTIM}}{f_P \left(2^{16} - 1 \right)} \right\rfloor \right\rceil, 0 \right). \tag{5.5}$$

It is mandatory to ceil the result of the logarithm since the value $K_{PCK(A)}$ is an integer and we are interested in the closest higher value of the prescaler exponent. The equation (5.5) means that only the positive values of the prescaling factor are taken since the logarithm can be even negative when the prescaler is between one and zero.

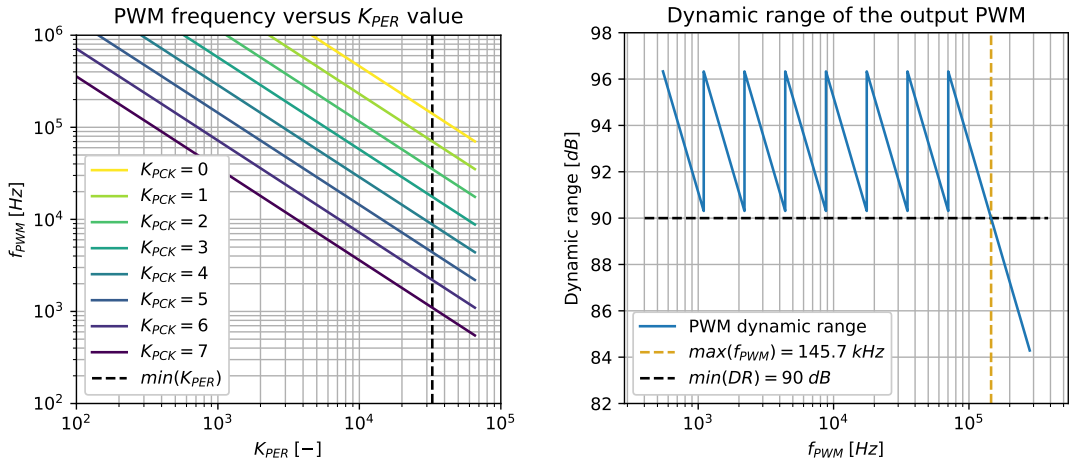
After the closest higher prescaler exponent, needed to cover the preset frequency, is chosen, the value of the period register can be computed using

$$\tilde{K}_{PER(A)} = 2^5 \frac{f_{HTIM}}{2^{\tilde{K}_{PCK(A)}} f_{PWM}} - 1. \tag{5.6}$$

The master timer is configured with the same prescaler and period value as the timer A, hence $K_{PER(M)} = K_{PER(A)}$, $K_{PCK(M)} = K_{PCK(A)}$. The timer B is set to generate the time base with n_S times shorter period, as it is used for generating a trigger event for sampling inductor current. Thus, the value of the period register of timer B is given by

$$K_{PER(B)} = \frac{K_{PER(A)}}{n_S}, \tag{5.7}$$

where $n_S = 8$. This algorithm will always result in the lowest possible prescaler ratio for the given output signal frequency. Therefore the highest possible value of $K_{PER(A)}$ or else $K_{PER(M)}$ is selected. This procedure gives the maximum of the dynamic range for the PWM signal generation, which is essential for the closed loop operation. Implementation of this algorithm is simple, when using properties of the integer numbers and replacing the powers with binary shifting, although the mathematical formula looks complicated.



a) Output signal frequency at different values of prescaller exponent

b) Output signal dynamic range among various frequency settings

Figure 50 Output signal frequency and dynamic range dependency on timer settings

The coverage of the output signal frequency for different prescaler exponents is shown in Fig. 50a. The dashed line shows the minimum value for the period register $\min K_{PER(A)}$ at which a new prescaling factor can be chosen, if possible. The value of the period register also represents the maximum number of steps in which the duty cycle can be preset. It can be written for the dynamic range of the PWM signal

$$DR = 20 \log \frac{\delta_{MAX} - \delta_{MIN}}{\Delta\delta} \approx 20 \log K_{PER(A)}, \tag{5.8}$$

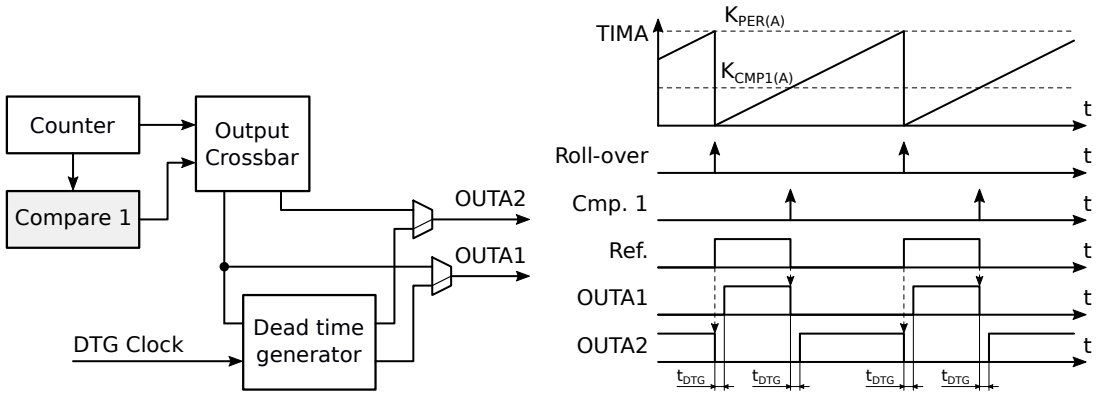
where δ_{MAX} and δ_{MIN} are maximum and minimum value respectively of the PWM duty cycle and the $\Delta\delta$ denotes the smallest change of the duty cycle. For the algorithm described above, the maximum dynamic range is always achieved as per the algorithm described above always finds the values of period register within the range $\min K_{PER(A)} \leq \tilde{K}_{PER(A)} \leq \max K_{PER(A)}$. Fig. 50b shows the variation of the output signal dynamic range as subject to the preset frequency.

The maximum frequency can be estimated as shown by black and orange dashed lines, taking into account the minimum dynamic range for the output signal.

5.1.4 Dead time configuration of the control signal

The firmware of the control unit also provides the possibility of configurable deadtime. As described before, the deadtime is inserted to the output using a deadtime counter that is clocked from the high-resolution timer clock source f_{HTIM}. If the hardware deadtime generation is enabled, the output signal is derived from the waveform defined for the first output of the timing unit. As a result, the complementary signals are generated only by configuring the waveform for the first output, which is done by writing only one value to a compare register.

The block diagram of the dead time generation is shown in Fig. 51a. This schematic reflects the actual configuration used in case of the control unit firmware. It can be seen that the output signals are provided by the dead time generator, not by the output cross bar unit. The dead time generator is driven by a clock signal derived from the high-resolution timer clock. Fig. 51b shows the waveforms of the dead time generation.



a) Schematic diagram of the deadtime generation

b) Example of the waveforms when deadtime generation is used

Figure 51 Hardware dead-time generation

The length of the deadtime is given by [17]

$$t_{DT(x)} = 2^{K_{PDT(x)}} \frac{K_{DT(x)}}{2^3 f_{HTIM}} = \frac{K_{DT(x)}}{f_{DTG}}, \tag{5.9}$$

where f_{DTG} is the dead time generator clock frequency, $K_{PDT(x)}$ is the prescaler factor of the deadtime counter of an arbitrary timing unit x and $K_{DT(x)}$ is the maximum value of the deadtime counter. The configuration values of the deadtime generator can be evaluated using a similar procedure to the one mentioned in the previous section. It is worthwhile to select the lowest possible value of the prescaler to cover the required deadtime, hence obtaining the highest resolution for the deadtime duration. It yields for the desired deadtime prescaling factor $\tilde{K}_{PDT(x)}$

$$2^{\tilde{K}_{PDT(x)}} = \left\lfloor 2^3 t_{DT(x)} \frac{f_{HTIM}}{\max\left(K_{DT(x)}\right)} \right\rfloor, \tag{5.10}$$

where $\max\left(K_{DT(x)}\right) = 2^9 - 1$ is the maximum value of the deadtime counter. Using the same procedure as in case of the frequency configuration, we get for the prescaler ratio

$$\tilde{K}_{PDT(x)} = \max\left(\left\lceil \log_2 2^{\tilde{K}_{PDT(x)}} \right\rceil, 0\right) = \max\left(\left\lceil \log_2 \left\lfloor 2^3 t_{DT(x)} \frac{f_{HTIM}}{2^9 - 1} \right\rfloor \right\rceil, 0\right). \tag{5.11}$$

This algorithm gives the lowest possible value of the prescaler ratio. The desired deadtime counter $\tilde{K}_{DT(x)}$ value can be calculated as

$$\tilde{K}_{DT(x)} = 2^3 t_{DT(x)} \frac{f_{HTIM}}{2^{\tilde{K}_{PDT(x)}}}. \tag{5.12}$$

The algorithm is implemented the same way as described in the previous section.

5.2 Microcontroller peripheral configuration

For the open loop control of the converter, it would be sufficient to configure one of the timer slave units to generate a PWM on its outputs and set the timer outputs to

produce complementary signals with a built-in deadtime generator. However, for the closed-loop regulation of the output voltage, it is needed to measure at least the output voltage. Thus an interconnection between the timer and an internal ADC is a possible solution.

In the case of the implemented controller, the constant current regulation is needed with control of the cycle mean value of the inductor current. The signal from a current transducer is "oversampled" eight times during one switching period to get the approximation of the mean value of the inductor current. Afterward, the mean value from the acquired samples is computed and is used as the compensator input. The output voltage is monitored the same way.

This section gives a brief overview of the HRTIM configuration to provide the power converter control. It shows the interconnection with other on-chip peripherals to provide handling of as many events as possible at the hardware level without the need for software intervention.

5.2.1 ADC modes of operation

The STM32F334 series of microcontrollers is equipped with two AD converters. Both ADCs are configurable to operate independently or can be used for interleaved operation [26]. In that case, the ADC1 is the master converter, and the ADC2 is the slave. Both ADCs can be configured to scan up to 18 channels. However, some of the channels are shared between the ADCs, and some of the channels are not available on processor pins. This section focuses on the ADC configuration and its usage to provide measurements of quantities necessary for the converter control.

Each ADC is equipped with a regular channel sequencer and an independent injected channel sequencer. The regular channels conversions can be configured to operate continuously or be triggered by an external event. They share the same data register in which the result of conversion is stored. In that case, if there are more than one channels in the regular sequence, it is convenient to use the DMA for transferring the data into the memory. The injected channel sequencer can be configured to convert up to four channels. An asynchronous event can trigger the injected sequence of conversions. The injected conversions take precedence over the regular conversions. There can only be up to four injected conversions. Each injected conversion has its data holding register.

5.2.2 Input and output voltage sensing

The control unit is designed with some degree of versatility as per the synchronous buck converter can be used as a synchronous boost just by swapping the output port with the input and vice versa. For instance, it is worthwhile to allow for overvoltage protection on both, the output and the input port of the converter. Based on this feature, the input and the output voltage signals are connected to the processor pins to be available for both ADCs in the MCU. The block schematic diagram in Fig. 52 shows the interconnection of the voltage sense signals to the MCU.

As stated before, one of the input or output voltage signal can be connected to a microcontroller pin that maps to a noninverting input of an internal analog comparator COMP6. The selection, whether the input or the output voltage is connected to the microcontroller pin is made using a solder jumper. The inverting input of the comparator can be internally connected to a channel one of the digital-analog converter two. The output of the comparator is internally connected to the external event EEV3 signal of the high-resolution timer. This interconnection is done directly without any intermedi-

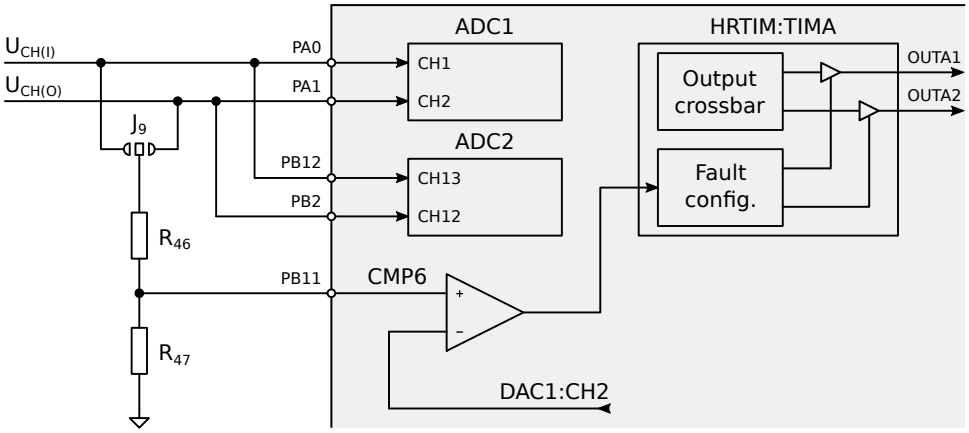


Figure 52 Block diagram of connection of voltage sensing signals to the MCU peripherals

ate stage to minimize the transport delays of the fault signal [17]. This configuration is used to provide overvoltage protection on an output or input port of the converter. The DAC1 defines the level when the protection is triggered and is configurable.

The ADC2 is used for lower rate conversions and for monitoring the internal voltage reference. The output and input signals are both also connected to the ADC2 inputs, so it is possible to make these conversions at lower rate except the current monitoring, which is connected only at the ADC1 input pin. This interconnection provides some degree of versatility in configuring the input and output voltage measurement. In actual configuration, the output voltage and inductor current are oversampled eight times during the switching period by the ADC1, while the input voltage is measured only once per switching period.

5.2.3 Current signal sensing and overcurrent protection

The ADC1 is used to measure the inductor current, output voltage, and possibly the input voltage. All mentioned signals are connected to the first three channels of the ADC1 that are capable of the fast conversions with sampling rate up to 5.1 Msps [18]. In the case of the current sensing, only the ADC1 is used. Fig. 53 shows the interconnection of the signals related to the current sensing to the microcontroller.

A differential amplifier amplifies the signal from the current transducer. This ampli-

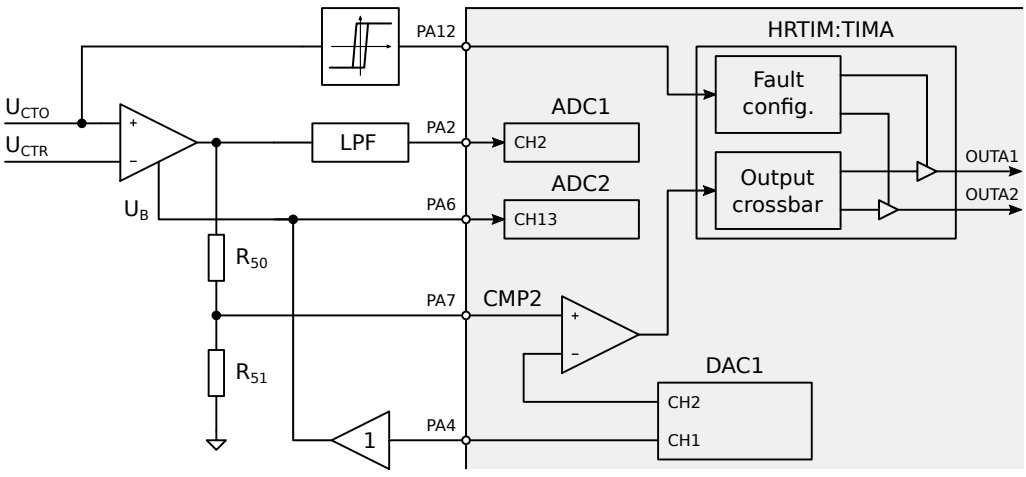


Figure 53 Block diagram of connection of current sensing signals to the MCU peripherals

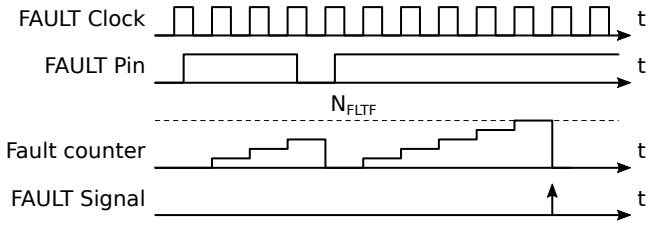


Figure 54 Filtering of the timer fault input signal [17]

fier is biased by voltage set by the internal DAC converter. The output of the DAC is buffered by a voltage follower, as mentioned in chapter 3. The bias voltage used to offset the differential amplifier back-sensed by the microcontroller. It is connected to a pin that can be mapped to a channel 13 of ADC2. The filtered and appropriately scaled signal from the current transducer is connected to the pin that allows mapping to channel 3 of ADC1. The output of the current sensor is also connected to a fast window comparator. The output of the window comparator connects to the MCU pin available for the high-resolution timer fault input. The fault input of the timer allows setting the control signal outputs to a predefined save state.

The output of the current transducer can be distorted by spikes injected in the measured signal due to high du/dt of the measured conductor. In such a case, the comparator can produce short signals during the switching transients that would always shut down the outputs of the high-resolution timer. This false triggering of overcurrent protection can be prevented by using an embedded digital filter of the high-resolution timer fault signal. The principle of the timer fault signal filtering is shown in Fig. 54.

The fault input signal is sampled at the rate of the fault clock f_{FLT}, which is derived from the high-resolution timer clock and can be divided by a configurable prescaler. The N_{FLTF} is the number of consecutive samples that need to report an active fault state before the fault signal is triggered. The length of the filter is configurable as well.

The output of the differential amplifier is also connected, after scaling down by a divider, to a pin that allows mapping to a noninverting input of an internal analog comparator. This interconnection enables implementing peak current control of the converter. The inverting input of the comparator can be mapped to an output of channel one of DAC2, providing a configurable reference for the peak-current control. The output of the comparator is connected to the HRTIM external event one, *EEV1*, signal.

5.3 Data acquisition with the use of the ADC

The quantities that are sampled at a faster rate, which is n_S times higher than the switching frequency are configured to be a part of a regular sequence on the ADC1. All the conversions take place sequentially after the same trigger event. The triggering event is the event from slave timer B of the HRTIM. The ADC2 measures the quantities that are sampled at the rate equal to the switching frequency. Since the ADC1 and ADC2 are configured to operate independently, all the conversions on both ADCs co-occur without interfering with each other. The internal voltage reference and the current measurement bias voltage are scanned using a sequence of injected conversions on the ADC2. Fig. 55 shows the block diagram of the interconnection of both ADCs and their respective trigger sources.

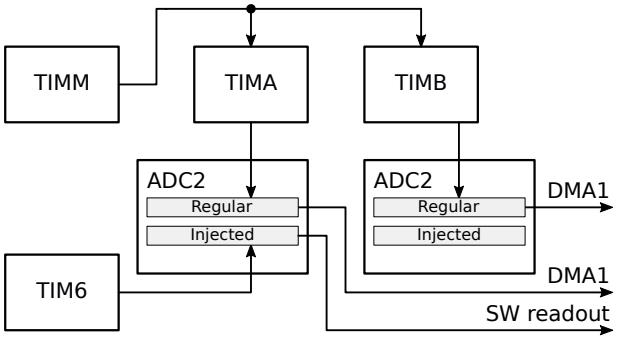


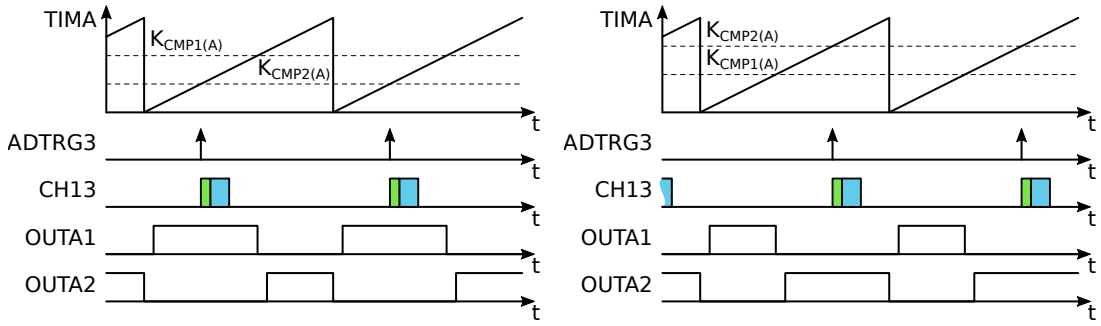
Figure 55 Block diagram of the trigger interconnection between ADCs

5.3.1 Generation of a trigger event for the ADC2

In case of the input voltage that is scanned at a lower rate, only once per switching period, the ADC2 is used. The ADC2 also measures the voltage of internal voltage reference to correct the measured voltages against ADC supply voltage variations. The internal voltage reference can be scanned with a minimum sampling time of 2.2 μs, hence monitoring the reference at a higher rate would ultimately impede other conversions on that ADC. This problem is overcome with the use of the injected conversion sequence on the ADC2. A regular sequence of conversions is used for measuring the quantities scanned at the same rate as the switching frequency.

The high-resolution timer TIMA compare two event triggers the regular conversions. The compare two event occurs when the value of the timer A counter matches the value of the compare two register $K_{CMP2(A)}$. The value of the $K_{CMP2(A)}$ is always set in the middle between the counter A roll-over and the compare one event, or vice versa, which time interval is longer. This setting is used to keep the quantities that are measured only once per period as far as possible from the switching transients. The principle of the sequence of regular conversions triggering is shown in Fig. 56.

On the other side, the injected sequence of conversions of the ADC2, which maintains the voltage reference and the current measurement bias voltage scanning, is triggered by a basic timer TIM6. This timer uses its trigger output TRGO signal that is internally connected to a multiplexer for the external triggers for the ADC2. The timer TIM6 is configured to operate independently to the high-resolution timer. It provides a time base with a period of $T_P = 50\ ms$, hence the trigger for the injected channels on the ADC2 occurs every 50 ms. Moreover, the injected sequence is configured to operate



a) Example of the waveforms when the $K_{CMP1(A)} < K_{PER(A)}/2$

b) Example of the waveforms when the $K_{CMP1(A)} < K_{PER(A)}/2$

Figure 56 Triggering of the sequence of regular conversions on ADC2

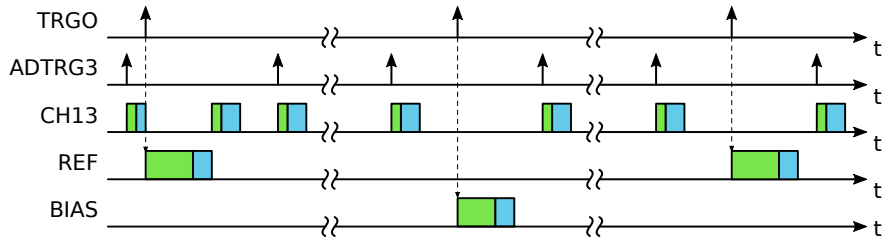


Figure 57 Example of triggering injected conversions on ADC2

in a discontinuous mode, so only one channel from the injected sequence is scanned per trigger. This approach makes the scanning period of the voltage reference and the current bias to be twice longer than the time base provided by the timer. Fig. 57 shows the triggering of the ADC2 in more detail.

Since the TIM6 is not in synchronicity with the high-resolution timer TIMA, the injected channels triggering happens asynchronously. If the injected conversion is triggered when a regular conversion is ongoing, the ADC postpones the regular conversion and starts to scan the injected channels that follow in the configured sequence. After the injected conversion is finished, the regular conversion is automatically retriggered.

5.3.2 Generation of a trigger event for the ADC1

The master timer unit is used to provide a common timebase. This unit is preset to count up and reset with a period equal to the converter switching period. For generating the output PWM signal, the TIMA slave unit is used. This timing unit is preset to count up and reset with the same period as the master timer. Starting both timing units at the same time instant makes them operate synchronously. Another slave timer is configured the same way as the master timer and timer A but with the value of the PER register eight times smaller than the master timer. This setting makes the timer B overflow and resets to zero eight times during one master period. It applies for the timer B period value

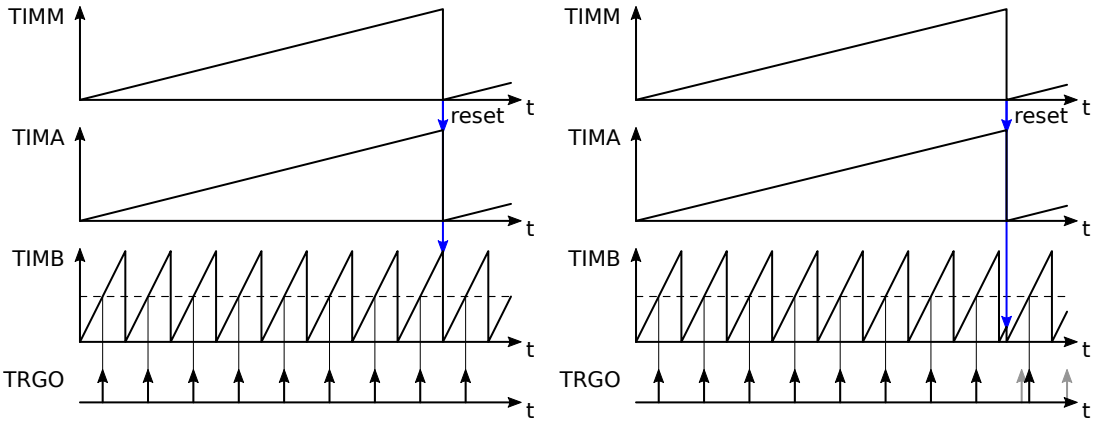
$$T_B = \frac{K_{PER(M)}}{f_{CLK(B)} n_S} \tag{5.13}$$

The value of the counter period register is a 16-bit integer. In case the master timer period is divisible by n_S, timer B is synchronous with the master timer, and the ADC triggers are generated synchronously as well. This situation is shown in Fig. 58a. If the value of the master timer period is not divisible by n_S, timer B will provide a time base that is not synchronous with the master timer. For keeping the timer B in synchronicity, the master timer is used to reset the timer B at the master timer roll-over event as per Fig. 58b. In this case, the first ADC trigger is delayed from the last trigger in the previous period by a time proportional to the division reminder.

The ADC triggers are generated using a compare event of the timer B. The value of the compare register of the timer B is always set to half of the period value to keep the trigger point as far from the beginning of the new period as possible. It applies for the compare one value

$$K_{CMP1(B)} = \frac{1}{2} K_{PER(B)}. \tag{5.14}$$

The actual value of the timer B compare one register is marked by the dashed line in Fig. 58.



a) Master timer period is divisible by oversampling factor

b) Master timer period is not divisible by oversampling factor

Figure 58 ADC trigger generation example

5.3.3 Transfering the data from ADC to the memory

The data from the ADCs are transferred into the memory using a Dirrect Memory Access — DMA. The DMA is a peripheral that allows for the data transfers within the microcontroller without the need for software intervention. The data can be transferred from an arbitrary peripheral to memory or vice versa. The DMA can also be used to transfer the data from one memory location into another. Use of the DMA for the data transfers helps to save software time of the CPU when performing time critical tasks. The DMA controller consists of several channels and an arbiter. The channels can be configured independently to transfer different amounts of data from various locations. However, one DMA peripheral can always serve only one channel at a time. The arbiter decides which channel is handled first when multiple channels are requesting for a data transfer, based on the channel priority. Each DMA channel has a configurable priority.

On the other hand, the DMA also has some limitations. For instance, the DMA cannot access some memory locations such as CCMRAM since this memory is not connected to the DMA bus in the bus matrix. In addition, when transferring from peripherals that are located at different clock domains, the access time can be longer as some wait states are inserted for the clock synchronization [36]. The inserted waitstates increase the latency between the transfer is triggered, and the time when the data are stored in the given location. This behavior has to be considered when using the DMA to transfer the data, especially when high data throughput is demanded.

In the case of the control unit, the DMA is used primarily for reading the data from ADCs. The data are transferred into the memory using a DMA1 channel one in case of the ADC1 and channel two in case of ADC2. The fast conversions that take place on the ADC1 are stored in one buffer of halfwords aligned to halfwords. The DMA sequentially stores the data for the inductor current channel and the output voltage channel. The DMA is configured to operate in circular mode, hence periodically refreshing the data in the memory buffer. Since the buffer length is equal to the number of samples per period, the refresh rate of the data is given by the switching period. After the DMA performs the last halfword transfer, it starts again from the first address and generates transfer complete interrupt. The data acquisition procedure is depicted in Fig. 59.

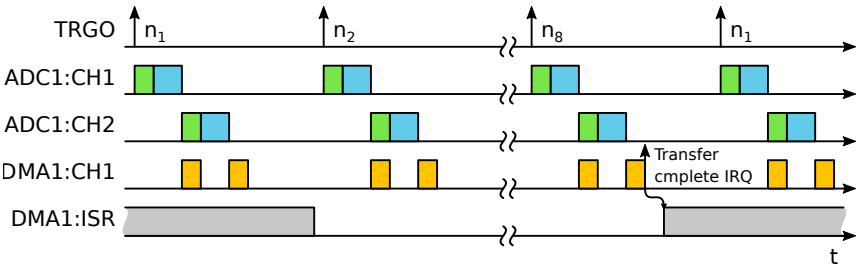


Figure 59 Principle of data acquisition on the fast ADC channels

5.3.4 DMA transfer timing and usage considerations

As described before, the ADC1 is used to acquire n_S samples per period of the output voltage and inductor current. Therefore the sampling time of the fast channels must be short enough not to exceed the "oversampling" period. It applies for the conversion time

$$T_{ADC} \leq \frac{1}{n_{CH} n_S \max\left(f_{PWM}\right)}, \tag{5.15}$$

where n_{CH} is the number of scanned fast channels. Since there are two fast channels sampled eight times during the switching period, and the maximum frequency of the output signal is defined to be 150 kHz, the maximum conversion time is less than 200 ns. The duration of the ADC conversion is given by the sampling time which can be configured and by a time needed for the SAR to convert the sampled value. It applies for the conversion time

$$T_{ADC} = T_{SMP} + T_{SAR}, \tag{5.16}$$

where T_{SAR} is equal to 12.5 clock cycles of the ADC in case of the 12-bit conversions [17]. The conversion time and the rate of the conversions limit the length of the sampling time of the ADC. Exceeding the maximum sampling time could cause the ADC to miss some triggers from the timer. As a result, less than n_S samples per period would be acquired. The DMA would interrupt the CPU after the n_S samples were transferred to the memory so the control algorithm would not be executed synchronously with the converter period.

Moreover, the timing of the data transfer from the ADC using the DMA becomes to be critical and analyzing the transfer timing is essential. One could object that there is enough time since the ADC holds the data from the conversion until the next conversion is finished. However, there are operating other channels of the same DMA peripheral that can be interrupted by the one with higher priority. This interference can add some more clock cycles to the overall data transfer latency. The DMA also shares the internal bus matrix with the CPU. In case the CPU attempts to access the same busses as demanded by the DMA, the core always takes precedence during the bus access arbitration [36, 17]. This interference can be reduced by special firmware design techniques such as placing the heap and stack to the SRAM [36].

The principles of the CPU access to the internal buses and the data transfer mechanisms that are managed by a bus matrix arbitration are considerably more complicated than described within the previous text and are far beyond the scope of this document. However, it is essential to take into account all the limitations of the DMA when using it for reading the data from ADC to prevent any ADC data overrun due to the inability of the DMA to read out the data in time.

5.4 Use of CCM RAM to execute time-critical algorithms

5.4.1 CCM RAM and system architecture brief overview

In a simplified view, the ARM Cortex-M4 core is interfaced with the rest of the microcontroller by several busses. These busses are part of a bus matrix that implements interconnection between the core busses and other microcontroller's peripheral. The primary busses of the Cortex-M4 core are a bus used for fetching instructions from memory, so-called I-Bus, and a bus for reading data which is also used for debugging, so-called D-Bus [3, 17, 23]. There is also a bus used for access to the microcontroller peripherals.

The STM32F334 family of microcontrollers is equipped with so-called Core Coupled Memory. It is a piece of random access memory that is accessible by both D-bus and I-bus [27]. Hence, it makes the CCM RAM available for storing the data and instructions of a program. Moreover, when accessing the CCM RAM, there are no wait states as it is, for example, in case of the Flash memory. The wait states are needed to provide some time to the Flash memory controller to access and read the data from memory [17]. However, the CCM RAM cannot be accessed by the DMA controller as the CCM RAM is not connected with the DMA bus.

Besides the CCM RAM, the STM32F334 contains a piece of static RAM that is interconnected either with D-Bus and I-Bus. The SRAM also connects to a DMA bus, which makes it accessible by the DMA controller for reading and writing a data into it. Given the data access and the program execution, the SRAM provides the same timings without wait states as in case of the CCM RAM.

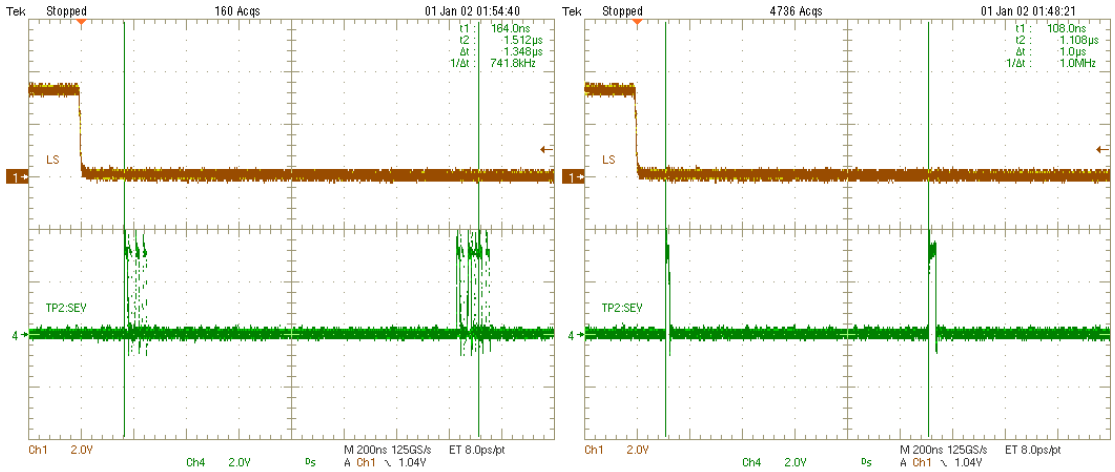
Storing the program code into the CCM RAM and a program data into SRAM allows the core to operate at the highest possible instruction rate [27]. This configuration can be used for executing time-critical algorithms and tasks. It is possible to store both the program and the data into the SRAM, but in this case, the core would be able to execute the code at a maximum rate, that is lower than in case of the previous configuration [27].

5.4.2 Placing interrupt routines into the CCM RAM

The above mentioned implies that it is worthwhile considering the usage of the CCM RAM for the controller algorithm. This configuration can speed up the compensator execution time by approximately twenty percent as proved by measurements. Also, placing the interrupt service routines helps to lower the delay between a time when an interrupt request is raised and a time when the core starts executing the code of the interrupt service routine. This configuration also lowers the jitter of both times.

If the code is executed from the Flash memory the time when the core starts running the code in interrupt service routine is primarily given by the Flash controller wait states inserted when fetching core is fetching the program instructions. In the case the CCM RAM is used for the ISR the time jitter is significantly smaller.

An example of the timing comparison can be seen in Fig. 60. The execution time of the controller algorithm was measured using a signalization event instruction — SEV. This instruction, when executed by the core, sends an event that is directly mapped to some GPIO ports. A GPIO pin that is configured in alternate function mode to reflect the signalization event is set to high logic level for exactly one clock cycle at the moment of the instruction execution. This method is the most accurate way of measuring the execution time of some program. The SEV signal can be seen on channel four labeled by *TP2:SEV*. Channel one marked by *LS* is the driving signal for the low-side switch.



a) Timing of the code execution from Flash memory

b) Timing of the code execution from the CCM RAM

Figure 60 Comparison of the execution time from the Flash memory and the CCM RAM

The SEV instruction was placed at the beginning of the ISR and the end of the ISR after the compensator code to measure the compensator algorithm execution time. Fig. 60a shows the length of the execution time when a program code was placed in Flash memory, and the data placement was left on compiler's decision. Fig. 60b presents the execution time measured when the code was executed from the CCM RAM, and the data were forced to be placed in SRAM. It can be seen that the execution time is considerably shorter without any time jitter.

It is important to note, that the measurement was done for the same algorithm placed between the SEV instructions and with the same compiler optimization level.

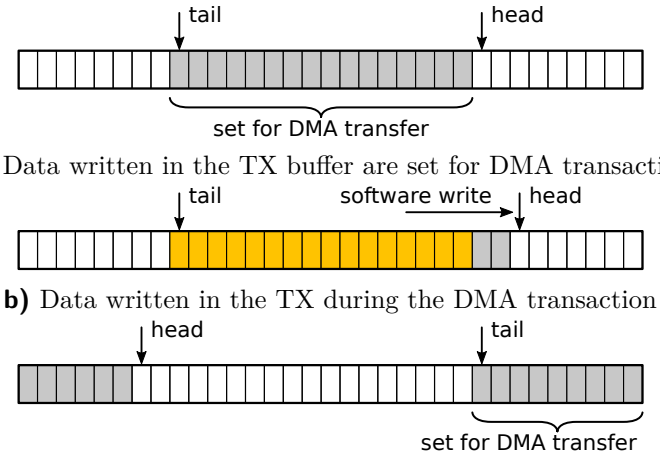
5.5 Communication with the host PC

As mentioned in chapter 3, an external USB to UART converter is used to provide a communication interface with the control unit. This solution comes from the fact that the used MCU does not include any USB peripheral. So the UART was chosen as a suitable solution since it is also more convenient to provide galvanic insulation of the full-duplex UART communication than isolating the USB. This section shows how the received and transmitted data are handled to decrease the communication overhead, and how the data are sent to the memory without wasting the CPU software time.

5.5.1 Handling of incoming and outgoing data over the UART

A built-in UART peripheral is used to serve the serial communication. The UART peripheral allows all the types of communication, both, the synchronous and asynchronous communication. It also provides simplex, half duplex, and full duplex communication. In the case of the control unit, the full-duplex asynchronous communication is used. The UART peripheral is capable of generating DMA transfer requests. Hence the data transfers into memory can be handled by the hardware, saving the CPU time.

Two circular buffers are used to handle the incoming and outgoing data. In case of the reception, the circular buffer is filled by the DMA transferring received data from the UART peripheral. The receive buffer is then read by software. In the case



a) Data written in the TX buffer are set for DMA transaction

b) Data written in the TX during the DMA transaction

c) The tail pointer is shifted after the DMA transaction is cmpleted

Figure 61 Procedure during the transmit buffer flushing

of the transmission, the data are written to the circular buffer by an application. The transmit buffer is then periodically flushed by the DMA transferring the data to the UART peripheral. For the receive and transmit buffer flushing, an internal timer TIM6 is used.

The timer is preset to generate a periodic interrupt event with period 50 ms. The transmit and the receive buffers are flushed every timer period. This procedure is done within the timer interrupt service routine. The circular buffers are defined by an allocated memory space and the head and tail pointers and a variable marking the region of memory that is being transferred by a DMA. The block diagram of the data transmission procedure is shown in Fig. 61.

If a data character is pushed to the circular buffer, the head pointer is shifted forward in the buffer address space. If the end of the buffer is reached, the head pointer is set at the beginning of the address space until the head pointer reaches the tail pointer. In such a case the buffer is full. If a timer interrupt event occurs, the transmit buffer is checked and if there are pending data, the part between the actual tail up to the head or end, whatever is closer, is set to be transmitted by UART using a DMA controller. This stage is shown in Fig. 61a. After this, a variable is set to inform the software that data in the mentioned region are being transmitted using the DMA, as shown in Fig. 61b.

After the DMA finishes the transmission, it generates a transfer complete interrupt request. In the service routine of the DMA interrupt, the region in the circular buffer marked by pending transmission is released, and a tail pointer is moved forward over the given area as depicted in Fig. 61c. It has to be taken into account that the state of the circular buffer may change during the data transmission and the head pointer will move forward. In this case, the new data are left in the buffer and are waiting for the next timer interrupt to be flushed. During the next interrupt, the latest data are set for the DMA transmission. This approach prevents any race conditions while handling the data.

Using the DMA to store the received data to the memory saves software time as there is no need for software-based data handling and no need for checking the UART peripheral status. The UART peripheral generates DMA requests for the following data, after successful transmission, on its own.

In case of the reception, the UART peripheral is configured to generate an interrupt

request. During the interrupt service routine, the data are copied from the UART and pushed to the receiver buffer by the application.

5.5.2 Processing of the messages from the host PC

The received data in the receive buffer are in the form of the string representing the particular command to the control unit. The string is read from the receiver buffer and saved into an operation buffer where is checked by a simple state machine. The state machine provides the interactive reading and returning of characters over the UART and behaves as a local echo. It allows of deleting characters from the operation buffer when a backspace key is pressed. If an end-of-line symbol is detected the received string is passed from the state machine to a text parser.

The text parser splits the input string by white spaces into tokens. The first token is then used to search in a table of commands supported by the control unit. If the command is found, the command method is given control over the parsed tokens. The particular command method is the lowest level of command string processing as it searches for the command arguments in the received symbols. The command arguments can be either characters or numeric. After extracting the values and all the options from the tokens, the command method executes functions of the control unit engine. All the command processing implements return value checking and inform the user about unallowed action or wrong parameters.

6 Regulation and controller design

The analytical model of the converter's dynamic behavior was described in chapter 4. Based on the derived model, a compensator design was performed. Also, the equations describing the converter dynamics were used to build a numeric simulation using Python programming language and its scientific libraries. The numeric simulations were used to test the converter behavior under different conditions. Both, the open loop and the closed loop dynamics were tested by simulation before implementing the compensator algorithm for the real power converter. This chapter aims to describe the controller used for the closed-loop regulation of the converter.

6.1 Converter control selection

Multiple approaches can be used for controlling the power converter. Two most basic methods of controlling the synchronous buck converter are presented in this section. One referenced method is implemented and used by the control unit, while the other one is not. However, the hardware configuration of the control unit allows the implementation of both methods.

6.1.1 Peak current control of the converter

The first method that can be used for the synchronous buck converter regulation is based on the peak current control often referred to as current programmed control [1, 2]. This control method is based on switching off the high-side switch when the inductor current rises to a predefined maximum value. The maximum value of the current can be derived by a dynamic compensator amplifying the difference between the sensed output voltage and a given reference. The block diagram of the peak current control scheme is depicted in Fig. 62.

The peak current control provides the cycle by cycle overcurrent protection that can be done simply by limiting the value of the peak current produced by the voltage regulator. Since the control input signal of the dynamic model of the converter is not directly the PWM signal duty cycle but the current peak value, the resulting model,

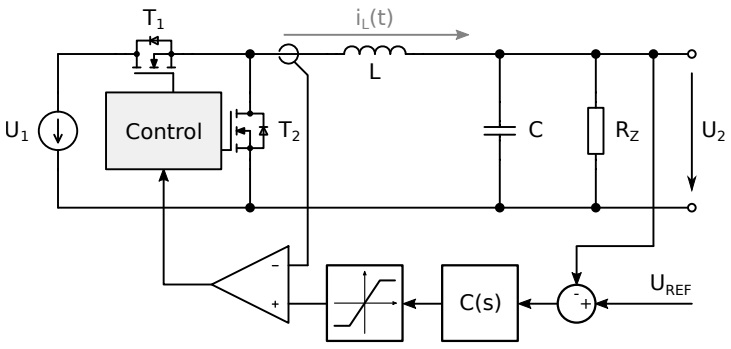


Figure 62 Schematic diagram of the peak control

lacks one pole that is caused by the inductor [1]. Thus the resulting transfer function of the converter is of the first order making the voltage compensator design more straightforward.

On the other hand, the peak current control suffers an instability for duty cycle in range $\delta \in \langle 0.5, 1 \rangle$ since any arbitrary change in the inductor current decays between two switching intervals with a factor [1]

$$\alpha = -\frac{\delta}{1-\delta}. \tag{6.1}$$

If the δ is higher then one half, then the value of α is higher than one. Hence the deviation in the inductor current will increase between two surrounding switching periods. This states results in instability of the current control loop causing the current oscillations. However, adding an auxiliary decreasing ramp signal to the sensed current overcomes this situation as described in [1]. The artificial ramp is reset every switching period of the converter. This kind of compensation is commonly referred to as slope compensation [1, 2].

The peak current control is not used in case of the designed control unit. Instead, the control unit uses regulation of cycle mean value of inductor current. However, the control unit design accounts with the possibility of the peak current control of the power converter. Hence the signal from the current transducer is available on an MCU pin that allows mapping to the internal analog comparator as described in the chapter 5.

6.1.2 Constant mean value of inductor current regulation

The other method that also fulfills the requirements of the converter control, and was used for the control unit design, is based on regulating the cycle mean value of the inductor current. In this case, the compensator is made up of two feedback loops. One control loop regulates for the constant cycle mean value of the inductor current. The second control loop is used for constant voltage regulation. The voltage controller amplifies the difference between sensed output voltage with a reference value and produces a reference value for the current control.

The principle is very similar to the control scheme described previously, The difference between this method and the peak current control is that the output action of the current controller is the duty cycle of the output PWM signal. The relationships derived in the previous chapter remains unchanged. However, in the case of the voltage regulation, the current control loop can be approximated by a low-pass filter. By considering the inductor current to be an input of the converter, the resulting transfer function lacks one pole present by the inductor current equation. This property is the same as in the case of the peak current control. The block diagram of the controller is

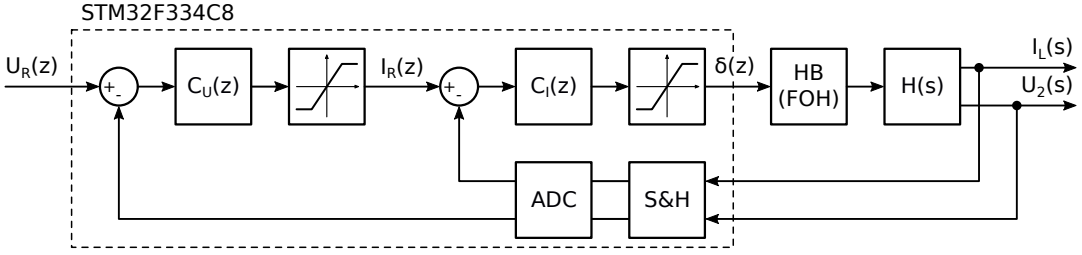


Figure 63 Block diagram of the power converter controller

shown in Fig. 63[1].

This approach allows for both, the constant current and constant voltage regulation. The output of the voltage controller is saturated to limit the mean value of the inductor current. This current limitation is useful in case of voltage reference step when the output capacitor bank is discharged. In such a case, the current could exceed the maximum value for which the transistor characteristic enters a saturation region. This condition could lead to power transistor damage.

The cycle mean value of the inductor current reflects the output current in steady state operation of the converter, $\langle i_L(t)\rangle_{T_S} \approx I_{OUT}$. In case a resistive load is connected on the output of the converter and the output voltage is set to a value that would cause exceeding the maximum mean value of the inductor current saturates the output action of the voltage controller. This condition causes the controller to enter the constant current mode with the current given by the saturation value.

6.2 PI compensator and its discrete time approximations

For both, the current control and the voltage control a PI compensator was chosen. Hence, a brief overview of the PI compensator and it's discrete time approximation is provided before proceeding to the implementation considerations.

Before proceeding with further description, I would like to mention that the compensator output is denoted by p instead of usually used u as the later would coincide with the symbol used for voltage.

6.2.1 Discrete time approximation of continuous compensator

The continuous time PI compensator is described by an equation of its output action

$$p(t) = K_P e(t) + \tilde{K}_I \int_0^t e(\tau)\, d\tau, \tag{6.2}$$

where $\tilde{K}_I$ is the integral constant, K_P is proportional constant and $e(t)$ is the difference between the desired value, often reffered as the reference, and the output value of a regulated quantity. The simplest way of the continuous-time system approximation is the used of backward difference approximation of derivative. The derivative is approximated as follows

$$\frac{dx(t)}{dt} \approx \frac{x(t) - x(t - T_S)}{T_S}. \tag{6.3}$$

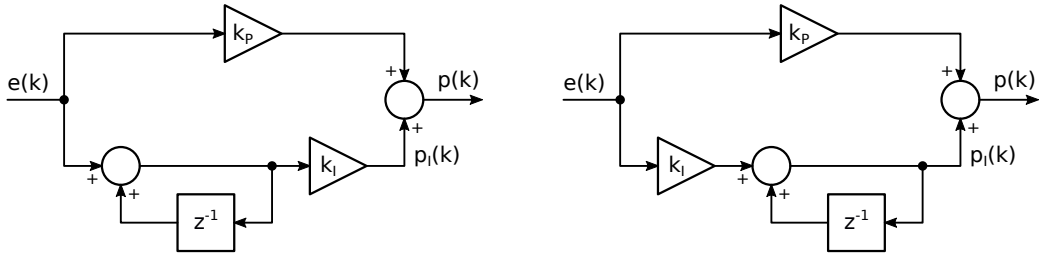
Applying Laplace transform on the left side term and Z transform on the right side term we get the relationship between the Laplace operator s and the Z-transform operator z.

$$s \approx \frac{1 - z^{-1}}{T_S}. \tag{6.4}$$

Now we can use this approximation for the Laplace image of the continuous time PI controller which is described by equation

$$P(s) = K_P E(s) + \tilde{K}_I \frac{E(s)}{sT_S}. \tag{6.5}$$

[1]The block *HB* denotes the half-bridge of the power converter that can be modeled as a Firs Order Hold transformation from the discrete time duty cycle into the continuous time.



a) variant A **b)** variant B

Figure 64 Block diagrams of two PS compensator variants

We obtain

$$P(z) = K_P E(z) + E(Z)\frac{\tilde{K}_I T_S}{1 - z^{-1}}. \tag{6.6}$$

Simplifying this equation and collecting terms $P(z)$ and $E(z)$ we get the equation

$$P(z)\left(1 - z^{-1}\right) = E(z)\left(K_P + T_S\tilde{K}_I - K_P z^{-1}\right). \tag{6.7}$$

Now we apply the inverse Z transform, and by solving for the actual output of the compensator, we get

$$p(k) = p(k-1) + \left(K_P + \tilde{K}_I T_S\right) e(k) - K_P e(k-1). \tag{6.8}$$

It is the output equation for the backward difference approximation of the continuous PI compensator. Using this form for the final algorithm is not effective as the terms multiplying the actual error can be computed in advance. By substitution, we get the equation of the compensator action response that can be implemented in the control unit firmware

$$p(k) = p(k-1) + A_0 e(k) - A_1 e(k-1). \tag{6.9}$$

where $A_0 = \left(K_P + \tilde{K}_I T_S\right) = K_I$ and $A_1 = K_P$.

Note that the integral constant $\tilde{K}_I$ differs from the K_I as the $\tilde{K}_I$ does not incorporate the length of the discrete time interval.

There is also a possibility to derive the PS compensator using a discrete time approximation based on bilinear transformation. This method comes from the approximation of the continuous time integral by trapezoidal integration. This method is often referred to as the Tustin method of discrete time approximation. However, more detailed description of the compensator algorithms and their variants is beyond the scope of this document.

6.2.2 Ordinary proportional-summation compensator

The discrete time approximation of the PI compensator based on the backward difference can be referred to as a Proportional Summation compensator — PS compensator. The PS compensator schematic is shown in figure Fig. 64.

The equation for the output of the PS compensator can be written in the form

$$p(k) = K_P e(k) + p_I(k), \tag{6.10}$$

where $p_I(k)$ is the contribution of the summation part of the compensator. In the case of variant A shown in Fig. 64a, it holds for the output action of the summation part

$$p_I(k) = K_I x(k), \tag{6.11}$$

where $x(k)$ is the value of the accumulator used for integrating the input error. It applies for the accumulator value

$$x(k) = e(k) + x(k-1). \tag{6.12}$$

Substituing the value of accumulator by $x(k) = p_I(k)/K_I$ yields the equation for the output action of the integral part expressed in terms of the $e(k)$ and $p_I(k)$

$$p_I(k) = K_I e(k) + p_I(k-1). \tag{6.13}$$

The compensator variant showed in Fig. 64b is equivalent to the previously described. The only difference is in applying the integral constant K_I. In this case, the accumulator of the compensator is directly the value of the integral contribution, hence $x(k) = p_I(k)$. The equation of the action response expressed in terms of $e(k)$ and $p_I(k)$ is in form

$$p_I(k) = K_I e(k) + p_I(k-1). \tag{6.14}$$

It is evident that both variants provide precisely the same output action. However, the difference is in the error accumulation for an integral part of the action response. The selection of the option depends on what kind of numbers and scales are used to realize the compensator numerically.

For instance, if the input error can be distributed over the full scale of number used to compute the compensator action response. If the constant K_I is smaller than one, it is better to multiply the error by the constant as the constant will scale the input error down and then accumulate. Hence, the variant B is more favorable as it preserves more of the range of the used number type for the accumulation. If the other variant would be used in this case, the integral part could overflow or better clip to the number range earlier. As a result, the compensator behavior could be distorted or saturated in fewer steps if a high error would appear on the compensator input.

In the opposite case, if the constant K_I is greater than one, and the input error is always significantly lower than the range of the used number, it is better to accumulate first and than multiply by the integration constant. Hence the variant A would be better. It is just an example of how the compensator structures unless they produce the same result, can behave differently under boundary conditions when they are implemented. This example is elementary since the discussion about the compensator implementation could be far more exhaustive and is beyond the scope of this document.

6.3 Implementation considerations of the controller

The controller block diagram was presented in section 6.1.2. This section aims to describe the implementation of the compensator.

The measured quantity comes to both compensators in the form of the output word provided by an analog to digital converter. The analog to digital converter provides

12-bit integer number representing the input voltage of the ADC. It applies for the output data word of an arbitrary channel x

$$D_{CH(x)} = \left(2^N - 1\right) \frac{U_{CH(X)}}{U_{DDA}}, \tag{6.15}$$

where $N = 12$ is the number of bits used by the analog to digital converter and U_{DDA} is the supply voltage of the analog to digital converter. The U_{DDA} is derived from the microcontroller power supply voltage U_{DD}. The ADC is equipped with an internal voltage reference that is measured at the manufacture of the MCU, and the calibration data are stored in non-volatile, read-only memory. The actual power supply voltage can be obtained by measuring the voltage across the internal voltage reference. It holds for the U_{DDA}

$$U_{DDA} = 3.3 \frac{D_{CAL}}{D_{REF}}, \tag{6.16}$$

where D_{CAL} is the calibration factor for the reference voltage and the D_{REF} is the data word returned by the ADC while scanning the voltage reference. The voltage on an arbitrary ADC channel x is then given by[2]

$$U_{CH(x)} = 3.3 \frac{D_{CAL} D_{CH(x)}}{D_{REF} \left(2^N - 1\right)}. \tag{6.17}$$

The inductor current, as well as the output voltage, are sampled at eight times higher rate than the switching frequency of the converter. A cycle mean value is evaluated from the acquired samples; however, the dimension of the output data provided to the compensator remains unchanged as it was a single raw data word supplied by the ADC.

As described in section 3.4, the signal conditioning paths are calibrated apriori, and the evaluated sensitivity and the offset of a static transfer function of the measurement channel are stored in the device. This way the controller can reproduce the original voltages or currents as they were before the signal conditioning blocks.

Both the constant current compensator and the constant voltage compensator uses the raw data from the ADC. Thus the reference value provided to the control unit in the same scale as the original quantities needs to be transformed into the ADC data word scale and transferred into the integer numbers. In the case of the output voltage, the reference value used by the compensator is given by

$$D_{CH(O)} = \frac{2^N - 1}{U_{DDA}} \left(S_O U_O + O_O\right). \tag{6.18}$$

The situation is a bit more complicated in case of the inductor current sensing. Concerning the section 3.4.1 describing the current measurement, it holds for the voltage at the ADC channel measuring the current

$$U_{CH(C)} = S_{C1} S_{C2} i_L + S_{C2} U_{CH(B)} + \tilde{O}_{C2}. \tag{6.19}$$

The data word representing a given value of inductor current is given by

$$D_{CH(C)} = \frac{2^N - 1}{U_{DDA}} \left(S_{C1} S_{C2} i_L + S_{C2} U_{CH(B)} + \tilde{O}_{C2}\right). \tag{6.20}$$

[2]The x is substituted by C for the channel measuring the inductor current or by O for channel measuring the output voltage.

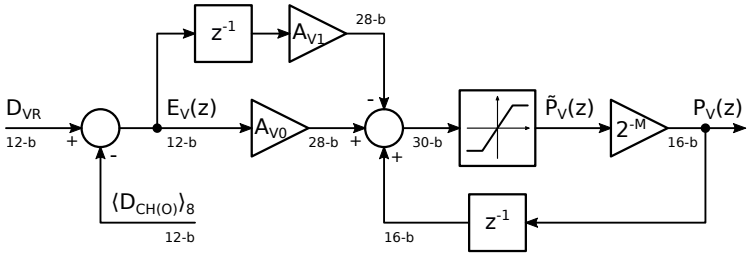


Figure 65 Block diagram of the PS compensator based voltage control

Using the data word returned by the ADC at channel used for scanning the bias voltage the above expression can be simplified to

$$D_{CH(C)} = \frac{2^N - 1}{U_{DDA}} \left(S_{C1} S_{C2} i_L + O_{C2}\right) + S_{C2} D_{CH(B)}. \tag{6.21}$$

The value $D_{CH(C)}$ is used by the voltage controller to saturate the output current. Since it is the integer number, the check of the limit and anti-windup protection is done efficiently in term of the execution time.

6.3.1 Voltage regulator algorithm structure

The voltage controller uses the PS compensator realized using backward difference approximation of the continuous PI compensator. The control algorithm is simple in its general form. The block diagram of the compensator implementation is shown in Fig. 65.

Since the compensator is implemented using integer numbers, it is essential to pay attention to the range of each operand to ensure the result will not overflow the range of used number.

The regulated quantity $\left\langle D_{CH(O)} \right\rangle_8$, which is in the form of the 12-bit unsigned integer representing the mean value from eight samples, is the same scale as the reference value. Hence the reference is the 12-bit unsigned integer. The computed error is then also at maximum 12-bit, but in this case, a signed integer as the error can be positive and negative. Other quantities in the compensator are stored as 32-bit signed integers, so the numbers can be in range $\langle -2^{31}, 2^{31} - 1 \rangle$. The small numbers under the lines mark the expected scales of each quantity in the compensator block diagram shown in Fig. 65.

As can be seen from the block diagram, the output of the voltage controller is scaled by a factor 2^{-L}. The resulting transfer function of the compensator can be expressed in the form

$$C_{VC}(z) = \frac{P_V(z)}{E_V(z)} = \frac{1}{2^M} \frac{A_{V0} - A_{V1} z^{-1}}{1 - z^{-1}} = \frac{\tilde{A}_{V0} - \tilde{A}_{V0} z^{-1}}{1 - z^{-1}}, \tag{6.22}$$

where $P_V(z)$ and $E_V(z)$ are the Z-transform images of the $p_V(k)$ and $e_V(k)$ respectively. The constants of the transfer numerator can absorb the factor 2^{-M} so it holds for $\tilde{A}_{V0} = 2^{-M} A_{V0}$ and for $\tilde{A}_{V0} = 2^{-M} A_{V1}$. This scaling makes the constants of the compensator transfer be in a fixed point number representation where the fractional part of the constant is represented by the lower M bits of the integer number.

This approach allows for the higher resolution of the compensator constants. Also, the scale down operation is done by using a binary shifting to the right by M bits. This operation is equivalent to dividing the output by 2^M, but takes only one CPU cycle instead of a division of the $\tilde{p}_V(k)$ by an arbitrary integer number.

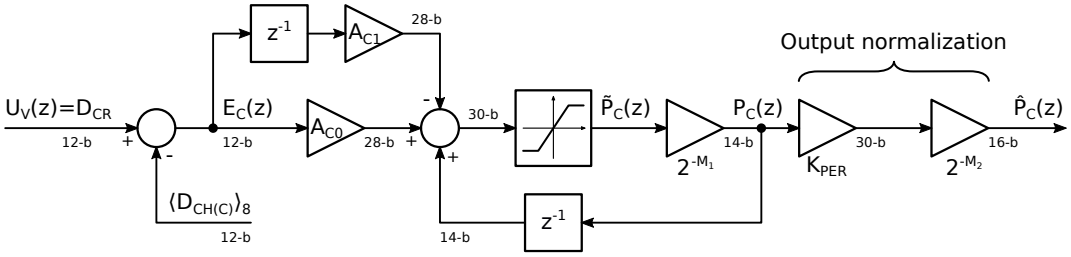


Figure 66 Block diagram of the PS compensator based current control

Anti-windup protection of the PS compensator

The saturation is inserted before the output action of the compensator is delayed one sample and fed back to the accumulator. This solution behaves as an effortless and fast anti-windup protection. The anti-windup makes the PS compensator behave correctly when the output of the regulator is saturated. In such a case the summation part of the compensator could keep accumulating the error signal $e_V(k)$ and would produce higher output action. Thus the summation part of the regulator would wind-up. If the regulated quantity would move closer to the reference or even the error would change its sign, the response of the compensator could be delayed since there would be enormous error accumulated during the output saturation.

6.3.2 Current regulator algorithm structure

The cycle mean value of the inductor current is regulated using a PS compensator. The compensator algorithm is the same as in the case of the voltage controller. However, some modifications were needed to provide the compensator robustness and make it behave the same at different conditions. Fig. 66 shows the block diagram of the exact realization of the current control algorithm.

The input of the compensator is the cycle mean value from the ADC raw data samples minus the reference value scaled to the 12-bit word, which is provided by the voltage controller. The output of the compensator $\tilde{p}(k)$ is scaled by a factor 2^{-M_1} to provide higher resolution for the compensator constants as described in the previous section. However, in the case of the current control, the action response of the regulator needs to be normalized since the output produced by the algorithm corresponds to the value of the compare one register of the high-resolution timer A used for generating the PWM. As stated in section 5.1.2, the duty cycle of the generated PWM is given by

$$\delta = \frac{K_{CMP1(A)}}{K_{PER(A)}}. \tag{6.23}$$

The model of the power converter presented in chapter 4 accounts for the duty cycle value in range $\delta \in (0, 1)$. Hence the transfer between the current controller output and the duty cycle coming into the converter is

$$\frac{\delta(k)}{p_C(k)} = \frac{1}{K_{PER(A)}}. \tag{6.24}$$

The resulting transfer of the current compensator can be expressed in the form

$$\frac{\delta(z)}{D_{CR}(z)} = \frac{\tilde{A}_{C0} - \tilde{A}_{C1} z^{-1}}{K_{PER(A)} \left(1 - z^{-1}\right)}, \tag{6.25}$$

The control unit allows for the configurable frequency of the PWM signal, so the value of timer A period register changes as a new value of frequency is selected. Due to this, the $K_{PER(A)}$ is variable as the frequency is variable. Hence, the output of the current controller is multiplied by the actual value of the period register of the timer to keep the compensator transfer to the PWM duty cycle constant across all the frequency configurations. The product of the compensator output and the period register value is then scaled by a factor 2^{-M_2} to preserve the original range of the compensator output action $p_C(k)$.

It holds for the output value coming to the timer compare unit

$$\hat{P}_C(z) = \frac{K_{PER(A)}}{2^{M_2}} P_C(z). \tag{6.26}$$

The overall transfer function of the current controller to the duty cycle of the PWM signal is given by

$$C_{CC}(z) = \frac{\delta(z)}{E_C(z)} = \frac{K_{PER(A)}}{2^{M_2}} \frac{\tilde{A}_{C0} - \tilde{A}_{C1} z^{-1}}{K_{PER(A)} \left(1 - z^{-1}\right)} = \frac{1}{2^{M_2}} \frac{\tilde{A}_{C0} - \tilde{A}_{C1} z^{-1}}{1 - z^{-1}}. \tag{6.27}$$

The value of $K_{PER(A)}$ cancels out, so the compensator transfer function to the duty cycle remains the same across all the timer A settings. However, the constant $\tilde{A}_{C0}$ is given by

$$\tilde{A}_{C0} = \frac{A_{C0}}{2^{M_1}} = \frac{k_P + T_S k_I}{2^{M_1}}, \tag{6.28}$$

where T_S is the switching period, which means that the contribution of the summation part varies with the PWM frequency as well, however, this is not an issue because the constants A_{C0} is evaluated every time the output frequency is changed. Since the PWM frequency cannot be changed during the control unit output is active, the term A_{C0} is always constant during the operation of the converter.

6.4 Closed loop control algorithm implementation

As soon as the interrupt request of the DMA transferring the data from the ADC into the memory is set, the microcontroller starts executing the interrupt service routine. In the service routine, a check is performed, whether the closed-loop operation is enabled or not. If the closed-loop operation is enabled, the execution of the control algorithm begins. As first, the control algorithm computes the cycle mean value of the current and possibly of the output voltage. This procedure is done in separate functions.

6.4.1 Evaluating the cycle mean value of acquired data

The mean value of an arbitrary set of samples $\mathbf{y} = \begin{pmatrix} y_1 & y_2 & \cdots & y_N \end{pmatrix}$ is given by

$$\langle \mathbf{y} \rangle_N = \frac{1}{N} \sum_{k=1}^{N} y_k. \tag{6.29}$$

This algorithm can be very easily implemented without any difficulty using simply a “for” cycle in the C programming language. However, the control loop algorithm is executed at the rate the same as the switching frequency of the converter. Since the minimum switching frequency is around 30 kHz and can go up to 150kHz, it is

Figure 67 Memory filling by the ADC raw data

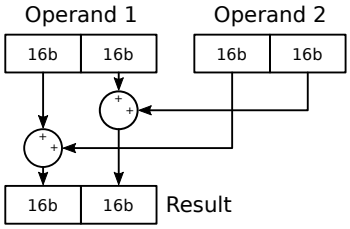


Figure 68 Block diagram of *UADD16* instruction operation [3]

mandatory to pay close attention to the control algorithm execution time. The control task has to be done before the next interrupt request of the DMA. This requirement limits the control algorithm execution time to the length of the converter switching period.

One possible solution is to make the control task execute every n-th period when the switching frequency increases. The control loop algorithm should always be run at a rate at least two times higher than is the dominant dynamics of the regulated system. In the case of the designed converter, the dominant behavior appears at frequencies below 10 kHz, hence running the control task at four or five times higher frequency is sufficient. For instance, if the converter operates with the switching frequency of 150 kHz, the control algorithm can be executed every third cycle.

This solution lowers the timing demands on the control algorithm execution. However, other tasks are executed on the same microcontroller as well, thus saving some time is of primary concern as it makes the application code and communication to the host PC responsive.

The data from the ADC1 that measures the output voltage and the inductor current are saved into memory by a DMA controller as described in the previous chapter. The data are stored sequentially as new samples from the ADC are read. The DMA transfers the data halfwords into a predefined buffer made up of an array of structures that contains two halfwords packed into a single word. Fig. 67 shows how the new data samples occupy a block of memory.

Every new data pair is aligned with a word. This data alignment allows using a DSP instruction *UADD16* that adds together corresponding halfwords of two words. This alignment enables to accumulate two values in a single operand within a single instruction. The operation of the *UADD16* instruction is depicted in Fig. 68. The only limitation is that the accumulated values must not exceed the range of the halfword. For instance, in case of the ADC configured in 12-bit resolution, the reminder to the halfword is four bits. Hence the maximum number of pairs of samples that can be accumulated this way is equal to $\max(n_S) = 2^4 = 16$. The evaluation of the cycle mean value of the acquired data point can be speeded up this way.

It is worthwhile computing the cycle mean value from several samples equal to a power of two. In such a case, the division by the number of samples can be replaced by a logical shift to the right operation. The logical shift instruction takes only one clock cycle compared to an integer division which can take up to twelve clock cycles [23]. The only overhead is added when the halfwords from the result have to be split into two words to perform the logical shifts. Listing 1 shows an example of the cycle mean

```
__CCMRAM ADC_DATA_T *cycle_mean(void)
{
  int i;
  uint32_t acc, *p_data = (uint32_t *) adc.raw_data;

  for (i = 0; i < OVERSAMPLING; i++) {
    acc = __UADD16(acc, *(p_data + i));
  }

  /* Expand the half words and store them to a memory */
  adc.raw_mean.output = ((uint16_t) (0x0000ffff & acc)) >> OVER_BITS;
  adc.raw_mean.current = ((uint16_t) (acc >> 16)) >> OVER_BITS;

  return (ADC_DATA_T *) &adc.raw_mean;
}
```

Listing 1 Implementation of cycle mean evaluation from acquired data

evaluation of the ADC raw data.

The `adc` is a structure that contains the input voltage, and cycle mean value of the output voltage and inductor current. The `adc` is a global variable so there are no arguments into the function so the function may be more easily inlinable.

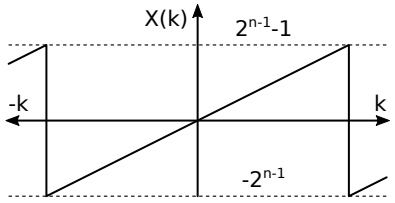
Since the cycle mean is evaluated only for the given type of the data set, it is also possible to write the *UADD16* instruction eight times in the code to get rid of a "for" cycle overhead. Anyway, when using the compilers optimization, it is highly probable that the compiler will use the repeating instruction several times instead of generating a cycle. The compiler may also optimize the cycle mean evaluation in the form of using the DSP instruction as mentioned, but it may not be guaranteed. This fact is the reason why knowing the DSP instructions and their explicit usage can become an advantage.

6.4.2 Compensator algorithm

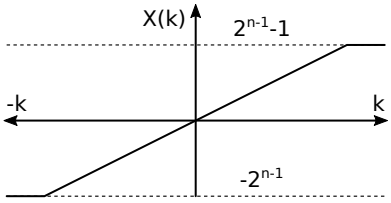
The algorithms of both, the current and the voltage compensator's are implemented according to the structures described in section 6.3. The PS compensator implementation in the C language is straightforward. The Listing 2 shows an example of the implementation of the constant voltage controller.

```
__CCMRAM static int32_t ps_action(PI_COMP_T *p_comp, int32_t y)
{
  int32_t e = p_comp->r - y;
  int32_t p;
  p = __QADD(p_comp->p_1, p_comp->a1 * e); /* Saturating addition */
  p = __QSUB(u, p_comp->a0 * p_comp->e_1); /* Saturating subtraction */

  if (p > p_comp->us_sc)
    p = p_comp->us << PI_DIV;
  if (p < p_comp->ls_sc)
    p = p_comp->ls << PI_DIV;

  /* Store the values for the next cycle */
  p_comp->p_1 = p;
  p_comp->e_1 = e;
  p >>= PI_DIV;

  return p;
}
```

Listing 2 Implementation of the PS compensator



a) Ordinary addition to the signed integer number of n bits



b) Saturated addition to the signed integer number of n bits

Figure 69 The difference between the ordinary addition and the saturated addition [3]

A structure `PI_COMP_T` contains the compensator constants of the compensator `a0` $\equiv A_{V0}$ and `a1` $\equiv A_{V1}$, and the values of the compensator output action and the input error from a previos controller step. It also contains the output upper and lower saturation levels `us_sc` and `ls_sc` respectively.

The numbers are added or subtracted from the accumulator using saturation arithmetic to prevent any misbehavior of the controller in case any number would from any reason exceed its expected range. For instance, the saturating addition of two integers adds their values together. But in a case the result would not fit into the 32-bit signed integer, it is clipped to the maximum value instead of overflowing and causing the result to appear opposite sign. The saturating subtraction works precisely the same way.

The difference between the signed addition or subtraction and the signed saturated addition or subtraction can be described as follows. Suppose the X is an n bit signed integer number which value is incremented by one for the positive k or decremented by one for the negative k. As can be seen in Fig. 69a the ordinary addition causes the number to overflow when reaching it's maximum values for $k = 2^{n-1}$ or underflows when reaching it's minimum value at $k = 2^{n-1} + 1$. This behavior could lead to an incorrect action response of the compensator. On the other hand, the saturating instruction clips the value of the number without causing overflow or underflow [22, 3] as can be seen in Fig. 69b.

The current compensator is implemented similarly. The only difference is the output normalization that is done to unify the output action of the current controller among different settings of the high-resolution timer.

6.5 Controller design verification by simulation

A simulation script in Python programming language was created based on the power converter model. Thanks to a variety of signal processing, math functions and algebraic libraries it is relatively simple to create complex models and solve them numerically and even symbolically. The Python programming language with all the scientific libraries was found as an applicable substitution of Matlab. Its main advantage is that it is free of charge. The only disadvantage is that more complex models need a bit of programming to make them work.

However, the Python was used as the basis for creating models and performing analysis of the power converter. Moreover, most of the plots and waveforms presented in this document were made in Python using a Matplotlib library. Matplotlib is a Python library that offers plenty of tools for plotting decent graphs that offers far more options for formatting and customization than plots in for example Microsoft Excel or Matlab. But as already mentioned, sometimes a more in-depth knowledge of the Python as the programming language is needed.

A Python class, including both, the averaged model and model that takes into account the converters switching behavior, was programmed to make the simulation of the synchronous buck converter. Hence, using this class, a simulation of the converters average response as well as the simulation taking into account the switching waveforms can be performed. Furthermore, automatic scripts were made for the analysis of the converter.

The simulation script allows for setting different kinds of the compensator and performing a simulation of the closed loop. The closed-loop behavior of the controller was simulated this way before the control algorithm was programmed into the control unit and tested on the real power converter. The simulation also allows for insertion of the signal conditioning block and their continuous transfer functions. Hence, the influence of the signal filtering on the closed loop stability can be tested. In case of the simulation that takes into account the waveforms during the converter switching also emulates the data acquisition from the evaluated waveforms of the inductor current and the output voltage as they were acquired and processed by the control unit itself.

The simulation is done by programming the converters model and using a library function for numerically solving ordinary differential equations. However, a more detailed description of the simulation script structure is beyond the scope of this document. Nevertheless, all the simulation scripts are attached on the CD.

6.5.1 Simulation of the current control

Block diagram of the current control of the power converter can be seen in Fig. 70. The transfer function of the inductor current measurement chain is denoted by the $G_{CS}(z)$ block. The gain G_{AD} is a transfer between the ADC input voltage and the corresponding data word which is equal to

$$G_{DA} = \frac{D_{CH(C)}}{U_{CH(C)}} = \frac{2^N - 1}{U_{DDA}}. \tag{6.30}$$

Since the transfer from the ADC input voltage to the ADC data word is only a scale, it is supposed to be frequency independent. However, this scaling has to be considered when deriving the closed loop transfer function from the reference as the reference value is in the same scale as the output data word of the ADC.

The current controller is characterized by its discrete time transfer function $C_{CC}(z)$. The averaged model of the converter can be seen as a continuous time, time-invariant dynamic system. However, the input of the converter is the duty cycle of the control signal. The value of the duty cycle is always fixed during one switching period. Hence, the value of the duty cycle is defined in discrete time.

The converter model was converted into its discrete time representation using the first-order hold method to perform the open-loop and closed-loop analysis. The open

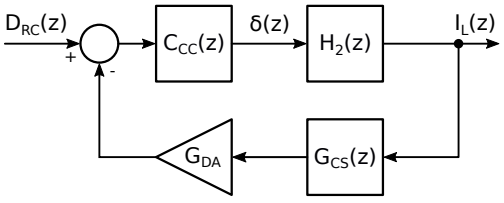


Figure 70 Block diagram of the current control feedback loop

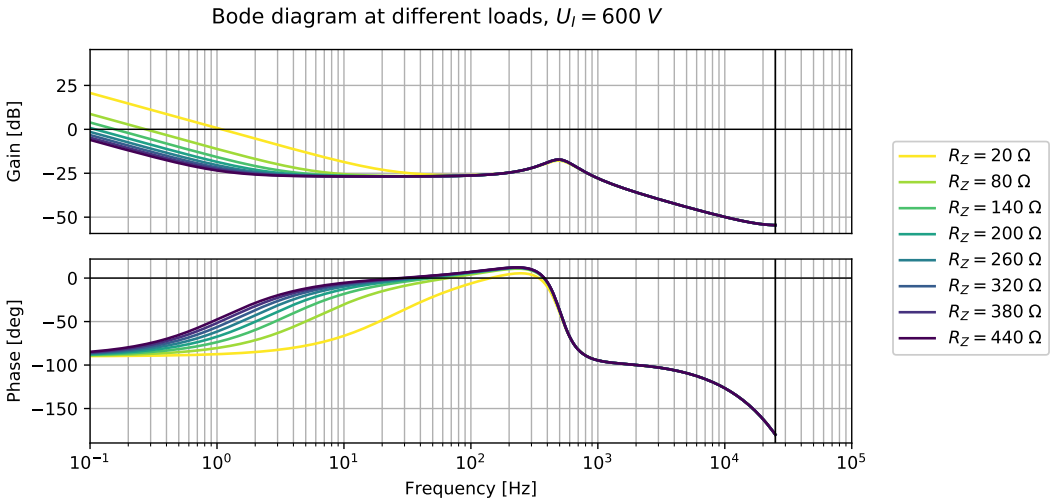


Figure 71 Bode diagram of the open-loop transfer of the current control

loop transfer function for the current controller is given by

$$L_{CC}(z) = C_{CC}(z)H_2(z), \tag{6.31}$$

where $H_2(z)$ is the discrete time approximation of the converter transfer function from the PWM duty cycle to the inductor current. The values of the compensator were found experimentally. A frequency characteristic of the open-loop connection under different output loads is shown in Fig. 71.

Note that the transfer is taken to the output quantity which is the Z-transform image of the inductor current $I_L(z)$. The measurement path influence is added to the feedback path, but in case of the controller design, the dynamics of the current measurement was neglected as the system dynamics is well below the cut-off frequencies of filters used for the current transducer signal conditioning. Moreover, the compensator was designed to provide stability of the control loop; the best performance was not the primary concern.

The closed-loop transfer function is given by

$$T_{CC}(z) = \frac{L_{CC}(z)}{1 + L_{CC}(z)C_{CS}(z)} = \frac{C_{CC}(z)H_2(z)}{1 + C_{CC}(z)H_2(z)G_{CS}(z)G_{DA}}, \tag{6.32}$$

where $G_{CS}(z)$ is the transfer of the current sensing path. At this point, it is considered to be only the DC gain of the current measurement chain as described above. The closed-loop was simulated using the model created in Python as mentioned at the beginning of this subsection. The simulated step response of the designed current control loop at different output loads is shown in Fig. 72.

It can be seen that the simulated step is from the value 0.5 A to 6 A. Note that the output voltage increase is not controlled since only the current controller was simulated.

6.5.2 Simulation of the voltage control

The output of the voltage controller is the desired value of the inductor current. Hence, the input of the power converter is considered to be the inductor current. The averaged state space equations derived in chapter 4 are as follows

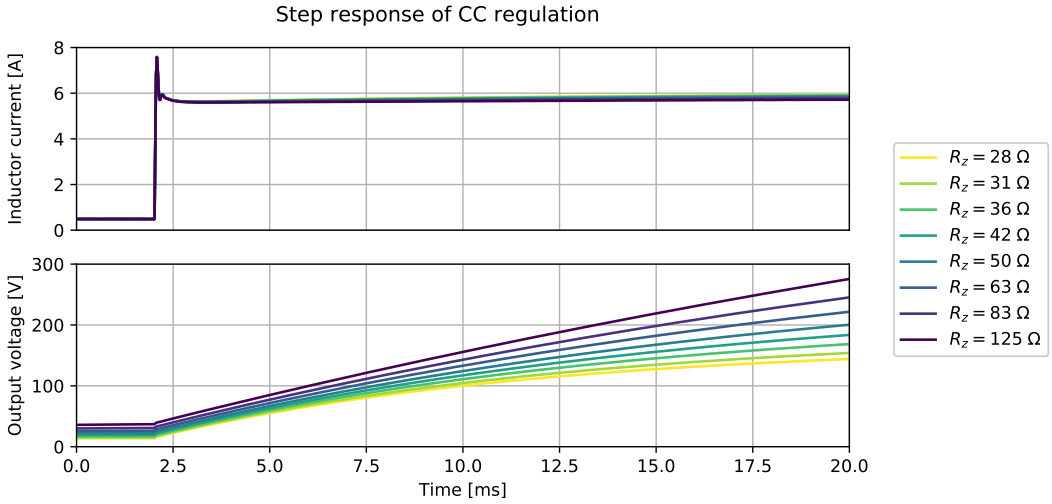


Figure 72 Simulated step response of the current control feedback loop

$$L\frac{d\left\langle i_L(t)\right\rangle_{T_S}}{dt} = \delta(t)\left\langle u_1(t)\right\rangle_{T_S} - (R_1 + R_{out})\left\langle i_L(t)\right\rangle_{T_S} - k_Z\left\langle u_C(t)\right\rangle_{T_S}, \tag{6.33}$$

$$C\frac{d\left\langle u_C(t)\right\rangle_{T_S}}{dt} = k_Z\left\langle i_L(t)\right\rangle_{T_S} - \frac{k_Z}{R_Z}\left\langle u_C(t)\right\rangle_{T_S}. \tag{6.34}$$

The output voltage equation is in form

$$\left\langle u_2(t)\right\rangle_{T_S} = R_{out}\left\langle i_L(t)\right\rangle_{T_S} + k_Z\left\langle u_C(t)\right\rangle_{T_S}. \tag{6.35}$$

By taking a closer look at the converter model, the duty cycle does not appear in the capacitor current equation. Hence there is no need for deriving the relationship between the duty cycle and the inductor current. If the inductor current is considered to be the input variable, the model can be simplified as follows

$$C\frac{d\left\langle u_C(t)\right\rangle_{T_S}}{dt} = k_Z\left\langle i_L(t)\right\rangle_{T_S} - \frac{k_Z}{R_Z}\left\langle u_C(t)\right\rangle_{T_S}. \tag{6.36}$$

The output voltage equation remains the same. Hence the linear state-space model is in the form

$$\frac{d\left\langle u_C(t)\right\rangle_{T_S}}{dt} = \begin{pmatrix} -\frac{k_Z}{CR_Z} \end{pmatrix}\left\langle u_C(t)\right\rangle_{T_S} + \begin{pmatrix} k_Z \end{pmatrix}\left\langle i_L(t)\right\rangle_{T_S}, \tag{6.37}$$

$$\left\langle u_2(t)\right\rangle_{T_S} = \begin{pmatrix} k_Z \end{pmatrix}\left\langle u_C(t)\right\rangle_{+}\begin{pmatrix} R_{out} \end{pmatrix}\left\langle i_L(t)\right\rangle_{T_S}, \tag{6.38}$$

where $R_{out} = R_C \parallel R_Z$ and $k_Z = R_Z/(R_Z + R_C)$. The resulting transfer function from the inductor current to the output voltage $H_3(s)$ is given by

$$H_3(s) = R_{out} + \frac{R_Z k_Z}{sC(R_C + R_Z) + 1}. \tag{6.39}$$

The converter model reduces to the first order system. However, the desired value of the inductor current, let's denote it $i_{LR}(t)$ is fed into the converter through the current control feedback loop. The current control loop can be viewed as a low-pass filter

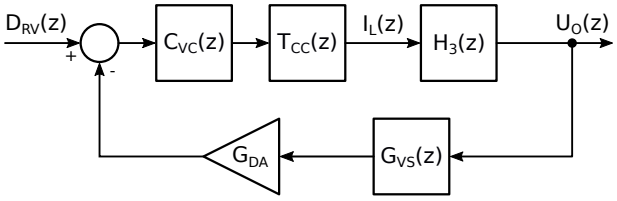


Figure 73 Block diagram of the voltage control feedback loop

inserted between the compensator output and the actual value of the inductor current. In such a case, the added block needs to be considered when designing and simulating the voltage control feedback loop.

The block diagram of the voltage control is shown in Fig. 73. Note that the output action of the voltage controller is not the same dimension as the inductor current, but is in the scale of integer numbers as presented in the previous sections.

The open-loop gain of the voltage control is given by

$$L_{VC}(z) = C_{VC}(z)T_{CC}(z)H_3(z), \tag{6.40}$$

where $H_3(z)$ is a discrete time approximation of the inductor to output voltage transfer function. The voltage control open-loop transfer function for an experimentally tuned compensator for different output loads is shown in Fig. 74.

The closed loop transfer of the voltage control feedback loop is given by

$$T_{VC}(z) = \frac{L_{VC}(z)}{1 + L_{VC}(z)C_{VS}(z)} = \frac{C_{VC}(z)T_{CC}(z)H_3(z)}{1 + C_{VC}(z)T_{CC}(z)H_3(z)C_{VS}(z)G_{DA}}, \tag{6.41}$$

where $C_{VS}(z)$ is discrete time approximation of the output voltage sensing path. As stated before, in case of the controller design the voltage sensing path is considered to be only a static transfer function. The response of the voltage control loop was simulated for various output loads using the software model of the converter. The reaction of the averaged model to a desired output voltage step from 50 V to 250 V is shown in Fig. 75.

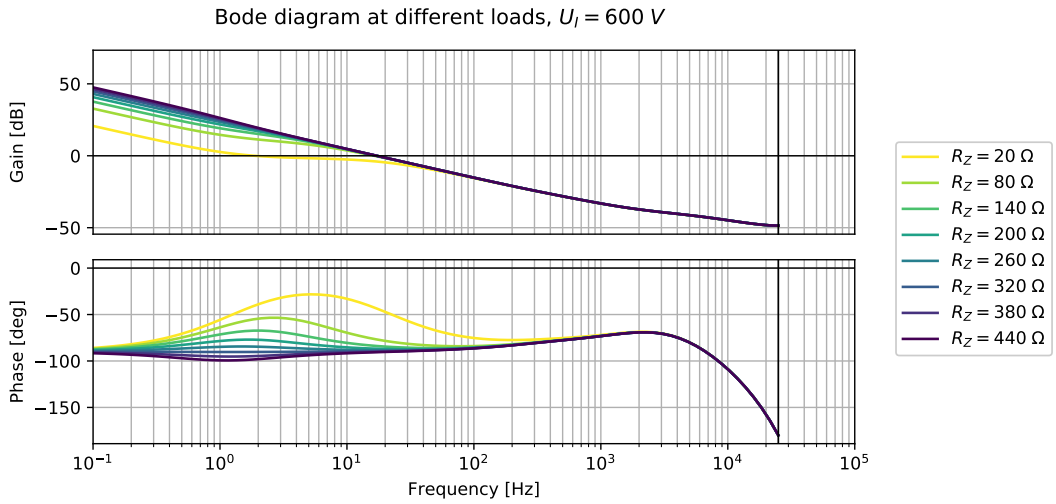


Figure 74 Bode plot of the open loop transfer of the voltage control

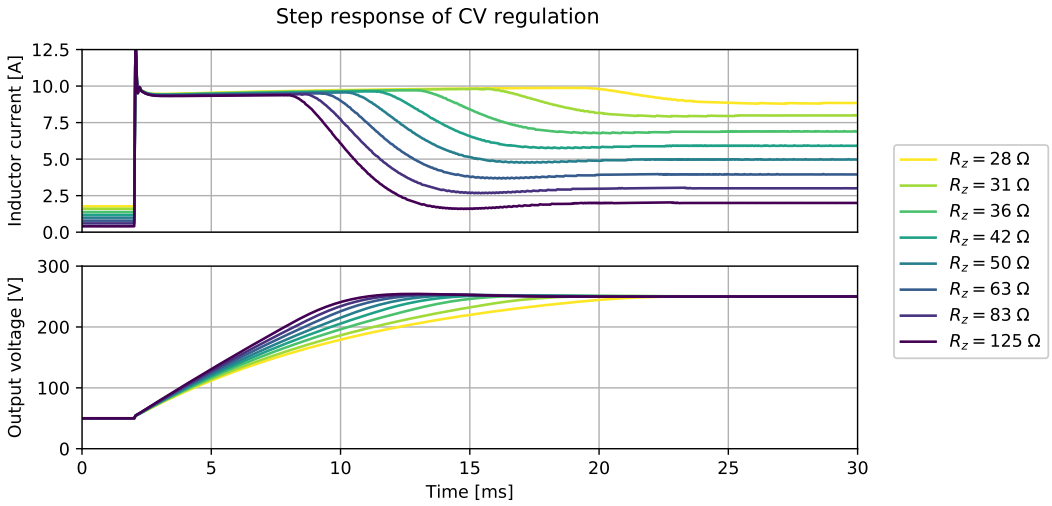


Figure 75 Simulated step response of the voltage control feedback loop

6.6 Testing the controller performance on the converter

Some tests were performed on the reference power converter to prove the controller performance and check the current control and voltage control stability. Since there is only a resistive load capable of the converter output power as described in chapter 2 the dynamic behavior of the converter unit was tested only for marginal conditions. The boundary conditions are the no-load operation and operation with the load resistance $R_Z = 28\ \Omega$ connected to the output of the power converter.

To compare the simulation of the closed-loop control and the behavior of the real converter response to the reference voltage step was observed. The waveforms of the output voltage and inductor current during the transients were acquired and are analyzed in the following sections.

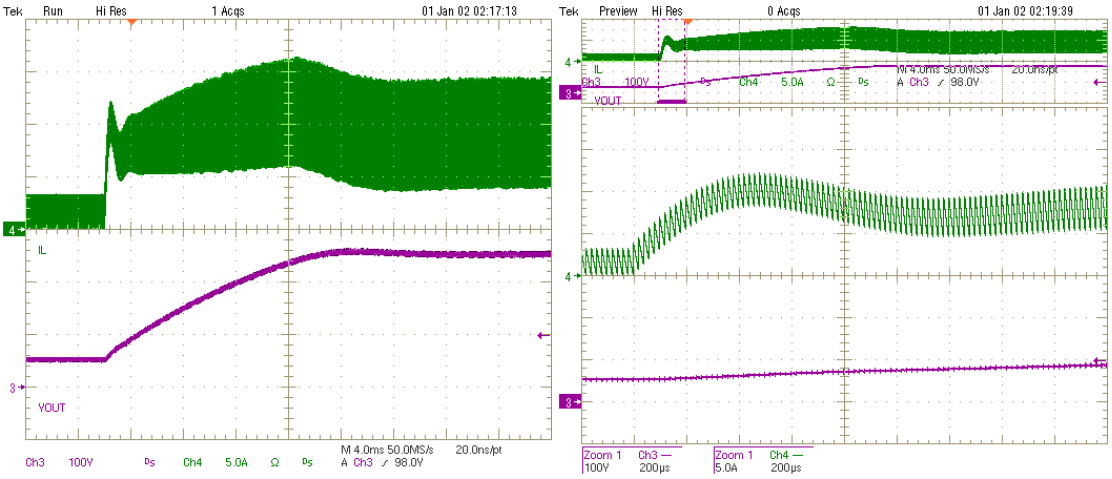
6.6.1 Increasing output voltage response

Before the step was initiated, the converter was switched into the closed loop mode. The maximum inductor current was set to a value that is higher than the output current given by the load resistance and the final output voltage. After the converter was settled at the output voltage $U_O = 50\ V$ a reference value was changed to $250\ V$. The response of the inductor current and the output voltage are shown in Fig. 76.

Fig. 76a shows the entire transient while Fig. 76b depicts the moment of the current settling when the voltage controller output was saturated due to a high error at the compensator input. Then, the controller operates in the constant current mode as the current is being limited by the saturation limit of the voltage compensator. As soon as the output voltage increases high enough, so the voltage regulator restores from the saturation, the inductor current decreases and is settling at the value given by the output voltage and the loading resistance.

The same step response was generated while the converter was operating without any load connected at the output. The waveforms acquired during the test are shown in Fig. 77.

The entire transient is shown in Fig. 77a. It can be seen that the duration of the constant current operation is much shorter compared to the previous case since only the output capacitor bank is being charged on the new output voltage. A detail of the



a) Entire transient of the step response

b) Detail of inductor current settling in constant current operation

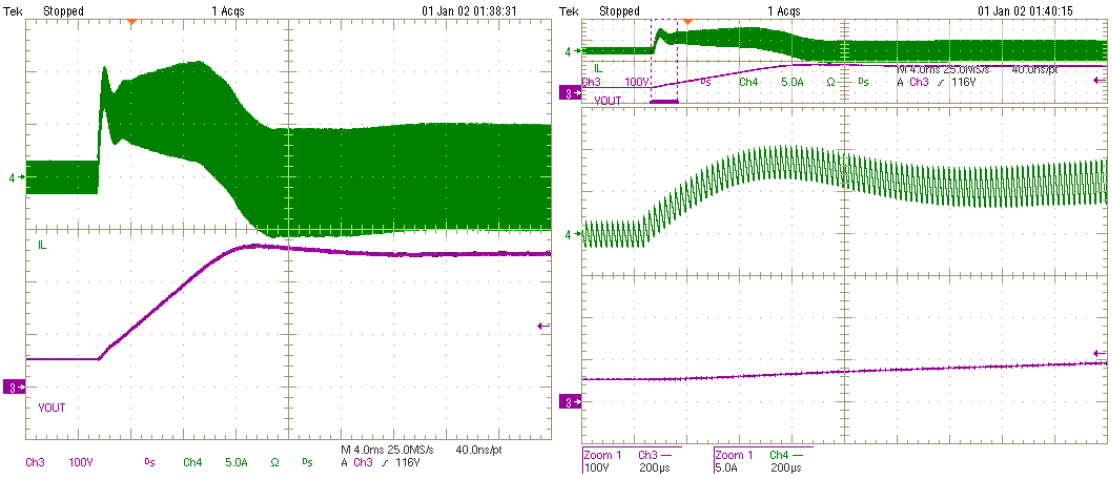
Figure 76 The converter's response to a reference voltage step from 50 V to 250 V with loaded output

current control settling is shown in Fig. 77b.

6.6.2 Decreasing desired output voltage

The output voltage settling is relatively fast in case of the step-up of the desired output voltage. It is mainly caused by the control unit current measurement range. As the control unit assumes the positive mean value of the output current in steady state, the majority of the current measurement range is reserved for positive inductor current. However, a small part of the current measurement is reserved even for negative inductor current as specified in chapter 3. Hence the output saturation of the voltage controller can be configured to allow current control to regulate the negative cycle mean value of the inductor current.

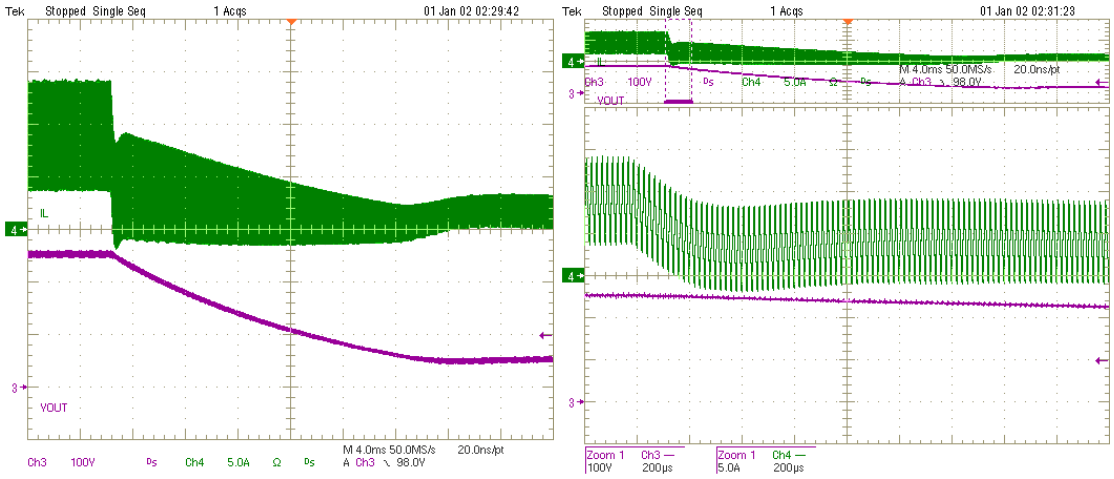
The negative current makes the response to a step-down of the desired voltage slightly



a) Entire transient of the step response

b) Detail of inductor current settling in constant current operation

Figure 77 The converter's response to a reference voltage step from 50 V to 250 V at no load



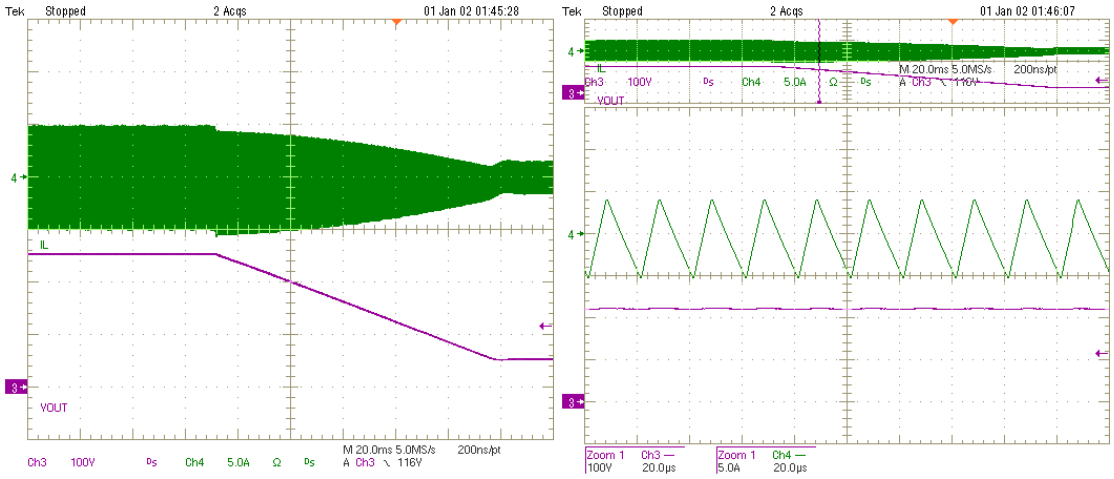
a) Entire transient of the step response **b)** Detail of current settling at the lower level

Figure 78 The converter's response to a reference voltage step from 250 V to 50 V with loaded output

faster since the negative current is actively discharging the output capacitor bank and it is more significant while the converter operates with no output load. However, attention has to be put on setting the lower saturation level of the current. If the inductor current is negative, the current is flowing from the output capacitor bank to the input, and the input capacitor bank is being charged. The energy drawn from the output has to be dissipated to prevent any significant increase of the input voltage, or used power supply has to be able to clamp its output voltage.

The minimum of the cycle mean value of the inductor current is then limited to only several tens of milliamperes below zero. The response of the converter to a step down of the reference voltage from 250 V to 50 V is shown in Fig. 78. The entire transient response is depicted in Fig. 78a. A detail of the current settling is shown in Fig. 78b. Thanks to the loaded output, the response is fast since the energy in output capacitors is being dissipated in the output load.

The response of the converter when no load is present at the output is presented



a) Entire transient of the step response **b)** Detail of the constant current operation

Figure 79 The converter's response to a reference voltage step from 250 V to 50 V at no load

in Fig. 79. The entire transient is shown in Fig. 79a. The duration of the transient is longer since the negative inductor current is limited. A detail of the inductor current is depicted in Fig. 79b. It can be seen that the cycle mean value is a few hundreds of milliamperes. This value was proved to be the maximum in case of used laboratory equipment.

7 Measuring the SiC MOSFET switching dynamics

As stated before, the purpose of the power converter is to provide a testing platform for testing and comparing SiC MOSFETs. Several tests and experiments were performed on the power converter so far. This chapter focuses on the analysis of the switching dynamics of the selected SiC MOSFETs.

7.1 Measuring of switching transients

Generally speaking, the measurement of any transient waveforms during switching of any SMPS sometimes requires the use of advanced techniques. Special care needs to be taken in selecting the measurement techniques as conditions can vary significantly with the use of different kinds of switching devices or using different topologies. With the increasing speed of the switching transients, it is essential to take into account the parasitic capacitances of probes, the limited bandwidth of test equipment and propagation delays introduced by probes, cabling or by signal conditioning circuits.

In the case of SiC MOSFETs, the switching transients can be much faster compared to IGBTs or Si MOSFETs. For example, the rise time or fall time of the drain-source voltage can reach values up to several tens of volts per nanosecond. Current commutation through the body diode of SiC MOSFET can reach several units of amperes per nanosecond. The converter design also influences the switching dynamics of the power transistors of any technology, for instance in case of the synchronous buck topology there is an influence of the critical loop as described more in detail in section 2.2.2.

Due to the fast switching transients of the SiC-based devices, it is challenging to measure any waveforms on the high-side switch. The parasitic capacitance of differential probes available in the laboratory is too high and common mode rejection is too low to withstand the high du/dt of the drain-source voltage of the low-side switch. This situation makes, for example, the gate-source voltage of the high-side switch practically unobservable, especially when reaching the performance limits of the switching devices. Due to this fact, all the tests and measurements made on the power converter reference design were performed on the low-side switch.

7.2 Measurement of the low-side MOSFET current

Since the critical-loop inductance is an essential parameter for the converter operation as described in section 2.2.2, it is not possible to interrupt the loop and insert any longer conductor for an external clamp-on current probe. Several tests have been performed to measure the low-side switch current using Rogowski coil. It was observed that the maximum current slope di/dt during the switching transient is high enough to exceed the maximum value of used Rogowski coil. Even more, the current commutation was fast enough to exceed the absolute maximum rating of the Rogowski coil transducer. It was decided to measure the current using a low inductance shunt resistor inserted

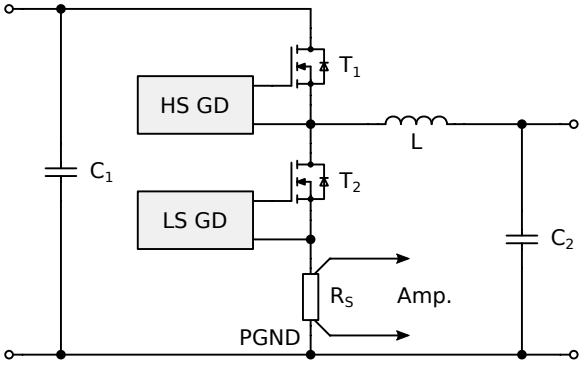


Figure 80 Schematic diagram of the current sense resistor placement

between the low-side switch source and the input foil capacitor. Fig. 80 shows the schematic diagram of the current sensing resistor placement.

It can be seen from the schematic diagram that the current sense resistor is a part of the critical loop of the power converter. Hence, special care was taken not to disrupt the power path too much as it could influence the behavior of the converter and impact the results of the current measurement. Also, the resistor is placed outside of the gate driver loop of the low-side transistor so the driving current is not observable and will not influence the measurement.

7.2.1 Current sense voltage amplifier

A simple circuit with an operational amplifier is added to sense the voltage on the shunt resistor. The amplifier provides impedance decoupling of the shunt resistor from the cabling and oscilloscope input. It also offers impedance matched output to drive a 50 Ω coaxial cable connected to the oscilloscope input switched into 50 Ω input impedance.

In the beginning, the amplifier of the current sense resistor voltage was realized as an inverting amplifier biased by a fixed voltage to overcome the need for symmetric power supply. The reason for that is the fact that the current can flow both directions through the sense resistor. The bias voltage was set to a value that caused the output voltage of the amplifier to be in the middle of the power supply voltage. An offset function of used oscilloscope was applied to compensate for the bias voltage of the amplifier. However, the first realization of such amplifier faced several issues, so a new one was created.

The new current sense circuit is realized using the same amplifier. The only difference is that the actual connection uses a split power supply, so there is no need for applying any bias to the output voltage of the amplifier. It also lacks issues associated with measurement of current waveforms of lover amplitudes since the oscilloscope offset function is limited when switching to lower vertical scales. The schematic diagram of the amplifier is shown in Fig. 81.

The output voltage of the amplifier is given by

$$u_2(t) \approx -\frac{R_3}{R_2} u_S(t), \tag{7.1}$$

where $u_S(t)$ is the voltage across the sense resistor. To make the output impedance of the amplifier to be approximately 50 Ω, a series resistor is added to the output. It holds for the overall output impedance of the amplifier

$$R_O = (R_{OA} + R_4) \parallel R_3, \tag{7.2}$$

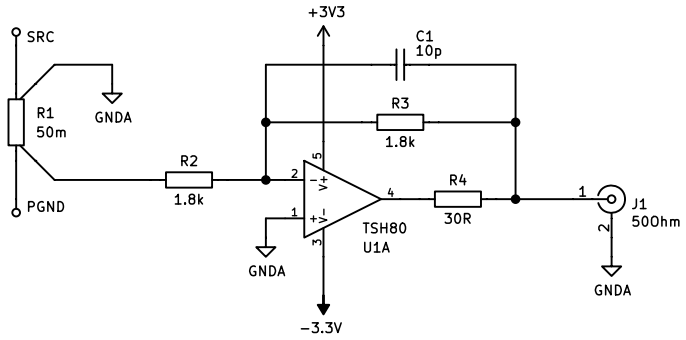


Figure 81 Schematic diagram of the current sensing circuit

where R_{OA} is the output impedance of the used operational amplifier. Since the R_{OA} is much smaller compared to the R_3 the output impedance is roughly given by the series connection of the operational amplifier output impedance R_{OA} and the added resistor R_4. If the feedback of the amplifier were taken directly from the operational amplifier output, the voltage measured by the oscilloscope would be given by the divider formed by the series resistor R_4 and the oscilloscope terminating impedance

$$u_{MSR}(t) = u_2(t)\frac{R_T}{R_T + R_4}, \tag{7.3}$$

where $R_T = 50\ \Omega$. The negative feedback of the amplifier is taken after the resistor R_4 in order to overcome this scaling. This simple trick makes the amplified signal to appear on the input of coaxial cable without any further scaling. The static gain of the amplifier is one, so the voltage measured by the oscilloscope is approximately the same as the voltage across the current sense resistor.

A video operational amplifier TSH80 was used for the realization. This amplifier prooved its characteristics and performed well in the measurement setup. The key parameters of the amplifier are summarized in Tab. 17.

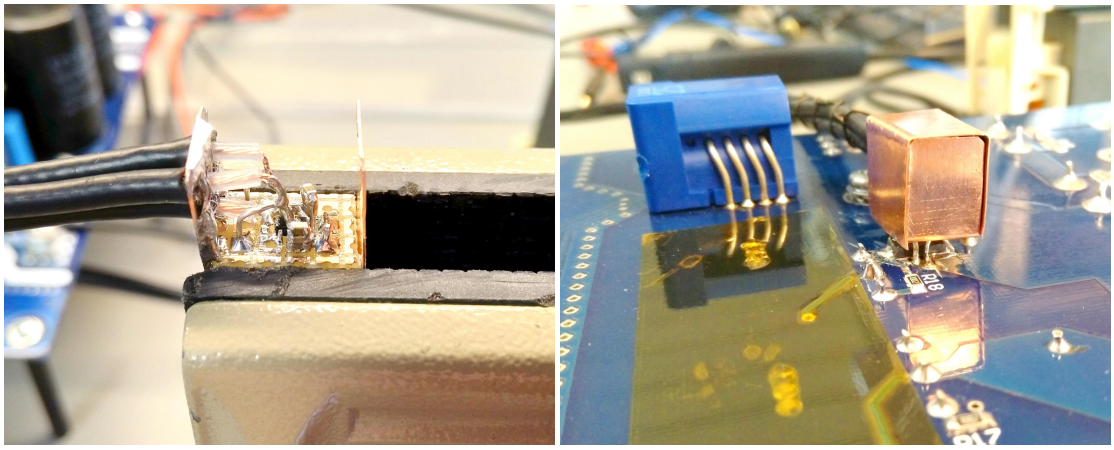
Parameter	Value
Bandwidth Product	87 MHz
Slew Rate	105 $V\,\mu s^{-1}$
Output impedance (approx.)[1]	20 Ω

Table 17 TSH80 video amplifier key parameters at supply voltage $U_{CC} = 5\ V$, data source: [31]

The whole circuit was made on a small piece of prototyping PCB using a single operational amplifier in a five-pin SOT23 package. The amplifier module is as tiny as possible and is placed on the top side of the current sense resistor that is in the bottom of the power stage board. The placement is optimized to minimize the signal path length.

Locating the current sense module close to the shunt resistor makes it close to the half-bridge middle point. It is thus exposed to high du/dt, and it can suffer a relatively high level of capacitive coupling from the half-bridge middle point. Due to this, the circuit was enclosed in a shielding box using a 0.5 mm thin copper plates connected to the ground to minimize the induced noise and provide shielding against the capacitive

[1] The output impedance was calculated using the load characteristic of the amplifier output provided in the datasheet, thus it is the DC resistance which may differ slightly from the high frequency impedance



a) Photo of the current sense amplifier circuit **b)** Photo of the enclosed module placed on the current sense resistor

Figure 82 Photos of the current sense module with operational amplifier

coupling. The module is powered from an external power supply using coaxial cables as can be seen in the photo of the opened module shown in Fig. 82a.

The enclosed amplifier circuit and its placement on the current sensing resistor are shown in photo in Fig. 82b.

7.2.2 Current sense resistor bandwidth

Measuring the current in the purpose of analyzing the switching transients, especially in case of SiC MOSFETs, using a low-cost current sensing resistor can be challenging. Since the current sensing resistor is a real component, its high-frequency behavior is greatly influenced by its parasitic inductance. Even the resistance value is in tens of milliohms, and the parasitic inductance is guaranteed by the manufacturer to be below five nanohenry, its impact is significant, especially when measuring high-speed transients.

The equivalent schematic of the current sense resistor is shown in Fig. 83. The equivalent circuit of the current sense resistor is made up of series connection of the resistive component R_S and the parasitic inductance L_S. The parasitic capacity C_P of the resistor is mainly caused by the geometry of the resistor soldering pads and their distance. However, the influence of the parallel capacity can be neglected since the value may not be higher than a few units of picofarads resulting in the resonant frequency of several units of gigahertz. The impedance of the current sensing resistor can be approximated by

$$Z_S(j\omega) = R_S + j\omega L_S. \tag{7.4}$$

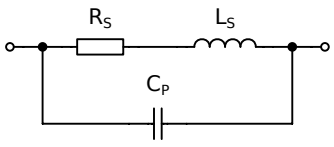


Figure 83 Equivalent schematic diagram of the current sense resistor

The voltage sensed across the resistor is given by

$$U_S(j\omega) = Z_S(j\omega)\, I_S(j\omega) = (R_S + j\omega L_S)\, I_S(j\omega). \tag{7.5}$$

The parasitic inductance of the resistor adds a zero to the transfer function causing amplification of high frequencies. It reduces the current sense resistor bandwidth over which the resistor can be used to measure the current waveforms reliably. The cut-off frequency of the resistor is given by

$$f_0 = \frac{R_S}{2\pi L_S}. \tag{7.6}$$

7.2.3 Frequency compensation of the current sense resistor

The current sense resistor inductance can be effectively compensated using the amplifier that senses the voltage across the resistor. For this purpose, a parallel capacitor C_1 is added to the feedback resistor R_3 to add a pole into the amplifier transfer function. The resulting transfer function can be approximated by

$$C_S(j\omega) = \frac{U_2(j\omega)}{I_S(j\omega)} \approx R_S \frac{R_3\left(1 + j\omega\frac{L_S}{R_S}\right)}{R_2\left(1 + j\omega\frac{1}{R_3 C_1}\right)\left(1 + j\frac{\omega}{\omega_{OA}}\right)}, \tag{7.7}$$

where ω_{OA} is the pole introduced by the operational amplifier while considering the compensated single-pole frequency characteristic of the amplifier. If the pole of the amplifier given by the R_3 and C_1 parallel connection is placed as close as possible to the zero introduced by the sensing resistor, the zero can be partially canceled, and the resulting transfer function can be approximated by

$$\tilde{C}_S(j\omega) \approx R_S \frac{R_3}{R_2\left(1 + j\frac{\omega}{\omega_{OA}}\right)}. \tag{7.8}$$

The only disadvantage of this method is that the parasitic inductance of the resistor has to be known with a certain degree of precision. Since the impedance of the current sense resistor is minimal, and the inductance is expected to be below five nanohenry, an ordinary LC meter cannot be used. The impedance of the resistor was estimated using E7402A EMC spectrum analyzer equipped with a signal generator. The signal transmitter and the receiver were connected directly to the sensing resistor as shown in Fig. 84.

The signal strength at the receiver input in steady state is given by

$$U_R(j\omega) = U_T(j\omega)\, \frac{Z_S(j\omega) \parallel Z_R}{Z_S(j\omega) \parallel Z_R + Z_T}, \tag{7.9}$$

where $Z_T = 50\ \Omega$ is the transmitter output impedance and $Z_R = 50\ \Omega$ is the receiver impedance. Both, Z_T and Z_R are supposed to be constant at all frequencies. The term

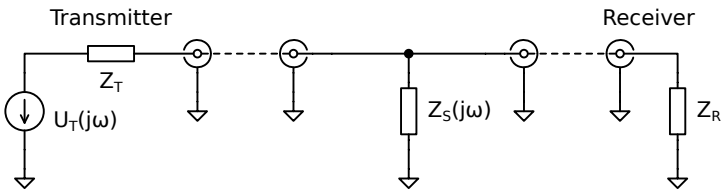
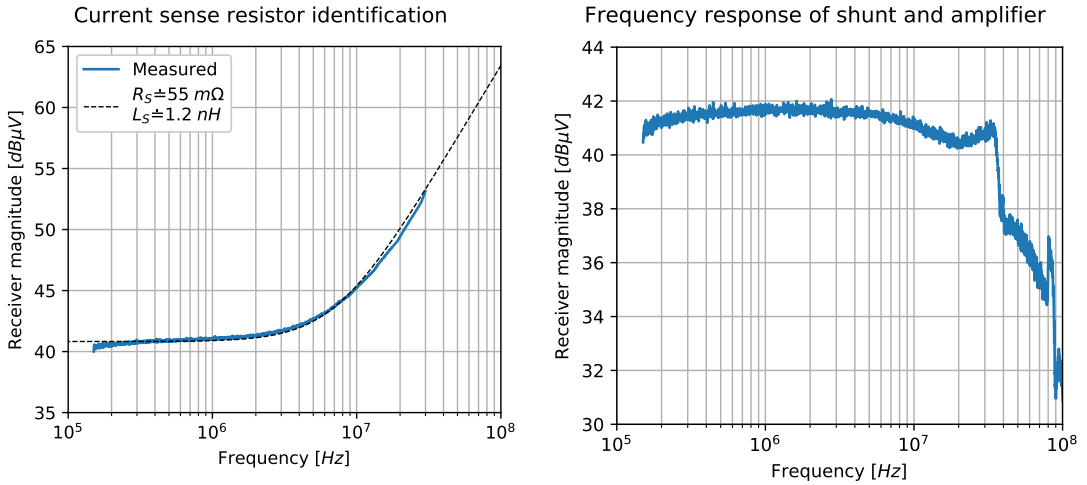


Figure 84 Measurement setup for current sense resistor identification



a) The frequency response of the current sense resistor

b) The frequency response of the current sense resistor and the amplifier

Figure 85 Current sense resistor frequency response compensation

$U_T(j\omega)$ is the transmitter output voltage. The results of the frequency measurements are shown in Fig. 85. Fig. 85a depicts the frequency response of the standalone resistor measured by the EMC spectrum analyzer. The data were analyzed, and values of the resistance and parasitic inductance were estimated using least squares linear fitting. It can be seen from the frequency spectrum that the actual resistance of the shunt is evaluated by ten percent higher than the nominal value. It is most likely caused by parasitic stray resistances of the measurement setup as the coaxial cables were stripped and soldered tightly to the current sense resistor. This setup may not be the best in term of the high-frequency measurement but was found to be sufficient for the current sense identification.

The overall frequency response of the shunt resistor and the amplifier with adjusted compensation for the parasitic inductance is shown in Fig. 85b. It can be seen that the response is flattened especially near the cut-off frequency of the sense resistor. The high frequency resonant like the curvature of the frequency response is probably caused by imperfect mounting and by the geometry of measurement cable placement.

7.2.4 Compensation of time delay in the test equipment chain

Before performing the measurement, it is needed to compensate for the time skewness of the signal paths owing to the analysis of fast transients as described earlier in this chapter. The highest observed du/dt of drain-source voltage during turn-off transient of the low-side MOSFET was nearly 50 Vns^{-1}. In case of input voltage $U_1 = 600\ V$, it takes the voltage to rise from zero to approximately half of the input voltage only several nanoseconds. The highest observed current slope of the low-side switch current was about 1.8 Ans^{-1}. This rate makes the transient to take about eight nanoseconds in case the current rises from 0 to 15 amperes. These times are comparable with signal propagation delay in coaxial cables of the voltage and current probes. The signal is also skewed by the limited bandwidth of the test equipment.

It is, therefore, necessary to perform a calibration of the time delays between used probes before the measurement. For this purpose, a signal generator was used to generate a rectangular waveform on a 50 Ω resistive load. In total four probes were

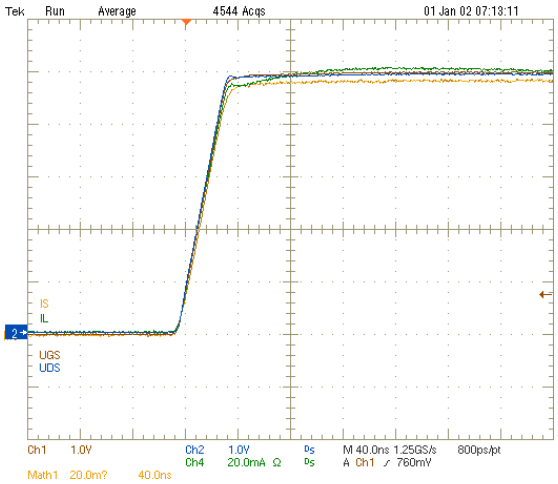


Figure 86 Screen capture of the waveforms with compensated time skewness

used. One low-voltage probe, used for measuring the gate-source voltage of the low-side MOSFET, one high-voltage probe for measuring the drain-source voltage, the current sensing module connected directly to an oscilloscope input and a current probe for inductor current measurement. The current probe was used to sense the current through the termination resistor, and the current sense module was connected to a provisory sense resistor with a higher value than the current sense resistor used for the transistor current measurement.

This procedure allows to roughly compensate for the different time delays between the test equipment. It is performed for a small signal; however, assuming the linearity of the used probes, the skewness should not vary significantly for higher level signals. Never the less, the possible uncertainty must be still taken into account even after performing the time delay compensation.

The propagation delay can be compensated using a feature of the used oscilloscope, so-called deskew. Fig. 86 shows the waveforms with corrected time skewness. Tab. 18 shows the approximate values of the time delay of test equipment, connected to a particular channel, relative to the channel one. It can be seen that in some cases, the values of relative time delay are even higher than the expected duration of transistor switching transients.

Channel	Probe	Time delay	Measured signal
Ch. 1	Low voltage probe — (reference)	0.00 ns	Gate-source voltage
Ch. 2	High voltage probe[2]	-0.80 ns	Drain-source voltage
Ch. 3	Current sense amplifier	7.75 ns	Source current
Ch. 4	Current probe	10.10 ns	Inductor current

Table 18 Values of the time skewness relative to the low voltage probe

7.3 Measuring the dynamic behavior of the SiC MOSFET

Several tests have been performed on the converter using the measurement setup described earlier. The measurements aimed to capture and analyze the waveforms during

[2]The negative value of the time skewness relative to the channel one is caused by shorter cable of the high voltage probe

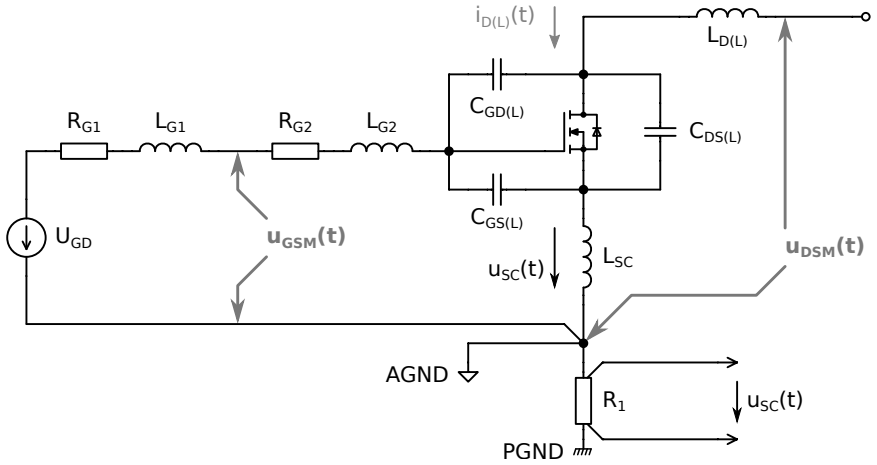


Figure 87 Schematic diagram of the probe placement regarding the parasitic elements

the power MOSFET switching transients. The analysis was done on SiC MOSFET transistors SCT20N120 that were used for the reference design. It is a high voltage SiC power MOSFET capable of high operating temperatures [33].

The waveforms presented in the following sections are the waveforms of the gate-source voltage, the drain-source voltage and the source current of the low-side switch. The inductor current is omitted from the screen captures for clarity. Moreover, the inductor current is almost constant at the time of the studied transient, and only reflects the current oscillations caused by recharging the parasitic parallel capacity of the power inductor and other capacities present in the half-bridge.

In the case of the source current, the math functions of the oscilloscope were used to reproduce the original current in the proper scale. The math one trace represents the source current of the low-side transistor. It is also important to mention that the direction of the drain-source current is negative relative to the direction of the inductor current per the two-port network convention. In such a case, the MOSFET current is positive when flowing into the drain electrode.

7.3.1 Overview of the measurement setup

Before analyzing the acquired waveforms, it is needed to understand what signals are exactly measured. Since the transients that are measured are very fast as described earlier, any stray inductances or parasitic capacitances added between the points of interest and the probes can appear as sources of disturbance of the measured signal. Fig. 87 depicts the simplified schematic diagram of the half-bridge with all the parasitic elements that could influence the observed waveforms. It also shows the notation of parasitic elements used in the following text.

The $u_{GSM}(t)$ marks the point where the gate-source voltage is measured. It can be seen that the sensed voltage cannot be related to the exact gate-source voltage that appears between the gate and the source electrode inside the MOSFET. The measured voltage is decoupled by an inductance L_{G2} and resistance R_{G2}. The inductance L_{G2} consists of parasitic gate inductance and stray inductance of the transistor leads. Similarly, the resistance R_{G2} is given by the combination of internal gate resistance and by the resistance of transistor leads.

Moreover, it can be seen that a voltage across the stray inductance L_{SC} adds to the measured voltage at channel one. It is the inductance of a part of the source electrode that is common for the inductor current loop and the gate driving loop.

This parasitic inductance can have probably the greatest influence on the measured gate-source voltage due to the very high di/dt during the current commutation. For instance, even several nanohenry of the inductance can produce several volts considering the maximum observed current slope in around one ampere per nanosecond.

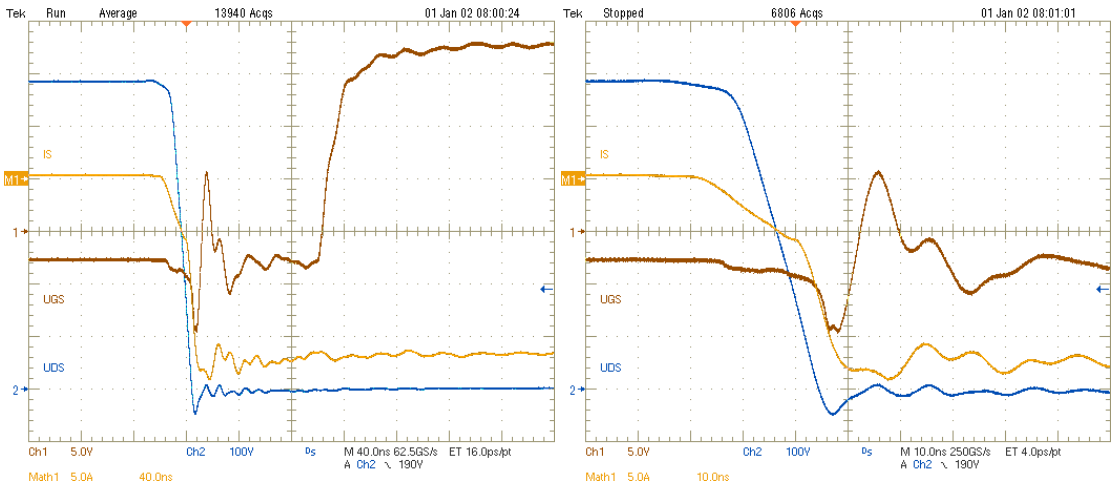
The $u_{DSM}(t)$ is the voltage measured across the drain and source electrodes of the transistor. This voltage may be influenced by the stray inductances of the transistor leads as well as by the parasitic inductance of the drain and source electrodes itself. However, the voltage across the parasitics is considerably smaller compared to the voltage blocked by the MOSFET, which is up to the input voltage rail. Hence, the influence of these inductances can be neglected as well as of the resistances of the drain and source that are not shown in the schematic for clarity.

The $u_{RS}(t)$ is the voltage among the sense resistor. The operational amplifier probably causes the most significant distortion of the current sense voltage. The most significant influence is as in case of other probes in the phase error caused by the propagation delays that were already compensated by time skewness calibration. However, the possible distortion by the limited bandwidth and slew rate of the operational amplifier has to be kept in mind, especially when investigating the acquired waveforms.

7.3.2 Observing turn-on transient of the low-side transistor

This section focuses on the turn-on transient of the low-side switch and the turn-off of the high-side switch at different output loads. During the steady state operation of the synchronous buck topology, the low-side switch is always turned on while the body diode is conducting. It is caused by the current inductor to be negative relative to the drain current direction marked in Fig. 87. Hence, the body diode conduction causes soft switching of the power transistor — the transistor switches at a moment when the forward voltage of the body diode is across the source and drain.

A turn-on transient of the low-side switch acquired during the output power 4.2 kW and the output current 12 A is shown in Fig. 88a. It can be seen from the waveform that the interesting part is the turn-off transition of the high-side switch. After the high-side switch is turned off, a dead time is inserted. The switch on of the low-side switch occurs when the gate-source voltage is driven high by the gate driver. The transistor channel



a) Waveforms after low-side swith turn-on **b)** Detail of the turn-on transient

Figure 88 Waveforms taken during the turn-on transient

takes over the body diode current when the $u_{GS(L)}(t)$ crosses the threshold voltage.

Fig. 88b shows the detail of the transient during the high-side switch turn-off. The observed waveform can be split into several time intervals. At the beginning of the first interval, the high-side MOSFET gate-source voltage falls close to the threshold voltage. If we take an approximation that the transistor transconductance is approximately constant above the threshold voltage, the drain current of the high-side switch $i_{D(H)}(t)$ starts to be limited.

At this considerably short time instant, the inductor can be seen as a constant current source. Considering the parasitic capacitance of the power inductor, it holds for the inductor current

$$i_L(t) = i_{D(H)}(t) + i_{D(L)}(t) + i_{L_C}(t), \tag{7.10}$$

where $i_{L_C}(t)$ is the current flowing through the inductor parasitic capacity, $i_{D(H)}(t)$ is the high-side switch drain current[3] and $i_{D(L)}(t)$ is the drain current of the low-side switch. The drain current of the low-side switch can be further split into two parts

$$i_{D(L)} = \tilde{i}_{D(L)}(t) + i_{M(L)}(t), \tag{7.11}$$

where $\tilde{i}_{D(L)}(t)$ is the current flowing hrough the channel of the MOSFET and $i_{M(L)}(t)$ is the current flowing through the Müller capacity $C_{GD(L)}$. Some part of the current recharging the Müller capacity is consumed by the gate driver and other part is flowing into the gate of the low-side transistor. Both currents return to the source electrode, which means, that the source current reflects the drain current of the transistor.

Taking a closer look at the equation 7.10, it is evident that the current through the high-side switch channel is limited, the current is forced to flow through the capacities of the low-side transistor, high-side transistor and the capacity of the inductor. Since it applies for current through any arbitrary capacity

$$i_C(t) = C\frac{du_C(t)}{dt}, \tag{7.12}$$

the voltage of the half-bridge starts to increase as the inductor current tends to recharge all the mentioned capacities. The Müller capacity $C_{GD(L)}$ and the drain-source capacity $C_{DS(L)}$ of the low-side switch were previously charged to the voltage blocked by the transistor, while the high-side switch capacities were discharged. The inductor current is split between the high-side and the low-side transistor. It can be seen from the waveform in Fig. 88b, that the low-side switch source current starts increasing slowly since the majority of the inductor current is recharging the high-side switch capacities, which is caused by their voltage dependency capacities as shown in Fig. 89.

Fig. 89 depicts the voltage dependency of the input capacity C_{ISS}, the output capacity C_{OSS} and the reverse transfer capacity C_{RSS}. They are the small signal capacities. It holds for the mentioned capacities [2]

$$C_{ISS} = C_{GS} + C_{GD}, \tag{7.13}$$
$$C_{OSS} = C_{GD} + C_{DS}, \tag{7.14}$$
$$C_{RSS} = C_{GD}. \tag{7.15}$$

[3]The high-side transistor source current differs from the drain current by a leakage current flowing through a parasitic capacity of the gate driver to surrounding fixed potential

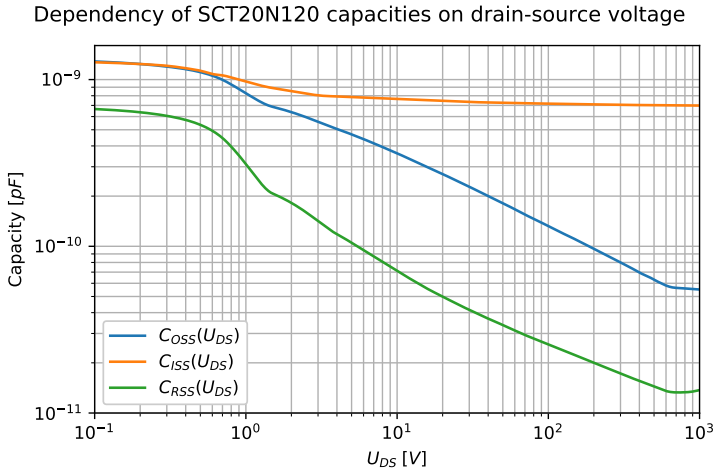


Figure 89 Dependency of MOSFET capacities on drain-source voltage, data source: [33] and SCT20N120 PSpice model

It can be seen from the graph in Fig. 89, that all the capacities are higher for lower voltages. Hence, the output effective capacity of the low-side switch $C_{OSS(L)}$, that was initially turned off, is much lower compared to the same capacity of the high-side switch — $C_{OSS(L)} \ll C_{OSS(H)}$ since $u_{DS(L)} \gg u_{DS(H)}$. Thus, at the beginning of the switch-off transient of the high-side switch, the majority of the inductor current is flowing through the high-side switch $C_{GD(H)}$ and $C_{DS(H)}$. The current through the Müller capacity of the high-side switch is being handled by the gate driver [2, 10].

As the voltage across the low-side switch $u_{DS(L)}$ falls and the high-side switch voltage $u_{DS(H)}$ rises, the $C_{OSS(L)}$ is increasing and the $C_{OSS(L)}$ is decreasing. The increase of the $C_{OSS(L)}$ causes the increase of the low-side switch current since the voltage slope remains approximately constant. Near the end of the voltage transition, the effective output capacity of the low-side switch is significantly higher than the same capacity of the high-side switch — $C_{OSS(L)} \gg C_{OSS(H)}$ since $u_{DS(L)} \ll u_{DS(H)}$, Hence the low-side transistor takes the majority of the inductor current.

The last phase of the transient appears at the moment when the capacitances inside the half-bridge are recharged to the voltages corresponding to the off-state and on-state of the high-side and the low-side MOSFET respectively. It can be seen from the waveforms in Fig. 88b that as soon as the diode starts to be forward biased, the voltage $u_{DS(L)}$ keeps decreasing under zero until the diode takes over the whole inductor current. This peak forward recovery voltage U_{FP} can be several times higher than the steady-state forward voltage.

Taking a closer look at the gate-source voltage u_{GSM}, an influence of the parasitic inductance of path common for the inductor current and gate driving loop L_{SC}, can be seen. During the current commutation, negative voltage spikes are added to the measured signal as a negative voltage across the parasitic inductance L_{SC} appears. Moreover, a voltage across the gate-source is influenced by the current flowing through the Müller capacity. However, this influence may not be as high as in case of the voltage induced by $di_{D(L)}/dt$ as per the measured waveforms.

The highest observed current slope when the body-diode takes over the inductor current is about 1.8 $A\,ns^{-1}$. Considering the parasitic inductance of a straight conductor to be very roughly 1 $nH\,mm^{-1}$, the voltage induced across the 4 mm long wire, which is approximately the length of the source lead, can be estimated to be around 7.2 V.

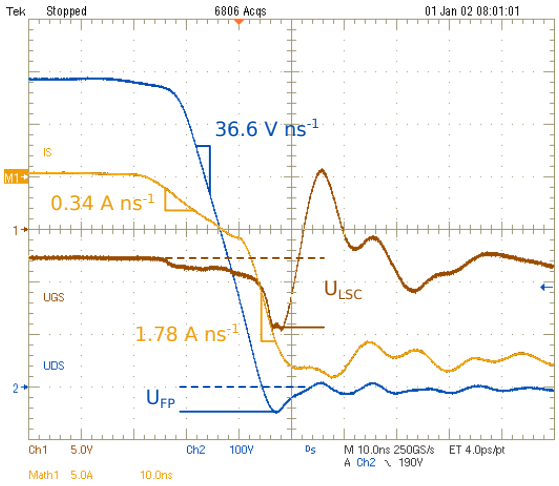


Figure 90 Analyzed high-side MOSFET turn-off transient

This estimation complies with the measured waveforms. Fig. 90 shows the analyzed waveforms of the high-side transistor switch off transient.

7.3.3 Observing turn-off transient of the low-side transistor

This section deals with an analysis of the low-side switch turn-off, and the high-side switch turn-on transient. During the steady state operation of the converter when the half of the inductor current ripple is lower than the mean value $\langle i_L(t)\rangle_{T_S}$, the low-side transistor is switched off when the inductor current is still positive. It makes the body diode of the low-side MOSFET take over the current while the channel is turned off. Hence, the body diode causes soft switching of the low-side transistor. This state is typical if the converter operates under the output load.

Conversely, if the converter operates under the light load operation, or if the half of the inductor current ripple is lower than the mean value of the inductor current, the inductor current becomes negative. Hence, the inductor current commutes through the high-side transistor body diode after the low-side transistor is switched off which results in the low-side transistor hard switching.

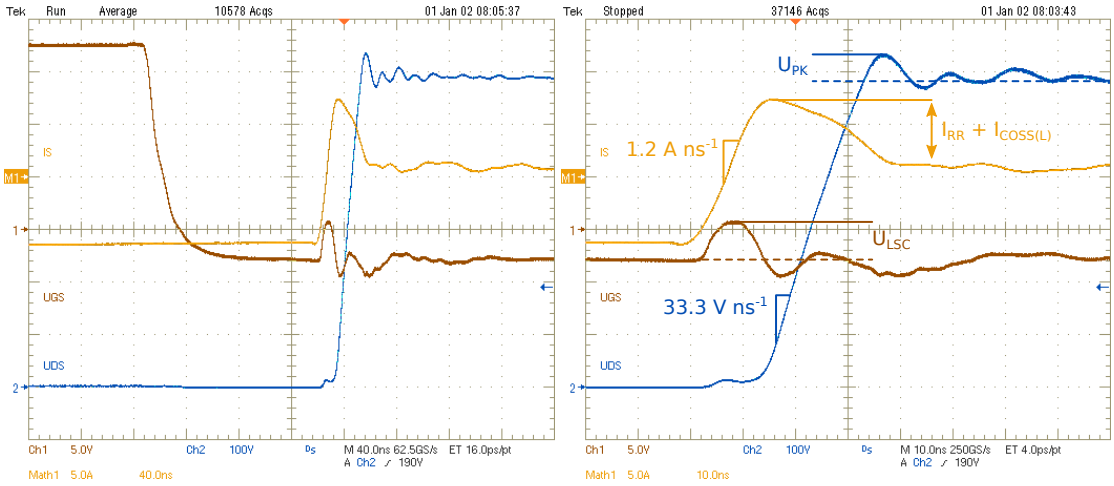
Soft switching of the low-side transistor

The transient during the full load operation is discussed in this section. The waveforms are acquired at the output power of 4.2 kW and output current 12 A.

The waveform of the transient is shown in Fig. 91a. After the gate-source voltage of the low-side switch is driven to the off state level, a dead time interval starts. It can be seen, that after the gate-source voltage falls below the threshold, the drain-source voltage decreases slightly by the forward voltage drop caused by the body diode.

As soon, as the high-side transistor is driven on, it takes over the inductor current, and the low-side switch current falls to zero. Since the low-side transistor body diode was forward biased and was initially conducting, the reverse recovery effect takes place. The reverse recovery charge of the diode has to be discharged by the high-side MOSFET. It causes the current $i_{S(L)}(t)$ to reverse the direction, and a positive peak caused by the diode recovery appears as can be seen in Fig. 91b. The diode reverse recovery current flows through the half-bridge from the high-side to the low-side switch.

By considering the capacitances of both, the high-side and the low-side transistor,



a) Waveforms of the high-side switch turn-on **b)** Detail of the turn-on transient of high-side switch

Figure 91 Waveforms of the turn-off of the low-side MOSFET and the turn-on of the high-side MOSFET

the inductor current is of opposite direction than needed to discharge the $C_{OSS(H)}$ to on-state drain-source voltage and charge $C_{OSS(L)}$ to the input voltage. Hence, current recharging the capacities of both transistors flows through the half-bridge in the same direction as the reverse recovery current of the low-side switch body-diode. The low-side switch current is the sum of the reverse recovery current and the current recharging the $C_{OSS(L)}$. However, it can be seen from the waveforms, that the reverse recovery of the body diode takes the majority of the measured current $i_{S(L)}(t)$ as there is no significant increase in drain-source voltage.

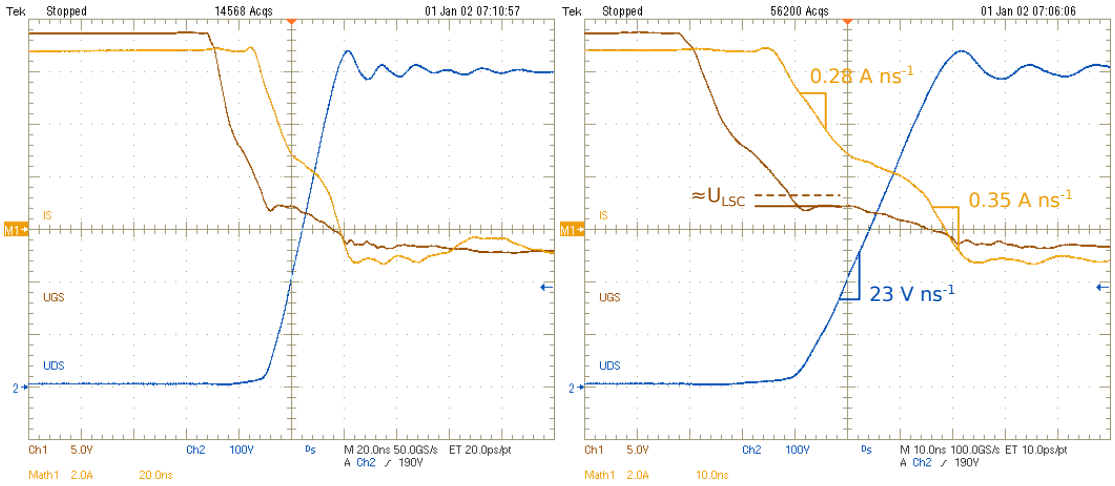
As soon as the reverse recovery current of the diode decays to zero, the majority of the current recharges the $C_{OSS(L)}$ capacity causing a rapid increase of the $u_{DS(L)}(t)$ voltage. As stated before, the inductor current is of an opposite direction so as long as the $u_{DS(L)}(t)$ voltage is increasing there is a current flowing through the half-bridge. Since the $C_{OSS(L)}$ capacity decreases with increasing $u_{DS(L)}(t)$ voltage, the current falls as the voltage slope is approximately constant.

The critical loop inductance causes the overshoot of the $u_{DS(L)}(t)$ voltage at the end of the switching transient by the U_{PK} marked in Fig. 91b. The voltage spread across the parasitic inductances of the critical loop adds to the input voltage and adds to the oscillations at the end of the transient. The ringing at the end of the transient is caused by the parasitic capacity of the inductor and capacities inside the half-bridge as the same ringing was observed in the current flowing through the inductor.

Similarly, the measured gate-source voltage $u_{GSM}(t)$ is influenced by the voltage generated across the inductance of path common for the inductor current loop and the gate driver loop. Fig. 91b shows the analyzed waveform during the investigated transient.

Hard switching during low-side transistor

This section shows the acquired waveforms during hard switching of the low-side MOSFET. The turn-off transient of the low-side transistor was observed at no output load. The converter was set to operate with duty cycle $\delta = 0.5$ to make the current ripple the maximum value. Moreover, the operating frequency of the converter was set to



a) Waveforms of the low-side switch turn-off **b)** Detail of the turn-off transient of the low-side switch

Figure 92 Waveforms of the turn-off of the low-side MOSFET

$f_S = 35\ kHz$ to increase the peak current at which the transistor switches off.

Fig. 92a shows the acquired waveforms. The switching transient can be again divided into several time instants. At the first point, the gate driver drives the output to the off-state voltage. The gate-source capacity is discharged through the gate resistance. As soon as the gate-source voltage falls close to the level at which the drain current starts to be limited by the transistor transconductance, the inductor current starts charging the output capacity of the low-side transistor $C_{OSS(L)}$. Since the $C_{OSS(L)}$ has the highest value for the on-state voltage across the drain and source, the majority of the current flows through the low-side switch.

The gate-source voltage at which the current starts to be limited is about $10\ V$ [33]. However, the observed gate-source voltage is distorted by the voltage across the parasitic inductance L_{SC} as described earlier. Hence the actual value is lowered when the high $di_{S(L)}(t)/dt$ is present.

As the gate-source voltage further decreases, the current that charges the $C_{OSS(L)}$ capacity increases and the $u_{DS(L)}(t)$ starts increasing. At this moment, the Müller effect takes place, and a current is being injected to the gate of the transistor. The injected current causes the voltage across the gate persists near the threshold voltage of the transistor. During that time, the $C_{OSS(L)}$ is charged and $C_{OSS(H)}$ is discharged by the inductor current. The nonlinearity of mentioned capacities as described in section 7.3.2 causes the inductor current distribution over the low-side and the high-side transistor to vary with increasing $u_{DS(L)}(t)$ voltage.

Since the $C_{OSS(L)}$ is decreasing rapidly and the $C_{OSS(H)}$ is increasing, the $i_{S(L)}$ falls down with increasing $u_{DS(L)}(t)$ since the voltage slope is approximately constant. The effect is complementary to the switch off of the high-side transistor.

The turn-off transition is done as soon as the drain-source voltage rises above the input voltage. At this moment, the high-side switch body diode starts to be forward biased and takes over the inductor current. The forward recovery voltage peak of the high-side switch body diode adds to the overall peak voltage present in the measured drain-source voltage.

8 Conclusion

This work provided the design description of high power, synchronous buck based converter. A reference design capable of the output power and input and output voltage ranges specified by the assignment was presented. A detailed overview of the converter power stage as well as of the necessary parts such as gate drivers and isolated DC/DC converters used for powering the gate drivers was provided. Concerning the critical loop of the converter, a detailed study of parasitic elements was performed. The parameters of the parasitic elements were extracted using a method of identification from the transient response in a time domain. Hence special techniques had to be used to process the acquired waveforms to obtain relevant results. However, repetitive results were finally obtained after fine-tuning the used signal processing methods.

The main goal of this work, however, was to design and realize a control unit for the power converter. Hence a detailed description of the control unit architecture was provided. The part implementing output voltage, input voltage, and inductor current signal conditioning was described in detail. The control unit signal processing and mainly the mapping of measured signals to the microcontroller unit was done to provide some level of versatility. It allows the control unit to be also used for control of a synchronous boost converter.

Even the control unit design has passed some evolution until the variant presented in this work, some points of improvement were found during the usage of the control unit. However, the control unit performs well, and a certain degree of safety is guaranteed as the control unit implements a variety of protections. Even during the firmware development, some protection mechanisms were already useful and prevented some dangerous conditions, especially the overcurrent condition. The control unit communication interface is done in its form to give full control of the power converter, so it provides configuration of the output PWM signal properties. The control unit allows switching between closed loop operation and open loop control and some additional features.

Following the converter design, the dynamic model of the converter behavior was derived using the method of averaged state space modeling. The model was used for creating simulations in Python and for designing and verifying the closed-loop response of the converter controller. A controller capable of both, the constant voltage and constant current was designed and implemented in the control unit firmware. Hence, the converter can operate with all kinds of load connected to the output, for example, with constant voltage load with minimal series resistance, as is for example, in case of battery packs. The closed-loop behavior of the converter controlled by the control unit was tested by observing the step response transient.

Finally, the power converter was used to perform several tests and measurements. The switching performance of the high voltage SiC power MOSFETs was the primary concern. For a detailed investigation of the switching waveforms, a simple circuit for measuring the low-side transistor current was proposed. The current measurement using a current sensing resistor proved as the only applicable approach since there was no measurement equipment capable of measuring such fast transients. A detailed study of the current sense resistor parasitics and its frequency compensation has been performed to reproduce the current waveform with reasonable fidelity.

Finally, a brief analysis of the switching waveforms was provided. However, digging deeper into the switching performance of the SiC-based MOSFETs and providing a more elaborate description and analysis of all the phenomena associated with high power semiconductor switching, would require more time and better knowledge of the topic, and is far beyond the scope of this text.

Appendix A

Schematic diagrams of the control unit

The schematic diagrams of the control unit are included here. The schematic diagrams are printed two-sided instead of printing one schematic per sheet of paper to save some paper. The complete block diagram of the control unit is in the schematic page shown in Fig. 93.

Schematic diagram of the DC/DC converter powering the control unit is shown in Fig. 94. The current sensing and voltage sensing schematic sheets are shown in Fig. 95 and Fig. 96 respectively. Fig. 97 depicts a schematic diagram of the control unit MCU. Primarily, the mapping of current sensing and voltage sensing signals to the MCU can be seen from this schematic. The communication interface can be seen in Fig. 98.

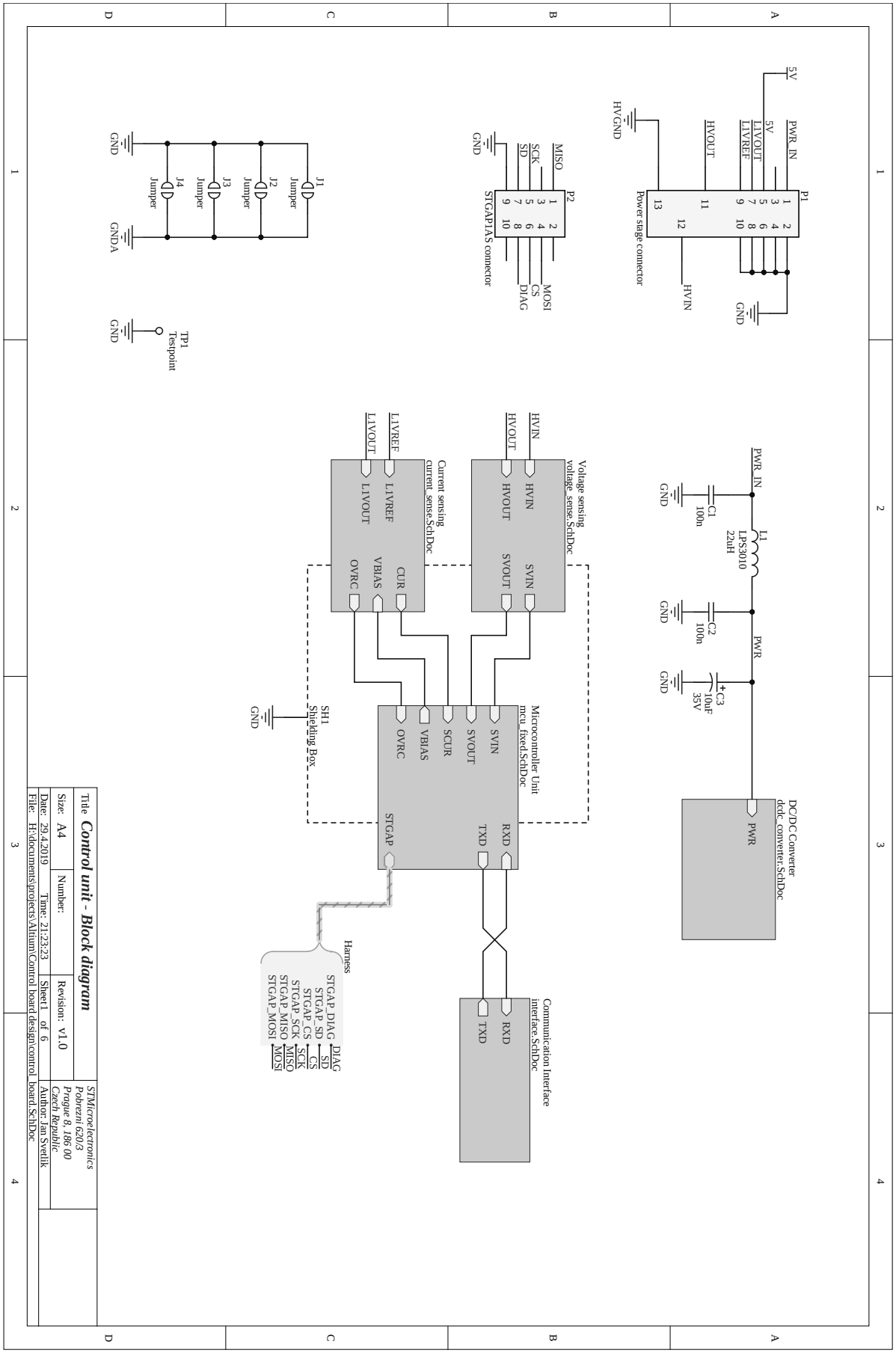


Figure 93 The schematic page of the control unit block diagram

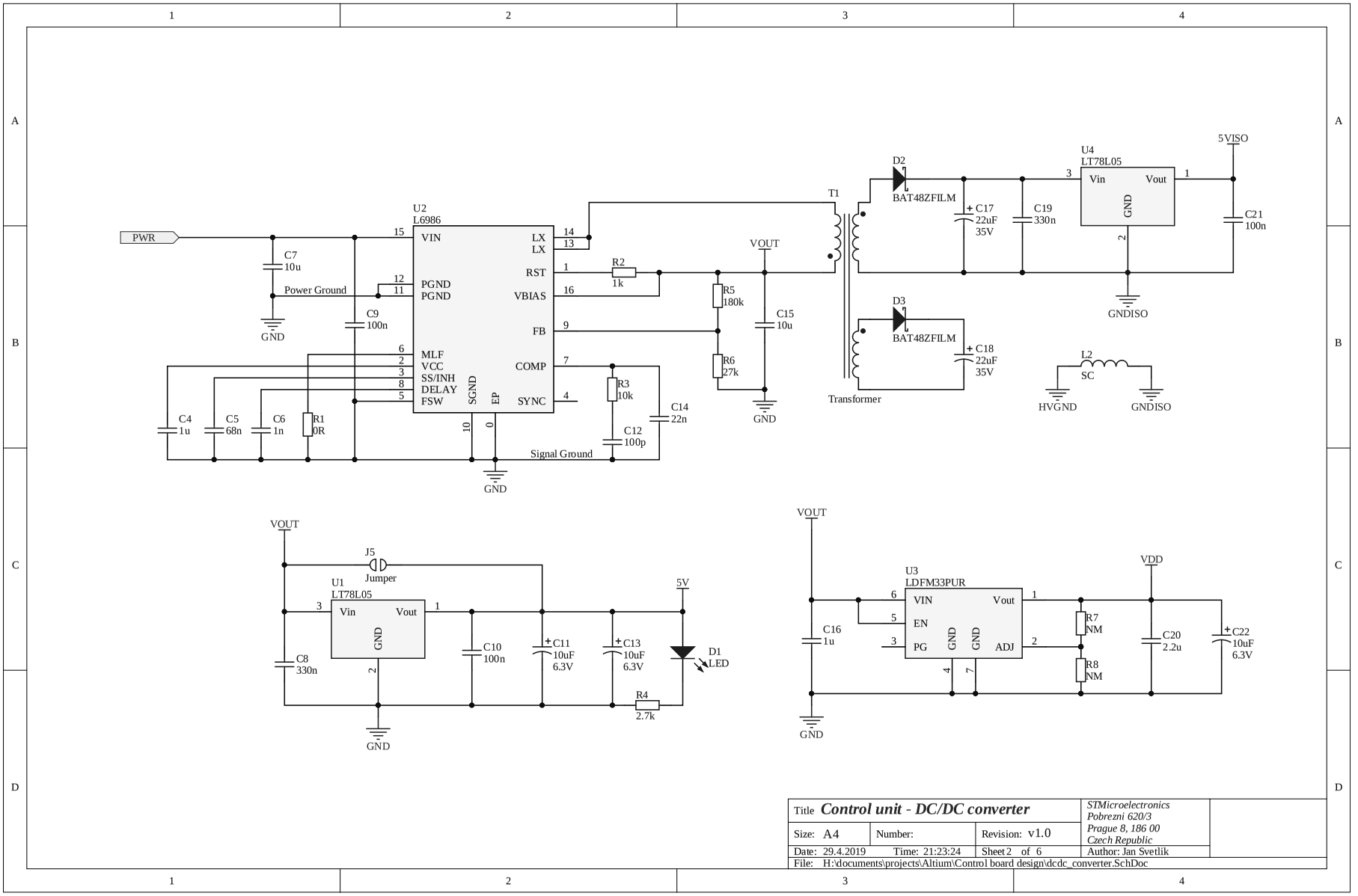


Figure 94 The schematic page of the control unit powering

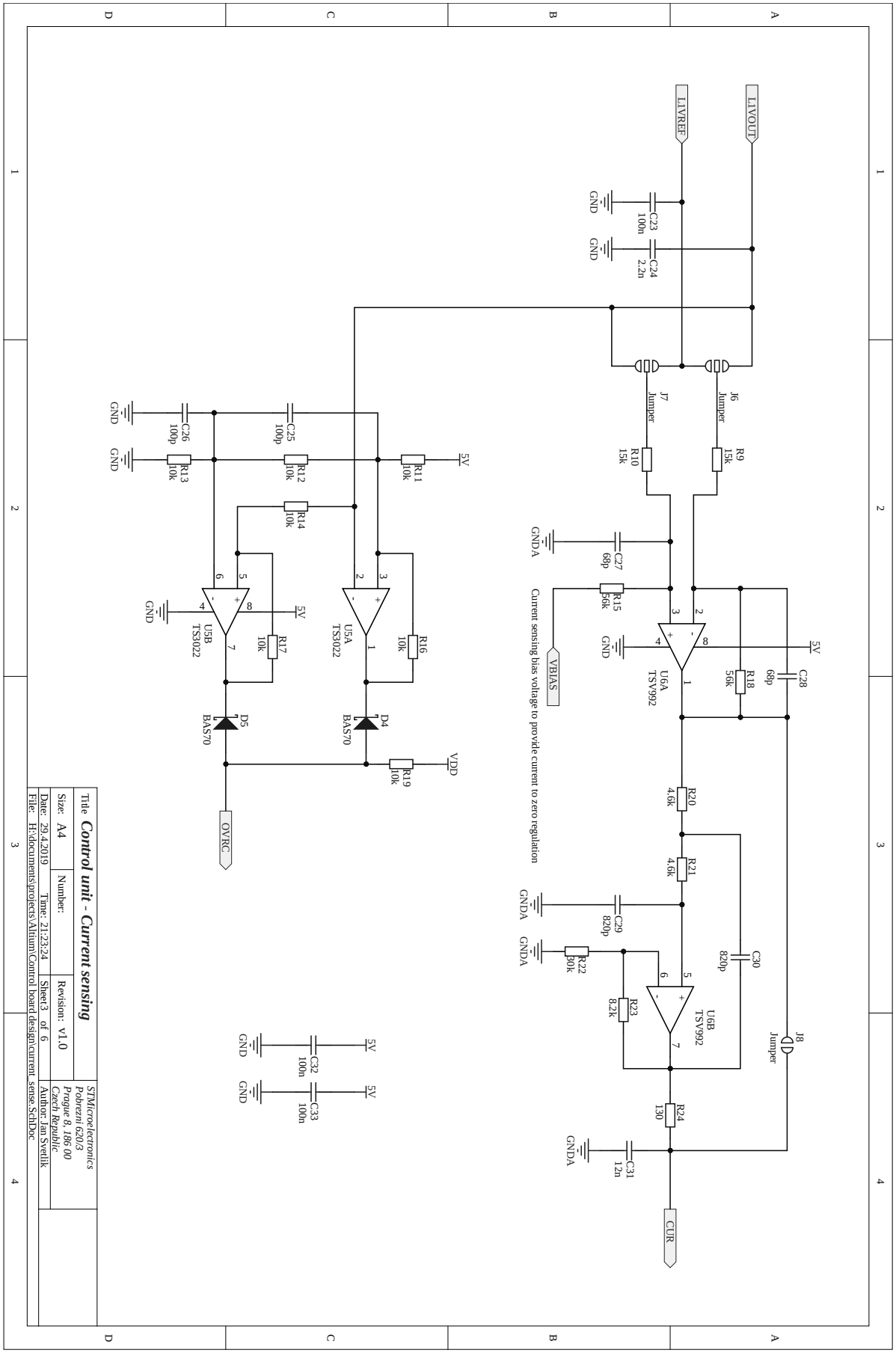


Figure 95 The schematic page of the signal conditioning of the current sensing

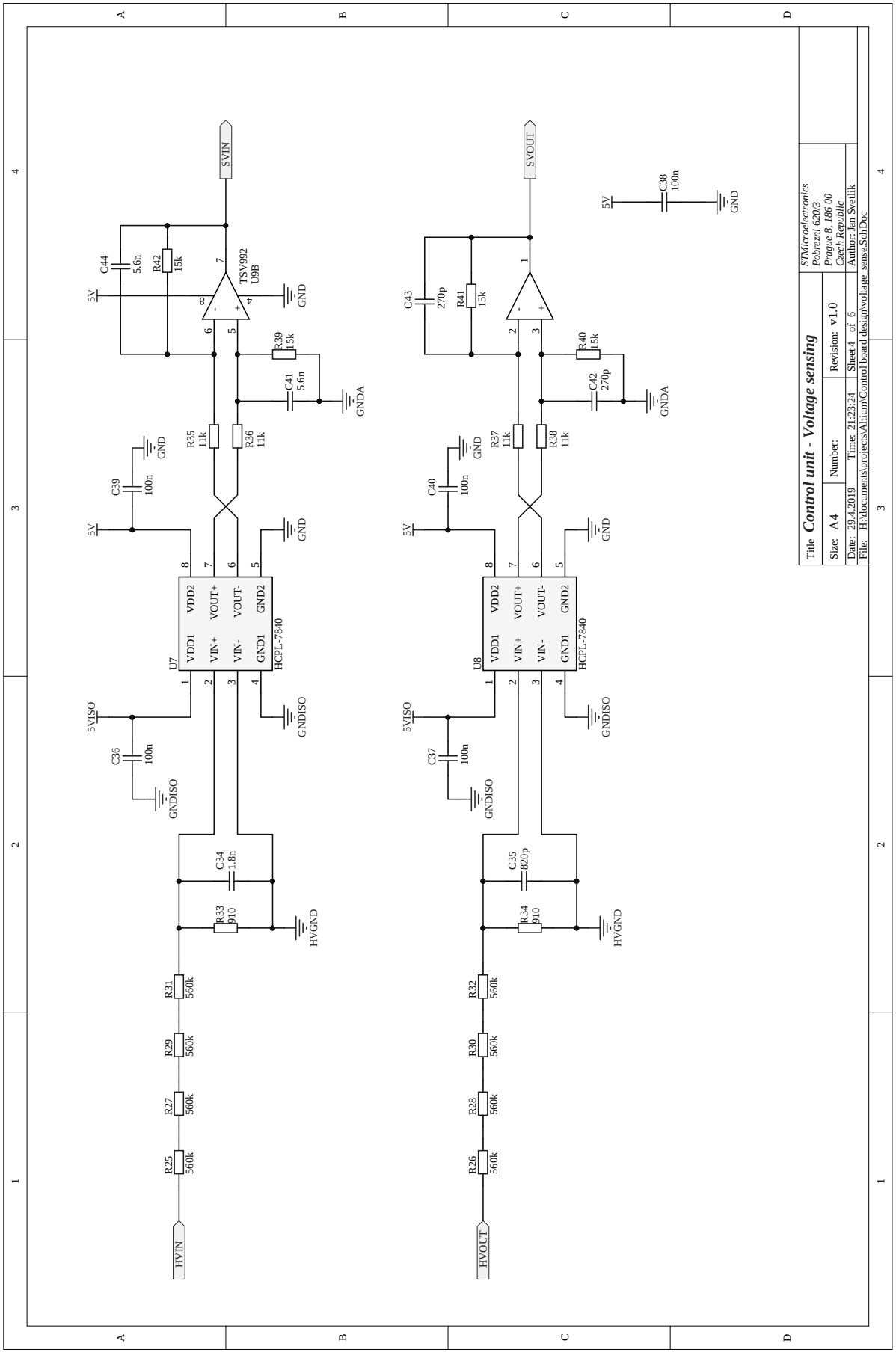


Figure 96 The schematic page of the signal conditioning of input and output voltage sensing

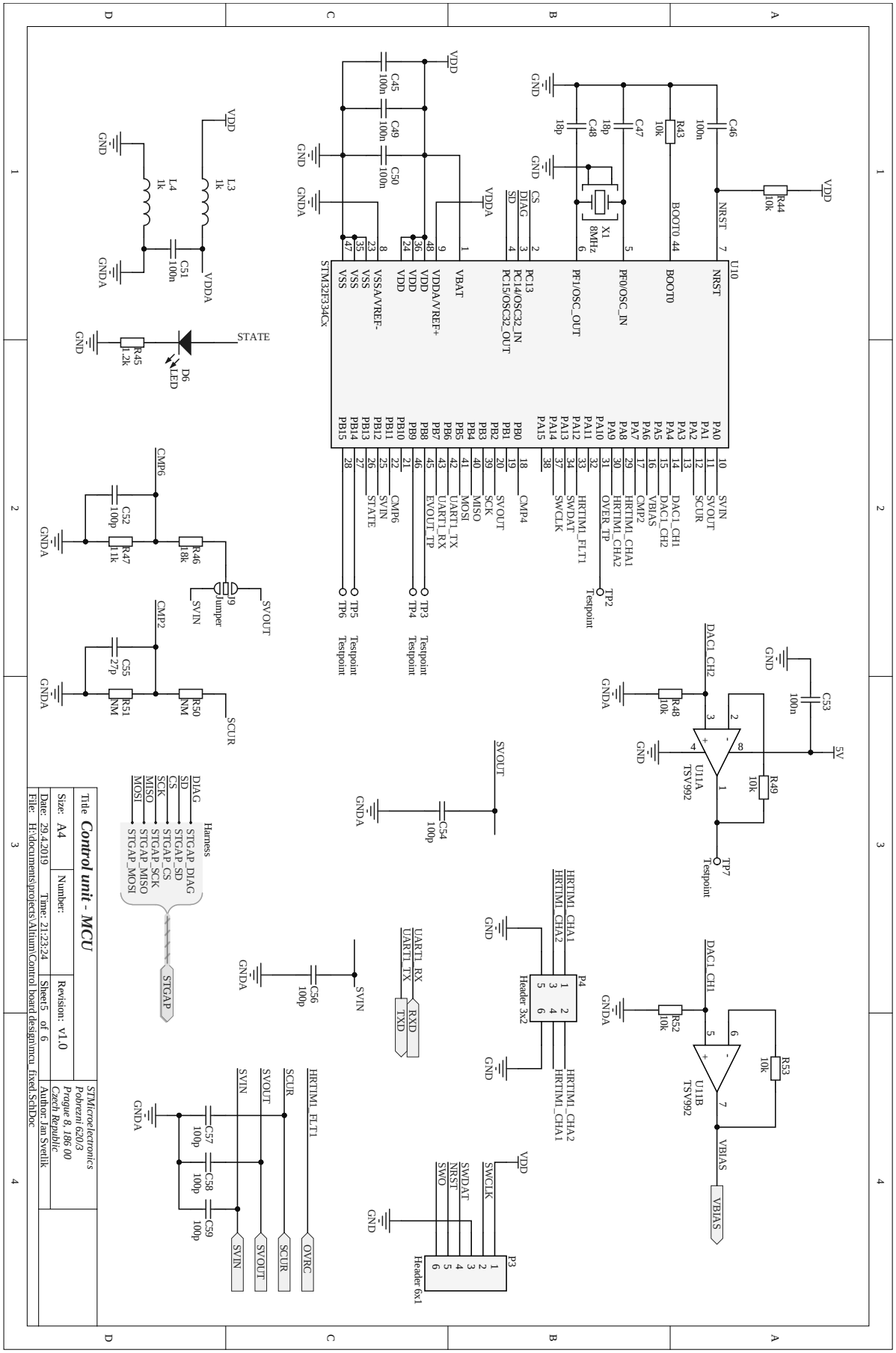


Figure 97 The schematic page of the microcontroller connection and input/output signal mapping

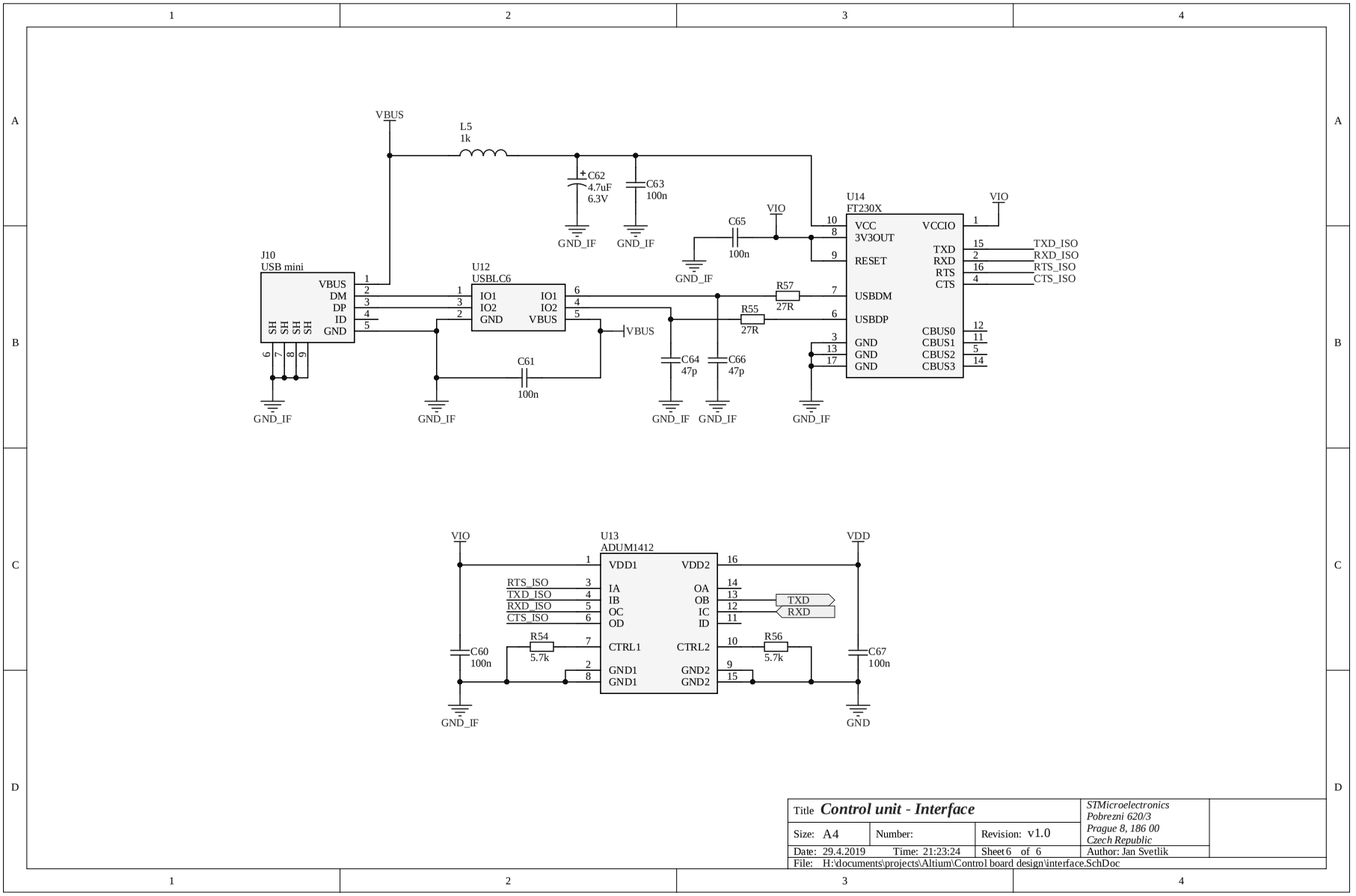


Figure 98 The schematic page of the insulated communication interface

Appendix B

Schematic diagrams of the converter power stage

This appendix contains schematic diagrams of the power stage of the converter. It also includes schematic sheets of all the gate driver modules and the isolated DC/DC module used for powering the gate drivers.

Fig. 99 shows the schematic diagram of the power stage half-bridge. The primary side of the power stage, including the gate driver modules and all the current transducer present on the current power stage version, is shown in Fig. 99.

Schematic diagram of the isolated DC/DC converter used for powering the gate driver modules is shown in Fig. 101.

Fig. 102 depicts schematic sheet of the STGAP1AS based gate driver module. The schematic diagrams of STGAP2S and STGAP2SC based gate driver modules are shown in Fig. 103 and Fig. 104 respectively.

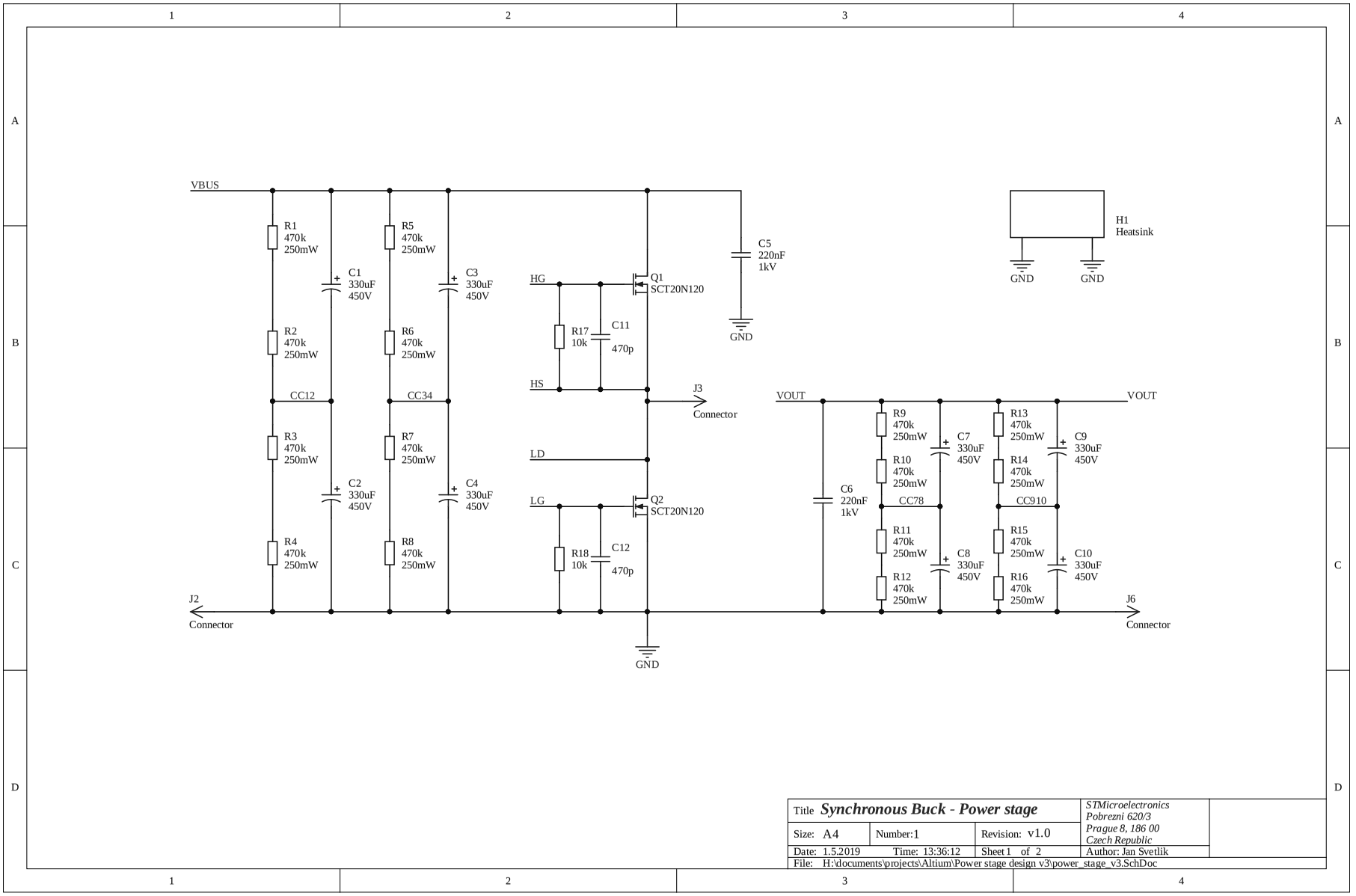


Figure 99 The schematic sheet of the power stage half-bridge

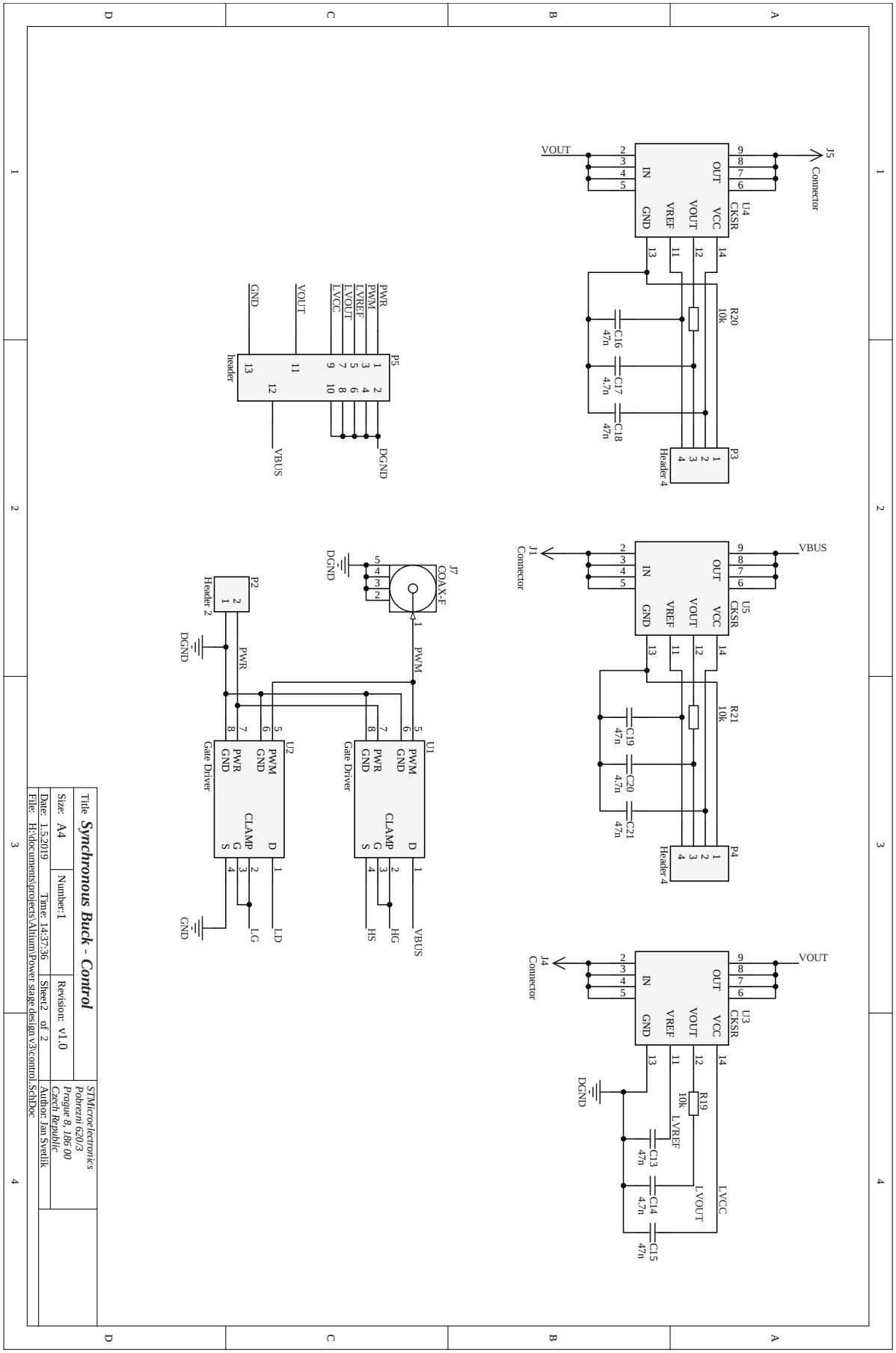


Figure 100 The schematic sheet of the power stage control and current transducers

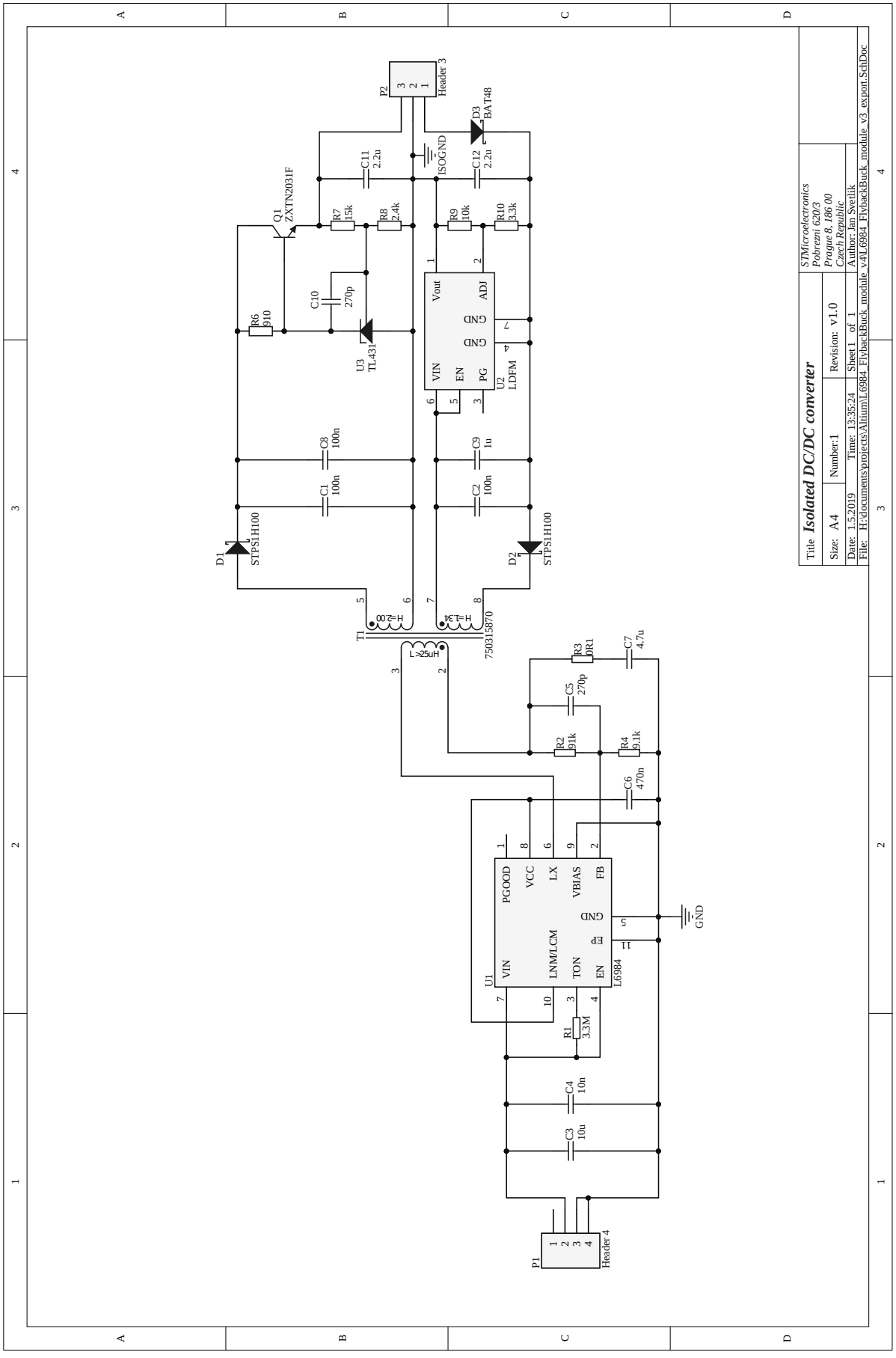


Figure 101 The schematic sheet of the isolated DC/DC converter used for powering the gate driver modules

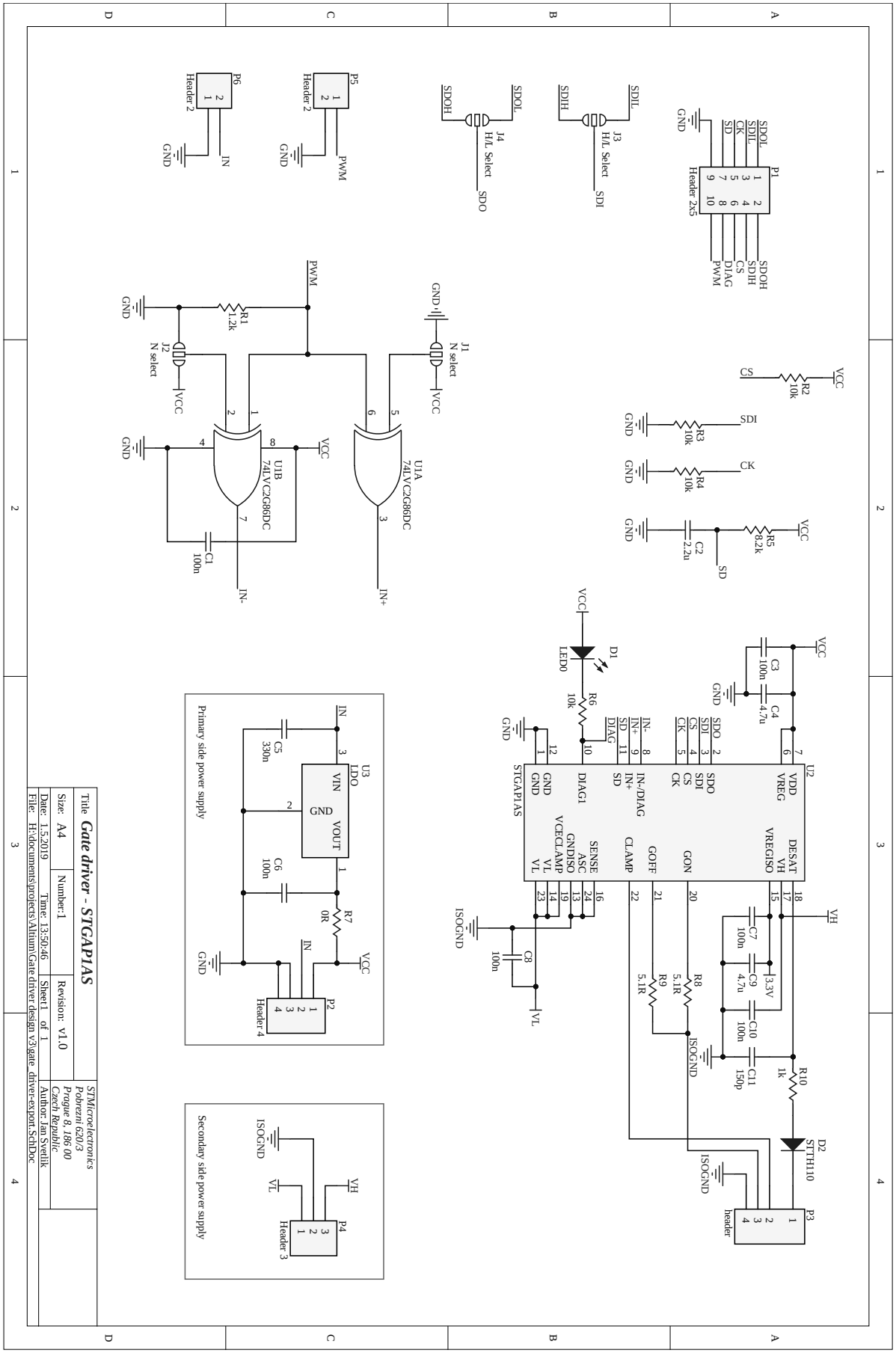


Figure 102 The schematic sheet of the STGAP1AS based gate driver module

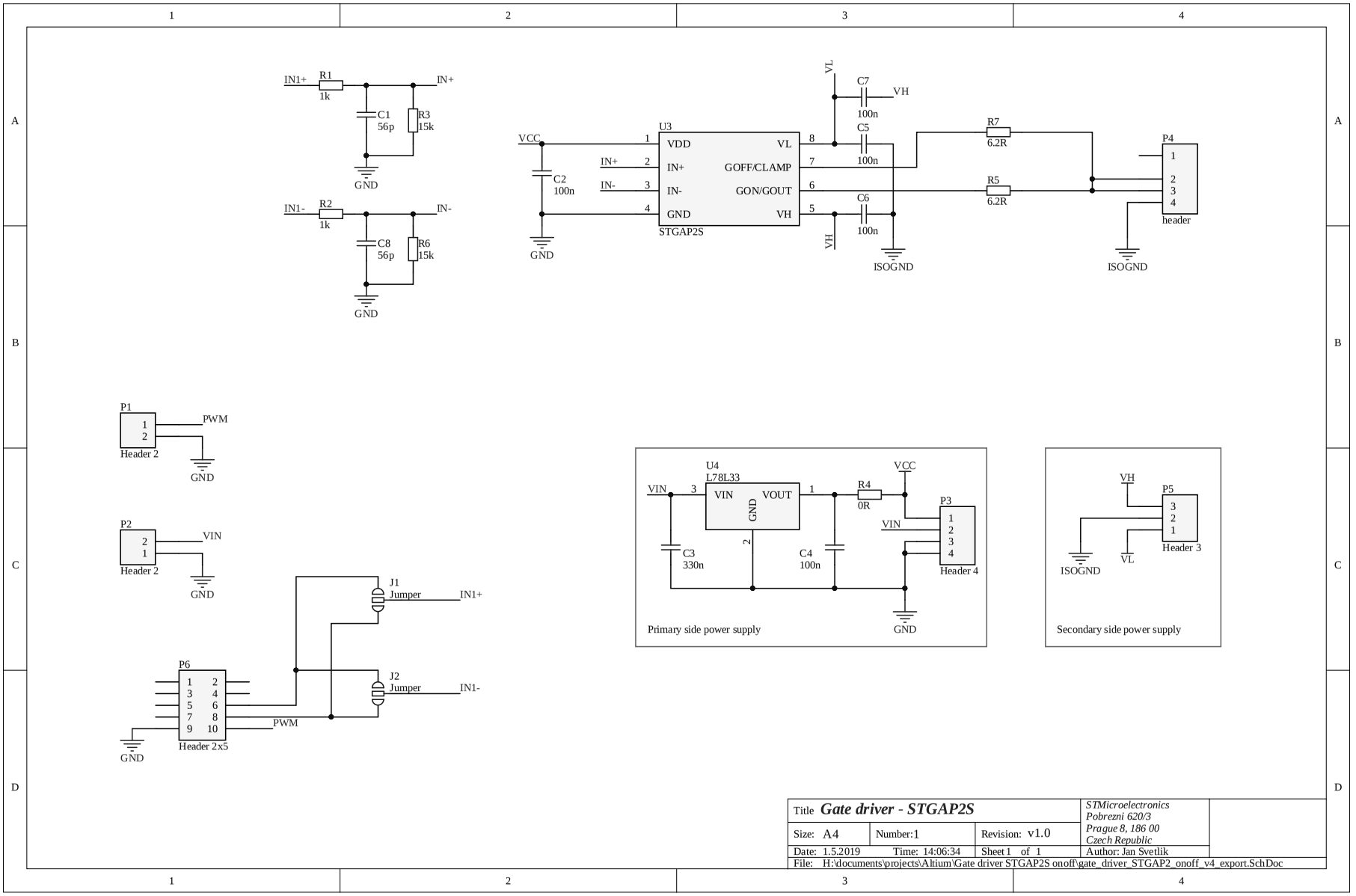


Figure 103 The schematic sheet of the STGAP2S based gate driver module

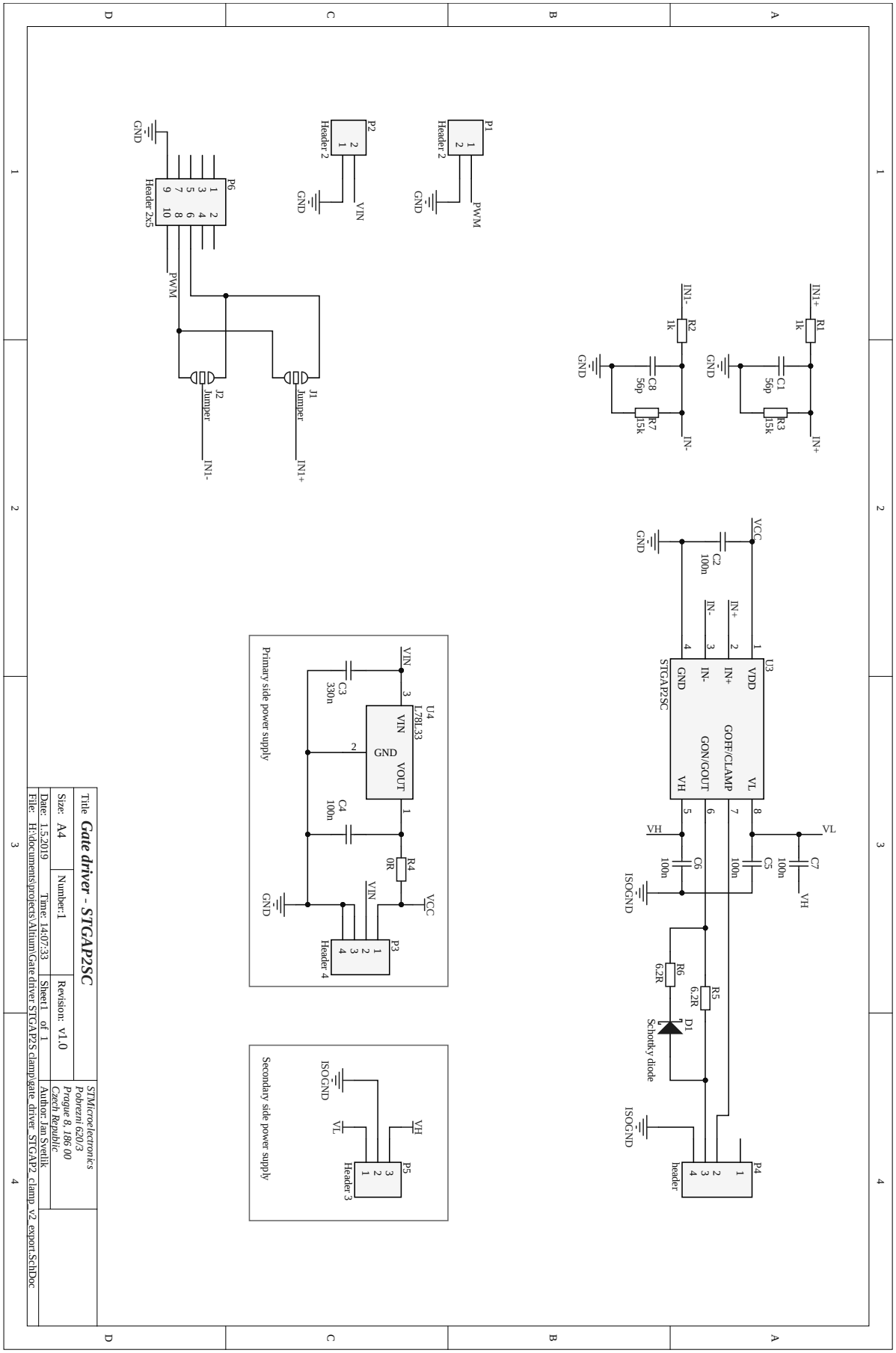


Figure 104 The schematic sheet of the STGAP2SC based gate driver module

Appendix C

Photos of the power stage and control unit

This appendix contains chosen photos of the control unit connected to the converter power stage. The control unit prototype interconnection with the converter power stage is shown in Fig. 105. The ST-Link programmer used as the UART to USB converter can be seen in the lower left corner. A photo of the final version of the control unit driving the power converter is shown in Fig. 106. A picture of the probe setup used for the acquisition of the waveforms of the switching transients during the converter operation is shown in Fig. 107.

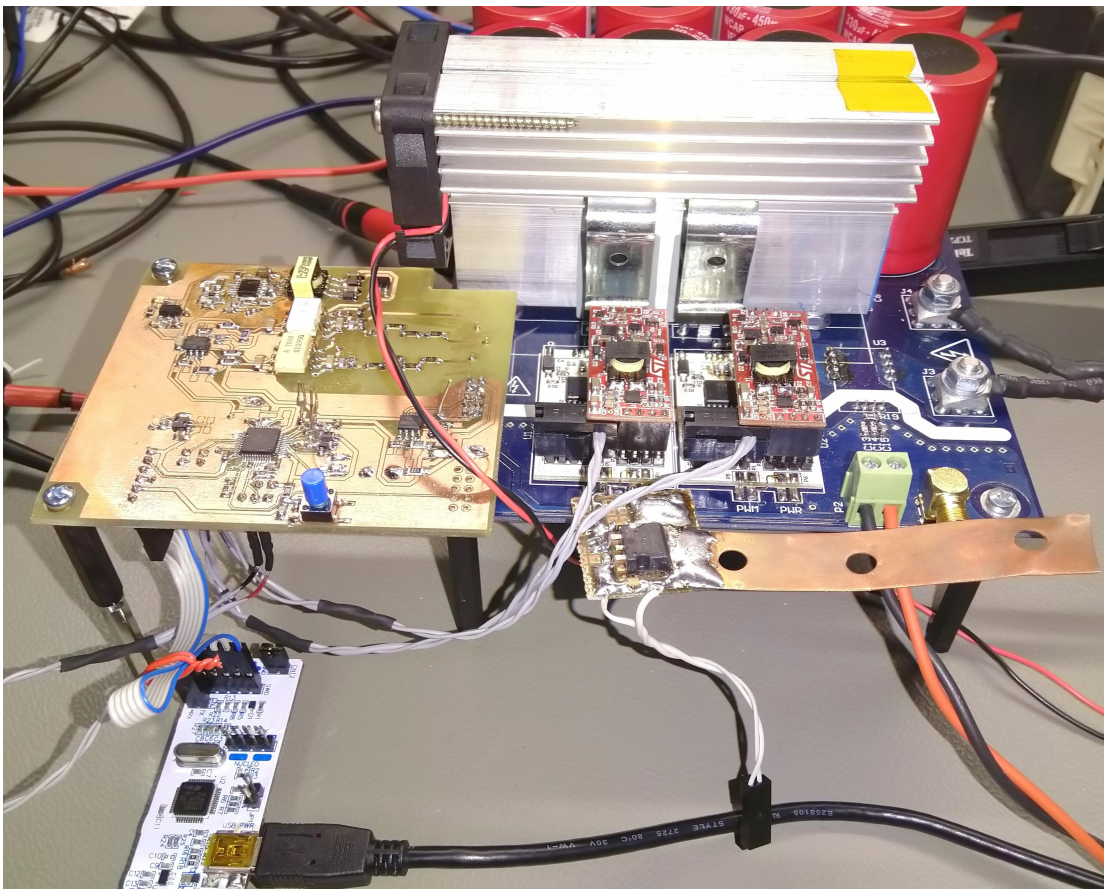


Figure 105 Photo of the power converter driven by the control unit prototype

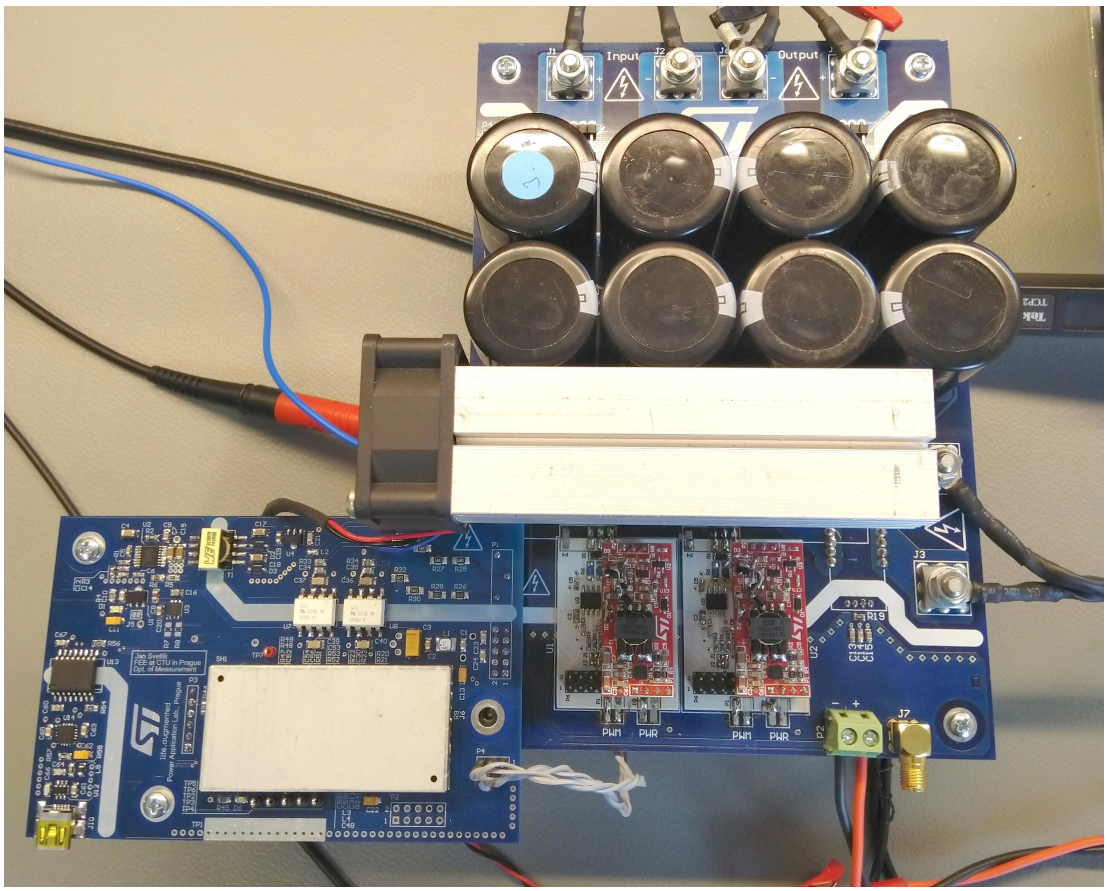


Figure 106 Photo of the power converter driven by the control unit

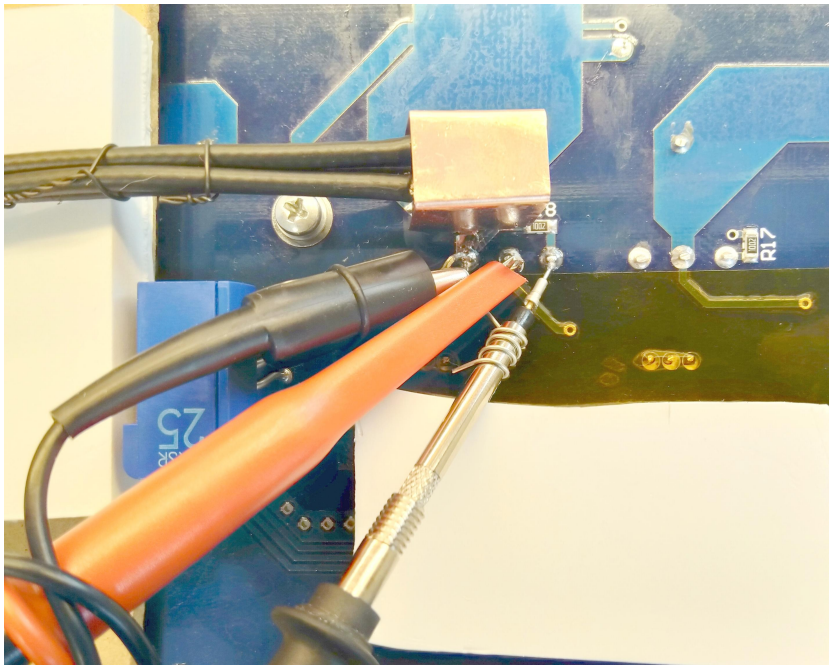


Figure 107 Photo of the probe placement used for the measurement and waveform acquisition of switching transients

Appendix D

Control unit frontend

The control unit communicates with a host PC over an emulated serial line as described in chapter 5. The control unit provides a simple terminal-based user interface (TUI) for configuration as well as for displaying an actual state of the converter. This attachment contains a description of the control unit frontend.

D.1 Control unit frontend overview

This section provides information about the control unit setup and usage. A detailed description of the control unit TUI is provided.

D.1.1 Setting up the communication

The control unit communicates with the host PC over an emulated virtual COM port provided by the FTDI USB to UART converter. For Linux users, the setup does not require installation of any drivers, since the drivers for the FTDI converters are a part of the Linux operating system. In the case of the Windows, the drivers for the USB to UART converter has to be installed before the use of the control unit. For the detailed description of the driver installation see [39].

Parameter	**Value**
Baud rate	115200 *Bdps*
Start bits	1
Stop bits	1
Parity check	none
Data bits	8

Table 19 COM settings used for the control unit communication

Tab. 19 summarizes the settings of the COM port used to communicate with the control unit.

The control unit TUI uses box-drawing characters to create a simple user interface. The characters sent over the COM port are eight bit long. Hence a font that allows for box drawing characters in an extended ASCII character table should be used, so the TUI screen is displayed correctly. In case the host PC is running Linux operating system, only the terminal character translation has to be switched to Cyrillic IBM855. In the case of the Windows, the box drawing characters are provided by a Terminal font. Hence the user should change the font in a currently used terminal emulator to the Terminal. Some applications, for example, Putty requires to switch translation to use font encoding to display the TUI of the control unit correctly.

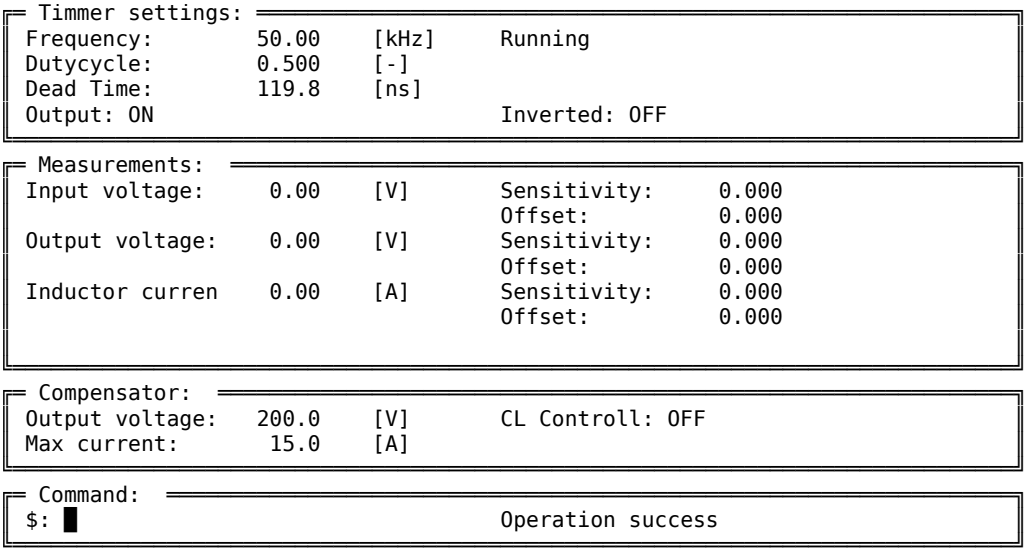


Figure 108 The main screen of the terminal user interface of the control unit

D.1.2 Terminal user interface description

The TUI consists of the main screen which can be seen in Fig. 108 and a help screen. The main screen is made up of four sections. The first section shows the basic settings of the control unit. It informs the user about the actual state of the control unit. In the left column, actual values of output signal frequency, dead time, and duty cycle are shown. The control unit state is displayed in the right upper corner. The last line of the first section informs about the output state and whether the output signals are swapped or not.

The second section relates to the output voltage, input voltage, and inductor current measurement. As described in chapter 5, a cycle mean value of the mentioned quantities is displayed. The value displayed is in its original scale as provided by the control unit calibration and correction mechanism. The current version of the control unit firmware shows the calibration values of each measurement chain.

The third section relates to closed loop settings. The left column displays actual parameters of the compensator in term of the maximum inductor current for the current mode control and the preset output voltage in constant voltage regulation. The closed-loop regulation status is displayed in the right column.

The last section belongs to the control unit command prompt. The command prompt itself provides information about the status of the previously executed command. If the control unit shows the main screen, the command prompt is active, and any command can be executed by typing in the command string, including its arguments and pressing enter.

In case a help command is issued, a help screen with the requested information is shown. In such a case, the command prompt is inactive, and the control unit does not accept any command. The help screen is closed by pressing enter.

D.2 Control unit operation

At the start-up, the control unit performs a short self-calibrating sequence that allows compensation of a part of the current measurement chain as described in chapter 3. After the startup, the control unit is in an idle state and is ready to accept commands

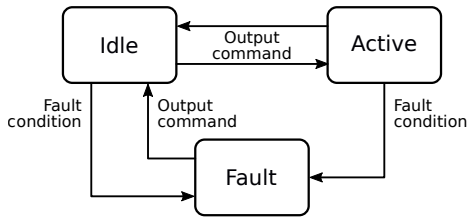


Figure 109 The control unit operation states

via its command prompt.

The control unit can be in one of the three states — Idle, Active, or Fault.

Idle: This state is the default state. It occurs in case the output signals are deactivated, and no fault condition occurred. The control unit can be switched to its active state by issuing output command which activates the output signal with parameters reported by the control unit.

Active: This state reports that the output signals of the control unit are activated. The control unit can be switched to the idle state by issuing the output command, which also deactivates the output signals.

Fault: This state cannot be reached by any command. The control unit is switched into the fault state in any case of failure and latches in it. During the transition from the active state into the fault state, the output signals are shut down. The fault state can be reached from both, the active and the idle state. The control unit can be switched to the idle state by executing output command only if the fault condition is removed. Otherwise, the control unit remains in the fault state. The fault state can be triggered by overcurrent or overvoltage protection.

Block diagram of the control unit states and possible transitions is shown in Fig. 109. By default, the control unit starts into the idle state and shows the main screen of the TUI.

D.3 Configuration commands supported by the control unit

The control unit can be configured using the terminal user interface by several sets of commands. There are several types of commands based on which functionality of the control unit is being configured. This section describes the set of commands supported by the firmware so far. A summary of all supported commands is provided in Tab. 20.

Each command is named by its primary function. Every numerical argument to the command is marked by an identifier in angle brackets, e.g., `<value>`. The name of the argument is used in the command description. Some commands provide more than one functionality. The functionality is selected by an argument switch. The list of switch values of the particular argument is separated by a backslash, e.g., `uin/uout/curr`. The switch may have only one value. Optional arguments to commands are listed in square brackets.

D.3.1 Output signals related settings

This section describes the set of the most basic commands used to configure the standard output signal properties.

Command	Short description
`f`	sets frequency of the output PWM signal
`d`	sets the duty cycle of the output PWM signal
`t`	sets the deadtime of the output signal
`o`	controls the state of the driving signals
`cal`	configures measurement calibration
`b`	sets the bias voltage for current measurement
`v`	sets output voltage for closed-loop control
`c`	sets maximum inductor current for closed-loop control
`cl`	toggles the closed-loop control of the converter
`r`	performs a restart of the control unit
`s`	redraws screen of the control unit
`h`	shows information about any command
`?`	shows basic information about the control unit

Table 20 Table with the summary of supported commands

Frequency: `f <value>`

The frequency command sets the frequency of the control signal to a `value` in kilohertz. The frequency can only be configured if the control signal outputs are in the inactive state. This command reconfigures the high-resolution timer to generate the PWM signal at the given frequency. However, as described in section 5.1, the high-resolution timer is capable of producing frequencies provided by the actual prescaler value and the value of the period register. As a consequence, the output frequency set by the control unit may not be the same as requested within the command. The actual frequency of the PWM signal that can be generated by the control unit is displayed on the terminal screen.

As soon as the output signal generation is enabled, this command does not allow to change the frequency and returns with *Output active* status.

Duty cycle: `d <value>`

The duty cycle command sets the duty cycle of the generated control signal. The `value` ranges from zero to one. The control unit displays the actual value of the duty cycle from a similar reason as in the case of the frequency command. The duty cycle can be configured even if the control signal generation is enabled to allow the converter open loop control during its operation. The duty cycle is limited in its range due to the high-resolution timer configuration requirements. If the value is out of the limit the command returns with *Dutycycle out of range* status.

In case the duty cycle is changed during the converter's operation, the duty cycle of the output signal is not altered stepwise, but a sweep sequence with a fixed slope is started. The sweep of the PWM duty cycle instead of abrupt change prevents a high current spike that would occur due to an output capacitor bank being charged. If the duty cycle is changed during the sweep sequence, the control unit returns *Quantity is sweeping*. This condition remains until the sweep sequence is done.

Dead time: `t <value>`

The deadtime command configures the dead time being inserted into the control signal to the `value`, which is in nanoseconds. As well as the frequency, the dead time can only be set when the control unit is in the idle state. The dead time can be

configured in discrete time steps given by the deadtime generator configuration as describe in section 5.1.4. As a result, the actual dead time of the generated control signal may not be the same as the required value. The current value that was found to be valid by the configuration algorithm is displayed in the terminal interface.

When the output signals are activated, it is no longer possible to change the deadtime. In such a case, the *Output active* state is returned by the control unit.

Output: `o [i]`

The output command enables the control signal generation in case the output was previously disabled. Conversely, if the output is active, the same command makes the control unit to disable the signal generation. If the `i` option is given to the command, the control signals are swapped. This action can be done only when the output is inactive. This feature allows swapping the signals for the high-side and the low-side transistor without the need for reconnecting signal cables.

In case the control unit is configured in open loop control, a sweep sequence is applied to the output signal when the output is activated. This procedure is done to prevent any high current that could occur due to discharged output capacitors. If the control unit operates in the closed loop mode, the compensator algorithm takes over the duty cycle control.

D.3.2 Current and voltage sensing related settings

This section focuses on a description of configuration commands related to the input voltage, output voltage, and current sensing.

Calibration: `cal uin/uout/curr s/o <value>`

The calibration command allows setting the calibration values for the input voltage, output voltage, or the current sensing measurement. The first argument is a switch that selects the measurement chain of which the calibration is being configured. The possible values of the switch are

`uin`	input voltage measurement transfer function
`uout`	output voltage measurement transfer function
`curr`	current sensing transfer function

It is possible to set the values of the offset and the sensitivity for both the output and the input voltage sensing paths. The selection of the sensitivity or the offset is provided by the second argument switch which has the following values

`o`	transfer function offset
`s`	transfer function sensitivity

In the case of the current measurement, only the sensitivity is provided as the offset is a part of the control unit self-calibration process. Hence, in case of the `curr` switch is selected, only the `s` switch is available. The `value` is in the base units of the selected parameter.

The calibration values can only be configured when the control unit is idle. If the command is issued when the control signals are activated, *Output active* status is returned.

Bias voltage: `b <value>`

The bias command allows configuring the bias voltage applied for the current sensing chain. The value is in volts and corresponds to the voltage produced by the DAC output used to bias the current measurement chain. The bias voltage can only be set during the control unit idle state when the output signal is deactivated. Attention must be paid not to disrupt the ability of the control unit to measure the inductor current. Setting the inappropriate value to the current hardware setup can lead to a current measurement distortion and can impact the closed loop regulation.

If the bias voltage is changed when the output signal is enabled, the bias voltage remains unaffected and *Output active* status is returned.

D.3.3 Closed loop control related settings

The control unit supports a few basic commands for configuring the closed loop regulation parameters. These parameters are the desired output voltage in constant voltage regulation and the maximum mean value of the inductor current that implies the maximum output current in steady state operation.

Output voltage: `v <value>`

The output voltage command sets the reference for the closed-loop regulation of the output voltage. The `value` is in volts and is appropriately scaled and transferred into the compensator reference value. If the converter is configured to operate in open loop mode and a new value of the output voltage is set, the preset value is saved, but the actual converter state is not affected.

As soon as the closed loop operation is turned on, and the output is set active, the preset voltage value is taken into account. The desired value of the output voltage can be changed at any time even during the converter is running, and the control unit is in the closed loop mode.

Inductor current: `c <value>`

The current command sets the maximum cycle mean value of the inductor current. The `value` is in amperes and is appropriately scaled and transferred into the saturation limits for the output of the voltage control loop. If the output load is too high that the current limit is reached or if the output load is of constant voltage character and the preset output voltage is higher than the load voltage, the controller enters the current limit and operates in constant current mode. The maximum value of the inductor current mean value can be set at any time even if the converter is working. If the control unit is configured in open loop mode, the new value of the maximum current is saved, but the current state of the converter is not influenced.

Control selection: `cl`

The closed loop command toggles between the closed loop and the open loop operation of the control unit. If the control unit operates in the open loop mode, this command switches the operation into the closed loop mode and vice versa. The control selection command can only be issued when the output is inactive for safety reasons. If the output is active and the closed loop command is issued, no action is performed, and the *Output active* status is returned.

D.3.4 Miscellaneous commands

The control unit also supports commands for redrawing the screen of the terminal user interface, restarting the control unit, or printing information about supported commands.

Restart: `r`

The restart command turns off the control signal output and performs the restart of the microcontroller. As a consequence, the control unit will boot into its default state with predefined settings. This command can be used for restarting the control unit in case of any unhandled error or failure.

Refresh screen: `s`

The refresh command redraws the terminal user interface in case the communication error occurred. The refresh command can be issued at any time and under any configuration of the control unit as it does not influence the current operation state. The refresh command clears the terminal screen and redraws the TUI without the need of the control unit restart. This action can be used when communication was interrupted, or a terminal emulator was restarted on the host PC.

Help: `h [<command>]`

The help command provides necessary information about the available commands. If the help command is executed without any argument, a list with all accessible commands is shown. The list of all supported commands contains a brief description of every command. The help command takes one optional argument, which is a string corresponding to any control unit command.

If the command string is passed to the help command, a detailed description of the command is provided. However, the command description available in the control unit is limited as it consumes the microcontroller flash memory. Hence, the information provided by the help command is not as detailed as in this reference manual.

About: `?`

The command provides brief information about the control unit firmware version and the usage of the control unit.

Appendix E

Contents of the attached CD

This section includes the contents of the CD attached to the thesis.

`calculations/`

This folder contains some Libre Office Calc sheets used for design calculations of the control unit.

`control_unit/`

This folder contains firmware of the control unit. A precompiled binary file of the latest firmware is included as well as source codes with the GIT repository. The GIT repository contains the whole version control history.

`datasheets/`

The datasheets of key components are included in this folder.

`materials/`

Additional materials such as reference manuals or application notes are provided in this folder.

`measurements/`

This folder contains an oscilloscope screen captures of all tests performed on the power converter. There are waveforms of the converter closed-loop control step response and measurements of the transient behavior of the power MOSFETs.

`photo/`

This folder contains some additional images of the control unit and the power converter that were too big to be included in the text.

`python_scripts/`

All python scripts used for data processing and simulations are included in this folder.

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