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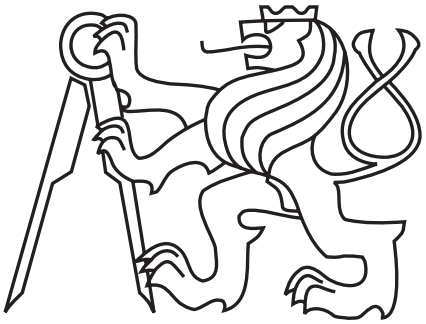

Doctoral Thesis

Analog Circuits for DC-DC Converters

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Analog Circuits for DC-DC converters

by

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Abstract

DC-DC converter are essential part in a whole range of applications. With the continuous integration and demand for higher efficiency more strict requirements are put on various circuits that make up the converter. The thesis pursues three circuit areas, current sensors, oscillators, zero crossing and overcurrent detectors.

Current sensors are used for overcurrent protection, regulation and in case of multiphase converters for balancing. A new high voltage current sensor for coil-based current sensing in DC-DC converters is presented. The sensor employs DDCC with high voltage input stage and gain trimming. The circuit has been simulated and implemented in 0.35 μm BCD technology as part of a multiphase DC-DC converter where its function has been verified. The circuit is able to sustain common mode voltage on the input up to 40 V while it occupies 0.387×0.345 mm^2.

In the second part, a function generator generating both square and triangle waveforms suitable for DC-DC converters is proposed. The generator employs only one low area comparator with accurate hysteresis set by a bias current and a resistor. Oscillation frequency and its non-idealities are analyzed. The function of the proposed circuit is demonstrated on a design of 1 MHz oscillator in STMicroelectronics 180 nm BCD technology. The designed circuit is thoroughly simulated including trimming evaluation. It consumes 4.1 μA at 1.8 V and takes 0.0126 mm^2 of silicon area. The temperature variation from $-40\,^{\circ}$C to $125\,^{\circ}$C is ± 1.5 % and the temperature coefficient is 127 ppm/$^{\circ}$C.

In the third part, a dual purpose over-current (OCD) and zero crossing detector (ZCD) for high voltage switching DC-DC battery chargers is presented. As in both buck and boost operation modes the current is sensed on high side power transistor it is possible to reuse the detection circuit which inherently saves silicon area. The circuit was designed in STMicroelectronics 0.18 μm BCD technology and occupies only 0.035 mm^2 while consuming 1.2 mW operating from 12 V power supply. The correct operation of the circuit was verified on silicon as part of a dual-phase battery charger.

The last presented circuit is an overcurrent detector with built-in reference and programmable threshold. It features a built-in detection threshold set by a V_{GS} of a MOS transistor and a resistor value R. The main benefits of this solution are lack of kickback noise on reference bias line, low power operation – consumes only when sensing current, high speed, and small area. All these properties are essential for ultra-low power converters. The circuit was designed in the same 0.18 μm BCD technology and its operation was verified on silicon. It occupies 0.011 mm^2 and consumes 16 µA static current (at zero inductor current).

Keywords: DC-DC converter, current sensor, oscillator, comparator

Abstrakt

DC-DC měniče jsou nepostradatelnou součástí řady aplikací. Vzhledem k neustálé integraci a požadavkům na vyšší účinnost jsou kladeny stále vyšší nároky na vnitřní obvody těchto měničů. Tato dizertační práce se zabývá třemi oblastmi: proudovými senzory, oscilátory, komparátory průchodu nulou a nadproudovými komparátory.

Proudové senzory se využívají pro nadproudovou ochranu, regulaci a v případě vícefázových měničů pro balancování fází. Nový vysokonapěťový proudový senzor pro měření proudu cívkou v DC-DC měničích je představen. Senzor využívá DDCC proudový konvejor s vysokonapěťovými vstupy a kalibrovatelným ziskem. Obvod byl simulován a implementován v 0.35 μm BCD technologii jako součást vícefázového DC-DC měniče, v rámci něhož byla jeho funkce ověřena. Obvod vydrží na vstupu souhlasné napětí až 40 V a zabírá na chipu 0.387×0.345 mm^2.

Ve druhé části je představen funkční generátor generující trojúhelníkový i obdélníkový signál vhodný pro DC-DC měniče. Generátor využívá jeden komparátor optimalizovaný na plochu s hysterezí nastavitelnou proudem a odporem. Výstupní frekvence a její závislosti jsou zanalyzovány. Funkční generátor s frekvencí 1 MHz je navržen v 180 nm BCD technologii společnosti STMicroelectronics. Funkce obvodu je doložena simulacemi včetně kalibrace. Teplotní variace frekvence od $-40\,^{\circ}$C do $125\,^{\circ}$C je ± 1.5 % a teplotní koeficient je 127 ppm/$^{\circ}$C.

Ve třetí části je prezentován kombinovaný nadproudový detektor (OCD) a detektor průchodu nulou (ZCD) pro vysokonapěťové spínané měniče pro nabíjení baterií. Jelikož oba detektory v buck i boost módu snímají proud na výkonovém tranzistoru připojeném ke stejnému vstupnímu, resp. výstupnímu uzlu, je možné oba dva detektory sloučit do jednoho pro ušetření plochy na chipu. Obvod byl navržen rovněž v 180 nm BCD technologii, zabírá plochu 0.035 mm^2 a spotřebuje 1.2 mW při 12 V napájecím napětí. Obvod byl vyroben jako součást dvoufázového obvodu pro nabíjení baterií a jeho funkce byla ověřena měřením.

Posledním prezentovaným obvoden je nadproudový detektor s vestavěnou referencí a programovatelným detekčním limitem nastaveným pomocí V_{GS} napětí MOS tranzistoru a rezistoru R. Hlavními výhodami tohoto řešení je absence rušení do reference, nízký odběr, vysoká rychlost a malá plocha. Všechny tyto vlastnosti jsou nutné v měničích s velice nízkou spotřebou. Obvod byl navržen ve stejné 180 nm BCD technologii a jeho funkce byla ověřena měřením. Obvod zabírá 0.011 mm^2 na chipu a má statickou spotřebu 16 µA (při nulovém proudu cívkou).

Klíčová slova: DC-DC měnič, proudový senzor, oscilátor, komparátor

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My greatest thank belongs to Jiří Hospodka who supervised the thesis, gave me advice and always encouraged me to continue and pursue the studies.

Most importantly, I would like to thank my family for support they are giving me for all my life.

I hereby declare that I have created this thesis on my own and exclusively using literature presented in the references. I agree with lending and publishing this work or its parts.

February 21, 2018 Martin Dřínovský

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Symbols and Abbreviations

ASIC	Application specific integrated circuits.
BCD	Bipolar, CMOS, DMOS (technology).
BJT	Bipolar junction transistor.
CCM	Continuous conduction mode.
CCII	Current conveyor, second generation.
C_{gd}	MOS gate-drain capacitance.
C_{gs}	MOS gate-source capacitance.
COB	Chip on board.
C_{ox}	MOS gate oxide capacitance per unit area.
CMC	Current mode control.
D	Duty cycle.
DAC	Digital to analog converter.
DCR	DC resistance (of inductor).
DCM	Discontinuous conduction mode.
DDCC	Differential difference current conveyor.
DMD	Discontinuous mode detector (synonym to ZCD).
DMOS	Double diffused MOS (MOS transistor structure to support high voltages).
EMI	Electromagnetic interference.
HS	(Referred to) low-side (switching inductor to input of output).
HV	High voltage.
LDO	Low drop-out regulator.
LS	(Referred to) low-side (switching inductor to ground).
LX	Inductor switched node.
MC	Monte Carlo (analysis).
MOS	Metal-oxide-semiconductor transistor.
OCD	Overcurrent detector.
OCP	Overcurrent protection (same as OCD).
OTA	Operational transconductance amplifier.
PCB	Printed circuit board.
PFM	Pulse frequency modulation.
PMIC	Power management integrated circuits.
PSR(R)	Power supply rejection (ratio).
PVT	Process, voltage, temperature (variations).
PWM	Pulse width modulation.
R_{dson}	MOS on-state drain-source resistance.
SMPS	Switch mode power supply.
t_{pd}	Propagation delay.
USB	Universal serial bus.
U_T	Thermal voltage kT/q.
V_{GS}	MOS gate-source voltage.
V_T	MOS threshold voltage.
VMC	Voltage mode control.
ZCD	Zero crossing detector.
η	Power efficiency.
μ	MOS carrier mobility.

1 Introduction

Since the advent of electronic circuits, one of the problems was how to supply them with the necessary voltage for their correct operation either from a battery or AC power grid. At the beginning, electromechanical relays and vibrators were used to generate high voltages to supply vacuum tubes. With the invention of transistors circuits capable of generating higher voltages (such as [1]) started to emerge as well as various discrete linear voltage regulators. But it was as late as 1967 when Bob Widlar (Fairchild) designed the first integrated voltage regulator μA723 [2] one of whose applications include a switching regulator. Nowadays voltage regulators, be it linear or switching, are an important class of integrated circuits and are present in portfolios of every major semiconductor manufacturer.

The increasingly complex systems, such as computers, mobile phones or tablets, can utilize tens of switching and linear regulators not only to power different voltage domains but also to isolate different subsystems and guarantee one doesn't influence the other. To save price and area these regulators are usually grouped in complex power management integrated circuits (PMIC) often made as application specific integrated circuits (ASIC) tailored to a specific application for a specific customer.

1.1 Linear voltage regulators

Linear voltage regulators convert higher input voltage to a lower output voltage (in absolute values, can be utilized for both positive and negative supply lines). Block diagram can be seen in Fig. 1.1a. The voltage difference (drop-out) $V_{\mathrm{IN}} - V_{\mathrm{OUT}}$ is spent on a power transistor M_{PASS}, which can be either MOS of BJT. The regulating element (operational amplifier) then controls the gate voltage of the power transistor in such a way that the feedback voltage generated by the feedback divider[1] is equal to the reference voltage. Then the output voltage is

$$V_{\mathrm{OUT}} = V_{\mathrm{REF}} \left(1 + \frac{R_1}{R_2}\right). \tag{1.1}$$

The feedback resistors can be both external or internal to the chip. The latter case is often used in high volume systems where every external component adds non-negligible cost to the manufacturer. In that case the voltage version is hardwired or preprogrammed in the chip or, as in the case of PMICs, can be programmed directly in application using some configuration protocol.

Although using N channel pass transistor has its benefits (better PSR, wider range of acceptable output capacitors) the drawback is high drop-out (needs at least V_{GS} higher input supply voltage) around 1 V. To overcome this, the so called low drop-out (LDO) regulators (Fig. 1.1b) use P channel pass transistor which can reach drop-outs below 100 mV.

The advantages of linear regulators include clean, low-noise output, regulation accuracy, good power supply rejection (PSR) or simplicity (low silicon area $\rightarrow$ cost). However, the major drawback of linear regulators is the power efficiency given as (neglecting quiescent

[1] Sometimes the feedback divider is not present and the regulator regulates directly to V_{REF}, this configuration is used for example in low-noise regulators.

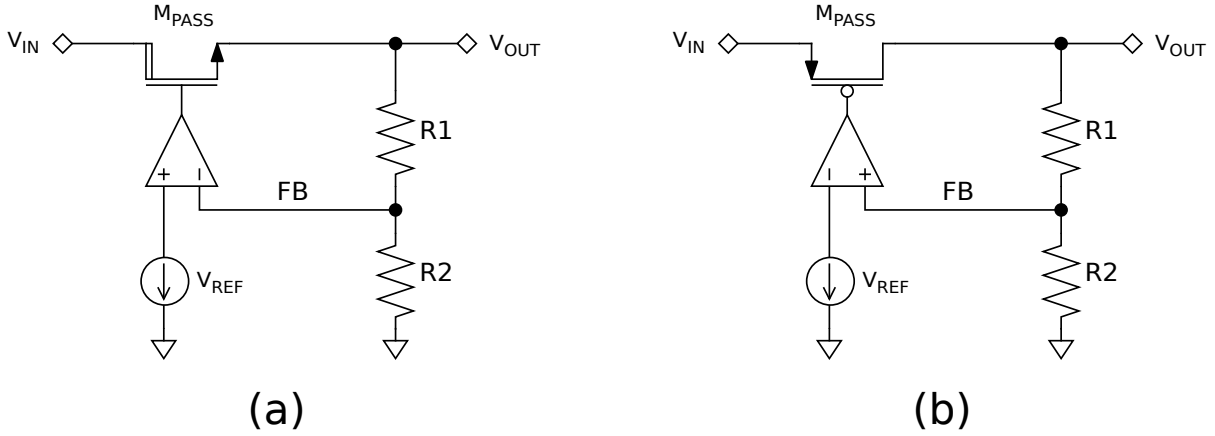


Figure 1.1: Block diagram of linear voltage regulators: (a) conventional, (b) low drop-out.

current of the regulator)

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}}. \tag{1.2}$$

This is a major drawback for a lot of systems, e.g. battery operated devices, and contributed for the fast development and adoption of switching mode power supplies.

1.2 Switching converters

Switching converters, also known as switch mode power supplies (SMPS) or DC-DC converters, use either capacitors[2] or inductors (or transformers) to convey energy between input and output. From an input voltage switching converters can generate lower output voltage and unlike linear regulators some topologies can generate higher output voltage or even negative output voltage. The major advantage of switching converters is their high efficiency (can be higher than 90%) due to which they find place not only in high power applications but also in low power ones, especially battery operated devices, where they complement or even replace previously used linear regulators On the other hand, disadvantages include output ripple, higher noise, lower regulation accuracy and cost (due to the higher complexity of the regulator and the higher component count).

There exist numerous non-isolated (use inductors) and isolated (use transformers) topologies and it is beyond the scope of this thesis to go into detail of all of them. Nevertheless, two of the most important topologies are briefly described next. Curious reader can find detailed analysis of various converters e.g. in [3].

Buck converter

One of the simplest switching converter topology is the buck converter as depicted in Fig. 1.2a. The energy transfer element is the inductor L whose one pole (the associated node is usually named LX, SW or phase) is switched between input voltage and ground using two switches, here represented by two transistors, high-side M_{HS} and low-side M_{LS}.

[2]Due to the focus of the thesis capacitor based DC-DC converters are not further described.

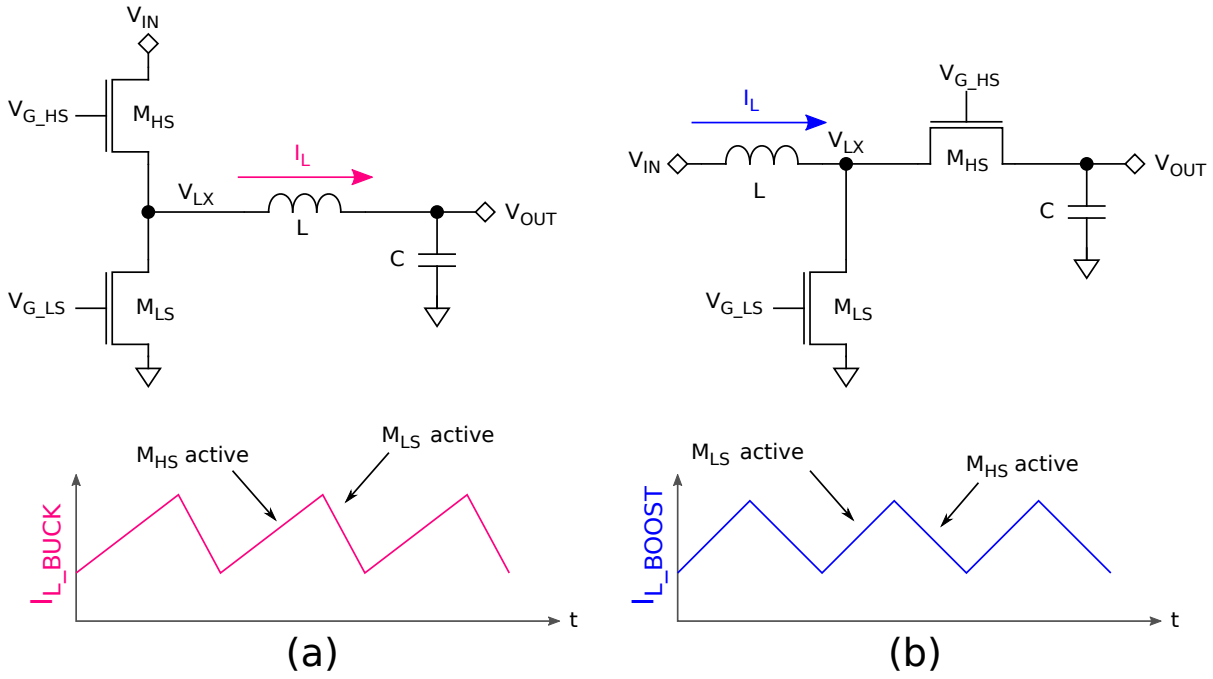


Figure 1.2: Topologies of SMPS converters: (a) buck , (b) boost.

The high-side transistor can be both P-channel or N-channel MOS. While NMOS is preferred for its lower on-state resistance (R_{dson}) it requires gate voltage higher than V_{IN} to turn-on. Although there exist methods to overcome this limitation (e.g. using bootstrap capacitor to power the high-side driver) they incur additional area and cost to the system, therefore a PMOS is usually used in place of M_{HS}. For low-side switch an NMOS is usually used.

To describe the operation of the buck converter let's assume that $V_{OUT} < V_{IN}$. When M_{HS} is active the constant voltage across the inductor (assuming ideal case, i.e. neglecting all switch and coil resistances and ripple on V_{OUT}) causes the inductor current to linearly increase with slope $(V_{IN} - V_{OUT})/L$. This phase is usually called the active phase or on phase and the duration in one period is denoted t_{ON}. When M_{LS} is active the switching node LX is tied to ground and the negative voltage across the inductor causes the current to decrease with slope V_{OUT}/L. This duration of this phase is usually denoted t_{OFF}.

In both phases the inductor current is flowing to the output and thus the average value of the inductor current is equal to the load current. The value of the output voltage is given by[3]

$$V_{OUT} = DV_{IN}, \tag{1.3}$$

where D is the duty cycle, i.e. the ratio of t_{ON} and the switching period T. The output voltage of the buck converter is therefore always $V_{OUT} \leq V_{IN}$. When the input voltage V_{IN} drops below requested output voltage the high-side switch gets turned-on for the whole period, this mode is usually called bypass mode.

[3] Assuming continuous conduction mode (CCM), see next.

Boost converter

In contrast to buck converter which generates V_{OUT} less than V_{IN}, the boost converter always generates output voltage higher than the input one. This topology is depicted in Fig. 1.2b. This time the inductor is connected on the input and its second pole is switched between ground and V_{OUT} again using two switches.

The low-side switch is realized using NMOS transistor and for the high side switch again both NMOS and PMOS can be used. However, when the generated output voltage is high it may become impractical to use integrated on-chip transistor (the higher the required voltage capability, the larger the area the transistor occupies). In this case a shottky diode is used in place of $\mathrm{M_{HS}}$.

The active phase starts when $\mathrm{M_{LS}}$ is active. The voltage across the inductor is V_{IN} and the inductor current increases with slope V_{IN}/L. In the second phase, $\mathrm{M_{HS}}$ is active instead and the inductor current discharges into the output capacitor and the load, dropping at a rate $(V_{\mathrm{OUT}} - V_{\mathrm{IN}})/L$.

The output voltage is then given as (again assuming ideal case and CCM operation)

$$V_{\mathrm{OUT}} = \frac{1}{1-D} V_{\mathrm{IN}}. \tag{1.4}$$

1.3 Anatomy of switching converters

The switching converters is a very broad topic and it is beyond the scope of this thesis to cover it entirely, thus only an example of what a typical buck converter is composed of is given. A block diagram of such a converter is in Fig. 1.3. The detailed study of each IP would take a book to cover, thus only a brief summary with the most important parameters is given.

Power MOSFETs

A feasibility study of every switching converter design starts with estimation of power transistors that make the switching half-bridge, i.e. $\mathrm{M_{HS}}$ and $\mathrm{M_{LS}}$. These transistors usually consume the largest silicon are of all blocks and directly impact efficiency both at high load and low load conditions.

At high load currents the converter losses are dominated by conduction (ohmic) losses due to (but not only) on-state resistance of the power transistors. The respective power losses for the buck converter are

$$P_{\mathrm{LS}} = (1-D) R_{\mathrm{LS}} \left(I_{\mathrm{load}}^2 + \frac{\Delta I_L^2}{12} \right), \tag{1.5}$$

$$P_{\mathrm{HS}} = D R_{\mathrm{HS}} \left(I_{\mathrm{load}}^2 + \frac{\Delta I_L^2}{12} \right), \tag{1.6}$$

where I_{load} is the load current, ΔI_L is the peak-to-peak ripple of the coil current and R_{LS} and R_{HS} are on-state resistance of the low-side and high-side power paths, respectively. The last two include not only the on-state resistance of the power transistors themselves but they include also the metalization up to the pin of the device. Significant layout effort is put to

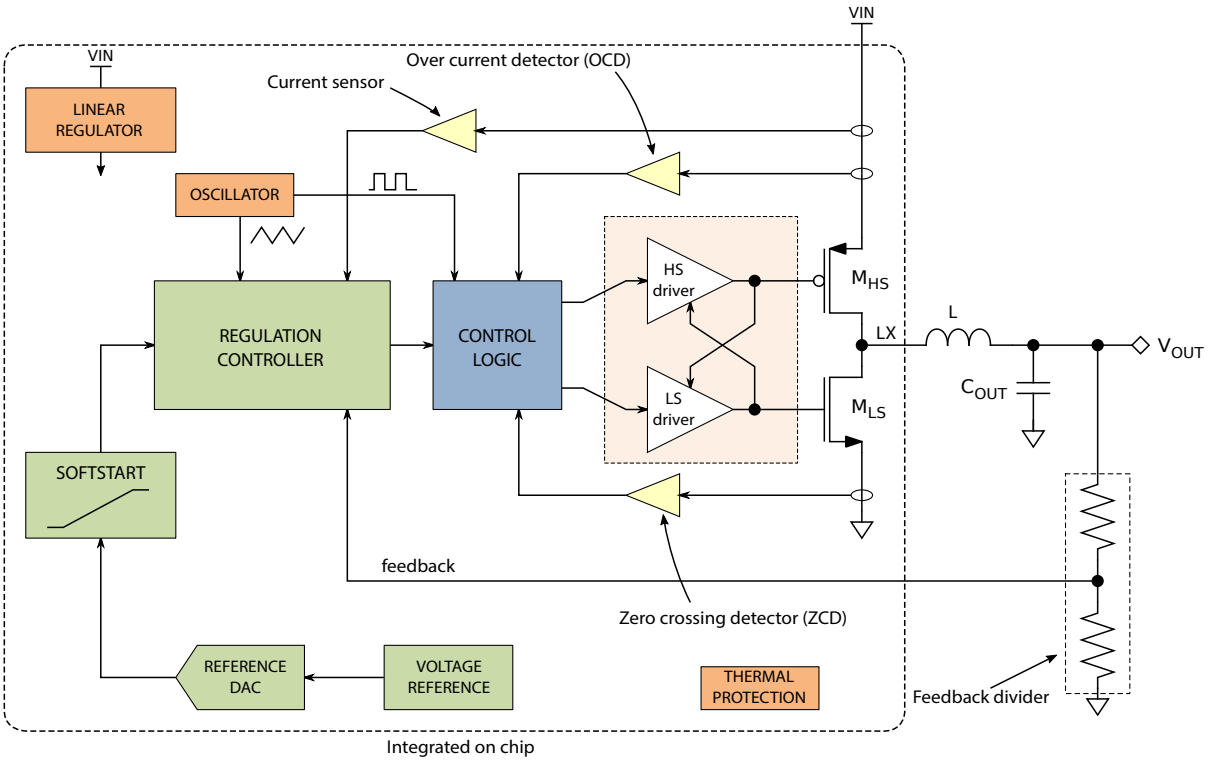


Figure 1.3: Block diagram of buck converter.

minimize the effect of metals and it is common to use special software for mesh analysis [4].

At low load currents the efficiency is limited by switching losses that linearly scale with switching frequency. The power transistor switching losses are caused by body diode conduction or by charging gate, gate-drain and drain capacitances. These effects scale with transistor size, there is therefore trade-off in power MOS size selection between conduction and switching losses.

To alleviate the switching losses one can divide the power transistor and turn-on only a fraction at light loads (one such a circuit is presented in [5]). The most common solution is, however, to scale down the switching frequency. This mode of operation is usually called pulse-skipping or pulse frequency modulation (PFM) mode.

The body diode conduction happens when there is a gap between one transistor switching off and the other on. During this time the coil tries to maintains its current and pushes the LX node below ground (or above V_{IN} in case of negative current, see ZCD) turning on the body diode of M_{LS}. Depending on particular technology process, this may turn on lateral or vertical parasitic BJTs and cause e.g. increased consumption or substrate injection deteriorating analog circuit performance. For this reason the analog circuit on the same die should have high substrate rejection ratio. To alleviate these problems it is sometimes necessary to put a barrier around the power transistors[4] which further increases the area of the power section.

[4]The problematic and type of such barriers is dependent on a particular technology at hand and is out of scope of this thesis.

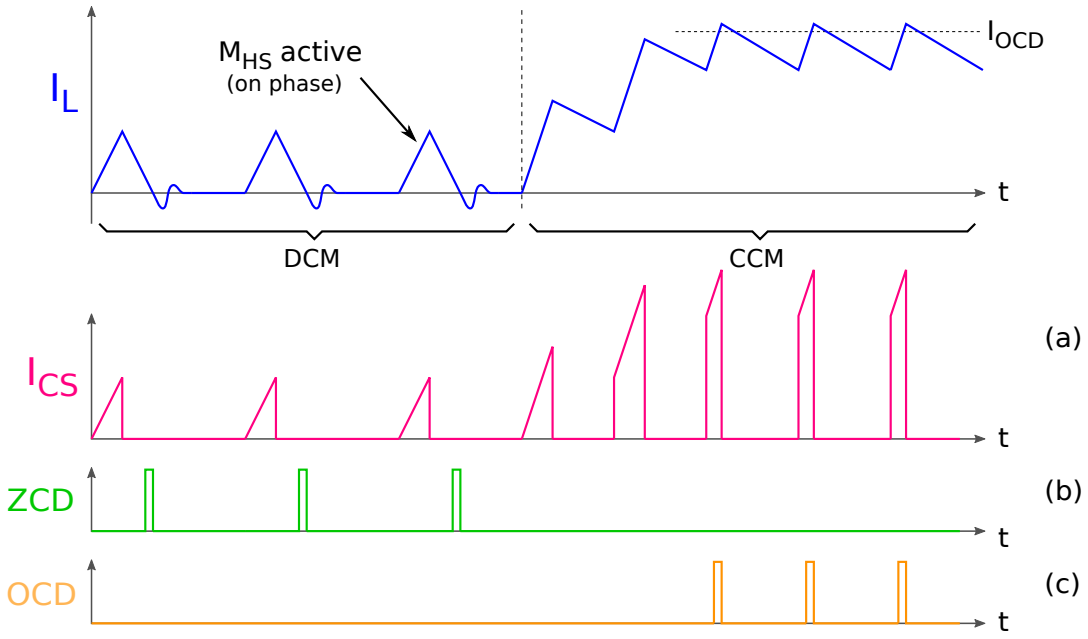


Figure 1.4: Inductor current waveform along with (a) current sensor (on phase sensing), (b) ZCD and (c) OCD outputs (not to scale).

Drivers

As stated above, power MOS transistors tend to have a very large area and consequently large gate-source C_{gs} and gate-drain C_{gd} capacitances.

The power transistors thus require a strong driver capable of delivering enough current to the gates to turn the power transistors on and off in a very short amount of time (in the range of nanoseconds). Moreover, the driver must be able to keep the power MOS off during abrupt transitions on the switching node LX as these might accidentally pull the gate up (in case of NMOS) through the C_{gd} capacitance. On the other hand, the transitions initiated by the driver should not be too fast as these cause large voltage spikes on bond wires and PCB metal parasitic inductances and can cause poor EMI performance or even some component voltage breakdown.

Another problem that must be prevented is a cross conduction during switching transition both in the power transistors and the drivers. This is usually solved by using feedback from the gate of the other transistors into the driver (see cross coupled feedback in the drivers in Fig. 1.3) and blocking turn-on until the other transistor turns off.

Current sensor

Measuring inductor, input or output current is used in DC-DC converters for several purposes. Multi-phase converters use the values of its inductor currents to balance the load across its phases. USB powered battery chargers measure input current value to regulate and guarantee they do not take more than the predefined current from the input.

The most power demanding and predominant type of current sensor used in switching converters senses inductor current in on or off phase as depicted in Fig. 1.4a. Various regulation loop architectures, such as current control mode (see below), use the value of

inductor current in on phase or off phase to terminate that phase when the current reaches a particular value. On phase current sensor also sometimes precedes over-current protection circuit (see below). The power demand comes from the required speed of this type of sensor. Given that current consumer converters operate at switching frequencies above 1 MHz the on phase duration can be as low as 10 % of it, i.e. below 100 ns. Another important parameters include linearity, time required to stabilize upon turn on or input offset.

Zero crossing detector

When the converter is heavily loaded, the power stage alternates between low-side and high-side transistors creating a triangular inductor current waveform with an average value equal to output load current. This mode is called continuous conduction mode (CCM) and can be seen in Fig. 1.4. However, if the load dropped to a small value the inductor current would still maintain a triangular waveform but part of the waveform will be below zero. In the extreme case of a zero load the inductor current would ripple around zero. Although the converter would operates with no load it would still dissipate a lot of power due to the conduction and switching losses.

To overcome this adverse effect it is common to turn M_{LS} off just before the inductor current reverses polarity thus limiting it to positive values only. When this happens the converter is said to operate in a discontinuous conduction mode (DCM).

Historically, a shottky diode was used in place of M_{LS} and no control was necessary. With the need for higher efficiency power transistors are preferred and a dedicated sensor is needed to emulate the diode behavior.

The sensor that allows that is called zero crossing detector (ZCD), zero comparator (ZCOMP) or sometimes discontinuous mode detector (DMD). This comparator usually senses voltage drop on M_{LS} (in buck M_{HS} in boost) and triggers on zero crossing as depicted in Fig. 1.4b. Although the ZCD is supposed to trigger at zero current setting some small threshold even for zero crossing detection allows to compensate for the delay of the system between the crossing of the threshold and the actual turning off of the power MOS. This early ZCD trigger incurs less power dissipation than letting the coil current reverse direction [6]. The comparator threshold should be therefore set as

$$V_{\mathrm{ZCD}} = -R_{\mathrm{dson}} \frac{V_{\mathrm{OUT}}}{L} t_{\mathrm{dly}}, \tag{1.7}$$

where R_{dson} is the on-state resistance of M_{LS}, and t_{dly} is the system's delay which comprises of ZCD, control logic and drivers delay. However, when the load is small the positive peak of the inductor current can be small and the time it takes to reach the zero can be smaller than t_{dly}. Hence, it is necessary to minimize t_{dly} and consequently the delay of the ZCD itself which leads to high current consumption of this block. Another important factors are input offset voltage or start-up time.

Over current detector

When the converter gets overloaded or the output is even shorted the current in the inductor can get higher than what is safe for correct operation of the circuit. To overcome this the converters feature a circuit called over current detector (OCD) or over-current protection (OCP).

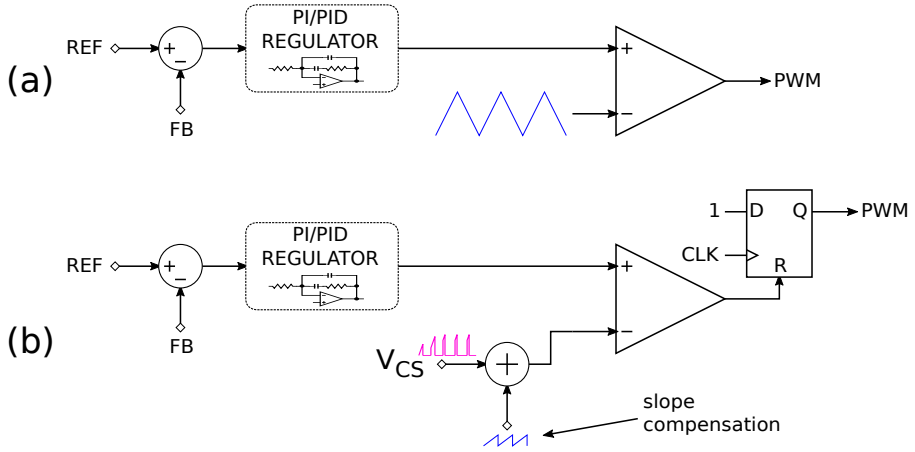


Figure 1.5: Control types: (a) Voltage mode control (VMC), (b) current mode control (CMC).

The common way to design such a protection is to stop the on phase (the one in which the current is increasing, M_{HS} in this case) once the inductor current crosses a predefined maximum value. This behavior can be seen in Fig. 1.4c. Depending on the design of the converter, the inductor current can be let discharged all the way to zero before a new cycle is started or the whole converter can be shut down. The latter case is called hiccup mode, after some timeout the converter attempts to start again.

The most important parameter for such a comparator is propagation delay, but unlike ZCD input offset voltage is not of the most importance since threshold is given as $V_{\mathrm{OCD}} = R_{\mathrm{dson}} I_{\mathrm{OCD}}$ and is in the range of hundreds of millivolts.

Regulation controller

There are many ways to control the switching converters, analog or digital, synchronous or asynchronous, etc. Two of the most common are described next.

Voltage mode control (VMC) is depicted in Fig. 1.5a. The difference between the reference voltage and the feedback taken from the (divided) output goes into an analog PID regulator (usually called error amplifier) whose output is then compared to a sawtooth or triangular waveform from an oscillator to produce a digital PWM signal to drive the switching of power transistors. The comparison to the periodic waveform makes the system periodic and as such must be analyzed. The triangular waveform is preferred for comparison as it crosses-samples the amplified error signal twice in a period allowing for a higher loop bandwidth [7].

In peak current mode control (CMC), depicted in Fig. 1.5b, the active phase (PWM=1) starts with a clock from the oscillator. The output of the current sensor is then compared to the amplified error and when it crosses the active phase is terminated. The output of the PID regulator is thus proportional to the peak current in the inductor. However, pure CMC suffers from subharmonic instability for duty cycles $> 50\%$. The common way to solve it is the so called slope compensation - superposing current sensor output with a ramp signal essentially combining CMC with a bit of VMC. Although CMC is more complex than VMC, it allows for simpler compensation and higher loop bandwidth.

In both cases the output of the PID regulator is clamped to fall within the bounds of the triangular waveform. If this protection was not implemented the amplified error would drift away when the converter is not in regulation (this can happen e.g. in bypass mode, when the output is overloaded or in no load conditions) and it would take time to slew back to the regulation region. This would produce overshoot or undershoot out the output.

Control logic

Control logic controls the behavior of the switching system. It gathers information from the regulation controller, ZCD, OCD and other parts of the systems and decides on the state of the system, whether to enter bypass mode, pulse-skipping or PFM mode and whether to switch low-side or high-side power transistors.Since it must react to immediate events it is implemented as asynchronous state machine, hand drawn from logic gates or synthesized from Simulink models.

Voltage reference and DAC

Every switching regulator contains a reference voltage generator - a bandgap reference. The output of the bandgap reference can be followed by a reference DAC which allows to set different output voltage settings. This method is preferred over changing feedback divider ratio as it changes also the loop gain and complicates compensation.

Softstart

If the converter started immediately with full voltage reference it would overshoot the desired output voltage and could damage the following circuitry. Also any short on the output would cause rapid inductor current build-up and potentially destruct the device. For this reason the reference voltage to the regulator and consequently the output voltage is slowly ramped up using a dedicated softstart block.

The softstart is usually implemented as charging a capacitor with a constant current or, if the reference DAC has high enough resolution, it can be done by ramping the digital value of the DAC.

Oscillator

Synchronous switching converter are usually synchronized by trimmed local oscillator. It must usually produce not only a digital waveform for control logic but also a sawtooth or triangular waveform depending on the type of the regulation controller.

In order to pass strict EMI rules frequency spreading can be implemented to reduce the peaks in the noise spectrum the converter generates. This can be implemented both in analog or in a digital way simply by changing the trimming bits of the oscillator by a pseudo random sequence.

Thermal protection

Since the integrated power transistors produce heat there is a risk of over-heating and potential destruction of the chip when it is not properly cooled. Every switching converter

therefore features thermal protection circuit which suspends operation when the temperature on the die reaches a certain threshold. Due to the relatively low thermal conductivity and large thermal time constants the temperature difference on the die can be over 10°C thus the thermal sensor should be placed as close to the power transistors as possible. For large SoC chips it is not uncommon to have several thermal sensors.

Linear regulator

Even though some switching converters already serve to generate low output voltage they need a way to power their internal circuitry from a high input voltage. For this reason a linear regulator can be present on the chip. It must have a good PSRR and substrate rejection ratio to not propagate the switching noise to the internal circuitry. If the consumption of the chip is high it deteriorates low load efficiency. In some cases the power supply of the internal circuits can then be switched to the output of the converter to take advantage of the better efficiency of the switching converter.

1.4 Thesis motivation

With the advent of portable consumer devices, such as smartphones, notebooks or smartwatches there has been continuous push for smaller (and thinner) and more power efficient application. The size constraints apply not only to ICs but also to the surrounding passive components, such as capacitors or inductors. In the context of switching converters, smaller capacitors are less capable to handle load variation which increases requirements on the reaction time of the switching converters and consequently on their switching frequency. However, higher switching frequency and smaller inductors in turn require faster analog circuitry inside the chip and therefore higher power.

Another trend to increase efficiency and cut down cost is to use higher supply voltage to deliver power to the application. This allows to use lower current and consequently thinner wires. One example, where this practice can be seen, is the charging of portable battery operated devices through USB using higher input voltage, such as USB Power Delivery [8] (up to 20 V) or Qualcomm Quick Charge (up to 22 V) standards.

The use of high voltages puts again emphasis on area of the blocks as they need to use special structures, such as DMOS transistors, to handle the high voltages[5], which take up a lot of silicon area.

The analog blocks which are affected the most by these demands are the ones which process the inductor current information as their requirements for speed scale with switching frequency. These blocks include current sensors, zero crossing and over current detectors. Moreover, the current information is usually sensed in high voltage domain (e.g. on high-side power transistor) which further complicates the design. One other block whose requirements scale with switching frequency is the oscillator. With the rest of the mentioned blocks it shares the same property of dealing with fast triangular signals and thus similar design techniques can be used.

As will be seen in the dedicated chapters, current solutions of these circuits often rely on standard structures and when facing requirements written above they take large area

[5] In the context of IC design, this usually means anything above the maximum allowable gate voltage, usually 5 V.

or power. This is especially true for non-standard applications which could benefit from dedicated new architectures.

1.5 Goals of the thesis

The goal of this thesis is to give an overview and outline design problems with the aforementioned blocks and contribute to development with regard to power, silicon area and high voltage capability requirements, especially for non-standard applications. These goals are:

Design high voltage bidirectional current sensor with off-chip inductor current sensing reducing area and need for special components. Standard solutions for off-chip sensing use operational amplifiers with both high voltage input and output. This complicates design because all the basic structures must be cascoded with high voltage components and consequently take a lot of silicon area. Moreover, bidirectional sensing is complicated and would load the sensing circuit.

Explore new architectures of triangle waveform generation for use in SMPS. With increasing demand for small form surface mount packages silicon area of every block can have an impact on whether the final design fits into the package or not. Standard solutions require two fast comparators or complex functional blocks consuming power and taking unnecessary silicon area.

Evaluate the possibility to combine OCD and ZCD functions for use in special combined converters, such as battery charging chips. Battery chargers combine buck and boost functionality in one circuit, both of which require overcurrent and zero crossing detectors. However, no combined OCD and ZCD solution has been presented so far. Having these functions in one IP would reduce area of the system, this is even more pronounced in multi-phase systems.

Find OCD solution mitigating reference kickback noise and slow startup. In ultra low power converters (quiescent current in the range of μA or less) the OCD circuit must be turned off when not immediately in use. The sudden switching on and off causes kickback noise on the bias lines that can propagate to the rest of the circuit. Moreover, biasing the block with low bias current causes long start-up times which complicates turning it on on a cycle-by-cycle basis. Sometimes, the block is enabled only when output voltage drops below regulation, but this may not protect the chip in sudden short on its output.

1.6 Organization

The organization of this thesis is as follows. Chapter two gives brief overview of current sensors and continues with a development of high voltage current sensor based around a differential difference current conveyor (DDCC) with high voltage input stage and gain trimming.

Chapter three deals with triangular waveform generating relaxation oscillators and presents a new topology suitable for DC-DC converters. This new relaxation oscillator employs only one low area comparator with accurate hysteresis set by a bias current and a resistor.

Chapter four is about current comparators. After an overview of ZCD and OCD architectures a new dual purpose high voltage buck over current/boost zero crossing detector is presented, followed by a new overcurrent detector with built-in reference.

Conclusion in chapter six gives a brief summary of the work done a gives an overview of the publication activity of the author.

2 Current Sensors

This chapter deals with current sensors, more specifically, current sensors for switching DC-DC converters sensing inductor current either continuously, or in a specific phase of the switching cycle (according to the needs of a particular control loop).

An overview of different current sensing principles can be found in [9, 10]. When the power MOS transistors are integrated on-chip the copy or sense MOS technique is used. For applications with off chip power transistors other techniques measuring inductor current must be used.

The next sections look into the most used sensing principles more in detail. Development of a novel high voltage current sensor follows.

2.1 On-chip inductor current sensing

Although many current sensing techniques exist [9] only few can be used for applications requiring sensing on on-chip power transistors. The sense-MOS technique of current sensing is well established and used throughout industry.

The principle of operation is depicted in Fig. 2.1. As described in the previous chapter the power MOS transistor in an SMPS operates as a switch. When turned-on its IV characteristic (for low V_{DS}) can be approximated by the one of an equivalent resistor

$$R_{\text{dson}} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}, \tag{2.1}$$

where μ is the mobility of the respected current carriers, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor, respectively and V_{TH} is the threshold voltage. When the inductor current I_L flows through the power transistor M_P it develops drain-source voltage $V_{DS} = R_{\text{dson}} I_L$. This voltage is then forced with an operational amplifier onto second transistor M_{SENSE}[1] whose current is then sent for processing. Because both V_{GS} and V_{DS} of the transistors are the same the ratio of the sense and coil currents is equal to the ratio of their R_{dson} and therefore their widths (length is always the same for both transistors to equalize short channel effects)

$$I_{\text{sense}} = I_L \frac{R_{dsonP}}{R_{dsonS}} = I_L \frac{W_{\text{sense}}}{W_P}, \tag{2.2}$$

where R_{dsonS}, W_{sense} and R_{dsonP}, W_P are the on-state resistances and total widths[2] of the sense and power transistors.

Given the constraints on power consumption the ratio of widths can be as low as 10^{-4} or even 10^{-5}. It can then happen that the width of the M_{SENSE} reaches the limits of the given technology. However, this is undesirable as the narrow channel effects will change M_{SENSE} parameters and consequently deteriorate ratio accuracy across temperature. Moreover, too small sense transistor will experience large mismatch and further ratio accuracy. Instead, it

[1] An alternative term for sense MOS is copy MOS.

[2] Counting all transistor modules and fingers.

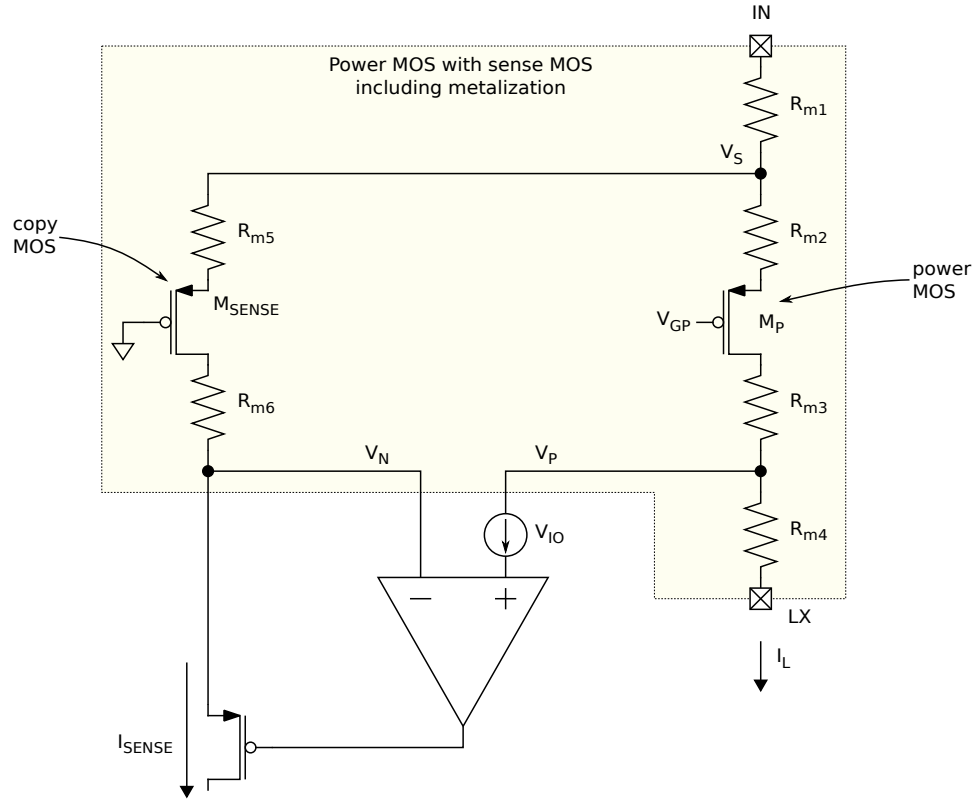


Figure 2.1: Sense/copy MOS current sensing technique.

is possible to reduce the ratio by stacking several modules of sense transistor in series. An example of this practice can be found in Chapter 4.

In reality the on-state resistances are not the sole ones that contribute to the total path resistance. Metal interconnection as well as bond-wire or ball resistances can contribute significant portion of the total resistance, especially for high current applications requiring very low total resistance. The power transistor is spreads across large area and divided into fingers and so the metal contributions are distributed. For further analysis a surrogate model in Fig. 2.1 is used. Another detrimental effect is due to the input offset voltage v_{io} of the operational amplifier. Taking all this into account the sensed current can then be expressed as

$$I_{\text{sense}} = I_L \frac{R_{dsonP} + R_{m2} + R_{m3}}{R_{dsonS} + R_{m5} + R_{m6}} + \frac{v_{\text{io}}}{R_{dsonS} + R_{m5} + R_{m6}}, \tag{2.3}$$

where R_{m2}-R_{m3} and R_{m5}-R_{m6} are metal and bond-wire resistances of the surrogate model.

Since metal and transistor resistances have different temperature coefficients it is necessary to balance the sense path metals denoted by R_{m5} and R_{m6} to be in the same proportion to R_{dsonS} as R_{m2} and R_{m3} is to R_{dsonP}, thus keeping the same ratio across temperatures. The temperature stability is also closely related to the position of M_{SENSE} in layout. As the power transistor heats up during operation M_{SENSE} should be placed close to it so they are at the same temperature.

As can be seen position of M_{SENSE} and its connection M_P, as well as picking up sensing nodes V_N and V_P is not an easy task. It must be done carefully with the help of post-layout metal extraction or even using specialized software [4].

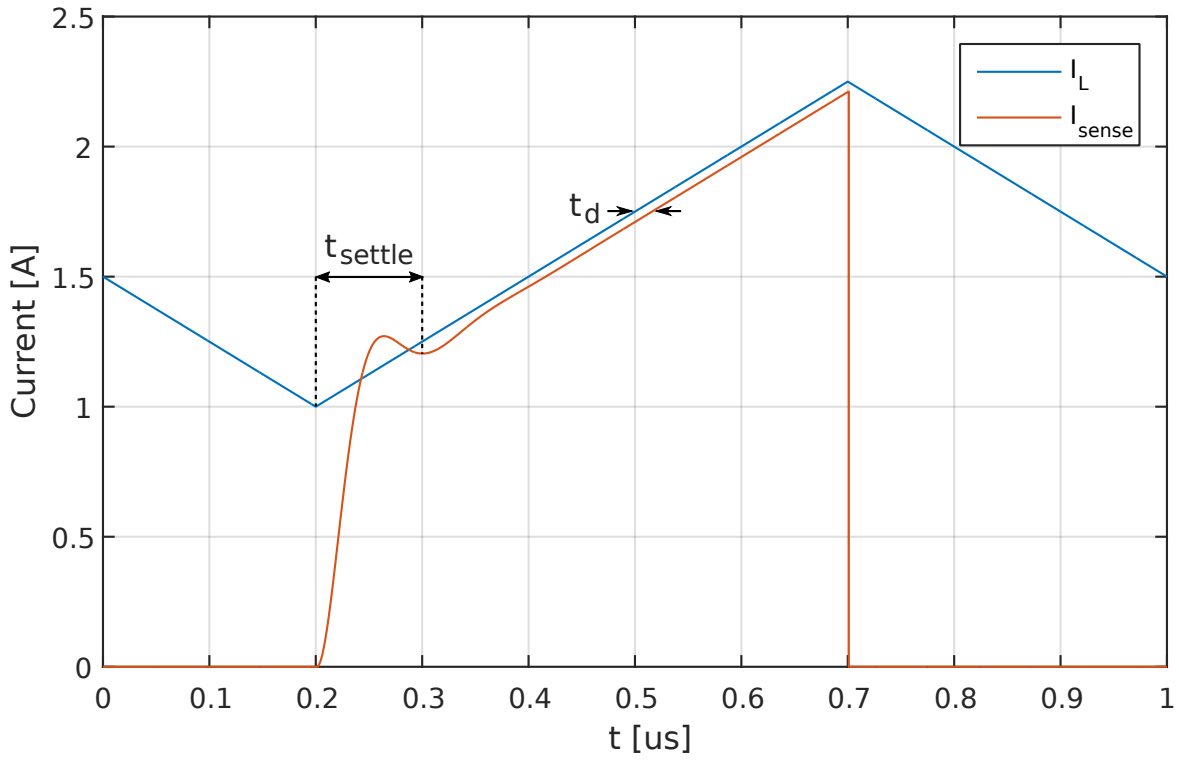


Figure 2.2: High-side current sensor transient response example (sensor output scaled to facilitate comparison).

The effect of operational amplifier's input offset voltage from Eq. 2.3 can be converted back to the inductor current as input current offset

$$I_{L\text{off}} = \frac{v_{\text{io}}}{R_{dsonP} + R_{m2} + R_{m3}}. \tag{2.4}$$

Given power path resistance of 100 mΩ an offset voltage of 1 mV will induce inductor measurement error of 10 mA. For over-current protection offset is usually not a problem since the threshold is usually in the range of amperes. For regulation purposes the mere offset may not be a problem as the integrator (see previous chapter for system description) will compensate it. However, negative offset will create a dead band at low current readings.

As the sensing is done only on one transistor the inductor current is sensed only in part of the switching period. In the rest of the period the switched inductor node LX is tied to the opposite power supply by second power transistors. During this time the input of the operational amplifier must be protected from this high voltage. The system thus contains a masking circuit which enables the current sensor (or just connects its input to LX node) only when it is safe, usually on the basis of voltage on LX and gate voltage of the power MOS.

A transient output example of a current sensor is depicted in Fig. 2.2. As stated above, sensing is enabled or unmasked only when the particular power MOS is on. When this happens the output of the current sensor needs some time t_{settle} to settle and to start follow the input current. This time is influence by many factors, such as bandwidth and phase margin of the current sensors or whether the LX node itself already settled to a value given

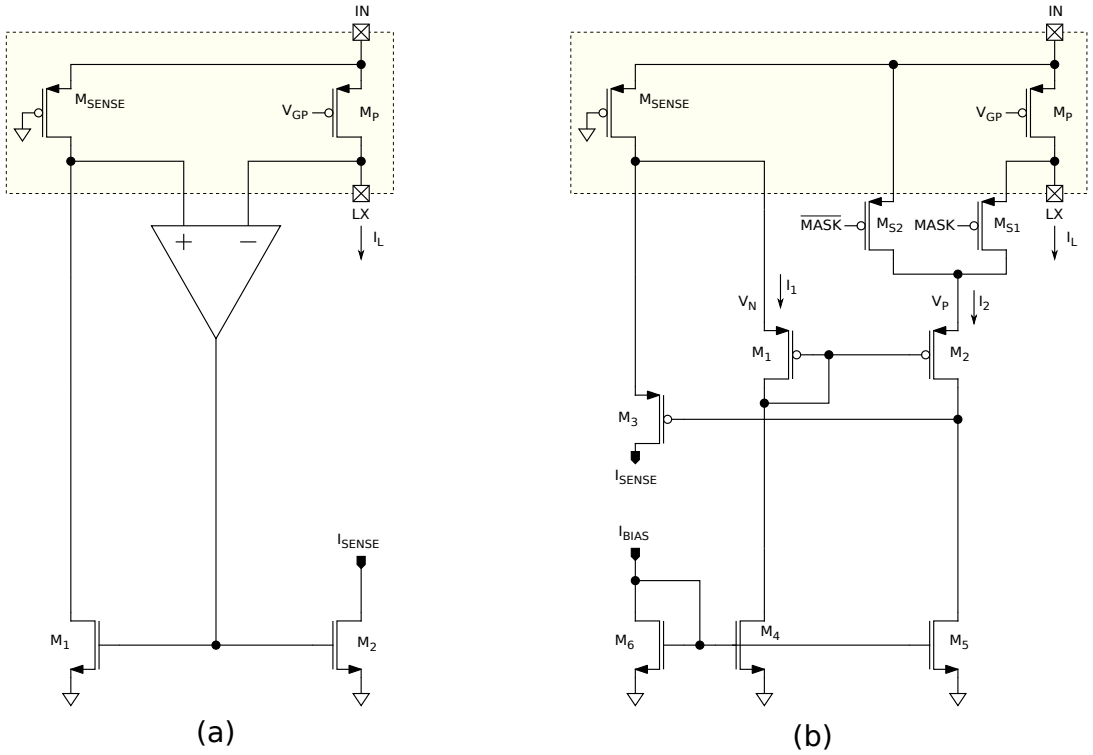


Figure 2.3: Sense MOS current sensor: (a) amp. w/ common source stage, (b) common gate amplifier.

by the resistance of the power path. Due to these effects and also due to possible capacitive coupling the output of the sensor can overshoot. This is a problem over-current protection or some regulator architectures (such as peak-current mode) as these could prematurely trigger. It is therefore common to generate another masking signal that indicates the output of the current sensor is valid and mask further circuits from processing current sensor output during its settling time.

Due to a finite bandwidth f_{BW} the current sensor tracks the input waveform with a delay. This delay can be estimated for a one pole system as

$$t_d = \frac{1}{2\pi f_{\mathrm{BW}}}. \tag{2.5}$$

Amplifier topologies

Now we will focus on the transistor topologies used for the amplifier. Fig. 2.1 uses operational amplifier with a source follower. In order to guarantee correct operation a folded cascode amplifier must be used to be able to process high input common mode voltages close to the supply line. One such a solution was presented in [11].

Instead of using source follower, the operational amplifier can drive a common source stage [12] as depicted in Fig. 2.3a. The common source transistor M_1 together with M_2 form a current mirror so the output current can be taken from M_2. Adding another output transistors to this current mirror we can easily distribute current information to different parts of the system.

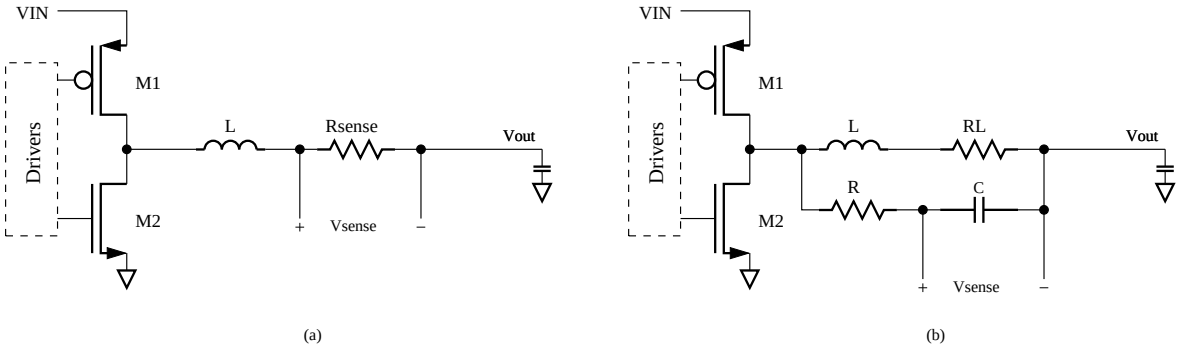


Figure 2.4: Off-chip inductor current sensing:(a) on external resistor and (b) filter-based sensing on coil resistance.

Instead of using traditional gate input operational amplifiers, more common practice is to employ simpler stages with common base [13] or common gate [14–17] amplifiers as can be seen in Fig. 2.3b. The differential input voltage $V_P - V_N$ is sensed through sources of M_1 and M_2 which form a source driven differential pair. Since it is loaded with a current source M_5 the gain of the stage can be written as $g_{m2}(r_{o2}||r_{o5})$, where g_{m2}, r_{o2} and r_{o5} are the transconductance and output resistances of the respective transistors. Although not shown, for higher output resistance and consequently higher gain the transistors M_1-M_2 and M_4-M_5 are usually cascoded. Cascodes are also important when high voltage capability is requested since they can provide the necessary protection from over-voltage on the main matched transistors[3].

Transistors M_{S1} switches the V_P node to LX when M_P is turned-on and sensing takes place. Otherwise V_P is switched to IN using M_{S2} thus making zero differential voltage and therefore zero output current (neglecting offset). This way the voltages of the sources of the differential pair are always close to each other so that they are stressed the same and protected from high voltage of LX. If this was not the case the unequal stress would cause offset shift over time or even damage of M_2 if $V_{\text{IN}} - V_{\text{LX}}$ went beyond its save operating area.

One drawback of the common gate amplifiers is their input currents I_1 and I_2, as I_1 creates a drop on M_{SENSE} and therefore induces input offset voltage of $R_{dsonS}I_1$. As in regulation $I_1 \doteq I_2$ one can introduce the same offset drop also in the second amplifier input if, for example, M_{S1} is sized the same as M_{SENSE}[4].

2.2 Off-chip inductor current sensing

For applications with off chip power transistors other techniques measuring coil current must be used.

One way of measuring coil current uses a sensing resistor in series with the coil as depicted in Fig. 2.4a. This has the disadvantage of introducing additional loss into the system and lowering overall efficiency. Other method uses the parasitic resistance of the coil (DCR) to measure the current [9]. This is done by adding a filter in parallel to the coil as shown in

[3]High voltage transistors, such as DMOS, tend to have worse matching properties so they are not used in places where precise matching is required.

[4]R_{dson} of M_P doesn't induce any error as it is negligible due to the very high ratio of M_P and M_{SENSE}

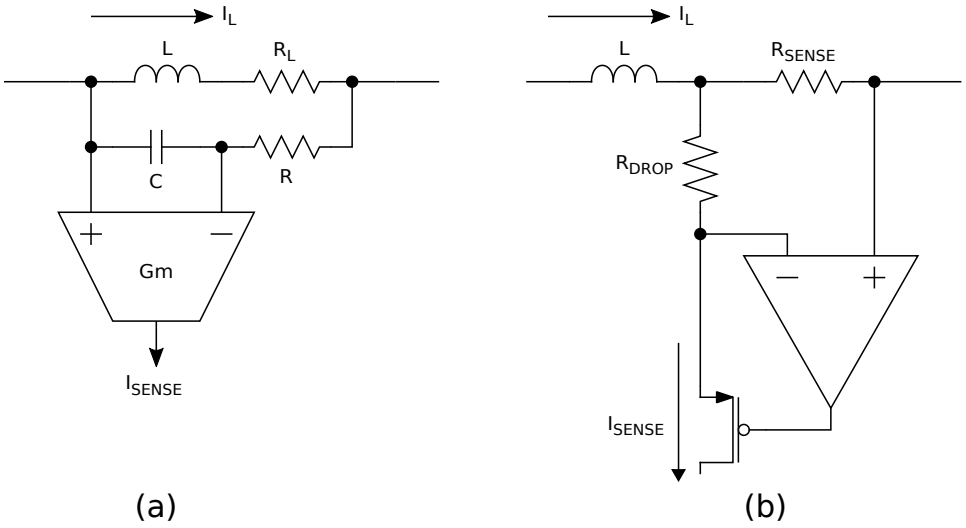


Figure 2.5: Off-chip sensing architectures:(a) transconductance amplifier, (b) drop compensation amplifier.

Fig. 2.4b, where R_L represents a DC resistance of the coil. If the following condition holds

$$RC = \frac{L}{R_L}, \tag{2.6}$$

then the voltage on the capacitor is proportional to the inductor current as

$$v_C(t) = R_L i_L(t). \tag{2.7}$$

One of the circuits sensing off-chip inductor current is presented in [18]. The sensing principle is depicted in Fig. 2.5a. It uses transconductance amplifier to sense the capacitor voltage proportional to the inductor current. However, as the transconductance in [18] is realized by a differential pair the process and temperature variations make current readings inaccurate.

The sensing circuit presented in [19], depicted in Fig. 2.5b, uses an operational amplifier and a source follower to sink current from a resistor R_{DROP} and equalize its drop to the one on sense resistor R_{SENSE}. This is in fact similar principle as the one in Fig. 2.1 and the same circuit topologies can be used here. The same principle is also used in [20], where the current sensors uses the current shunt monitor chip INA139. However, these circuits do not support bidirectional current sensing.

The circuit in [21] uses instrumentation amplifier to sense the coil current, however, it requires high voltage operational amplifiers. Another solution [22] uses capacitors to sample the input voltage but it requires capacitors with high voltage capability. These are usually available only as metal-metal capacitors and as such consume a lot of silicon area.

Another solution was proposed by the author of this thesis in [C]. The block diagram of this current sensor is in Fig. 2.6. The basic building block is the DDCC [23] with multiple outputs which is described in ideal form as

$$I_{\mathrm{REF}} = 0,\ I_P = 0,\ I_N = 0, \tag{2.8a}$$
$$V_X = V_{\mathrm{REF}} + \alpha(V_P - V_N), \tag{2.8b}$$
$$I_{Z1} = I_{Z2} = I_X - I_{\mathrm{off}}, \tag{2.8c}$$

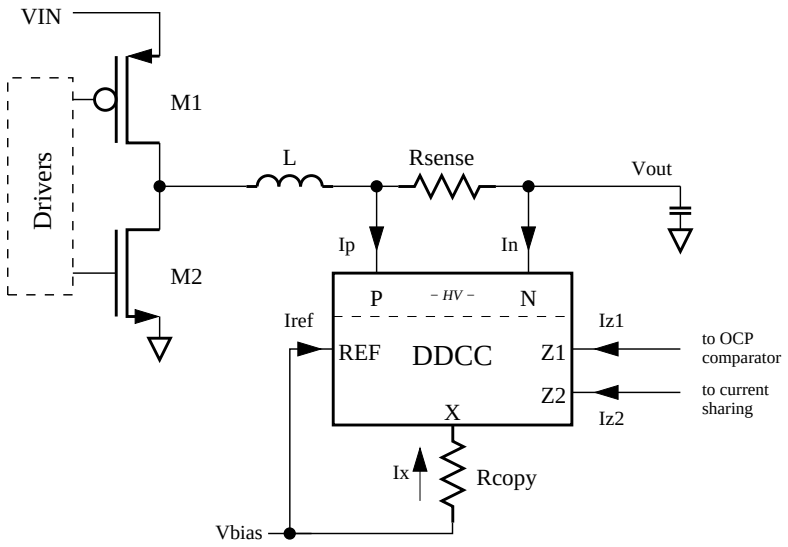


Figure 2.6: Block diagram of a DDCC based current sensor.

where I_{off} is internally added offset current to allow simple bidirectional signal processing by the subsequent circuitry and the gain α equals 1 for a traditional DDCC.

The sensed voltage difference on the R_{sense} is copied by the DDCC onto a resistor R_{copy}, therefore the output currents are proportional to the coil current as

$$I_{Z1,2} = \alpha I_L \frac{R_{\text{sense}}}{R_{\text{copy}}} - I_{\text{off}}. \tag{2.9}$$

The output currents are identical and can be easily added and scaled according to the various needs of the application. The V_{bias} is a constant inaccurate voltage selected in the common mode range of the inputs.

The analysis of the DDCC behaviour has been carried in [23]. For accurate α the internal feedback loop must have a sufficient gain, this is guaranteed by cascoding of the internal current mirrors. Another major source of inaccuracy are the nonlinearities.

The main component of DDCC is a differential difference amplifier, its nonlinearities are analyzed in the next section.

2.3 Analysis of a DDA

Differential difference amplifier (DDA) is one of the most used modern functional block first proposed in [24]. It is also a basic block for building other functional blocks such as DDCC [23]. The DDA has two inverting and two non-inverting inputs as can be seen from the symbol shown in Fig. 2.7a. The ideal DDA is governed by the following equation

$$v_{out} = A\left(v_{p1} - v_{n1} + v_{p2} - v_{n2}\right), \tag{2.10}$$

where A is an open-loop gain of the DDA.

The DDA function is usually implemented by summing outputs of two transconductors and amplifying it. One of the possible CMOS implementations is in Fig. 2.7b. The output current of two differential pairs is summed and amplified by two stages.

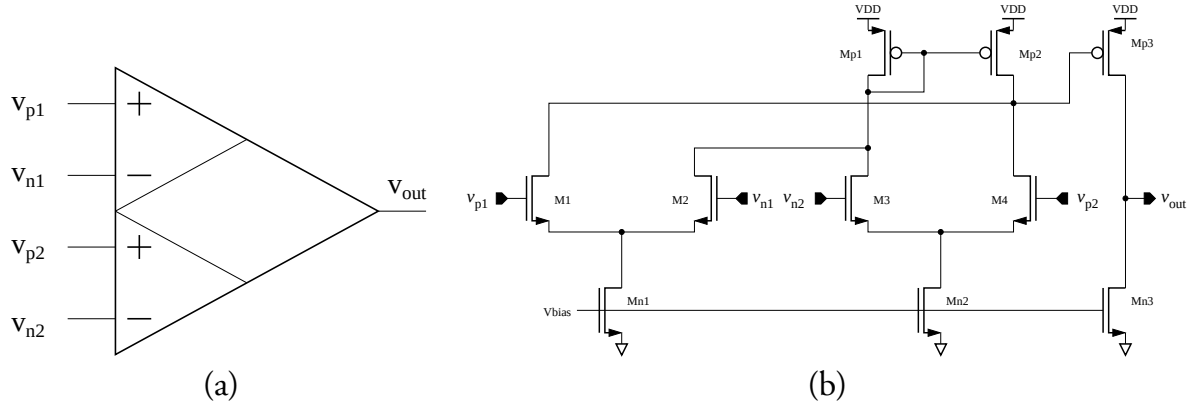


Figure 2.7: Differential difference amplifier: (a) symbol, (b) example of CMOS implementation.

However, this process involves various sources of errors. First, the transconductors may not be fully linear in the whole input voltage range. This is especially true when the mere differential pairs are used as in Fig. 2.7b. Second, the gain of the two transconductors may differ, and third, the transistor mismatch and the potential asymmetry of the circuit causes offset.

The analysis of the open loop parameters of the DDA was carried out in [25], however, the parameters were derived only for MOS transistors in strong inversion using a square law model and it doesn't offer closed form solutions for DDA under feedback. This chapter focuses on the analysis of the DDA in unity gain configuration, which is used the most in various function blocks such as the aforementioned DDCC. Although the derivations are approximate the results are provide qualitative view on the studied system.

Differential pair nonlinearity

The nonlinearity of a differential pair can be seen in Fig. 2.8 which depicts a normalized transconductance of a differential pair with respect to its maximal value at zero input voltage. As the magnitude of the input differential voltage increases the transconductance drops. As will be seen next, this drop leads to nonlinearity of the DDA.

For evaluation of Fig. 2.8 a BSIM6/EKV model was used [26, 27] as it smoothly models all regions of operation (weak, moderate and strong inversion regions) of a MOS transistor and simplified equations for analysis are available. Using this model, the IV relationship for a transistor in saturation can be expressed as

$$I_D = \frac{W}{L} I_0 \mathrm{IC}. \tag{2.11}$$

where W is a width of the transistor, L is its length, I_0 denotes a technology current and IC stands for an inversion coefficient. Technology current is a parameter of the EKV model given as

$$I_0 = 2n\mu C_{\mathrm{ox}} U_T^2, \tag{2.12}$$

Inversion coefficient IC is a positive quantity and characterizes the level of inversion of a MOS transistor. It is dependent on the terminal voltages of the MOS transistors according

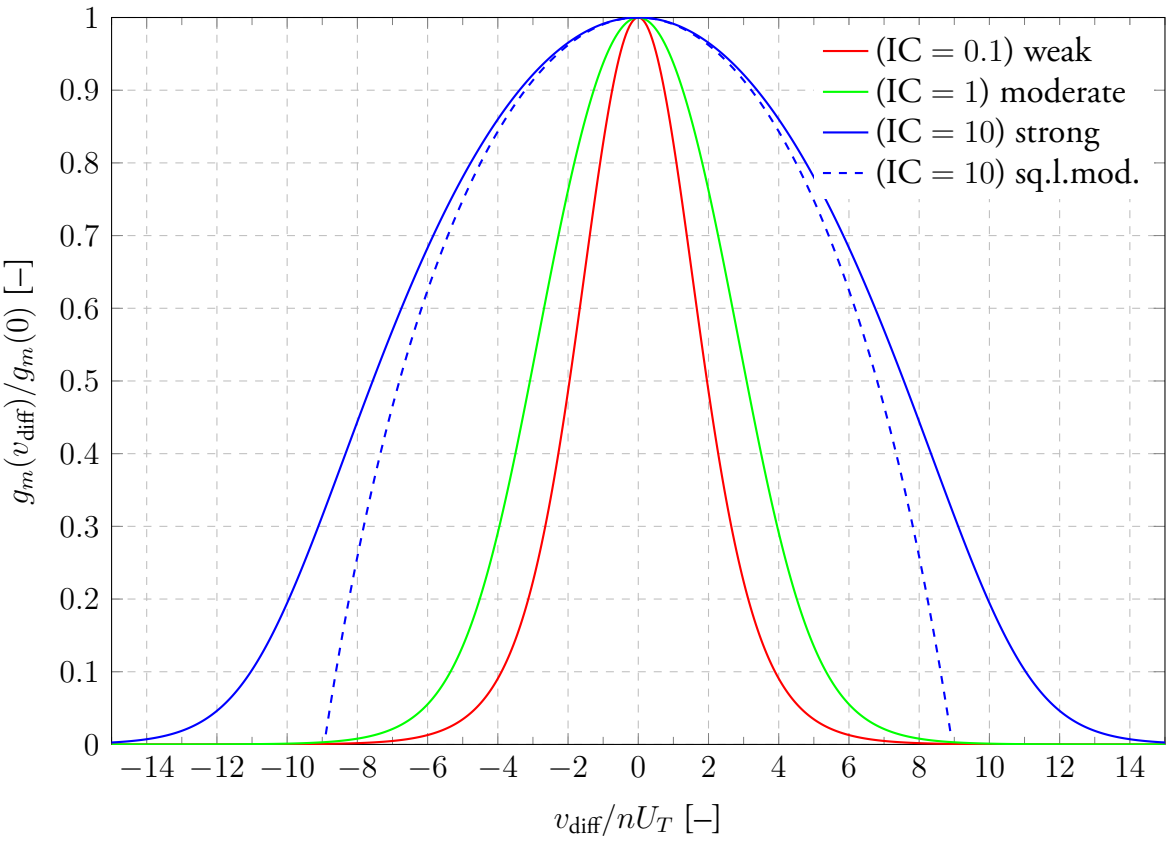


Figure 2.8: Dependence of the transconductance of a differential pair on input voltage difference for various bias conditions.

to the following equation (note that all voltages are referenced to bulk, e.g. $V_S \equiv V_{SB}$)

$$\text{IC} = \ln^2\left(1 + e^{\frac{V_P - V_S}{2U_T}}\right) \cong \ln^2\left(1 + e^{\frac{V_G - V_T - nV_S}{2nU_T}}\right), \tag{2.13}$$

where n denotes substrate factor, V_T threshold voltage, U_T thermal voltage[5] and V_P the so called pinch-off voltage, which can be linearly approximated around threshold voltage as $V_P \cong \frac{V_G - V_T}{n}$.

Using this model in Fig. 2.8, it can be seen that as the magnitude of v_{diff} increases the transconductance falls approaching zero and differential pair therefore stops transferring the signal. The closer the differential pair operates to weak inversion the steeper the drop of the transconductance is.

The x-axis is scaled to nU_T which makes this graph technology independent and will serve as the basis of further analysis.

The figure also presents transconductance analysis using a traditional square law model [28] (dashed line), however, it fails to correctly approximate the transconductance at higher input voltages as the transistor carrying less current falls into weak inversion.

[5]Thermal voltage $U_T = kT/q$, the value for 300 K is 25.85 mV.

Analysis

The simplified block diagram of the DDA in unity gain configuration can be seen in Fig. 2.9, where f denotes the transfer function of the transconductor and R is a cumulative gain

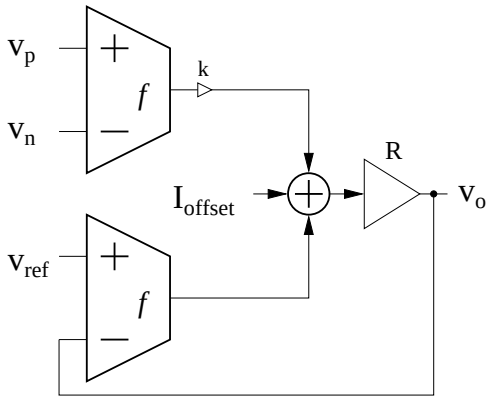


Figure 2.9: Simplified block diagram of DDA in unity gain configuration with major non-idealities.

of all the subsequent stages. The mismatch of tail currents of differential pairs can cause transconductances mismatch. This can be, in the first order, represented by a factor k. The offset is represented by I_{offset}. The function f itself is without offset and satisfies the following two conditions

- $f(0) = 0$,
- $f(-v) = -f(v)$, i.e. function is odd.

Following Fig. 2.9, we can write

$$kf(v_p - v_n) + f(v_{\text{ref}} - v_o) + I_{\text{offset}} = \frac{v_o}{R}. \tag{2.14}$$

If k was equal to zero the circuit would be a simple operational amplifier and v_o would follow (with a gain error) v_{ref}. Adding the second current contributor $kf(v_p - v_n)$ to the loop can be viewed as adding an offset, we can therefore without lack of generality change variables and analyze $v_{\text{out}} = v_o - v_{\text{ref}}$ as a function of $v_{\text{in}} = v_p - v_n$. We then get

$$kf(v_{\text{in}}) - f(v_{\text{out}}) + I_{\text{err}} = \frac{v_{\text{out}}}{R}, \tag{2.15}$$

where we used the fact that f is an odd function to push the minus sign out of the argument of f and for simplicity we grouped $I_{\text{offset}} - \frac{v_{\text{ref}}}{R}$ into I_{err}. Because of the unity gain configuration the v_{out} is expected to be v_{in} except for some error Δ

$$v_{\text{out}} = v_{\text{in}} + \Delta. \tag{2.16}$$

Now if Δ is small we can expand f at v_{in} using only the first term of the Maclaurin series

$$f(v_{\text{in}} + \Delta) \doteq f(v_{\text{in}}) + \Delta \left.\frac{\mathrm{d}f}{\mathrm{d}v}\right|_{v=v_{\text{in}}} \equiv f(v_{\text{in}}) + \Delta g_m(v_{\text{in}}), \tag{2.17}$$

where we denoted derivate of f as g_m. Now using (2.16) and (2.17) in (2.15) we get

$$(k-1)f(v_{\text{in}}) + g_m(v_{\text{in}})\Delta + I_{\text{err}} = \frac{v_{\text{in}} + \Delta}{R}. \tag{2.18}$$

Solving for Δ and adding v_{in} gives back expression for v_{out}

$$v_{\text{out}} = v_{\text{in}} + \Delta = \frac{((k-1)f(v_{\text{in}}) + I_{\text{err}} + g_m(v_{\text{in}})v_{\text{in}})\,R}{1 + g_m(v_{\text{in}})R}. \tag{2.19}$$

Now all the terms use small signal quantities except for $f(v_{\text{in}})$. For very small v_{in} it can be approximated as $g_m(0)v_{\text{in}}$, however, a better approximation can be made using $g_m(v_{\text{in}})$ (which is already present int the expression) if we look at Taylor's expansion of both $f(v)$ and $g_m(v)$

$$f(v) = \sum_{i=0}^{\infty} k_{2i+1}v^{2i+1} = k_1 v + k_3 v^3 + k_5 v^5 \ldots \tag{2.20}$$

$$g_m(v) \equiv \frac{\mathrm{d}}{\mathrm{d}v}f(v) = \sum_{i=0}^{\infty}(2i+1)k_{2i+1}v^{2i} = k_1 + 3k_3 v^2 + 5k_5 v^4 \ldots \tag{2.21}$$

Because f is odd function the expansion has only odd terms. Now if we approximate $f(v)$ as

$$f(v) \approx \left(\frac{1}{3}g_m(v) + \frac{2}{3}g_m(0)\right) v = k_1 v + k_3 v^3 + \frac{5}{3}k_5 v^4 + \ldots \tag{2.22}$$

we see that it is able to reconstruct the first two non-zero terms of the expansion 2.20.

Gain and offset

The important circuit characteristics can now be expressed. Offset voltage is simply v_{out} evaluated at zero

$$v_{\text{off}} = v_{\text{out}}|_{v_{\text{in}}=0} = \frac{I_{\text{err}}R}{1 + g_m(0)R} = \frac{I_{\text{offset}}R - v_{\text{ref}}}{1 + g_m(0)R}. \tag{2.23}$$

Another important parameter is gain at zero input voltage

$$A_0 = \left.\frac{\mathrm{d}v_{\text{out}}}{\mathrm{d}v_{\text{in}}}\right|_{v_{\text{in}}=0} = \frac{kg_m(0)R}{1 + g_m(0)R}. \tag{2.24}$$

Nonlinearity

If transcoductance f was linear across the input voltage range, the output voltage would be also linear and given by $A_0 v_{\text{in}} + v_{\text{off}}$. However the non-linearity of f leads to the non-linearity of $v_{\text{out}}(v_{\text{in}})$ relationship. This can be characterized using the nonlinearity parameter NL defined as a relative error with respect to the ideal linear behavior after the correction of gain and offset error

$$\text{NL} = \frac{v_{\text{out}} - v_{\text{off}}}{A_0 v_{\text{in}}} - 1. \tag{2.25}$$

Substituting (2.19), (2.23) and (2.24) into (2.25) we get the expression for nonlinearity

$$\mathrm{NL} = \frac{1}{g_m(0)R}\left(1 - \frac{1+g_m(0)R}{1+g_m(v_{\mathrm{in}})R}\right) - \frac{I_{\mathrm{err}}}{v_{\mathrm{in}}g_m(0)k}\left(1 - \frac{1+g_m(0)R}{1+g_m(v_{\mathrm{in}})R}\right) + \frac{k-1}{k}\frac{1+g_m(0)R}{1+g_m(v_{\mathrm{in}})R}\frac{\frac{f(v_{\mathrm{in}})}{v_{\mathrm{in}}} - g_m(v_{\mathrm{in}})}{g_m(0)}. \tag{2.26}$$

If we now use (2.22) we get

$$\mathrm{NL} = \left(1 - \frac{1+g_m(0)R}{1+g_m(v_{\mathrm{in}})R}\right)\left(\frac{1}{g_m(0)R} + \frac{2}{3}\frac{1-k}{k}\left(1 + \frac{1}{g_m(0)R}\right) - \frac{I_{\mathrm{err}}}{kg_m(0)v_{\mathrm{in}}}\right). \tag{2.27}$$

We can further simplify this expression by assuming $g_m(v_{\mathrm{in}})R \gg 1$. This also implies that $g_m(0)R \gg 1$ because $g_m(0) \geq g_m(v_{\mathrm{in}})$. The final expression for nonlinearity is therefore

$$\mathrm{NL} = \left(1 - \frac{g_m(0)}{g_m(v_{\mathrm{in}})}\right)\left(\frac{1}{g_m(0)R} + \frac{2}{3}\frac{1-k}{k} - \frac{I_{\mathrm{offset}} - \frac{v_{\mathrm{ref}}}{R}}{kg_m(0)v_{\mathrm{in}}}\right). \tag{2.28}$$

The only time this expression involves $g_m(v_{\mathrm{in}})$ is in ratio with $g_m(0)$. The ratio can be easily determined from the transconductance characteristics of the differential pair (Fig. 2.8). For design purposes, given the operating voltage range and the expected region of operation of the differential pair (IC parameter), the ratio can be looked up and the sensitivity of the nonlinearity on the design parameters ($g_m(0)$, R, k, I_{offset}) can be evaluated.

Figures 2.10 and 2.11 show comparison of calculated values from expression (2.28) with a nonlinearity computed by simulation of (2.15) using the aforementioned BSIM6/EKV transistor model. The evaluation was done for differential pair in strong inversion with $\mathrm{IC} = 10$. The open loop gain $g_m(0)R$ was set to 60 dB. Fig. 2.10 depicts nonlinearity variation with the multiplying factor k which is varied by $\pm 5\%$. Offset current variation can be found in Fig. 2.11. The current is varied by $\pm 0.1\,\mu$A which for the given $g_m(0)$ translates to input offset voltage of ± 1 mV. It can be seen in both figures that the higher the nonlinearity the higher the difference between the calculated and numerically computed value reaching maximal difference of 23% for $v_{\mathrm{in}}/nU_T = -8$ in Fig. 2.10. This stems from the initial assumption that Δ is small and the corresponding first order expansion (2.17). Nevertheless, considering the practical requirement for nonlinearity to be maximally several percent the equation (2.28) provides an insight into dependence of nonlinearity on key design parameters.

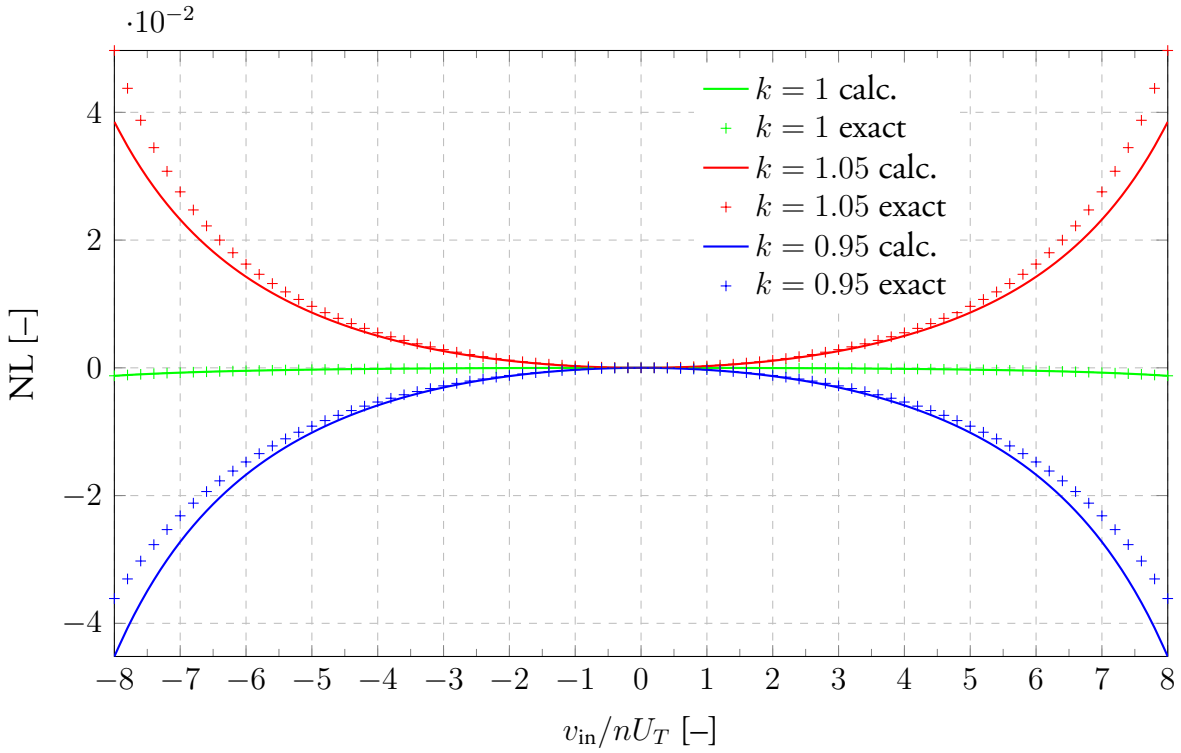


Figure 2.10: Nonlinearity with gain mismatch: calculated with (2.28) and simulation of (2.15), $g_m(0) = 100\,\mu\text{S}$, $R = 10^7\,\Omega$, $I_{\text{offset}} = 0\,\mu\text{A}$, $v_{\text{ref}} = 0\,\text{V}$, IC $= 10$.

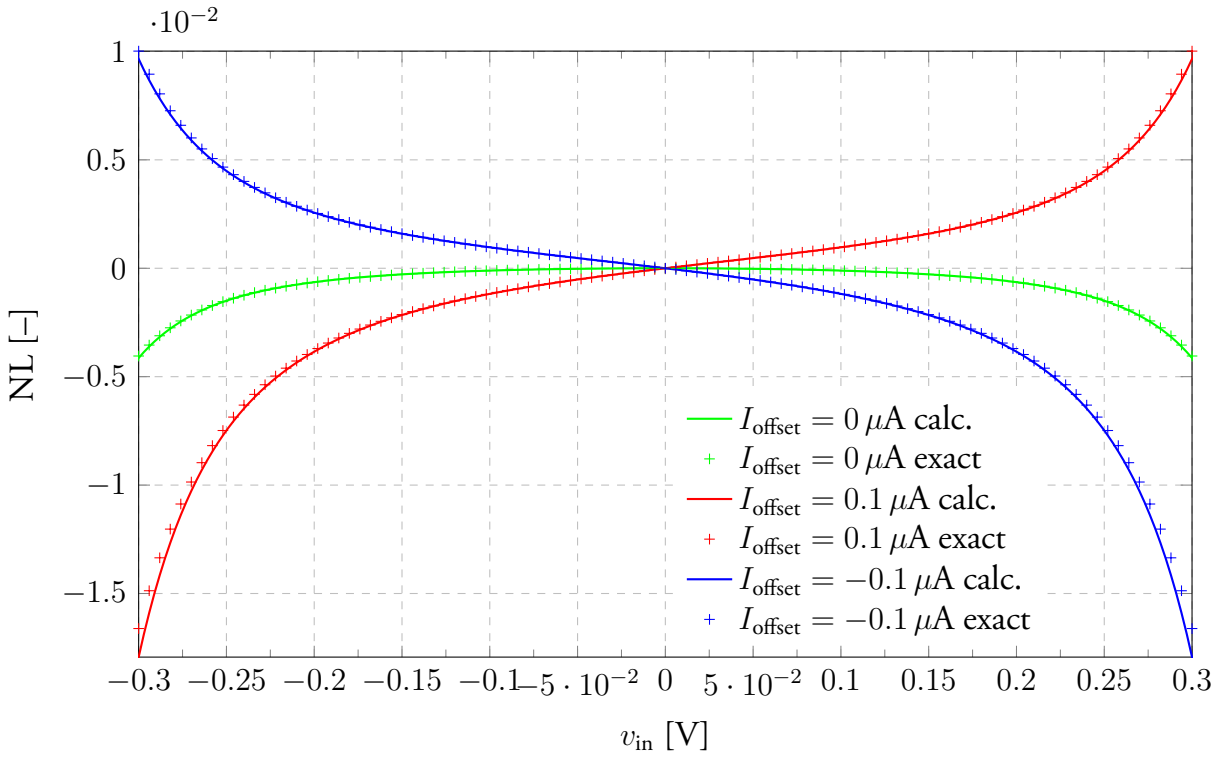


Figure 2.11: Nonlinearity with offset: calculated with (2.28) and simulation of (2.15), $g_m(0) = 100\,\mu\text{S}$, $R = 10^7\,\Omega$, $k = 1$, $v_{\text{ref}} = 0\,\text{V}$, IC $= 10$, $nU_T = 30$ mV.

2.4 High voltage coil current sensor employing DDCC

A high voltage current sensor based on Fig. 2.6 was designed. To save the application board space and reduce component count the resistor R_{copy} is implemented on-chip. However, the technological spread of the resistor leads to the inaccuracy of the gain. This is compensated by trimming the gain α as will be described further.

The schematic of the proposed DDCC can be found in Fig. 2.12. The circuit employs two 3.3 V differential pairs denoted as high voltage (HV) and low voltage (LV) owing to the voltage levels they are processing. The HV pair is composed of transistor M1-M2 and the LV pair is composed of transistors M3-M4. The current from the two differential pairs is summed by the folded cascode (M7-M8, M10-M15) followed by a second gain stage (M9, M16-M17), voltage follower M20 completes the feedback loop around the low voltage differential pair. The current mirrors M23-M28 copy the current through terminal X to the outputs Z1 and Z2. Current source M21-M22 adds an offset current I_{off} for bidirectional operation.

The HV differential pair is biased from the HV supply by means of the current mirror M29-M32 where the cascodes are based on DMOS transistors. To sustain high voltage the HV differential pair is cascoded by DMOS transistors M5-M6. In order to not load differential pair or its biasing a separate circuit composed of M33-M38 is used to bias the gates. The M33-M35 form a differential pair with M33 and M34 averaging the input voltage.

The transfer of the voltage from the HV input pair to the node X is given by the ratio of the transconductances of the two differential pairs, i.e.

$$\alpha = \frac{g_m^{HV}}{g_m^{LV}} = \frac{g_m^{M1}}{g_m^{M3}}. \tag{2.29}$$

The mismatch between the two differential pairs and their bias current will cause mismatch between the two transconductances. This together with the process variations of the internal resistor R_{copy} will lead to the gain inaccuracy. Both of these effects can be trimmed by using the relation for α and trimming the transconductance of the HV stage. This is done by varying the bias current of the HV stage since to a first degree the transconductance is proportional to the bias current [26]. To ensure good linearity, the differential pairs are bias in strong inversion. The bias current is set by the gain trimming DAC and mirrored by the HV current mirror M29-M32.

The gain trimming DAC is depicted in Fig. 2.13. It is based on binary scaled current sources with added offset current. The typical current value is 24 uA with a trimming range spanning from 16 uA to 31 uA.

Using previously derived Eq. 2.28 we can estimate the nonlinearity caused by the trimming as

$$\text{NL} = \frac{2}{3}\frac{1-k}{k}\left(1 - \frac{g_m(0)}{g_m(v_{\text{in}})}\right). \tag{2.30}$$

Assuming strong inversion operation, nU_T of 40 mV and input voltage range 50 mV then $g_m(v_{\text{in}})/g_m(0)$ is about 0.97. The nonlinearities for minimum and maximum trimming then turn out to be about -1% and 0.5%, respectively.

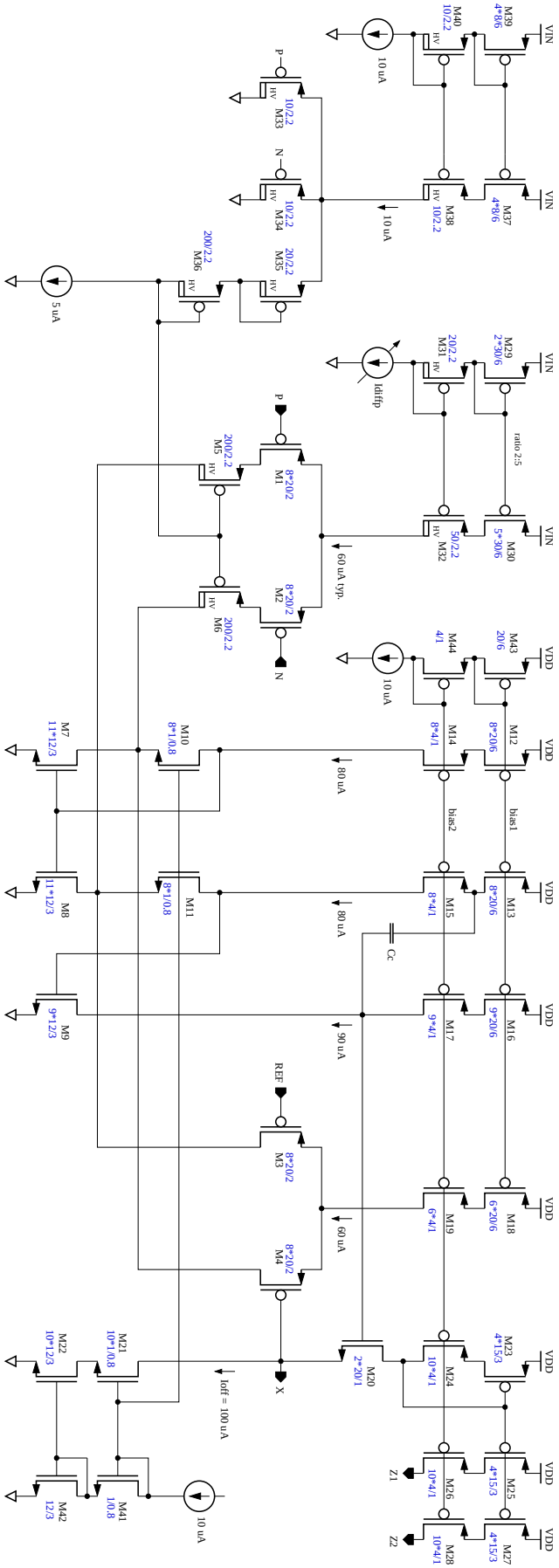


Figure 2.12: Schematic of the proposed DDCC based current sensor (dimension are in μm).

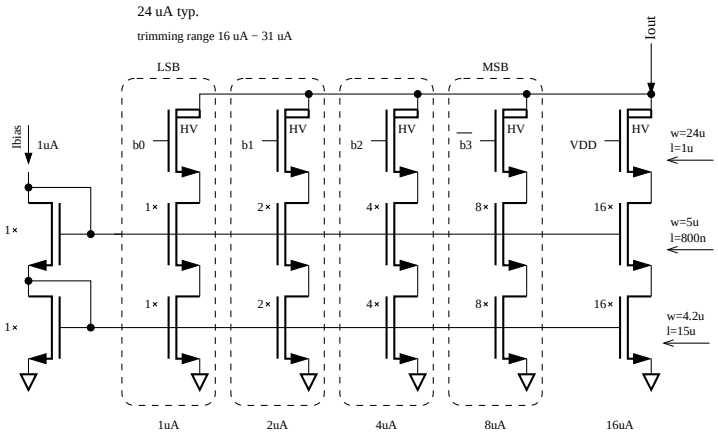


Figure 2.13: Gain trimming DAC (dimensions apply for entire rows).

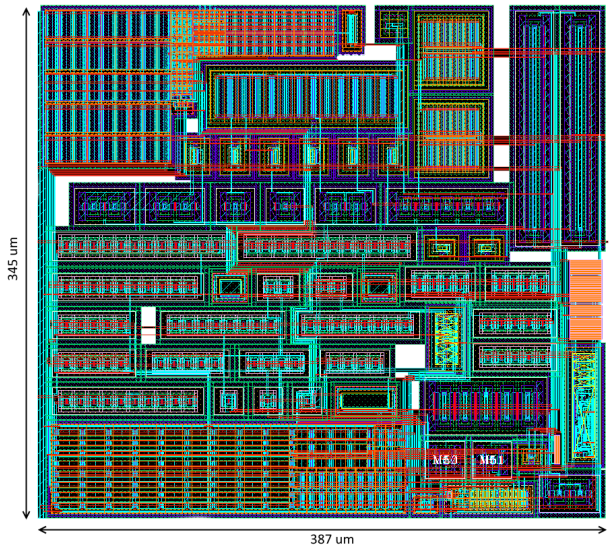


Figure 2.14: Layout of the proposed circuit (courtesy of STMicroelectronics).

Implementation and results

The proposed current sensor was layouted by STMicroelectronics and realized in 0.35 um BCD technology from the same company. The area of the current sensor is 0.387×0.345 mm^2 as can be seen in Fig. 2.14. The LV part is supplied from an on-chip 3.3 V regulator whereas the HV part is supplied from the input voltage of the DC-DC converter which can go as high as 40 V. For a typical input voltage of 12 V the circuit consumes 3.2 mW.

Fig. 2.15a shows the simulated transfer characteristics for different trimming combinations. The gain trimming range is within ± 22 % with a step about 2.8 %. This is sufficient to trim the process variation of the internal resistor R_{copy} which is the major contributor of the gain variation.

The nonlinearity characteristics can be seen in Fig. 2.15b. The discrepancy of the simulated values with respect to the calculated ones can be accounted for by the large trimming range beyond the assumption of small tail current difference in the previous section.

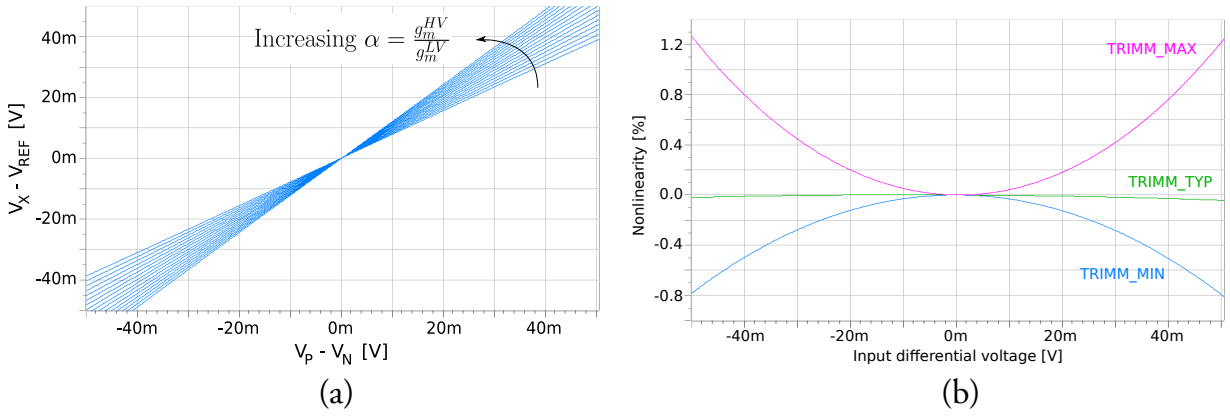


Figure 2.15: (a) Transfer characteristics, (b) achieved nonlinearity $(I_{\text{sim}}/I_{\text{ideal}} - 1)$ for different trimming steps.

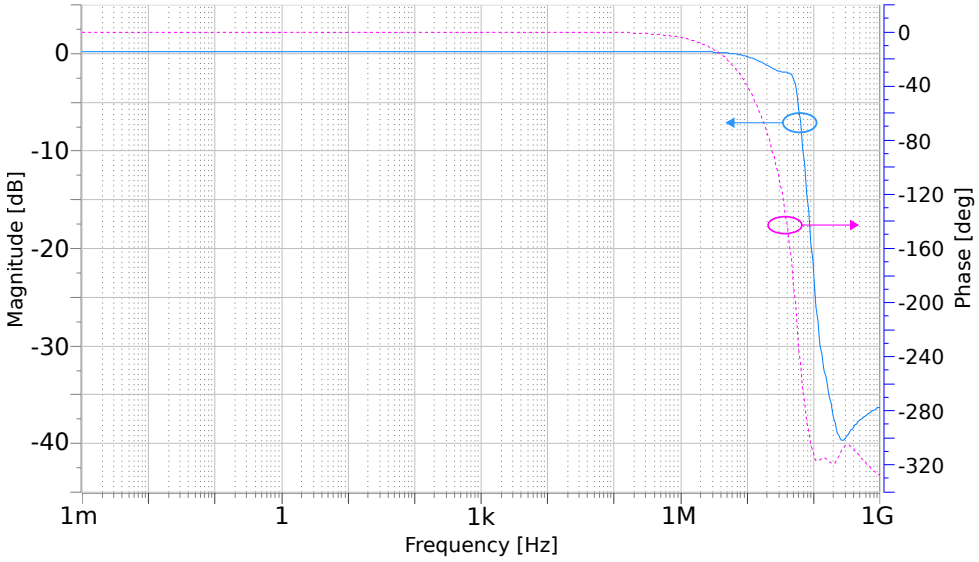


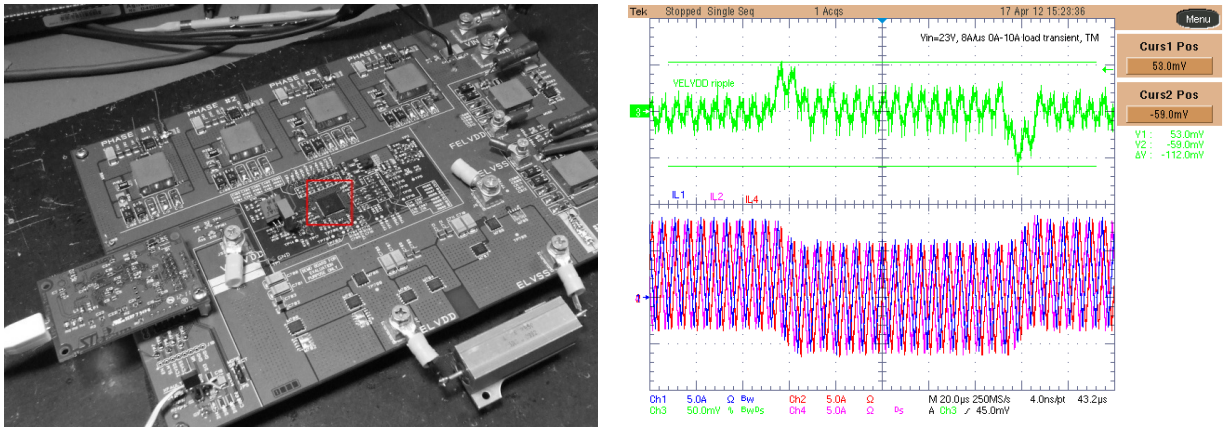
Figure 2.16: Gain and phase characteristics of V_X/V_{sense}.

The AC gain and phase response from the input terminal to the X node are in Fig. 2.16. The bandwidth reaches 50.9 MHz.

The proposed circuit was taped-out as part of a four-phase buck DC-DC converter whose application board is in Fig. 2.17a. The output of the current sensor is used for overcurrent protection and for balancing the current evenly among all the phases. Although the current sensor could not be measured directly the operation can be verified by the balancing function of the system, as shown in Fig. 2.17b. The waveforms labeled IL1, IL2 and IL4 are coil currents corresponding to three of the phases and are sensed by the described circuit as in Fig. 2.6. The same average currents of the phases show correct operation of the circuit.

2.5 Summary

In this chapter a new circuit for coil current sensing in high voltage DC-DC converters has been presented. A method for gain trimming based on transconductance variation of the



(a) (b)

Figure 2.17: (a) Application board with the device (mark in square) featuring the proposed current sensor, (b) output voltage and current of three phases balanced with the help of the proposed sensor (images courtesy of STMicroelectronics).

input stage has been described.

The proposed solution has no static input current and the usage of high voltage components is limited to the input stage thereby reducing power consumption and silicon area. This is in contrast with traditional approaches, such as [19, 20, 21], where the operational amplifier has to be designed with both the input and output stages able to sustain high voltage. Another benefit is the ability of bidirectional current sensing which is not possible in some of the previous architectures. Another approach presented in [22] requires high voltage capacitors and the need for reset phase further complicates design and top-level integration. On the other hand, the presented sensor does not employ any special components but the standard CMOS and DMOS transistors present in any BCD type technology. Also the continuous operation simplifies integration with the rest of the application.

The circuit has been implemented in STMicroelectronics 0.35 um BCD technology and occupies area of 0.134 mm^2. It has been integrated as part of a multi-phase DC-DC converter and its function has been verified. The proposed solution is suitable for DC-DC converters with external power MOS transistors where traditional sensors based on copy MOS transistors are not possible as one cannot effectively match integrated transistors with external ones from a different lot or possibly a different technology.

3 Oscillators

Relaxation oscillator circuits are present in almost every electronic application such as microcontrollers, DC-DC converters or RFID chips. With increasing demand for small form surface mount packages silicon area of every block can have an impact on whether the final design fits into the package or not. Recently several architectures with low silicon area have been proposed. In [29] a capacitor is linearly charged and the threshold is compared with a current-mode comparator. In [30] a voltage on an exponentially charged capacitor is compared with a hysteresis comparator. However, none of these solutions generate triangular waveform suitable for use in switching converters.

In voltage mode controlled DC-DC converters the waveform generated by the on-chip oscillator is compared to the output of the error amplifier generating a digital PWM signal. As was stated in the introductory chapter a triangular waveform is preferred as it allows for a higher loop bandwidth.

3.1 Triangular relaxation oscillators

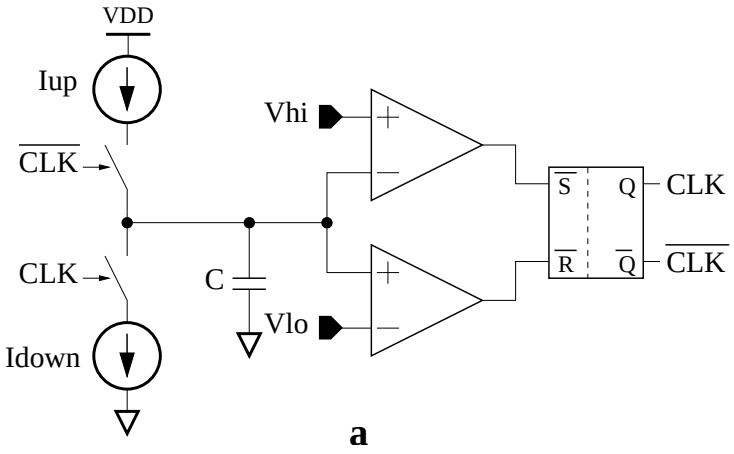


Figure 3.1: Conventional triangle generating oscillator.

Conventional approach to generate a triangular waveform is depicted in Fig. 3.1. A capacitor is charged with a constant current of alternating orientation generated by a current source between two voltage levels V_{lo} and V_{hi}. Considering $I_{\text{up}} = I_{\text{down}} = I$ then the oscillation period (neglecting comparator delays and other second-order effects) is

$$T = 2(V_{\text{hi}} - V_{\text{lo}})\frac{C}{I}. \tag{3.1}$$

If the current I is derived from a voltage reference as $I = V_{\text{ref}}/R$ then the overall period is proportional to RC time constant. The advantage of this solution are the well defined top and bottom boundaries of the triangular waveform. The disadvantage is the requirement of two fast comparators.

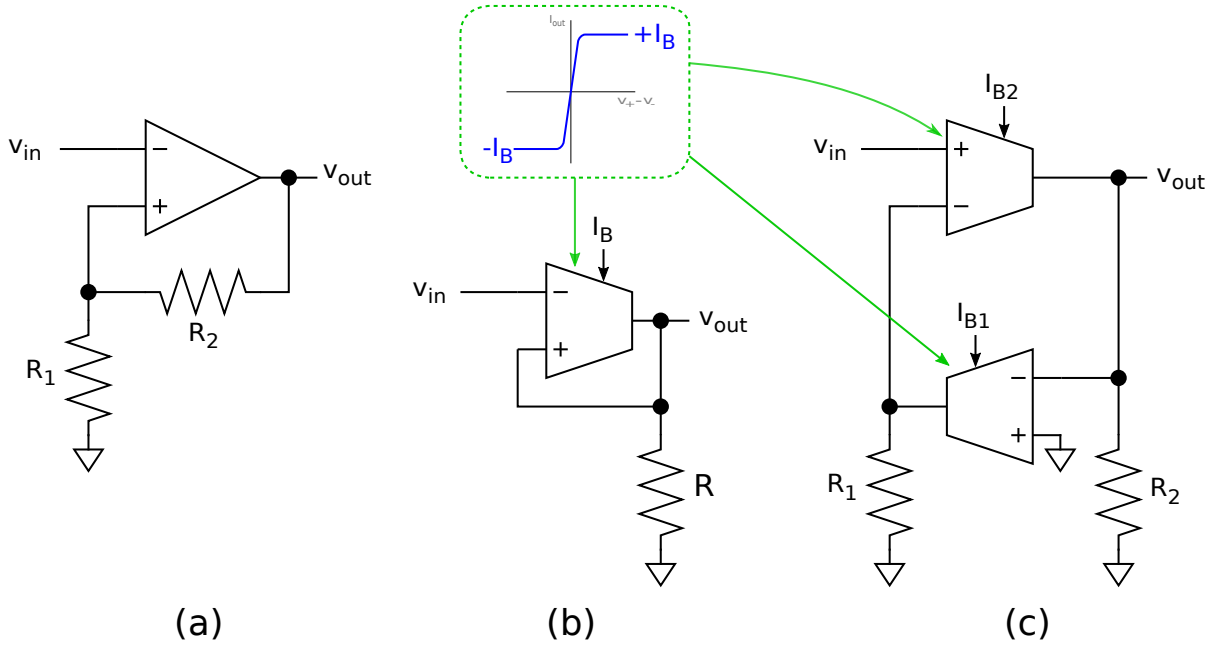


Figure 3.2: Hysteresis comparators: (a) [32], (b) [33], (c) [34].

Instead of using two comparators another solutions employs only a comparator. In [31] a CMOS Schmitt trigger is used. The main drawback of such a circuit is that the hysteresis and consequently the amplitude and frequency are sensitive to PVT variations.

To address this issue, the solution in [32] uses a comparator with a hysteresis set by an external resistor network as depicted in Fig. 3.2a. The two symmetrical thresholds are

$$V_{\mathrm{TH}\pm} = V_{\mathrm{sat}\pm}\frac{R_1}{R_1 + R_2}, \tag{3.2}$$

where $V_{\mathrm{sat}\pm}$ are the saturation voltages of the comparator usually equal to the positive and negative supply voltages, respectively. This solutions thus requires stable supply voltage.

In [33] the hysteresis is set with a resistor and a saturation current of an OTA as can be seen in Fig. 3.2b. The thresholds are then given as

$$V_{\mathrm{TH}\pm} = \pm I_B R, \tag{3.3}$$

where I_B is the saturation current of an OTA which can be set externally as a bias current of a differential pair. To reduce the linear region and increase gain [33] uses two stage OTA design. Similarly, solution presented in [34] uses two OTAs to form a Schmitt trigger as can be seen in Fig. 3.2c. The thresholds are again dependent on the bias current of an OTA.

All these solutions require either comparator or OTA with a differential input stage. Moreover if a symmetrical supply is not available the grounds of the resistors must be held at some common mode voltage (usually half the supply voltage) which further increases power consumption.

Another class of triangular generators is based on the so-called modern functional blocks. In [35] two second-generation current conveyors (CCII) are used for square/triangular generation. A current mode generator is presented in [36] using two multiple-output current controlled current differencing transconductance amplifiers (MO-CCCDTA). Another voltage mode solution uses two differential voltage current conveyors (DVCC) in [37].

Reference	# of passives	# of transistors	Architecture	Output signal
[31]	1	19	CS + CMOS Schmitt trig.	Voltage
[32]	4	N/A	CS + Opamp	Voltage
[33]	2	15	CS + OTA	Voltage
[34]	3	N/A	3× OTA	Voltage
[35]	4	N/A	2× CCII	Voltage
[36]	1	58	2× MO-CCCDTA	Current
[37]	4	N/A	2× DVCC	Voltage.
[38]	3	24	DO-VDBA + FB-VDBA	Voltage
[39]	3	52	ZC-CG-VDCC	Both
[40]	1	N/A	ZC-CG-VDCC	Both
Proposed	**2**	**20**	**CS + single input comp.**	**Voltage**

Table 3.1: Comparison of selected architectures.

A differential output generation was presented in [38] using dual output and fully balanced voltage differencing buffered amplifiers (DO-VDBA and FB-VDBA, respectively). Solutions in [39] and [40] employ single Z-copy controlled gain voltage differencing current conveyors (ZC-CG-VDCC) for voltage/current output functional generator.

The overview of the mentioned architectures can be seen in Tab. 3.1. All the circuits employing modern functional blocks utilize complex analog structures that take a lot of silicon area and power. Number required passive elements is also a concern as these tend to take significant area of the design as will be seen next.

3.2 Triangle/square waveform generator using area efficient hysteresis comparator

In order to improve on the issues of the aforementioned circuits a new triangular relaxation oscillator has been developed. This circuit requires only one single ended comparator and therefore saves both silicon area and power consumption.

Circuit analysis

The schematic of the proposed waveform generator is in Fig. 3.3a. Transistors M_1 and M_4 work as current sources with M_{2-3} as switches controlling charging and discharging of the capacitor C. For symmetrical waveform both current must be equal. Hysteresis comparator is composed of transistors M_{5-9}. M_6 together with R work as $V \rightarrow I$ converter whose output current is compared to I_{M5} produced by M_5. M_8 and M_9 then form a second stage of the comparator whose output is further amplified by a digital CMOS buffer. Hysteresis is created by shorting the resistor by M_7. If the bulk of M_6 is shorted to the source the body effect is avoided and the two threshold voltages are (assuming high gain in the first stage of the comparator):

$$V_{\text{low}} = V_{gs6}|_{I_{M5}} \tag{3.4}$$

$$V_{\text{high}} = V_{gs6}|_{I_{M5}} + R\, I_{M5} \tag{3.5}$$

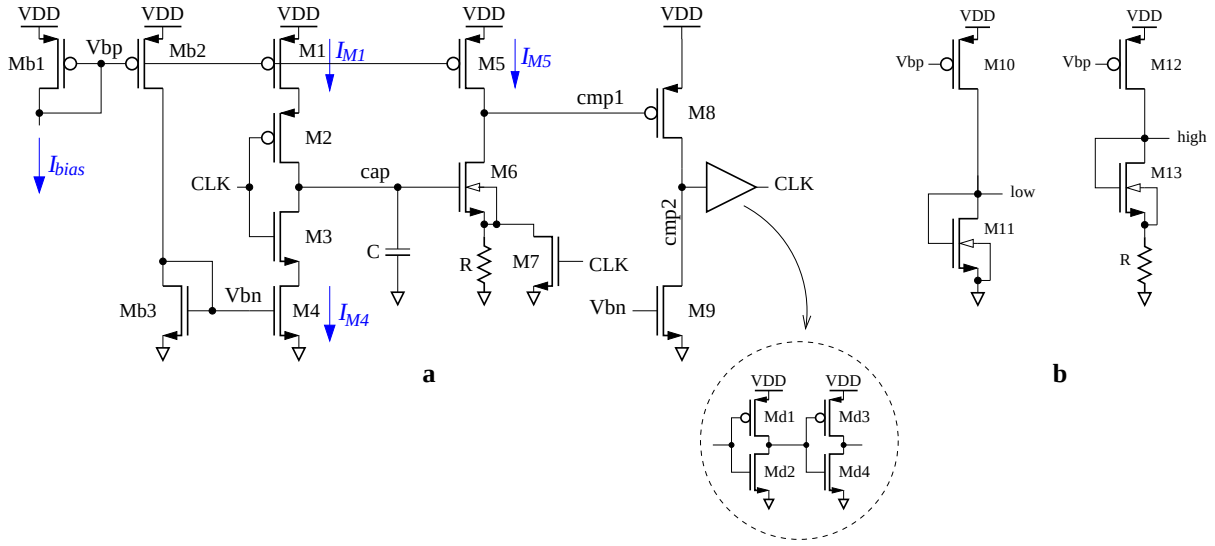


Figure 3.3: Proposed circuit: (a) Waveform generator, (b) reference generators (when not explicitly shown the bulks are tied to V_{DD} or ground for PMOS and NMOS, respectively).

Absolute value of the two voltages is dependent on the gate-source voltage of M_6 but the difference depends only on the current in the first stage of the comparator and the resistor value.

Some applications (e.g. DC-DC converters) may require reference voltages corresponding to the comparator thresholds. These can be extracted with the circuits depicted in Fig. 3.3b. M_{11} is sized to have the same current density as M_6 so that $V_{gs11} = V_{gs6} = V_{\mathrm{low}}$. Similarly, if $I_{M12} = I_{M5}$ and M_{13} is the same size as M_6 then the voltage on the drain of M_{13} corresponds to V_{high}. By the same principle, if needed, setting the resistor value between 0 and R (resistor value in the oscillator) can generate any voltage within the oscillator output voltage range.

Due to the delay of the comparator the capacitor voltage v_{cap} overshoots the threshold V_{high} by $\mathrm{SR}^{+}t_d^{+}$, where SR^{+} is the positive slew rate on the capacitor given by $\frac{I_{M1}}{C}$ and t_d^{+} if the rising propagation delay of the comparator. Similarly for the opposite phase v_{cap} undershoots V_{low} by $\mathrm{SR}^{-}t_d^{-}$, SR^{-} being negative slew rate given by $\frac{I_{M4}}{C}$ and t_d^{-} being falling propagation delay. The rising and falling half-periods are

$$T^{+/-} = \frac{(V_{\mathrm{high}} + \mathrm{SR}^{+}t_d^{+}) - (V_{\mathrm{low}} - \mathrm{SR}^{-}t_d^{-})}{\mathrm{SR}^{+/-}} \tag{3.6}$$

Substituting (3.4) and (3.5) into (3.6) and summing both half-periods we get for a symmetrical waveform ($\mathrm{SR}^{+} = \mathrm{SR}^{-}$) the following oscillation period

$$T = 2\left(RC\frac{I_{M5}}{I_{M1}} + t_d^{+} + t_d^{-}\right). \tag{3.7}$$

The frequency of oscillation is therefore dependent on the product of R and C as is the temperature dependence. The effect of the comparator delay can be compensated by increasing the value of C.

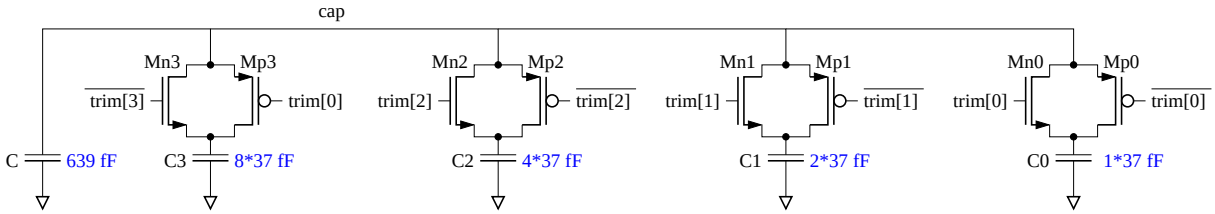


Figure 3.4: Trimming circuit.

The comparator delay portion of the oscillation period is dominated by t_d^- caused mostly by slewing of the *cmp1* node from saturation voltage of M_6 V_{ds6}^{sat} to the threshold of the second stage give by $V_{\text{DD}} - |V_{\text{THP}}|$, where V_{THP} is the threshold voltage of PMOS transistor M_8. This delay t_{slew} can be estimated as follows. Slewing starts when the input voltage of the comparator crosses threshold V_{low}. Around this operating point M_6 can be approximated by a corresponding transconductance g_{m6} that is charging a parasitic capacitance C_p of node *cmp1*. As the voltage on the capacitor v_{cap} continues to linearly decrease so does the current charging C_p given by $g_{m6}v_{\text{cap}}$. The slewing time can be computed by the following integral

$$V_{\text{DD}} - |V_{\text{THP}}| - V_{ds6}^{\text{sat}} = \int_0^{t_{\text{slew}}} \frac{g_{m6}v_{\text{cap}}}{C_p}\mathrm{d}t = \int_0^{t_{\text{slew}}} \frac{g_{m6}\text{SR}^- t}{C_p}\mathrm{d}t \tag{3.8}$$

Solving for t_{slew} leads to

$$t_d^- \approx t_{\text{slew}} = \sqrt{\frac{2(V_{DD} - |V_{THP}| - V_{ds6}^{\text{sat}})C_p}{g_{m6}\text{SR}^-}} \tag{3.9}$$

Equation (3.9) shows that to decrease the slewing delay of the comparator the parasitic capacitance C_p must be minimized and the transconductance g_{m6} must be maximized. The former can be done by minimizing M_8 for lower gate capacitance, the latter by increasing drain current of M_6 which is given by I_{M5}.

Design

The proposed waveform generator with 1 MHz frequency was designed in STMicroelectronics 180 nm BCD technology with supply voltage of 1.8 V. Values of the passive components were selected to be easily integrated on-chip: $R = 500\,\text{k}\Omega$, $C = 1\,\text{pF}$. For good linearity a MOM (Metal-Oxide-Metal) capacitor was selected together with N+ polysilicon resistor for good temperature behavior.

Since the on-chip resistors and capacitors have large process variations trimming is usually employed to put the resultant frequency within a given specification. This can be accomplished by trimming either the resistor or the capacitor. The drawback of the resistor trimming is a change of triangle amplitude with trimming code. This may not be an issue when only a digital output is used but may pose a problem for subsequent processing when the triangular output is used as well, e.g. in DC-DC converters. For this reason the capacitor trimming was selected and the trimming circuit can be found in Fig. 3.4. The main capacitor C is accompanied with four binary scaled capacitor $C_0 - C_4$ which can be switched parallel to the main capacitor using transfer gates controlled by trimming bits.

The unit capacitance of the trimming capacitors and therefore the trimming range was selected according to the technology spread of the oscillation period and is about ± 30 %. The remaining value of the main capacitor C was then reduced by the parasitic capacitances of the transistors connected to the *cap* node, e.g. drain/source capacitances of M_{n0-3}, M_{p0-3}, M_2, M_3 or gate capacitance of M_6. This correction makes 65 fF.

The typical bias current as well as all the branch current through M_{b1}, M_{b2}, M_1 or M_5 is 1 μA. In order to stabilize the amplitude of the triangle waveform the bias current should have inverse temperature and process dependency as the resistor R. This is not a problem as the bias current I_{bias} distributed across the chip is usually derived from a trimmed bandgap voltage V_{bg} and a reference resistor R_{bias} as $I_{\text{bias}} = V_{\text{bg}}/R_{\text{bias}}$. If R_{bias} is the same resistor type as R then the triangle waveform amplitude is a scaled copy of the bandgap voltage.

The transistor dimensions are summarized in Tab. 3.2. The gate lengths of the transistors

Table 3.2: Transistor dimensions.

Component	**Width / Length**
M_{b1}, M_{b2}, M_1, M_5, M_{10}, M_{12}	2 μm / 2 μm
M_{b3}, M_4, M_9	1 μm / 4 μm
M_2	2 μm / 0.18 μm
M_3	1 μm / 0.18 μm
M_6, M_{11}, M_{13}	2 μm / 0.56 μm
M_7	1 μm / 0.18 μm
M_8, M_{d1}, M_{d3}	1 μm / 0.24 μm
M_{d2}, M_{d4}	0.7 μm / 0.24 μm
M_{n0-3}	0.7 μm / 0.18 μm
M_{p0-3}	1 μm / 0.18 μm

operating as switches were kept at minimum of the given technology at 180 nm. However, the transistors operating as current sources have gate lengths in the order of micro meters for high output resistance and good matching. The former has impact on the triangular waveform linearity and the latter on statistical duty cycle variations.

Figure 3.5 shows a layout of the proposed circuit (excluding reference generators of Fig. 3.3b). The circuit takes 0.0126 mm^2 out of which the largest part is taken by the capacitors and the resistor.

Simulation results

The designed circuit has been simulated in Eldo simulator from Mentor Graphics. The bias current was derived from a constant voltage source and an N+ polysilicon resistor to simulate chip bias current behavior and to stabilize amplitude of the triangle waveform across corners and temperature.

The simulated transient waveforms of the main circuit including the reference generators are depicted in Fig. 3.6a. It can be seen that the triangular waveform generated on the *cap* node exceeds the ideal boundaries given by the reference voltages V_{low} and V_{high} (waveforms *low* and *high*). This is caused by the propagation delays of the comparator t_d^+ and t_d^- as discussed in Section 2. The origin of the propagation delays can be seen on the depicted waveforms of internal nodes of the comparator *cmp1* and *cmp2* which show slew rate

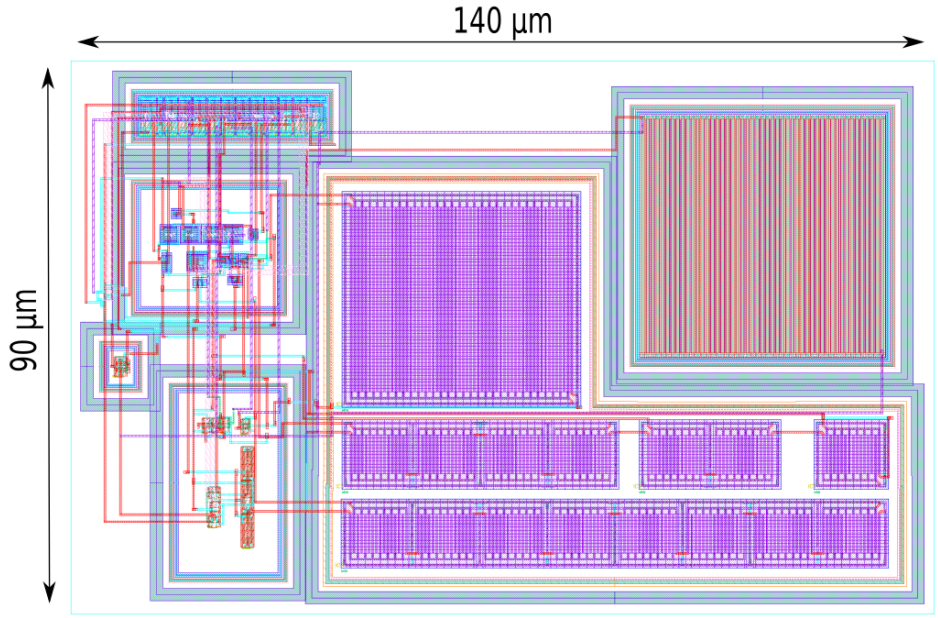
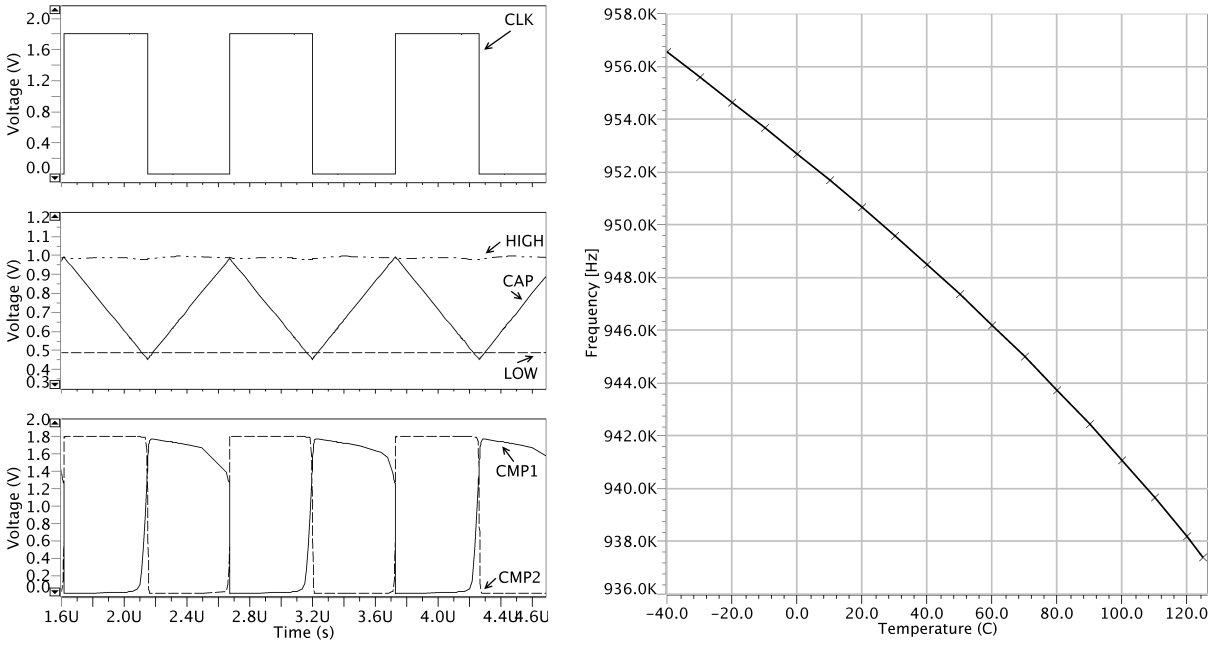


Figure 3.5: Layout of the circuit.



(a) (b)

Figure 3.6: Simulation results: (a) transient simulation, (b) frequency temperature variation.

limitation caused by the designed constant current of M_5 and M_9. The square waveform output *clk* is then produced by reshaping the signal on node *cmp2* by the digital CMOS buffer.

The oscillating frequency for a typical corner is 0.94 MHz, read from the waveforms t_d^+ is 3 ns and t_d^- is 34 ns out of which t_{slew} is about 28 ns. We can compare this result with

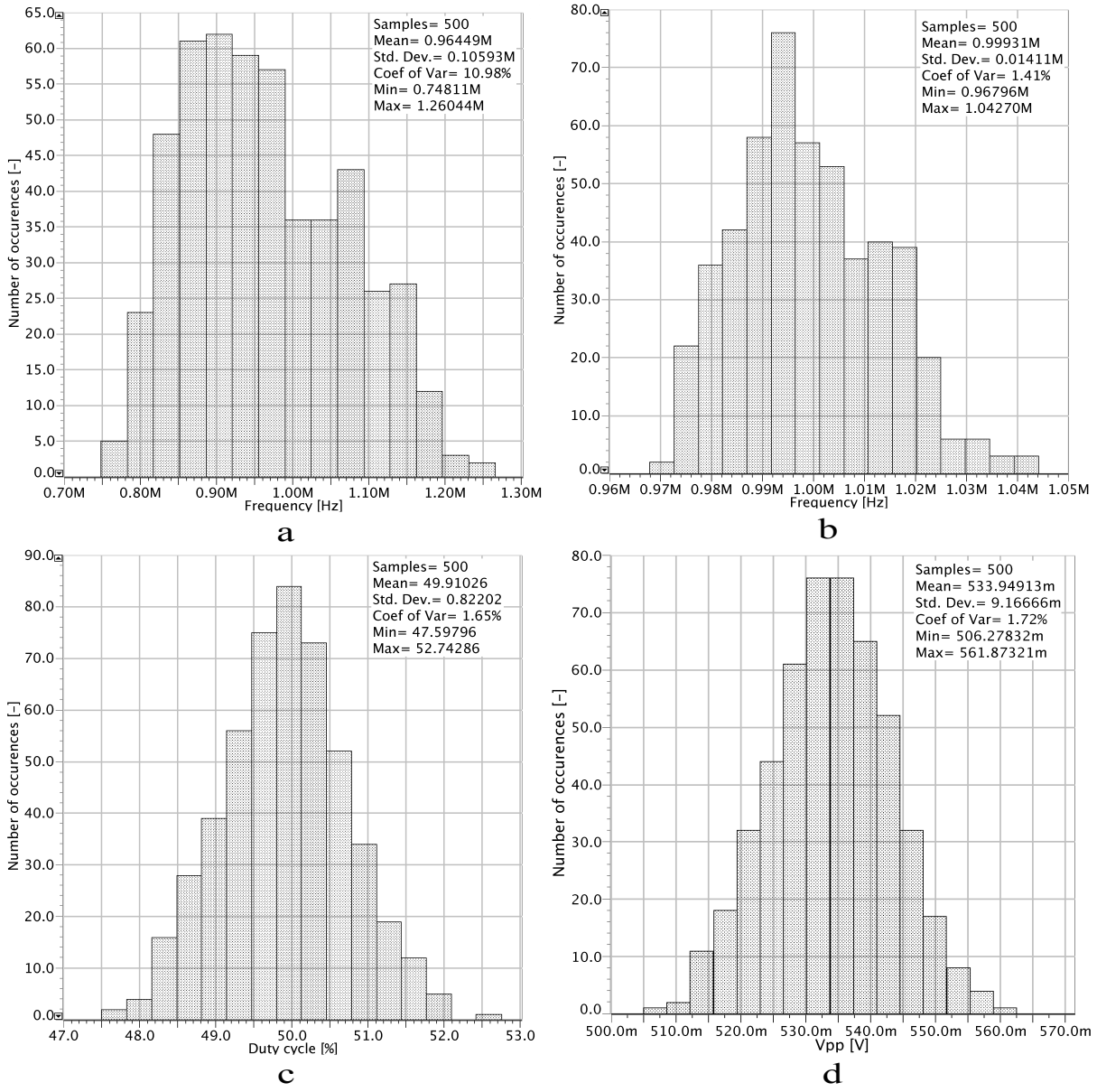


Figure 3.7: Monte Carlo analysis histograms: (a) Frequency before trimming, (b) frequency after trimming, (c) duty cycle, (d) peak-to-peak output voltage.

a theoretical value given by equation (3.9). Using (values from operating point analysis) $V_{DD} = 1.8\,\mathrm{V}$, $|V_{THP}| = 0.55\,\mathrm{V}$, $V_{ds6}^{\mathrm{sat}} = 0.19\,\mathrm{V}$, $C_p = 4.9\,\mathrm{fF}$, $g_{m6} = 18\,\mu\mathrm{S}$ and $\mathrm{SR}^- = 1\,\mathrm{V}/\mu\mathrm{s}$ we get theoretical value of t_{slew} equal to 24 ns which is in good agreement with the simulated value.

Variation of the oscillation frequency with temperature can be see in Fig. 3.6b. For the extended temperature range spanning from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ the total frequency variation is $\pm 1.05\,\%$ and the temperature coefficient is therefore $127\,\mathrm{ppm}/^{\circ}\mathrm{C}$.

The average current consumption of the generator core (w/o ref. gens. on Fig. 3.3b) is $4.1\,\mu\mathrm{A}$. This is equivalent to $7.38\,\mu\mathrm{W}$ at the respective supply voltage.

In order to evaluate process spread of the circuit a Monte Carlo (MC) analysis was run on top of the transient simulation. Further to assess the effectiveness of the trimming

method a transient sweep across all the trimming steps was simulated in each MC run and the value closest to the target value (i.e. 1 MHz in this case) was selected. This in fact simulates a real factory trimming.

Figure 3.7 shows histograms and statistical parameters of 500 runs of MC analysis. Results of oscillation frequency before trimming can be seen in Fig. 3.7a. The maximum deviation from the nominal frequency is 26 % and is caused by the process variability of sheet capacitance and sheet resistance in the given technology process. Figure 3.7b shows histogram of frequency after trimming. The maximum deviation is now 4.27 % from the nominal frequency.

Duty-cycle variation histogram is in Fig. 3.7c and its standard deviation is 0.82 %. This statistical variation of the duty-cycle is caused by the mismatches of current mirrors $M_{b3} - M_4$ and $M_{b2} - M_1$ and can be improved by enlarging the area of the transistors [41].

Figure 3.7d shows histogram of the peak-to-peak amplitude of the triangle waveform. As described above, the bias current was assumed to be derived from an ideal bandgap voltage reference and the same resistor type as resistor R. The amplitude of the triangle waveform is thus not affected by the process spread of the resistor (which is around $\pm 20\%$) and is given mostly by the mismatches of M_{b1}, M_5 and R.

3.3 Summary

The chapter presented triangular waveform generators suitable for use in switching DC-DC converters. After a brief presentation of state of the art solutions a new topolopy was presented.

A 1-MHz waveform generator based on the proposed topology was designed in STMicroelectronics 180-nm BCD technology consuming $7.38\,\mu$W and occupying only $0.0126\,mm^2$. The temperature and process stability of the oscillation frequency depends on the resistors and capacitors available in the given technology. The type of these elements can be selected to at least partially compensate for the temperature behavior of each other. In the presented design a temperature coefficient of 127 ppm/°C was achieved. To cope with the process spread a trimming is usually employed as was demonstrated.

Referring back to Tab. 3.1 it can be seen that the proposed topology has one of the best component count. Although no direct area comparison can be made (no data for of other solutions), this fact, together with the fact that it has limited matching critical transistors in the comparator (no differential pairs), means this solution requires less silicon area than the competing circuits.

4 Current Comparators

In a typical DC-DC converter the coil current is bounded by two limits. As shown in the block diagram in Fig. 1.3 and explained in the associated discussion the bottom limit is set by a zero crossing detector (ZCD). This detector triggers when the inductor current is about to reverse direction and turns off the driving MOS, thus effectively simulating a diode. The top limit is imposed by an over current detector (OCD, also known as over current protection – OCP) which terminates the switching cycle before the inductor current leaves values safe for operation of the converter.

This chapter gives an overview of various architecture of these current comparators and follows up with a development of a combined buck over-current/boost zero crossing detector.

4.1 Zero crossing detectors

As stated above the ZCD monitors the zero crossing of the inductor current. The sensing is done on a transistor that is turned on in the part of the switching cycle where the inductor current is decreasing towards zero. For buck converter this is on low-side transistor M_{LS} as can be seen in Fig. 4.1a.

As the voltage drop on M_{LS} is proportional to I_L a voltage comparator can be used to sense the inductor current reversal. Fig. 4.1b shows the associated current and voltage waveforms. The voltage drop when M_{LS} is turned on is

$$V_{\mathrm{LX}} = -R_{\mathrm{dson}} I_L, \tag{4.1}$$

where R_{dson} is on-state resistance of M_{LS}.

In ideal case, the ZCD triggers exactly at zero current and immediately M_{LS} turns off preventing I_L to go negative. However, in real circuits, due to non-idealities the turning off point will vary around the zero causing some additional power loss in the system. The analysis of this was carried out in [6] and its qualitative findings are depicted in Fig. 4.1c. As can be seen, late M_{LS} turn-off (turning off when I_L is already negative) incurs higher extra power dissipation than early turn-off by an equivalent value. For this reason it is customary to target ZCD threshold not at zero, but at a negative voltage value (positive current) so that including all delays and offsets the turn off point of M_{LS} is before or around zero.

One of the non-idealities that impact the turn off point is the input offset of the ZCD comparator. Because R_{dson} can be very low, even below 100 mΩ, the input offset voltage of the comparator can cause significant inductor current crossing error

$$I_{L\mathrm{err}} = \frac{v_{\mathrm{io}}}{R_{\mathrm{dson}}}, \tag{4.2}$$

where v_{io} is the input offset voltage of the zero crossing comparator.

Another important parameter of ZCD is its propagation delay t_{pd}, i.e. time between the input of the comparator crossing the defined threshold and the comparator output changing

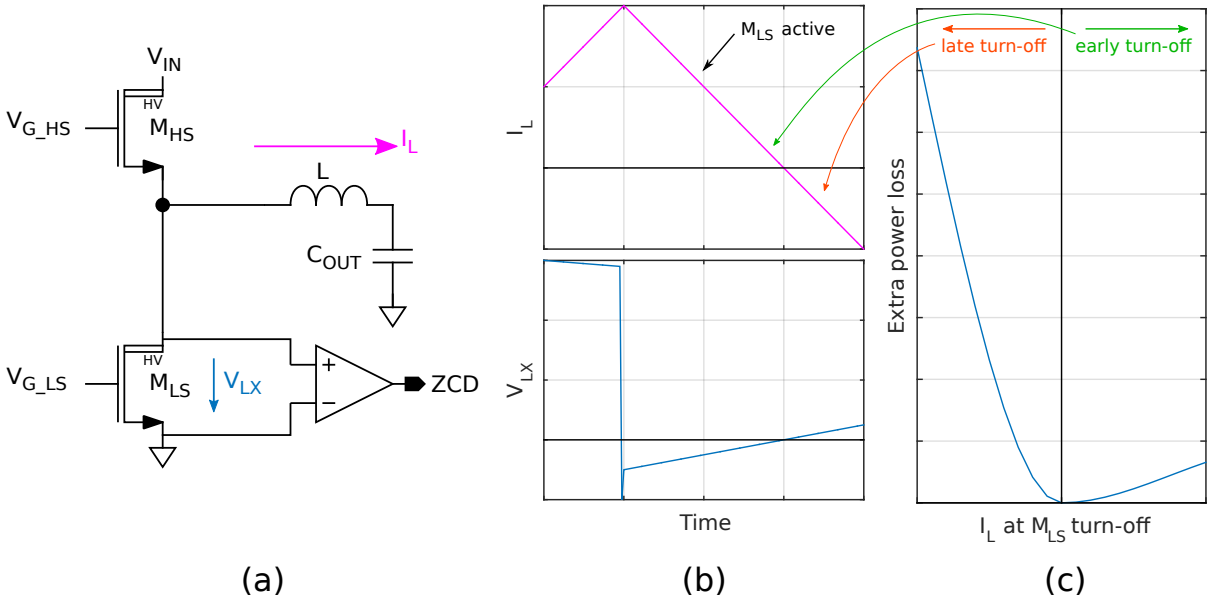


Figure 4.1: ZCD sensing: (a) block diagram and (b) its waveforms (not to scale), (c) incurred power loss due to non-ideal zero crossing (trend only).

value. The low value of propagation delay is important because during this time (and also during propagation delays of control logic and drivers) the inductor current drops by

$$\Delta I_{\mathrm{L}} = \frac{V_L}{L}(t_{\mathrm{pd\_zcd}} + t_{\mathrm{pd\_logic}} + t_{\mathrm{pd\_drv}}), \tag{4.3}$$

where V_L is the voltage across the inductor (equals V_{OUT} for buck converter) and $t_{\mathrm{pd\_zcd}}$, $t_{\mathrm{pd\_logic}}$, $t_{\mathrm{pd\_drv}}$ are the propagation delays for the ZCD, control logic and drivers, respectively. Given that $t_{\mathrm{pd\_logic}}$, $t_{\mathrm{pd\_drv}}$ consists mostly of propagation delay of logic gates, $t_{\mathrm{pd\_zcd}}$ dominates the total delay.

As was already said, this delay can be compensated by setting comparison threshold to trigger at $I_L > \Delta I_{\mathrm{L}}$ so that the M_{LS} turn off point is still in positive currents. However, this works only in cases when the peak inductor current is larger than ΔI_{L}, otherwise I_L will be already at negative value by the time the propagation delay elapses. This is a problem for low duty cycles and high switching frequencies, it is therefore desirable to lower the propagation delay as much as possible.

Comparator topologies

Similar to current sensor amplifiers in Chapter 2, the most common solution used in ZCD comparators is to employ common gate amplifier in the first stage. In [43, 44] a common gate with a current source load is used. This principle is depicted in Fig. 4.2a. The input differential voltage is sensed by sources of M_1 and M_2. Together with M_5 and M_6 (which work as current source load) they form the first amplification stage. Second stage is formed by transistors M_3 and M_7. Typically, gain of each stage can reach 40 dB or more, depending on technology and if cascoding is used (cascodes are not depicted for simplicity), therefore

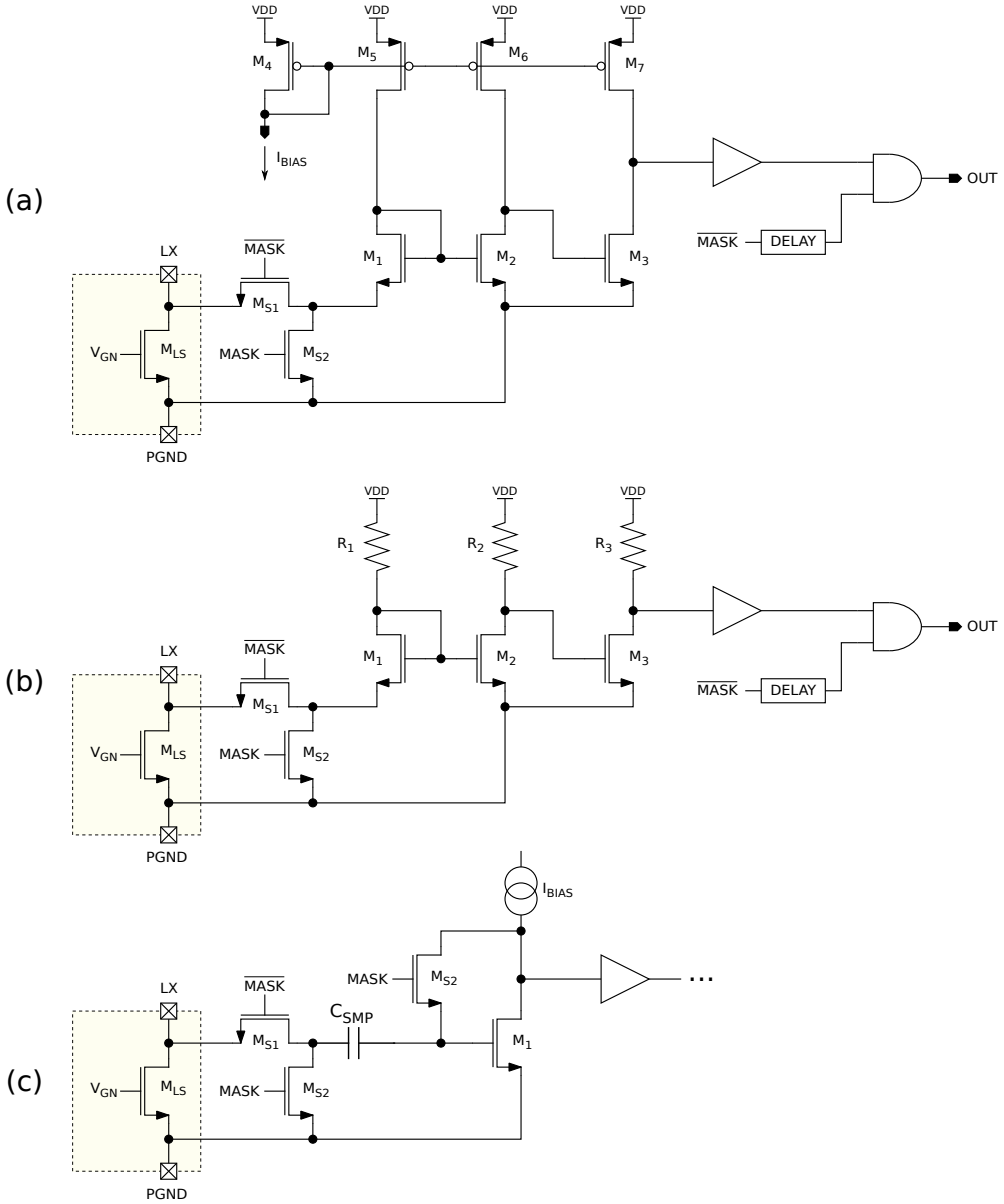


Figure 4.2: ZCD circuits: (a) basic common gate input comparator, (b) common gate with resistor load, (c) auto-zero comparator [42].

the signal at the output of the second stage has large enough swing to be picked by a digital buffer.

When M_{LS} is off and LX node is high, transistors M_{S1} and M_{S2} serve to mask the high voltage on LX and short the differential input of the comparator preventing from unequal stress on the matched transistors. M_{S1} has one other function, together with the current from M_5 it creates an offset in the switching threshold so that the comparator triggers earlier as explained above.

When the comparator is enabled/unmasked, it takes some time to settle to a correct value. Moreover, LX node may have not settled itself, thus the comparator may trigger prematurely. This would have disastrous effect on the performance of the switching converter

as M_{LS} would turn off just after it has turned on and I_L would have to discharge completely through body diode M_{LS}, i.e. causing huge power loss. To prevent this from happening, the ZCD output itself is unmasked with a delay. This delay can be as high as 20 ns (e.g. in [44]) or more.

It was shown in [45] that considering the same power consumption, having more stages with a smaller gain leads to a faster response than having all the required gain only in one stage. One way to achieve this is to replace the current source loads with resistors as in [46]. A version redrawn for buck converter is in Fig. 4.2b. The gain of one stage with resistor load R is

$$A_{1\mathrm{stg}} = g_m R = \frac{g_m}{I_D} R I_D = \frac{g_m}{I_D} V_R = \frac{g_m}{I_D}(V_{\mathrm{DD}} - V_{\mathrm{GS}}), \tag{4.4}$$

where g_m is transconductance of the amplification transistor, I_D is its drain source current, g_m/I_D its transconductance efficiency and V_R is the voltage drop on the resistor which is for the given case equal to supply voltage V_{DD} minus the gate source voltage of the transistor V_{GS}. Given that for a transistor operating in strong inversion the transconductance efficiency can be around 10 V^{-1} and for V_{DD} of 1.8 V[1] the gain of a simple resistor loaded stage can be over 20 dB. Using two of these stages usually doesn't make enough gain to drive its output up to supply rails for a sufficiently small input voltage, thus coupling to the next stage is not trivial as disproportion of equilibrium operating points leads to a PVT unstabilized offset.

As was stated, input offset is an important parameter in design of ZCDs. One way to lower it is to make the matched devices large as the mismatch is inversely proportional to device area [41]. However, larger devices have larger parasitic capacitances which negatively impacts propagation delay. For this reason some authors use calibration or auto-zero techniques to improve the input offset.

One such an example presented in [42] is depicted in Fig. 4.2c. The circuit works in two phases. When M_{LS} is off and MASK $= 1$ the circuit is in auto-zero phase. M_1 is diode connected through M_{S2} and its gate-source voltage V_{GS} is sampled on capacitor C_{SMP}. When M_{LS} is on and MASK $= 0$ the circuit operates in comparison mode. The left side of the capacitor is then connected to LX and M_1 together with its current source load forms a gain stage.

Since for zero input voltage the output of the stage equals V_{GS} (as it was the sampled point) coupling to the digital gate is not ideal and can cause PVT dependent systematic offset. This drawback is removed in [47], where the digital gate is replaced with an auto-zeroed comparator. Moreover, the current source load is replaced by a resistor for faster propagation delay.

4.2 Over current detectors

As introduced in the introduction, one of the protection mechanism in switching DC-DC converters is the over current detector. This detector senses the coil current (usually just on the power transistor causing increase of the current – e.g. high side for buck converter) and compares it with a reference current. When the sensed current crosses the given threshold the over current signal is triggered and the control logic of the converter terminates the active phase.

[1] Operating voltage for low voltage components in a typical 180 nm technology.

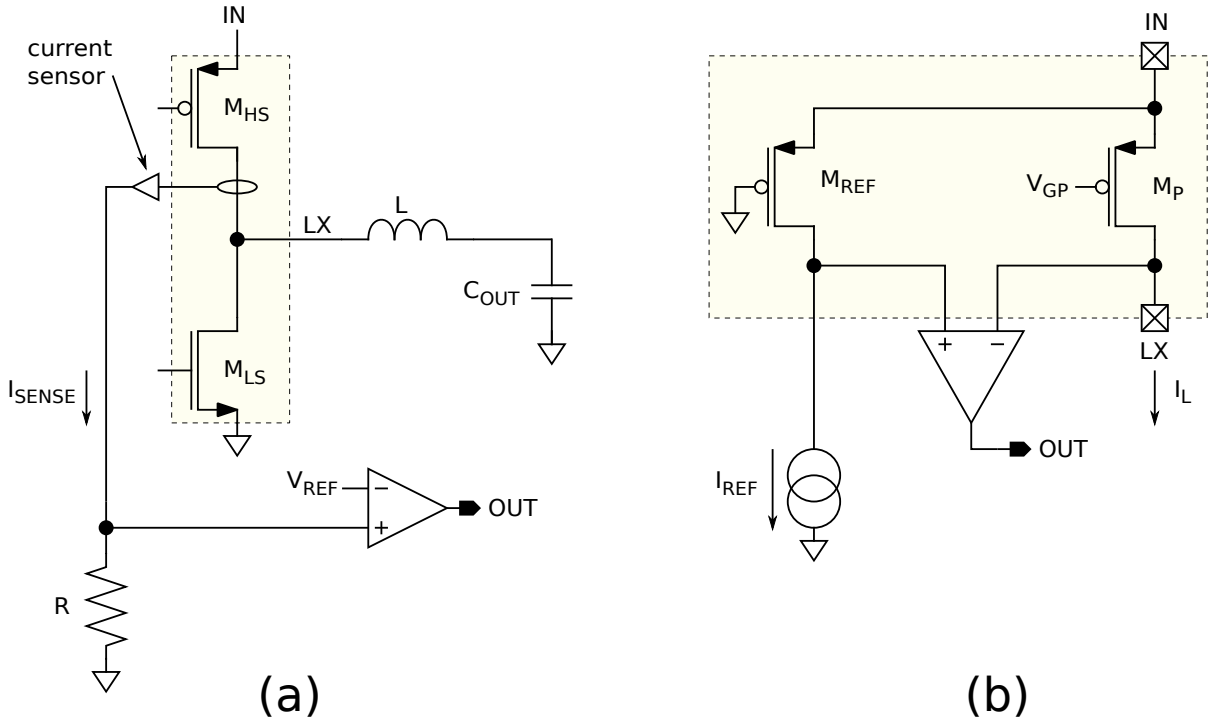


Figure 4.3: OCD architectures: (a) using current sensor, (b) comparing voltage on copy MOS.

The requirements for propagation delay and start-up time are similar to ZCD comparators. The worst case happens when I_L crosses the threshold just after the high side transistor (for buck converter) is enabled. The propagation delay then cannot be compensated by additional offset and it must be low enough that the current rise of I_L does not cause any damage before thee OCD has a chance to trigger.

On the other hand, the requirement for input offset voltage is not so stringent as the comparison threshold tends to be in the range of amperes. As explained on example in Chapter 2, given R_{dson} of 100 mΩ and offset voltage of 1 mV will induce inductor current error of 10 mA which is much smaller than thresholds normally used in OCD comparators.

There are two architectures of OCD comparators. One is as depicted in Fig. 4.3a. It uses a current sensor[2] which outputs a scaled copy of the current through the power MOS I_{SENSE}. In [48] and [49] this current is converter to a voltage on a resistor R and then compared to a voltage reference V_{REF} with a standard voltage comparator.

In [50] a current comparator is used instead of the voltage one to save its power consumption.

Another architecture can be found in Fig. 4.3b. A reference current I_{REF} is used to create voltage drop on a copy MOS M_{REF}. A comparator is then used to compare this reference voltage with a voltage drop on the power MOS M_P created by the inductor current. This solutions was used e.g. in [51]. For the comparator structures similar to the ones found in Fig. 4.2 can be used.

[2]For current sensors see Chapter 2.

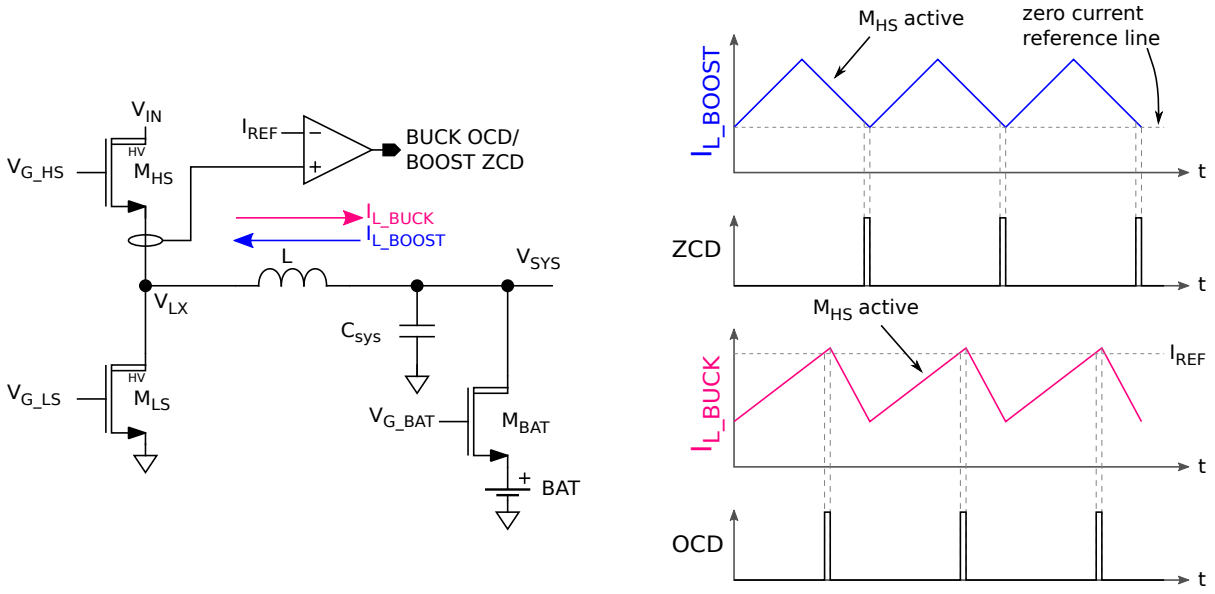


Figure 4.4: Battery charger system block diagram

4.3 Dual purpose HV buck OCD/boost ZCD for portable battery chargers

The increasing battery capacities in portable devices, such as smartphones, place higher requirements on battery charging chips to charge the battery in the shortest time possible. One way to provide the required power through the conventional cables and connectors, such as USB, is to use high input voltage [8]. Step-down DC-DC converter (buck) is then used to convert the high input voltage to the levels suitable for the battery. Additionally, the devices often need to power external accessories. In that case, the battery charger is configured as a boost converter to step the battery voltage up to the required voltage [52].

Such a system is depicted in Fig. 4.4. Transistors M_{HS} and M_{LS} form the switching power half-bridge generating system voltage V_{SYS} when the input voltage is connected. When the external input voltage is not present the system voltage is provided by the battery which is connected to the system voltage through transistor M_{BAT}. This provides additional control for battery charging and allows battery disconnection [52].

For the given system, OCD in buck as well as ZCD in boost mode both sense the current through the high side MOS M_{HS} (ZCD in buck and OCD in boost is sensed on M_{LS}). It is therefore desirable if both detectors share the same circuitry. This is especially true for high voltage systems where the required high voltage devices, such as DMOS transistors, take a lot of silicon area.

Although, as has been seen in the previous section, there has been development in both OCD's and ZCD's no combined solution has been presented so far. This section presents such a solution of a combined detector for portable battery chargers.

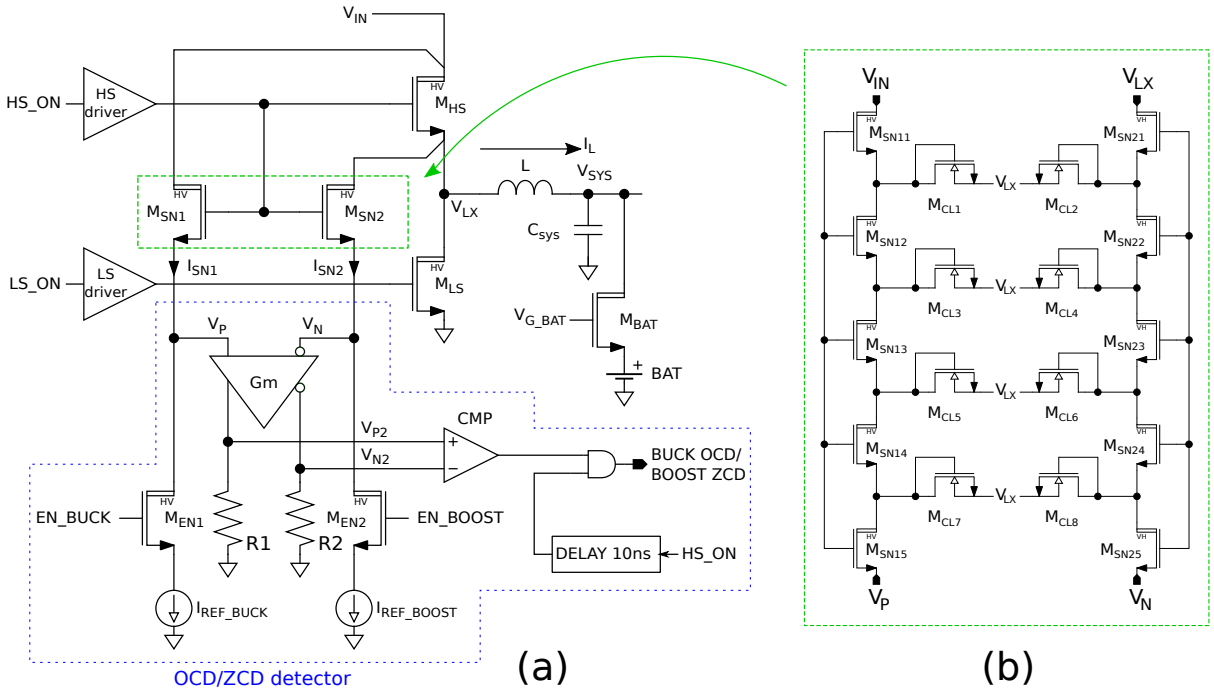


Figure 4.5: (a) Block diagram of the system with the proposed detector, (b) serial connection of copy MOS transistors for higher copy ratio.

Design

The architecture of such a detector is proposed in Fig. 4.5a. To support high voltage operation the power half-bridge M_{HS} and M_{LS} is composed of DMOS transistors. When M_{HS} is turned on its V_{DS} voltage is equal to $R_{\mathrm{DSon}}I_{\mathrm{L}}$, where R_{DSon} is the resistance of the high side MOS in on-state and I_{L} is the the coil current flowing from V_{in}. M_{SN1} and M_{SN2} are sense MOS transistors of the same kind as M_{HS} [10]. By having their width N times smaller than the width of the power MOS $W_{\mathrm{SN1,2}} = W_{\mathrm{HS}}/N$ their on-state resistance equals $R_{\mathrm{DSon\_SN1,2}} = NR_{\mathrm{DSon}}$. Therefore the voltage between V_{P} and V_{N} is

$$V_{\mathrm{P}} - V_{\mathrm{N}} = R_{\mathrm{DSon}}\left(I_{\mathrm{L}} - NI_{\mathrm{REF}}\right), \tag{4.5}$$

where $I_{\mathrm{REF}} = I_{\mathrm{SN1}} - I_{\mathrm{SN2}}$ is the difference of the currents flowing through M_{SN1} and M_{SN2}. This voltage difference is then pre-amplified and shifted to a low voltage domain by a transconductance stage Gm and resistors R_1 and R_2. For a source driven transconductance stage the amplified differential voltage is given as

$$V_{\mathrm{P2}} - V_{\mathrm{N2}} = \frac{g_m R_{1,2} R_{\mathrm{DSon}}\left(I_{\mathrm{L}} - NI_{\mathrm{REF}}\right)}{1 + g_m N R_{\mathrm{DSon}}}, \tag{4.6}$$

where g_m is the transconductance of the Gm amplifier. Using pre-amplifier optimizes propagation delay [45] and alleviates precision requirements on the subsequent stages. The final decision is taken by the comparator CMP and its output is then masked by a delayed high side enable signal HS_ON. The masking avoids any unwanted glitches when M_{HS} is not conducting and the additional 10 ns delay during the start of the operation prevents false triggering when the circuit is being powered-up.

When the device operates in buck mode EN_BUCK signal is high, M_{EN1} is on and I_{REF} is equal to $I_{\mathrm{REF\_BUCK}}$ which sets the OCP threshold to $I_{\mathrm{L}} = NI_{\mathrm{REF\_BUCK}}$.

Conversely, when the device operates in boost mode EN_BOOST is high, M_{EN2} is on and I_{REF} is equal to $-I_{\mathrm{REF\_BOOST}}$ which sets the ZCD threshold to $I_{\mathrm{L}} = -NI_{\mathrm{REF\_BOOST}}$.

As written before, although the ZCD is supposed to trigger at zero current setting some small threshold even for zero crossing detection allows compensating for the delay of the system between the crossing of the threshold and the actual turning off of the power MOS. The value of this threshold can be written as

$$I_{\mathrm{L\_ZCD}} = \frac{V_{\mathrm{IN}} - V_{\mathrm{SYS}}}{L} t_d, \tag{4.7}$$

where t_d is the time delay that needs to be compensated. Note that in boost mode V_{IN} is in fact output voltage higher than V_{SYS}. In practice, the worst case operating conditions leading to the highest threshold are used.

The higher the power MOS to sense MOS ratio N the lower the reference current I_{REF} can be for a given threshold. It is therefore desirable to maximize the ratio N in order to save power. When the ratio N gets high the requirement for the width of the sense MOS transistors can become so small that narrow channel effects of the transistors can compromise matching accuracy or it may even violate the minimum channel width constraint in a given technology.

If that is a case the ratio N can be made higher by connecting several sense MOS devices in series as depicted in Fig. 4.5b. As the power transistors, as well as the sense transistors, work in linear region, serial connection of $M_{\mathrm{SN11}} - M_{\mathrm{SN15}}$ has equivalent R_{DSon} equal to the sum of individual transistors

$$R_{\mathrm{DSon\_SN1}} = \sum_{i=1}^{5} R_{\mathrm{DSon\_SN1}i} \tag{4.8}$$

and similarly for R_{DSon} of the second branch $R_{\mathrm{DSon\_SN2}}$. The sense transistors being DMOS can sustain high voltages between drain and source. However, during high side/low side commutation, the gate-source voltages can swing beyond the safe operating area of the transistors. To prevent this from happening the nodes in between the sense transistors are clamped against the switching node V_{LX} using transistors $M_{\mathrm{CL1}} - M_{\mathrm{CL8}}$.

The details of the transconductance stage Gm and reference current sources are shown in Fig. 4.6. Transistors $M_1 - M_4$ form symmetrical source driven differential stage [53] while the drift MOS transistors $M_5 - M_7$ provide high voltage protection. As the structure is symmetrical, with zero input differential voltage the input currents (i.e. source currents to M_1, M_3 and M_2, M_4) are equal, thus they do not influence the threshold of the detector as, according to eq. 1, only the difference in I_{SN1} and I_{SN2} matters.

When the high side is turned on and the gates of copy MOS transistors are pulled up the sources of $M_1 - M_4$ get pulled up as well and the transconductance stage starts to operate. The symmetry of the Gm stage ensures that any spikes and glitches caused by charging of the parasitic capacitors are symmetric and the resulting output differential voltage is zero.

The reference currents are generated using current mirrors $M_8 - M_9$ and $M_{10} - M_{11}$ from a bias current I_{REFB} which supplies only the current mirror active in the given mode using a pair of switches $M_{12} - M_{13}$. The current mirror ratios are set according to the desired thresholds of the detector. The drift MOSes M_{EN1} and M_{EN2} again provide high voltage protection.

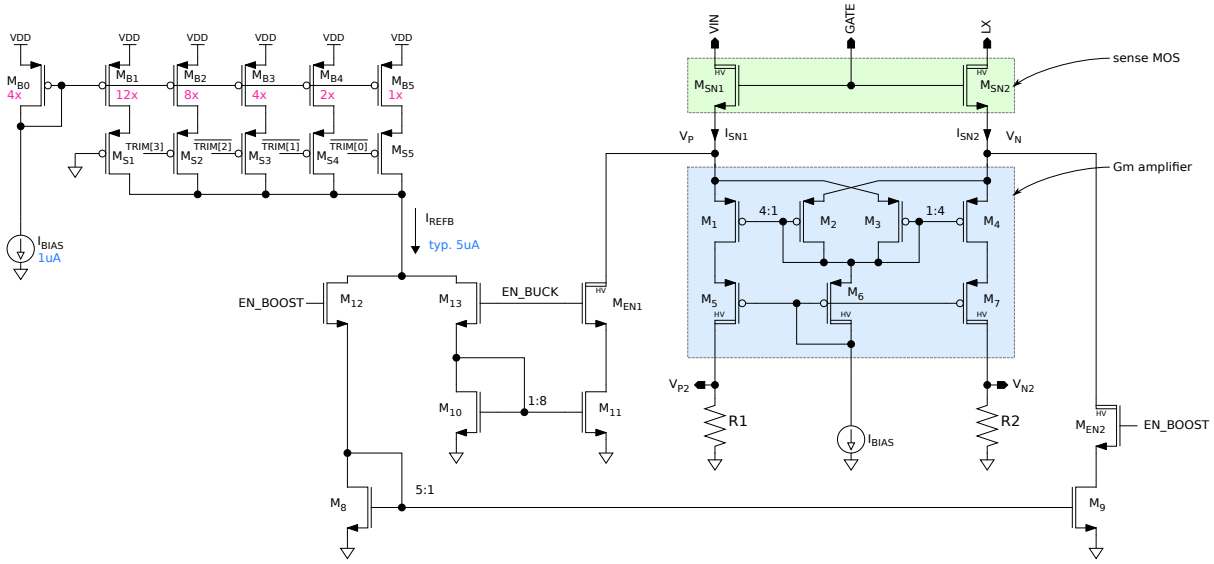


Figure 4.6: Schematic of the Gm amplifier and reference current sources.

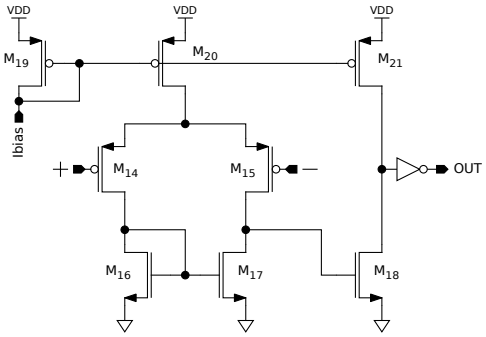


Figure 4.7: Schematic of the comparator CMP.

The reference bias current I_{REFB} is trimmed to compensate for any offset in the detector or mismatch between the sensing and power transistors. The trimming circuit is depicted in Fig. 4.6 and consists of a binary scaled current mirror $M_{B0} - M_{B5}$ whose outputs are switched using transistors $M_{S1} - M_{S5}$. The typical output value is 5 μA with zero trimming (combining currents from M_{B1} and M_{B2}). The trimming range spans from 3 μA to 6.75 μA which corresponds to -40% and +35%, respectively, with trimming step of 5%.

The comparator CMP is depicted in Fig. 4.7 and is a classic two gain stage circuit followed by an inverter to fully recover the digital signal.

Results

The design was layouted by and realized in STMicroelectronics using 0.18 μm BCD technology as part of the high voltage dual phase switching battery charger with each phase using the proposed detector. Microphotograph of the die together with the layout of the detector can be seen on the in Fig. 4.8a. The detectors are located close to the power transistors on the right.

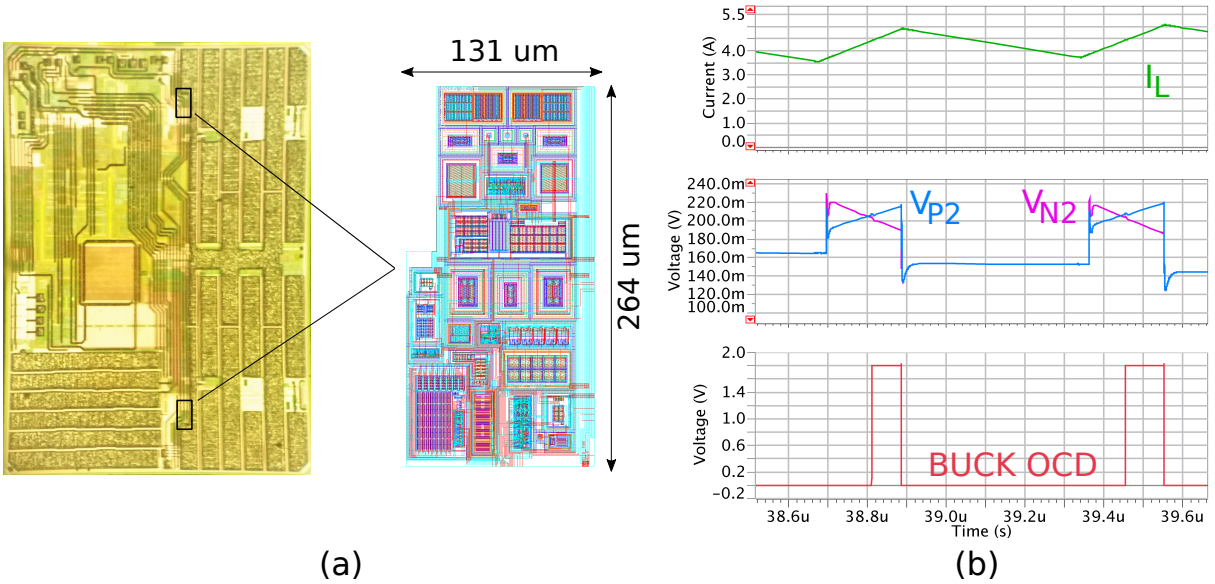


Figure 4.8: (a) Microphotograph of the chip and the layout of the detector (courtesy of STMicroelectronics), (b) transient simulation results in OCD mode.

The R_{DSon} of the high-side transistor M_{HS} is 30 mΩ and the power MOS to sense MOS ratio N is 10^5. This high ratio was realized utilizing five sense MOS transistors in series as depicted in Fig. 4.5b.

The detector occupies 0.035 mm^2 (excluding the area of sense MOSes as they are integrated with the high side power MOS for better matching) of silicon area and consumes 1.2 mW when operated from 12 V input supply voltage with a propagation delay of 24 ns.

The threshold of the overcurrent detector in buck mode was set typically at 4 A. The threshold of the zero crossing detector in boost mode was chosen to compensate any delays and mismatches in the system and the detector itself. Assuming minimum system voltage of 3 V, maximum boost output voltage of 5.2 V, 1 μH coil and total system propagation delay of around 35 ns we get (according to Eq. 4.7) around 77 mA. Including margin for mismatched and process variations the threshold was set to 100 mA.

Fig. 4.8b shows the transient simulation results of the detector in buck OCD mode, the output of the amplifier V_{P2} and V_{N2} and the digital output of the detector. The exact threshold was set using R3D mesh analysis software [4] as the precision of standard post-layout extracted simulation as in Fig. 4.8b is not sufficient in the given technology.

The design was manufactured, trimmed and measured on the bench. Fig. 4.9 shows the measured waveforms of the of the coil current and buck OCD/boost ZCD output. As marked with the cursors the thresholds of the detector are 4.06 A and 104 mA for buck OCD and boost ZCD, respectively.

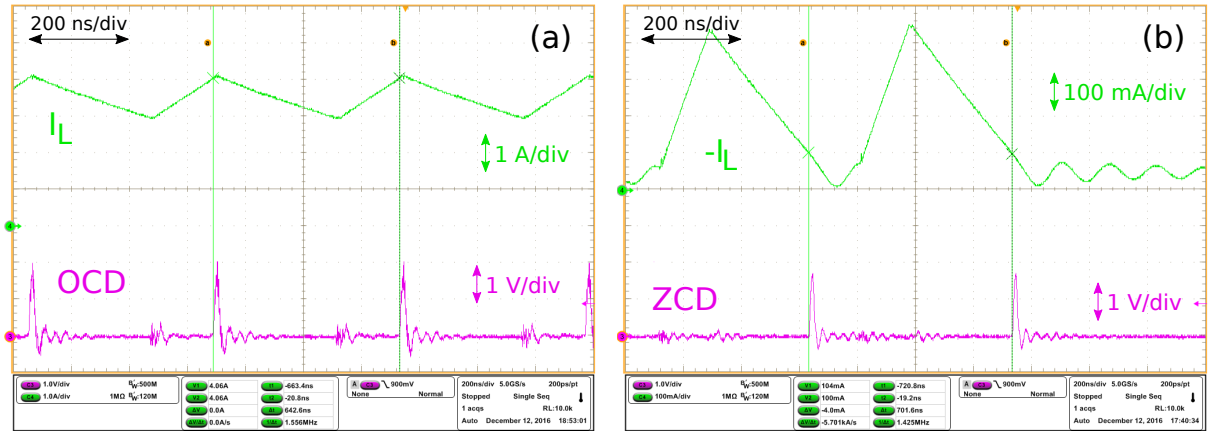


Figure 4.9: Oscilloscope screenshot of the detector operation in: (a) buck mode, (b) boost mode.

4.4 Overcurrent detector with built-in reference

Since the overcurrent detector (OCD) senses the immediate value of the current it must have low propagation delay and therefore consumes a lot of current. For low power converters operating in PFM or pulse skipping mode (low current load) this can become a significant source of power consumption. For this reason when ultra low power operation is necessary the OCD block is normally powered off and is started only for the duration of the active pulse when the current in the coil is increasing.

In ultra low power converters (in the range of μA or less total power consumption) the reference going into the OCD is very low (sub μA) and therefore it takes quite some time for the OCD to settle to the correct threshold at the begging of the switching pulse. Moreover sudden biasing the whole OCD block causes kickback noise through the current bias to the bias distribution block and because of its low power consumption it settles quite slowly compromising precision of other blocks on the chip.

This section presents a solutions that solves this problem using an overcurrent detector employing comparator with built-in reference.

Architecture

The block diagram of the overcurrent detector can be found in Fig. 4.10. Similarly to Fig. 4.3a it uses a current sensor to create a scaled copy of the current flowing through the high side power MOS I_{HS}. This current is then converted to voltage on resistor R_0. A cascade of simple transistor-resistor amplification stages follow (there can multiple of stages, minimally one). When the voltage on R_0 crosses a threshold voltage of M_1, M_1 starts conducting pulling its drain low. This in turn triggers the second stage and so on. At the end of the cascade of the stages the total amplification factor is high enough to use a series of simple logic invertes to shape the signal into final digital form.

The threshold current of the proposed circuit is given by

$$I_{\mathrm{HS\_THR}} = \frac{1}{k}\frac{V_{\mathrm{GS}}^{M1}}{R_0}, \tag{4.9}$$

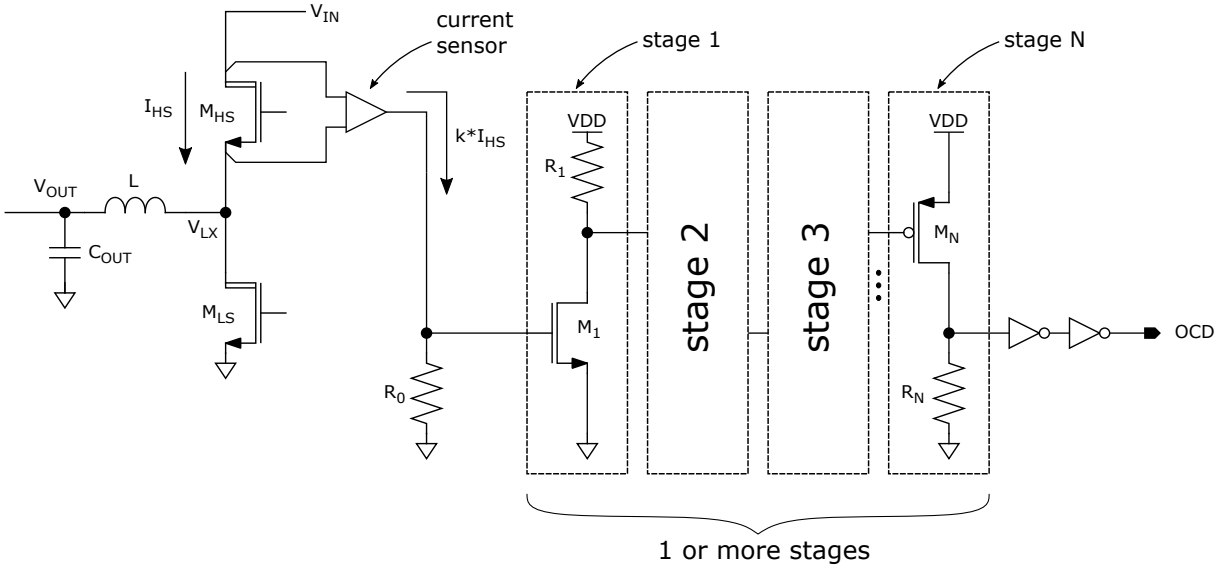


Figure 4.10: Block diagram of the circuit.

where k is the scale factor of the current sensor and V_{GS}^{M1} is the gate source voltage of M_1 at the threshold. This is in turn, using the square-law model, given by

$$V_{\mathrm{GS}}^{M1} = V_{\mathrm{TH}} + \sqrt{\frac{2I_{D1}L_1}{\mu C_{\mathrm{OX}} W_1}}, \tag{4.10}$$

where μ and C_{OX} are the usual model parameters, W_1 and L_1 are the width and length of the transistor, respectively. The drain current I_{D1} is current at which the second stage triggers V_{GS}^{M2}/R_1 which is approximately V_{TH}^{M2}/R_1, i.e. with each stage the small differences of threshold voltage and actual V_{GS} makes smaller and smaller influence on the threshold of the OCD (this difference is divided by the gain of the preceding stages). After several stages even the uncertainity of the inverter threshold observing the output of the last stage is negligible and so the threshold is in the first order independent on the supply voltage.

The temperature dependence of the threshold according to eq. 4.9 depends on V_{GS}^{M1} and R_0. By using appropriate resistor type or a combination of different resistor types the temperature variation of V_{GS}^{M1} can be compensated.

Using simple amplification stages with low impedance nodes a very low propagation delay can be achieved.

Design

An implementation of the aforementioned architecture was designed for use in a power management SoC for embedded processors. It features 4 different buck converters with different output current capability and therefore different overcurrent limit settings. To save design time a single buck converter and consequently single OCD instance was designed with configurable threshold settings. The configuration bits would then be set by metals on top level of the chip.

One of the target application for the SoC are battery operated systems. The converters thus need to have ultra-low power mode and be ready to support high current for when

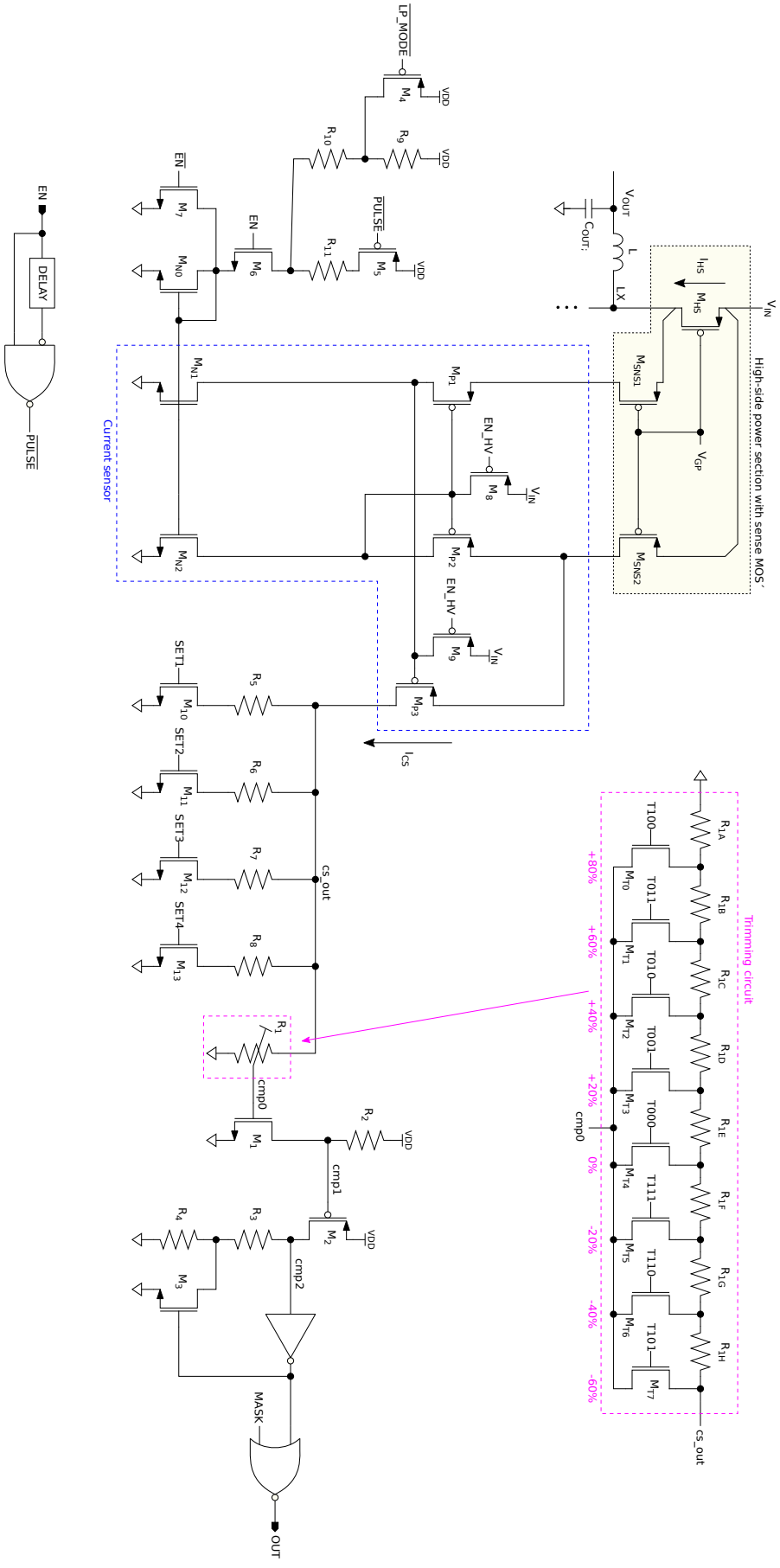


Figure 4.11: Example implementation of the proposed circuit.

the processor system wakes up. In order to support these very low quiescent currents all the circuits that do not operate should be shut down. This applies to the OCD as well as it should consume current only when the high side switch is turned on. The primary concern is therefore fast start-up time.

The schematic of the circuit is in Fig. 4.11. M_{HS} is the high side power PMOS and M_{SNS1} and M_{SNS2} are two sense/copy MOSes as explained in Chapter 2. Having also M_{SNS1} compensates for the systematic mismatch caused by the input current of the amplifier.

The current sensor is formed by M_{P1}–M_{P3} and M_{N1}–M_{N2}. It is a standard configuration as described in Fig. 2.3 and in the associated discussion. The maximum value of the supply voltage is 5.5 V so it can be handled with standard 5 V components available in the given technology and no high voltage cascoding is necessary.

As no precise sensing is required for overcurrent detection the circuit can get away with a relatively small open loop gain of 40 dB. This can be achieved even without any standard voltage cascodes. Making the current sensor simple allows for high bandwidth of around 65 MHz with a typical bias current of 5 µA through each of M_{N1} and M_{N2}.

In order to support the aforementioned fast start-up time a resistor bias scheme was adopted. The bias current is therefore given by

$$I_{\mathrm{bias}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{GS\_M0}}}{R_{10}}, \tag{4.11}$$

where V_{DD} is the supply voltage from the internal 1.8 V regulator and $V_{\mathrm{GS\_M0}}$ is the gate-source voltage of transistor M_0. A resistor R_{10} of an appropriate type was used to ensure that all the PVT variation doesn't cause the current sensor to work inappropriately.

When the converter enters bypass mode the high side power switch is turned on for its entire duration and the same applies to the OCD. In order to lower the total current consumption in this mode a resistor R_9 is put in series with R_{10} to lower the bias current from the default 5 µA to about 1 µA. The total consumption in this mode is then roughly 3 µA.

In order to push down the start-up time even more a small kick to the biasing circuit is implemented. This is accomplished by switching R_{11} in parallel with R_{10} (or $R_9 + R_{10}$ in bypass mode) for a small time of 1 ns when the circuit is enabled.

The current sensor gain is 20 μA/A, i.e. for each 1 A of inductor current 20 µA flows on the output of the current sensor I_{CS} through the transistor M_{P3}. Part of this current then flows through R_1 and a fraction of the developed voltage is sensed by the gate of M_1, which is a part of the comparator as described above. The comparator is using two amplification stages formed by M_1-M_2 and resistors R_2-R_4. Transistor M_3 along with resistor R_4 create a small hysteresis to quickly traverse the switching region of the following inverter.

Since M_1 takes the input signal from a fraction of voltage on R_1, trimming can be realized by switching different ratios of $V_{\mathrm{cmp0}}/V_{\mathrm{cs\_out}}$ as highlighted in the magenta box in Fig. 4.11. The trimming step is 20% so the expected precision at room temperature is around half of it, i.e. 10%.

In order to support different threshold settings different combinations of shunt resistors R_5–R_8 can be switched in parallel to R_1 to increase the thresholds. This makes threshold settings independent from trimming. The inductor current threshold of the circuit is then given as

$$I_{\mathrm{HS\_THR}} = \frac{1}{k}\frac{V_{\mathrm{GS}}^{M1}}{x_{\mathrm{trim}}}\left(\frac{1}{R_1} + \frac{SET_1}{R_5} + \frac{SET_2}{R_6} + \frac{SET_3}{R_7} + \frac{SET_4}{R_8}\right), \tag{4.12}$$

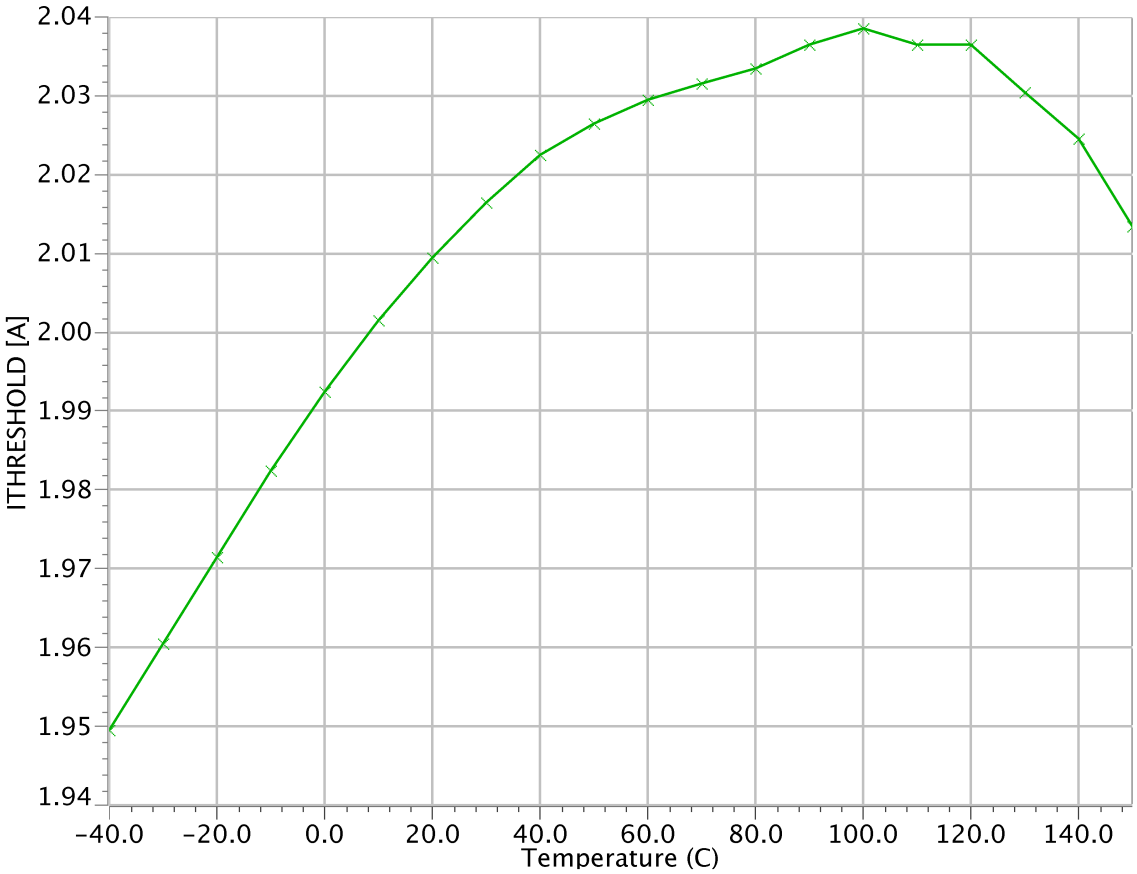


Figure 4.12: Temperature sweep simulation result.

where k is the current sensor gain, V_{GS}^{M1} is the gate source voltage of M_1 at the threshold, x_{trim} is the trimming ratio $V_{\text{cmp0}}/V_{\text{cs\_out}}$ and $SET_x \in \{0, 1\}$ represent on-states of transistors M_{10}–M_{13}.

Table 4.1: Contribution of different branches on current threshold.

$I_{\text{HS\_THR}}$	I_{R1}/k	I_{R5}/k	I_{R6}/k	I_{R7}/k	I_{R8}/k
1.3 A	1.0 A	0.3 A	OFF	OFF	OFF
1.5 A	1.0 A	OFF	0.5 A	OFF	OFF
2.0 A	1.0 A	OFF	OFF	1.0 A	OFF
3.0 A	1.0 A	OFF	OFF	1.0 A	1.0 A

The various thresholds that can be set along with the contributions of the different branches on the thresholds can be seen in Tab. 4.4. The branch contributions were selected based on ease of realization and splitting of resistors into modules.

For better temperature stability two different resistor types are were used to compensate temperature dependence of V_{GS}^{M1}, one being poly resistor and the other diffusion one. The resulting temperature characteristic for 2 A threshold is depicted in Fig. 4.12. It can be seen the variation of the threshold is from -2.5% at low temperatures up to 2% at around $100°\text{C}$. This is sufficient given that requirements for PVT variation of the threshold is around 20%.

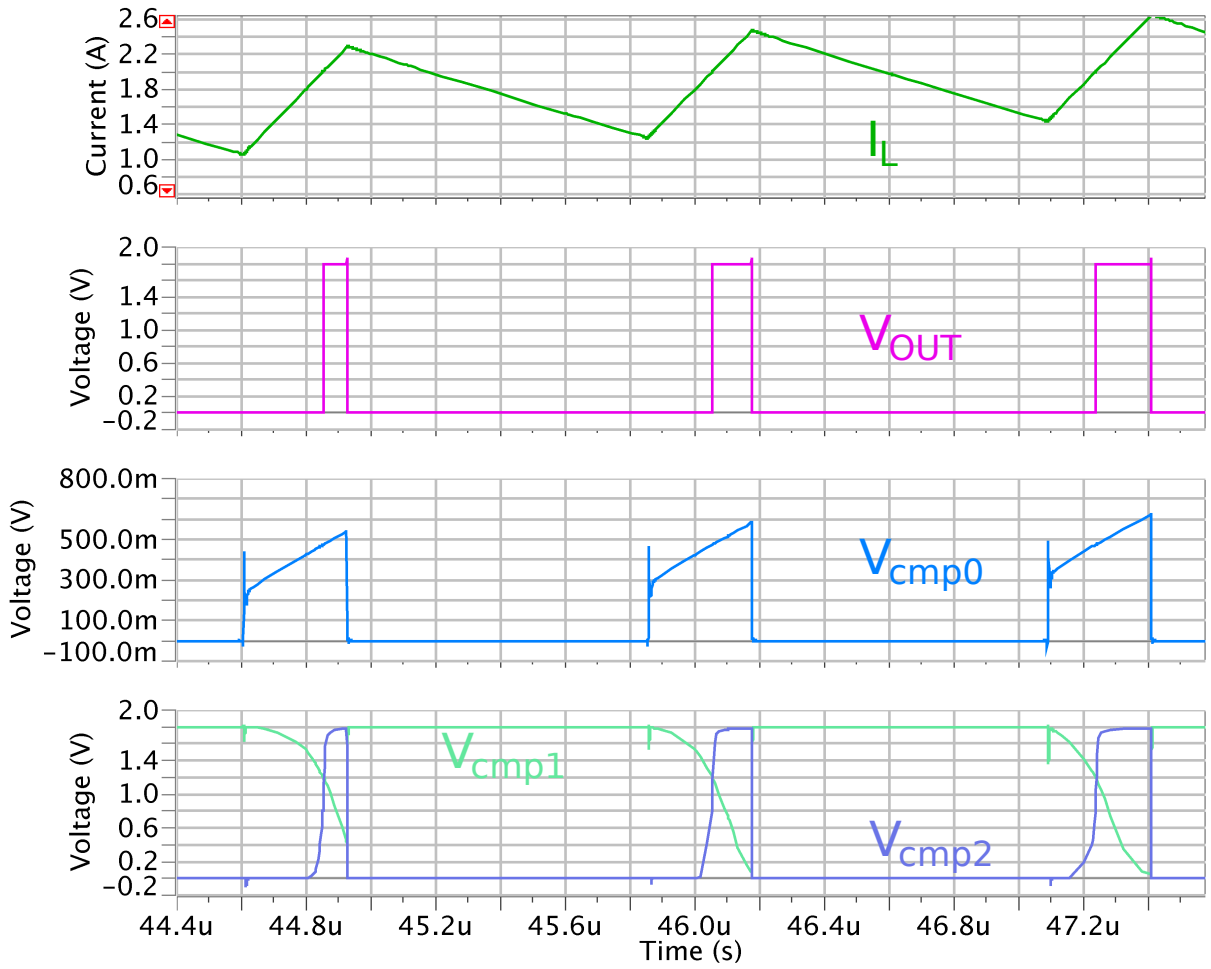


Figure 4.13: Transient simulation result.

Results

The circuit was designed in 180 nm BCD technology from STMicroelectronics. Fig. 4.13 shows the transient simulation results for a 2 A threshold setting. All the internal nodes of the comparator are shown along with the inductor current.

The static consumption of the circuit well below the threshold is around 16 µA plus 20 µA per each ampere of inductor current. This consists mostly of the consumption of the current sensor and the biasing circuit. When well below the threshold none of the transistors M_1 and M_2 in the comparator conduct so they do not consume current.

Table 4.2: Propagation delays.

I_{HS_THR}	t_{pd} **schematic**	t_{pd} **PLS**
1.3 A	11.2 ns	21.8 ns
1.5 A	11.1 ns	21.2 ns
2.0 A	9.9 ns	19.1 ns
3.0 A	9.0 ns	17.5 ns

Values of the propagation delay before and after post-layout are in Tab. 4.4. Unfortu-

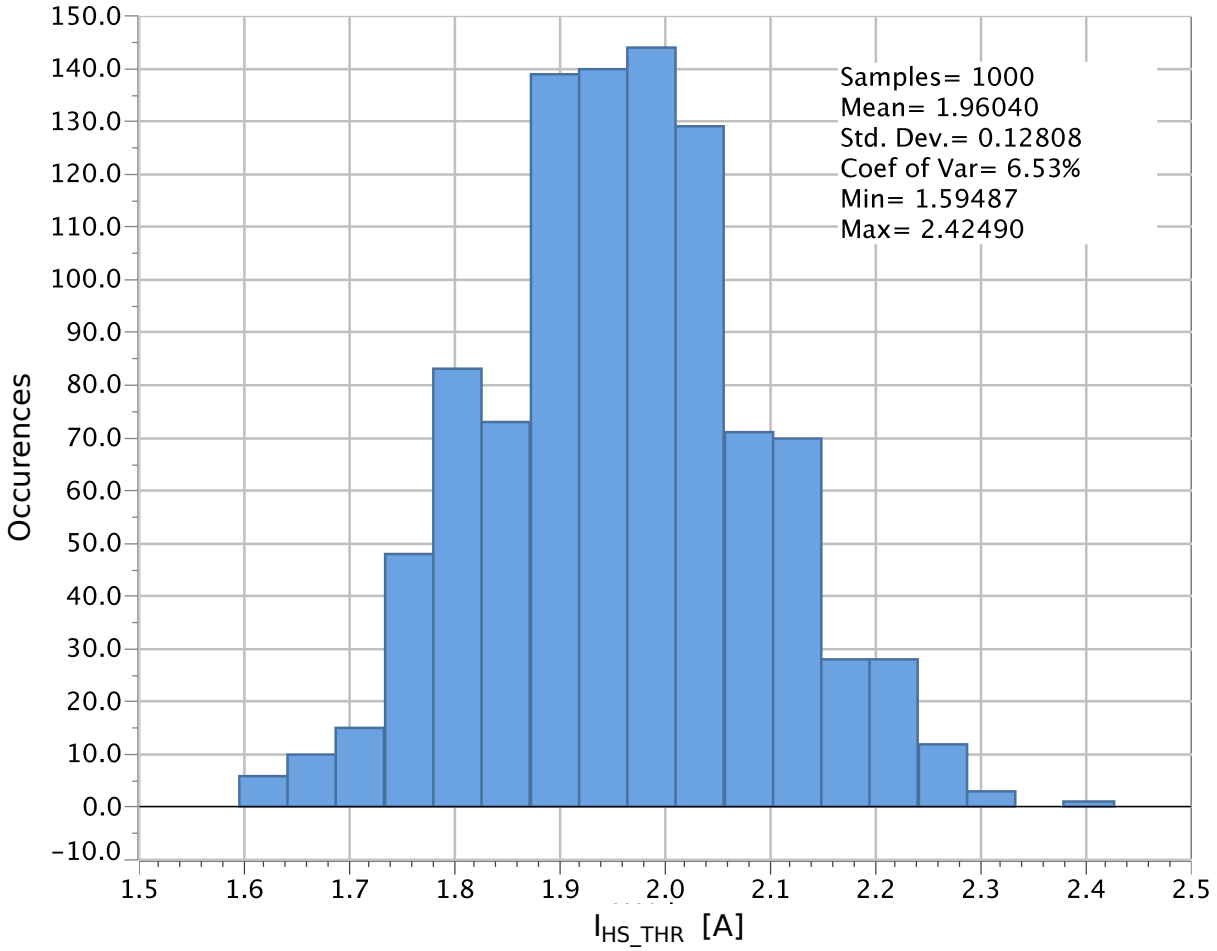


Figure 4.14: Monte Carlo simulation of current threshold spread (statistical corners).

nately due to the rush of the project the layout has not been optimized. This can be seen on the post-layout values which are almost double compared to the pure schematic ones. It also illustrates the importance of layout parasitics as the speed of the circuits approach technology limitations.

Monte Carlo simulation of the current threshold spread (without trimming) for a 2 A setting can be found in Fig. 4.14. The standard deviation is around 6.5 %.

The trimming range was set to span from -60% to +80%, this is much more than the expected variation, but it was required as a safety measure since the principle of operation is new.

The design was layouted in STMicroelectronics and manufactured as part of an SoC targeted as a power management for embedded processors. Fig. 4.15a shows the manufactured chip wire bonded on a PCB (COB – chip on board). This is used for an early measurements before packaged samples come out of factory.

Fig. 4.15b shows the layout of the chip. Besides boost and several LDO regulators, there are four buck converters each employing the presented circuit. The layout of the converter is depicted in Fig. 4.15c. Power transistors can be seen on the right. The sense MOSes are located just next to the power PMOS bottom power MOS) on its left side. The highlighted block is then the designed overcurrent detector whose layout is expanded in Fig. 4.15d. The

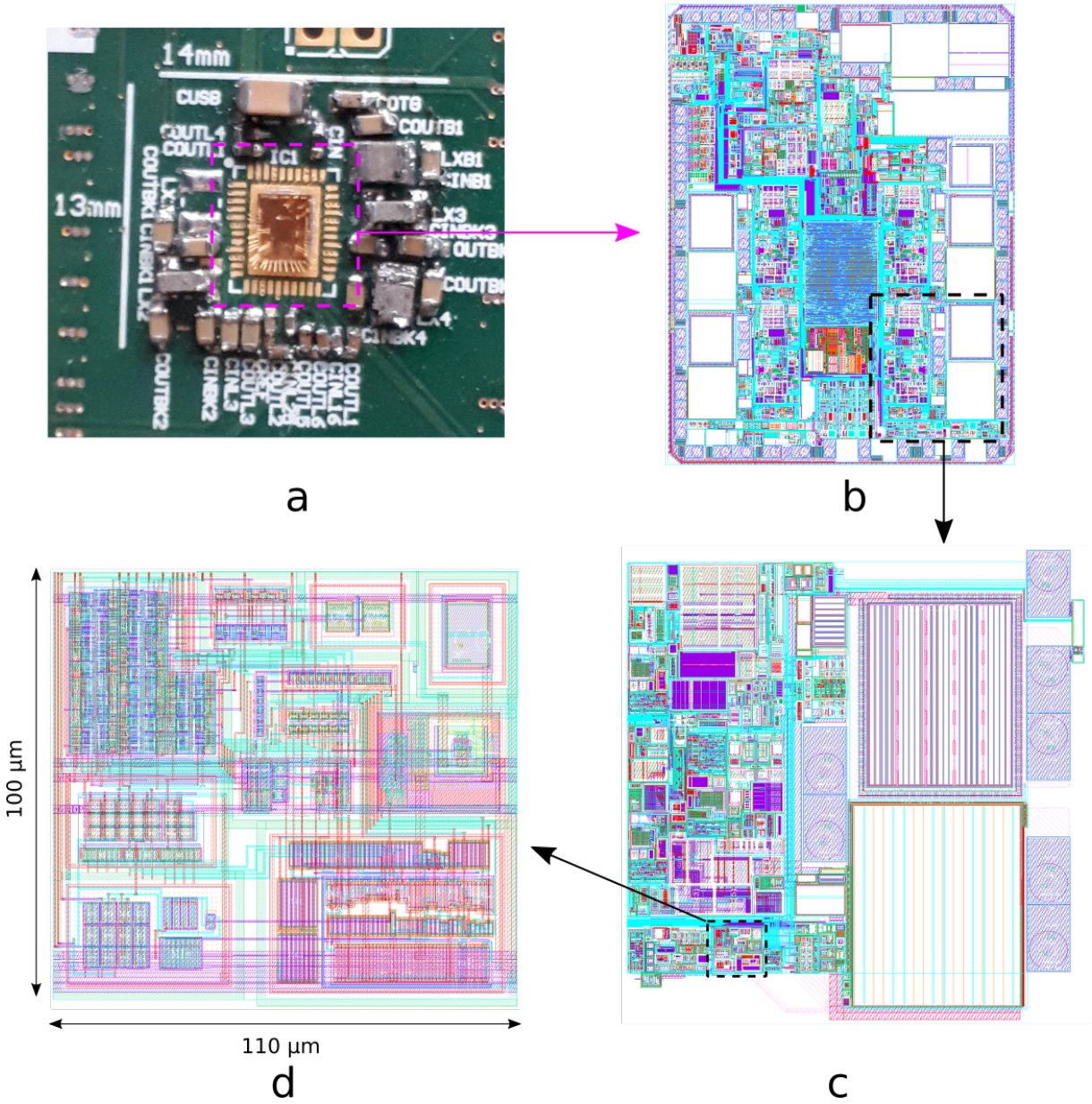


Figure 4.15: (a) Photo of COB with the designed circuit,(b) layout of the chip, (c) layout of the buck converter, (d) layout of the designed circuit (layouts courtesy of STMicroelectronics).

size of the solution (excluding sense MOSes) is 0.011 mm^2.

The operation of the designed circuit is demonstrated on the oscilloscope screenshot in Fig. 4.16 for the 1.5 A threshold setting. The figure shows the inductor current I_L, voltage on the LX switching node and output of the designed detector observed through a dedicated digital testing circuitry (as it uses standard digital output buffers, not designed for very high frequencies, the rise and fall times of the pulse are not sharp). The measured threshold is about 1.4 A (taking into account expected delay of 21 ns). As soon as the overcurrent condition is detected the power PMOS turns off and the overcurrent detector with it. The observed digital output thus goes to zero as well.

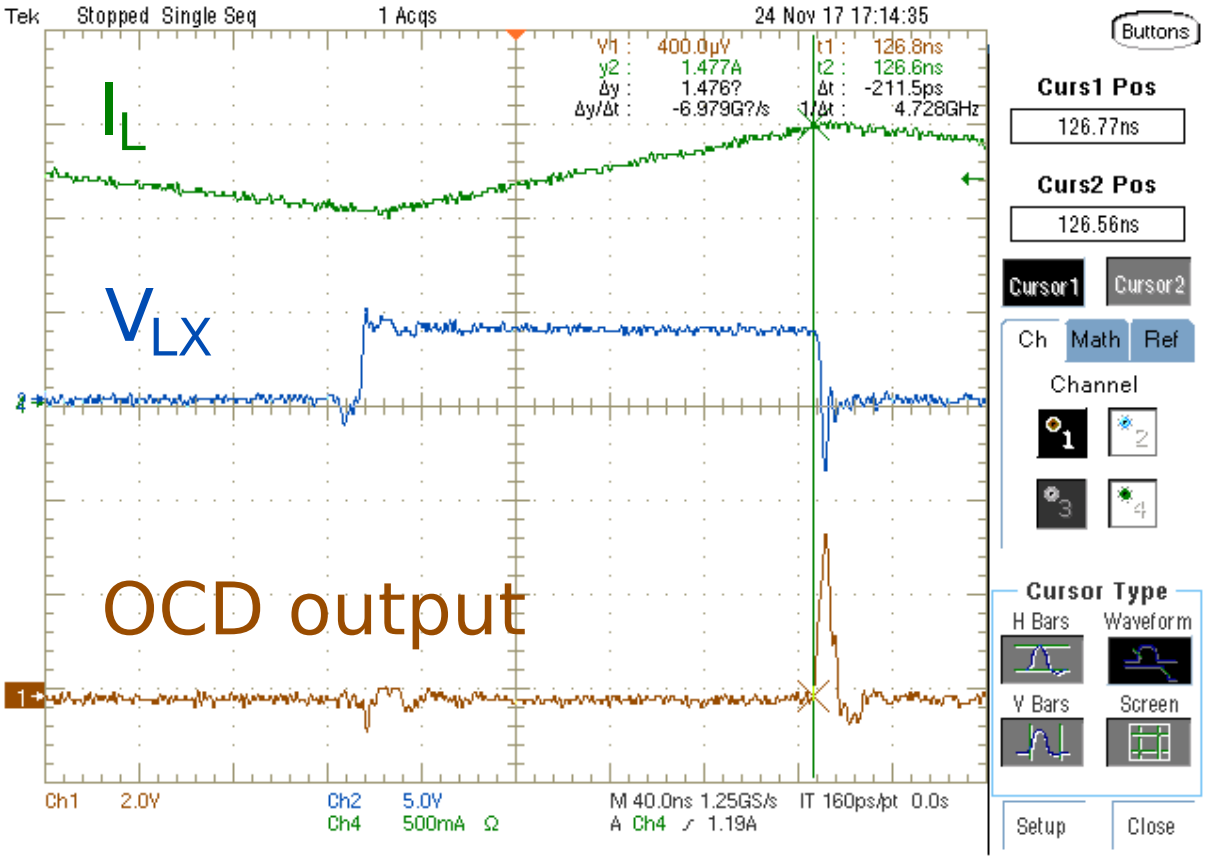


Figure 4.16: Oscilloscope screenshot showing the OCD operation for 1.5 A setting.

4.5 Summary

In this chapter a high voltage high side detector for DC-DC converters functioning both as an overcurrent and zero crossing detector was presented. The circuit finds its use in portable devices which must be able to charge a battery as well as provide voltage for external accessories. Combining these two functions into a single circuit allows saving silicon area which is even more important for multiphase DC-DC converters.

The proposed circuit was designed in 0.18 μm BCD technology occupying 0.035 mm^2. The circuit was manufactured as part of a dual-phase battery charger being placed twice on the die – one instance per phase. The measured results show correct operation in both OCD and ZCD modes.

The second presented circuit was an overcurrent detector with a built-in reference. It features a built-in detection threshold set by a V_{GS} of a MOS transistor and a resistor value R. The main benefits of this solution are lack of kickback noise on reference bias line, low power operation – consumes only when sensing current, high speed and small area. All these properties are essential for ultra low power converters.

The circuit was designed in the same 0.18 μm BCD technology and its operation was verified on silicon. It occupies 0.011 mm^2 and consumes 16 µA static current (at zero inductor current).

5 Conclusion

The thesis dealt with analog circuits for DC-DC converters. Being this such a broad topic three circuit areas have been selected to pursue: current sensors, oscillators and current comparators (both over current and zero crossing detectors). All of these share a common nature of the signals they process, fast triangular signal. In each of the three main chapters, one area was analyzed and, with respect to the goals set in the introductory chapter, the following contributions were made.

Chapter 2 presented a high voltage current sensor for DC-DC converters useful for off-chip DCR sensing or sensing on a resistor put in series with a coil. The circuit has been simulated and implemented in 0.35 μm BCD technology as part of a multiphase DC-DC converter where its function has been verified. The circuit is able to sustain the input common mode voltage up to 40 V, it occupies 0.387×0.345 mm^2 and consumes 3.2 mW typically. The main benefits of the circuit are the ability of bidirectional current sensing, no static input current and limitation of high voltage components only in the first stage. The presented current sensor is protected by US Patent 9,035,639 [C]. The findings were also published in an impacted journal [B].

Chapter 3 proposed a new relaxation oscillator generating both square and triangle waveforms. The frequency of the designed circuit is 1 MHz, it consumes 4.1 μA at 1.8 V and takes 0.0126 mm^2 of silicon area. The temperature variation from $-40\,^{\circ}$C to $125\,^{\circ}$C is ± 1.5 % and the temperature coefficient is 127 ppm/$^{\circ}$C. The solution uses only one area efficient hysteresis comparator thus saving silicon area. This circuit was also published in [A].

Chapter 4 presented two designs. The first is a combined high voltage high side detector for DC-DC converters functioning both as an overcurrent and zero crossing detector. The circuit is intended for portable battery chargers which must be able to charge a battery as well as provide voltage for external accessories. The proposed circuit was designed in 0.18 μm BCD technology occupying only 0.035 mm^2 and its operation was verified on silicon. It consumes 1.2 mW when operated from 12 V input supply voltage with a propagation delay of 24 ns. Combination of the two detectors into one saves silicon area, which is even more pronounced in multiphase DC-DC converters.

The second presented circuit is an overcurrent detector with built-in reference. The circuit doesn't use any external reference and can be fully turned-off with zero current consumption when not sensing. This is a benefit over standard solutions as kickback noise and slow startup are problems in very low power converters. The circuit was designed and manufactured in 0.18 μm BCD technology and its operation was verified on silicon. It occupies only 0.011 mm^2 and consumes 16 µA at zero inductor current.

Further work

As requirements on power consumption, area and speed (higher switching frequencies) increase the traditional analog only design of the aforementioned high-speed circuits becomes more difficult and approaches technology limits. In author's opinion, more focus will be given to design the simplest analog stages possible and rely on auto-zero and digital/mixed-signal circuit auto correction of its non-idealities. This benefits from the technology node scaling as digital circuits shrink faster from one node to other than the analog ones.

Author's Publications

Publications related to the thesis topic

Impacted articles

[A] Martin Drinovsky and Jiri Hospodka. "Triangle/square waveform generator using area efficient hysteresis comparator". In: *Radioengineering* 25.2 (2016), pp. 332–337.

[B] Martin Drinovsky and Jiri Hospodka. "High Voltage Coil Current Sensor for DC-DC Converters Employing DDCC". In: *Radioengineering* 24.4 (2015), pp. 988–992.

Patents

[C] Martin Drinovsky. "Voltage-to-current sensing circuit and related DC-DC converter". *US Patent 9,035,639*. May 2015.

Citations

Article [A] was cited in:

[A1] Lu, Yangyang, Jing Zhu, Yunwu Zhang, Weifeng Sun, Kuo Yu, and Jian Chen. "A high linearity current-controlled CMOS relaxation oscillator with frequency self-calibration technique." In: *Analog Integrated Circuits and Signal Processing* 92.1 (2017), pp. 29–37.

[A2] Sotner, Roman, Jiri Petrzela, Jan Jerabek, Ondrej Domansky, Lukas Langhammer, and Tomas Dostal. "Special electronically reconfigurable lossy/lossless integrator in application of functional generator." In: *27th International Conference Radioelektronika (RADIOELEKTRONIKA)*, Brno, 2017, pp. 1–5.

Patent [C] was cited in:

[C1] Jamaica L. Barnette, "Operating a DC-DC converter including a coupled inductor formed of a magnetic core and a conductive sheet". *US Patent 9,219,422*. December 2015.

[C2] Jamaica L. Barnette, "Operating and manufacturing a DC-DC converter". *US Patent 9,236,347*. January 2016.

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[C5] Christian Augesky and Daniel Portisch, “Power supply with a switch converter”. *US Patent 9,606,565*. March 2017.

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