

DRV8816 DMOS Dual 1/2-H-Bridge Motor Drivers

1 Features

- H-Bridge Motor Driver Individual
 - Drives a DC Motor or Other Loads
 - Low $R_{DS(on)}$ MOSFETs (0.4- Ω TYP)
- Low-Power Sleep Mode
- 100% PWM Supported
- 8- to 38-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package
- Configurable Overcurrent Limit
- Protection Features
 - VBB Undervoltage Lockout (UVLO)
 - Charge Pump Undervoltage (CPUV)
 - Overcurrent Protection (OCP)
 - Short-to-Supply Protection (STS)
 - Short-to-Ground Protection (STG)
 - Overtemperature Warning (OTW)
 - Overtemperature Shutdown (OTS)
 - Fault Condition Indication Pin (nFAULT)

2 Applications

- Printers
- Industrial Automation
- Robotics
- Motorized Levers

3 Description

The DRV8816 provides a versatile power driver solution with two independent 1/2-H bridge drivers. The device can drive one brushed DC motor or one winding of a stepper motor, as well as other devices like solenoids. A simple INx/ENx interface allows easy interfacing to controller circuits.

The output stages use N-channel power MOSFETs configured as 1/2-H-bridges. The DRV8816 is capable of peak output currents up to ± 2.8 A and operating voltages up to 38 V. An internal charge pump generates needed gate drive voltages.

A low-power sleep mode is provided which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal protection functions are provided for UVLO, charge pump fault, OCP, short-to-supply protection, short-to-ground protection, overtemperature warning, and overtemperature shutdown. Fault conditions are indicated through a nFAULT pin.

The DRV8816 is packaged in a 16-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br)

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8816	HTSSOP (16)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

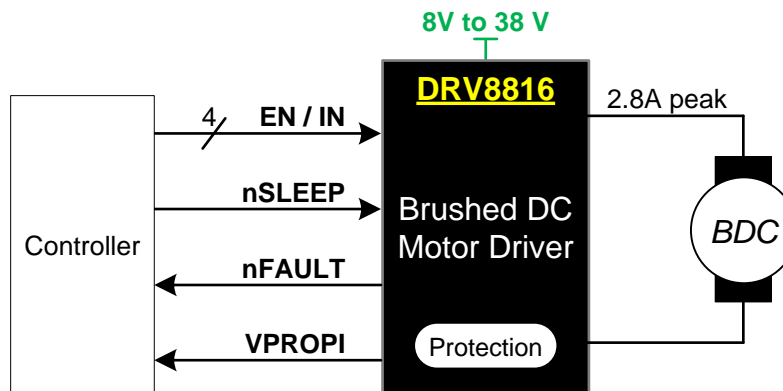


Table of Contents

1 Features	1	8.4 Device Functional Modes.....	11
2 Applications	1	9 Application and Implementation	13
3 Description	1	9.1 Application Information.....	13
4 Simplified Schematic	1	9.2 Typical Application	13
5 Revision History	2	10 Power Supply Recommendations	16
6 Pin Configuration and Functions	3	10.1 Bulk Capacitance	16
7 Specifications	4	10.2 Power Supervisor.....	16
7.1 Absolute Maximum Ratings	4	11 Layout	17
7.2 Handling Ratings.....	4	11.1 Layout Guidelines	17
7.3 Recommended Operating Conditions	4	11.2 Layout Example	17
7.4 Thermal Information	5	11.3 Thermal Protection.....	18
7.5 Electrical Characteristics.....	5	12 Device and Documentation Support	19
7.6 Typical Characteristics.....	6	12.1 Trademarks	19
8 Detailed Description	8	12.2 Electrostatic Discharge Caution.....	19
8.1 Overview	8	12.3 Glossary	19
8.2 Functional Block Diagram	8	13 Mechanical, Packaging, and Orderable	19
8.3 Feature Description.....	8	Information	19

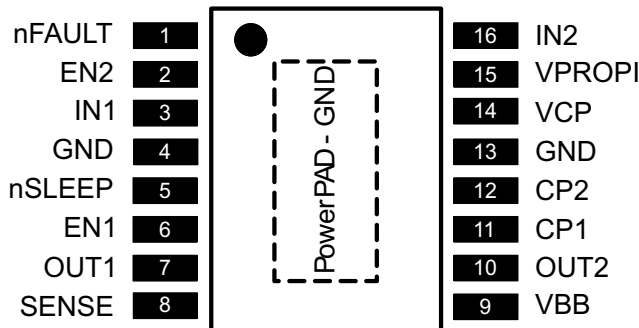
5 Revision History

Changes from Original (September 2013) to Revision A

Page

• Added <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	4
• Updated Figure 5.....	12

6 Pin Configuration and Functions


Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
CP1	11	PWR	Charge pump switching node	Connect a 0.1- μ F X7R capacitor rated for VBB between CP1 and CP2
CP2	12	—		
GND	4, 13, PPAD	PWR	Device ground	Connect to system ground
VBB	9	PWR	Power supply input	Connect to main power supply. Bypass to GND with a 0.1- μ F ceramic capacitor and a larger bulk capacitor rated for at least the VBB voltage
VCP	14	PWR	Charge pump output	Connect a 0.1- μ F 16-V ceramic capacitor between VCP and VBB
CONTROL				
EN1	6	I	$\frac{1}{2}$ -H bridge enable	Logic high enables $\frac{1}{2}$ -H bridge output; logic low puts the FETs in HI-Z; internal pulldown
EN2	2			
IN1	3	I	$\frac{1}{2}$ -H bridge control	Logic high enables the high-side $\frac{1}{2}$ -H bridge FET; logic low enables the low side FET; internal pulldown
IN2	16			
nFAULT	1	O	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
nSLEEP	5	I	Device sleep mode	Pull logic low to put device into a low-power sleep mode; internal pulldown
OUTPUT				
OUT1	7	O	$\frac{1}{2}$ -H bridge output	
OUT2	10	O	$\frac{1}{2}$ -H bridge output	
SENSE	8	O	H-bridge low-side connect	Connect directly to GND or through a sense resistor to set OCP
VPROPI				
VPROPI	15	O	Current-proportional output	

Table 1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VBB}	VBB	GND	0.1- μ F ceramic capacitor and a larger bulk capacitor rated for at least the VBB voltage
C_{VCP}	VCP	VBB	0.1- μ F 16-V ceramic capacitor
R_{nFAULT}	VCC ⁽¹⁾	nFAULT	>1 k Ω resistor
R_{nSLEEP}	VCC ⁽¹⁾	nSLEEP	If nSLEEP isn't actively controlled, use a pull-up resistor of less than 20 k Ω
R_{SENSE}	SENSE	GND	Optional low-value resistor. If not used, connect SENSE pin directly to GND.
R_{VPROPI}	VPROPI	GND	If VPROPI is used, add a 100k Ω resistor to GND

(1) VCC is not a pin on the DRV8816, but a VCC supply voltage pullup is required.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _B	Power supply voltage	-0.6	40	V
	Charge pump positive switching pin (CP2)	-0.6	V _B + 7	V
	Charge pump negative switching pin (CP1)	-0.6	V _B	V
	Digital pin voltage range (IN1, IN2, EN1, EN2, nSLEEP, nFAULT)	-0.3	7	V
	V _B to OUT _x	-0.6	40	V
	OUT _x to SENSE	-0.6	40	V
V _(SENSE)	Sense voltage (SENSE) ⁽²⁾	-0.5	1.0	V
	H-bridge output current (OUT1, OUT2, SENSE)	0	2.8	A
	V _{PROPI} pin voltage range (V _{PROPI})	-0.3	3.6	V
T _A	Operating ambient temperature	-40	85	°C
T _J	Operating junction temperature	-40	190	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Transients of ±1 V for less than 25 ns are acceptable.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-40	125	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		
		-2000	2000	
		-500	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _B	Power supply voltage range	8	38	V
V _I	Input pin voltage range	0	5.5	V
f _{PWM}	Applied PWM signal (IN1, IN2, EN1, EN2)		100	kHz
I _{OUT}	H-bridge output current		2.8	A
T _A	Ambient temperature	-40	85	°C

- (1) Power dissipation and thermal limits must be observed.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV8816		UNIT
		PWP		
		16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	43.9		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance ⁽³⁾	30.8		
R _{θJB}	Junction-to-board thermal resistance ⁽⁴⁾	25.3		
ψ _{JT}	Junction-to-top characterization parameter ⁽⁵⁾	1.1		
ψ _{JB}	Junction-to-board characterization parameter ⁽⁶⁾	25		
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	5.6		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VBB)							
VBB	VBB operating voltage			8		38	V
I _{VBB}	VBB operating supply current	f _{PWM} < 50 kHz			6		mA
		Charge pump on, Outputs disabled			3.2		mA
I _{VBBQ}	VBB sleep-mode supply current	nSLEEP = 0, T _J = 25°C				10	μA
CONTROL INPUTS (IN1, IN2, EN1, EN2, nSLEEP)							
V _{IL}	Input logic low voltage	IN1, IN2, EN1, EN2		0		0.8	V
V _{IH}	Input logic high voltage			2		5.5	
V _{IL}	Input logic low voltage	nSLEEP		0		0.8	V
V _{IH}	Input logic high voltage			2.2		5.5	V
I _{IL}	Input logic low current	IN1, IN2, EN2, nSLEEP	V _{IN} = 0 V		0		μA
I _{IH}	Input logic high current		V _{IN} = 5 V		25		
I _{IL}	Input logic low current	EN1	V _{IN} = 0 V		0		μA
I _{IH}	Input logic high current		V _{IN} = 5 V		100		
R _{PD}	Pulldown resistance	IN1, IN2, EN2, nSLEEP			200		kΩ
		EN1			50		
SERIAL AND CONTROL OUTPUT (nFAULT)							
V _{OL}	Output logic low voltage	I _{sink} = 1 mA				0.4	V
DMOS DRIVERS (OUT1, OUT2, SENSE)							
R _{DS(on)}	Output ON resistance	Source driver, I _{OUT} = -2.8 A, T _J = 25°C			0.48		Ω
		Source driver, I _{OUT} = -2.8 A, T _J = 125°C			0.74	0.85	
		Sink driver, I _{OUT} = -2.8 A, T _J = 25°C			0.35		
		Sink driver, I _{OUT} = -2.8 A, T _J = 125°C			0.52	0.7	
V _{TRIP}	SENSE trip voltage	R _{SENSE} between SENSE and GND			500		mV

Electrical Characteristics (continued)

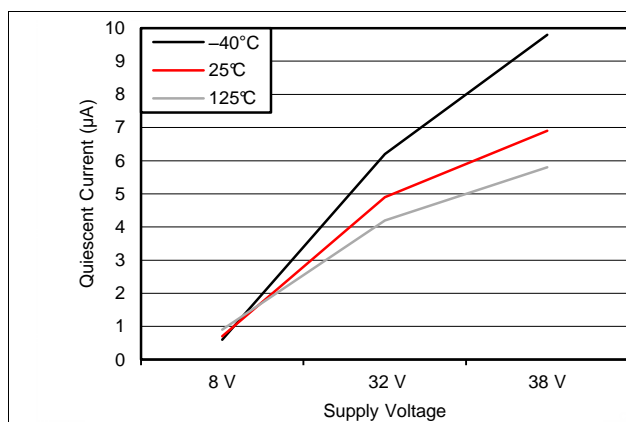
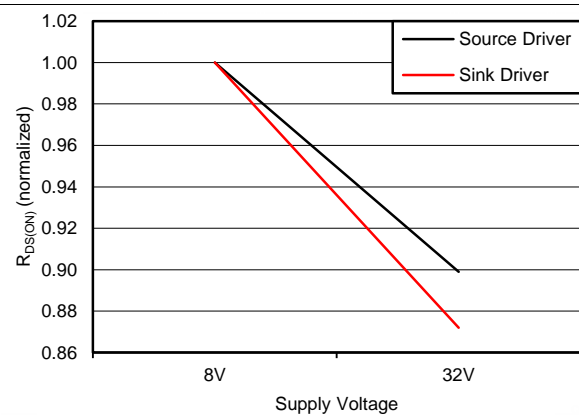
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_f	Body diode forward voltage	Source diode, $I_f = -2.8$ A			1.4	V
		Sink diode, $I_f = 2.8$ A			1.4	
t_{pd}	OUTx propagation delay	From High-Z to High		70		ns
		From High-Z to Low		700 ⁽¹⁾		
		From High to High-Z		120		
		From High to Low		700		
		From Low to High-Z		350		
		From Low to High		350		
t_{COD}	Crossover delay		500		ns	
DAGain	VPROPI amplifier gain	Sense = 0.1 to 0.4 V		5		V/V
PROTECTION CIRCUITS						
V_{UVLO}	VBB UVLO	VBB rising		6.5	7.5	V
V_{CPUV}	VCP UVLO ⁽²⁾	VBB rising; CPUV recovery		12	13.8	V
I_{OCP}	Overcurrent protection trip level		3			A
t_{DEG}	Overcurrent deglitch time			3.0		μ s
t_{OCP}	Overcurrent retry time			1.6		ms
T_{OTW}	Thermal warning temperature	Die temperature T_j		160		$^{\circ}$ C
$T_{OTW HYS}$	Thermal warning hysteresis	Die temperature T_j		15		$^{\circ}$ C
T_{OTS}	Thermal shutdown temperature	Die temperature T_j		175		$^{\circ}$ C
$T_{OTS HYS}$	Thermal shutdown hysteresis	Die temperature T_j		15		$^{\circ}$ C

(1) If OUT2 is High, the typical time for OUT1 to go from High-Z to Low is 1700 ns.

 (2) Whenever VCP is less than $V_M + 10$ V, a CPUV event occurs. This fault will be asserted whenever VBB is below 12 V. Note that the H-bridges will remain enabled until $V_{BB} = V_{UVLO}$ even through nFAULT is pulled low.

7.6 Typical Characteristics


 Figure 1. I_{VBBQ} vs VBB

 Figure 2. $R_{DS(ON)}$ vs VBB (normalized to VBB = 8V)

Typical Characteristics (continued)

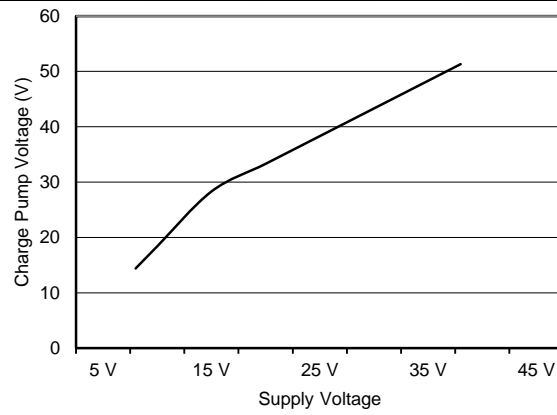


Figure 3. VCP vs VBB

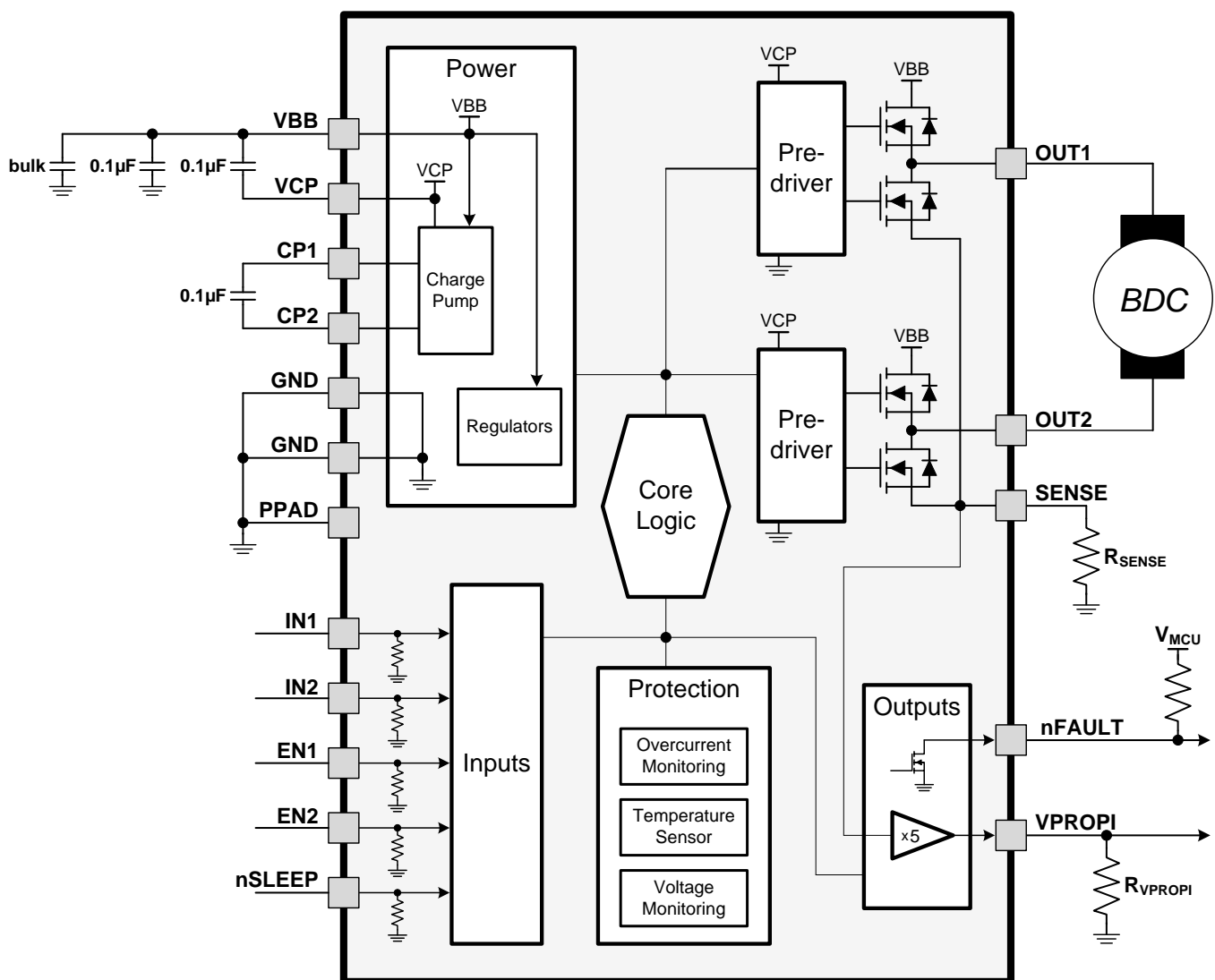
8 Detailed Description

8.1 Overview

The DRV8816 uses 4 CMOS inputs to control 2 high-voltage high-current outputs, while integrating protection features, fault reporting, a sleep mode, and current sensing. EN1 and IN1 control OUT1, and EN2 and IN2 control OUT2, according to Table 2. The device is designed to drive two independent loads or one brushed DC motor, as shown in Figure 4 and Table 3.

When an R_{SENSE} resistor is used, the DRV8816 will automatically disable itself if V_{SENSE} exceeds 500mV—this provides a user-programmable overcurrent threshold. The VPROPI output equals the sense voltage amplified by a factor of 5, and it can be used by a microcontroller to know the motor current, in order to Pulse-Width Modulate the DRV8816 inputs and regulate motor current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bridge Control

The DRV8816 is controlled using separate enable and input pins for each ½-H-bridge.

Feature Description (continued)

Table 2 shows the logic for the DRV8816.

Table 2. DRV8816 Logic

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

If a single DC motor is connected to the DRV8816, it is connected between the OUT1 and OUT2 pins as shown in Figure 4. Two DC motors may also be connected to the DRV8816. In this mode, it is not possible to reverse the direction of the motors; the motors will turn only in one direction. The connections are shown in Figure 4.

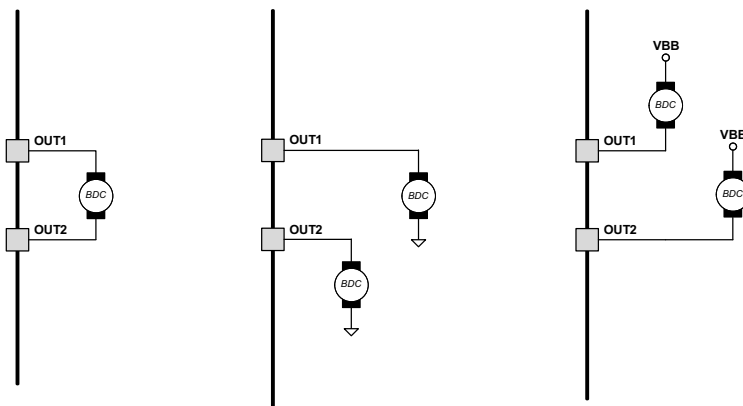


Figure 4. Bridge Control

Table 3 shows how motor operation for a single-brushed DC motor is controlled.

Table 3. Motor Operation for a Single-Brushed DC Motor

EN1	EN2	IN1	IN2	OUT1	OUT2	Operation
0	X	X	X	Z	X ⁽¹⁾	Off (coast)
X	0	X	X	X ⁽¹⁾	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

(1) The Half-H bridges are independent; output state depends on ENx and INx.

Table 4 shows how motor operation for dual-brushed DC motors is controlled.

Table 4. Motor Operation for a Dual-Brushed DC Motor

	ENx	INx	OUTx	Operation
Motor connected to GND	0	X	Z	Off (coast)
	1	0	L	Brake
	1	1	H	Forward
Motor connected to VBB	0	X	Z	Off (coast)
	1	0	L	Forward
	1	1	H	Brake

8.3.2 Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1- μF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1- μF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

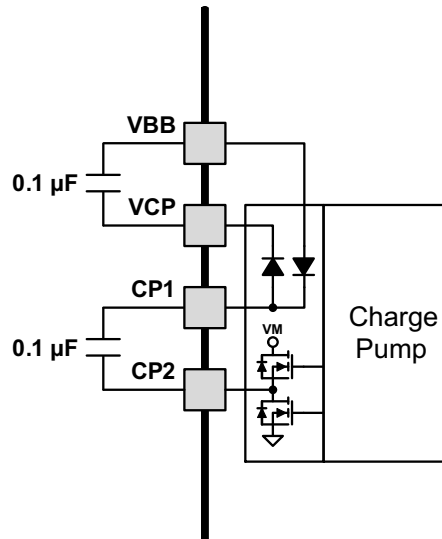


Figure 5. Charge Pump

8.3.3 VPROPI

The VPROPI output is equal to approximately 5x the voltage present on the SENSE pin. VPROPI is meaningful only if there is a resistor connected to the SENSE pin; if SENSE is connected to ground, VPROPI measures 0 V. Also note that during slow decay (brake), VPROPI measures 0 V. VPROPI can output a maximum of 2.5 V, because at 500 mV on SENSE, the H-bridge is disabled.

8.3.4 Protection Circuits

The DRV8816 is fully protected against VBB undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

8.3.4.1 VBB UVLO

If at any time the voltage on the VBB pin falls below the UVLO threshold voltage, all FETs in the H-bridge will be disabled and the charge pump will be disabled. Operation will resume when VBB rises above the UVLO threshold. Note that nFAULT does not indicate a UVLO because the CPUV fault is always asserted below VBB = 12 V.

8.3.4.2 VCP UVLO (CPUV)

During a CPUV event, the VCP voltage is measured to be below VCP + 10 V. If at any time the voltage on the VCP pin falls below the UVLO threshold voltage, the nFAULT pin is driven low. The nFAULT pin is released after operation has resumed. Note that this fault does not disable the output FETs and allows the device to continue operating. When VBB is below 12 V, this fault condition is always asserted and nFAULT is pulled low.

8.3.4.3 OCP

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge are disabled, nFAULT is driven low, and a t_{OCP} fault timer is started. After this period, t_{OCP} , the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after t_{OCP} expires it is determined the short condition is not present, normal operation resumes and nFAULT is released.

8.3.4.4 OTW

If the die temperature increases past the thermal warning threshold, the nFAULT pin is driven low. After the die temperature has fallen below the hysteresis level, the nFAULT pin is released. If the die temperature continues to increase, the device enters overtemperature shutdown as described in [OTS](#).

8.3.4.5 OTS

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the charge pump is shut down. After the die temperature has fallen to a safe level, operation automatically resumes.

8.4 Device Functional Modes

8.4.1 SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. The PCB should be designed with wide metal paths on each side of the resistor, to minimize IR drop that would decrease sense accuracy. Likewise, the distance from the sense resistor to the DRV8816 and bulk capacitor should be minimized.

To set a manual overcurrent trip threshold, place a resistor between the SENSE pin and GND. When the SENSE pin rises above 500 mV, the H-bridge output is disabled (High-Z). The device will automatically retry with a period of t_{OCP} . The overcurrent trip threshold can be calculated using $I_{TRIP} = 500 \text{ mV}/\Omega$. The overcurrent trip level selected cannot be greater than I_{OCP} .

If a sense resistor is not used, tie the SENSE pin directly to GND; in that case, the I_{OCP} detection of current through the internal FETs still functions.

Device Functional Modes (continued)

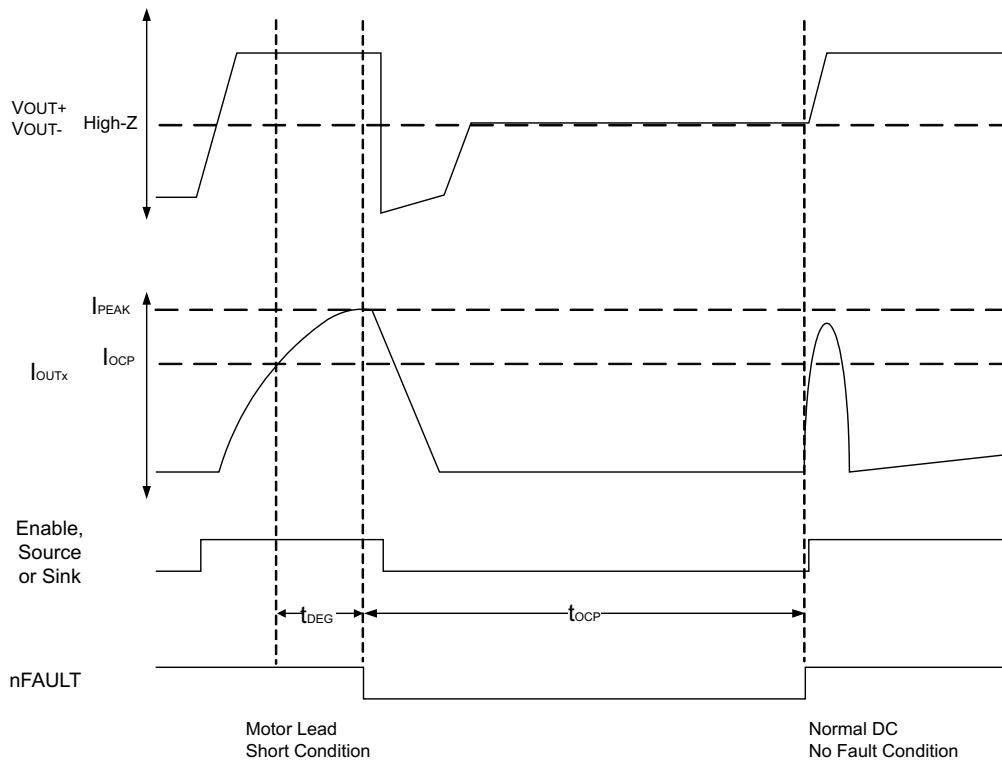


Figure 6. Overcurrent Threshold

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8816 is typically used to drive a brushed DC motor.

9.2 Typical Application

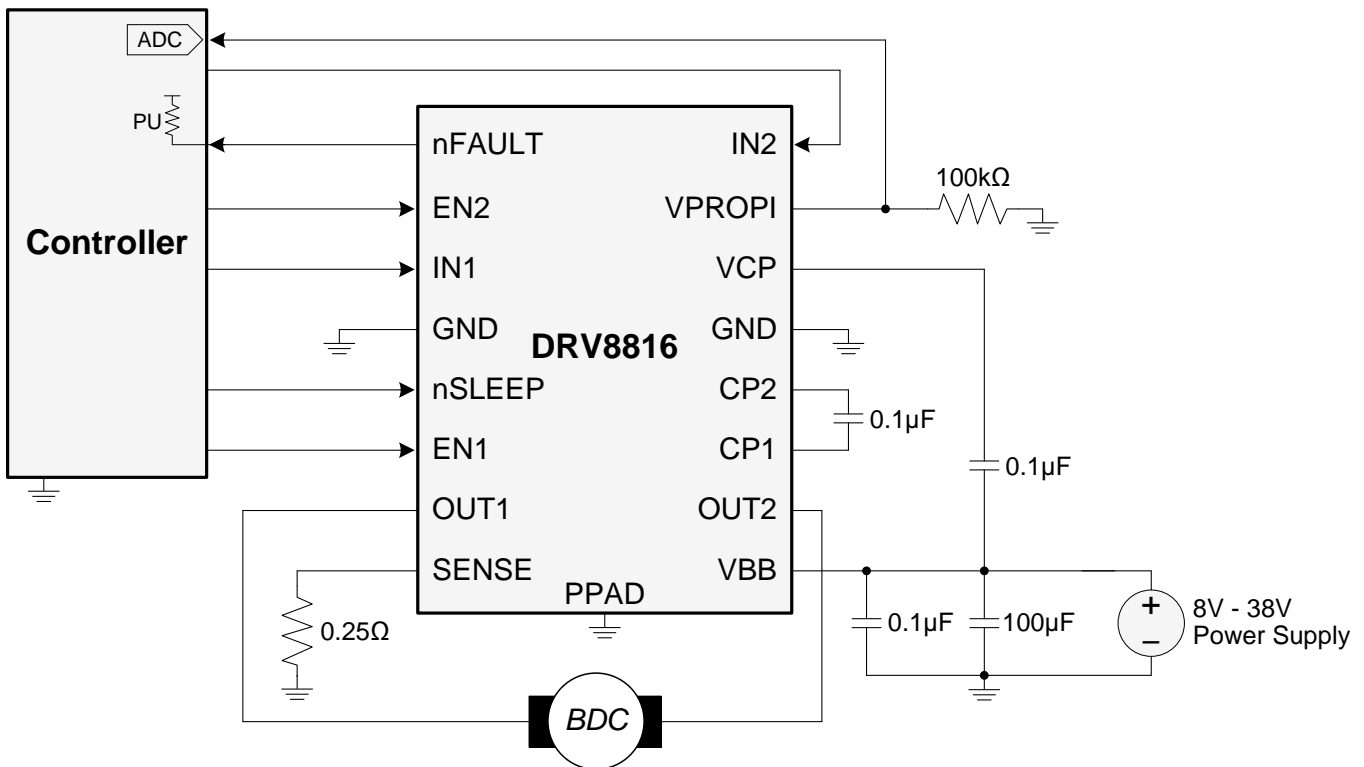


Figure 7. Typical Application

9.2.1 Design Requirements

Table 5 shows parameters to consider when designing.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{BB}	24V
Motor RMS current	I_{RMS}	0.8A
Motor startup current	I_{START}	2A
Motor current trip point	I_{TRIP}	2.5A

9.2.2 Detailed Design Procedure

9.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.2.2 Power Dissipation

The power dissipation of the DRV8816 is a function of RMS motor current and the each output's FET resistance ($R_{DS(ON)}$).

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \quad (1)$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of $R_{DS(ON)}$ is about 1Ω. With an example motor current of 0.8A, the dissipated power in the form of heat will be $0.8A^2 \times 1\Omega = 0.64W$.

The temperature that the DRV8816 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order to dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8816 had an effective thermal resistance $R_{\theta JA}$ of 47°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 35^\circ\text{C} + (0.64\text{W} \times 47^\circ\text{C/W}) = 65^\circ\text{C} \quad (2)$$

9.2.2.3 Motor Current Trip Point

When the voltage on pin SENSE exceeds V_{TRIP} (0.5V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{TRIP} level.

$$R_{SENSE} = 0.5V / I_{TRIP} \quad (3)$$

To set I_{TRIP} to 2A, $R_{SENSE} = 0.5V / 2A = 0.25\Omega$.

To prevent false trips, I_{TRIP} must be higher than regular operating current. Motor current during startup is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It can be beneficial to limit startup current by using series inductors on the DRV8816 output, as that allows I_{TRIP} to be lower, and it may decrease the system's required bulk capacitance. Startup current can also be limited by ramping the forward drive duty cycle.

9.2.2.4 Sense Resistor Selection

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3A, RMS motor current is 2A, and a 0.05Ω sense resistor is used, the resistor will dissipate $2A^2 \times 0.05\Omega = 0.2W$. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

9.2.3 Application Curves

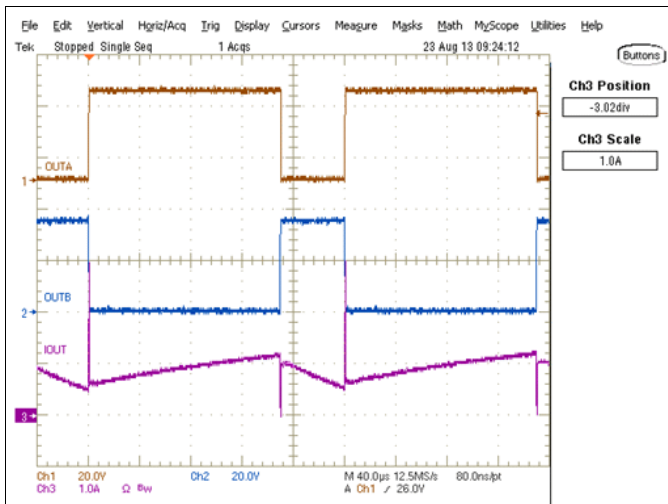


Figure 8. Forward Drive, Fast Decay

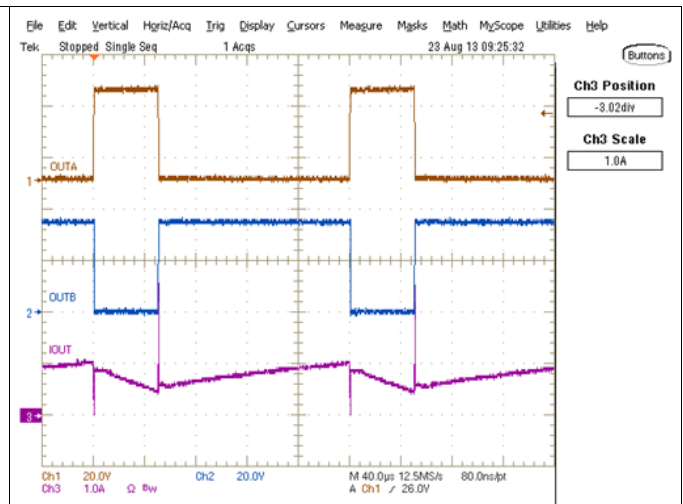


Figure 9. Reverse Drive, Fast Decay

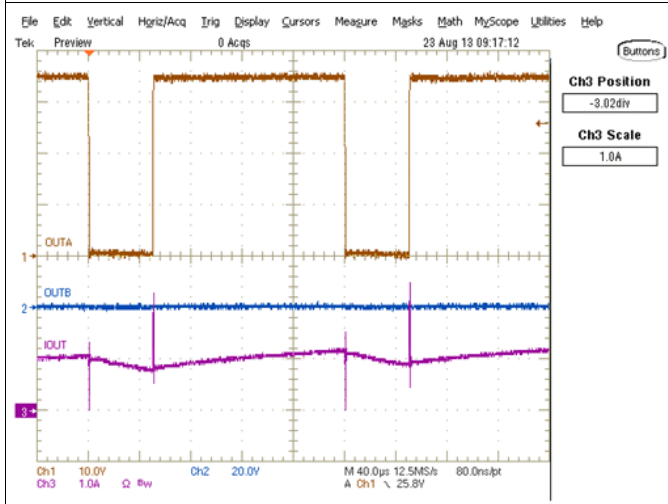


Figure 10. Forward Drive, Slow Decay

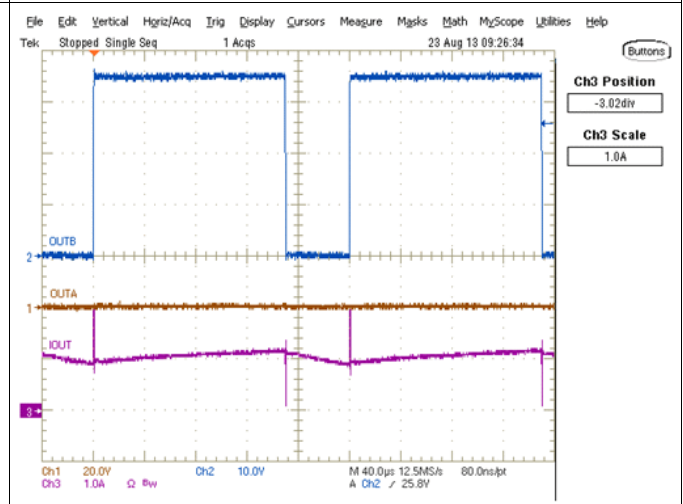


Figure 11. Reverse Drive, Slow Decay

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor systems.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

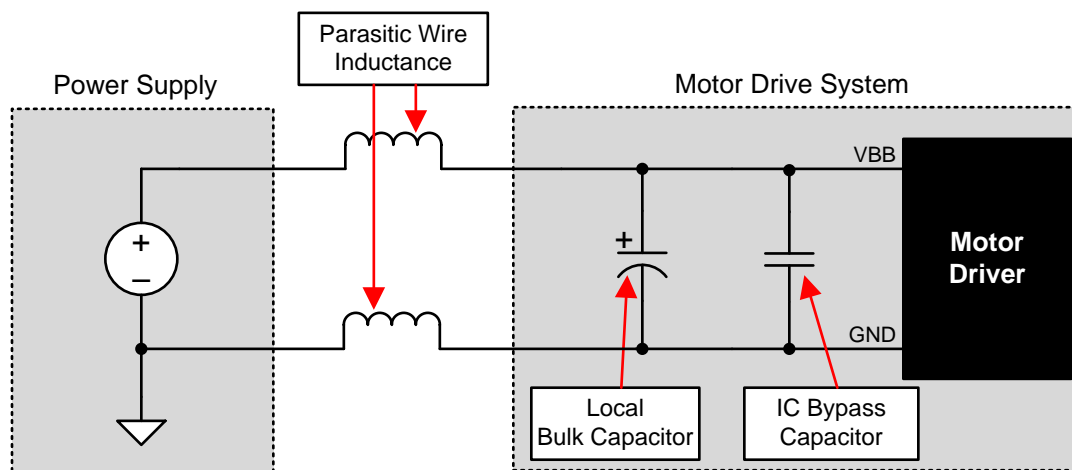


Figure 12. Example Setup of Motor Drive System with External Power Supply

10.2 Power Supervisor

Control input nSLEEP is used to minimize power consumption when the DRV8816 is not in use. This disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

11 Layout

11.1 Layout Guidelines

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8816 must be soldered directly onto the board. On the underside of the DRV8816 is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 μ F) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2 should be as close to the pins of the device as possible, in order to minimize lead inductance.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation.
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETS.
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. (4)

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

$I_{OUT(RMS)}$ is equal to approximately 0.7 \times the full-scale output current setting.

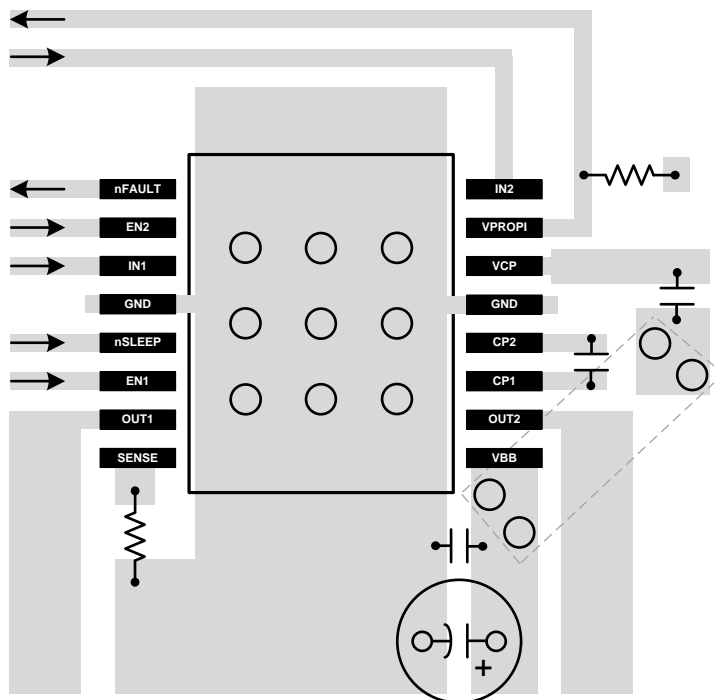
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

11.1.1 Ground

A ground power plane should be located as close to DRV8816 as possible. The copper ground plane directly under the thermal pad makes a good location. This pad can then be connected to ground for this purpose.

11.2 Layout Example



11.3 Thermal Protection

If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level. Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8816PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816	Samples
DRV8816PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8816PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

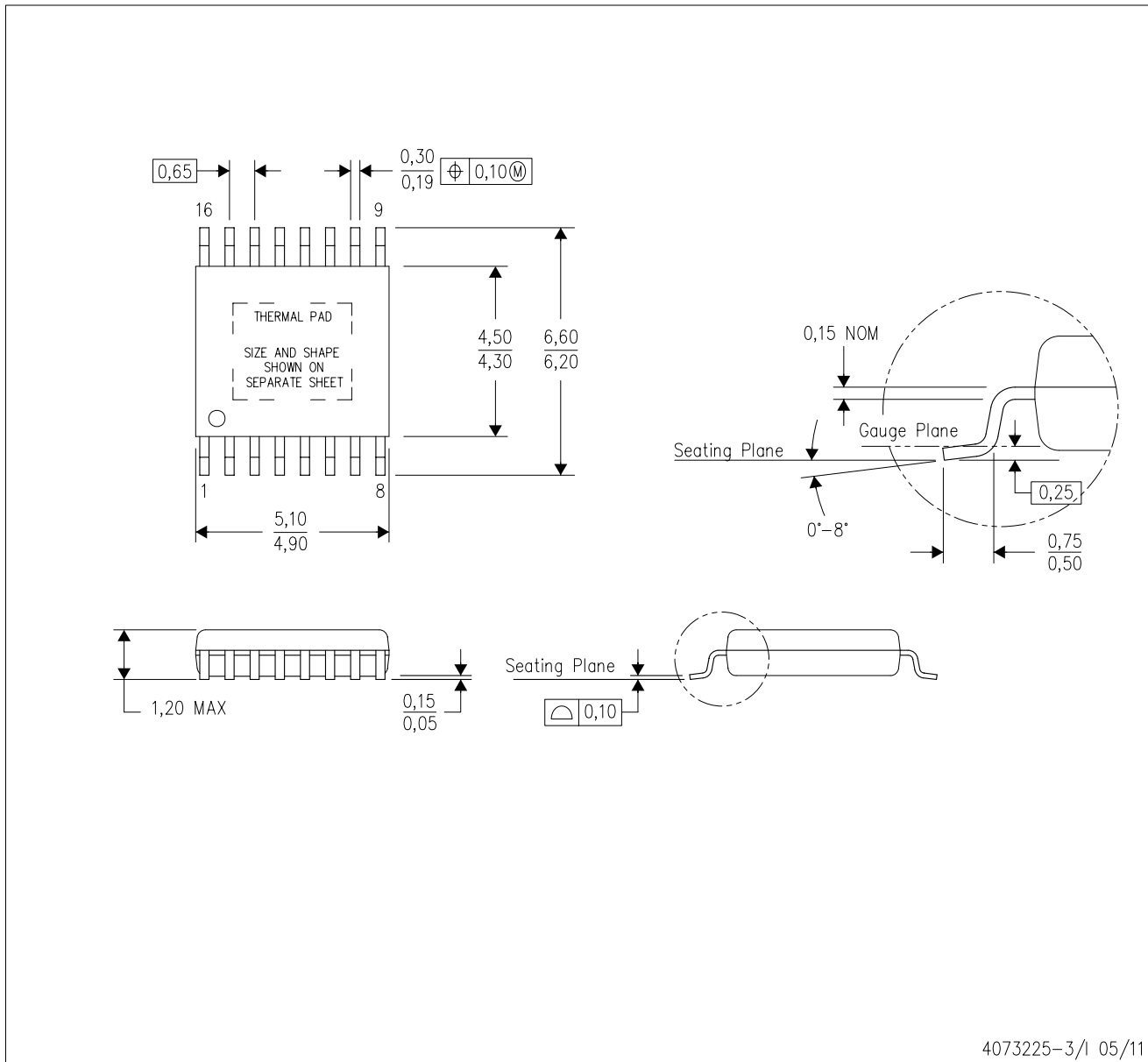


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8816PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

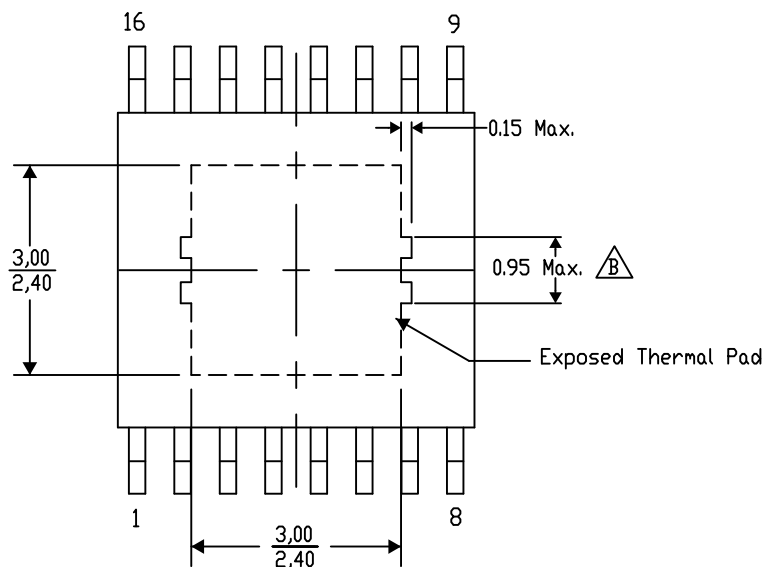
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-8/AJ 10/14

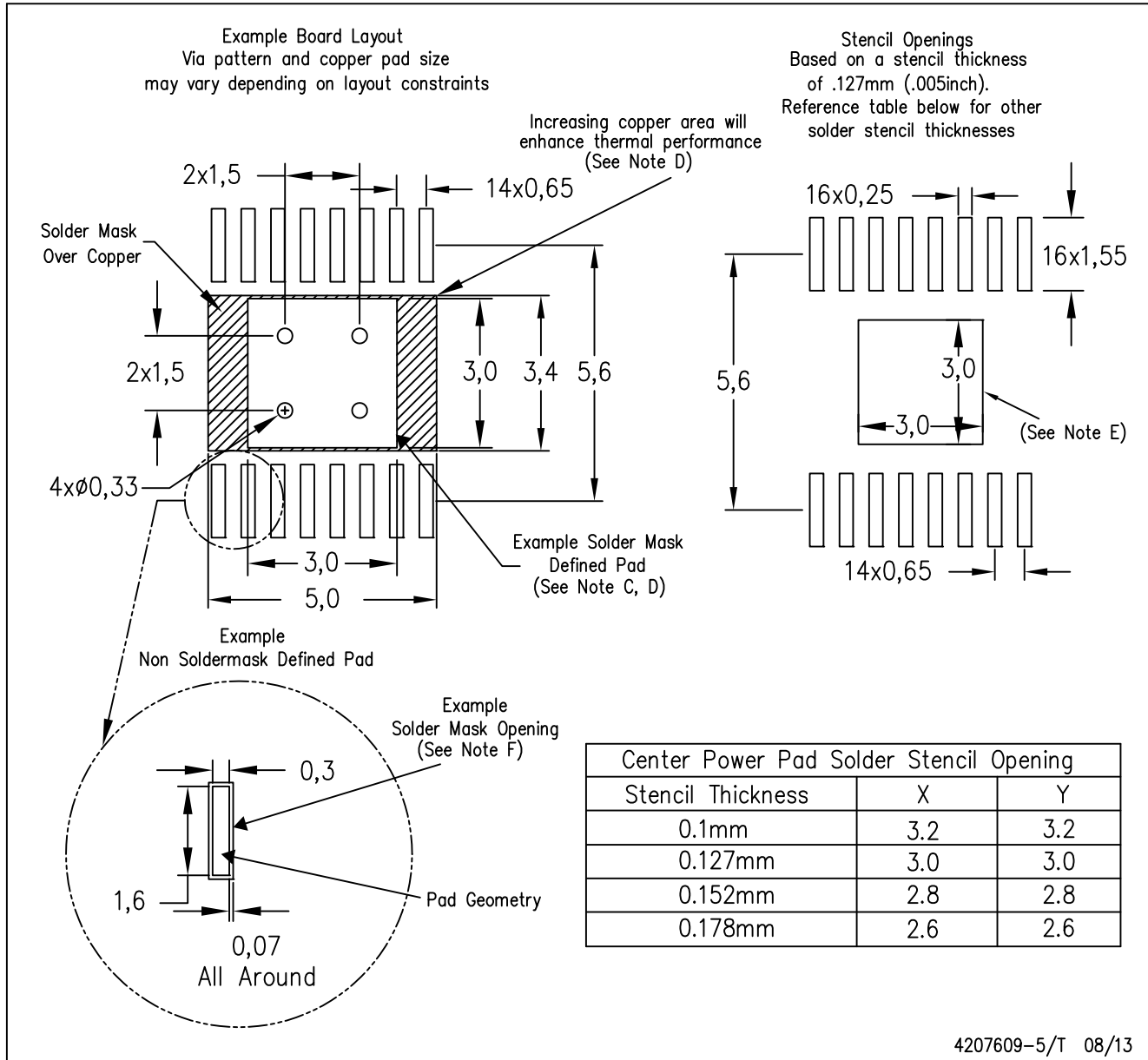
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com