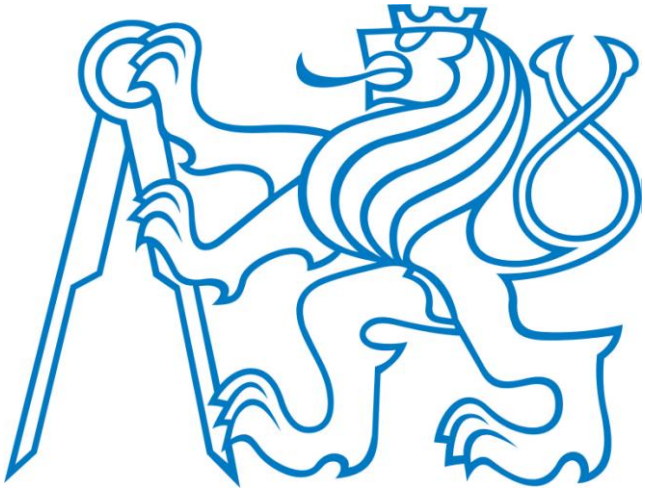
CZECH TECHNICAL UNIVERSITY IN PRAGUE

FACULTY OF ELECTRICAL ENGINEERING

DEPARTMENT OF ELECTRIC DRIVES AND TRACTION



Master Thesis

# Minimal Design of IO-link Device

*Bc. Denys Postoialko*

Supervisor: Ing. Filip Vodrážka

Study Programme: Electrical Engineering, Power Engineering and Management

Specialization: Electrical Machines, Apparatus and Drives

26th of May 2017

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

# ZADÁNÍ DIPLOMOVÉ PRÁCE

## I. OSOBNÍ A STUDIJNÍ ÚDAJE

Příjmení: **Postoialko** Jméno: **Denys** Osobní číslo: **453159**

Fakulta/ústav: **Fakulta elektrotechnická**

Zadávající katedra/ústav: **Katedra elektrických pohonů a trakce**

Studijní program: **Elektrotechnika, energetika a management**

Studijní obor: **Elektrické stroje, přístroje a pohony**

## II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

**Minimal design of IO-link device**

Název diplomové práce anglicky:

**Minimal design of IO-link device**

Pokyny pro vypracování:

1) Create overview of the IO-Link standard.
2) Create the schematic and PCB layout of the IO-Link Device Minimal Design in Eagle software.
3) Prepare test plan based on the IO-Link standard.
4) Execute planned tests with the IO-Link Device Minimal Design.
5) Create necessary documentation for the project.

Seznam doporučené literatury:

[1] IO-Link Interface and system specification V1.1.2, 07/2013, IO-Link Community 10.002
[2] IO-Link Test specification V1.1.2, 07/2014, IO-Link Community 10.032
[3] IO-Link system Functional manual, 01/2013, SIEMENS A5E31637677-AA
[4] Programmable controllers . Part 2: Equipment requirements and tests, International standard, IEC 61131-2
[5] M. Duncan: EAGLE V6 Getting Started Guide, 2013, ISBN 978-1-907920-20-2

Jméno a pracoviště vedoucí(ho) diplomové práce:

**Ing. Filip Vodrážka, Siemens, s.r.o.**

Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) diplomové práce:

Datum zadání diplomové práce: **13.01.2017** Termín odevzdání diplomové práce: **26.05.2017**

Platnost zadání diplomové práce: **30.06.2018**

| Podpis vedoucí(ho) práce | Podpis vedoucí(ho) ústavu/katedry | Podpis děkana(ky) |
|---|---|---|

## III. PŘEVZETÍ ZADÁNÍ

Diplomant bere na vědomí, že je povinen vypracovat diplomovou práci samostatně, bez cizí pomoci, s výjimkou poskytnutých konzultací. Seznam použité literatury, jiných pramenů a jmen konzultantů je třeba uvést v diplomové práci.

| Datum převzetí zadání | Podpis studenta |
|---|---|

# Acknowledgements

Here I would like to thank my supervisor Ing. Filip Vodrážka, who helps me throughout all time of the project and takes the greatest part in the diploma thesis preparation. In addition, I would like to thank all members of SIEMENS REMOTE IO team, namely: Leader of the project – Oto Guertler, hardware supervisors – Jiři Polický and Viktor Žalud, firmware supervisors – Miloš Fenyk; Tomás Dirbak and Ondřej Volf, without whose help this project will not be done and realized.

# Prohlášení

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

# Declaration

I declare that the submitted work I have produced independently and have listed all used information sources in accordance with the Methodological Guideline on Ethical Principles of the Preparation of University Graduate Thesis.

Prague, 26th of May, 2017 ..... Denys Postoialko

# Abstrakt

Cílem diplomové práce " Minimal Design of IO-link Device " je návrh zcela nového zařízení IO-Link pro SIEMENS, které by mělo mít minimální velikost a vlastnosti, které předepisují technické normy. Podobně popis všech hlavních technických rozhodnutí, výrobních bodů bude prezentován v diplomové práci, stejně jako celá řada testů a experimentů.

# Abstract

The aim of the master thesis “Minimal Design of IO-link Device” is the design of fundamentally new IO-Link Device for SIEMENS, which should has minimal size and possesses the qualities described by technical norms. Likewise, the description of all main technical decisions, production points will be presented in the thesis as well as whole range of tests and experiments.

# Contents

# 1. Introduction

IO-Link is a special digital communication for easily connection and communication of various sensors and actuators mainly by serial bus. The main advantages of IO-Link is easy connection to fieldbus, fast automatic transmission of measured values, remote tuning and configuration with automatic sensors and detailed control functions. The big advantage is backward compatibility with conventional switched output.

IO-Link is a fairly new digital point-to-point communication type focused mainly on the current intelligent sensors and actuators for industrial automation. It originated as digital substitution of still predominant analog outputs 0-10 V 4-20 mA, or as a substitution of the switch outputs.

Normally, sensors with IO-Link communication connected to bus systems through the Managing input-output modules (Remote I/O devices). This function in the event of IO-Link communication takes IO-Link Master, which maps connected IO-Link Devices and acts as a gateway to superior fieldbus. With help of the IO-Link the Master can transmit, control and diagnostic data from the sensor and vice versa recoveries readings. This sensor can be operated remotely fully, including changing its settings or detecting its status. Although the sensor equipped with IO-Link is also still backwards compatible with traditional switching signals compliant with IEC 61131-2 [1].

The integrated communication requirements for last years have been increasing. At the same time, sensors and actuators are becoming more intelligent. This is where the Siemens solution can fulfil the highest level of automation and quality of the increasing number of IO-Link products. As an open interface, IO-Link can be integrated into all automation systems and fieldbus communications. Consistent interoperability fulfills maximum investments protection. IO-Link enables the automatic integration of the measured points for energy control systems without additional costs. This makes it easy to determine and then analyze energy consumption.

The Siemens takes great part of IO-Link market. Today the Siemens IO-Link portfolio is presented mainly from IO-Link Masters from SIMATIC series such as ET 200eco, ET 200pro, ET 200S; and communication modules such as ET 200SP, ET 200AL, S7-1200. The IO-Link Device from Siemens is presented only by K20 module, which allows connect up to 8 binary sensors in one Device and can be connected to the Master, however it is really old block that requires redesign [2].

The main goal of this thesis is to design completely new IO-Link Device for Siemens, which contributes to occupy a niche of IO-Link Devices on the market. The designed IO-Link Device must fulfil requirements determined by Siemens and pass all kinds of tests and certifications.

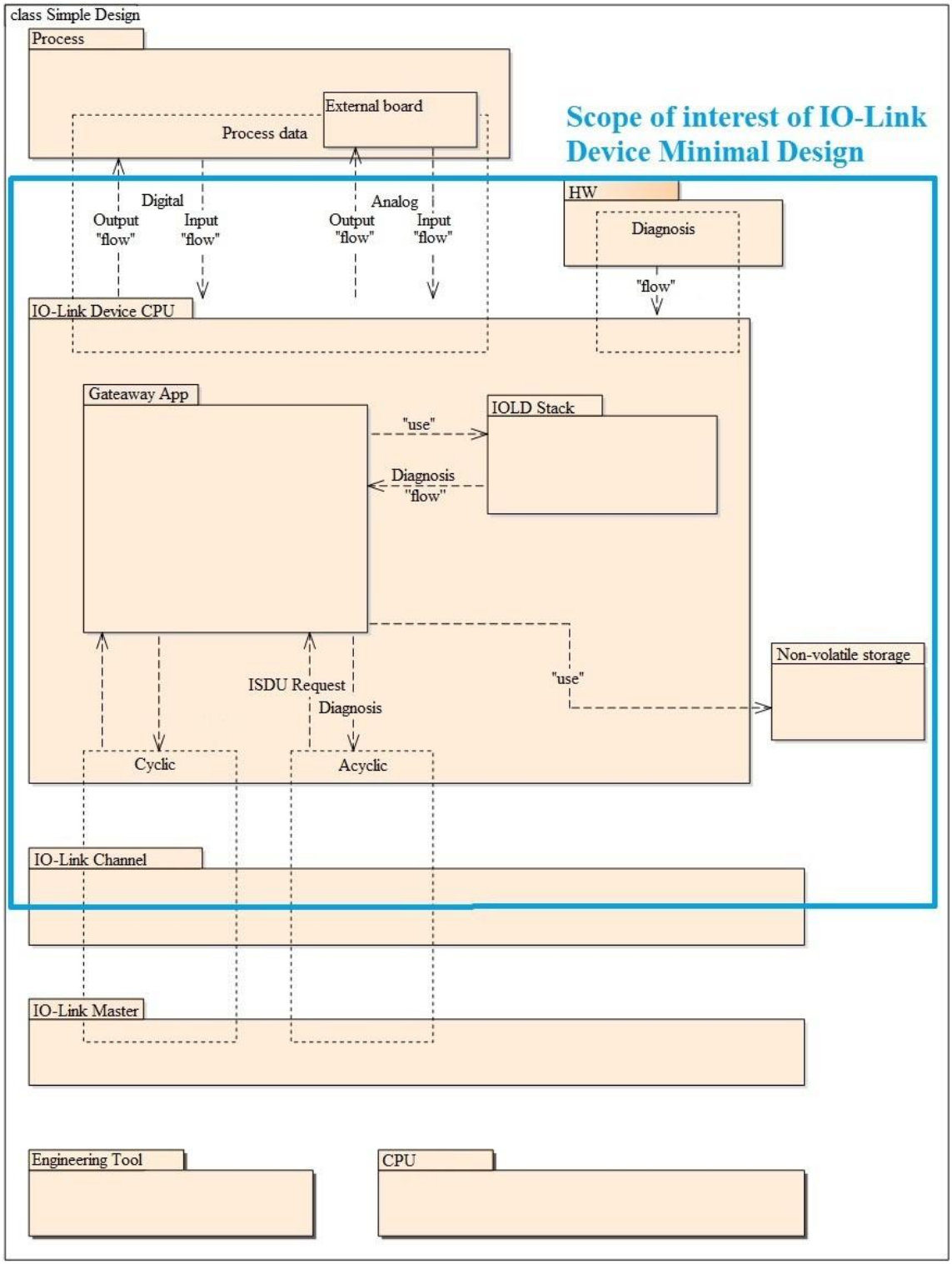



*Figure 1.1: Scope of interests of IO-Link Device Minimal Design*

## 1.1. Thesis outline

Chapter 2 provides a brief introduction of the IO-Link construction and communication. Chapter 3 defines requirements determined by SIEMENS and main view of the future Device. Chapter 4 presents time schedule of planned work. Chapter 5 contains calculations and expected limits of use. Chapter 6 presents results of modelling and manufactured prototype. Chapter 7 contains part of tests, which the Device must fulfill. Chapter 8 presents conclusion of the thesis.

# 2. Introduction to IO-Link

This chapter presents the most known parts and representations of IO-Link communication and devices. The description and formal definition of communication between Master and Device are provided.

## 2.1. Topology of IO-Link communication

IO-Link is a protocol for connecting of devices standardized according to IEC 60947-5-2 [3]. The architecture of the constructed network based on this protocol consists of:

- IO-Link Master;
- IO-Link Device - mainly sensors and drives;
- Standard three/five-wire connectors.

Basic communication structure is practically a star, in center of which is the IO-Link Master, which controls and communicates with Slave units (Devices) by point-to-point communication, which transmits data automatically, gets and sends they back. Physically Master must have as many connecting interfaces (connectors) as many units (sensors) must be connected. This eliminates the need for addressing units at the actual IO-Link communication level.

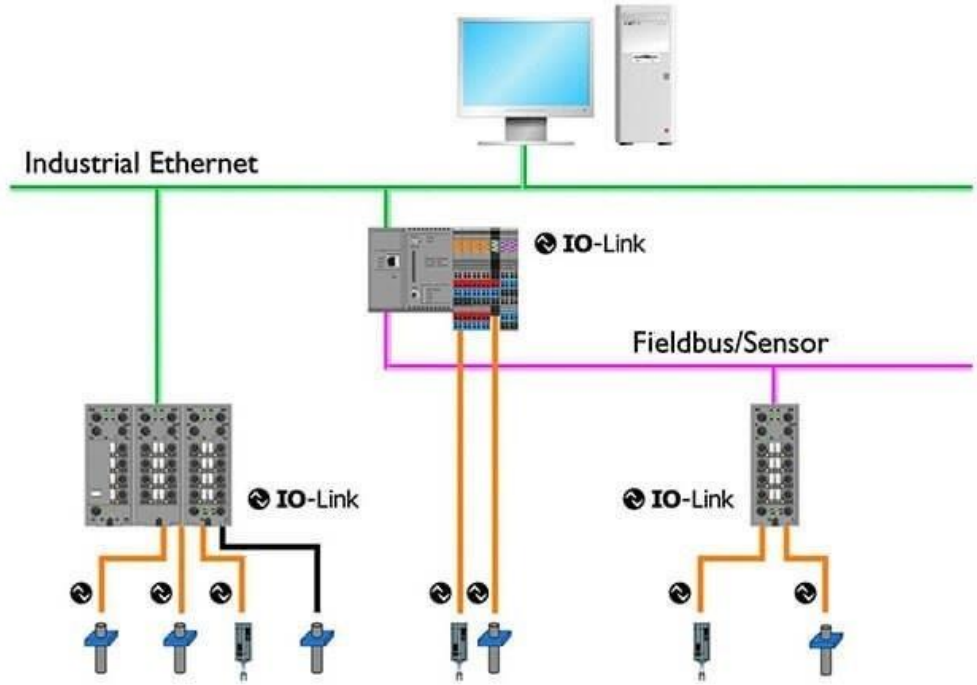



*Figure 2.1: Example of IO-Link architecture* [4]

Transfer Model consists of physical layer (PHY), a data line layer (DLL) and of the application layer (AL), which is watched by the operating system. Moreover, each Master output for every

connected Slave units has its own physical and link layer. Application level of IO-Link communication is one common for all Slave units.

| Transfer layers model | Description |
|---|---|
| AL (Application Layer) | Defines and implements services and protocols for access to processes and data on demand (parameters, events, services) |
| DLL, DL (Data Link Layer) | Describes, defines and implements data transfer between Master and Slave unit |
| PHY, PL (Physical Layer) | Describes the physical properties of transmission and provides access to the transmission (cable) |
| SM (System Management) | A special layer - defines and implements the start of communication on the part of the Master and Slave units |

*Table 2.1: Table of transfer model communication IO-Link bus*

Communication is realized as transmission of many telegrams in form of simple bytes, which then together they form one transmission frame contained all necessary useful data for realizing of the transmission. Framework already creates DLL. It takes care about not only the preparing of useful data that must be transferred, but also performs basic decoding commands and services that must to be performed. This is provided and made by the most secure application layer that defines and executes the required services, protocols for access to the processes, and desired information (process data, parameter settings, events, services). Independently of this structure system management operates and provides binding, respectively, initiating of communication and basic management.

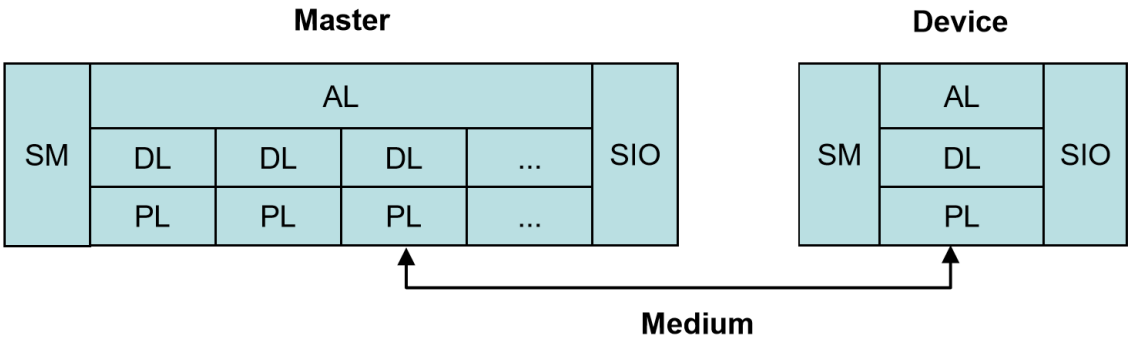



*Figure 2.2: Transfer communication model on the Master and Device side* [5]

## 2.2. Physical layer

Physical layer (PHY) is a process, by which Master and Slave unit physically transmit data. PHY represents a known and proven 8-bit asynchronous serial data transmission (UART). Therefore, the length of two or three wire communication cable is limited to 20 m and the transmission rate may be 4.8, 38.4 or 230.4 kilobytes / sec.

| Baud Rate | $T_{cycle}$ | Frames |
|---|---|---|
| 4.8 kBaud | 18 ms | 21 000 |
| 38.4 kBaud | 2.3 ms | 35 000 |
| 230 kBaud | 0.4 ms | 55 000 |

*Table 2.2: Table of transmission speeds, the cycle times (Tcycle) and the number of transmitted frames* [5]

Coding of bits in serial transmission is made by the Non Return to Zero unit, where the state logic "1" corresponds to 24V between the wires L+ and C/Q. State logical "0" corresponds to 0V between same wires. According to these the bit coding in IO-Link communication can use already mentioned possibility of two-wire or three-wire interface, which is referred as PHY1 and PHY2 respectively.

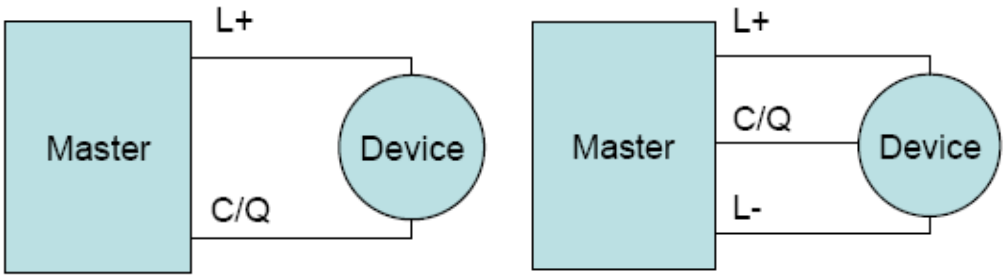



*Figure 2.3: Possible implementation of IO-Link interface: two-wire communication PHY1 (left) and three-wire communication PHY2 (right)* [5]

For PHY1 communication and power supply of Slave unit (sensor) is carried out through the two wires L+ and C/Q thanks to time division multiplexing. For this reason, it is not necessary to keep the minimum transfer time $T_{Cycle}$ and the maximum transmission speed is only 4.8 kbit/s. For PHY2 bits transferring already uses a special wire C/Q and continuously power supply the L+ and L-. Therefore, there is no necessary time division multiplex. Sometimes it can be met 5-wires interface, which have galvanic isolated additional power supply Ua, which is used for isolated power actuator (see Figure 2.4).

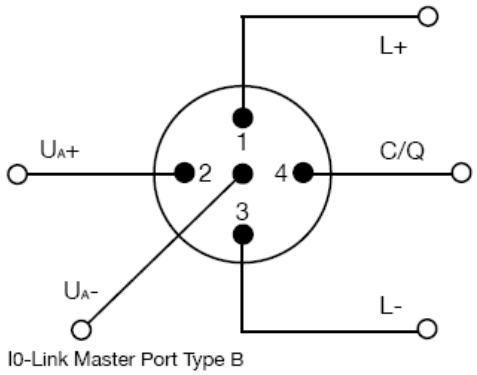



*Figure 2.4: 5-wire IO-Link connector* [5]

From the viewpoint of physical connection the IO-Link standard defines connectors that can be used for connection. These are euro connectors M5, M8 and M12, on the Master side connector is defined as female, on the Slave side as male.

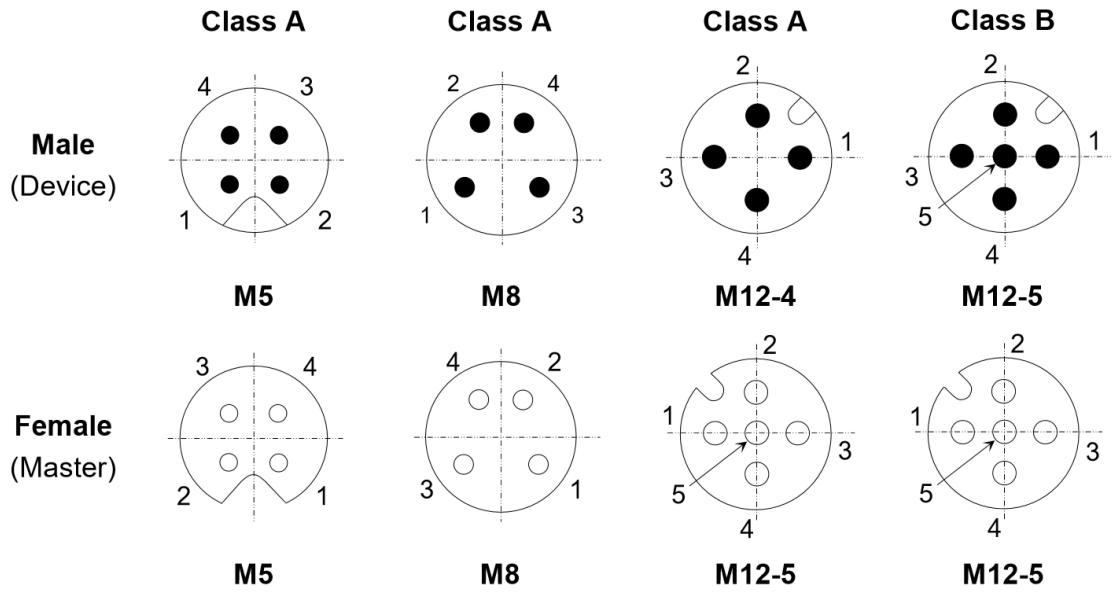



*Figure 2.5: Possible connectors for realization of IO-Link communication* [5]

Names of pins are standardized by IEC 60947-5-2 [3]:

pin 1 – power supply 1L+,

pin 2 – power supply 2L+,

pin 3 – 1M,

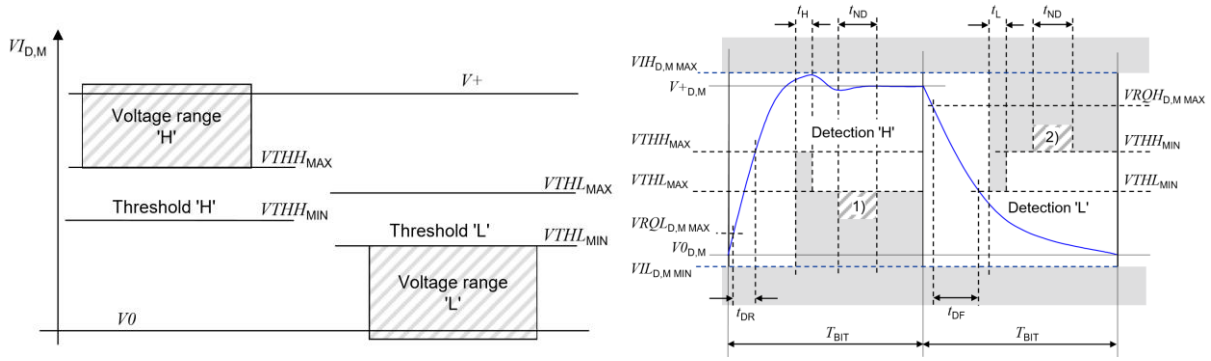
pin 4 – signal C/Q,

pin5 – 2M.

For a correct transition from one level to another, it is necessary to meet the voltage requirements, and the requirements of time (see Figure 2.6). The values of voltage levels are defined in Table 2.3.

| Parameter | Designation | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| $VTHH_{S,M}$ | Input threshold "H" | 10.5 | n/a | 13 | V | Note 1 |
| $VTHL_{S,M}$ | Input threshold "L" | 8 | n/a | 11.5 | V | Note 1 |
| $VHYS_{S,M}$ | Hysteresis between input thresholds "H" and "L" | 0 | n/a | n/a | V | Note 2 |
| $VIL_{S,M}$ | Permissible voltage range "L" | 1 | n/a | n/a | V | |
| $VIH_{S,M}$ | Permissible voltage range "H" | n/a | n/a | 1 | V | |
| Note 1: Thresholds are compatible with definition of Type 1 digital inputs in IEC 61131-2 [1].<br>Note 2: Hysteresis voltage VHYS = VTHH-VTHL | | | | | | |

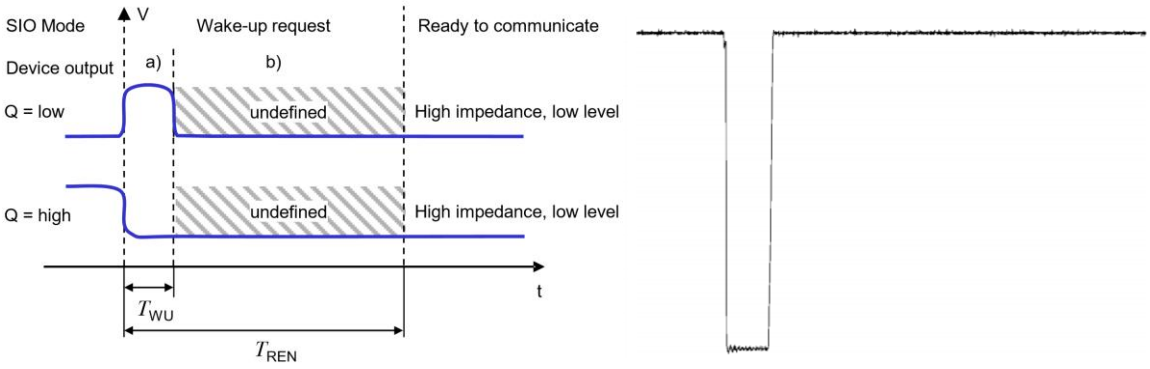
*Table 2.3: Static parameters of receiver* [5]




a) switching thresholds b)switching thresholds

*Figure 2.6: Signal properties of IO-Link communication* [5]

Wake-up procedure is defined as a pulse for initiating of communication. Device in Standard I/O mode can act as binary sensors and have the output permanently to "0" or "1". Therefore, in the specification it is presented in two versions, as shown on Figure 2.7. In any case, the signal reaches the desired level for the initial launch of communications.




a) wake-up specification b) wake-up request

*Figure 2.7: Wake-up properties* [5]

Time characteristics of the wake-up process are described in the Table 2.4.

| Parameter | Designation | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| $T_{WU}$ | Pulse duration of wake-up request | 75 | n/a | 85 | µs | Master property |
| $T_{REN}$ | Receive enable delay | n/a | n/a | 500 | µs | Device property |

*Table 2.4: Wake-up request definitions* [5]

After receiving the wake-up pulse, the Device expects the UART adaption of a character from the Master. Since the Device supports only one communication speed, it can accept valid data transmitted only with the supported rates. Master usually begins transmission at the highest communication speed. If Device is unable to connect at a given speed, Master repeats attempt with lower speeds. After receiving a valid character, Device responds and the communication is established. Master gave clear information on what speed the following communication will take place. An example of this process is in Figure 2.8.

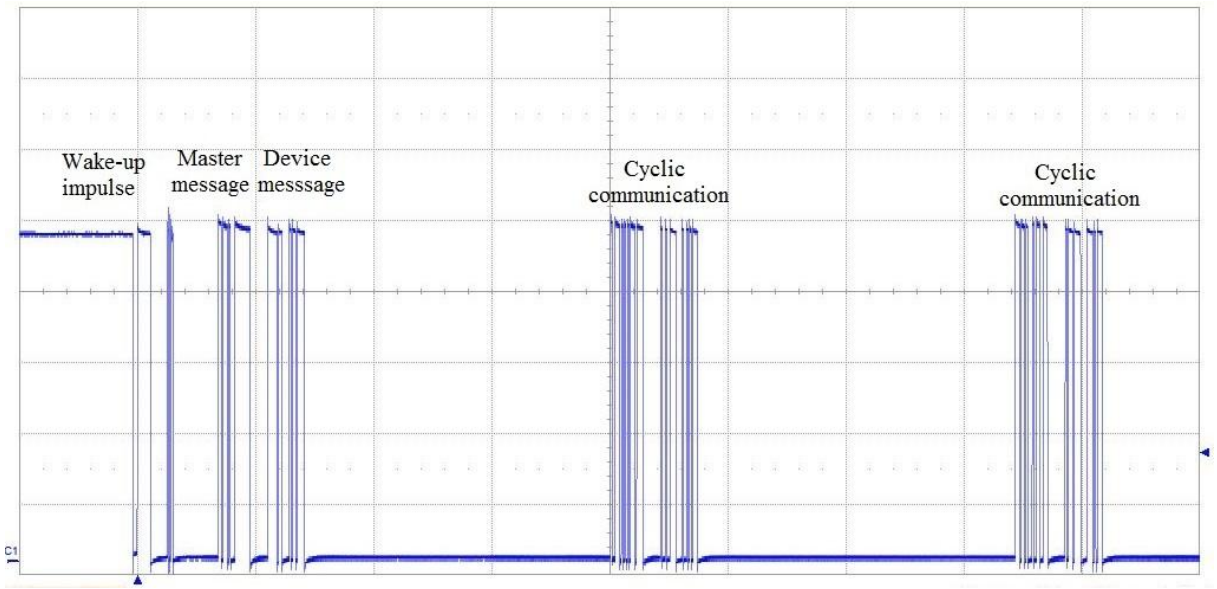



*Figure 2.8: Example of communication process*

## 2.3. Possibility of IO-Link as the traditional switching output

Slave units designed for IO-Link communication support Standard I/O mode and IO-Link mode. Standard I/O mode represents a classic mode with switching output signal from the Slave unit, which normally has a majority of current sensors. On the Master side, signal level is evaluated as a discrete switching signal. On the Slave unit side, discrete signals (levels) are received and transmitted at the pin C/Q.

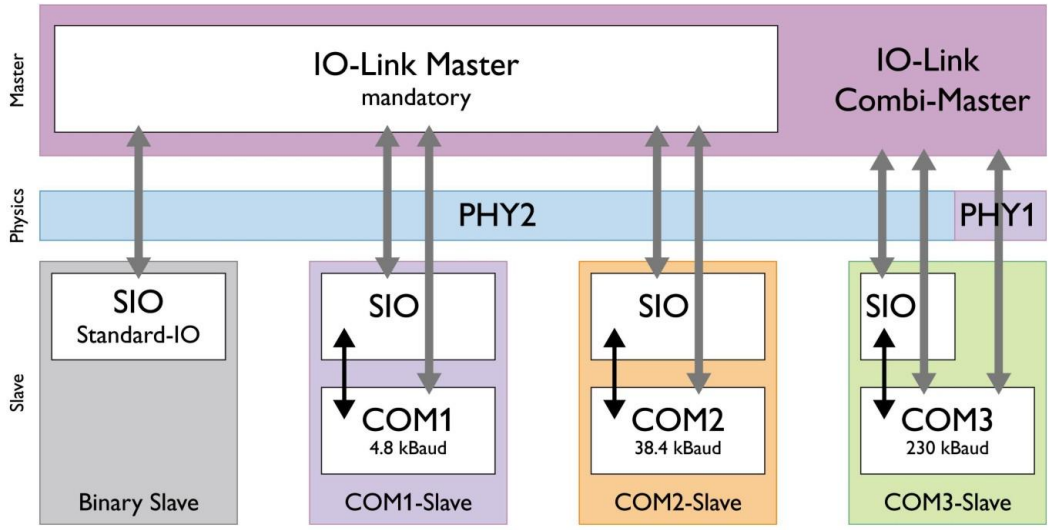



*Figure 2.9: Possibility of connection of IO-Link Slave units to Master* [6]

## 2.4. Data link layer

The data link layer is the main part of the IO-Link communication because it regulates the data transmission via IO-Link interface and serves as an operational interface between the software application layer and hardware physical layer.

User data sent from the application via the application layer in the data link layer are organized into telegrams for transmission by physical layer, where the meaning of transmitted bytes is defined by the frame type and datalink command that is added to the link layer.

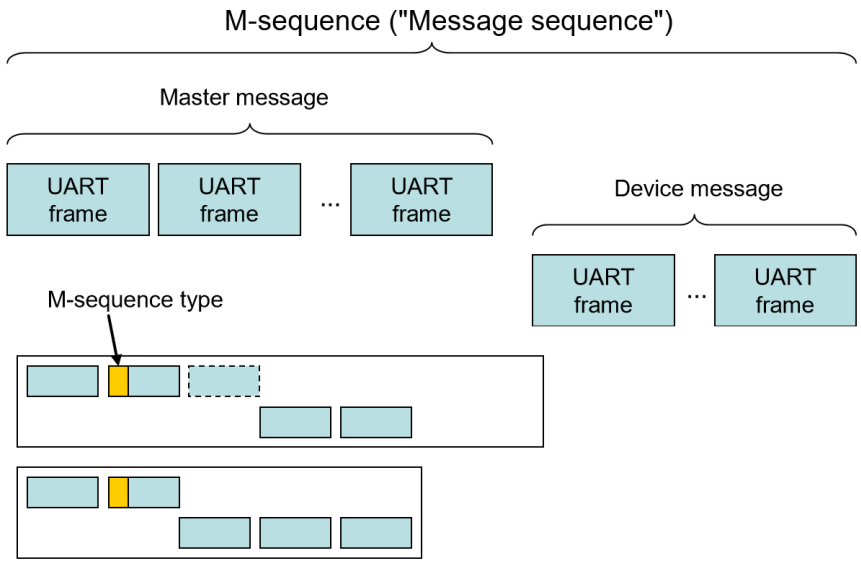



*Figure 2.10: Construction of IO-Link frame* [5]

In IO-Link case, the communication is a direct transfer of UART telegram through IO-Link interface either in the Master-Slave direction or in Slave-Master direction. Group of telegrams, which realize a communication between Master and Slave units, is a Frame. Types of frames are fixedly defined by standard and define the combinations of the signals from the Master and Slave units depending on transmitted data in both directions.

Each frame incorporates information about the Data channel of IO-Link communication, while each frame type represents a different type of data channel and thus transmits different data, information and requirements. Their specifications meet the diverse requirements of sensors or actuators to the width and the amount of process data and the current operating conditions, and transmission.

Sending data vary according to its purpose, determined by the frame type and the type of the data channel, and divides to:

- **Process data** - information transmitted with high priority according to a fixed schedule. Transfer starts automatically on startup sequence without the need to request an application. Process data includes measured values and the control variable. Cycle of process

data defines the timetable for sending process data about each station. Depending on the amount of items of data channel it can contain one or more cycles.

- **On-request data** - information that is transmitted acyclical to request from application. To this type of parameters belong Slave application parameters and data of various events.
- **Direct parameters / diagnostic data** - specific data on request that are transmitted without confirmation in a dedicated data channel.
- **Events / Service PDU** - information on request. Its transfer is initiated by setting a flag in the event CHK/STAT byte in Slave unit located in a dedicated data channel. Events can be initialized by the application or communication protocol. Transfer "Service PDU" realizes the transmission of large amounts of data with a request for confirmation. It uses such as exchange application data objects.

In the IO-Link communication specification, the above data types (process data, diagnostic data, on-request data and events) are mediated through the various channels. They are independent of each other and precisely define the property of transmitted data in each frame, i.e. they practically tell the Master and Slave units what data they are and how they should be handled (where to store, how to process, etc.). Thus, data channels make routes that accurately transmit the data to the correct storage or processing location. The data channel forms part of the so-called DL command (dataline command). These are used to provide read or write access to the four data channels defined above.

## 2.5. Application layer

The application layer of IO-Link communication is used as such as the interface between the DLL and the parent application. AL receives a decoded frame from the link layer in the way that it receives information about the service, which has to be performed and what kind of data must be used, conversely, passes the DLL information about what to do.

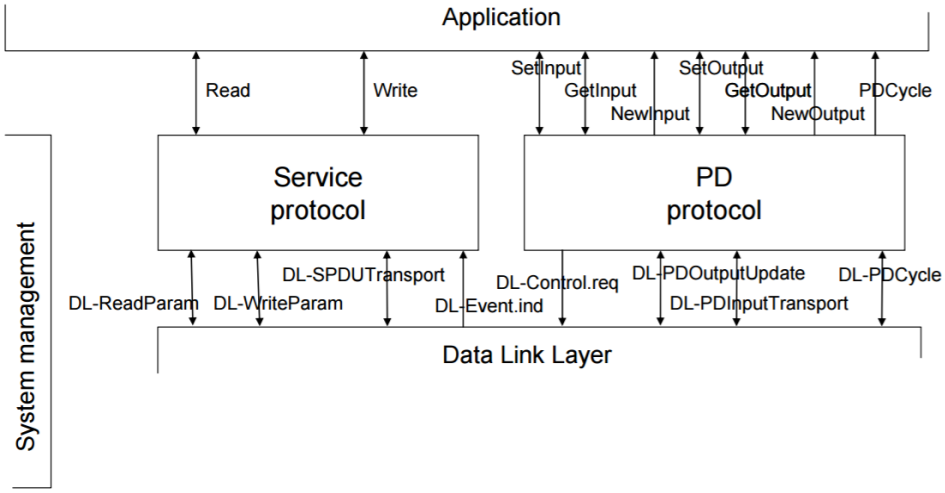



*Figure 2.11: Structure and interface of the AL* [5]

The available services depend on the unit type. Master and Slave units have exactly defined roles as well as the client and server in the context of executing individual AL services. For example, in the case of Master, it is possible to name the services of writing, reading, interrupting, rejecting, defining, setting or reading of the input or output etc.

| Service | Description of service/ command | Type of data | Master | Slave |
|---|---|---|---|---|
| Read | Read on-request data from the specified Slave port | On-request data | AL generates request - sends | AL accepts the request and responds |
| Write | Writing on-request data at the specified Slave port | On-request data | AL generates request - sends | AL accepts the request and responds |
| Abort | Command to stop the previous reading or writing | On-request data | AL generates request - sends | AL accepts the request and responds |
| Reject | Rejecting read / write request | On-request data | AL generates request - sends | AL accepts the request |
| NewInput | The application information indicates that new process data is available in the DLL Master Unit | Process data | Generates AL and transmits to the parent application | nothing |
| GetInput | Request to read process data from the DLL Master Unit | Process data | Generates the parent application itself into AL | nothing |
| SetInput | Request to update a process data in the DLL Slave Unit | Process data | nothing | Generates the parent application itself into AL |
| PDCycle | Information about the end of the process data broadcast | Process data | nothing | AL generates and transmits to the parent application |
| GetOutput | Request to reread process data from DLL of Slave Unit | Process data | nothing | Generates the parent application itself into AL |
| NewOutput | The parent-application information indicates that new process data is available in DLL Slave Drive | Process data | nothing | AL generates and transmits to the parent application |
| SetOutput | Request to update process data in the DLL Master Unit | Process data | Generates the parent application itself into AL | nothing |
| Event | Event or error message in AL | - | Receives events from Slave Unit | Generates and receives events |
| Control | Passing control data from master to slave unit | - | AL generates and sends control data | AL receives and processes control data |

*Table 2.5: List of services and commands AL IO-Link communication* [5]

## 2.6. Great range of IO-Link possibilities

Although IO-Link is "just" a non-network communication standard, the structure of the standard is quite complex between the control system and the individual units, mostly by the formation of different sensors. This makes it not easy to swap various IO-Link encoders without the need for a complicated reprogramming of the control system. The sensors from one family can be set up immediately by simply uploading the operating parameters stored in the control system. Fortunately, there is no need to program the communication because specialized integrated microcontrollers, converters and transceivers are already on the market and already run IO-Link. This fact is also confirmed by the great number of companies, which product whole range of IO-Link Masters and Devices with sensors, encoders and controllers.


*Figure 2.12: IO-Link members* [5]

# 3. IO-Link Device Minimal Design requirements

For IO-Link Device Minimal Design was put forward the following functional requirements and quality attributes:

**1. General Behavior**

1. IOLD shall fulfill IO-Link specification V1.1 [5], [7];
2. IOLD shall have protected and programmable SPI channel as an interface for external boards connection (analog input/output prototyping by internal or external developer);
3. Configurable in full range of IO-Link parameters according to the specification;
4. Data Storage Functionality shall be supported;
5. IO-Link FW update support;
6. Crystal has to be selected to be possible to configure with required precision;
7. MCU shall have all GPIOs/peripheries used;
8. IOLD shall have defined pin header for connection to external process board part:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| +3V3 | GPIO1 (MOSI) | GPIO2 (MISO) | GPIO3 (CLK) | GPIO4 (CS) | GPIO5 | GPIO6 | GPIO7 | GPIO8 | +3V3 |
| GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |

*Table 3.1: Pinout of pin header*

9. AD converter MCU periphery input should be placed as alternate function of GPIO5-6 if the selected MCU has this periphery;
10. I2C MCU periphery input should be placed as alternate function of GPIO7-8 if the selected MCU has this periphery;
11. There shall be 2A protection of the input 1L+ power supply.

**2. HW Requirements**

1. MCU shall have UART periphery (TX, RX) for IO-Link communication;
2. MCU's UART periphery shall transfer data at maximum with 230400 Bauds;
3. IOLD shall contain non-volatile storage with at least 3 kB;
4. IOLD shall contain volatile storage for storing of 1000 trace messages (16kB of RAM spared just for this);
5. MCU shall be ARM based;
6. As small as possible;
7. As cheap as possible;
8. Status LEDs based on the IO-Link spec (probably one red and one green LED);
9. Reserved 4 GPIOs for future use;
10. Under voltage detection - threshold configurable by resistor components;
11. Enough internal memory in the MCU for adding technology code in the future (32k FLASH, 16k RAM);

12. 2kB internal FLASH for data storage;
13. Based on STM IO-Link PHY;
14. Fulfill of IO-Link conformance test;
15. Temperature range -40°C to 60°C ambient;
16. Design to EMC requirement;
17. Minimal power dissipation;
18. Polarity protection;
19. 1L+ Power supply (from 18V to 30V);
20. M12 IO-Link connector;
21. Internal watchdog available on MCU;
22. J-Tag periphery or Serial Wire Debug (SWD) interface shall be available on MCU.

**3. Maintainability**

1. FW of IOLD shall be updatable according to IO-Link FW update specification;
2. Traces messages shall be stored volatility;
3. Fatal error messages shall be stored non-volatility.

**4. Usability**

1. JTAG connector is placed on a board in such a way that it is accessible without completely removing of housing - e.g. if the bottom part of housing is removable then after simply removing of this cover the J-Tag (with pinout reduction) shall be connected without any collision with other parts.

# 4. Tasks and time planning for the project

The project “The Minimal Design of IO-Link Device” needs very careful planning since it is made under leadership of SIEMENS and its technicians. Standardly, the development of any SIEMENS product passes the development stages as known as milestones. The main milestones are creation of idea, creation of new project with distinctive name and responsibility persons, designing schematics and layouts, production with subsequent testings, presentation the new device on the market.

The longest part of any design for hardware designer is making the electrical scheme and production, which depends on producer. It can continue from 2 to 8 weeks.

Officially, start of the project was appointed on start of November and finished in the end of May. The result of the project must be a production of 15 working prototypes with completely prepared documentations, schematics, layouts, orders and test plans.

The list of planning activities is shown in Table 4.1.

| Activities | Working week | Date |
|---|---|---|
| Functional specification. Collecting and preparing all project requirements. Requirements negotiation with potential producers | 3 weeks | 7.11.16 – 27.11.16 |
| Schematic drawing. Making of calculations and simulations. Preparing basic design | 4 weeks | 28.11.16 – 15.1.17 |
| Layout | 4 weeks | 16.1.17 – 12.2.17 |
| HW detailed design document | 4 weeks | 30.1.17 – 19.2.17 |
| Prototype production. Soldering of components. Delivery | 6 weeks | 13.2.17 – 26.3.17 |
| Tests and test report creation | 6 weeks | 27.3.17 – 7.5.17 |
| Result presentation | 1 week | 8.5.17 – 15.5.17 |

*Table 4.1: Project time planning*

As it was mentioned above the longest and hardest part of design of IO-Link Device Minimal Design were making the electrical scheme and subsequent layout.

# 5. Design and calculations

## 5.1. Block diagram

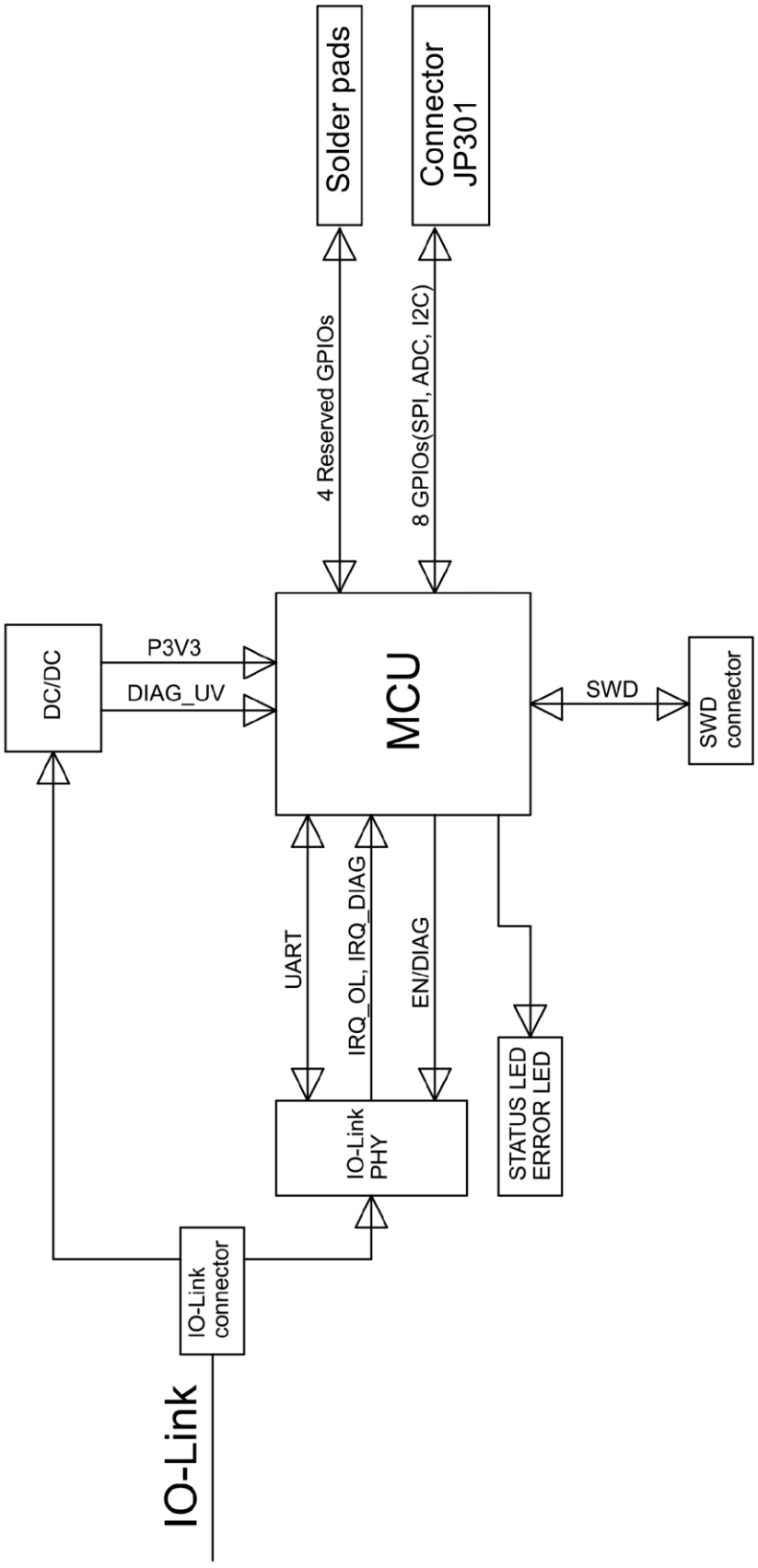



*Figure 5.1: Block diagram of future module*

## 5.2. Power supply

Power supply as a heart of any device must fulfill a great range of requirements such as voltage and current ripple, EMC requirements, undervoltage and overcurrent protections. In the IO-Link Device Minimal Design the power supply takes the greatest part of future design.

According to the requirements power supply should work in 18-30V input voltage range, provides at least 0.1A forward current, has the lowest power dissipation, has the smallest size according to concept of Minimal Design, has voltage supervisor, and fulfills EMC requirements.

During the choice, the main attributes of DC/DC converter were type of package, voltage stability, current-efficiency characteristic, availability of necessary protections and being in the stock. On the market, there are a great list of possible variants, among which were chosen next one:

| **Characteristic** | **TPS5401DGQT** | **TPS54040ADRCT** | **LT3502EDC** | **LT3502AIDC** |
|---|---|---|---|---|
| Input voltage, V | 3.5-42 | 3.5-42 | 3-42 | 3-40 |
| Output voltage, V | 0.8-39 | 0.8-39 | 0.8-36 | 0.8-36 |
| Forward current, A | 0.5 | 0.5 | 0.5 | 0.5 |
| Package | MSOP-10 5.0x3.0mm | MSOP-Power PAD-10 3.0x3.0 mm | DFN-8 2.0x2.0 mm | DFN-8 2.0x2.0 mm |
| Efficiency | Eco-mode allows achieve good efficiency at low loads | Eco-mode allows achieve good efficiency at low loads | | |
| Protections | Undervoltage, overvoltage, overcurrent, soft start, adjustable undervoltage operating point | Undervoltage, overvoltage, overcurrent, soft start, adjustable undervoltage operating point | Short-circuit robust, soft start | Short-circuit robust, soft start |
| Price, Kč | 38.37 farnell.com wasn't in stock | 80.61 farnell.com | 114.57 farnell.com | 153.22 farnell.com |

*Table 5.1: Comparison of DC/DC converters*

After analysis TPS54040 was chosen as a base for DC/DC buck converter in MSOP-Power PAD-10 package.

The simple scheme of TPS54040 and its passive elements connection is shown on Figure 5.2.

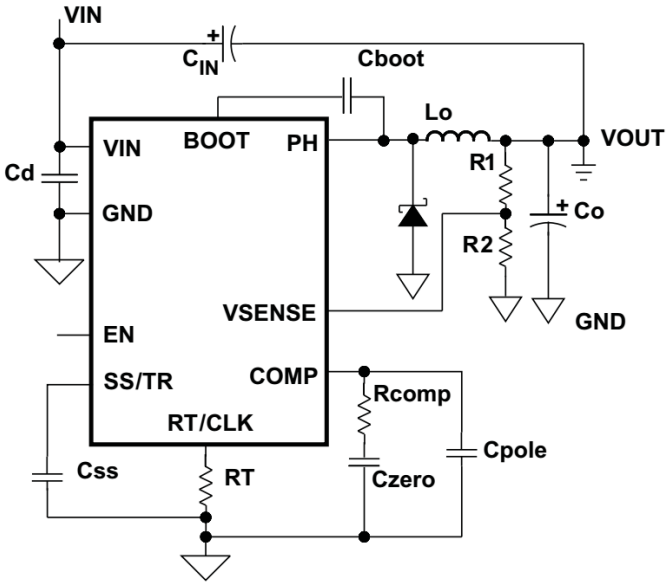



*Figure 5.2: Simple schematic of TPS54040A* [8]

## 5.2.1. Calculations

**1. Selecting the switching frequency**

The switching frequency of the TPS54040A is variable in wide range from 100 kHz to 2.5 MHz. The design of power supply starts from calculation of maximal possible frequency.

Maximal possible frequency for our case [8]:

$$f_{sw.max}=\left(\frac{1}{t_{ON}}\right)\cdot\left(\frac{I_L\cdot R_{dc}+V_{OUT}+V_d}{V_{IN}-I_L\cdot R_{hs}+V_d}\right)=\left(\frac{1}{130\text{ns}}\right)\cdot\left(\frac{0.1\text{A}\cdot 0.13\Omega+3.3\text{V}+0.5\text{V}}{30\text{V}-0.1\text{A}\cdot 0.4\Omega+0.5\text{V}}\right)=962.9\text{ kHz},\quad(5.1)$$

where $t_{ON}$ - controllable on time; $I_L$ - load current, $R_{dc}$ - inductor resistance, $V_{OUT}$ - output voltage, $V_{IN}$ - maximal input voltage, $R_{hs}$ - switch resistance, $V_d$ - diode voltage drop.

By datasheet 700 kHz frequency is advised for standard applications, then

$$RT(k\Omega)=\frac{206033}{(f_{sw}(kHz))^{1.0888}}=\frac{206033}{(700)^{1.0888}}=164.5\text{ k}\Omega\Rightarrow 180\text{ k}\Omega\text{ . [8]}\qquad(5.2)$$

Switching frequency will be

$$f_{sw}(kHz)=\sqrt[1.0888]{\frac{206033}{RT(k\Omega)}}=\sqrt[1.0888]{\frac{206033}{180}}=644\text{ kHz}\ .$$

Since resistor has 1% precision, switching frequency can differ from calculated value.

For RT=180kΩ + 1%=181.8kΩ => $f_{sw}$ = 614 kHz;

for RT=180kΩ - 1% = 178.2kΩ => $f_{sw}$ = 684 kHz.

## 2. Output inductor selection

$K_{IND}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low equivalent series resistance output capacitors such as ceramics, a value as high as $K_{IND} = 0.3$ may be used.

Minimal value of inductor [8]

$$L_{omin} = \frac{V_{INmax}\text{-}V_{OUT}}{I_o \cdot K_{IND}} \cdot \frac{V_{OUT}}{V_{INmax} \cdot f_{sw}} = \frac{30V\text{-}3.3V}{0.1A \cdot 0.3} \cdot \frac{3.3V}{30V \cdot 644kHz} = 152\ \mu H \Rightarrow L_o = 180\ \mu H\ .\ [8] \quad (5.3)$$

Current ripple in the inductor

$$I_{ripple} = \frac{V_{OUT} \cdot (V_{INmax}\text{-}V_{OUT})}{V_{INmax} \cdot L_o \cdot f_{sw}} = \frac{3.3V \cdot (30V\text{-}3.3V)}{30V \cdot 180\mu H \cdot 644kHz} = 25mA\ .\ [8] \quad (5.4)$$

RMS and peak inductor currents

$$I_{Lrms} = \sqrt{(I_o)^2 + \frac{1}{12} \cdot \left( \frac{V_{OUT} \cdot (V_{INmax}\text{-}V_{OUT})}{V_{INmax} \cdot L_o \cdot f_{sw}} \right)^2} = \sqrt{(0.1A)^2 + \frac{1}{12} \cdot \left( \frac{3.3V \cdot (30V\text{-}3.3V)}{30V \cdot 180\mu H \cdot 644kHz} \right)^2} = 110mA\ ,[8] \quad (5.5)$$

$$I_{Lpeak} = I_O + \frac{I_{ripple}}{2} = 0.1A + \frac{25mA}{2} = 113mA\ .\ [8] \quad (5.6)$$

Choose $L_o$ = 180µH 0.1A inductor.

## 3. Output capacitor

There are three primary provisions for selecting the output capacitor value.

The output capacitance need to be enough to supply the current difference for 2 clock cycles while only allowing droop in the output voltage.

$$C_{out} > \frac{2 \cdot \Delta I_{OUT}}{f_{sw} \cdot \Delta V_{OUT}} = \frac{2 \cdot 0.1A}{644kHz \cdot 1\% \cdot 3.3V} = 9.41\mu F \Rightarrow 10\mu F\ ,\ [8] \quad (5.7)$$

where $\Delta I_{OUT}$ - change in output current, $\Delta V_{OUT}$ - allowable change in the output voltage.

The minimum capacitance has to keep the output voltage overshoot to a desired value

$$C_{out} > L_o \cdot \frac{(I_{oh}^2\text{-}I_{ol}^2)}{(V_f^2\text{-}V_i^2)} = 180\mu H \cdot \frac{(0.1^2A\text{-}0^2A)}{(((1+1\%) \cdot 3.3V)^2V\text{-}3.3^2V)} = 8.22\mu F \Rightarrow 10\mu F\ ,\ [8] \quad (5.8)$$

where $I_{oh}$ - the output current under heavy load, $I_{ol}$ - the output under light load, $V_f$ - the final peak output voltage, $V_i$ - the initial capacitor voltage.

The minimum output capacitance, which is needed to fulfill the output voltage ripple specification

$$C_{out} > \frac{1}{8 \cdot f_{sw}} \cdot \frac{1}{\frac{V_{Oripple}}{I_{ripple}}} = \frac{1}{8 \cdot 644\text{kHz}} \cdot \frac{1}{\frac{1\% \cdot 3.3\text{V}}{25\text{mA}}} = 0.147\mu\text{F} => 1\mu\text{F} \text{ . [8]} \quad (5.9)$$

Just for support, the ripple current of output capacitor

$$I_{co} = \frac{V_{OUT} \cdot (V_{INmax} - V_{OUT})}{\sqrt{12} \cdot V_{INmax} \cdot L_o \cdot f_{sw}} = \frac{3.3\text{V} \cdot (30\text{V} - 3.3\text{V})}{\sqrt{12} \cdot 30\text{V} \cdot 180\mu\text{H} \cdot 644\text{kHz}} = 7.3\text{mA} \text{ . [8]} \quad (5.10)$$

Choose $C_o$ = 10µF 25V capacitor.

## 4. Catch diode

The selected diode must have a reverse voltage rating greater than $V_{INmax}$. The diode peak current rating must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. Efficiency of the regulator is indirectly proportional to the forward voltage of the diode. As a good example proven itself as the best variant for small application with low price, was chosen Schottky diode SD103AWS.

Chosen SD103AWS Schottky diode parameters are shown in Table 5.2.

| Characteristic | Symbol | SD103AWS | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>Working Peak Reverse<br>Voltage DC Blocking Voltage | $V_{RRM}$<br>$V_{RWM}$<br>$V_R$ | 40 | V |
| RMS Reverse Voltage | $V_{R(RMS)}$ | 28 | V |
| Forward Continuous Current | $I_{FM}$ | 350 | mA |
| Non-Repetitive Peak Forward Surge Current | $I_{FSM}$ | 1.5 | A |
| Reverse Breakdown Voltage ($I_R$ = 100µA) | $V_{(BR)R}$ | 40 | V |
| Forward Voltage Drop ($I_F$ = 200mA) | $V_F$ | 0.6 | V |
| Peak Reverse Current ($V_R$ = 30V) | $I_R$ | 5 | µA |
| Total Capacitance | $C_T$ | 35 | pF |

*Table 5.2: Electrical characteristics of SD103AWS* [9]

Power dissipation of SD103AWS will be

$$P_d = \frac{(V_{INmax} - V_{OUT}) \cdot I_{OUT} \cdot V_{fd}}{V_{INmax}} + \frac{C_j \cdot f_{sw} \cdot (V_{IN} + V_{fd})^2}{2} = \frac{(30\text{V} - 3.3\text{V}) \cdot 0.1\text{A} \cdot 0.45\text{V}}{30\text{V}} + \frac{35\text{pF} \cdot 644\text{kHz} \cdot (24\text{V} + 0.45\text{V})^2}{2} = 0.041\text{W}, \quad [8] \quad (5.11)$$

where $V_{fd}$ - forward voltage of the diode, $C_j$ - junction capacitance.

Temperature of working diode at maximal load

$$T_{jd}=T_A+R_{th}\cdot P_d=25°C+625°C/W\cdot 0.041W=50.625°C, \quad (5.12)$$

where $T_A$ - ambient temperature (often taken 25ºC), $R_{th}$ - thermal resistance junction-ambient.

## 5. Slow start capacitor

The slow start capacitor determines the minimum amount of time it needed for the output voltage to reach its nominal programmed value during power up.

Time of slow start is

$$T_{SS}>\frac{C_{OUT}\cdot V_{OUT}\cdot 0.8}{I_{SSavg}}=\frac{10\mu F\cdot 3.3V\cdot 0.8}{0.1A}=0.26ms=>0.3ms, [8] \quad (5.13)$$

where $I_{SSavg}$ - the average input current.

$$C_{ss}=\frac{T_{ss}\cdot I_{ss}}{V_{ref}\cdot 0.8}=\frac{0.3ms\cdot 2\mu A}{0.8V\cdot 0.8}=0.938nF => 1nF, [8] \quad (5.14)$$

where $I_{ss}$ - slow start current = 2 µA.

Choose $C_{ss}$ = 1nF 25V capacitor.

## 6. Under voltage lock out set point

The Under Voltage Lock Out (UVLO) can be made by using simple resistor voltage divider on the EN pin of the TPS54040. The TPS54040 has two thresholds; one is for power on, another for power off.

Since on the input of scheme there is opposite voltage diode, at 18V on the IOLD input on the $V_{start}$=1L+ - $V_{Diode}$ =18V- 1V- 0.7V=16.3V , where 1V is used like buffer for safe operation with undervoltage detection.

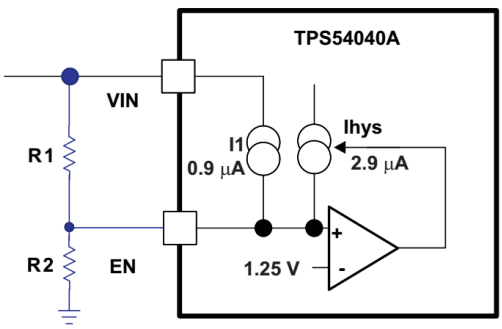



*Figure 5.3: Adjustable Undervoltage Lockout (UVLO)* [8]

Calculations of the resistors for UVLO:

$$R_1 = \frac{V_{start} - V_{stop}}{I_{hys}} = \frac{16.3V - 15.3V}{2.9\mu A} = 345k\Omega \Rightarrow R_1 = 360k\Omega \text{ , [8]} \quad (5.15)$$

$$R_2 = \frac{V_{ENA}}{\frac{V_{start} - V_{ENA}}{R_1} + I_1} = \frac{1.25V}{\frac{16.3V - 1.25V}{360k\Omega} + 0.9\mu A} = 27.8k\Omega \Rightarrow R_2 = 30k\Omega \text{ . [8]} \quad (5.16)$$

Chosen resistors has 1% tolerance, therefore back calculation was done.

The obtained values of $V_{start}$ and $V_{stop}$ are

$$V_{start} = 15.926V + 0.3V / -0.294V.$$

$$V_{stop} = 14.882V + 0.289V / -0.283V.$$

## 7. Output Voltage and Feedback Resistor

The output voltage is determined with a resistor voltage divider from the output line to the $V_{SENSE}$ pin. As $R_2$ (see Figure 5.2) was chosen 15kΩ 1%, and using the equation 5.17, calculate $R_1$

$$R_1 = R_2 \cdot \left( \frac{V_{OUT} - 0.8V}{0.8V} \right) = 15k\Omega \cdot \left( \frac{3.3V - 0.8V}{0.8V} \right) = 46.875k\Omega \Rightarrow R_1 = 47k\Omega \text{ . [8]} \quad (5.17)$$

With 15kΩ and 47kΩ resistors the output voltage will be

$$V_{OUT} = 3.307V + 0.14V / -0.095V.$$

## 8. Power Dissipation Estimate

The power dissipation of TPS54040 includes conduction loss ($P_{con}$), switching loss ($P_{sw}$), gate drive loss ($P_{gd}$) and supply current ($P_q$).

Calculations are made for standard operational conditions: $V_{IN} = 24V$ and $I_{OUT} = 0.1A$ .

$$P_{con} = I_{OUT}^2 \cdot R_{DS(on)} \cdot \frac{V_{OUT}}{V_{IN}} = (0.1A)^2 \cdot 300m\Omega \cdot \frac{3.3V}{24V} = 0.413mW \text{ , [8]} \quad (5.18)$$

$$P_{sw} = V_{IN}^2 \cdot f_{sw} \cdot I_{OUT} \cdot 0.25 \cdot 10^{-9} = (24V)^2 \cdot 644kHz \cdot 0.1A \cdot 0.25 \cdot 10^{-9} = 9.274mW \text{ , [8]} \quad (5.19)$$

$$P_{gd} = V_{IN} \cdot 3 \cdot 10^{-9} \cdot f_{sw} = 24V \cdot 3 \cdot 10^{-9} \cdot 644kHz = 46.368mW \text{ , [8]} \quad (5.20)$$

$$P_q = 116 \cdot 10^{-6} \cdot V_{IN} = 116 \cdot 10^{-6} \cdot 24V = 2.784mW \text{ . [8]} \quad (5.21)$$

Total losses will be equal

$$P_{tot} = P_{con} + P_{sw} + P_{gd} + P_q = 0.413 + 9.274 + 43.368 + 2.784 = 58.838mW \text{ . [8]} \quad (5.22)$$

Using number of total losses it is possible to calculate changes in temperature during work

$$T_j = T_A + R_{th} \cdot P_{tot} = 25°C + 62.5°C/W \cdot 58.838mW = 28.67°C \quad (5.23)$$

Calculations show that the highest losses will occur in driving scheme of the MOSFET. Widely, for this case used schemes with charging-discharging capacitors, which has big losses during

process of charging-discharging. Second place takes switching losses, which depends directly from resistance drain-source of MOSFET, forward current and switching frequency. Regulating this three parameters it can possible to decrease this losses.

Totally, the temperature of board during normal operation conditions will increase on 3.67°C.

### 5.2.2. Simulation

Texas Instruments allows use special simulation program for designing DC/DC converter – SwitcherPro Design. Result of simulation is shown on Figure 5.4 [10]. Simulation confirms calculations.

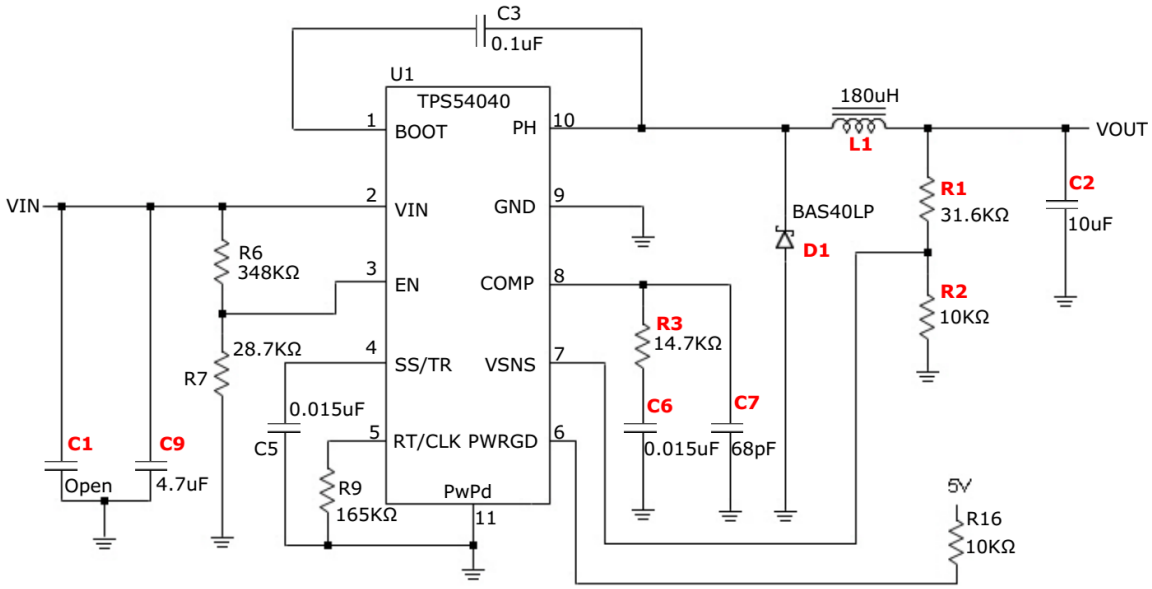



*Figure 5.4: Simulation results*

### 5.2.3. EMI – RC snubber

Including an RC snubber can effectively damp out ringing by increasing the switching losses.

The position of RC snubber should be as close as possible to switching pin and power ground. In buck converters as TPS54040 RC snubber must be placed before catching diode and inductance (see Figure 5.5).

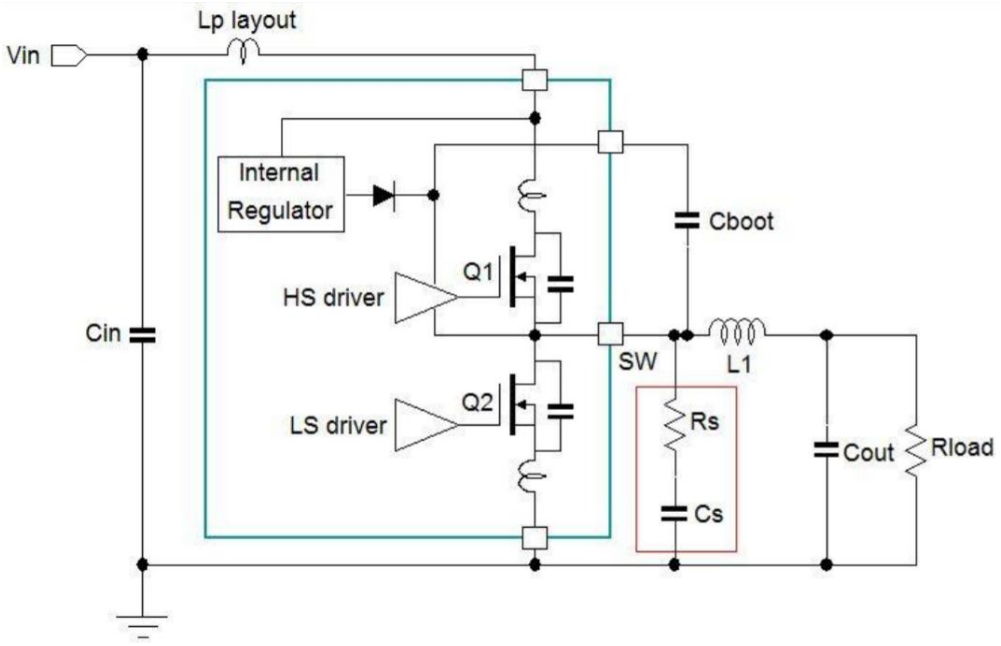



*Figure 5.5: RC snubber placement* [11]

Parasitic resonant LC circuit can be sufficiently dumped by adding the snubber resistor $R_s$. The value of $R_s$ depends on necessary damping effect of snubber and parameters of parasitic LC components. The value of snubber resistor can be calculated by using equation 5.24.

$$R_s = \frac{1}{2\xi}\sqrt{\frac{L_p}{C_p}}, \text{ [11]} \qquad (5.24)$$

where $\xi$ is the damping factor. Normally $\xi$ can range from 0.5 (slightly underdamped) to 1 (critically damped).

The magnitude of parasitic inductance $L_p$ and capacitance $C_p$ is standardly not given, and can be measured in the next way:

1. Measure the original ringing frequency $f_{RING}$ in the rising edge.

2. Use small capacitance and connect it between measured pin and ground. Measure the ringing frequency. Capacitance has to be added until 50% of the original ringing frequency will not be reached.

3. This reduction means that the original capacitance is four times lower than the total resonance capacitance. The original capacitance $C_p$ is 1/3 of the applied in experiment capacitance.

4. The parasitic inductance $L_p$ can be calculated by $L_p = \frac{1}{C_p \cdot (2\pi f_{RING})^2}$. [11] (5.25)

The series capacitor $C_s$ of the RC damper must be large enough that the damping resistor can perform a stable resonance damping during the circuit loop. Too large values of the capacitor increase the power loss during the charging and discharging of the capacitor. Usually $C_s$ is chosen 3-4 times higher than the $C_p$.

In addition to damping the resonance, the RC damper will also slightly increases the rise and fall time of the switching signal. However, charging and discharging the damper capacitance will

result in additional peaks of current peaks during switching, which can increase EMI in areas with a lower frequency.

For example, let's imagine that $f_{RING}\approx 2.5MHz$. After assembling different values of capacitors, there was obtained that at 47pF capacitor $f_{RING}\approx 1.3MHz$. $C_p$ is thus 47/3 = 16pF.

$L_p$ can be found from $L_p = \frac{1}{C_p \cdot (2\pi f_{RING})^2} = \frac{1}{16pF \cdot (2\pi \cdot 1.3MHz)^2} = 0.94mH$.

$R_s$ can be calculated from $R_s = \frac{1}{2\xi}\sqrt{\frac{L_p}{C_p}} = \frac{1}{2 \cdot 0.5}\sqrt{\frac{0.94mH}{16pF}} = 7.651k\Omega \Rightarrow 10k\Omega$.

$C_s$ is chosen $4xC_p$ and becomes approximately 68pF.

## 5.3. Microcontroller unit

The microcontroller unit as a main control element in the Minimal Design must fulfill the following requirements: UART periphery (230400 Bauds, what corresponds COM3 speed in IO-Link specification v.1.1.2); at least 3kB non-volatile memory; at least 16 kB RAM; ARM based; contains SPI, 2 channels ADC, I2C interfaces; 2kB internal FLASH for data storage; JTAG connection for troubleshooting.

After analysis of market there were chosen next MCUs:

| | STM32F071 C8U6 | STM32L071 K8U6 | STM32F301 K6U6 | STM32L151 C6U6A |
|---|---|---|---|---|
| UART periphery (230400) | YES | YES | YES | YES |
| SPI, ADC, I2S | YES | YES | YES | YES |
| ≥3kB non-volatile memory | YES | YES | NO | YES |
| ≥16 kB RAM | YES | YES | YES | YES |
| ≥2kB Flash memory | YES | YES | YES | YES |
| JTAG interface | Only SWD | Only SWD | YES | YES |
| Package | LQFP48 (7x7mm) | UFQFPN32 (5x5mm) | UFQFPN32 (5x5mm) | UFQFPN48 (7x7 mm) |
| Price, $ | 1.192 | 1.36 | 1.273 | 1.63 |

*Table 5.3: Chosen MCUs*

In the project JTAG interface can be substituted by SWD interface without any troubles.

Since 32-pin packages have not abilities to connect High-speed external crystal, STM32L071C8 with package LQFP48 was chosen.

### 5.3.1. Power supplying of MCU

Every power supply pair such as VDD/VSS or VDDA/VSSA must be decoupled with filtering ceramic capacitors, which must be connected as close as possible to pins of MCU with taking into account the functional layers of PCB. Typical power supply pins connections shown on Figure 5.6. According to Figure, for STM32L071C8 will be used 3x100nF and 3x10µF capacitors for $V_{SS}$ and $V_{DD}$ connection, 100nF and 1µF capacitors for $V_{SSA}$ and $V_{DDA}$.

VDDIO2 (special pin for IO pins supply) is also connected to VDD, and for it will be used 100nF and 1µF capacitors.

For additional noise dumping will be used 1nF, 10nF, 1µF and 22µF capacitors.

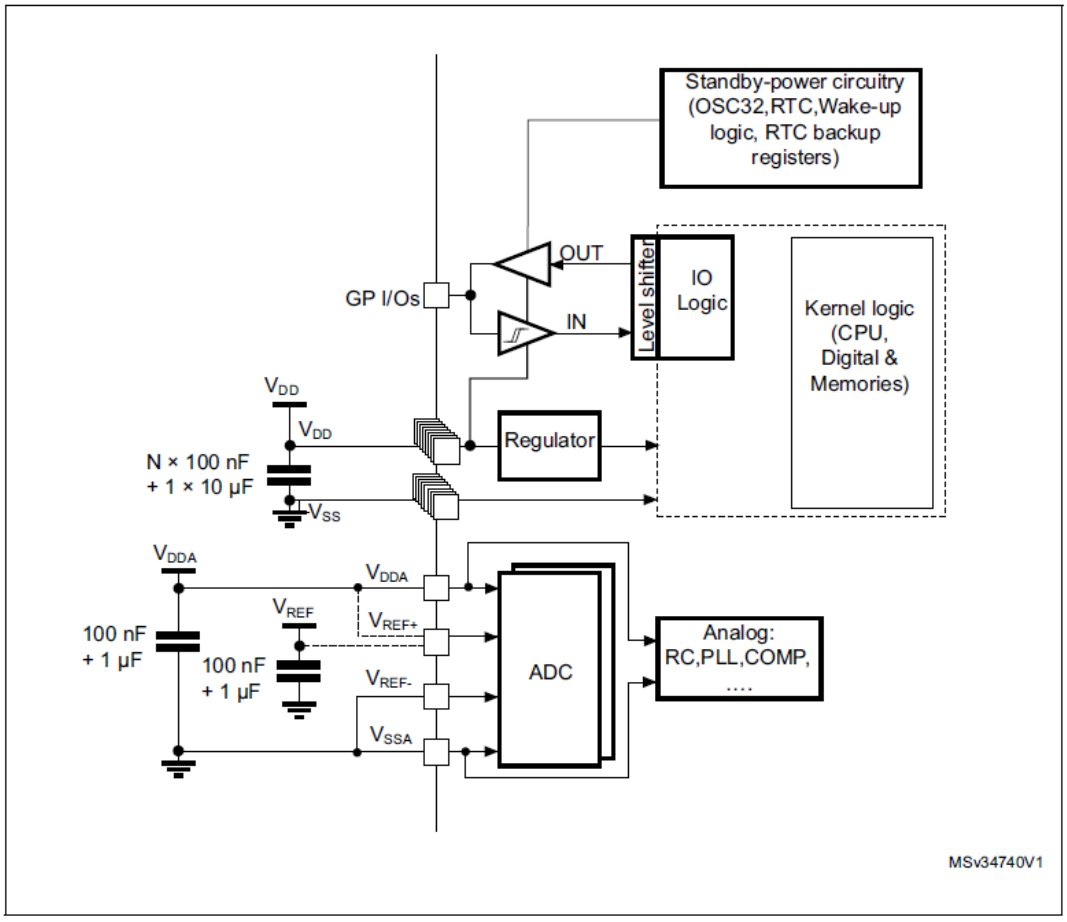



*Figure 5.6: Power supply scheme of STM32L071C8* [12]

## 5.3.2. Oscillator choice

As clock will be used 11.0592 MHz external high-speed crystal for providing UART COM3 transmission speed, which is equal 230400 Bauds. This frequency was chosen in case of convenience of calculation:

$$11.0592\text{MHz} = 230400\text{Bauds} \cdot 16 \cdot 3, \text{ [13]} \tag{5.26}$$

where 16 and 3 are postscalers in the MCU.

Crystal will be shunted by 1MΩ resistor that will work as feedback resistor for the internal inverter to which the crystal with condensers are connected, and provides the inverter's work into the linear region. After first switching the power, the feedback resistor helps frequency-making capacitors to get ringing at the right frequency faster.

## 5.3.3. BOOT mode

BOOT mode is a choice of place, from where will start uploading of working program. As BOOT mode in the STM32L071C8 is used BOOT0, which means only two abilities of boot modes. There will be used both possibilities with help of resistor switch. All boot modes are shown in Table 5.4 [12].

| BOOT mode selection | Boot mode | Aliasing |
|---|---|---|
| BOOT0 | | |
| 0 | Main flash memory | Main Flash memory is selected as boot space |
| 1 | System memory | System memory is selected as boot space |

*Table 5.4: Boot modes* [12]

PCB will be designed for both variant of boot usage. Pin connection is shown on Figure 5.7.

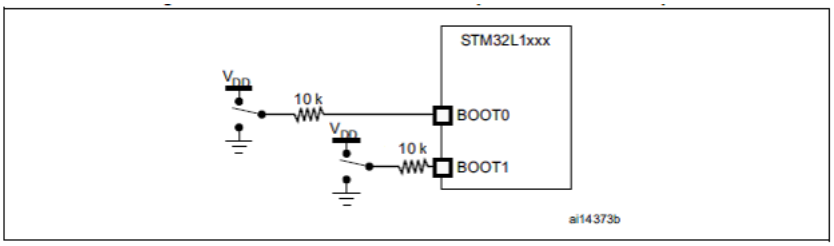



*Figure 5.7: Boot mode selection implementation example* [12]

## 5.3.4. NRST connection

NRST connection is used for the reset of the MCU externally. Since in our system external reset will be done through JTAG connector, only a capacitor is recommended connect to NRST to improve EMC performance by protecting the device against parasitic resets [14].

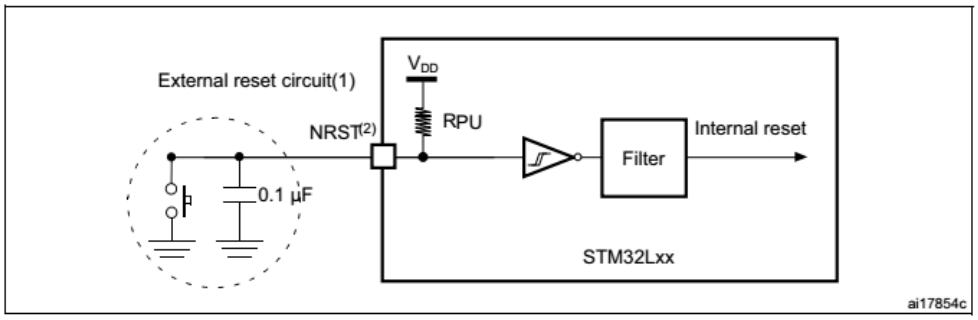



*Figure 5.8: NRST connection* [12]

For NRST work were chosen 10kΩ resistor and 1nF capacitor. Calculation of RC circuit is listed below.

$$t=-\ln\left(\frac{V_{ss}-V_c}{V_{ss}}\right)\cdot R\cdot C=-\ln\left(\frac{3.3V-3.29V}{3.3V}\right)\cdot 10k\Omega\cdot 1nF=58\mu s \quad . \qquad (5.27)$$

## 5.3.5. SWD connection

The IO-Link Device Minimal Design needs to upload and debug working program. To this aim JTAG or SWD connection is used as widely used interfaces. JTAG interface represents 5-wire interphase while SWD has only 2-wire interphase.

The STM32L071C8 core integrates the serial wire debug (SWD) port. It is a debug port with a 2 pins: clock and data, which are widely used as the debug access port [15].

| SWD pin name | SWD port | |
|---|---|---|
| | Type | Debug assignment |
| SWDIO | I/O | Serial wire data input/output |
| SWCLK | I | Serial wire clock |

*Table 5.5: SWD port pins*

Since in our work it's used JTAG connector, it's necessary correctly connect SWD and JTAG. Right connection is shown in Table 5.6.

| **JTAG** | |
|---|---|
| **Pin** | **Purpose** |
| TCK | Clock |
| TMS | State Machine Control |
| TDI | Data In |
| TDO | Data Out |
| TRST | Reset |

| **SWD** | |
|---|---|
| **Pin** | **Purpose** |
| SWCLK | Clock |
| SWDIO | Data Input/Output |
| - | - |
| - | - |
| - | - |

*Table 5.6: Signal comparison between JTAG and SWD* [15]

## 5.4. PHY

PHY is an integrated circuit designed to perform the physical layer functions of the standard I/O network model.

The PHY chips allow other link-layer devices, called MACs, to connect to a physical transmission layer, such as an optical fiber or a copper cable. The PHY standard microchip includes physical coding sublayer modules and a transmission medium sublayer. The physical coding sublayer module performs the functions of encoding and decoding the transmitted and received data stream. The purpose of coding is to simplify the process of restoring the data stream of the receiver.

IO-Link transceivers differ on Master and Device transceivers. The Master transceivers are widely used and are in big range on the market. Another situation is with Device transceiver. The widespread producers of Device transceivers are ST and MAXIM.

ST offers one possibility – L6362A. The main distinguishing abilities are wide supply voltage range – 7 to 36 V, high output current capability – 220mA, selectable output stage: high side, low side and push-pull, full set of protections such as overcurrent, overvoltage, undervoltage etc., linear voltage regulator 3.3V or 5V, which can be used for supplying of MCU.

MAXIM provides higher range of possibilities – MAX14821 and MAX14827. For our case, MAX14827 is of interest, because it has UART communication and hasn't unnecessary pins and functions. According to datasheet, MAX14827 works on 9-60V power supply voltage, provides 1A forward current, has selection of driver current, multiplexed SPI/UART interface option, linear voltage regulator 3.3V or 5V, all range of protections.

The both devices are pretty the same that means the price will make decision. The price of L6362A is 69 Kč; price of MAX14827 is 118 Kč (mouser.com).

After comparison of all possible variants, L6362A IO-Link Device Transceiver was chosen.

The main part of any IO-Link Transceiver is PNP and NPN MOSFETs, which switch 24V supply voltage, thereby receive and send messages between Master and Device. Every MOSFET has own protections and can be controlled separately. Communication between PHY and MCU is made through UART interphase.

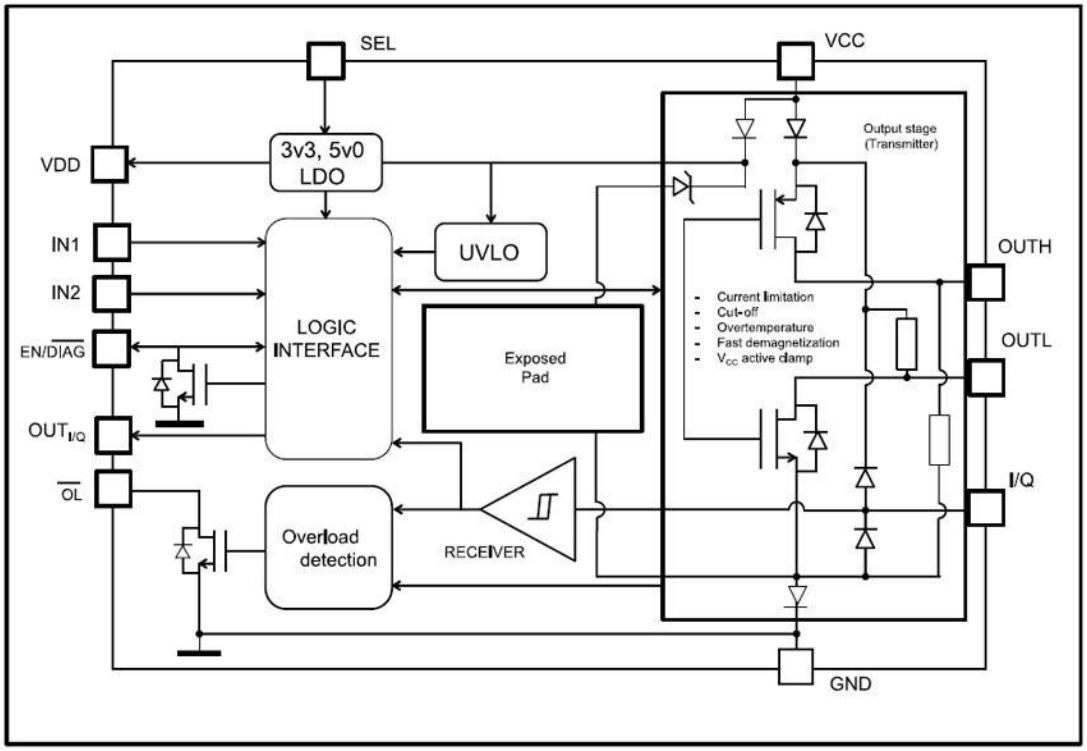



*Figure 5.9: Block diagram of L6362A* [16]

## 5.5. LED identification

In the Device red and green LEDs are used. The package of LEDs must be as small as possible, therefore package 0402 was chosen. The typical current for each LED is about 2mA.

### 5.5.1. Interface to MCU

The LEDs are supplied from 3.3V from MCU. The maximal load of each MCU GPIO is over 20mA (sink or source) and the maximal current of MCU must be less than 240mA (sink and source).

Table with current characteristics from the MCU datasheet:

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD\_x}$ power lines (source) | 100 | mA |
| $\Sigma I_{VSS}$ | Total current into sum of all $V_{DD\_x}$ ground lines (sink) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sunk sourced by any I/O and control pin | -25 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) | ±25 | |

*Table 5.7: MCU current ratings* [12]

It means LED can be connected directly to the GPIO pin.

Current limit resistor can be calculated as

$$R_{adLED\_G} = \frac{P3V3\text{-}V_{LED\_G}}{I_{LED}} = \frac{3.3V\text{-}1.7V}{2mA} = 800\Omega \Rightarrow 820\Omega . \quad (5.28)$$

$$R_{adLED\_R} = \frac{P3V3\text{-}V_{LED\_R}}{I_{LED}} = \frac{3.3V\text{-}1.8V}{2mA} = 750\Omega \Rightarrow 820\Omega . \quad (5.29)$$

The light intensity will be the same for both LED at the 2mA forward current.

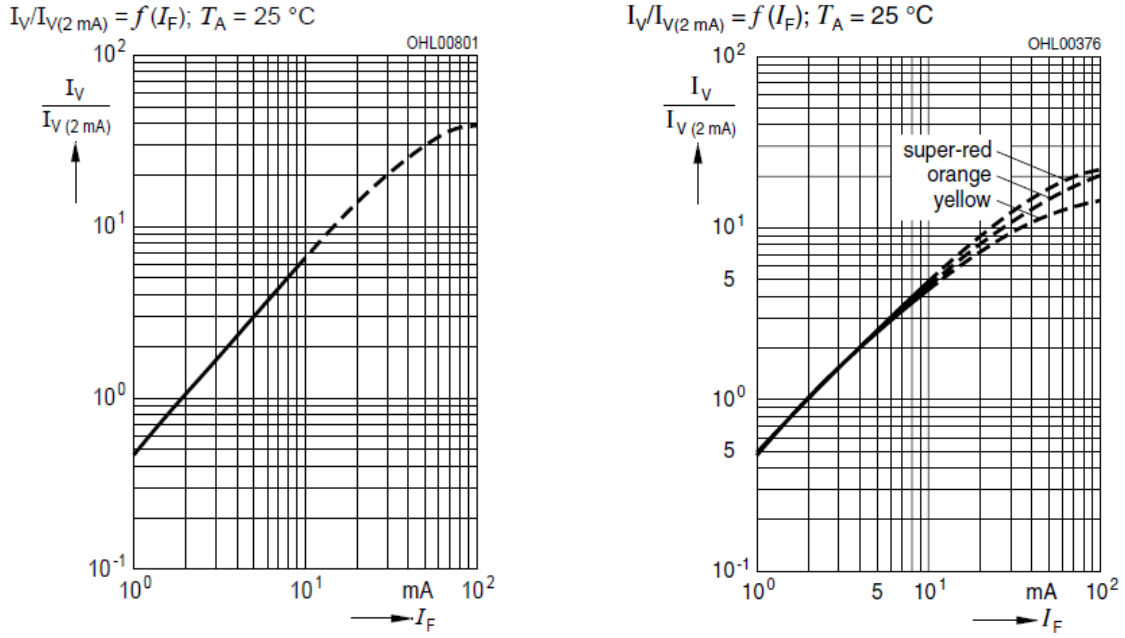



*Figure 5.10: Relative luminous intensity: left – for green LED, right – for red LED* [17] [18]

# 6. Manufacturing concept

## 6.1. Principal electrical scheme

Principal electrical scheme is made on three pages and consists from blocks:

1. Power supply;
2. MCU;
3. IO-Link periphery and LED diodes.

Final scheme is situated in attachments.

## 6.2. Performance

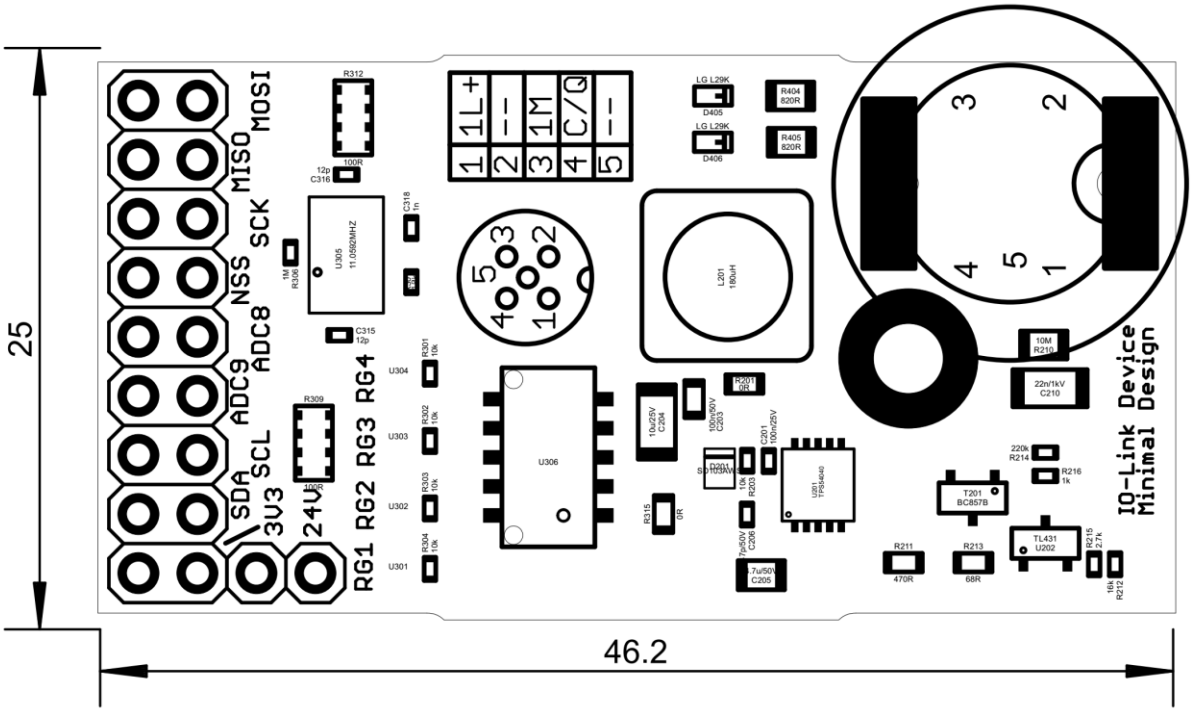



*Figure 6.1: Performance of IOLD (top view)* [19]

# 7. Testings of the Device

Purpose of this Chapter is to describe the results of tests which will be carry out for verification and control of correct work and communication of IO-Link Device Minimal Design.

Tests will consist of:

- power supply testings;
- IO-Link testings;
- temperature testing;
- verification of functional mains power input port;
- EMC testings.

List of used equipment is shown below

| | |
|---|---|
| DC Power Supply | Type: AIM-TTi MX180TP |
| DC Power Supply | Type: BK Precision 9115 |
| Oscilloscope | Type: LeCroy HDO6054 |
| DC Electronic Load | Type: AIM-TTi LD400P |
| Digit Multimeter | Type: Keysight 34365A |
| Digit Multimeter | Type: Keysight U1271A |
| Waveform Generator | Type: RIGOL DG2041A |
| Autotransformer | Type: MERTEL HSN 260/4,5 |
| Isolating transformer | Type: DIAMETRAL OT230.030 |
| Environmental chamber | Type: ECOCELL 222 |
| Spectrum analyzer | Type: Keysight MXE N9038A |
| Conducted immunity test system | Type: TECTRA CIT-10 |
| Attenuator | Type: BIRD 75-A-FFN-06 |
| Coupling/Decoupling network | Type: TECTRA CDN-145-32A |
| DC Power supply | Type: STATRON 9229 |
| LISN | Type: SCHWARZBECK NSLK 8126 RC |

Additional SIEMENS Remote-IO equipment for tests is shown below:

| | |
|---|---|
| PS307 10A | MLFB: 6ES7307-1KA02-0AA0 |
| CPU319-3PN/DP | MLFB: 6ES7318-3EL01-0AB0 |
| SM374 IN/OUT16 | MLFB: 6ES7374-2XH01-0AA0 |
| IM155-6PN HF | MLFB: 6ES7155-6AU00-0CN0 |
| BA 2xRJ45 | MLFB: 6ES7193-6AR00-0AA0 |
| ET200SP CM 4xIO-Link | MLFB: 6ES7137-6BD00-0BA0 |

## 7.1. Electrical test of power supply

The main goal of testing of power supply is to check and compare the calculated and real values. According to obtained numbers will be made the decision about believability of procedure of calculations.

### 7.1.1. Efficiency and losses

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of power supply for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to power supply.
4) Tune input voltage to 18V, measure input and output power. Calculate efficiency.
5) Repeat 4$^{th}$ step with 24V and 30V.
6) Repeat 2$^{nd}$-5$^{th}$ steps without load.

**Result:**

| **Input voltage VSD, V** | **18** | **24** | **30** |
|---|---|---|---|
| Input power, mW | 447 | 467 | 491 |
| Output power, mW | 312 | 312 | 312 |
| Efficiency, % | 69.79 | 66.81 | 63.54 |

*Table 7.1: Efficiency measurements with load*

| **Input voltage VSD, V** | **18** | **24** | **30** |
|---|---|---|---|
| Input power, mW | 2.448 | 3.096 | 3.75 |

*Table 7.2: Power losses without load*

### 7.1.2. Supply ripple, stability, start up overshoot - PASSED

Tests limits / Expected values:

Output voltage: 3.307V +0.14V/-0.095V
Frequency: 644 kHz + 40 kHz/-30kHz
Slow start – 0.3ms
Voltage ripple - 1% of $V_{OUT}$
Current ripple - 25mA

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to power supply.
4) Tune input voltage to 18V.

5) Measure ripple of output current and voltage, time of slow start, measure output voltage and frequency.
6) Repeat $4^{th}$-$5^{th}$ steps with 24V and 30V input voltage.

**Result:**

| **Input voltage VSD, V** | **18** | **24** | **30** |
|---|---|---|---|
| Output voltage, V | 3.2984 | 3.3017 | 3.3053 |
| Frequency, kHz | 622 | 625 | 625 |
| Slow start, ms | 0.255 | 0.256 | 0.26 |
| Voltage ripple, % | 1 | 0.81 | 1.03 |
| Current ripple, mA | 4.92 | 5.07 | 4.96 |

*Table 7.3: Measurements for 6.1.2 test*

Examples of result at 18V are shown on Figures 7.1 – 7.3.

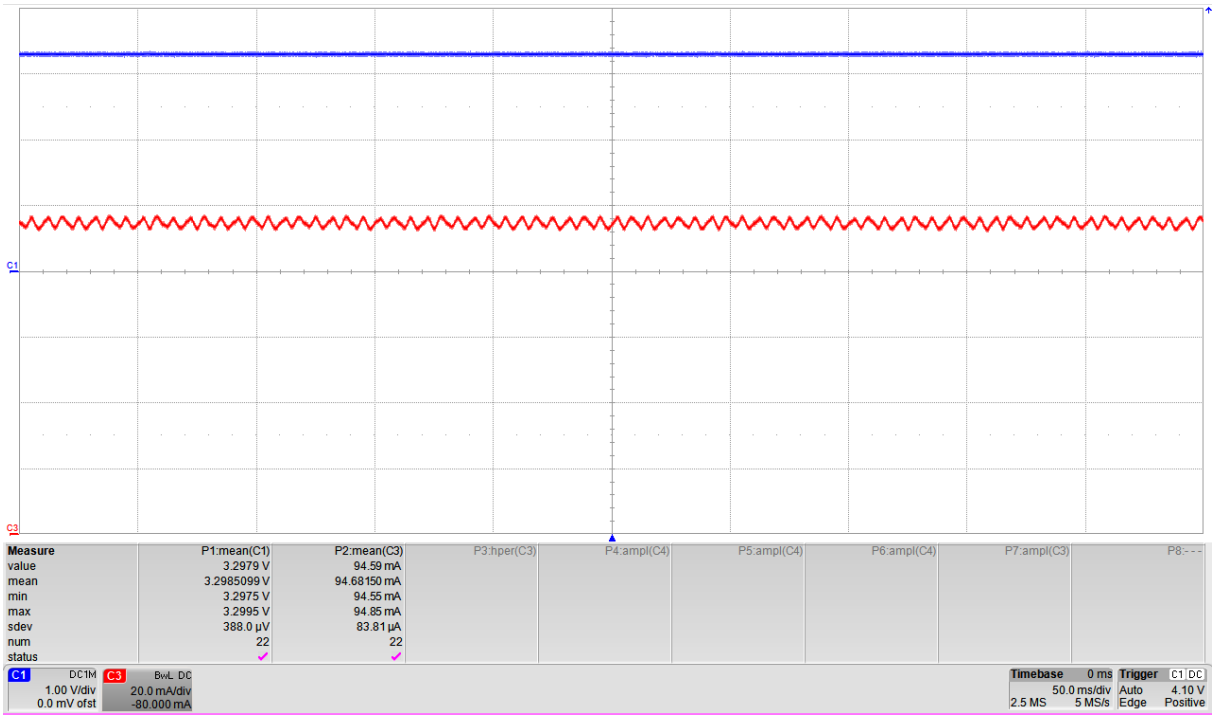



*Figure 7.1: Voltage (blue) and current (red) ripples at 18V input voltage*

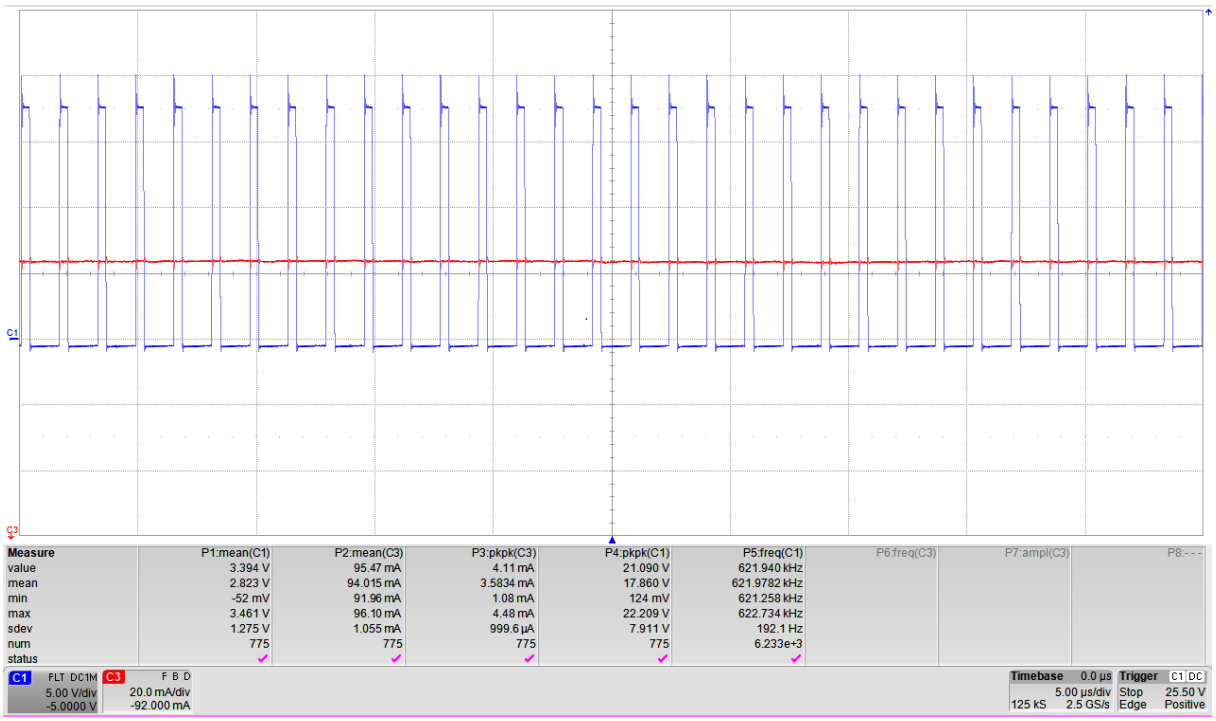



*Figure 7.2: Output frequency (blue) and current (red) ripple at 18V input voltage*

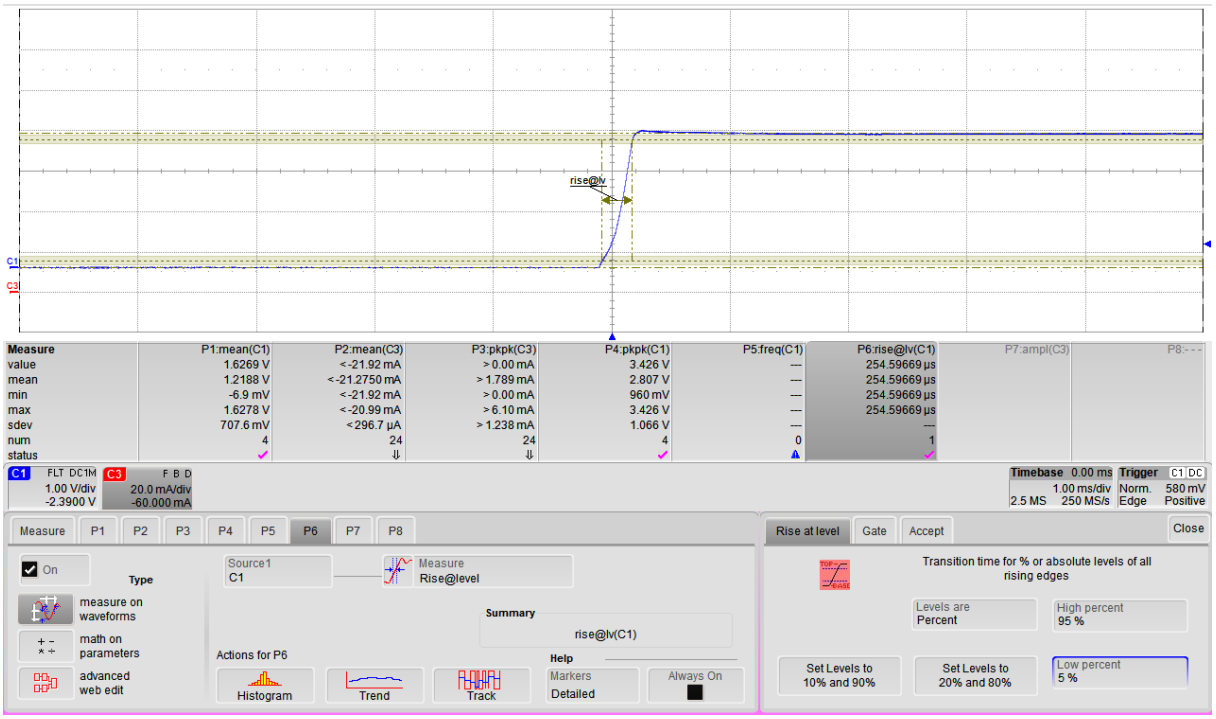



*Figure 7.3: Slow start of buck converter at 18V input voltage*

For measuring time of slow start was used internal function of LeCroy HDO6054 “Rise level”. This function allows measure the time of rising in set by user parameters. In our case, it measures time between 5% and 95% of signal, what is standard values for this case.

## 7.1.3. Diagnostic levels and delay - **PASSED**

| | |
|---|---|
| Tests limits / Expected values: | Start up voltage: >15.93V +0.3V/-0.29V<br>Stop voltage: <14.88V +0.29V/-0.28V |
| Measured values: | Start up voltage: 16.08V<br>Stop voltage: 14.84V |

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to power supply.
4) Tune input voltage to 0V.
5) Increasing input voltage, measure start up voltage. Test should be made three times.
6) Tune input voltage to 24V.
7) Decreasing input voltage, measure shut down voltage. Test should be made three times.

**Result:**

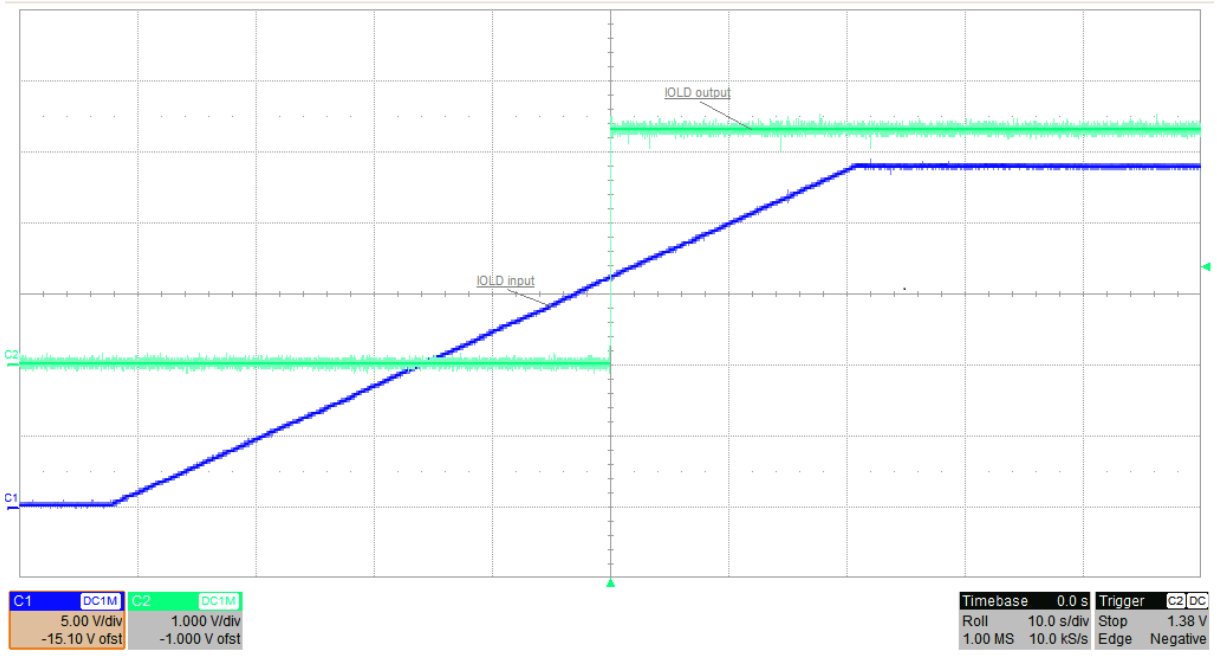



*Figure 7.4: Example of start up limit determining: green – IOLD output, blue – IOLD input*

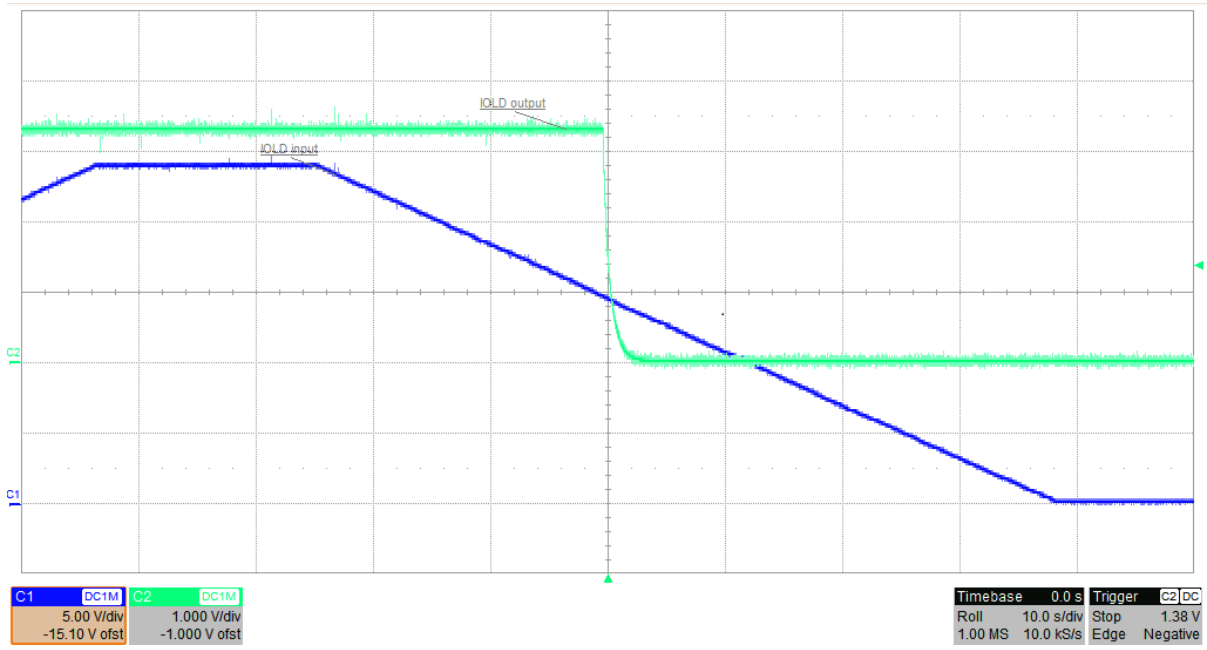



*Figure 7.5: Example of shut down limit determining: green – IOLD output, blue – IOLD input*

## 7.1.4. Consumption of all supplies - PASSED

Tests limits / Expected values: <100mA

Measured values: Consumed current – 10mA

**Test description:**

1) Connect IOLD (pins 1L+ and 1M) to 24V.
2) Tune communication between IOLD and IOLM via C/Q.
3) Measure the total consumed current in 1M wire.

## 7.1.5. Buffering of power supply - PASSED

Tests limits / Expected values: Voltage difference - 1% $V_{OUT}$
Time delay – 3.11µs

Measured values: 160µs

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to 24V.
4) Generate the switching off impulse in 1L+ wire. Increasing the time of impulse, achieve appreciable voltage drop.

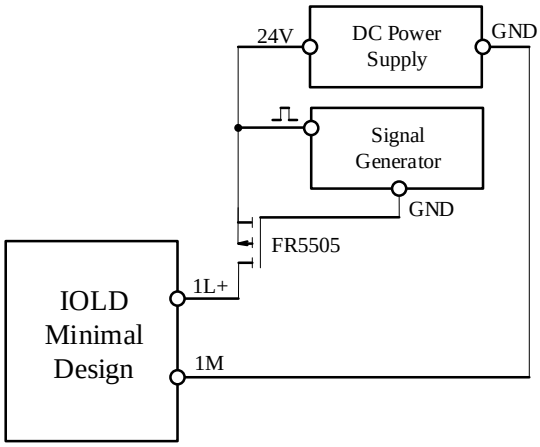



*Figure 7.6: Principal scheme of test setup*

**Result:**

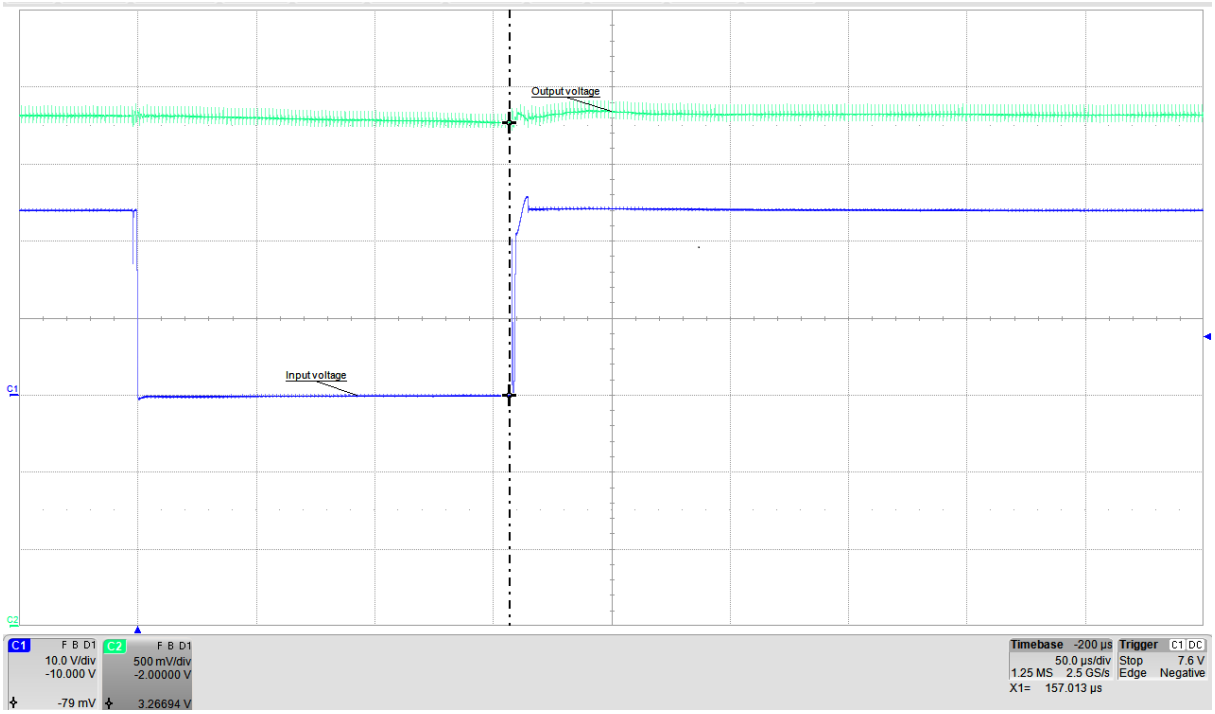



*Figure 7.7: Switching impulse 160µs: green – IOLD output, blue – IOLD input*

**Conclusion**: obtained results satisfied calculations. Moreover, buffering of power supply approximately in 50 times higher than it needs. In future redesign, the output capacitor will be changes by smaller one.

Procedure of power supply design is correct. This design can be used as an example or ready-made solution.

## 7.2. Verification of functional mains power input port

The aim of this subchapter is describing the results of testings according to international standards such as IEC 61131-2 and NAMUR NE 21.

### 7.2.1. Rated input voltage - PASSED

Test source: IEC 61131-2 / 6.4.1.1 [19]

Tests limits / Expected values: Module should work properly during all types of tests

| | |
|---|---|
| Rated Voltage | $U_N$ =24V |
| - Lower limit voltage (static / average) | 20,4V |
| - Upper limit voltage (static / average) | 28,8V |
| - Lower limit voltage (dynamic) | 18,5V |
| - Upper limit voltage (dynamic) | 30,2V |
| Non-Periodic Overvoltages / Value Note: Duration 500ms / Recovery time 50s | 35V |
| Test at minimum operational voltage | 0,85 x $U_N$ / Ripple continuous 0,05 x $U_N$ / 30 min |
| Performance criterion | A |
| Test at maximum operational voltage | 1,20 x $U_N$ / Ripple continuous 0,05 x $U_N$ / 30 min |
| Performance criterion | A |

*Table 7.4: Measurement requirements according to IEC 61131-2 / 6.4.1.1* [19]

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to power supply.
4) Tune power supply for static tests: firstly, tune to 20.4V and check output voltage; secondly, tune to 28.8V and check output voltage.
5) Tune signal to lower limit for dynamic test. Signal frequency is 50Hz. Wire the principal scheme shown on Figure 7.8. Observe voltage output waveform throughout 30 min. Check stability and output voltage of IOLD.
6) Repeat 5$^{th}$ step with upper limit for dynamic test.
7) Tune power supply for non-periodic overvoltage test. Check stability and output voltage of IOLD.

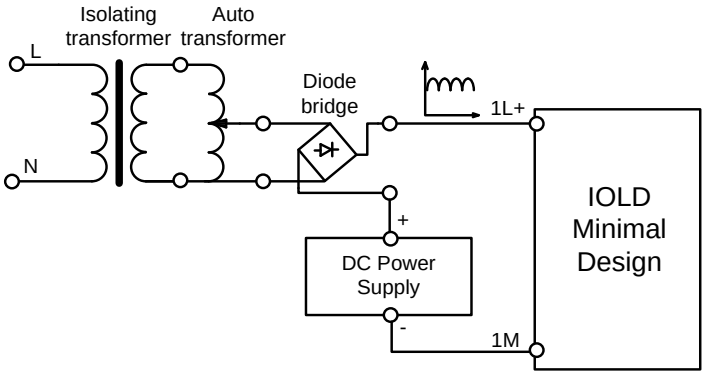



*Figure 7.8: Principal scheme of testing setup for dynamic tests*

**Results:**

As an example there are presented waveforms for lower limit voltage (dynamic) on Figure 7.9, waveforms for non-periodic overvoltage on Figure 7.10.

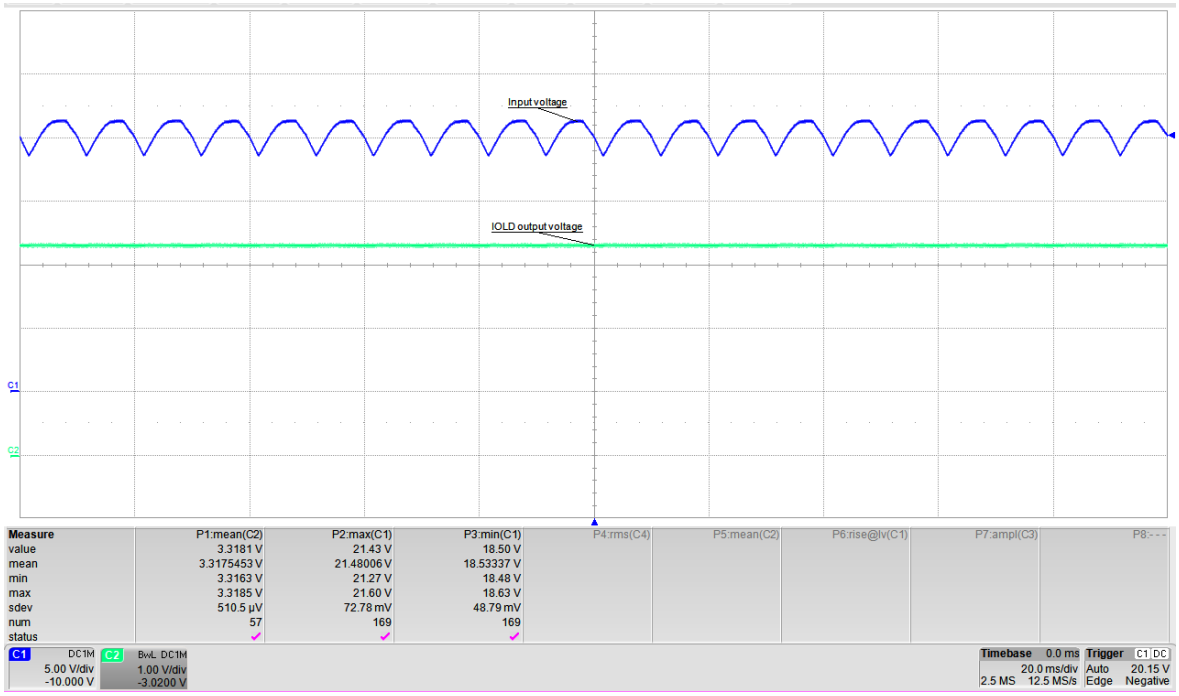



*Figure 7.9: Lower limit voltage (dynamic) waveforms*: *green – IOLD output, blue – IOLD input*

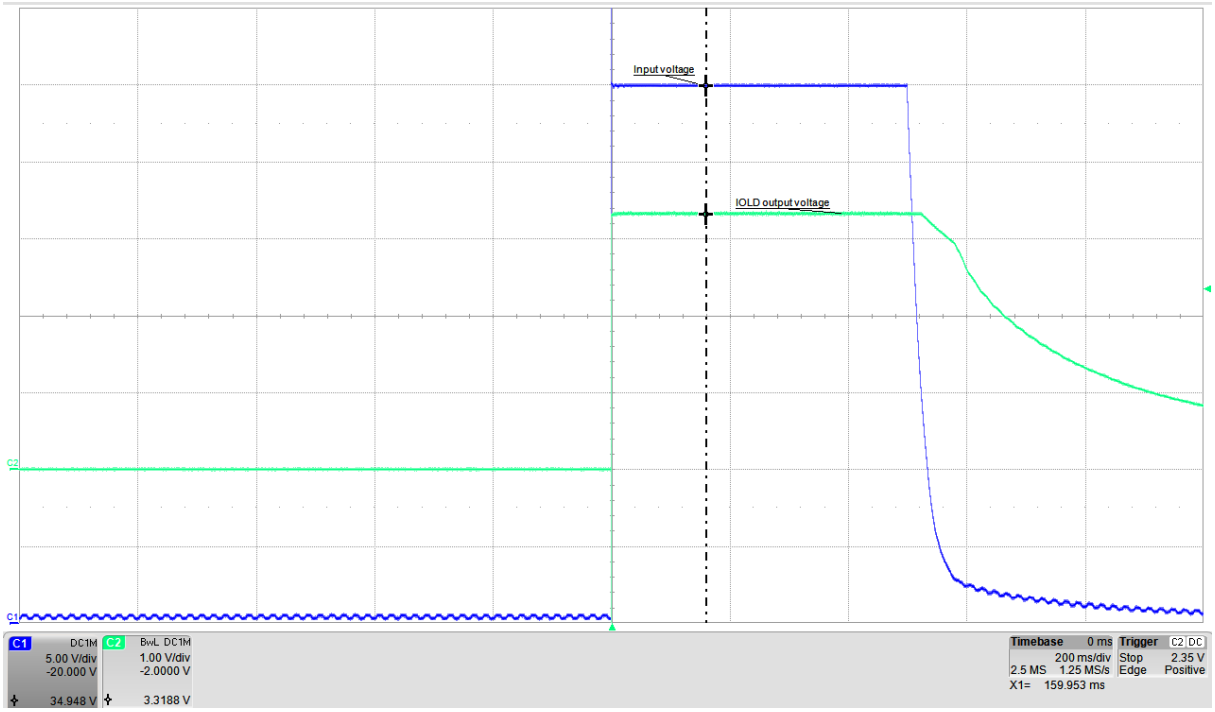



*Figure 7.10: Non-Periodic overvoltage waveform: green – IOLD output, blue – IOLD input*

**Conclusion**: according to pictures shown above, the Device keeps its correct work during all types of test signals and at all types of limits. Any troubles have not observed.

## 7.2.2. Fast supply voltage variation test - PASSED

| | |
|---|---|
| Test source: | IEC 61131-2 / 6.4.2.2 [19] |
| Tests limits / Expected values | Start up voltage: >15.93V +0.3V/-0.29V |
| | Stop voltage: <14.88V +0.29V/-0.28V |
| Measured values: | $SUL_{av}$: 16.0456V |
| | $SDL_{av}$: 14.8331V |

**Test description:**

1) Desolder 0R resistor.
2) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
3) Connect IOLD (pins 1L+ and 1M) to power supply.
4) Generate voltage signal shown on Figure 7.11.

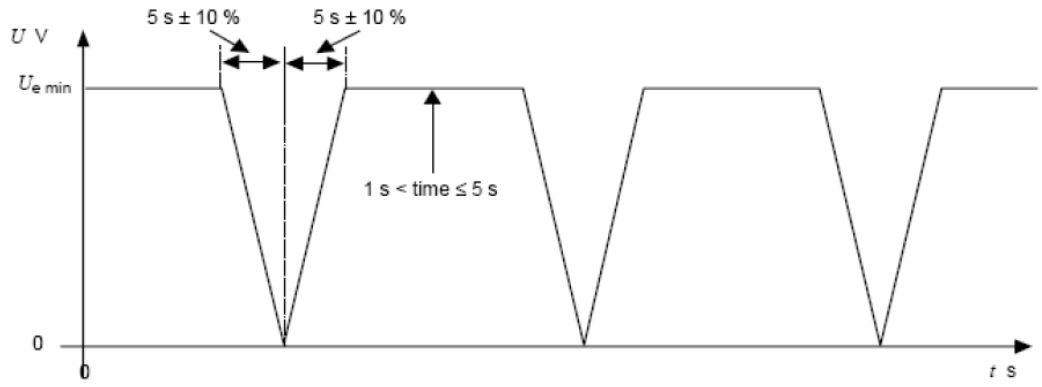



*Figure 7.11: Testing signal according to IEC 61131-2 / 6.4.2.2* [19]

5) Measure shut down and start up limit. Repeat test three times.

**Results:**

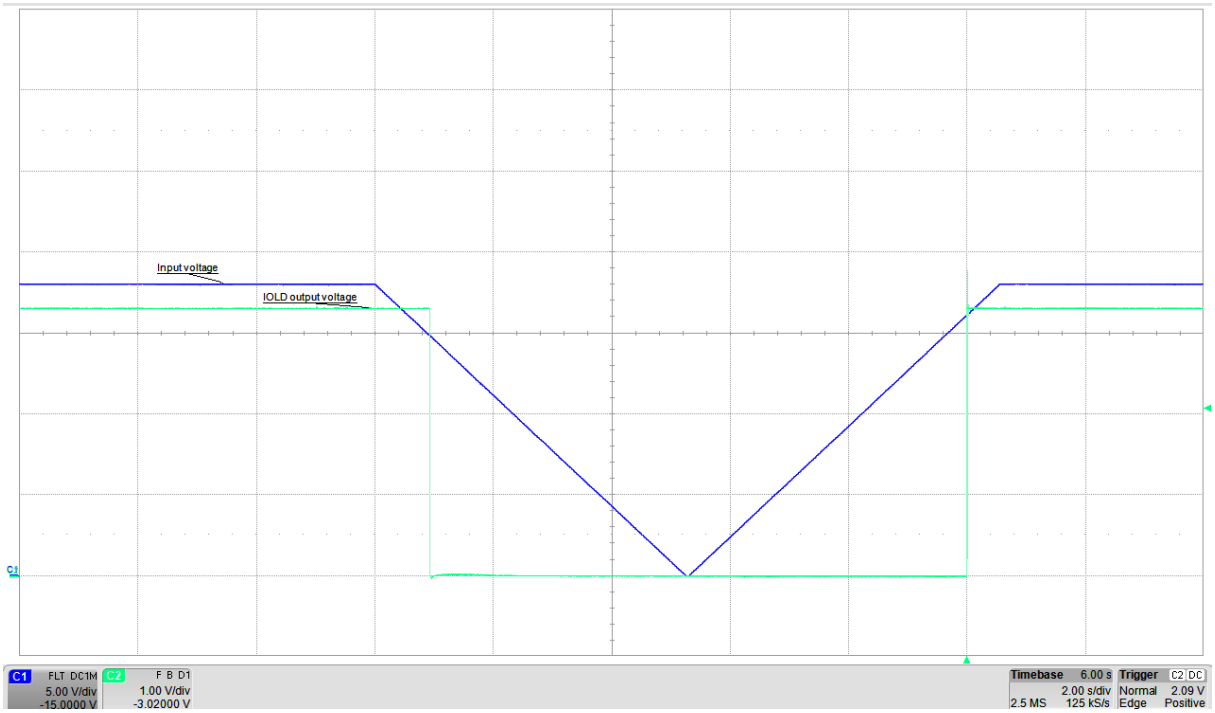



*Figure 7.12: Fast supply voltage variation test*: *green – IOLD output, blue – IOLD input*

**Conclusion**: according to obtained figure, the Device switches on and off in specified limits calculated before. The figure confirms this.

### 7.2.3. Shut down / start up test - PASSED

Test source: IEC 61131-2 / 6.4.1.3, 6.4.1.4 [19]

**Test description:**

Shut down test:

During power supply shut down, behavior of system should be observed. During shut down any change, except as provided by the system, and failure should not be.

All necessary data should be saved correctly. Time of under-voltage detection switching must be enough for saving all data. All elements must work correctly after shut down.

Start-up test:

During supply start up, behavior of system should be observed. During startup, any change, except as provided by the system, and failure should not be.

Communication between IOLD, IOLM and other devices should start work correctly. All data must be correct and full. LED, which shows correct work, must light. LED, which shows incorrect work, must not light.

**Conclusion:** during the all types of test, the Device always starts its work correctly, without any troubles. Shut down process is also going according to specified procedure of switching off.

### 7.2.4. Making current limit - PASSED

Test source: NAMUR NE 21 [20]

Tests limits / Expected values: $I_{ppMAX} \leq 113mA \bullet 15 = 1695mA$

Measured values: $I_{ppMAX}$ (VSD=18V) =708mA

$I_{ppMAX}$ (VSD=24V) =744mA

$I_{ppMAX}$ (VSD=30V) =768mA

**Test description:**

1) Tune communication between IOLD and IOLM.
2) Connect IOLD (pins 1L+ and M) to 18V power supply.
3) Switch on IOLD and measure the current peak in 1L+ wire.
4) Repeat 2nd-3rd steps for 24V and 30V.

**Result:**

As an example of measurement will be shown current peak at 18V input voltage on Figure 7.13.

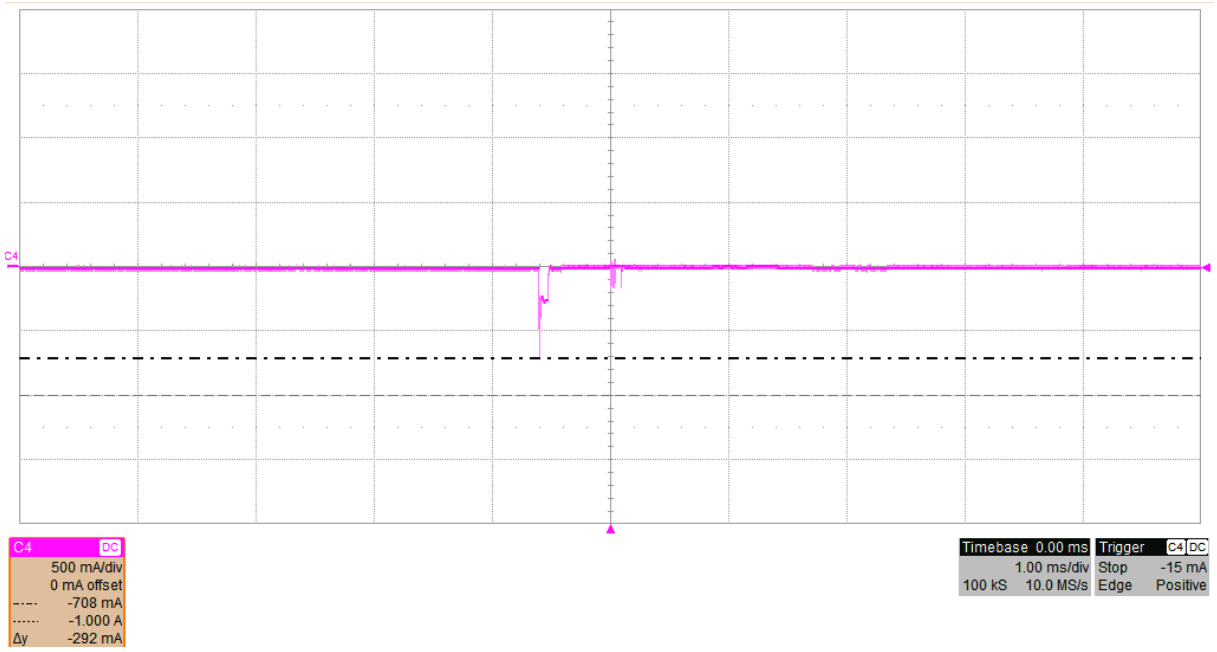



*Figure 7.13: Switching on current peak at 18V input voltage*

**Conclusion:** according to obtained values, the Device starts work correctly, current peak does not cross specified limit.

## 7.2.5. Incorrect connection - PASSED

| | |
|---|---|
| Test source: | IEC 61131-2 / 6.4.3.1 [19] |
| Tests limits / Expected values: | $I_R \leq 10\mu A$ |
| Measured values: | $I_R$ (VSD=18V) =4µA. |
| | $I_R$ (VSD=24V) =5µA. |
| | $I_R$ (VSD=30V) =6µA. |

**Test description:**

1) Connect IOLD (pins 1L+ and 1M) to power supply.
2) Tune input reverse voltage to 18V.
3) Measure reverse current.
4) Repeat 2nd-3rd steps for 24V and 30V.

## 7.3. Temperature testings - PASSED (+60ºC) / FAILED (-40ºC)

| | |
|---|---|
| Test source: | IEC 61131-2 / 6.2.1 [19] |
| Tests limits / Expected values: | Typical voltage level: 3.307V |
| | High voltage limit: 3.447V |
| | Low voltage limit: 3.212V |

**Test description:**

1) Check initial conditions of temperature chamber and thermocamera.
2) Desolder 0R resistor.
3) Set climatic chamber to -40°C.
4) Connect 33Ω 0.5-1W to output of buck converter for providing 100mA load current.
5) Connect IOLD (pins 1L+ and 1M) to power supply.
6) Tune input voltage to 18V.
7) Measure output voltage, current, frequency.
8) Repeat $6^{th}$-$7^{th}$ steps for 24V and 30V.
9) Change load in range 33-400 Ω. Repeat $7^{th}$-$8^{th}$ steps.
10) Repeat $4^{th}$-$9^{th}$ steps for +60°C.

11) Solder 0R resistor.
12) Tune communication between IOLD and IOLM via C/Q.
13) Tune climatic chamber to -40°C.
14) Check current consumption and right data exchange.
15) Tune climatic chamber to +60°C.
16) Check current consumption and right data exchange.

**Result:**

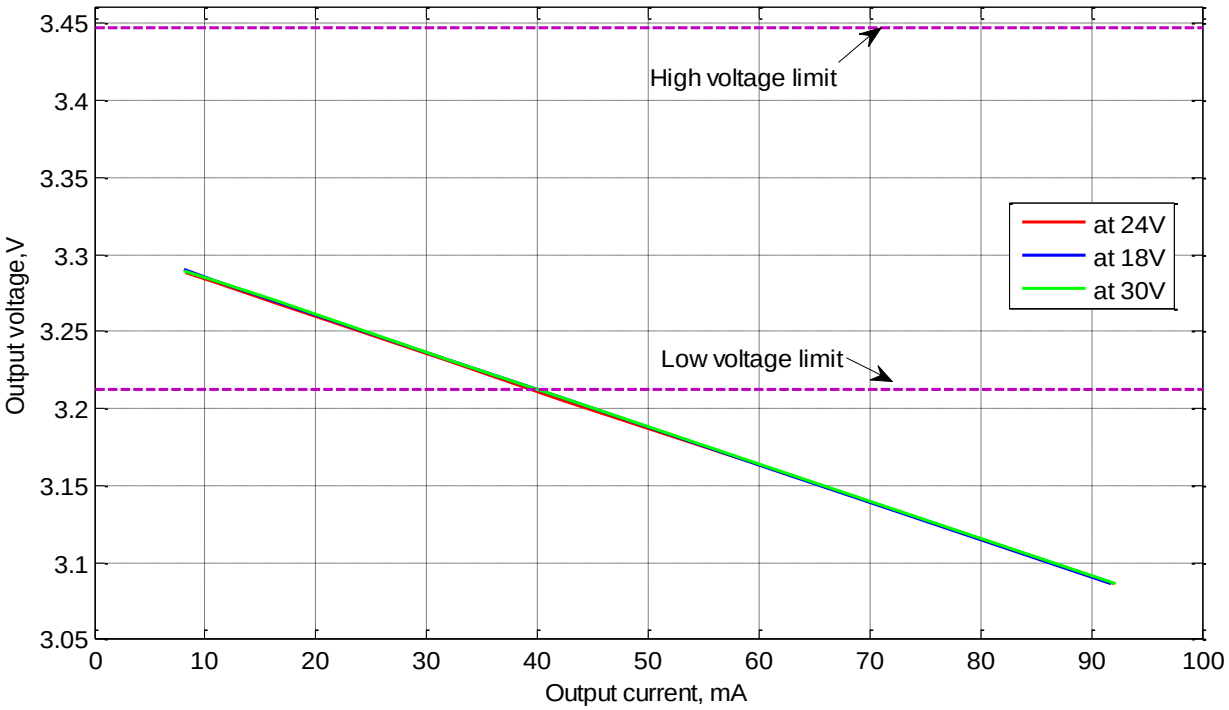



*Figure 7.14: Volt-ampere characteristic at -40°C*

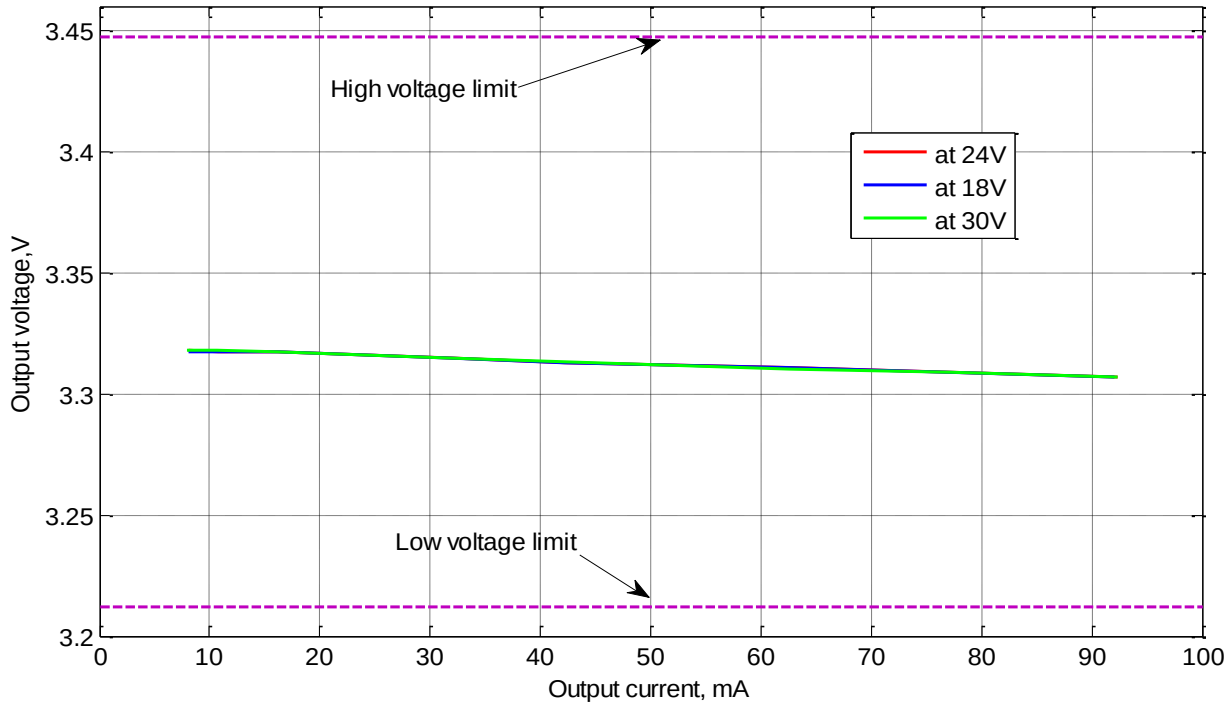



*Figure 7.15: Volt-ampere characteristic at +60°C*

**Conclusion:** according to obtained results, the Device passed temperature test for +60°C, and didn't pass for -40°C because overflowed specified voltage limits. Part of impulses is vanished, in case of skip part of impulses by converter, what is characteristically for converters at low loads. Communication was stable during all time of test (1 hour).

## 7.4. EMC testings

### 7.4.1. Measurement of conducted interference – PASSED

Goal: Determine the value and frequencies of noise, which IOLD transfers to the power grid

Test source: CISPR 16-1 [21]

Tests limits / Expected values:

| | Site | Frequency range | Limits |
|---|---|---|---|
| Limit 1 | Bridge and deck zone | 10 kHz – 150 kHz<br>150 kHz – 350 kHz<br>350 kHz – 30 MHz | 96dBµV – 50 dBµV<br>60dBµV – 50 dBµV<br>50 dBµV |
| Limit 2 | General power distribution zone | 10 kHz – 150 kHz<br>150 kHz – 350 kHz<br>350 kHz – 30 MHz | 120dBµV – 69 dBµV<br>79 dBµV<br>73 dBµV |

*Table 7.5: Measurement limits according to CISPR 16-1* [21]

There are two possibilities for usage of tested Device: in bridge and deck zone, and in general power distribution zone. This decision will depend on that fact if obtained waveform crosses or not specified limits shown above. If waveform crosses Limit 1 (Bridge and deck zone), it can be used only in general power distribution zone. If waveform crosses Limit 2 (General power distribution zone), Device cannot be used in industry and needs redesign.

**Test description:**

1) Wire the scheme shown on Figure 7.16.
2) Connect spectrum analyzer to LISN.
3) Measure conducted emission for N-wire (tune on LISN).
4) Check results according to limits.
5) Measure conducted emission for L-wire (tune on LISN).
6) Check results according to limits.

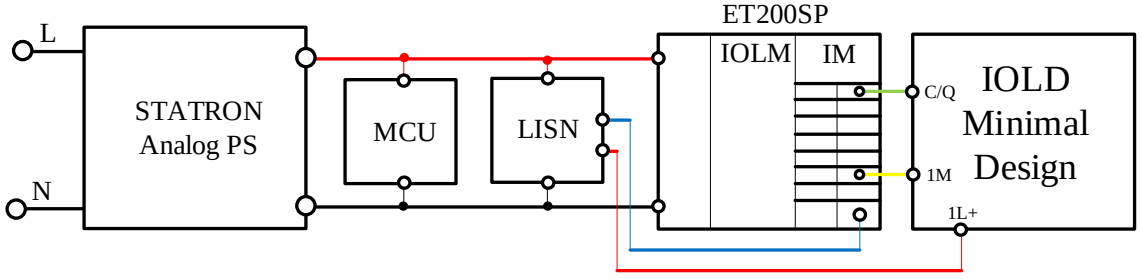



*Figure 7.16: Principal scheme for measurement of conducted inference*

**Result:**

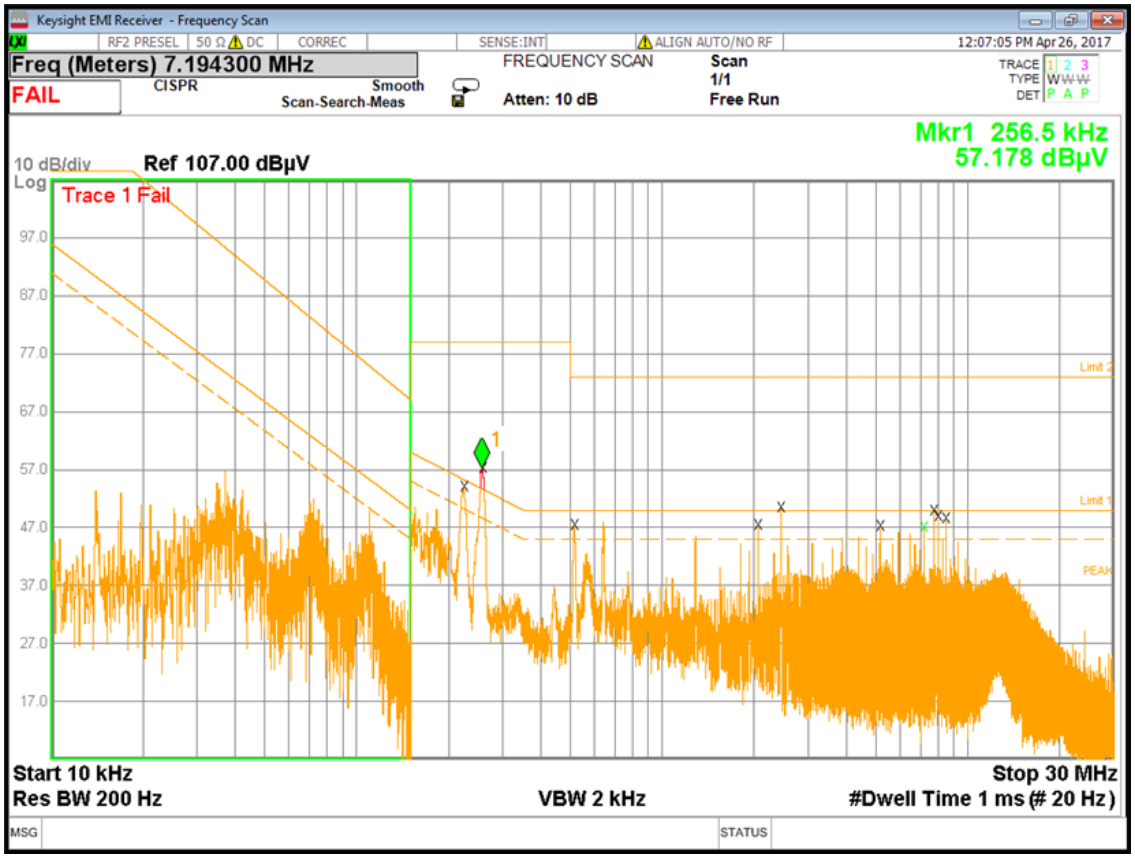



*Figure 7.17: Conducted interference from IOLD on N-wire*

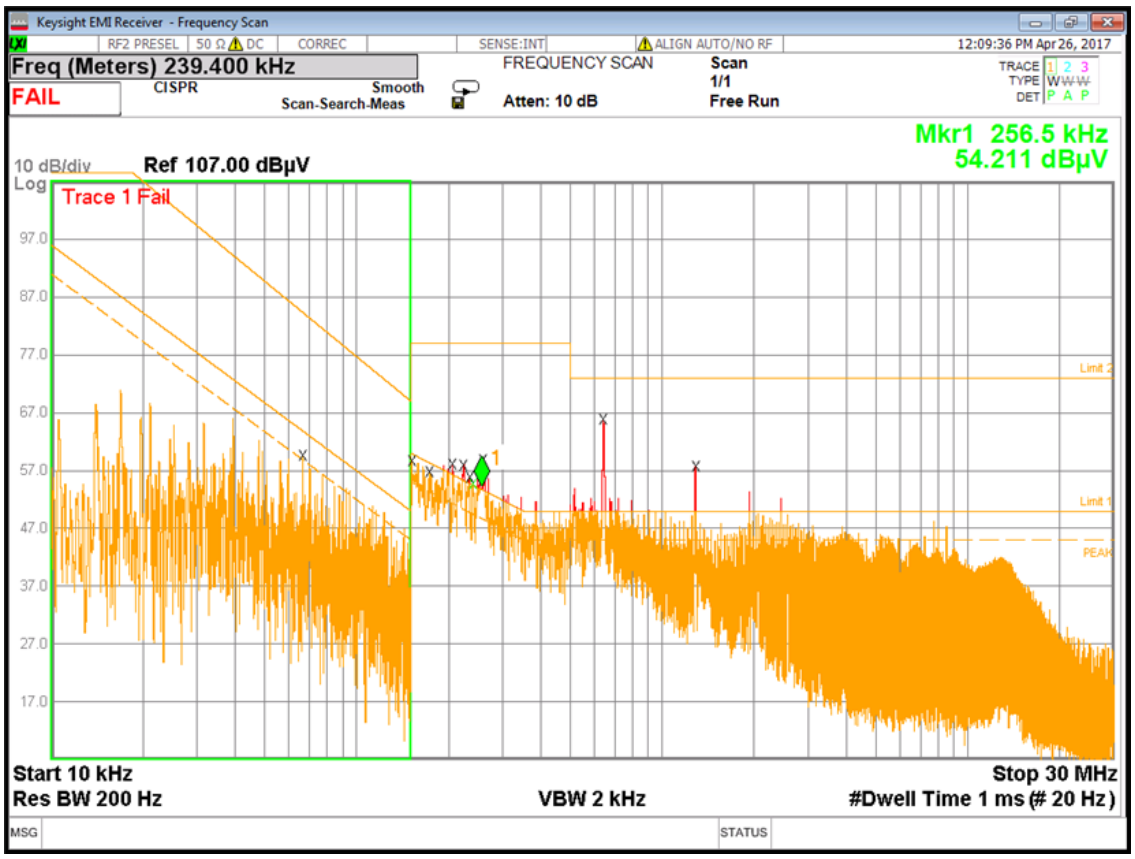



*Figure 7.18: Conducted interference from IOLD on L-wire*

| Frequency | QPD Amplitude | QPD Delta | Crossed limit |
|---|---|---|---|
| For N-wire | | | |
| 257.1 kHz | 57.331 dBµV | 3.691 dB | Limit 1 |
| For L-wire | | | |
| 222.9 kHz | 55.889 dBµV | 0.564 dB | Limit 1 |
| 258.6 kHz | 57.97 dBµV | 4.398 dB | Limit 1 |
| 639.28 kHz | 66.549 dBµV | 16.549 dB | Limit 1 |
| 1.2807 MHz | 57.213 dBµV | 7.213 dB | Limit 1 |

*Table 7.6: Values of maximal deviations from specified limits*

**Conclusion:** the goal of test is to determine the possible places and conditions for future correct employment of the Device, according to noise, which IOLD sends to the power grid. The limit for "Bridge and deck zone" was crossed one time for N-wire and four times for L-wire, what means that t**he IOLD Minimal Design v001 can be used in General power distribution zone.** Configuration "N-wire" and "L-wire" means that IOLD sends noise to the Neutral wire and Line wire in the power grid. LISN give us possibility to measure its influence separately on every power line wire. IOLD can be modified for usage in bridge and deck zone with using special input-output filters, another type and thickness of isolation and total redesign of Device.

### 7.4.2. Fast transient burst immunity test - PASSED

| | | |
|---|---|---|
| Goal: | | Check IOLD survival if apply burst signal to its wires |
| Test source: | | EN 61000-4-4 [22] |
| Tests limits / Expected values: | Pulse: | Amplitude: ± 1 kV / ± 2 kV |
| | | Rise time: 5 ns (10/90 % value) |
| | | Width: 50 ns (50 % value) |
| | | Repetition rate: 5 kHz |
| | | Performance criterion: B |

Note 1: The test should be applied to L+, C/Q and M simultaneously.

Note 2: Performance criterion A - The SDCI operating at an average cycle time shall not show more than six detected M-sequence errors within test. No interruption of communication is permitted.

Note 3: Performance criterion B - The error rate of criterion A shall also be satisfied after but not during the test. No change of actual operating state (e.g. permanent loss of communication) or stored data is allowed.

**Test description:**

1) Wire the scheme shown on Figure 7.19.
2) Tune the burst generator for generation of ±1kV 5 kHz impulses.
3) Make experiment; check the workability of IOLD and number of fails during the test.
4) Number of fails ≤ 6.
5) Repeat experiment with ±2kV 5 kHz.

CDN – Coupling-Decoupling Network – devices used for test reproducibility and protection of tested devices. CDNs have to used for direct transmitting of the disturbing signal to the different cables connected to the equipment under the test (EUT) and for preventing applied test signals from generators to other devices and auxiliary equipment (AUX).

CCC – Cable Coupling Clamp – reusable test conductor for the measuring of the shielding properties of cables.

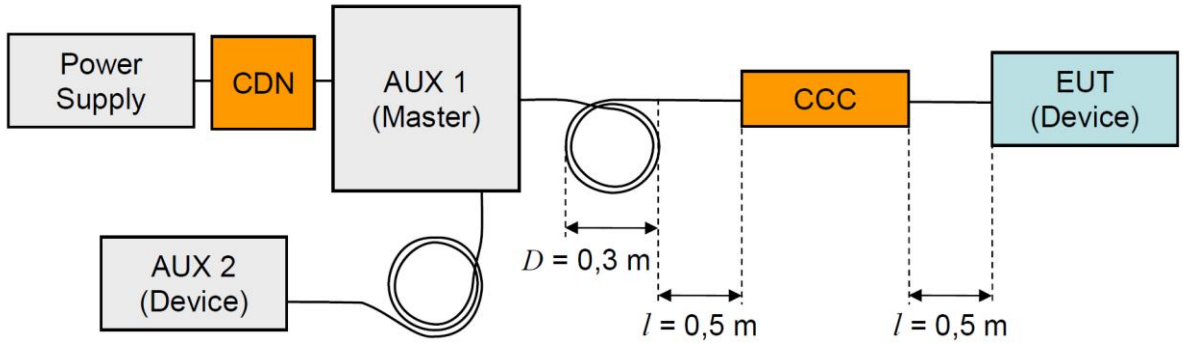



*Figure 7.19: Test setup for fast transients (Device)* [22]

**Conclusion:** during the test, the burst signals were applied to all ports of the Device. The test equipment generates 75 impulses 200µs duration every 300 ms. Total time of one package of impulses is 15 ms, total time of test is 180 seconds.

The goal of test is correct work of the Device, what means the absence of mistakes during the test or theirs number should be ≤ 6.

During the test, any mistake was not detected. After the test, Device works correctly.

## 7.4.3. Conducted high frequency test - PASSED

| | | |
|---|---|---|
| Goal: | | Check workability of communication between IOLD and IOLM, if to its wires will be applied high frequency noise with different frequency |
| Test source: | | EN 61000-4-6 [23] |
| Tests limits / Expected values: | Signal: | Frequency: 150 kHz – 80 MHz<br>Amplitude modulation: 80% 1 kHz<br>Signal level: 10 V RMS<br>Performance criterion: A |

**Test description:**

1) Wire the scheme shown on Figure 7.20. Measured equipment is supplied from isolating transformer.

2) Make calibration for conducted immunity test system with 50Ω load (use 150Ω to 50Ω adapter).

3) Set necessary configuration in control program of measuring device.

4) Start the program and check workability of IOLD throughout all time of experiment.

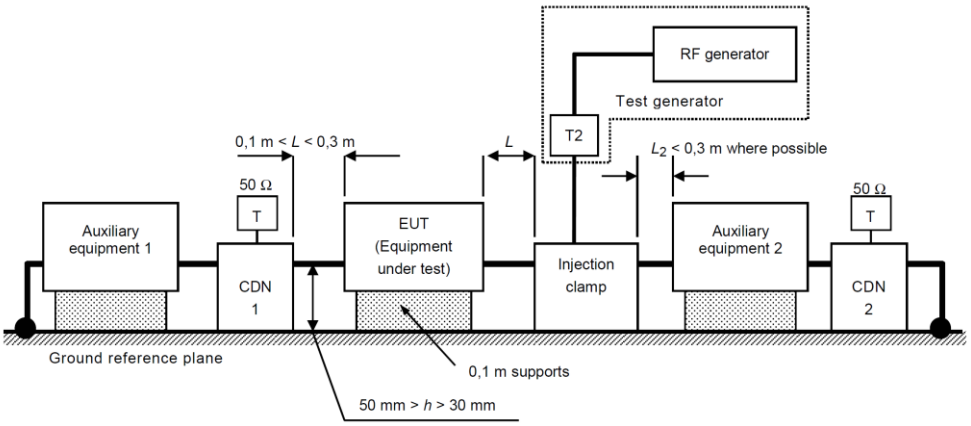



*Figure 7.20: Schematic set-up for immunity test to RF conducted disturbances* [22]

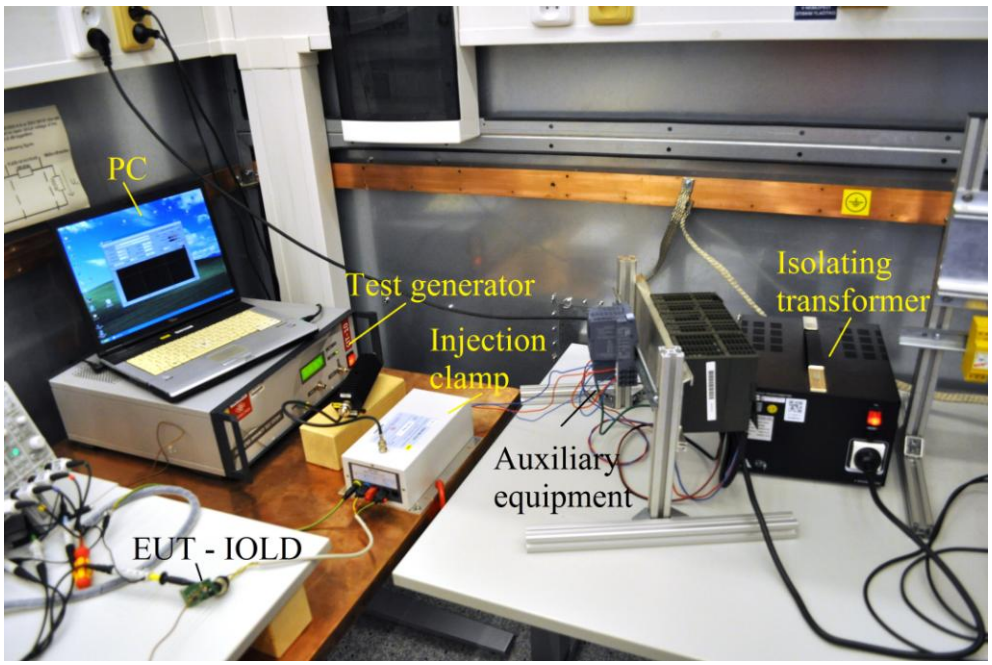



*Figure 7.21: Performance of measuring scheme*

**Conclusion:** with help of special generator, high frequency signal was applied to all ports of the Device. The goal of test is unbroken communication between the Device and Master, and correct work of the Device after the test, what were reached.

## 7.5 IO-Link tests

### 7.5.1. High-level input threshold voltage at Device C/Q port - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0016 [23] |
| Tests limits / Expected values: | 10.5V≤VID≤13.0V |
| Measured values: | VID (VSD=18V): 11.0225V |
| | VID (VSD=30V): 11.4913V |

**Precondition:** Device set to digital input test mode

**Test description:**

1) Apply minimum supply voltage (VSD = 18 V) to Device
2) Sweep voltage VID at C/Q from 5 V to 15 V
3) Monitor test input signal / indicator derived from input signal at C/Q
4) Measure VID for transition of test signal low >> high.
5) Repeat test with maximum supply voltage (VSD = 30 V)

**Result:**

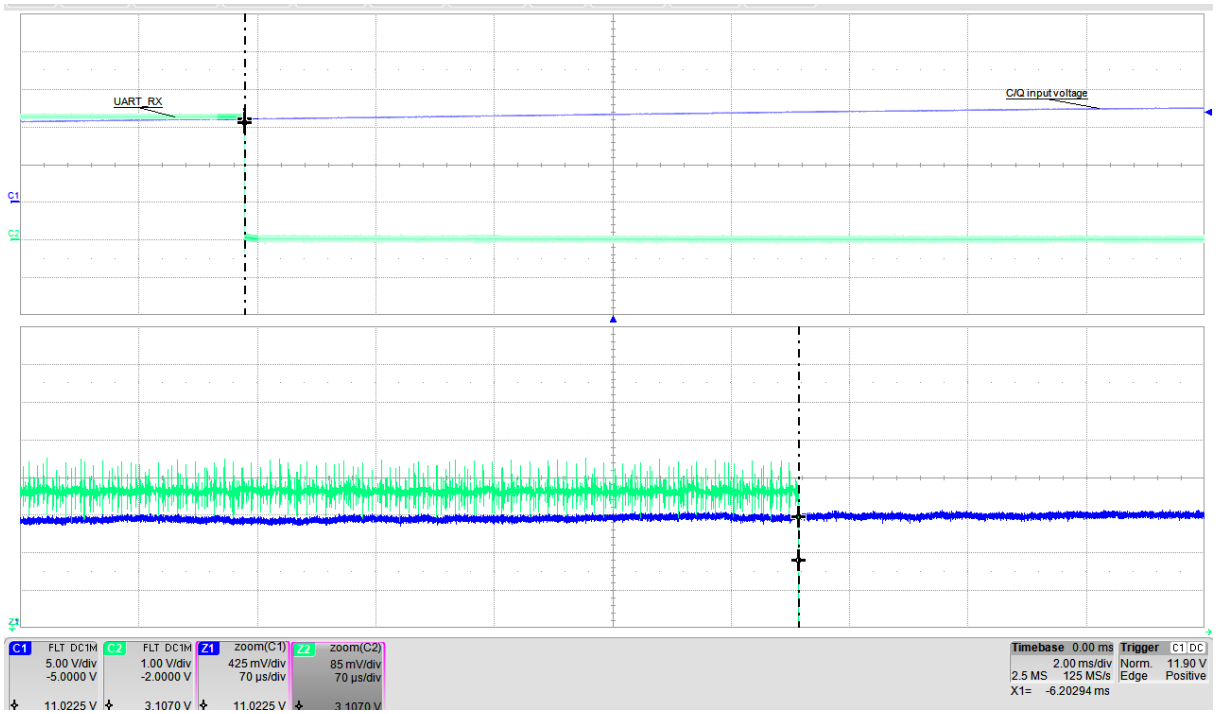



*Figure 7.22: Switch on limit VID (VSD=18V) : green – UART RX signal, blue – C/Q input voltage*

## 7.5.2. Low-level input threshold voltage at Device C/Q port - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0017 [23] |
| Tests limits / Expected values: | 8.0V≤VID≤11.5V |
| Measured values: | VID (VSD=18V): 9.1425V |
| | VID (VSD=30V): 9.5206V |

**Precondition:** Device set to digital input test mode

**Test description:**

1) Apply minimum supply voltage (VSD = 18 V) to Device
2) Sweep voltage VID at C/Q from 15 V to 5 V
3) Monitor test input signal / indicator derived from input signal at C/Q
4) Measure VID for transition of test signal high >> low.
5) Repeat test with maximum supply voltage (VSD = 30 V)

**Result:**

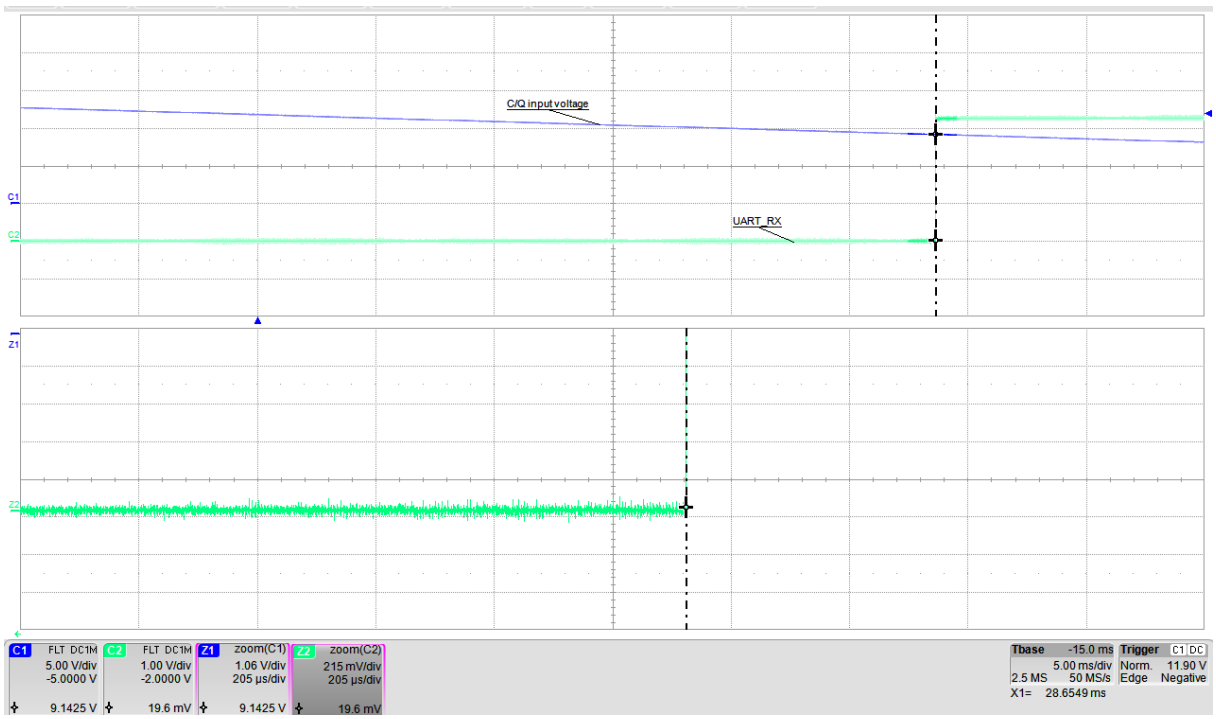



*Figure 7.23: Switch off limit VID (VSD=18V) : green – UART RX signal, blue – C/Q input voltage*

## 7.5.3. High-side DC driver limit at Device C/Q port - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0019 [23] |
| Tests limits / Expected values: | IQHD≤500mA |
| Measured values: | IQHD (VSD=18V): unstable |
| | IQHD (VSD=30V): unstable |

**Precondition:** a) Device set to standard I/O mode

b) C/Q output is high

**Test description:**

1) Apply minimum supply voltage (VSD = 18 V) to Device
2) Apply maximum DC driver load (current sink > 500 mA) to C/Q
3) Measure current IQHD at C/Q output
4) Check if IQHD is exceeding the specified limit
5) Repeat test with maximum supply voltage (VSD = 30 V)

**Result:**

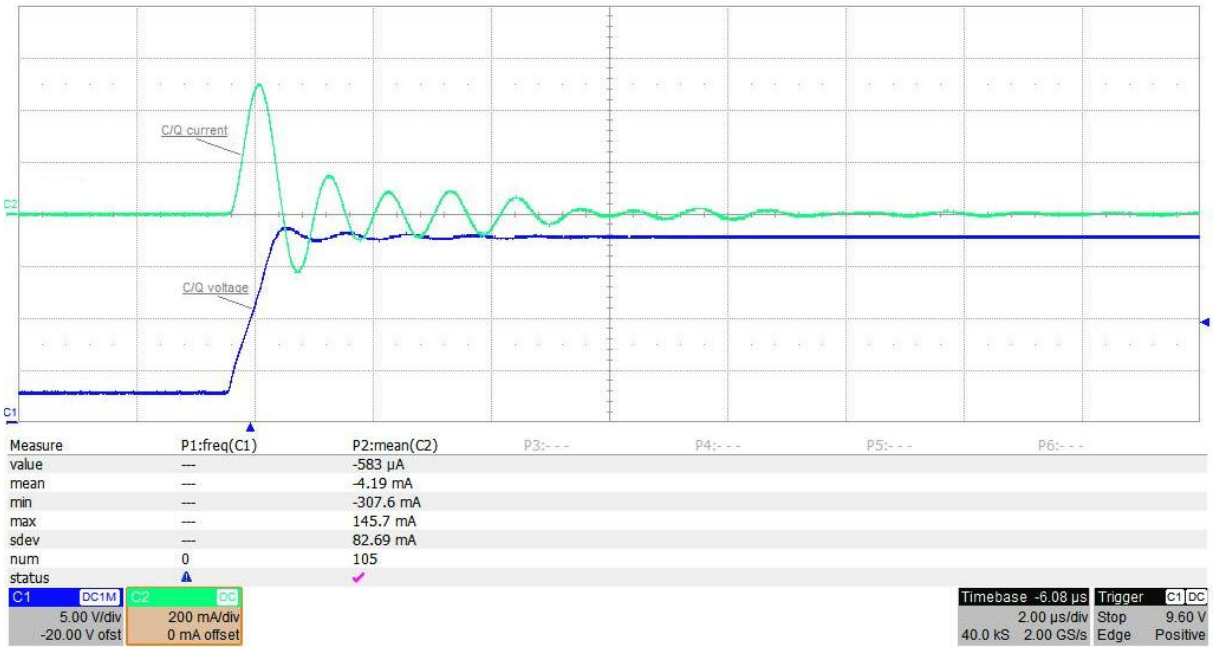



*Figure 7.24: C/Q output voltage and IQHD current at 18V input voltage : green – C/Q current, blue – C/Q voltage*

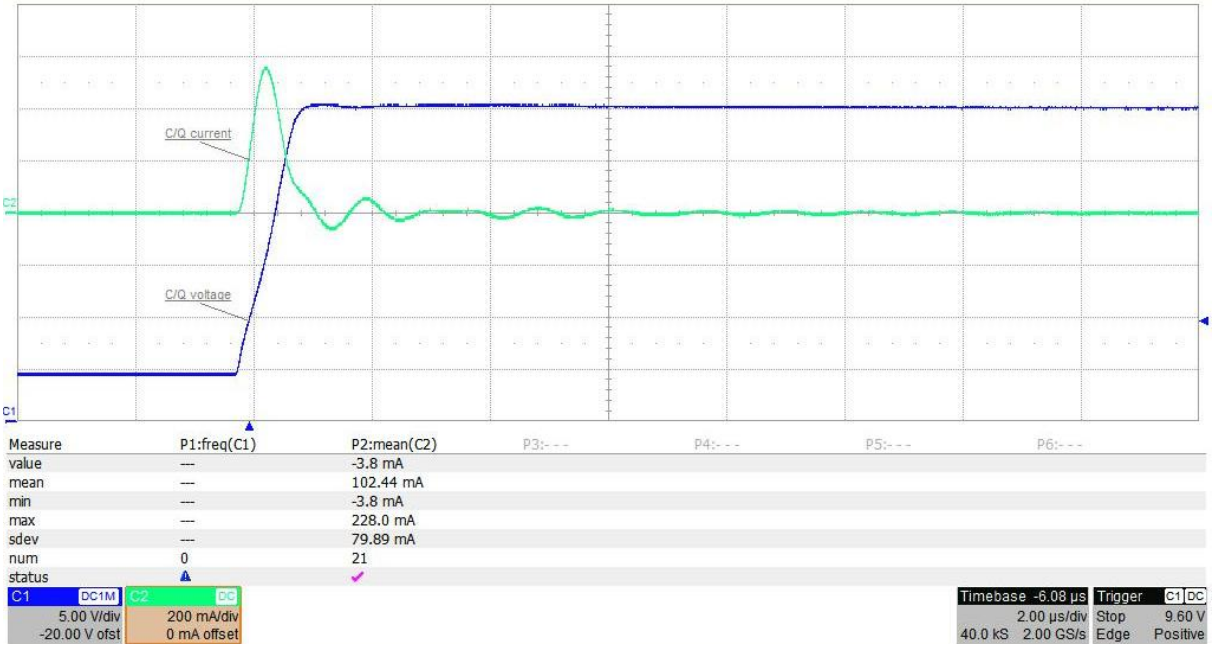



*Figure 7.25: C/Q output voltage and IQHD current at 30V input voltage* : *green – C/Q current, blue – C/Q voltage*

**Conclusion:** test is passed in case of satisfying of condition IQHD≤500mA and condition "current shall not statically flow". In PHY, there is protection for overcurrent, which is equal 450mA that is why the output waveforms are unstable.

## 7.5.4. Low-side DC driver limit at Device C/Q port - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0020 [23] |
| Tests limits / Expected values: | IQLD≤500mA |
| Measured values: | IQLD (VSD=18V): 288mA |
| | IQLD (VSD=30V): 297mA |

**Precondition:** a) Device set to standard I/O mode

b) C/Q output is low

**Test description:**

1) Apply minimum supply voltage (VSD = 18 V) to Device
2) Apply maximum DC driver load (current sink > 500 mA) to C/Q
3) Measure current IQLD at C/Q output
4) Check if IQLD is exceeding the specified limit
5) Repeat test with maximum supply voltage (VSD = 30 V)

**Result:**

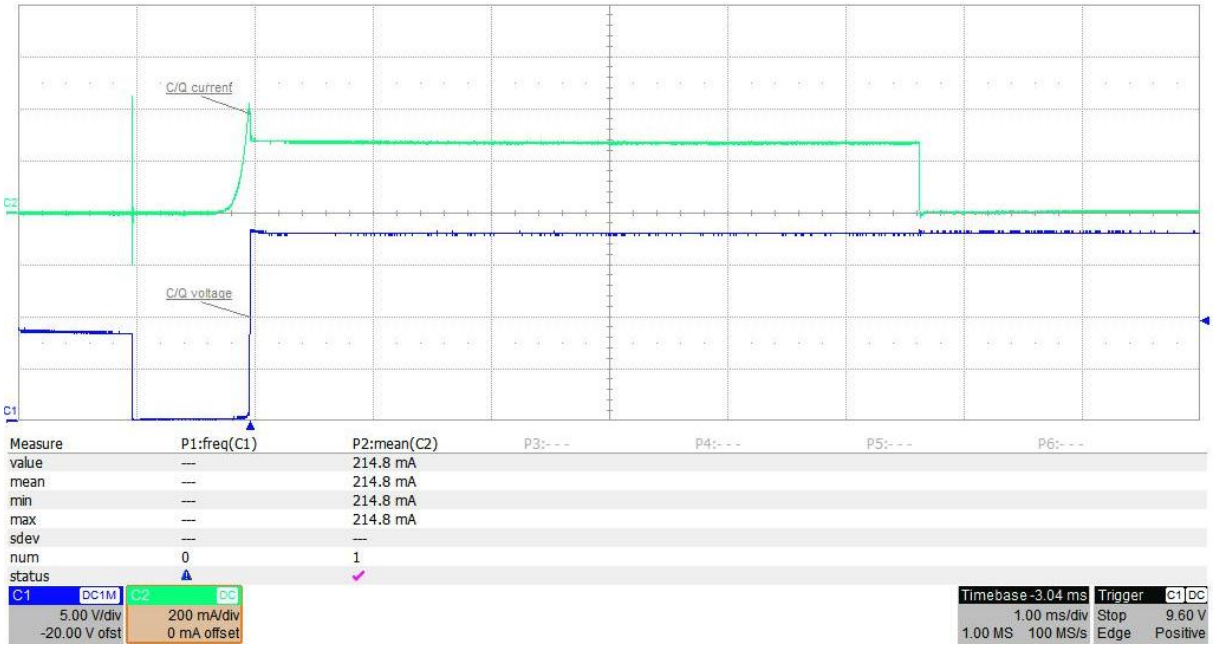



*Figure 7.26: C/Q output voltage and IQLD current at 18V input voltage* : *green – C/Q current, blue – C/Q voltage*

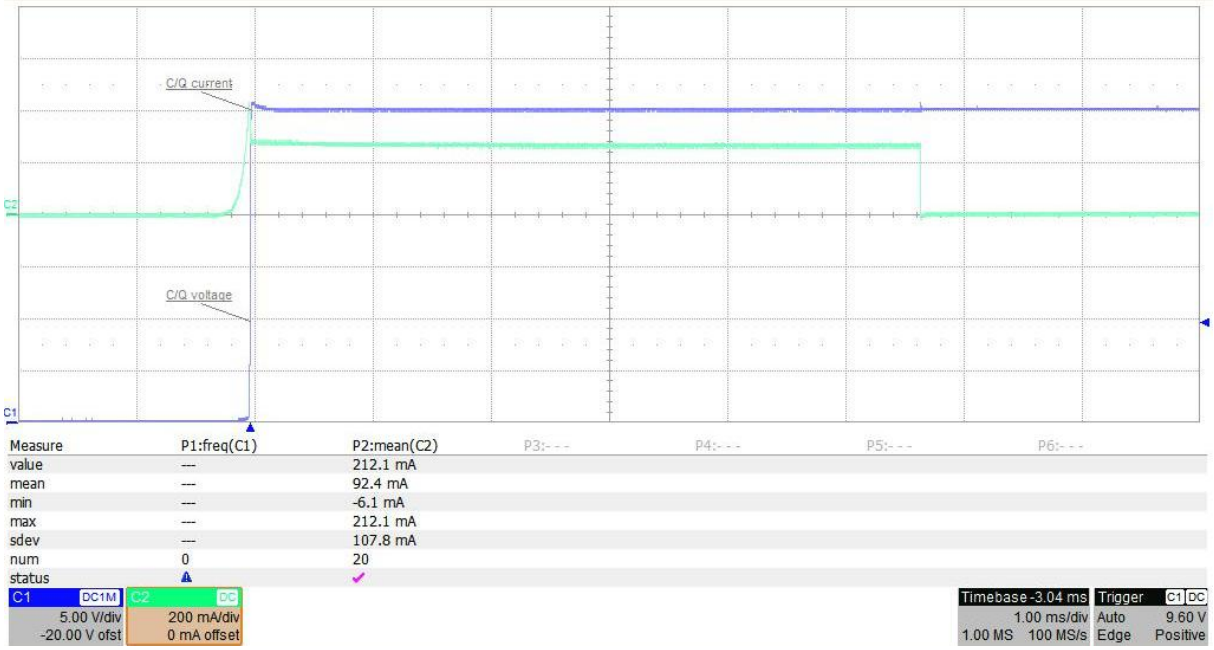



*Figure 7.27: C/Q output voltage and IQLD current at 30V input voltage* : *green – C/Q current, blue – C/Q voltage*

**Conclusion:** test is passed in case of satisfying of condition IQLD≤500mA and condition "current shall not statically flow". In PHY, there is protection for overcurrent, which is equal 450mA that is why the output waveforms are unstable. Protection works periodically what says about overheating during its work.

## 7.5.5. Permissible voltage range at Device C/Q port - FAILED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0300 [23] |
| Tests limits / Expected values: | Communication established |
| Measured values: | Damage of diodes |

**Precondition:** a) Device is in SDCI mode
b) Disconnect C/Q from Master port
c) Device is waiting for reception of SDCI messages (C/Q in receive state)

**Test description:**

1) Apply maximum supply voltage (VSD = 30 V) to Device
2) Apply voltage of +1V between C/Q and L+ via a series resistance of 1Ω for at least 1 min
3) Apply voltage of -1V between C/Q and M via a series resistance of 1Ω for at least 1 min
4) Attach a Master and perform communication

**Conclusion:** during the test, the protection diodes were destroyed. Because of this in the next redesign there was made the decision to substitute the PHY protecting Schottky diodes SD103AWS by the next diode:

| | |
|---|---|
| Name | Schottky Diode NXP PMEG4010EJ.115 |
| Forward current | 1A |
| Reverse voltage | 40V |
| Package | SOD323F (1.6x3.5mm) |

## 7.5.6. Wake-Up pulse detection low - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0026 [23] |
| Tests limits / Expected values: | Test signal/indicator indicate a received wake-up request |

**Precondition:** Device in SIO-mode or after power-on (no communication). C/Q level is brought to high-signal.

**Test description:**

1) Apply minimum supply voltage (VSD = 18 V) to Master
2) Apply current pulse with IQWU = $IQPKL_{min}$ (current source) and $TWU_{min}$ (75 µs) to C/Q.
3) Monitor test signal / indicator at Device
4) Check if test signal / indicator indicate a wake-up request
5) Repeat test with $TWU_{max}$ (85 µs)
6) Repeat test ($TWU_{min/max}$) with maximum supply voltage (VSD = 30 V)

**Result:**

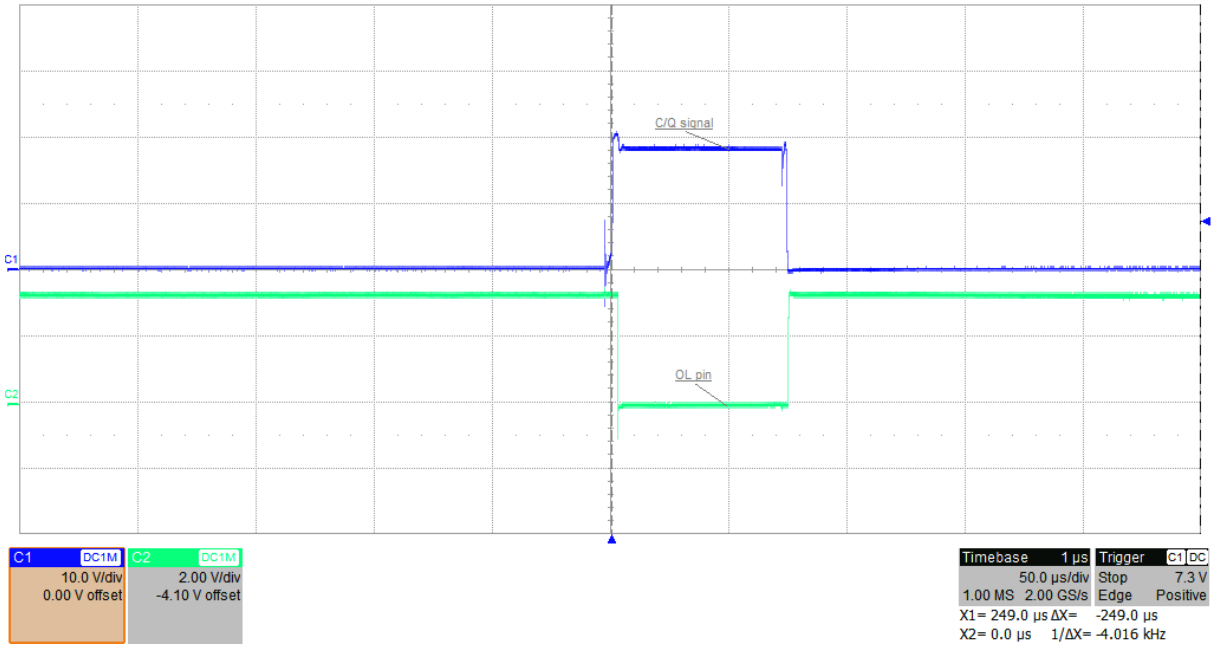



*Figure 7.28: Direct wake-up impulse with TWUmax = 75 µs at VSD = 18V : green – OL pin, blue – C/Q voltage*

**Conclusion:** according to obtained figures, the Device correctly indicates wake-up pulse at any duration of pulse in range 75µs - 85µs and at any voltage at range 18V – 30V.

## 7.5.7. SDCI readiness delay - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0029 [23] |
| Tests limits / Expected values: | $TRDL_{max}$=300ms, $VSD_{min}$=18V, WURQ=85µs<br>SDCI mode is entered |

**Test description:**

1) Apply supply voltage (VSD = 24 V) to Device
2) Apply a wake-up sequence with a delay of $TRDL_{max}$ after VSD has reached $VSD_{min}$.
3) Check if the SDCI mode was entered within the first wake-up sequence

**Result:**

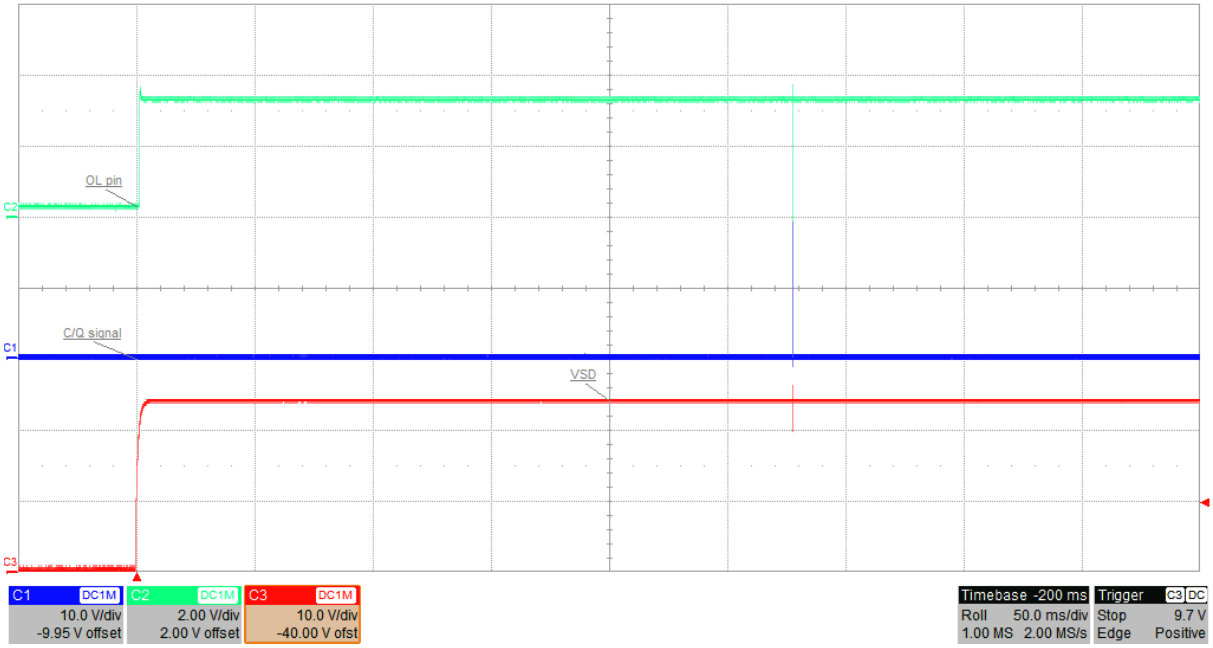



*Figure 7.29: Direct wake-up impulse with TWUmax = 85 µs TRDLmax=280ms at VSD = 24V : green – OL pin, blue – C/Q voltage, red – Device supply voltage*

**Conclusion:** according to obtained figure, the Device correctly indicates wake-up pulse after switching on. In our case $TRDL_{max}$=280ms.

## 7.5.8. Time to Fallback after Master command - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0302 [23] |
| Tests limits / Expected values: | OPERATE: 3 MasterCycleTime (82ms)≤$T_{FBD}$≤500ms |
| | PREOPERATE: 3 Tinitcyc (22 ms) ≤$T_{FBD}$≤500ms |

**Precondition:** a) Master and Device system in SIO-Mode

b) Device with SIO-support stimulated to deliver a H-level at C/Q

**Test description:**

1) Set Device to SDCI OPERATE mode
2) Set Device to standard I/O mode (apply “Fallback” Master command)
3) Monitor level at C/Q
4) Measure time from end of the First Device reply message to a Master write message with MasterCommand “Fallback” and the transition to stable 'H -level at C/Q
5) Repeat steps 2nd-4th with Device set to SDCI PREOPERATE mode

**Result:**

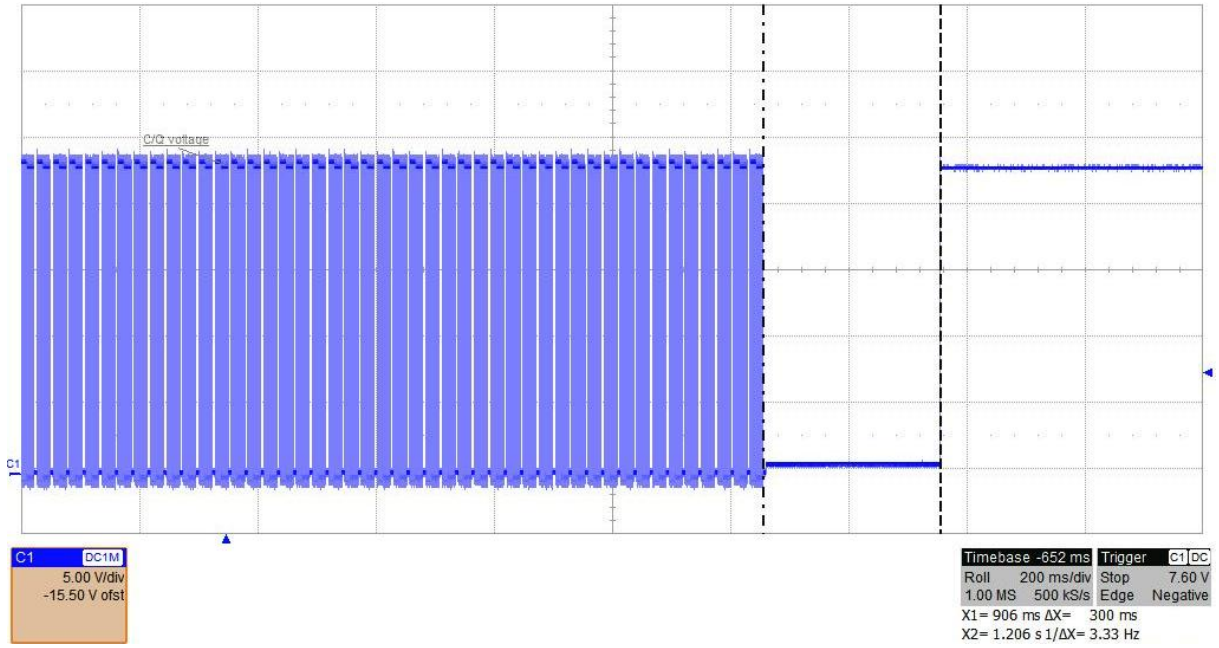



*Figure 7.30: Reaction of Device after MasterCommand "Fallback", OPERATE mode*

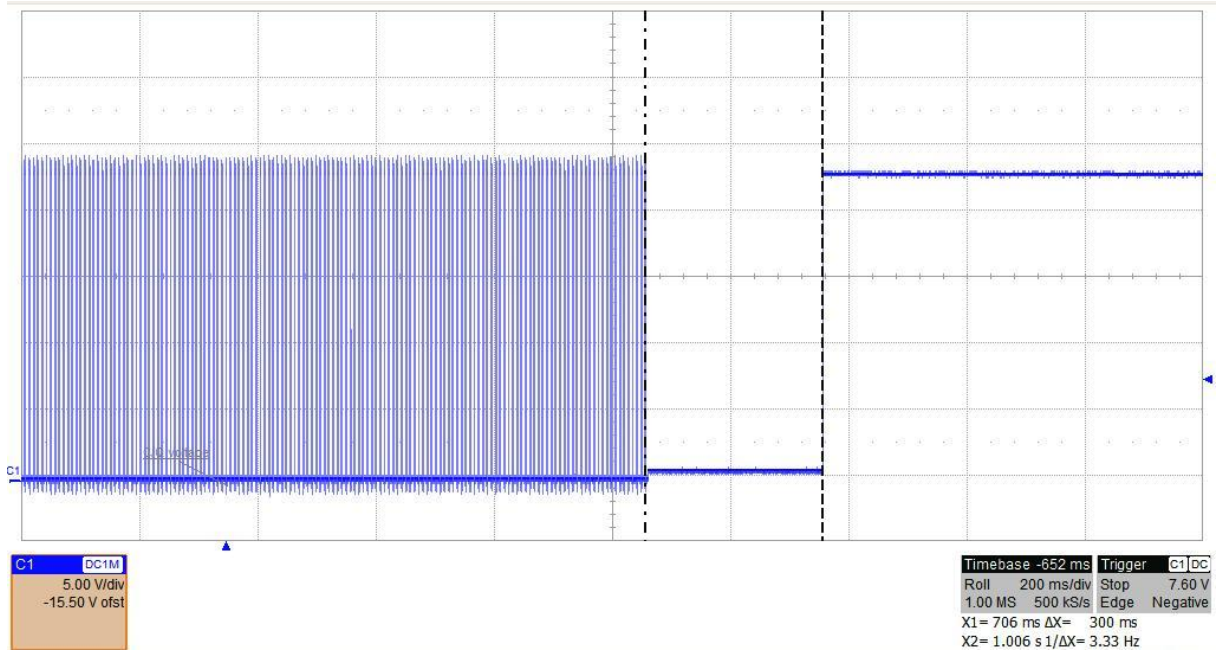



*Figure 7.31: Reaction of Device after MasterCommand "Fallback", PREOPERATE mode*

**Conclusion:** according to obtained figures, the Device correct answers to Master Fallback command.

## 7.5.9. UART frame eye-diagram with minimum load (Device) - PASSED

| | |
|---|---|
| Test source: | IO-Link Test specification V1.1.2 - SDCI_TC_0297 [23] |
| Tests limits / Expected values: | Bit waveform meet requirements of the eye-diagram |

**Test description:**

1) Attach line simulation (l = 0.5 m) with minimum load values ($C_{max}$ < 50 pF, $R_{max}$ = 100 mΩ)
2) Apply minimum supply voltage (VSM = 20V)
3) Set Master to SDCI mode
4) Check UART frame waveform on the receiver side
5) Repeat with maximum supply voltage (VSM = 30V)

**Result:**

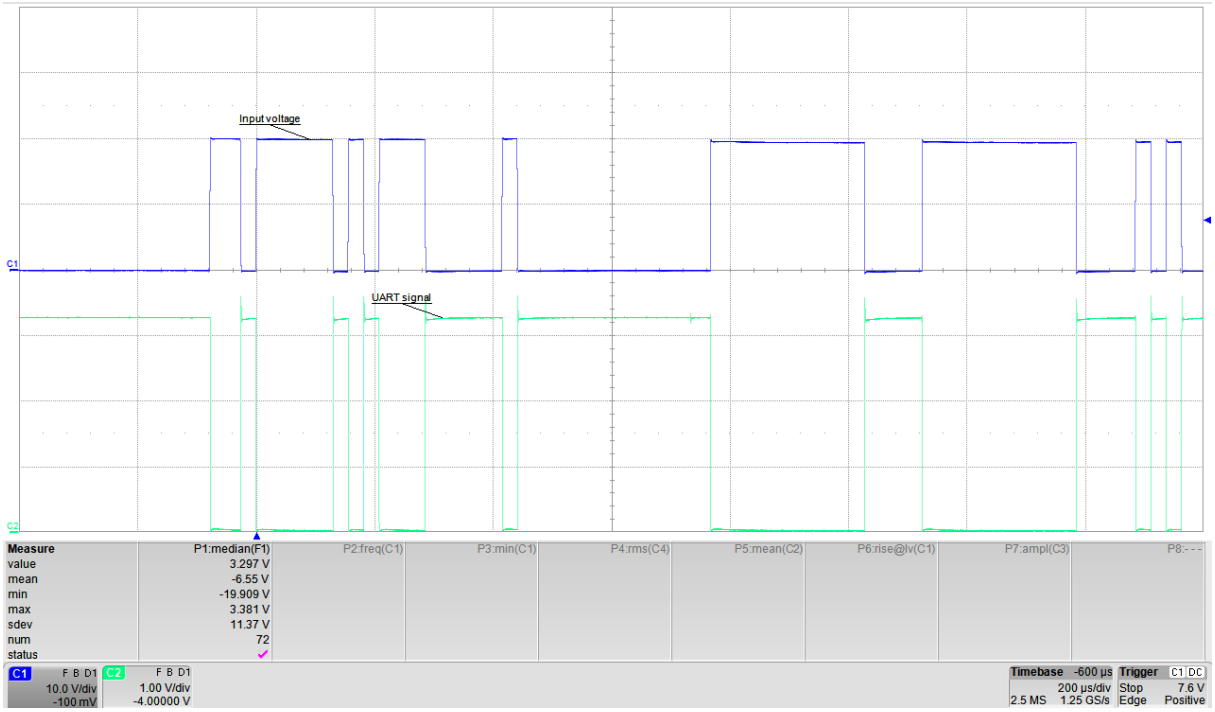



*Figure 7.32: Master and UART frame waveforms at VSM = 20V : green – UART signal, blue – C/Q voltage*

**Conclusion:** according to obtained figures, the waveforms are almost identical. Difference is small, what is not critical for IO-Link communication.

# 8. Conclusion

In this thesis, a quick look on IO-Link technology, its applications and usage in data transition have been granted. There were described all main layers: physical, data link, application layers.

The IOLD consists from four parts: power supply and periphery, microcontroller unit and periphery, PHY and LED's. Power supply is designed to 3.3V output voltage and 0.1A forward current. Likewise, as MCU was chosen STM32F071C8U6, to which directly were connected identification LEDs and PHY. For providing necessary communication speed was chosen 11.0592 MHz crystal.

After production and assembling of all components on PCB, every working unit was tested according to standards such as IEC 61131-2, NAMUR NE 21, CISPR 16-1, EN 61000-4-4, EN 61000-4-6 and IO-Link Test specification V1.1.2. Results of testings satisfied calculations and standard's norms. However, not all test was passed. That means the IO-Link Device Minimal Design needs in future be redesigned, namely, replacement of two Schottky diodes, which provide protection of PHY from reverse currents and changes in supply voltage; supplement additional filters for using the IOLD in bridge and deck zone.

Since the IO-Link Device Minimal Design is only the prototype of future device, more accurate, strict testings and possible small redesign are waiting for IOLD. According to this, I consider the aim of this diploma work is fulfilled.

# List of attachments

Principal scheme of IO-Link Device Minimal Design (confidential)

# CD content

CD contains the pdf version of diploma thesis and electrical principal scheme of IO-Link Device Minimal Design. The content of CD is confidential. After defense of a diploma thesis CD will be destroyed according to copyright rules.

# List of abbreviations

AC – Alternating Current

ADC – Analog-to-Digital Converter

AL – Application Layer

ARM – Advanced RISC Machine

CISPR – Comité International Spécial des Perturbations Radioélectriques

DC – Direct Current

DL command – Dataline command

DLL – Data Line Layer

EMC –Electromagnetic Compatibility

EMI – Electromagnetic Interference

EUT – Equipment Under the Test

FW – Firmware

GND – Ground

GPIO – General-Purpose Input/Output

I2C – Inter-Integrated Circuit

IEC – International Electrotechnical Commission

IOLD – IO-Link Device

IOLM – IO-Link Master

$I_{ppMAX}$ – Maximal peak-to-peak current

IQHD – DC driver current P-switching output ("On" state)

IQLD – DC driver current N-switching output ("On" state)

IQPKH – High peak current of Master’s wake-up current pulse

IQPKL – Low peak current of Master’s wake-up current pulse

IQWU – Amplitude of Master’s wake-up current pulse

JTAG – Joint Test Action Group

LED – Light-Emitting Diode

LISN – Line Impedance Stabilization Network

MCU – Microcontroller Unit

PCB – Printed Circuit Board

PHY – Physical Layer

QPD – Quasi-Probability Distribution

RAM – Random-Access Memory

RF – Radio frequency

RISC – Reduced Instruction Set Computer

SDCI – Single-Drop Digital Communication Interface

SDL – Shut down voltage limit

SM – System Management

SPI – Serial Peripheral Interface

STM – Synchronous Transfer Mode

SUL – Start up voltage limit

SWD – Serial Wire Debug

$T_{BIT}$ – bit time (measured in s)

TRDL – Wake-up readiness following power-on

$T_{REN}$ – Receive enable delay

$T_{WU}$ – Pulse duration of wake-up request

UART – Universal Asynchronous Receiver-Transmitter

VDD, VDDA – “+” pin for power supplying

VDDIO2 – VDD pin for power supplying only IOs of MCU

VHYS – hysteresis of receiver threshold voltage (measured in V)

VID – Input voltage at connection C/Q with reference to V0 (measured in V) of Device

VIH – input voltage range at connection C/Q for high signal (measured in V)

VIL – input voltage range at connection C/Q for low signal (measured in V)

VRQHD – Residual voltage 'H'

VRQLD – Residual voltage 'L'

VSD – Voltage Supply of Device

VSS, VSSA – “-” pin for power supplying

VTHH – threshold voltage of receiver for safe detection of a high signal (measured in V)

VTHL – threshold voltage of receiver for safe detection of a low signal (measured in V)

# List of Figures

# List of Tables

# Literature and references


[1] IEC 61131-2. Programmable controllers – Part 2: Equipment requirements and tests

[2] SIEMENS. IO-Link Masters. URL: *http://w3.siemens.com/mcms/programmable-logic-controller/en/basic-controller/s7-1200/special-modules/tabcard/pages/io-link.aspx*

[3] IEC 60947-5-2:2007, Low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - Proximity switches

[4] Overview: Is IO-Link the new communication standard? URL: *http://blog.wika.com/knowhow/io-link/*

[5] IO-Link Interface and system specification V1.1.2, 07/2013, IO-Link Community 10.002

[6] IO-Link – popis digitální komunikace pro sensory. URL: *http://automatizace.hw.cz/iolink-popis-digitalni-komunikace-pro-senzory*

[7] IO-Link system Functional manual, 01/2013, SIEMENS A5E31637677-AA

[8] TPS54040 0.5-A, 42-V Step Down DC/DC Converter with Eco-Mode (TM). URL: *http://www.ti.com/lit/ds/symlink/tps54040.pdf*

[9] SD103AWS - SD103CWS. URL: https://www.diodes.com/assets/Datasheets/ds30101.pdf

[10] SwitcherPro(TM) Switching Power Supply Design Tool. URL: *http://www.ti.com/tool/switcherpro*

[11] Reducing EMI in buck converters. URL: *http://www.richtek.com/Design%20Support/Technical%20Document/AN045*

[12] STM32L071x8 STM32L071xB STM32L071xZ. Access line ultra-low-power 32-bit MCU ARM®-based Cortex®-M0+, up to 192KB Flash, 20KB SRAM, 6KB EEPROM, ADC. URL: *http://www.st.com/content/ccc/resource/technical/document/datasheet/b5/24/80/11/51/59/47/f7/DM00141136.pdf/files/DM00141136.pdf/jcr:content/translations/en.DM00141136.pdf*

[13] AN4467. Getting started with STM32L0xx hardware development. URL: *http://www.st.com/content/ccc/resource/technical/document/application_note/fd/f4/6b/40/9a/b5/41/a2/DM00112257.pdf/files/DM00112257.pdf/jcr:content/translations/en.DM00112257.pdf*

[14] AN1709. EMC design guide for ST microcontrollers. URL: *http://www.st.com/content/ccc/resource/technical/document/application_note/a2/9c/07/d9/2a/b2/47/dc/CD00004479.pdf/files/CD00004479.pdf/jcr:content/translations/en.CD00004479.pdf*

[15] Texas Instruments. Serial Wire Debug—Ideal for Microcontrollers. URL: *http://www.ti.com/lit/wp/spmy004/spmy004.pdf*

[16] L6362A – IO-Link Device Transceiver. URL: http://www.st.com/content/ccc/resource/technical/document/datasheet/12/f7/23/8b/fa/07/48/98/DM00170703.pdf/files/DM00170703.pdf/jcr:content/translations/en.DM00170703.pdf

[17] LG L29K. URL: *http://www.osram-os.com/Graphics/XPic2/00077107_0.pdf*

[18] LS L29K. URL: *http://www.osram-os.com/Graphics/XPic2/00077099_0.pdf*

[19] M. Duncan: EAGLE V6 Getting Started Guide, 2013, ISBN 978-1-907920-20-2

[20] NAMUR NE 21. Electromagnetic Compatibility of Industrial Process and Laboratory Control Equipment

[21] CISPR 16-1:2015. Specification for radio disturbance and immunity measuring apparatus and methods - Part 1: Radio disturbance and immunity measuring apparatus

[22] EN 61000-4-4. Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical Fast Transient / Burst Immunity Test

[23] IEC 61000-4-6. Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields

[24] IO-Link Test Specification V1.1.2, 07/2014, IO-Link Community 10.032