Opponent's report on the master's thesis

„Implementation of the MSC compression algorithm in field programmable array"

Author: **Bc. Jakub Řada**

The reviewed master's thesis is the well-written work about (besides other things) a hardware implementation of multistream compression algorithm (MSC) that was invented by Czech scientist. The work contains the description of MSC algorithm step by step, there are discussed its different modifications (coding) and reflected its advantages and disadvantages there. The RTL design method is described in the general level only. The choice of hardware is focused on the specified requirements for the algorithm and it is also assessed in chapter 7. It is necessary to note that the student has studied the software implementation in details although only one sentence about it is written it his master's thesis. The core of the work is chapter 5 and 6. The chapters describe the whole MSC hardware design, operational specifications of individual structures. The implemented algorithm couldn't be verified unambiguously because the decompression algorithm wasn't a goal of this work. There was also described the problem regarding to lack of memory. However, the problems should be expected in such a kind of work.

Five goals had to be fulfilled in the presented master's thesis:

1) Get acquainted with principles of logical circuits design in the FPGA.
2) Read up working principles of the multistream compression algorithm.
3) Design the block architecture of the compression module with regard to the implementation on a hardware platform.
4) Specify the requirements for selection of the FPGA needed for the implementation.
5) Implement selected blocks.

I can say that the fulfilment of tasks 1) and 2) is apparent from the content of the entire work and the writing of chapters 2 and 3 can be considered as their objective fulfillment. The task 4) is fulfilled in chapter 4. Tasks 3) and 5) are fulfilled in chapters 5 and 6.

The main objective contribution of this master's thesis is the original hardware implementation of the compression algorithm that was never done before.

As the opponent, I have one minor remark to the thesis. There is written in the thesis that you use two time domains. However, the "connection" of domains isn't described in more details. Can you explain, please, how is it really solved in your design during the defence?

Based on my comments

I recommend the master's thesis for the defence.

Summary classification of the master's thesis.....A (excellent)…1.0

In Prague on January 12th 2017

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