

REFERENCE OF DIPLOMA THESIS SUPERVISORS

Implementation of the MSC Compress Algorithm in Field Programmable Gate Arrays

student
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The diploma thesis is focused on the design and implementation of the special compress algorithm created and patented by Jiří Kochánek. Before this thesis has been finished, the algorithm was implemented only in a software way by the author of the algorithm himself with using of pseudo-parallelism features. There were indications of high yields from modifying the algorithm to a parallel implementation.

The topic of the diploma thesis was really wide. For fully understanding the algorithm principles, the candidate had to study the C source codes rigorously. Before starting own effective FPGA implementation the candidate rewrote the source code and made debugging on a PC platform. The candidate carried out an analysis of available FPGA and on the basis of that chose an appropriate part for further implementation and then fully designed selected parts of the algorithm for assigned platform in the VHDL language.

The candidate has demonstrated that he is capable of advanced creative engineering attitude.

During elaborating the thesis the candidate not only had to study the design principles of digital circuits using FPGA platform but also he had to learn how to design in VHDL language, which is not lectured in any course carried on by the Faculty of Transportation Sciences. We must pinpoint his personal interest in this issue; he regularly attended consultations with the thesis supervisors.

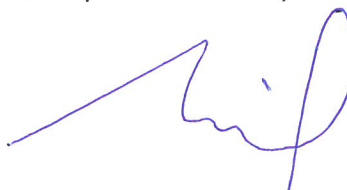
From formal and linguistic point of view, the thesis is on a very good level. The work assignment has been fulfilled in all points.

Both supervisors evaluate the diploma thesis by the mark **A (excellent)** and recommend it for the defence.

doc. Ing. Vít Fábera, Ph.D.
Ústav aplikované informatiky v dopravě



Ing. Tomáš Musil, Ph.D.
Ústav dopravní telematiky



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