

Electronic Systems

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Subject Master's Thesis Review

Date 21 May 2015 Having read the Master's thesis titled "Algorithms for Mapping and Scheduling Real-Time Streaming Applications on Heterogeneous Multi-core Platforms", by Bc. Jakub Kopřiva, I proceed to provide my assessment of it.

The topic of the thesis is interesting to me, covering a relevant area of research and I enjoyed reading it. The scope of the thesis is quite broad, tackling not just the problems of mapping and scheduling of dataflow applications on heterogeneous multi-core platforms, as alluded to in the title, but also the reduction of the processing time required to achieve these solutions. The thesis is in general well written with an acceptable level of English used.

Chapter 1 provides the introduction, stating the problems that the thesis addresses. The problems are clearly defined, but there is a lack of motivation for design choices that have already been taken at this stage, such as the use of SDF as a model of computation and ILP for optimisation. While it is understandable that this information might be provided in later chapters, I cannot find these motivations anywhere in the thesis.

Background information is provided in Chapter 2, giving a clear and concise overview of SDF modelling with appropriate illustrations. Section 2.2 provides a short overview of HSDF without motivation for why this is necessary as it was not mentioned up until this point. HSDF is not mentioned again until the experimentation in Chapter 6 where the number of HSDF actors/channels are compared with the number of SDF actors/channels for equivalent graphs. It is not clear what this comparison contributes to the thesis as it is unrelated to the rest of the contents.

A problem formulation is provided in Chapter 3. It is a short chapter that starts with the sentence "We have been given a SDF model to work with." This is not sufficient motivation for solving a problem. In general, this chapter expands on the problem statement given in the introduction given the background information.

Chapter 4, from my understanding, is also primarily a background chapter. Section 4.1 provides a description of an existing SDF ILP formulation. Equation 4.2 appears to be missing a "(t)" after E_{t_s} . Figure 4.2 has labels with static values for t of 0 and 4 on cores p_1 and p_2 , respectively. This appears to be a copy and paste mistake. Section 4.2 provides what is described as a baseline ILP improvement. I disagree with the use of the word improvement. Section 4.2 extends the constraints used to restrict the search space for the objectives that this thesis wishes to achieve. Whether this is an improvement of the baseline ILP is subjective. Section 4.3 provides linearisations of some of the constraints from



Section 4.1. In my opinion, Section 4.3 is implementation detail of the background material from Section 4.1, rather than a significant contribution of the thesis. There also appears to be missing constraints $X_{i,j}(t) \ge 0$ and $Z_t \ge 0$.

Contributions of this thesis are mainly contained in Chapter 5. These contributions are "lazy constraints" for the CPLEX solver and a "symmetry breaking" algorithm, to reduce the search space. The introduction of Chapter 5 does not mention the symmetry breaking contribution. No motivation is given for why the CPLEX solver is used, or why lazy constraints are the focus of the speed up attempts. Nevertheless, detailed explanations are given on how the lazy constraints are implemented for the Java CPLEX API.

The symmetry breaking algorithm reduces the search space by effectively not considering time-wise equivalent mappings. The assumptions made about the platform in Chapter 2 ignore inter-core communication timings making the model idealistic, and in my opinion unrealistic in comparison to physical multi-core platforms. The presented symmetry breaking relies on identifying cores with the same computation timing, but ignores communication timing. For instance two identical cores on a NoC can have the same computation timing but different communication timings. For the assumed simple multicore model in Chapter 2, the symmetry breaking technique is a reasonable measure to reduce the search space and a detailed implementation description is provided.

In conclusion, in my opinion the thesis satisfies the high-level goals that it set out to solve. The motivations behind the decisions made are not always clear or even explained at all. The contributed lazy constraints and symmetry breaking techniques are explained in detail. Sufficient implementation details are given that it should be possible to reproduce this work.

Considering the quality of the technical contribution and the writing standard of the thesis itself, I think this work deserves the **grade of C**.

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