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CONTROL STRATEGY OF FIVE-LEVEL FLYING CAPACITOR INVERTER

Doctoral Thesis

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Nomenclature

Abbreviations

AC – alternate current

APOD – alternative phase opposition disposition

D – diode

DC – direct current

DSP – digital signal processor

FCI – flying capacitor inverter

FCMI – flying capacitor multilevel inverter

GTO – gate turn-off (thyristor)

HB – hysteresis band

HV – high voltage

HVDC – high voltage direct current

IGBT – insulated gate bipolar transistor

IGCT – integrated gate commutated thyristor

LV – low voltage

M^2C – modular multilevel converter

MC – multilevel converter

MI – multilevel inverter

MV – medium voltage

PCB – printed circuit board

PD – phase disposition

POD – phase opposition disposition

PP-IGBT – press-pack insulated gate bipolar transistor

p.u. – per unit

PWM – pulse width modulation

R – resistive (load)

RL – resistive-inductive (load)

S – switching cell

SFO PWM – switching frequency optimal pulse width modulation

SSR – solid state relay

SVM – space vector modulation

SV PWM – space vector pulse width modulation

THD – total harmonic distortion

V – switched-off device

WTHD – weighted total harmonic distortion

Symbols

C – capacity

f – frequency

I – electrical current (i – instantaneous value)

j – imaginary unit

L – inductance

M – modulation index

m – number of phases

N – number of voltage levels; set of natural numbers; quantity in general

P – frequency ratio

R – resistance

V – electrical voltage (v – instantaneous value)

X, x – reactance, p.u. reactance

φ – phase shift between fundamental harmonics of voltage and current

ω – angular frequency

Indices

c – carrier

C – capacitor

d – DC (e.g. in the DC link)

F – filter

FC – flying capacitor

G – gate

j – ordinal number of the flying capacitor

L – load

N – net

n – nominal

out – output

p – phase (phase-to-zero)

r – reference

RC – redundant combination

s – switching

SC – switching cell

x – substitutive index (e.g. phases A, B, C or numbers 1, 2, 3 and so)

μ – harmonic order

ν – harmonic order

Abstract

This Thesis deals with the control strategy of five-level flying capacitor inverters. At the beginning, the subject of multilevel inverters is generally discussed. The crucial topologies and their schemes are introduced, their principal functions are described and their use is mentioned.

After the initial state-of-art overview, the flying capacitor multilevel inverter (and particularly the five-level FCI) and its different performances are described in detail. Furthermore, the most important modulation techniques, as well as the voltage balancing of flying capacitors are explained. The core of this Thesis is the analysis of possible switching modes and the verification of their applicability. Afterwards, a simulation model of a three-phase five-level flying capacitor inverter is introduced and the simulation results are presented.

The third chapter discusses the possibility of using the flying capacitor multilevel inverter as an active filter. Several specific requirements are taken into consideration and subsequently analyzed, the simulation model is presented together with the simulation results.

Finally, a laboratory model of the three-phase five-level flying capacitor inverter is introduced and described. At the end, the experimental results are introduced and it is shown that they confirm the correctness of the propounded switching analysis.

Acknowledgements

First and foremost, I would like to express my deepest gratitude to my supervisor, Prof. Ing. Jiří Pavelka, DrSc., for all his support, guidance, advice and numerous opportunities to work on interesting projects he has provided over the years and for his patience and kindness. I feel privileged to have been his student.

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1 Introduction

1.1 Motivation

Converters for electric drives control are going through permanent development. At the early stages electric machines used to be controlled by mechanical converters. The best known and most widespread mechanical converters at that time were the Ward Leonard drive system and later the rotary converters. In 1902 the first electrical converter, a mercury rectifier, was invented and was widely used since the 1920s. It was made obsolete by a semiconductor converter in the 1960s. As the technological progress of semiconductor devices improved, the voltage and current ranges of applications grew rapidly (Rahimo, 2010; Wellemann *et al.*, 2008). Today, four types of semiconductor devices are available for using in medium or high voltage (MV or HV) industrial applications: gate turn-off (GTO) thyristor, integrated gate commutated thyristor (IGCT), insulated gate bipolar transistor in press-pack (PP-IGBT) or in module (IGBT-Module). PP-IGBTs by Westcode and Toshiba reach 4.5 kV / 4.8 kA, Mitsubishi produces GTO thyristors on 6 kV / 6 kA. IGBT-Modules manufactured by ABB reached 6.5 kV / 1.5 kA and 4.5 kV / 2.4 kA, the same devices developed by Infineon and Hitachi are on 3.3 kV / 3 kA and 1.7 kV/ 7.2 kA. IGCTs by ABB exceed the border of 6 kV / 3.2 kA (Rahimo, 2011). In addition, ABB manufactured a prototype of IGCT on 10 kV and 1 kA (Bernet and Sommer, 2010). Unfortunately, the dynamic parameters, above all the switching frequency, do not reach the values of low voltage devices. Nevertheless, it can be generally said that the rapid development in the semiconductor industry produces devices for higher and higher voltage and current area with better and better dynamic properties.

Despite the progress, the parameters of the devices are still not high enough for the use in "classical" three-phase inverters with six power semiconductor devices for the MV or HV applications (Thielemans *et al.*, 2009), e.g. for variable speed drives (the electric traction, winding engines, pumps for long-distance transport of gas and liquid mediums etc.) (Stemmler, 1993; Hammond, 1997) and for compensatory and filtration applications (Fujita *et al.*, 1995). With the growth of non-linear loads such as cycloconverters, rectifiers, arc furnaces and asymmetrical loads, the active power filters are also widely used due to the clearing of high disturbances in the power supply system (Yoshioka *et al.*, 1996; Bollen, 1999; Martins *et al.*, 2011). Classical semiconductor inverters switch on high frequency between the positive and the negative pole and have high conduction losses, relatively. Both, the voltage step between two poles and the higher switching frequency exert influence over the quality of an output voltage waveform. If the required output voltage is higher than the

rate value of power electronic devices available on market then some method of voltage reduction per one device must be used. Lower voltage stress can be achieved by connecting them in series – this method has been widely used for more than 35 years, e.g. in the first light high voltage direct current (HVDC) transmission link between Hellsjön and Grängesberg in 1997 (Eriksson *et al.*, 1998). Input DC voltage of both inverters is ±10 kV, i.e. 20 kV between levels. Output RMS line-to-line voltage of inverter is 10 kV. The distance between stations is 10 km. In each arm there are 22 in series connected IGBTs. The IGBTs were selected according to small deviation of parameters. This selection allows complying a uniform voltage distribution between the transistors. The advantage of this method is simple control strategy; as disadvantages we should mention the above mentioned selection of transistors and the high voltage changes caused by switching of one arm. That is why this method is not practically used. In addition, to connect IGBTs in series is possible only with auxiliary circuits (Baek *et al.*, 2001).

Other, modern solution is to feed the electric drives from multilevel converters (MCs), mostly from multilevel inverters (MIs) that provide the possibility to eliminate series connected semiconductor devices in the MV and HV applications which is considered the main problem.

Using them in these applications resolves not only the problem of voltage equable distribution across semiconductor switches, but it also makes possible to:

- eliminate the need of bulky and expensive step-down transformers,
- reduce the connection cables cross-sections,
- improve the harmonic content of output voltage and phase current consequently thanks to output quantity waveforms; as a result better electromagnetic compatibility is obtained,
- reduce the costs of output filters thanks to lower dv/dt stress of semiconductor switches (the dielectric stress of motor winding insulation which occurs due to reflections inside the cables is reduced),
- operate in applications where semiconductor switches are not able to operate at high switching frequencies.

Of course, the MCs also have several drawbacks. The large number of semiconductor devices ranks among the most obvious drawbacks. With the increasing number of voltage levels, the number of semiconductor devices rises. Besides, more voltage levels require more passive elements; each semiconductor switch needs its own driver, it is necessary to have an

independent galvanic isolated zero potential for each driver etc. The MC turns into a larger and more complex system, especially when it comes to spatial demands, construction, measurement and control.

Some disadvantages and limitations depend on the particular topology of the MC. As Thai (2003) mentions, diode-clamped multilevel topology brings the problem of a DC link voltage unbalance, and consequently of unequal stress across semiconductor devices, H-bridge multilevel topology depends on separated DC sources, and flying (clamping) capacitors topology is limited by the heat capacity of the flying capacitors etc. Even the M^2C topology needs many separate, isolated DC-supplies or battery parts (Marquardt, 2010).

Although MCs can operate with lower switching frequency, there are several applications, e.g. MV or HV active filters or power line conditioners, for which the switching frequency is the limiting parameter.

1.2 Converter Topologies on the Market

From the electric energy conversion point of view we distinguish four basic converter types (Pavelka and Čeřovský, 2002). Rectifiers convert an input AC voltage and current to an output DC voltage and current, choppers convert an input DC voltage and current to an output DC voltage and current of different values, inverters convert an input DC voltage and current to an output AC voltage, current, frequency and count of phases, AC converters convert an input voltage, current, count of phases and frequency to an AC energy with different parameters. The frequency converters that convert an input frequency to an output frequency and that simultaneously maintain the count of phases create a subgroup of AC converters and they are the most wide-spread converters in the field of electrical drives. The basic topologies of converters for electrical drives can be classified as in Fig. 1 (modified Bernet and Sommer, 2010). Nevertheless, it is good to keep in mind that each power electronic converter is composed of power electronic devices that are connected into a particular electric scheme and that are controlled by a particular control strategy.

1.2.1 The Direct Frequency Converter

The direct frequency converters can convert the input AC quantities directly to AC output quantities. In other words, direct frequency converters use only semiconductor devices with no DC link circuit. The most widespread direct frequency converter is called the cycloconverter. The cycloconverters are preferred for their very low speed applications and

for synchronous machine supply. Its disadvantage is that the output frequency must be limited to one-third of the input frequency in order to maintain reasonable power output efficiency.

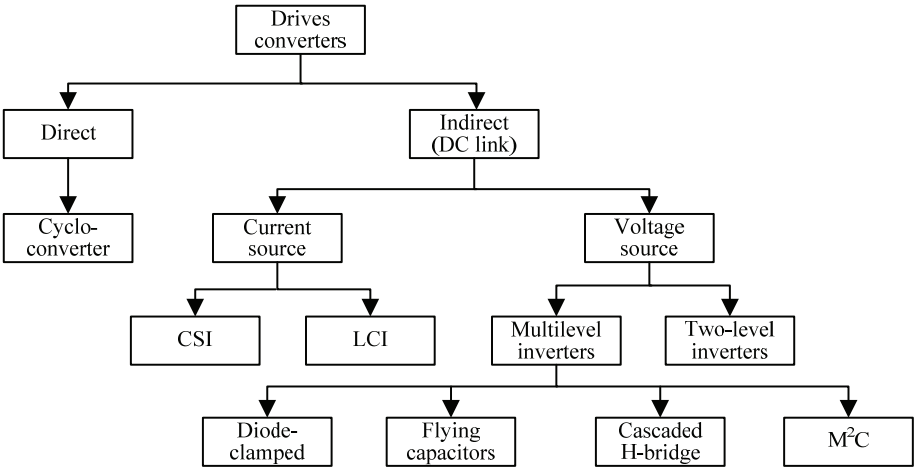


Fig. 1 Classification of drives converter toplogies

Another type of direct frequency converter is the matrix converter. It is a relatively new sort of converter. Crucial advantages of this high dynamic converter lie in a four quadrants operation and a power factor regulation. The control algorithms of this kind of converter are rather complex, that's why the converter control requires very powerful microprocessors.

1.2.2 The Indirect Frequency Converter

This type of the converter consists of a line (input) rectifier, a DC link and a load (output) inverter. There are converters with a current DC link (Fig. 2) and converters with a voltage DC-link (Fig. 3) that are more widely used.

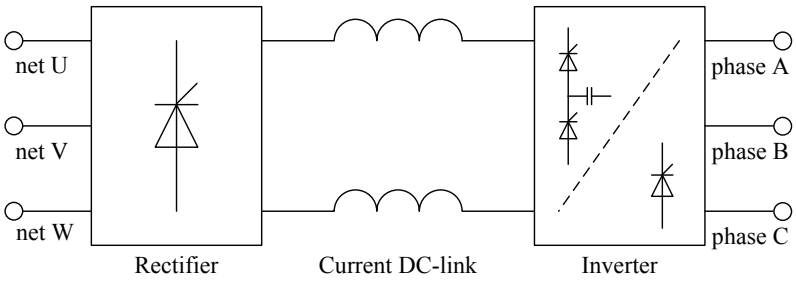


Fig. 2 Frequency converter with a DC link (current source)

An inverter with a current DC link consists of a line controlled rectifier that holds the desired current in the DC link thanks to reactors there and of an inverter. If the inverter is self-

commutated, the whole converter is called a current source inverter (CSI). If we deal with an inverter with outer commutation, the whole converter is called load commutated inverter (LCI) and it is used as a source for synchronous motor medium and high power ratings (1-80 MW) (Morris and Armitage, year unknown). The synchronous motor works in this case as a DC machine and the inverter works as a static commutator.

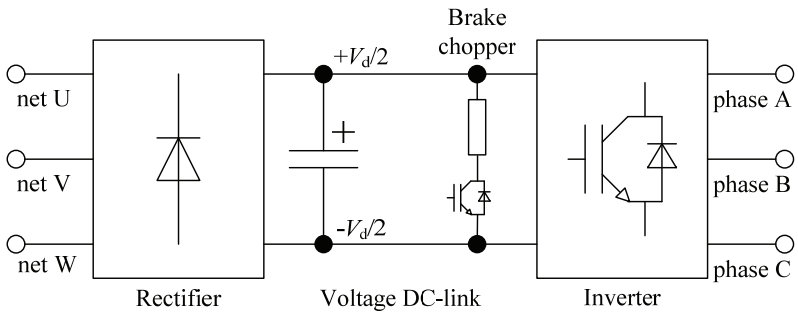


Fig. 3 Frequency converter with a voltage DC link (voltage source)

If a capacitor is placed in the DC link, the DC link maintains a quasi-constant voltage on the input of the inverter and the inverter behaves then like a voltage source. If the input rectifier is of a diode or a thyristor type, the DC link should also contain a simple brake chopper. Neither the diode nor the irreversible thyristor rectifier can return electric energy back to the supply source. When the voltage across the capacitor is raising more than allowed, the excess energy must be burnt up in the resistor.

The diode and thyristor rectifiers combined with the brake chopper have been recently replaced by compatible rectifiers. By using the compatible rectifiers, the operation in a recuperation mode is enabled which means that bidirectional power-flow is feasible.

1.2.3 Two-level Inverter

The simplest scheme of an inverter is the two-level inverter. One phase of this inverter is formed by two series connected switches. A scheme of a three-phase two-level inverter is presented in Fig. 4. Each output phase U, V, W can be connected to one out of the two input DC voltage levels of the V_d, positive ($+V_d$) or negative ($-V_d$). The connection to the positive level is realized by switching-on one of the following devices S_1, resp. S_3, resp. S_5. Similarly, the connection to the negative level is realized by switching-on one of the devices S_4, resp. S_6, resp. S_2.

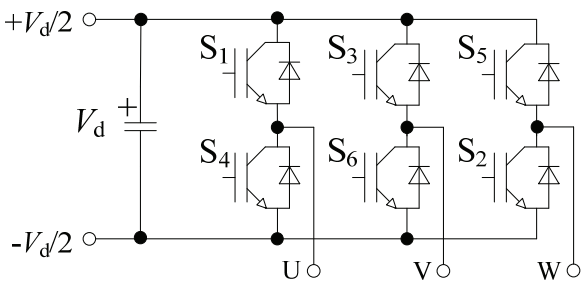


Fig. 4 Basic scheme of a three-phase two-level inverter

The controller must ensure that the devices connected in series, pairs $S_1 + S_4$, $S_3 + S_6$ and $S_5 + S_2$, will never turn on at the same time. If they were switched on simultaneously, it would causes a hard short-circuit of input levels which would damage the devices (Pavelka and Kobrle, 2011).

1.2.4 Multilevel Converters

The essence of the MC is to divide the output phase voltage range (bordered by two levels – upper and lower one) into several inner levels with an equal voltage distance from each other. The magnitude of this distance determines the permitted voltage stress of the semiconductor devices that are used. If this distance gets wider, the voltage stress increases across the first device and decreases across the second one. When this deviation becomes excessively large, the device can be endangered and the core of the MC gets lost. That is why ensuring correct and constant voltage levels is one of the most important control tasks. It is usually called a voltage balancing.

The first and the simplest MCs were not based on the semiconductor technique, but on a magnetic coupling. The waveform of the output multilevel voltage was obtained by adding several rectangle voltages that were produced by classical inverters under square-wave control. Their rectangle phase shifted output voltages supplied the coupling transformers and the voltages summed on the secondary sides of these transformers were added into a staircase multilevel waveform.

1.2.4.1 Cascaded H-bridge Topology

The first MC based on semiconductors was described and constructed by Baker and Bannister (1975). It was a cascaded topology which is a serial connection of one-phase converters. Today, these converters are known as cascaded H-bridge converters.

A basic scheme of a three-phase five-level cascaded H-bridge multilevel inverter is shown in Fig. 5. Each leg is composed of one phase full bridges connected in chain. The bridges are composed of four switches with their free wheel diodes S_1, S_2, S_3, S_4 and of one independent voltage source. As voltage sources batteries, fuel cells or solar cells are usually used. All the voltage sources have an identical voltage. The output voltage of each bridge can obtain values $-V_d$, 0 or $+V_d$. The switching combination of S_1, S_2, S_3, and S_4 determines one out of the following three different operating states:

a) If switches S_2 and S_3 are turned on, the output voltage of the bridge equals $+V_d$. (The source voltage is connected into the circuit with its positive pole to the upper terminal of the bridge.)

b) If switches S_1 and S_4 are turned on, the output voltage of the bridge equals $-V_d$. (The source voltage is connected into the circuit with its negative pole to the upper terminal of the bridge.)

c) If switches S_1 and S_2 or S_3 and S_4 are turned on, the source voltage is disconnected from the circuit and this bridge (with its voltage) does not contribute to the resulted voltage of one arm. Its output voltage equals to 0.

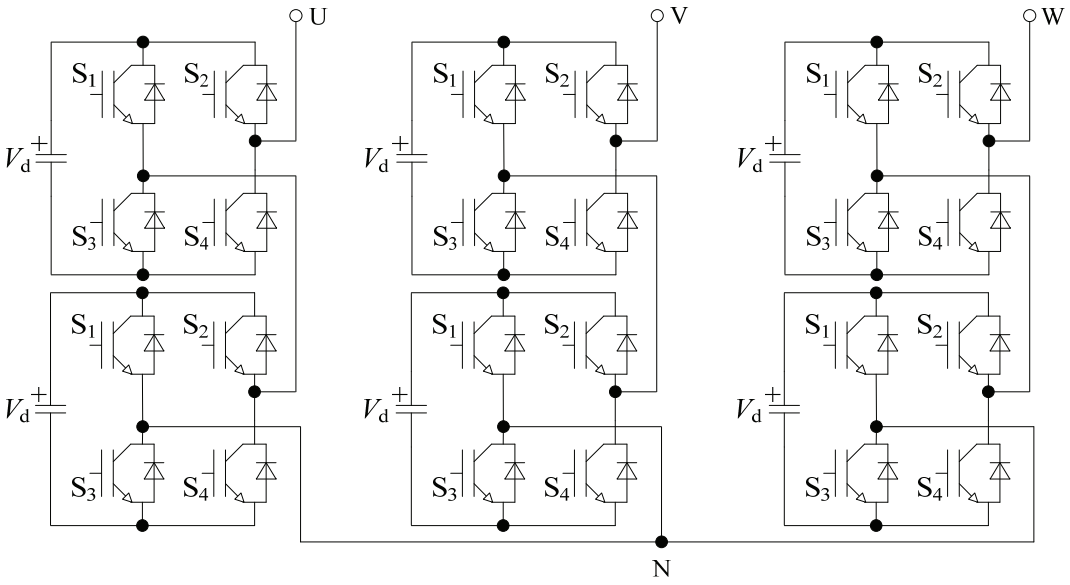


Fig. 5 Basic scheme of a three-phase five-level cascaded H-bridge multilevel inverter

The advantage of this scheme is that all bridges have the same configuration and therefore the possibility of a modular inverter construction arises. This makes the manufacturing cheaper. Thanks to the modularization there is the possibility to easily produce more voltage

levels and to increase the content of the basic harmonic in the output waveform (Pavelka and Kobrle, 2011).

If there are no independent voltage sources, it is necessary to have the same number of galvanic separated voltage sources with individual and isolated power suppliers as depicted in Fig. 6. As a result it requires a special multi-winding transformer - so it is not a transformerless topology any more. This is the biggest disadvantage of the cascaded H-bridge inverter. However, there is a possibility to use capacitors as voltage sources in bridges and to develop a suitable control strategy for the stabilization of capacitor voltages, generally speaking. Another disadvantage is the high number of power electronic devices.

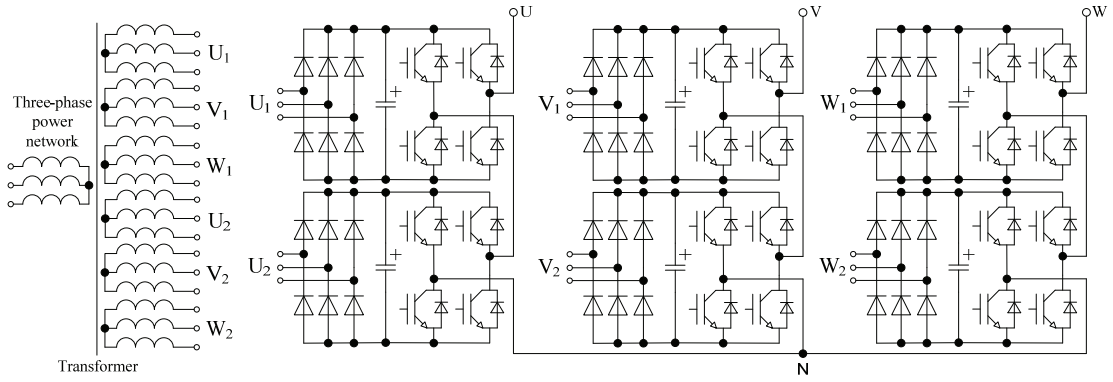


Fig. 6 Scheme of a five-level cascaded H-bridge multilevel inverter with a multi-winding transformer

The cascaded H-bridge converters are nowadays widely used because of their very good harmonic spectrum and because of their relatively easy control. We can find them in applications such as automotive all-electric drives, automotive hybrid drives (Tolbert *et al.*, 2002), power line conditioners (Peng *et al.*, 1997; Tolbert *et al.*, 2000), static var generation (Peng *et al.*, 1996; Peng and Lai, 1997) and compensation (Joos *et al.*, 1997) and converters for renewable energy sources (Tolbert and Peng, 2000).

For illustrative purposes, the contemporary power and voltage values of produced converters are presented. Siemens manufactures this type of inverter (Perfect Harmony) to power 30 MVA at 13.8 kV with IGBTs, ABB in five-level performance to power 24 MVA at 6.9 kV with IGCTs (Beuermann *et al.*, 2006).

1.2.4.2 Diode-clamped Topology

Five years after the description and realization of the first cascaded H-bridge MC, Baker (1980) proposed a new topology – a neutral-point-clamped multilevel inverter, namely a

three-level and a five-level connection. However, just one year later Nabae, Takahashi and Akagi (1981) published an article concerning the implementation of pulse-width modulation for this topology and they introduced their first results of the three-level performance. This topology was the first one that made it possible to produce an output voltage from only one DC source.

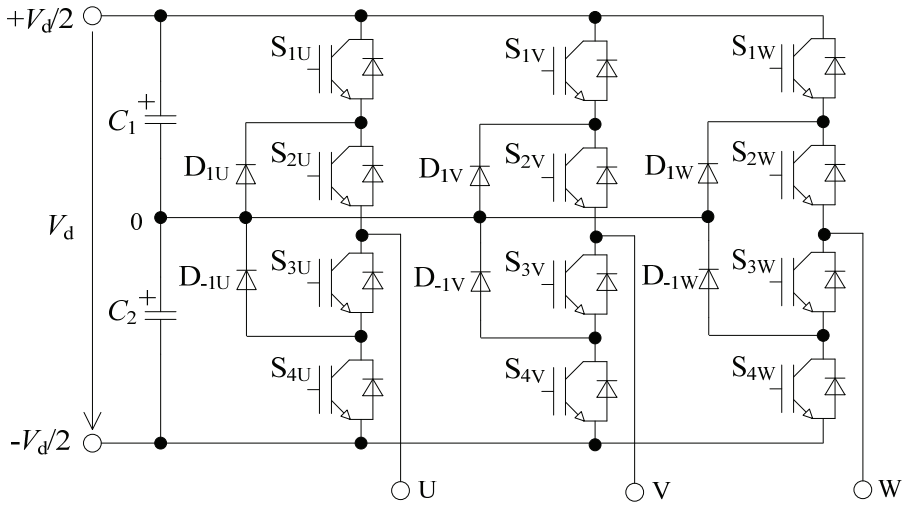


Fig. 7 Basic scheme of a three-phase three-level neutral-point-clamped multilevel inverter

The scheme depicted above shows a three-phase three-level neutral-point-clamped multilevel inverter (Fig. 7). Each phase consists of four switches (S_{xx}) and two diodes (D_{xx}). The voltage across them is determined by the voltage divider that is formed by capacitors (C). The middle point of the DC link (between these two capacitors) is called the neutral point (0) and it is common for all three phases. The voltage dividing is reached with the help of the diodes connected to the neutral point and that is also why this topology is very often called diode-clamped topology.

All switches in one phase are divided into complementary switching pairs: S_{1U} and S_{3U}, S_{2U} and S_{4U}, which means that if one device from the complementary pair turns on, the second one must turn off and vice versa. According to the state of all four switches in one phase, three different values of output phase voltages (e.g. v_{U0}) can be reached on each output terminate: $+V_d/2$, 0 and $-V_d/2$. When e.g. the switches S_{1U} and S_{2U} are turned on, the output phase voltage v_{U0} is $+V_d/2$ and the clamping diode D_{-1U} ensures that the switch S_{3U} blocks the voltage across the capacitor C_1 and S_{4U} blocks the voltage across C_2.

In case there are more levels the situation is similar but not the same. The scheme of a five-level diode-clamped inverter is outlined in Fig. 8. The input DC voltage V_d is divided

across four capacitors C_1, C_2, C_3 and C_4. Each nod of two neighbouring capacitors creates a voltage level, common for all phases. There are five phase voltage levels together in each phase: $+V_d/2$, $+V_d/4$, 0, $-V_d/4$, and $-V_d/2$. Let us discuss only the phase U - the situation in the remaining phases is rather analogous. The switching combination of complementary pairs $S_{1U} + S_{5U}$, $S_{2U} + S_{6U}$, $S_{3U} + S_{7U}$, and $S_{4U} + S_{8U}$ determines one out of the following five different operational states and also the value of the output phase voltage:

a) The switches S_{1U}, S_{2U}, S_{3U} and S_{4U} are turned on. The output voltage v_{U0} is thus equal to $+V_d/2$.

b) The switches S_{2U}, S_{3U}, S_{4U} and S_{5U} are turned on. The output voltage v_{U0} is thus equal to $+V_d/4$.

c) The switches S_{3U}, S_{4U}, S_{5U} and S_{6U} are turned on. The output voltage v_{U0} is thus equal to 0.

d) The switches S_{4U}, S_{5U}, S_{6U} and S_{7U} are turned on. The output voltage v_{U0} is thus equal to $-V_d/4$.

e) The switches S_{5U}, S_{6U}, S_{7U} and S_{8U} are turned on. The output voltage v_{U0} is thus equal to $-V_d/2$.

It is quite clear now that each switch blocks the voltage $V_d/4$. However, the clamping diodes must block different voltages or they must be connected in series as depicted in Fig. 8 when they have the same ratings as the active switches. That is the basic difference between three-level and more-level performance. If all clamping diodes have the same ratings, then their count increases quadratically to the number of levels in one phase (Lai and Peng, 1996).

In industrial applications appear three-, four-, five- and six-level converters. Like the H-bridge MCs, the diode-clamped converters are also used as static var compensators (Hochgraf *et al.*, 1994; Menzies and Zhuang, 1995). This topology is also quite popular in motor drive applications (Tolbert *et al.*, 1998; Tolbert *et al.*, 2002), however only in a three-level performance because diode-clamped converters of more than three levels cannot be stabilized without any auxiliary power circuits (Sivkov, 2011). Lai and Peng (1996) designed a diode-clamped inverter as an interface between HV DC and AC transmission line, Schneider Electric uses this topology for its medium power UPS systems (Rizet, 2010). This topology in a three-level performance was also the base of the first unified power-flow controller in the world (Renz *et al.*, 1998).

To illustrate this, today's power relations are obvious from the following: Siemens manufactures this type of converter to power 28 MVA at 4.16 kV with IGBTs, ABB to power

27 MVA at voltage 3.3 kV with IGCTs, Converteam to 42 MVA at 6.6 kV with PP-IGBTs (Beuermann *et al.*, 2006).

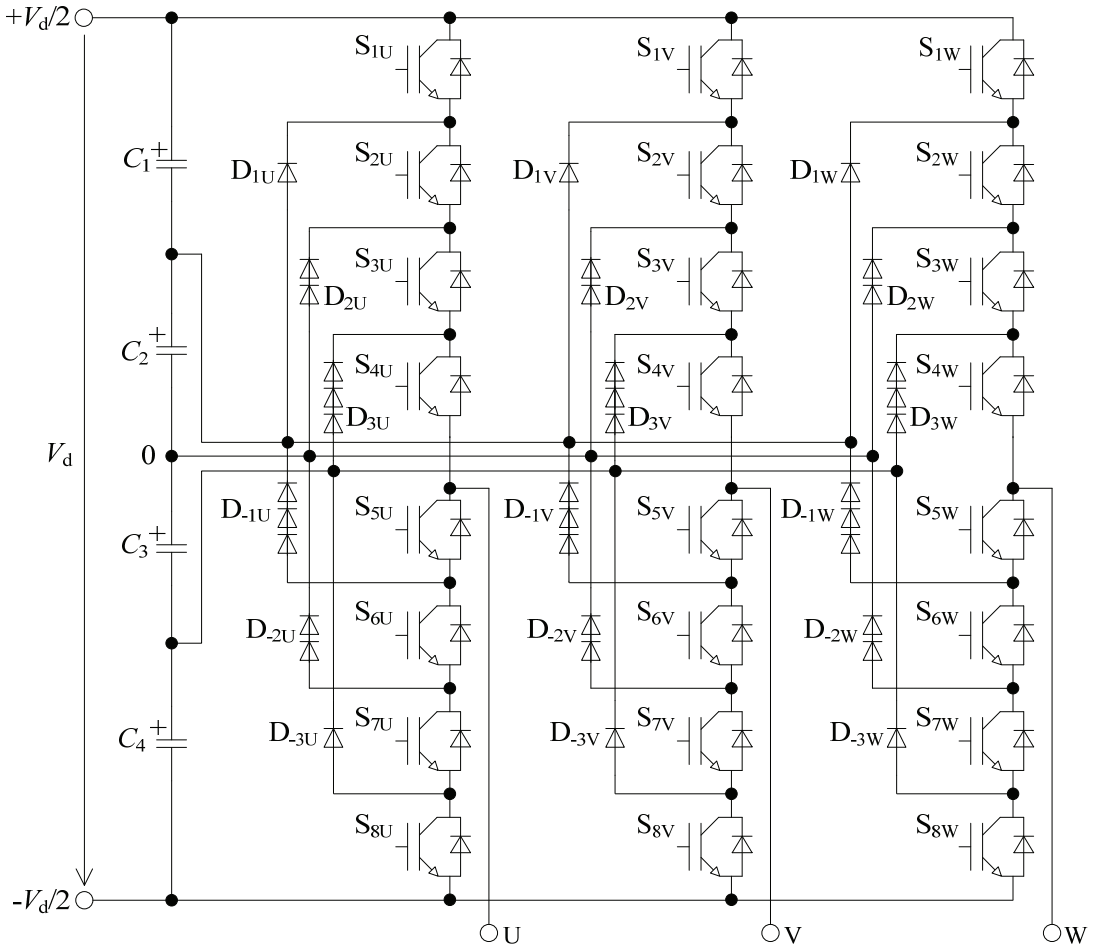


Fig. 8 Basic scheme of a three-phase five-level diode-clamped multilevel inverter

1.2.4.3 Flying Capacitor Topology

During the 1980s the development of the MCs did not move much forward. Only after ten years, at the turn of the decade, finally appeared articles about new applications, e.g. nuclear fusion, and new control methods. The next turning point came at the beginning of the 1990s when Meynard and Foch (1992) presented the flying capacitor converter – as a multilevel chopper and a multilevel inverter.

Just as the output voltage is clamped by diodes in the case of a diode-clamped MI, it is clamped by capacitors in the case of flying capacitor multilevel inverter (FCMI). If related to the earth this capacitor seems to be floating, therefore it is called the flying capacitor

(Dijkhuizen and Duarte, 1998). Furthermore, compared to a diode-clamped converter, the suitable control enables voltage stabilization across the flying capacitors without any auxiliary power circuits thanks to phase redundancies (Sinha and Lipo, 1997).

Nowadays, the four-level flying capacitor inverters of power 8 MVA at 4.2 kV with IGBTs are produced by Converteam (Bernet and Sommer, 2010), at 6 kV with IGCTs and at 10 kV with IGBTs by ČKD Elektrotechnika, a.s.

Because this Thesis deals with exactly this type of topology, a detailed description of it is given in chapter 2.

1.2.4.4 M²C Topology

The last crucial topology appeared just after the turn of the millennium when Lesnicar and Marquardt (2003) presented the modular multilevel converter (M^2C). Its basic scheme is presented in Fig. 9. It looks a little bit like the first H-bridge topology, but the difference is in the use of half bridges instead of full bridges. The half bridges are usually called submodules. The voltage across each submodule must be measured and can therefore be freely controlled.

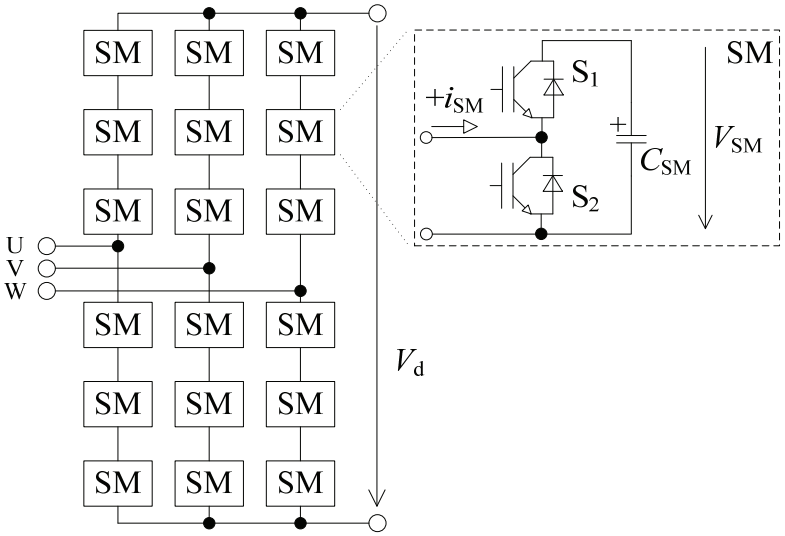


Fig. 9 Basic scheme of a modular multilevel converter (SM = Submodule)

As can be seen in Fig. 9, M^2C is strictly modular and it does not need any additional external components or circuits for a four-quadrant operation of the converter. What is worth noticing is that there is no capacitor in the DC link. This fact rapidly decreases the possibility of a short circuit in the DC link. With respect to the reliability and safety it is very beneficial to replace the damaged submodule during the converter operation without switching it off.

Each submodule can reach two values of its output voltage in four states during the operation:

a) The switch S_1 is turned on, the switch S_2 is turned off and the current i_{SM} is positive. The output voltage of the submodule is then equal to $+V_{SM}$ and the capacitor C_{SM} is charged.

b) The switch S_1 is turned on, the switch S_2 is turned off and the current i_{SM} is negative. The output voltage of the submodule is then equal to $+V_{SM}$ and the capacitor C_{SM} is discharged.

c) The switch S_1 is turned off, the switch S_2 is turned on and the current i_{SM} is positive. The output voltage of the submodule is then equal to 0.

d) The switch S_1 is turned off, the switch S_2 is turned on and the current i_{SM} is negative. The output voltage of the submodule is then equal to 0.

A state with both switches turned-off is not an operating state because the current then cannot flow through the submodule arbitrarily.

Except for the above mentioned advantages, Marquardt (2010) adds the following: there is no need of passive filters on the AC side, there are very low switching losses, the efficiency is high and there is fully dynamic control of both the AC and the DC side. As drawbacks he mentions insufficient maximum temperatures of capacitors with high energy density and bulky capacitors that hamper integration.

Today this converter topology is still in the centre of interest because it is suitable for solar power generation, HVDC transmission, and especially for grid connection of off-shore wind plants (Gambach and Schuster, 2010), power supply of large cities and electric supplies for railway grids (Nee, 2010). Converters of the M^2C topology are employed in the project Skagerrak 4 of the Norwegian and Danish state-owned energy enterprises Statnett and Energinet.dk. This ca 240 km long HVDC Light transmission between Danmark (mainly thermal and wind power-based systems) and Norway (mainly hydroelectric power-based systems) will be of 700 MW power rating; the voltage levels on both AC sides are on 400 kV, on the DC side 500 kV (Statnett, 2013; ABB). It is the first time that the voltage source converter is used at such a high voltage levels as well (Abildgaard, 2012). The project should be finished at the end of 2014 (Statnett, 2013).

1.3 Previous Research on the Department of Electrical Drives and Traction

Multilevel inverters have been researched by the Department of Electric Drives and Traction at our Faculty for a couple of years already. Two dissertation theses regarding multilevel converters were successfully defended.

The first defence took place in 2003 (Thai, 2003). Tran Vinh Thai defended his Thesis entitled *Multilevel Inverters for High Voltage Drives*. His Thesis gives an overview of the three basic topologies and the basic modulation strategies and deals with the problem of voltage balancing in one-phase FCMI. He came to the conclusion that the three-level flying capacitor inverter (FCI) is self-balanced except for the case of pure reactive load. It means that the FCMI operates properly under a modulation strategy without any voltage balancing strategy. However, the deviation of voltage across flying capacitor is relatively high. The more-level FCIs cannot be balanced without a balancing strategy – the voltages of flying capacitors diverge from their rated values and in case of pure reactive load, the FCMI behaves as an undamped resonant LC circuit. Besides, Thai implemented the balancing strategy into the simulation models of one-phase three-, four- and five-level FCIs. The balancing mechanism was turned out to be a stochastic process. Thai attempted to construct a prototype of the one-phase five-level FCI. He designed the power part, measurement and control circuits nevertheless his prototype remained unfinished.

The second defence took place in 2011 (Sivkov, 2011). Oleg Sivkov defended his Thesis entitled *Five-level Inverter with Flying Capacitors*. His Thesis also contains an overview of the three basic topologies. He closely investigates the usage of diode-clamped and flying capacitor MIs. He came to the conclusion that for a more than three-level diode-clamped inverter, the voltage across the DC link capacitors cannot be balanced with just a control strategy. In order to keep it balanced, independent sources or additional circuits are required. The FCMI on the other hand allows stabilization of the voltage across the DC link capacitors for any count of levels without any auxiliary circuits. Furthermore, Sivkov focused on the comparison of capacitor voltage swinging in three-level diode-clamped and flying capacitors MIs. He calculated that a three-level FCI requires a 2–2.4 times larger capacity then a three-level diode-clamped MI in order to get the same capacitor voltage swinging - in the case of a resistive load. In the case of an inductive load, FCMI requires a 5–6 times larger capacity. Finally, he constructed a model of a one-phase five-level FCI according to the Thai's design, he did a couple of measurements and verified that the balancing algorithm, stated in Thai's thesis, is working.

1.4 Objectives

Two defended doctoral theses mentioned in chapter 1.3 serve as a good stepping stone for further research in the field of FCMIs. Therefore, this Thesis is intended to be their logical follow-up.

The first objective of this Thesis is **to summarize the pieces of knowledge about FCMIs and their control strategies**.

The switching process of a MI is patterned on a switching process of a classical two-level inverter. However, theoretically another possibility of switching can be implemented in the case of a MI. Up to now, there have not been published any reason why the switching processes are identical. That is why the second goal is **to analyze and to evaluate the potential switching processes for a five-level FCI**.

The third aim is **to create a functional simulation model of a three-phase five-level FCI** because the voltage stabilization across flying capacitors as well as the analysis can be tested with it.

There were also constructions attempts in both of the previous theses. Therefore, the next objective is **to design and construct a compact laboratory model of a three-phase five-level FCI**. Thai's laboratory model failed to do, Sivkov's one-phase model functioned, but all flying capacitors were clamped to both poles of the DC link by resistors because of their pre-charging and resistors were connected there during the operation of the inverter. In the new three-phase laboratory model the flying capacitors have to be charged without being clamped by resistors.

The best way how to check up the proposition, is to implement it to a real system. Therefore, the fifth objective is **to verify the conclusions drawn from the previous analysis**. It has to be secured that the risky and dangerous operations that the analysis counts with will not damage the real model.

At the beginning of my Ph.D. study there appeared an opportunity to cooperate with the Chinese Beijing Jiaotong University. The name of the common project was *Multilevel Inverter for High Voltage Active Filters*. The Chinese side worked on the task with the cascaded H-bridge MI, the Czech side with the FCMI. I participated in this project with my Ph.D. research. Therefore, **the evaluation of the possibility to use a multilevel inverter as an active filter** is yet another objective of this Thesis.

2 Flying Capacitor Multilevel Inverter

2.1 Principal Function of the Flying Capacitor Inverter

Generally, in the theory of multilevel inverters, the complexity of the power circuit as well as the control increases rapidly with every other addition level. Therefore, the principle function of the flying capacitor inverter (FCI) will be explained on a three-level inverter first. The relationships and natural connections between inverters with different number of levels and the complexity growth will be apparent if three-, four- and five-level inverters will be introduced.

2.1.1 Three-level Flying Capacitor Inverter

As mentioned in chapter 1.2.4.3, the main idea of a flying capacitor multilevel inverter (FCMI) is to create the next voltage level by clamping of a capacitor. The easiest basic power scheme of a FCMI, the one-phase three-level flying capacitor inverter, is depicted in Fig. 10 and it consists of a DC link, which is represented by two identical capacitors C, flying capacitor C_1, four switching semiconductor devices V_1 - V_4 with their anti-parallel diodes D_1 - D_4 and a load Z. The pair V_x + D_x is called a switching cell (S_x). (The labelling V_x for switching semiconductor devices (e.g. IGBT), D_x for diodes and S_x for switching cells is used consistently throughout the whole Thesis.) The nominal value of the DC link voltage is marked as V_d. By a series connection of two identical capacitors C, the virtual zero point (midpoint) is determined. Thus, it can be said that there are three values of the potential in the DC link: $-V_d/2$, 0, $+V_d/2$. The output voltage V_{out} can acquire one of these voltages in every instance. That is why this connection is of a three-level connection. There are four switching devices ordered to the series connection. The positive terminal of the flying capacitor is clamped between the first and the second switching cell, the negative one between the third and the fourth. The middle point of the leg between the second and the third switching cell is the output terminal. The nominal voltage of the flying capacitor V_{C1n} is a half of the nominal voltage in the DC link:

$$V_{C1n} = \frac{V_d}{2} \tag{1}$$

The capacitor C_1 is called the flying capacitor (or sometimes floating capacitor), because the potential of both terminals can change with the potential of the DC link.

As a consequence of the basic functioning of the FCMI there must be two pairs of complementary switching cells in the connection: $S_1 + S_4$ and $S_2 + S_3$. That means that when one cell of a pair is switched on, the second one must be switched off and vice versa. Whereas if both switch cells are switched on, two capacitors that behave as voltage sources are connected in series without any noticeable resistance and the equalizing current flows through the circuit. It has the character of a short-circuit current. The devices switch together in a switching pair as in the case of a standard two-level inverter. Therefore, there are $2^2 = 4$ possible switching states in the steady state, as seen in Table 1.

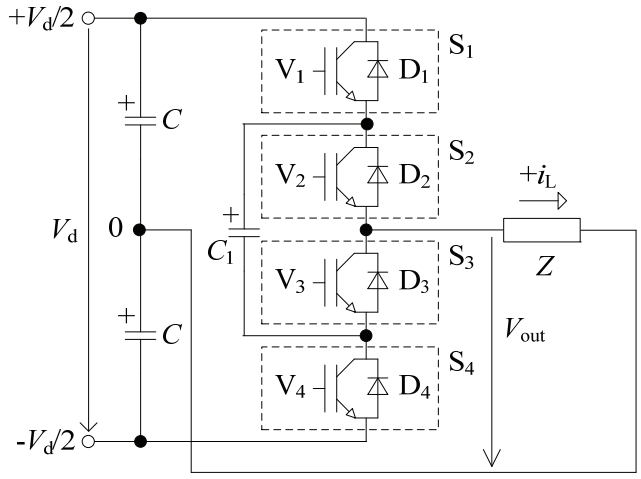


Fig. 10 Basic scheme of a one-phase three-level flying capacitor multilevel inverter

Table 1 Switching states of a three-level FCI (positive load current)
(0 = device is turned off, 1 = device is turned on)

Switching state	**S_1**	**S_2**	**S_3**	**S_4**	**V_{out}**
1	0	0	1	1	$-V_d/2$
2	1	0	1	0	0
3	0	1	0	1	0
4	1	1	0	0	$+V_d/2$

If the switching cells S_1 and S_2 are turned off, S_3 and S_4 have to be turned on and the load is connected between 0 and $-V_d/2$. If S_1 and S_2 are turned on, cells S_3 and S_4 have to be turned off and the load is connected between 0 and $+V_d/2$. When S_1 and S_3 are turned on and S_2 and S_4 are turned off, the voltage across the load is zero. That follows from Kirchhoff's loop rule according to an equivalent circuit in Fig. 11:

$$V_{C1} + V_{out} - V_C = 0 \tag{2}$$

If both capacitors C and C_1 are charged on the value $+V_d/2$ then the following parity is valid:

$$V_{out} = \frac{V_d}{2} - \frac{V_d}{2} = 0 \tag{3}$$

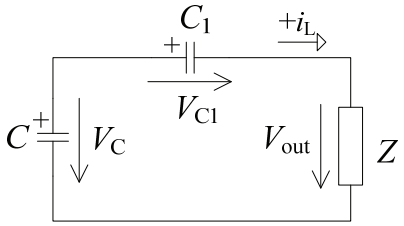


Fig. 11 An equivalent circuit for switching state 2

This is true only when the voltage across all capacitors is held at the nominal value of the capacitors by an additional auxiliary power circuit because the flowing current charges and discharges all the capacitors. It depends on its actual direction.

Under the same conditions, the situation is similar when S_2 and S_4 are turned on and S_1 and S_3 are turned off. Then, the voltage across the load is also zero. Again, it follows from the Kirchhoff's loop rule according to an equivalent circuit in Fig. 12:

$$V_C - V_{C1} + V_{out} = 0 \tag{4}$$

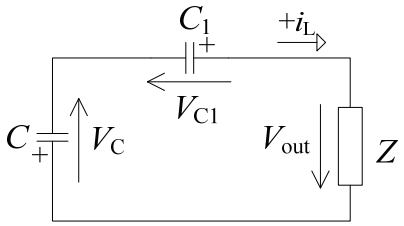


Fig. 12 An equivalent circuit for switching state 3

If both capacitors C and C_1 are charged on the value $+V_d/2$, then also in this case the equation (3) is valid. The load voltage is the same in states 2 and 3. States producing the same

voltage level are called redundant states. Possible redundancies are often used to an advantage in the control strategies (see chapter 2.3).

A switched-off device V_x with its free-wheel diode D_x acts in a turned off state as an electrical contact and allows the current to flow in both directions. If this current $i(t)$ flows through a capacitor with the capacity C_x then the change of the capacitor voltage V_{Cx} is given by the equation:

$$v_{Cx}(t) = V_{Cx}(0) + \frac{1}{C_x}\int_0^{t_x} i(t)\mathrm{d}t = V_{Cx}(0) + \Delta v_{Cx}(t) \qquad (5)$$

where $v_{Cx}(t)$ is an instantaneous value of the capacitor voltage at the time t,

$V_{Cx}(0)$ is an initial voltage across the capacitor at the time $t = 0$,

C_x is the capacity of a relevant capacitor,

$i(t)$ is an instantaneous value of the current at the time t,

$\Delta v_{Cx}(t)$ is an instantaneous value of the voltage change across the capacitor at the time t,

$\int_0^{t_x} i(t)\mathrm{d}t$ is a charge $Q(t)$ that passed through the capacitor with the capacity C_x during the time interval $\langle 0; t_x \rangle$.

The equation (5) shows that:

- the voltage $v_{Cx}(t)$ increases or decreases according to the polarity of the current $i(t)$,
- the quantity of the voltage change $\Delta v_{Cx}(t)$ across the capacitor is directly proportional to the integral of the current $i(t)$ in a time interval $\langle 0; t_x \rangle$, i.e. directly proportional to the charge $Q(t)$ flowing through the capacitor,
- the quantity of voltage change $\Delta v_{Cx}(t)$ across the capacitor is indirectly proportional to the quantity of the capacity C_x,

- the quantity of voltage change $\Delta v_{\mathrm{Cx}}(t)$ across the flying capacitor is independent on the initial value of the voltage $V_{\mathrm{Cx}}(0)$.

The three-phase connection of the three-level FCI contains three times more semiconductor devices and flying capacitors than the one-phase three-level FCI - its scheme is depicted in Fig. 13. Because the load can either be in a star or a delta connection, no midpoint (virtual zero point) in the DC link is physically needed. The principle function is the same as in the one-phase version and, as is apparent from Fig. 13, each phase (or leg, as it is sometimes called) can be controlled separately, independent of the other legs. This is the main advantage compared with the diode-clamped multilevel inverter. All three flying capacitors have the same nominal value of voltage:

$$V_{\mathrm{C1An}} = V_{\mathrm{C1Bn}} = V_{\mathrm{C1Cn}} = \frac{V_{\mathrm{d}}}{2} \tag{6}$$

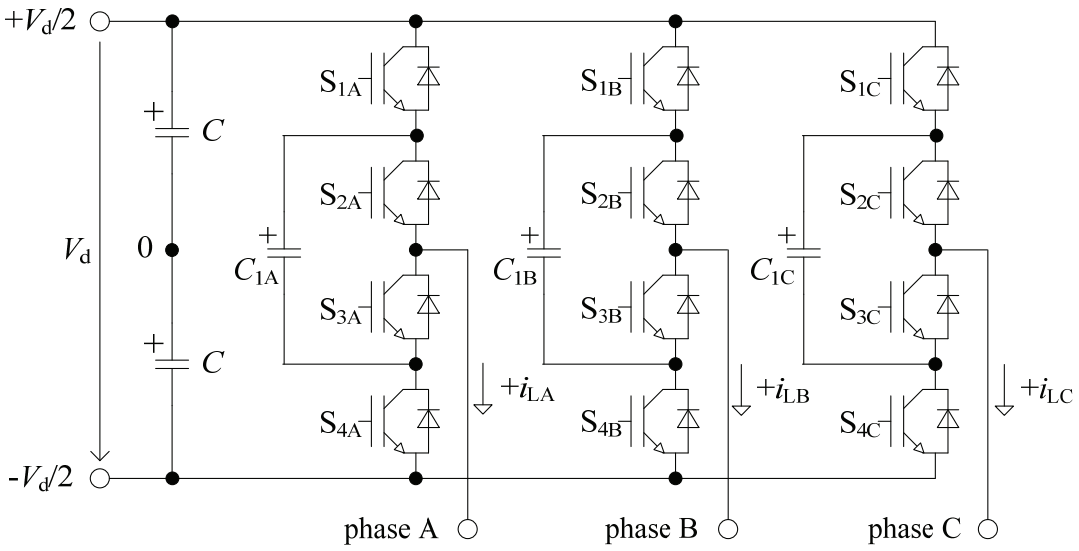


Fig. 13 Basic scheme of a three-phase three-level flying capacitor multilevel inverter

2.1.2 Four-level Flying Capacitor Inverter

To form the four-level FCI means to obtain four voltage levels between the output terminal of a converter and the DC link midpoint, specifically $-V_{\mathrm{d}}/2$, $-V_{\mathrm{d}}/6$, $+V_{\mathrm{d}}/6$, $+V_{\mathrm{d}}/2$. It will be achieved by adding two more switched-off devices (switching cells) and one more flying

capacitor to each phase of the inverter. The power scheme of the one-phase performance can be seen in Fig. 14.

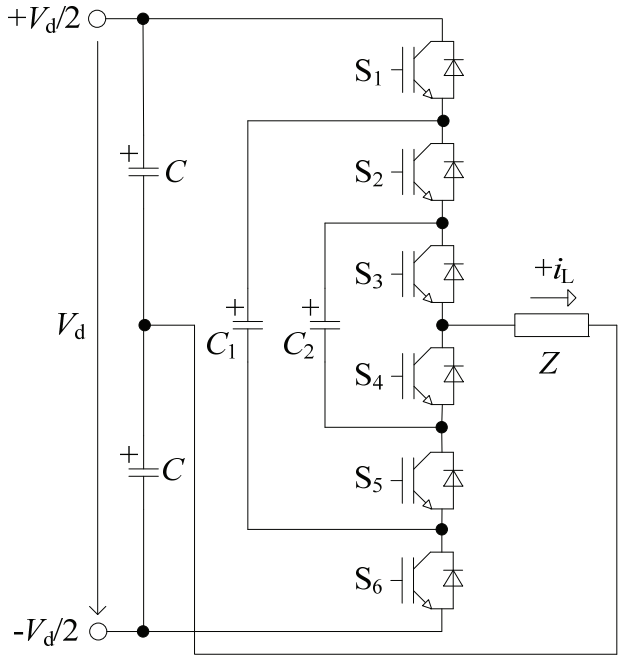


Fig. 14 Basic scheme of one-phase four-level flying capacitor multilevel inverter

The positive terminal of the flying capacitor C_1 is clamped between the first and the second switching cell, the negative one between the fifth and the sixth. Similarly, the positive terminal of the flying capacitor C_2 is clamped between the second and the third switching cell, its negative terminal between the fourth and the fifth. The middle point of the leg between the third and the fourth switching cell is the output terminal. Nominal voltages of the flying capacitors V_{C1n} and V_{C2n} are:

$$V_{C1n} = \frac{2}{3} V_d \tag{7}$$

$$V_{C2n} = \frac{V_d}{3} \tag{8}$$

A zero voltage cannot be directly reached on the output of the four-level FCI while it is operating, because the even number of voltage levels divides the range of the input (DC link)

voltage into an odd count of voltage bands and the zero voltage level lies in the middle of the middle band.

Six switching cells make it possible to operate in $2^3 = 8$ switching states. Their overview is summed up in Table 2. It is worth noticing that each middle level can be reached by three different manners of switching. The redundancy is higher than in case of a three-level inverter and all redundant switching states can be used in the control strategy.

Table 2 Switching states of a four-level FCI (positive load current) (0 = device is turned off, 1 = device is turned on)

Switching state	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**V_{out}**
1	0	0	0	1	1	1	$-V_d/2$
2	1	0	0	1	1	0	$-V_d/6$
3	0	1	0	1	0	1	$-V_d/6$
4	0	0	1	0	1	1	$-V_d/6$
5	1	1	0	1	0	0	$+V_d/6$
6	0	1	1	0	0	1	$+V_d/6$
7	1	0	1	0	1	0	$+V_d/6$
8	1	1	1	0	0	0	$+V_d/2$

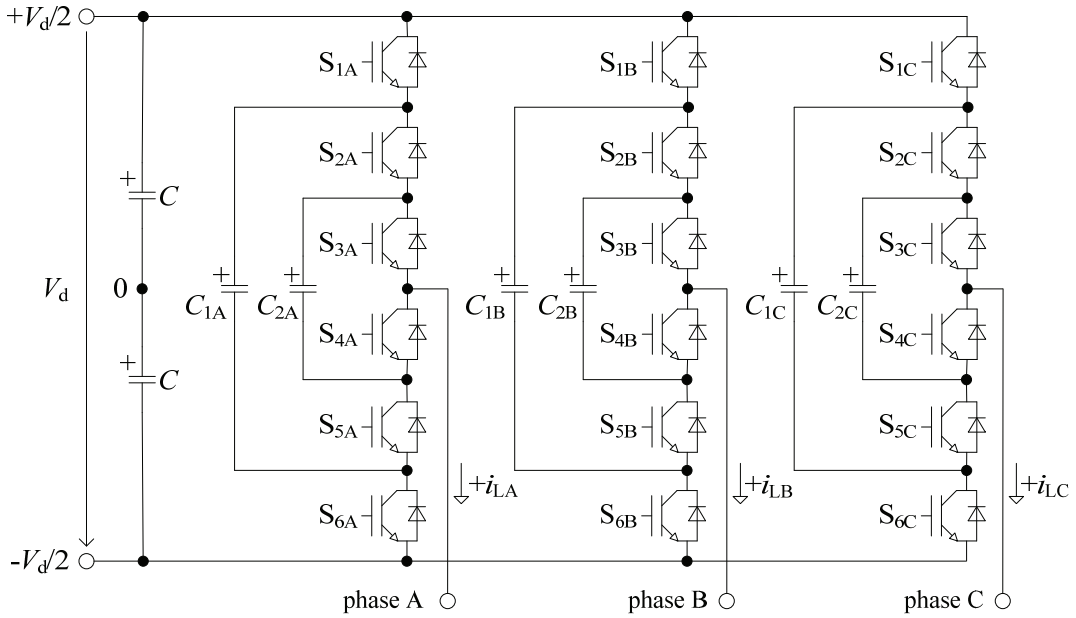


Fig. 15 Basic scheme of a three-phase four-level flying capacitor multilevel inverter

The three-phase performance is depicted in Fig. 15. Similarly as in the case of the three-phase connection of the three-level FCI, the three-phase four-level FCI contains three times more semiconductor devices and flying capacitors than the one-phase four-level FCI and no virtual zero point in the DC link is physically needed. Also the principle functioning is the same as in the one-phase performance and each phase is controlled separately. All matching flying capacitors have the same nominal values of voltage:

$$V_{\mathrm{C1An}} = V_{\mathrm{C1Bn}} = V_{\mathrm{C1Cn}} = \frac{2}{3} V_{\mathrm{d}} \tag{9}$$

$$V_{\mathrm{C2An}} = V_{\mathrm{C2Bn}} = V_{\mathrm{C2Cn}} = \frac{V_{\mathrm{d}}}{3} \tag{10}$$

2.1.3 Five-level Flying Capacitor Inverter

When one complementary switching pair and one more flying capacitor are added into the leg of a four-level performance, a five-level FCI is created. The positive pole of the flying capacitor C_1 is clamped between the first and second switching cell, the negative one between the seventh and the eight one. Likewise, the positive terminal of the second flying capacitor C_2 is clamped between the second and the third switching cell, its negative terminal between the sixth and the seventh one. The positive pole of the last flying capacitor C_3 creates a knot with the third and the fourth switching cell, the negative pole with the fifth and the sixth one. The middle point of the leg between the fourth and fifth switching cell creates the output terminal.

A one-phase scheme of a five-level FCI is pictured in Fig. 16. The clamped flying capacitors help to generate voltage levels $-V_{\mathrm{d}}/2$, $-V_{\mathrm{d}}/4$, 0, $+V_{\mathrm{d}}/4$ and $+V_{\mathrm{d}}/2$ between the phase terminal and the virtual zero point if they are charged to their nominal values of voltage:

$$V_{\mathrm{C1n}} = \frac{3}{4} V_{\mathrm{d}} \tag{11}$$

$$V_{\mathrm{C2n}} = \frac{V_{\mathrm{d}}}{2} \tag{12}$$

$$V_{C3n} = \frac{V_d}{4} \tag{13}$$

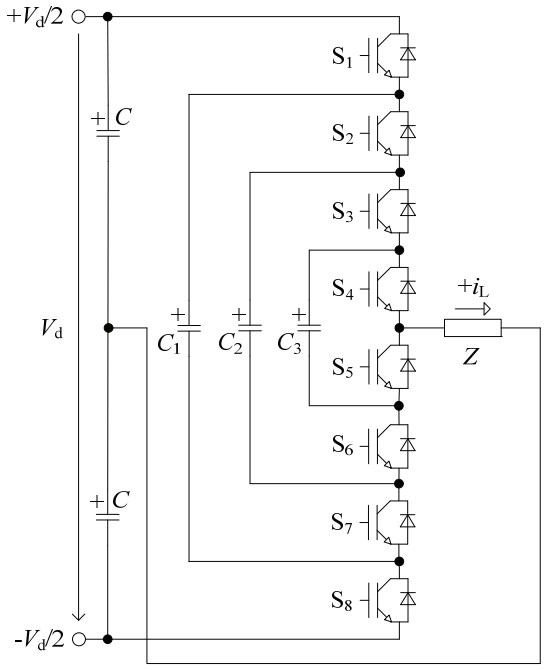


Fig. 16 Basic scheme of a one-phase five-level flying capacitor multilevel inverter

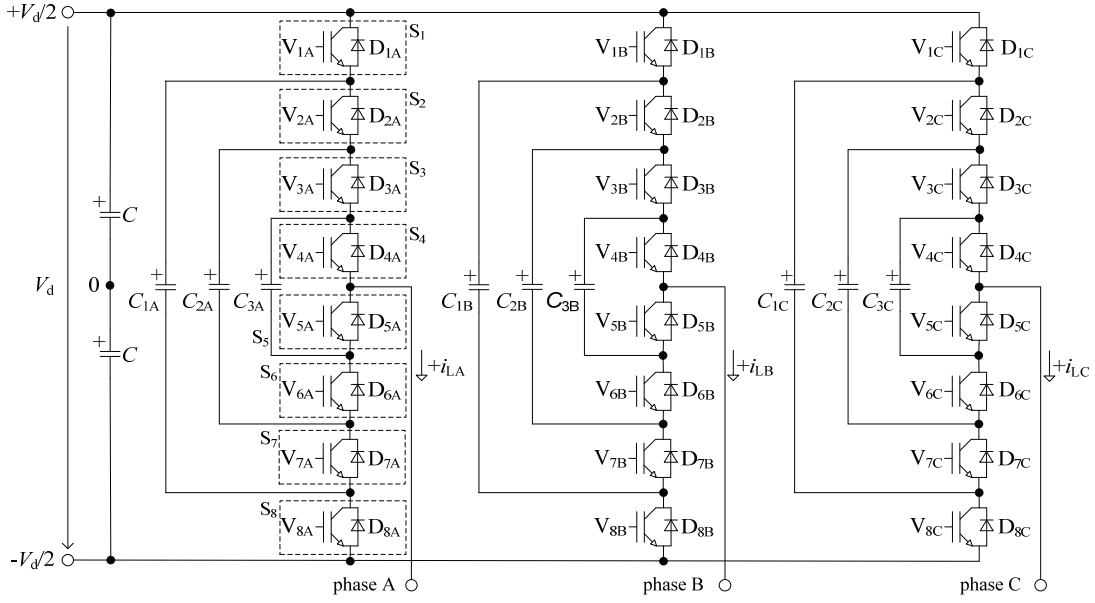


Fig. 17 Basic scheme of a three-phase five-level flying capacitor multilevel inverter

Four pairs of switching cells make it possible to operate in $2^4 = 16$ switching states. All relevant possibilities are mentioned in Table 2. It is apparent that the number of redundant states is higher again than in the previous performances. It is the odd-level FCI that causes that a zero voltage level is produced.

The three-phase connection contains already more than twenty IGBTs as seen from Fig. 17. It operates analogically to the three- and four-level FCI. The nominal values of the matching flying capacitors are given by the equations (14) - (16).

Table 3 Switching states of a five-level FCI (positive load current) (0 = device is turned off, 1 = device is turned on)

Switching state	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**V_{out}**
1	0	0	0	0	1	1	1	1	$-V_d/2$
2	1	0	0	0	1	1	1	0	$-V_d/4$
3	0	1	0	0	1	1	0	1	$-V_d/4$
4	0	0	1	0	1	0	1	1	$-V_d/4$
5	0	0	0	1	0	1	1	1	$-V_d/4$
6	1	1	0	0	1	1	0	0	0
7	0	1	1	0	1	0	0	1	0
8	0	0	1	1	0	0	1	1	0
9	1	0	1	0	1	0	1	0	0
10	0	1	0	1	0	1	0	1	0
11	1	0	0	1	0	1	1	0	0
12	1	1	1	0	1	0	0	0	$+V_d/4$
13	1	1	0	1	0	1	0	0	$+V_d/4$
14	1	0	1	1	0	0	1	0	$+V_d/4$
15	0	1	1	1	0	0	0	1	$+V_d/4$
16	1	1	1	1	0	0	0	0	$+V_d/2$

$$V_{C1An} = V_{C1Bn} = V_{C1Cn} = \frac{3}{4}V_d \tag{14}$$

$$V_{C2An} = V_{C2Bn} = V_{C2Cn} = \frac{V_d}{2} \tag{15}$$

$$V_{\mathrm{C3An}} = V_{\mathrm{C3Bn}} = V_{\mathrm{C3Cn}} = \frac{V_{\mathrm{d}}}{4} \tag{16}$$

2.1.4 More-level Flying Capacitor Inverters

By adding more flying capacitors and switching cells, the number of voltage levels increases and the distances between them decreases. This decreasing of distance is the main source of advantages mentioned in chapter 1.1. However, both the number of voltage levels and the number of switching combinations increase simultaneously. Then the following can be stated about an *N*-level connection of an *m*-phase FCI:

$$N_{\mathrm{FCm}} = m\left(N-2\right) \tag{17}$$

$$N_{\mathrm{IGBTm}} = 2m\left(N-1\right) \tag{18}$$

$$N_{\mathrm{SC}} = 2^{(N-1)} \tag{19}$$

$$N_{\mathrm{RC}} = N_{\mathrm{SC}} - N \tag{20}$$

where N_{FCm} represents the number of flying capacitors in *m* phases, N_{IGBTm} represents the number of switching cells in *m* phases, N_{SC} gives the number of switching combinations and N_{RC} the number of redundant combinations. For illustration, the rapid growth of switching combinations (and hence the complexity) as well as the growth of power devices (and hence the space and cost demands) of a three-phase FCIs is outlined in Fig. 18.

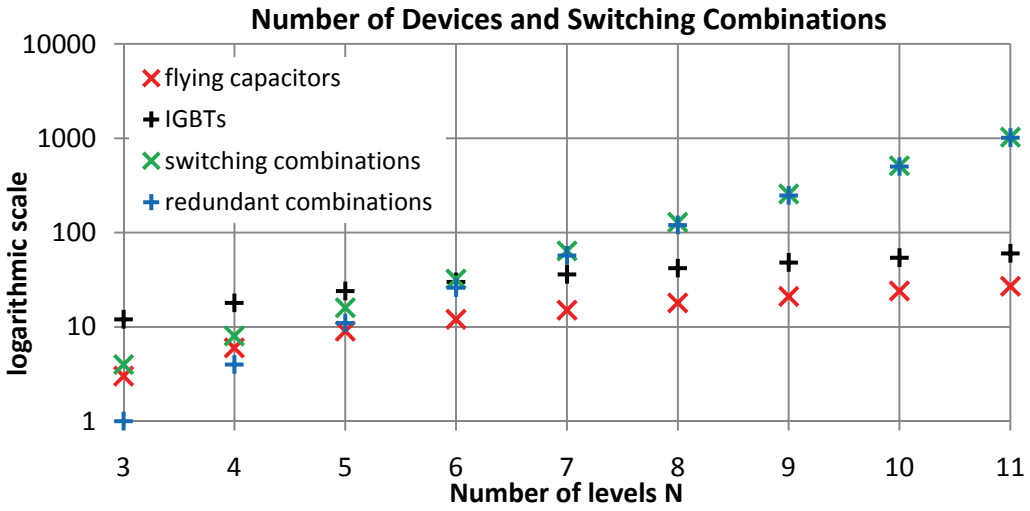


Fig. 18 Illustration of a three-phase FCI copmlexity in relation to the increasing number of levels

The nominal voltage values of flying capacitors can be counted according to the following formula (Pavelka and Kobrle, 2011):

$$\begin{pmatrix} \frac{N_{FC1}-1+1}{N-1} & 0 & \cdots & 0 \\ 0 & \frac{N_{FC1}-2+1}{N-1} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{N_{FC1}-j+1}{N-1} \end{pmatrix} \begin{pmatrix} V_d \\ V_d \\ \vdots \\ V_d \end{pmatrix} = \begin{pmatrix} V_{C1n} \\ V_{C2n} \\ \vdots \\ V_{CFCn} \end{pmatrix} \tag{21}$$

where j is the ordinal number of the flying capacitor; the dimension of the first, regular matrix is $N \times N$.

For comparison, the nominal voltages of flying capacitors are listed in Table 4. The main conclusion drawn from this table is that with growing number of voltage levels the requested nominal voltage of the flying capacitors also increases.

Fig. 18 and Table 4 clearly show that FCI is a convenient topology only if you create seven levels or less (Bernet and Sommer, 2010). Nowadays, the M^2C topology is used for applications where several hundred of voltage levels are required (Jacobsson *et al.*, 2010).

Table 4 Nominal voltages of flying capacitors

N	3	4	5	6	7	8	9	10	11
N_{FC}	1	2	3	4	5	6	7	8	9
V_{C1}	0.5 V_d	0.67 V_d	0.75 V_d	0.8 V_d	0.83 V_d	0.86 V_d	0.88 V_d	0.89 V_d	0.9 V_d
V_{C2}	-	0.33 V_d	0.50 V_d	0.6 V_d	0.67 V_d	0.71 V_d	0.75 V_d	0.78 V_d	0.8 V_d
V_{C3}	-	-	0.25 V_d	0.4 V_d	0.50 V_d	0.57 V_d	0.63 V_d	0.67 V_d	0.7 V_d
V_{C4}	-	-	-	0.2 V_d	0.33 V_d	0.43 V_d	0.50 V_d	0.56 V_d	0.6 V_d
V_{C5}	-	-	-	-	0.17 V_d	0.29 V_d	0.38 V_d	0.44 V_d	0.5 V_d
V_{C6}	-	-	-	-	-	0.14 V_d	0.25 V_d	0.33 V_d	0.4 V_d
V_{C7}	-	-	-	-	-	-	0.13 V_d	0.22 V_d	0.3 V_d
V_{C8}	-	-	-	-	-	-	-	0.11 V_d	0.2 V_d
V_{C9}	-	-	-	-	-	-	-	-	0.1 V_d

2.2 Modulation Techniques Used for the Flying Capacitor Inverter

Nowadays, practically all multilevel converters operate in switch mode (Thai, 2003). That means that the semiconductor switched-off device is either turned off or turned on with a little voltage drop across it. This process of switching the electronic devices on and off is called modulation and the international research has been developing optimum strategies to implement it for more than 40 years (Holmes and Lipo, 2003). The control pulses for the devices arise in the modulator and they are produced quickly enough that the capacitors and inductors can filter or average this alternated signal.

There are many particular modulation techniques suitable for various types of inverters and their mutual comparison can be carried out from several points of view, e.g. the switching losses, distortion and harmonic generation, complexity of algorithms or speed of response.

Very often the quality of modulation technique is determined by the total harmonic distortion (THD) and the weighted total harmonic distortion (WTHD). The factor THD expresses the content of harmonics in the waveform and it can be mathematically written as:

$$\mathrm{THD} = \sqrt{\sum_{\nu=2,3,\ldots}^{\infty} \left(\frac{V_\nu}{V_1} \right)^2} \tag{22}$$

where V_ν, V_1 are the RMS values of the monitored quantities and ν is the harmonic order.

The factor WTHD expresses the normalized weighted THD, mathematically written as:

$$\mathrm{WTHD} = \frac{\sqrt{\sum_{\nu=2,3,\ldots}^{\infty} \left(\frac{V_\nu}{\nu}\right)^2}}{V_1} \tag{23}$$

The modulation techniques for the MIs evolved from the modulation techniques of classical two-level inverters (Hussein, 2009). The most widely utilized modulation is the pulse width modulation (PWM) for controlling of voltage source inverters (Holmes and Lipo, 2003). Another popular modulation technique is the hysteresis modulation for control of the current output of voltage source inverters (Shukla, 2011). PWM is the technique which changes the switch-on/switch-off ratio (duty cycle) of the inverter switches at a high switching frequency in order to achieve the desired average low frequency voltage or current output. The classification of PWM techniques is not unified; even in the field of two-level inverters. The authors sometimes contradict each other (Tolbert and Habetler, 1998; Holmes and Lipo, 2003; Thai, 2003; Bandaru and D Rayudu, 2011; Rodríguez *et al.*, 2002; and others). Anyway, it can be generally said that the PWM techniques for multilevel inverters can be divided into three main groups:

- Programmed PWM
- Carrier-based PWM
- Space vector PWM

2.2.1 Programmed Pulse Width Modulation

This modulation technique falls into the category of the so called off-line modulations. It means that the moments of turning-on and turning-off are calculated in advance and they are based on a specific criterion which is typically the minimization of system losses. The result of the calculation is thus a set of switching instants. Every properly computed switching instant of this set can reduce or cancel the desired value of harmonic. According to this computation, there are two useful criteria that gave the names to the two modulation techniques: Harmonic elimination PWM and Minimum harmonic distortion PWM.

Holmes and Lipo (2003) claim that the programmed PWM shows very good values of WTHD. However, they admit that this modulation appears to be practical only when the output voltage range is relatively small. Hence it is appropriate for UPS applications. In

addition, the programmed PWM is usually employed with H-bridge MIs (Zhong *et al.*, 2004). Should the output voltage amplitude of a MC be wider and the dynamic faster, some other PWM technique has to be used. Because of these reasons, this modulation technique will not be described in more detail.

2.2.2 Carrier-based Pulse Width Modulation

The carrier-based PWM is the most widespread modulation of classical two-level inverters because of the simplicity of its implementation (Tolbert and Habetler, 1998). The characteristic feature of the carrier-based modulation is the comparison of two waveforms – a reference and a carrier waveform. Reference signal is the desired low-frequency waveform, usually a sine wave; carrier signal is the high-frequency waveform, ordinarily of sawtooth or triangle shape (see chapter 2.2.2.2). The output terminal with the resulting signal is connected either to the upper positive DC terminal when the reference waveform is larger than the triangle carrier waveform, or to the lower negative DC terminal when the reference waveform is smaller than the triangle carrier waveform.

The same thing – when it comes to the widening and simplicity of the carrier-based PWM – is also true for the MIs. At the beginning of the 1990s a categorization of all the modulation possibilities for MIs was published in (Carrara *et al.*, 1992) and it is considered, together with (Carrara *et al.*, 1993), as the fundamental work concerning modulation of multilevel inverters. Chapter 2.2.2.3 deals with it in more detail.

2.2.2.1 General Mathematical Expression of Switched Pattern

The main monitored feature of the PWM is the content of harmonic components. It can be solved either by the Fourier analysis of the switched signal or analytically. In the following text, the analytical determination will be described because it gives a clear imagine of the essence of carrier-based PWM. The analytical method was first described by Bowes and Bird (1975).

It is well known that each periodic function $f(\omega t)$ of a variable can be composed of an infinite set of sine and cosine functions – the Fourier series (e.g. Vancl and Čuřík, 1921):

$$f(\omega t) = \frac{a_0}{2} + \sum_{\nu=1}^{\infty} \left(a_\nu \cos \nu\omega t + b_\nu \sin \nu\omega t \right) \tag{24}$$

where ν is the harmonic order and

$$a_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} f(\omega t)\mathrm{d}\omega t;\ \nu = 0,1,...\infty \tag{25}$$

$$a_\nu = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\omega t)\cos\nu\omega t\mathrm{d}\omega t;\ \nu = 0,1,...\infty \tag{26}$$

$$b_\nu = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\omega t)\sin\nu\omega t\mathrm{d}\omega t;\ \nu = 1,2,...\infty \tag{27}$$

The PWM switched signal consists of a periodic function of two variables with different angular frequencies and phase shifts $f(w(t),z(t))$ where:

$$w(t) = \omega_c t + \theta_c \tag{28}$$

$$z(t) = \omega_r t + \theta_r \tag{29}$$

where ω_c is the angular frequency of a carrier waveform and θ_c is its phase shift, ω_r is the angular frequency of a reference waveform (fundamental angular frequency) and θ_r is its phase shift.

Bowes (1975) showed that even a function of two variables can be composed by the Fourier series:

$$\begin{aligned} f(w,z) = \frac{a_{00}}{2} + \sum_{\nu=1}^{\infty}\left(a_{0\nu}\cos\nu z + b_{0\nu}\sin\nu z\right) + \sum_{\mu=1}^{\infty}\left(a_{\mu 0}\cos\mu w + b_{\mu 0}\sin\mu w\right) + \\ + \sum_{\mu=1}^{\infty}\sum_{\substack{\nu=-\infty \\ (\nu\neq 0)}}^{\infty}\left[a_{\mu\nu}\cos(\mu w+\nu z) + b_{\mu\nu}\sin(\mu w+\nu z)\right] \end{aligned} \tag{30}$$

where

$$a_{\mu\nu} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(w,z) \cos(\mu w + \nu z) \, \mathrm{d}w \, \mathrm{d}z \tag{31}$$

$$b_{\mu\nu} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(w,z) \sin(\mu w + \nu z) \, \mathrm{d}w \, \mathrm{d}z \tag{32}$$

After the substitution from equations (28) and (29) to (30), it yields:

$$\begin{aligned} f(t) = \frac{a_{00}}{2} &+ \sum_{\nu=1}^{\infty} \left[a_{0\nu} \cos(\nu\omega_{\mathrm{r}} t + \nu\theta_{\mathrm{r}}) + b_{0\nu} \sin(\nu\omega_{\mathrm{r}} t + \nu\theta_{\mathrm{r}}) \right] + \\ &+ \sum_{\mu=1}^{\infty} \left[a_{\mu 0} \cos(\mu\omega_{\mathrm{c}} t + \mu\theta_{\mathrm{c}}) + b_{\mu 0} \sin(\mu\omega_{\mathrm{c}} t + \mu\theta_{\mathrm{c}}) \right] + \\ &+ \sum_{\mu=1}^{\infty} \sum_{\substack{\nu=-\infty \\ (\nu\neq 0)}}^{\infty} \begin{bmatrix} a_{\mu\nu} \cos(\mu\omega_{\mathrm{c}} t + \mu\theta_{\mathrm{c}} + \nu\omega_{\mathrm{r}} t + \nu\theta_{\mathrm{r}}) + \\ + b_{\mu\nu} \sin(\mu\omega_{\mathrm{c}} t + \mu\theta_{\mathrm{c}} + \nu\omega_{\mathrm{r}} t + \nu\theta_{\mathrm{r}}) \end{bmatrix} \end{aligned} \tag{33}$$

where the first term represents the DC offset, the second one represents the fundamental component (alternatively with undesired baseband harmonics), the third one represents the carrier harmonics and the last one represents the sideband harmonics. Thus, it is possible to express with the equation (33) all switched patterns of a carrier-based PWM. Then, comparison of various carrier-based PWM strategies is possible from the perspective of the harmonic content. It should be also noted that the frequency of a monitored harmonic component is represented by the expression:

$$\omega_{monitored} = \nu\omega_{\mathrm{r}} + \mu\omega_{\mathrm{c}} \tag{34}$$

The coefficient ν determines the order of the sideband harmonic in the set of harmonics that are around the μ^{th} carrier harmonic.

2.2.2.2 Common Modulation Techniques

There are two basic modulation techniques, which differ from each other in the shape of the carrier signal, as indicated above.

The sawtooth modulation is depicted in Fig. 19. The ramps of the same direction from -1 p.u. to 1 p.u. form the reference signal. The edges of the pulses for IGBTs are generated in the point of the intersection. Note, that the instants when the edges of the pulses fall do not depend on the reference signal.

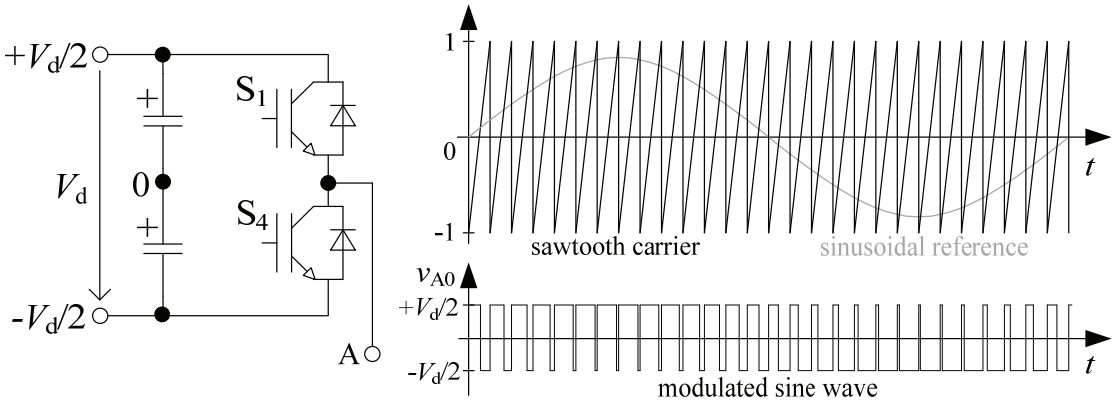


Fig. 19 Sawtooth pulse width modulation (naturally sampled)

Fig. 20 shows the triangle modulation. The carrier waveform comprises of symmetrical triangles -1 p.u. to 1 p.u. The fact that both edges of the pulses are modulated improves the harmonic spectrum. Therefore, this modulation technique is more common.

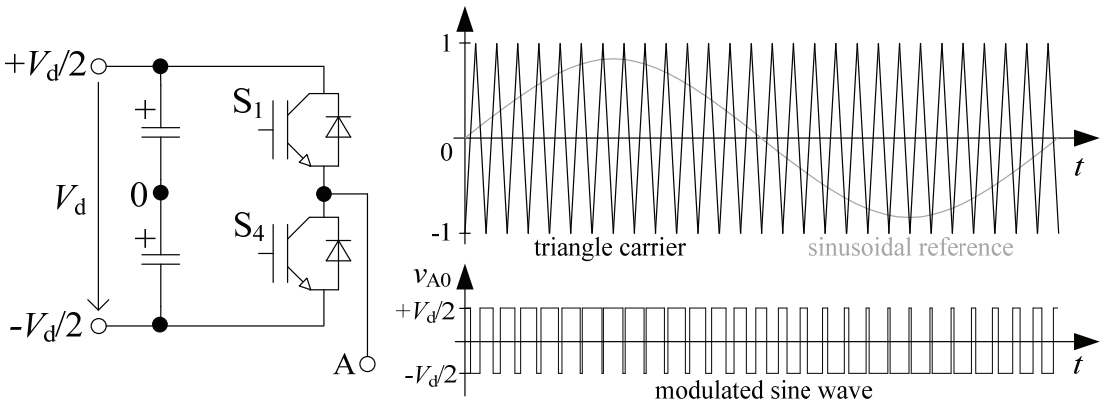


Fig. 20 Triangle pulse width modulation (naturally sampled)

The way how the modulation techniques are realized influences their quality. An analogue realization looks like it is outlined in the previous figures and it is known as the naturally sampled PWM. However, the implementation of a naturally sampled PWM in a digital system is difficult. That is why the so called regularly sampled PWM was developed. Its symmetrical version is based on the fact that the reference waveform changes its value at the instant when

the carrier triangle acquires either its positive or negative peaks. Fig. 21 shows an example of a triangle regularly sampled PWM with sampling in positive peaks.

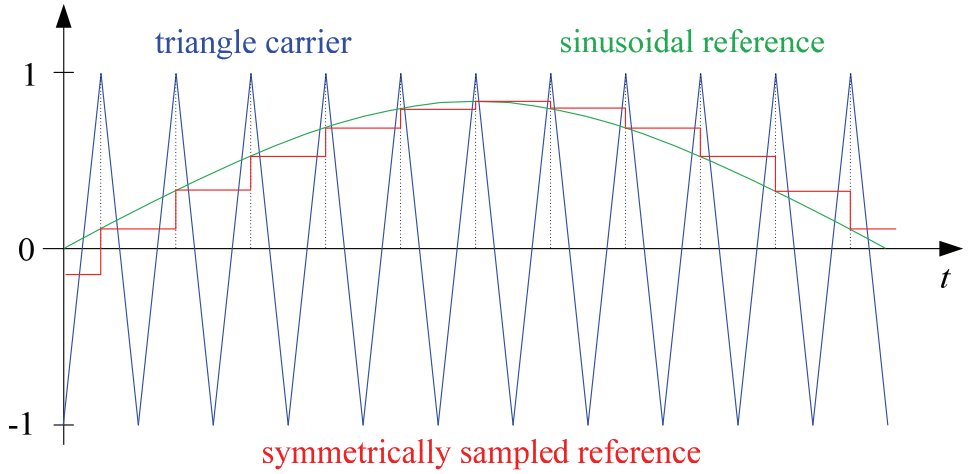


Fig. 21 Principle of the regular sampled PWM with a symmetrical positive peak sampling

In case of the asymmetrical version, the reference waveform is sampled at every peak of the triangle carrier as shown in Fig. 22.

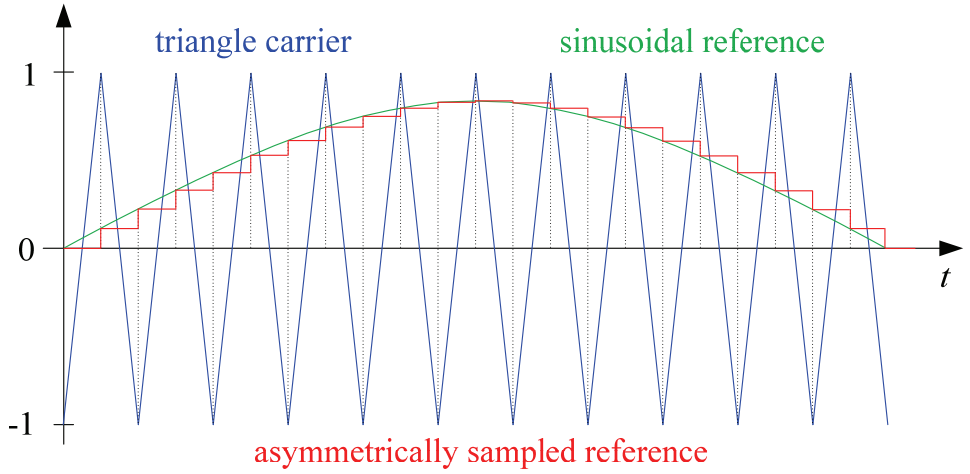


Fig. 22 Principle of the regular sampled PWM with an asymmetrical sampling

The harmonic content of the before mentioned techniques is presented in Table 5 (Holmes and Lipo, 2003). As can be seen from this table, the most convenient harmonic content of the digital implementation has an asymmetrical regular sampled PWM with triangular carrier.

Table 5 Harmonic content of several PWM techniques for modulation index M = 0.9 and frequency ratio P = 21. All data are normalized with respect to $V_d/2$ (%).

Harmonic order	Sawtooth Naturally Sampled PWM (%)	Sawtooth Regularly Sampled PWM (%)	Triangle Naturally Sampled PWM (%)	Triangle Regularly Sampled PWM - Symmetrical (%)	Triangle Regularly Sampled PWM - Asymmetrical (%)
1	90.0	89.9	90.0	89.7	89.9
2	0.0	6.0	0.0	0.5	0.0
3	0.0	0.6	0.0	0.1	0.2
4	0.0	0.1	0.0	0.0	0.0
5	0.0	0.0	0.0	0.0	0.0
16	2.1	0.8	0.0	0.0	0.0
17	7.0	4.3	1.2	0.6	0.7
18	17.7	15.0	0.0	1.1	0.0
19	30.5	31.9	26.8	24.8	25.1
20	25.5	27.9	0.0	5.3	0.0
21	51.2	51.2	71.2	71.2	71.2
22	25.5	21.5	0.0	5.0	0.0
23	30.5	28.3	26.8	28.1	28.4
24	17.7	19.4	0.0	1.8	0.0
25	7.0	9.8	1.2	1.9	1.9
26	2.1	4.1	0.0	0.1	0.0
WTHD	3.88	4.91	3.86	3.86	3.84

2.2.2.3 Modulation Techniques for Flying Capacitor Multilevel Inverters

(Carrera *et al.*, 1993) extended the classical PWM for the diode-clamped MIs. However, the same concept can be also used for FCMIs. In the multilevel approach is also operated with one reference signal but there are several triangular carriers. Their number depends on the number of levels. For an *N*-level inverter, *N*-1 carriers are required. All carriers have the same frequency and the same peak-to-peak amplitude and the bands they occupy are fully contiguous. Similarly as in the case of classical PWM, the reference waveform is compared with the carriers at every instant. There are *N*-1 bands and the result of the comparison in each band is the connection to the nearest higher level if the reference signal is higher than the carrier one or the connection to the nearest lower level if the reference signal is lower than the carrier.

In the three-phase operation, there are three reference sinusoidal waveforms shifted of 120 electrical degrees each. There are two possible realizations. Firstly, three shifted references are compared with one set of *N*-1 carriers, or secondly, one reference is compared with one set of *N*-1 carriers and this is used three times with an appropriate shift.

As can be seen in chapter 2.2.2.1, the content of harmonics depends on the frequencies and amplitudes of both waveforms. Therefore, two indices are set up from the practical point of view – a frequency ratio *P* and a modulation index *M*. The frequency ratio is defined as the ratio of the carrier frequency to the reference frequency:

$$P = \frac{\omega_c}{\omega_r} = \frac{f_c}{f_r} \tag{35}$$

The modulation index is defined as the ratio of the reference amplitude A_r to the amplitude of all carrier bands together:

$$M = \frac{A_r}{(N-1)A_c} \tag{36}$$

where A_c is the amplitude of one carrier band.

The mutual position of the carrier waveforms divides the carrier-based PWM of the MIs into three groups (Carrera *et al.*, 1993) introduced by their established abbreviations:

1. APOD (Alternative Phase Opposition Disposition) - all carriers are alternatively in opposition.
2. POD (Phase Opposition Disposition) – all carriers above the zero value reference are in phase with each other, but in opposition with those below the zero.
3. PD (Phase Disposition) – all carriers are in phase.

All three dispositions for five levels are depicted in Fig. 23.

As for the content of harmonics according to (Carrera *et al.*, 1993), when frequency ratio *P* is high, all three modulations are comparable, because all harmonics are shifted to high frequencies (and they can be effortlessly filtered). When *P* is not high enough, the PD PWM seems to be the worst because of its big content of harmonic at frequency ω_c. However, in the three-phase performance, this harmonic disappears from the spectrum and then it shows the lowest harmonic distortion (Agelidis and Calais, 1998). The results of the APOD PWM and

the POD PWM are identical for three levels but the POD PWM is the worst modulation for the case of five levels if we consider its harmonic spectrum (Holmes and Lipo, 2003).

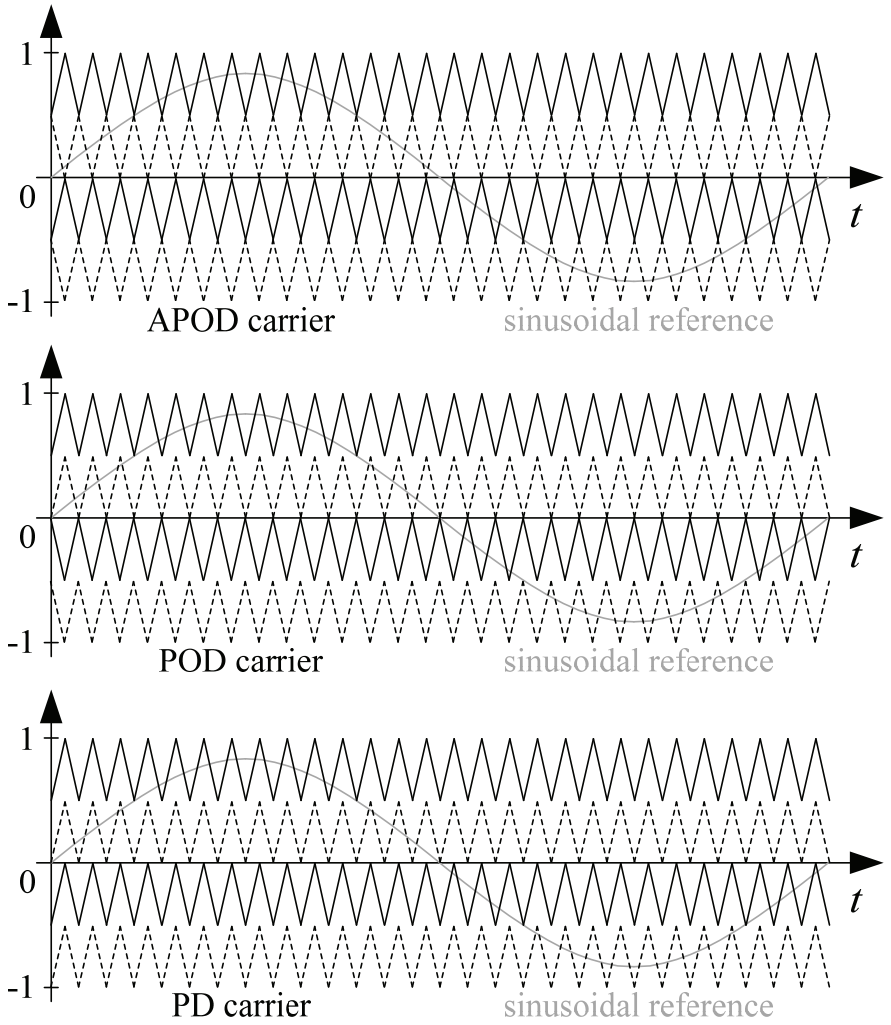


Fig. 23 Carrier dispositions of a PWM for five-level flying capacitor inverter (M = 0.83, P = 28)

2.2.2.4 PWM Scale Improving

As mentioned above, the PWM technique is quite simple and popular. However, it has one disadvantage unless it is slightly modified - the full extent of the input voltage cannot be applied to the output terminates of the inverter.

Let us assume a connection of the voltage source inverter as depicted in Fig. 4. The average rectified DC link voltage V_d can be expressed by:

$$V_{\mathrm{d}} = \frac{3\sqrt{2}\sqrt{3}}{\pi} V_{\mathrm{p,net}} \tag{37}$$

where $V_{\mathrm{p,net}}$ stands for a RMS phase input voltage of the supply net (Pavelka and Čeřovský, 2002).

Because the output terminal of an inverter can be connected either to the positive DC link pole $+V_{\mathrm{d}}/2$ or to the negative one $-V_{\mathrm{d}}/2$, the amplitude of the phase output voltage is $V_{\mathrm{d}}/2$ and its effective value $V_{\mathrm{p,out}}$ is:

$$V_{\mathrm{p,out}} = \frac{V_{\mathrm{d}}}{2\sqrt{2}} \tag{38}$$

The ratio of these two voltages gives the maximum utilization of the input phase voltage $V_{\mathrm{p,net}}$:

$$\frac{V_{\mathrm{p,out}}}{V_{\mathrm{p,net}}} = \frac{V_{\mathrm{d}}}{2\sqrt{2}} \frac{3\sqrt{2}\sqrt{3}}{\pi V_{\mathrm{d}}} = \frac{3\sqrt{3}}{2\pi} = 0.827 \tag{39}$$

From this calculation follows that a motor designed for a full net voltage and connected to the inverter output terminals will be capable of only 82.7% of its rated power. In the case of very large capacitors in the DC link, the capability increases to 88.6% because the capacitors remain charged on maximum value of the line-to-line input voltage:

$$\frac{V_{\mathrm{p,out}}}{V_{\mathrm{p,net}}} = \frac{V_{\mathrm{d}}}{2\sqrt{2}} \frac{\sqrt{2}\sqrt{3}}{V_{\mathrm{d}}} = \frac{\sqrt{3}}{2} = 0.886 \tag{40}$$

When it comes to a three-phase inverter, it has been found out that the maximum modulation index can be increased by injecting a third harmonic into the reference signal (Neascu, 2001). Let us suppose the injected reference sinusoidal voltage $v\,(\omega_{\mathrm{r}} t)$:

$$v\left(\omega_{\mathrm{r}} t\right) = \frac{V_{\mathrm{d}}}{2} M \sin \omega_{\mathrm{r}} t + \frac{V_{\mathrm{d}}}{2} M_3 \sin 3\omega_{\mathrm{r}} t \tag{41}$$

where M_3 is the modulation index of the third harmonics. It is clear that the third harmonic has no effect on the reference value when $\omega_{\mathrm{r}} t$ is a multiple of $\pi/3$. In order to find

the M_3, the resulting function caused by superposition should have its maximum in $\pi/3$ (Javůrek, 2003; Pavelka and Pavelka, 2006). This maximum can be solved by:

$$\frac{\mathrm{d}v(\omega_\mathrm{r} t)}{\mathrm{d}\omega_\mathrm{r} t} = \frac{V_\mathrm{d}}{2} M \cos\omega_\mathrm{r} t + 3\frac{V_\mathrm{d}}{2} M_3 \cos 3\omega_\mathrm{r} t = 0 \tag{42}$$

For $\omega_\mathrm{r} t = \pi/3$, the relationship for the modulation indices is found:

$$M = 6M_3 \tag{43}$$

The value of the modulation index after injecting the third harmonic is then:

$$\begin{gathered} v\left(\frac{\pi}{3}\right) = \frac{V_\mathrm{d}}{2} M \sin\frac{\pi}{3} + \frac{V_\mathrm{d}}{2}\frac{M}{6}\sin 3\frac{\pi}{3} = \frac{V_\mathrm{d}}{2} \\ M = \frac{2}{\sqrt{3}} = 1.155 \end{gathered} \tag{44}$$

Although the injection offers minimal harmonic advantage for PWM of the MIs, thanks to the increase of the modulation index of ca 15%, the PWM gives exactly the same results as a space vector modulation – judged by its modulation index.

2.2.3 Space Vector Pulse Width Modulation

Space vector pulse width modulation (SV PWM) is a form of PWM based on the space vector theory and it is often called either just space vector modulation (SVM) or carrierless PWM (Holtz, 1992). The main advantage compared to the carrier-based PWM is the explicit identification of pulses placement, especially for creating a zero space vector (Holmes and Lipo, 2003).

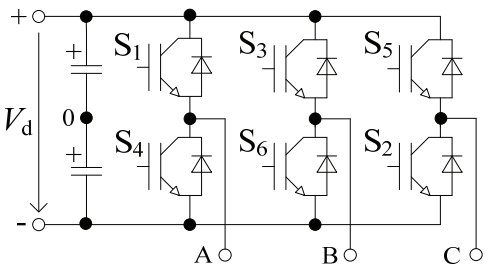
The principle of SVM can be easily explained on a classical three-phase two-level inverter which comes out from the fact that only eight switching combinations are possible to create. These eight combinations synthesize eight space vectors according to the table in Fig. 24. It says that e.g. the space vector $\overrightarrow{V_1}$ is synthesized when:

$$v_{\mathrm{A0}} = +V_\mathrm{d}/2,\ v_{\mathrm{B0}} = +V_\mathrm{d}/2,\ v_{\mathrm{C0}} = -V_\mathrm{d}/2 \tag{45}$$

Six of the space vectors $\left(\vec{V}_1 \div \vec{V}_6\right)$ are active vectors and two $\left(\vec{V}_7 \text{ and } \vec{V}_8\right)$ are passive or usually called zero vectors.

In fact, the space vectors are phase voltages of a three-phase system transformed into the stationary reference plane $\alpha\beta$ according to the transformation relationship (Měřička and Zoubek, 1968):

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix}\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{46}$$



S_1	S_2	S_3	S_4	S_5	S_6	SV
1	1	0	0	0	1	$\vec{V}_1$
1	1	1	0	0	0	$\vec{V}_2$
0	1	1	1	0	0	$\vec{V}_3$
0	0	1	1	1	0	$\vec{V}_4$
0	0	0	1	1	1	$\vec{V}_5$
1	0	0	0	1	1	$\vec{V}_6$
1	1	1	0	0	0	$\vec{V}_7$
0	0	0	1	1	1	$\vec{V}_8$

Fig. 24 Possible switching combinations for creating eight space vectors

After the transformation, all space vectors can be displayed as stationary vectors in a complex plane as depicted in Fig. 25 (a). The active vectors are of the magnitude 2/3 V_d.

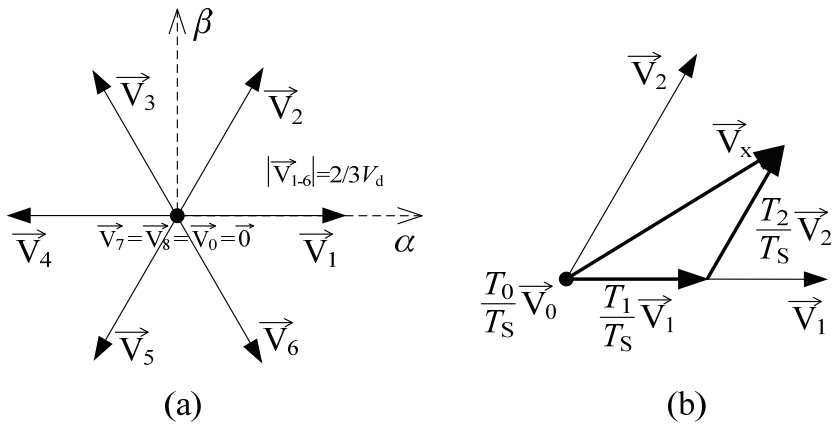


Fig. 25 (a) Space vectors in complex plane; (b) Composition of any space vector

Using these eight space vectors, any other space vector can be created. If it is required to switch e.g. the $\overrightarrow{V_x}$ in Fig. 25 (b), it will be constructed by the three closest vectors (two active, one passive) using geometry summation. Mathematically:

$$\overrightarrow{V_x} = \frac{T_0}{T_S}\overrightarrow{V_0} + \frac{T_1}{T_S}\overrightarrow{V_1} + \frac{T_2}{T_S}\overrightarrow{V_2} \tag{47}$$

where T_1 is the time for which the vector $\overrightarrow{V_1}$ is selected, T_2 is the time for which the vector $\overrightarrow{V_2}$ is selected, T_0 is the time for which the zero vector $\overrightarrow{V_0}$ is selected and T_S is the switching period. Besides, there is one condition that has to be fulfilled that the switching period T_S is the sum of the periods T_1, T_2 and T_0. (Neascu, 2001).

The sequence of switching is not defined. However, the most usual switch pattern is drawn in Fig. 26 - the active pulses are centred in each half carrier period.

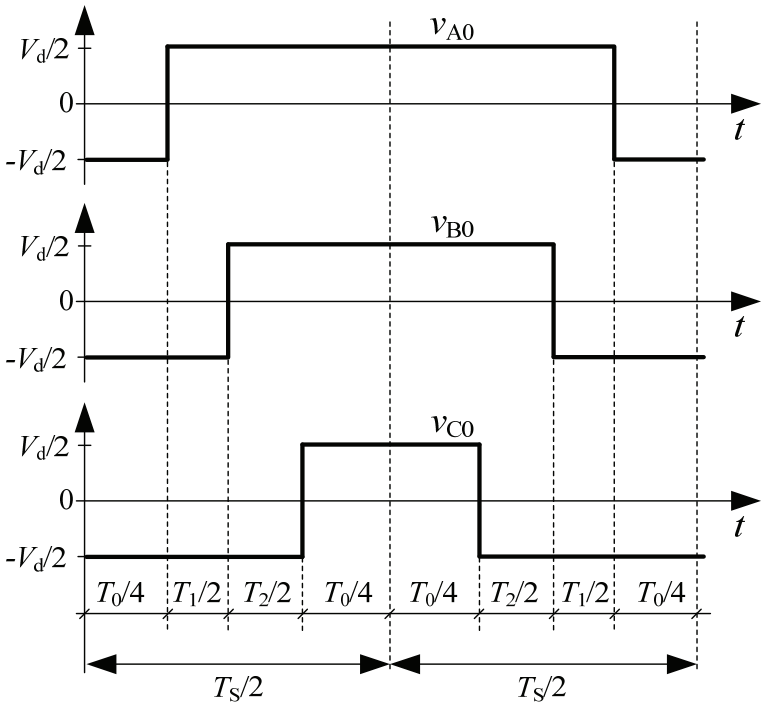


Fig. 26 Switch pattern with centred pulses

This is the same sequence as can be produced by a modified carrier-based PWM, the so called switching frequency optimum PWM (SFO PWM) (Urmila and Subbarayudu, 2010).

A rough idea of the algorithm for the construction of the desired space vector can be then:

1. Determining the inner triangle of the hexagon.
2. Computing the periods T_1, T_2 and T_0.
3. Making a suitable sequence of pulses.

The SV PWM technique and this algorithm are also applicable to MIs. There is a space vector diagram for a five-level MI depicted in Fig. 27.

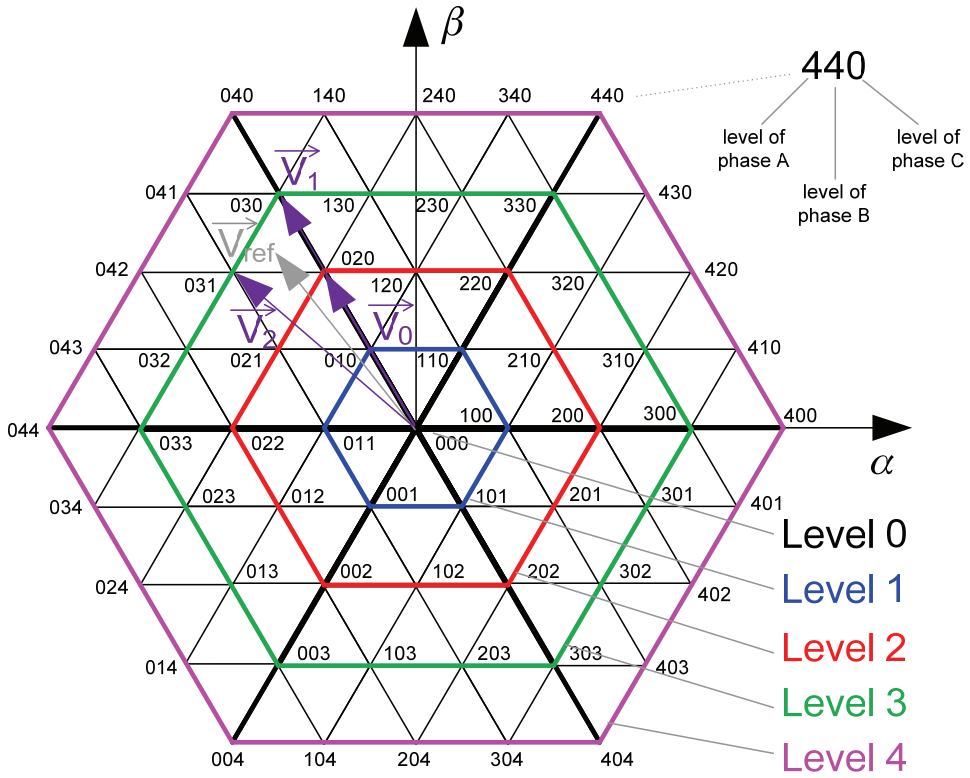


Fig. 27 Space vectors for five-level flying capacitor inverter in complex plane without the redundant states

In order to synthesize any desired space vector, the equation (47) can be applied. It is immediately obvious that the number of basic space vectors, redundant states and complexity has increased dramatically. The transitions between particular triangles have no unified rules and the control becomes complicated (Holmes and Lipo, 2003). (Li *et al.*, 2000) even split the control of the five-level inverter into two phase shifted three-phase inverters to simplify it. However, should we keep the character of the SVM, as mentioned above, the carrier-based SFO PWM can be used because it gives exactly the same results as the SV PWM for both

two-level and multilevel inverters. For the sake of logical continuity, the SFO PWM is prescribed in this chapter. Three reference waveforms of phase voltages v_a^*, v_b^* and v_c^* are given according to (McGrath *et al.*, 2001) by the uncomplicated relations:

$$v_k^* = v_k + v_{\text{off}} + v'_{\text{off}};\ k = \text{a, b, c} \tag{48}$$

where v_a, v_b and v_c are the original voltages of the three-phase system, further

$$v_{\text{off}} = -\frac{\max\left(v_a, v_b, v_c\right) + \min\left(v_a, v_b, v_c\right)}{2} \tag{49}$$

$$v'_{\text{off}} = \frac{V_d}{2(N-1)} - \frac{\max\left(v'_a, v'_b, v'_c\right) + \min\left(v'_a, v'_b, v'_c\right)}{2} \tag{50}$$

where

$$v'_k = \left(v_k + v_{\text{off}} + \frac{V_d}{2}\right) \bmod \left(\frac{V_d}{N-1}\right);\ k = \text{a, b, c} \tag{51}$$

2.2.4 Hysteresis Modulation

Hysteresis modulation, or more frequently hysteresis current control, is a method of voltage source inverter controlling. Its goal is to generate an output current in such a way that it follows the reference current waveform. This method asynchronously controls the semiconductor devices in an inverter in order to ramp the current up and down through the inductor so that it can track the reference current signal (Ingram and Round, 1999). Hysteresis current control is a control method that is the easiest to implement (Brod and Novotny, 1985). Its principle is easy to explain – again on a classical two-level inverter.

2.2.4.1 Hysteresis Current Control of Two-level Inverter

According to Ingram and Round (1999) a hysteresis current controller is implemented in a closed loop control system as depicted in Fig. 28. An error signal, $e(t)$, is used to control the switches in the inverter. This error is the difference between the desired current $i_{\text{ref}}(t)$, and the current being injected by the inverter $i_{\text{real}}(t)$. When the current error $e(t)$ reaches the upper limit of the controller, the switching devices are switched to produce a voltage that forces the

real current down. When the error reaches the lower limit, the current is increased in a similar way. The minimum and maximum values of the error signal are e_{min} and e_{max} respectively and their purpose is clear from Fig. 29. The range of the error signal, $e_{max} - e_{min}$, directly controls the amount of ripple in the output current from the inverter which is called the hysteresis band (HB). The hysteresis limits e_{min} and e_{max}, relate directly to an offset from the reference signal and they are referred to as the lower hysteresis limit and the upper hysteresis limit. The current is forced to stay within these limits (in the HB) even while the reference current is changing.

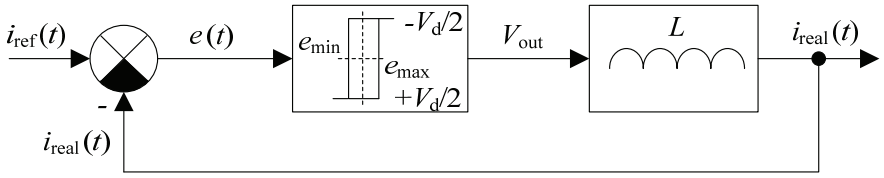


Fig. 28 Hysteresis current control in a closed loop control system

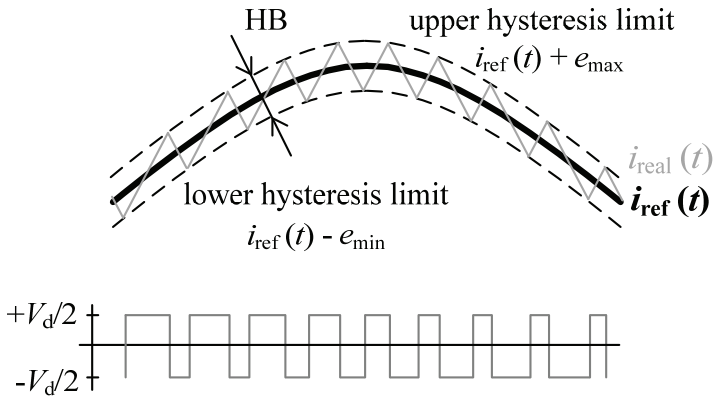


Fig. 29 Waveforms of hysteresis current control

The switching frequency is altered by the width of the hysteresis band, by the size of the inductor L (that the current flows through) and by the DC voltage applied to the inductor by the inverter. Larger inductance will yield smaller di/dt for a given voltage and so the inclination of the sawtooth waveform in Fig. 29 will be smaller.

2.2.4.2 Hysteresis Current Control of Five-level FCI

For MIs, higher number of voltage levels is available, so the simple hysteresis logic can be applied more widely. The first hysteresis technique used up to now was published by (Marchesoni, 1992). It is based on the creation of additional symmetrical hysteresis bands

around the reference signal and their purpose can easily be deduced from Fig. 30 (Shukla, 2011). Whenever the current error crosses the inner boundary B, the output of the inverter is decreased or increased by one level. It depends on which hysteresis boundary has just been crossed. The voltage change, which occurs, will force the current error to reverse its direction without reaching the next outer band. However, if the error does not reverse its direction, it will continue through the boundary of band B to the next outer band B_1. At this point, the next higher or lower voltage level is switched. This process continues until the current error direction reverses. If the voltage level applied at the boundary crossing of the error is insufficient to force the current error back, no next voltage level is applied as the current again crosses this boundary next time after the previous voltage level change with the same inclination. The current error is allowed to go until the next voltage level change at the next higher or lower boundary crossing of the current error to force it back as is evident from Fig. 30 (Shukla, 2011).

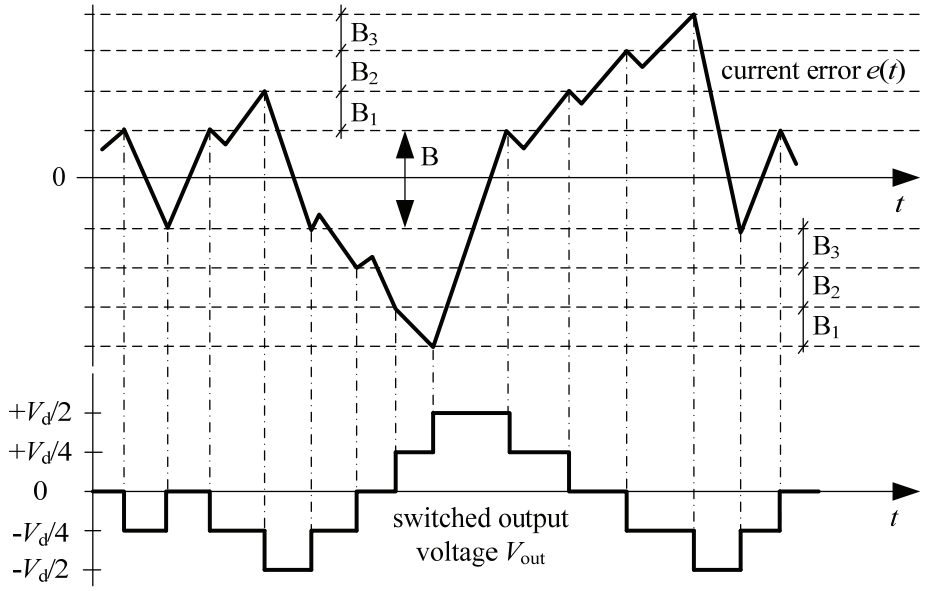


Fig. 30 Hysteresis current control of five-level flying capacitor inverter

2.3 Voltage Balancing of Flying Capacitors

In chapter 2.1, the principal function of a flying capacitor inverter is explained. In the same chapter the notion is introduced that the voltages across the flying capacitors determine the values of inner voltage levels and moreover the nominal voltages across the flying capacitors of three-, four- and five-level inverters are stated. If the nominal voltages of flying capacitors are maintained on the values given by the equation (21), the voltage levels are evenly spread

out over the range of the input voltage which is the required situation. To maintain the nominal voltages it is possible to either add additional auxiliary power circuits or to apply a control strategy (Kobrle and Pavelka, 2012b). The maintenance of nominal voltage by a control strategy will be discussed later. This way of maintaining the nominal voltage is usually called voltage balancing.

Fig. 11 and Fig. 12 demonstrate the effect of a flowing load current on the voltage across a flying capacitor in the case of a three-level inverter. The situation is similar in the case of any-level FCI. Fig. 31 shows equivalent circuits of all sixteen possible switching states for a five-level FCI according to Table 3. Note, that the connections are drawn for a positive load current. This current either charges or discharges the flying capacitors.

Mathematically, the change of voltage across the flying capacitor is expressed by equation (5). Note that the magnitude of the voltage change (for a switching mode) can be expressed as:

$$\Delta v_{\mathrm{Cx}}(t) = \frac{\Delta i(t)}{C_{\mathrm{x}}} T_{\mathrm{s}} = \frac{\Delta i(t)}{f_s C_{\mathrm{x}}} \tag{52}$$

where T_s is the switching period and f_s is the switching frequency.

The principal functioning of the PWM technique for MIs is explained in chapter 2.2.2.3. If the above mentioned facts related to the switching pulse generation (esp. Fig. 23) were used for a five-level FCI, then, according to Table 3, it is clear that the switching process would only operate with “basic” switching states 1, 5, 8, 15, 16 – exactly one switching state for each voltage level. In agreement with Fig. 31 and Fig. 16, for the switching state 1 can be written that:

$$V_{\mathrm{out}} = Z \cdot i_{\mathrm{L}}(t) = -V_C = -\frac{V_{\mathrm{d}}}{2} \tag{53}$$

Similarly for switching state 16:

$$V_{\mathrm{out}} = Z \cdot i_{\mathrm{L}}(t) = +V_C = +\frac{V_{\mathrm{d}}}{2} \tag{54}$$

It follows from equations (53) and (54) that the load voltage is constant in these states and its value is given by the range of the voltage in the DC link.

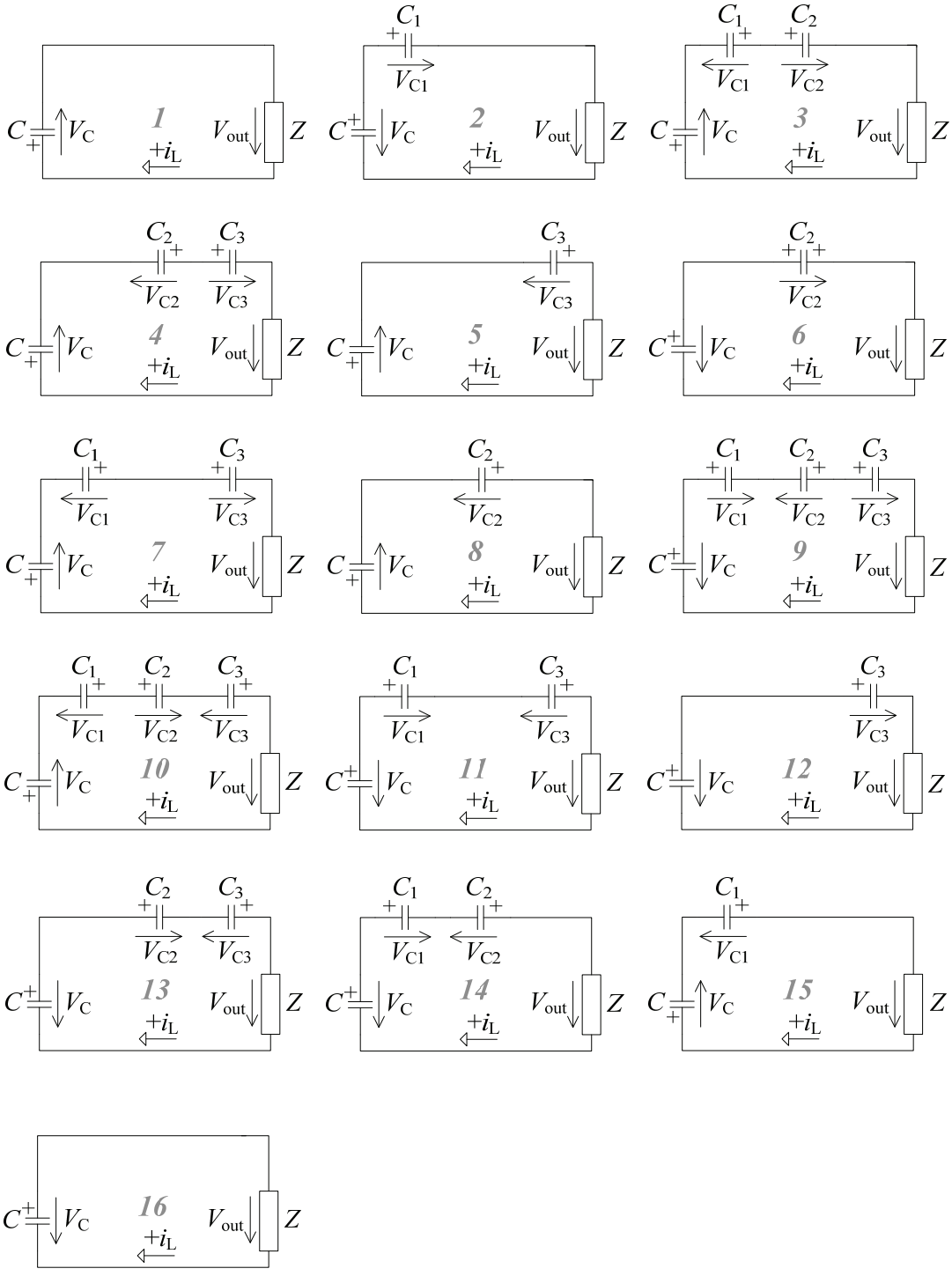


Fig. 31 Equivalent circuits for all 16 switching states of the five-level flying capacitor inverter (the grey numbers in the middle of the circuits are numbers of the switching states)

States 5, 8 and 15 are quite similar, except for the flying capacitor. Generally, it can be written that:

$$V_{\text{out}} = Z \cdot i_{\text{L}}(t) = v_{\text{Cx}}(t) - V_C \tag{55}$$

It is also apparent that the load current can be expressed as:

$$i_{\text{L}}(t) = -C_{\text{x}} \frac{\text{d}v_{\text{Cx}}(t)}{\text{d}t} \tag{56}$$

By the merging the equations (55) and (56), the following result is obtained:

$$ZC_{\text{x}} \frac{\text{d}v_{\text{Cx}}(t)}{\text{d}t} + v_{\text{Cx}}(t) = V_C \tag{57}$$

Equation (57) is the first order non-homogeneous differential equation. Its solution is:

$$v_{\text{Cx}}(t) = V_C \left(1 - \text{e}^{-\frac{t}{ZC_{\text{x}}}}\right) + \text{K}\text{e}^{-\frac{t}{ZC_{\text{x}}}} = \frac{V_{\text{d}}}{2}\left(1 - \text{e}^{-\frac{t}{ZC_{\text{x}}}}\right) + \text{K}\text{e}^{-\frac{t}{ZC_{\text{x}}}}; \text{x} = 1,2,3 \tag{58}$$

where the coefficient K represents the initial value of the voltage across the flying capacitor.

Equation (58) says that the voltages across all three flying capacitors would stabilize on value $V_{\text{d}}/2$ in a steady state. This is in contradiction with the presumptions (11) - (13). Therefore, the five-level FCI is not able to operate exclusively under the carrier-based PWM. It is a so called not self-balanced inverter. For voltage balancing of flying capacitors is it necessary to use the redundant switching states in the control algorithm.

2.3.1 State Diagrams

For the understanding of the balancing algorithm, construction of the so called state diagrams is very useful. These diagrams show how many switching states are possible, how many and which states are redundant (i.e. which states produce the same voltage levels), what the situation is across the flying capacitor and which transitions are possible. The state diagrams are created by combining Table 3 and Fig. 31. From the equation (5) follows, depending on the polarity of the load current i_{L}, that the capacitor is either charged or discharged.

Consequently, charging or discharging are not associated with the switching state only, but also with the polarity of the passing current. It is obvious that when one direction of the current does charge the capacitor, the second one discharges it.

To avoid voltage stress of the IGBTs, the only acceptable changes of the output voltage are the ones that are the closest to the neighbouring levels. With respect to this condition the state diagrams in Fig. 32 can be designed. The first one shows the situation for the positive current polarity, the second one for the negative current polarity. The signs +, -, 0 in the lower part of the circle indicate the situation across the flying capacitor: + means that the capacitor is being charged, - that the capacitor is being discharged, 0 the capacitor is staying intact. The arrows show the possible transitions from one permitted state to another. (The possibilities of transitions will be discussed in chapter 2.4 in detail.) By transiting, e.g. from level 0 to level 1, it is possible to choose from the four neighbouring switching combinations. Thus, switching states 2, 3, 4 and 5 are redundant states. One convenient switching state will then be selected according to the instantaneous voltage across the flying capacitor as well as the current direction in order to minimize the voltage ripple across the capacitor. By setting these conditions and by determining the process priorities in question, the right control strategy for voltage balancing can be designed.

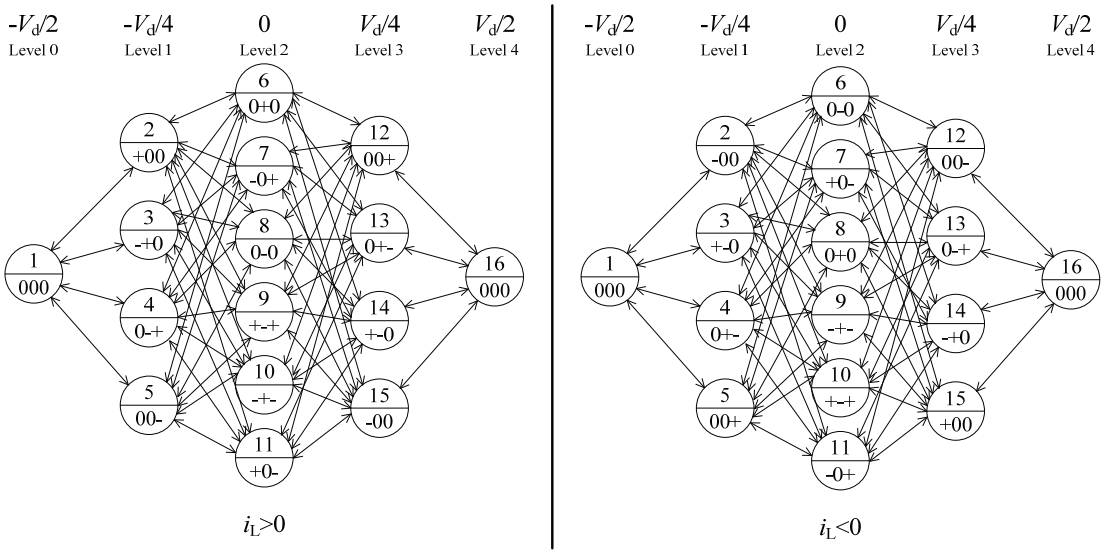


Fig. 32 State diagrams of five-level flying capacitor inverter

2.3.2 Control Algorithm for the Flying Capacitor Voltage Balancing

In previous chapters, it was proved that it is not possible to stabilize the flying capacitor voltage without redundancy and that the switching redundancy is not utilized under the

carrier-based PWM only. The control algorithm for the five-level FCI proposed in this chapter can be considered a two stage modulation system (Gateau, 2010). This system takes the requirement of a pulse width modulator and also the other requirements into account. It also ensures the best switching combination for the next switching step. These are the two main goals:

1. The requirement of the desired voltage level according to the results of the carrier-based pulse width modulator.
2. Choosing the most suitable switching state with regard to the voltage balancing of flying capacitors.

A more detailed idea of the two stage modulation system (Kobrle and Pavelka, 2009) is depicted in Fig. 33. The desired "basic" switching state (1, 5, 8, 15 or 16), or rather the desired voltage level, is a requirement of the carrier-based PWM modulator. This requirement is processed by the balancing algorithm and the result of the assessment represents the most suitable switching state, or rather the set of control signals for the IGBTs. It is necessary to mention that in the case of the two stage modulation system, the output of the pulse width modulator is adjusted, so the properties of this system and a pure PWM differ from each other. Nevertheless, the comparison of the mentioned carried-based techniques within the two stage modulation system shows that concerning the spectral quality the PD PWM remains the best choice (Gateau, 2010).

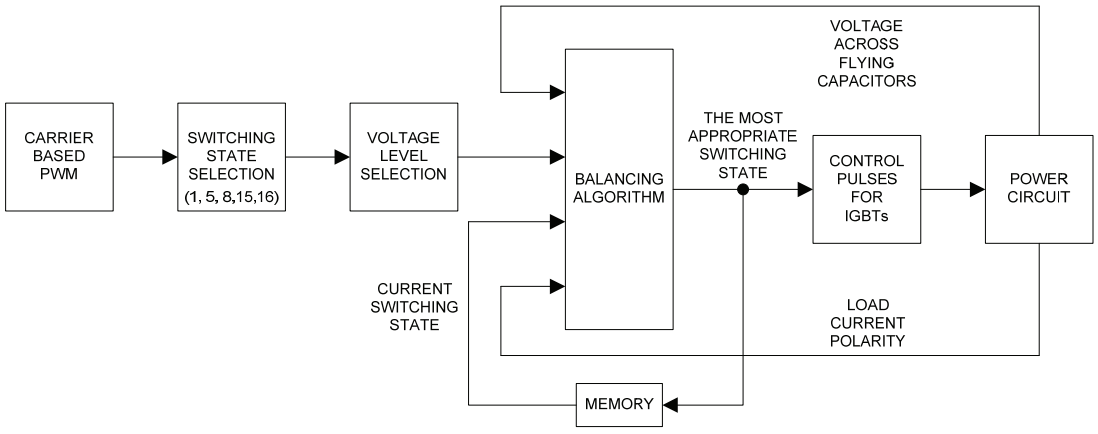


Fig. 33 Basic idea of the two stage modulation system

In compliance with the state diagrams in Fig. 32, the balancing algorithm needs three more pieces of input information for its proper function. That is:

- the polarity of the load current in order to select the correct diagram

- the current switching state in order to determinate the right way of transitioning to the next switching state
- the current voltage across all flying capacitors

But this says nothing about the manner of voltage stabilization. It could be carried out according to (Kobrle and Pavelka, 2009) where the algorithm was published:

The basic knowledge needed to select the proper state diagram and the current voltage across all flying capacitors that are measured is the instantaneous direction of the load current. Then, the flying capacitor with the biggest relative deviation from its relevant nominal voltage is detected and the polarity of the deviation is determined. According to the actual switching state and the desired voltage level, a new switching state is selected, so that the voltage across it will be stabilized or will stay at the current value. The eventuality of staying at the current value has to be permitted, since not always are there convenient switching states that can charge or discharge the capacitor as necessary. If there are two possibilities of switching that would stabilize the capacitor with the biggest deviation, the same evaluation of magnitude and polarity of the deviation will be carried out for the remaining two capacitors and the most suitable one will be selected.

The presented algorithm ensures stabilization of the voltage across flying capacitors. In fact, similar algorithms are usually implemented either as a combinatorial or as a state machine (Gateau, 2010). An optimized implementation – when it comes to the maximum execution speed - using look-up tables is described in chapter 2.5.2.

2.4 Analysis of the Switching Process of a Five-level FCI

In chapter 1.4 was stated that the switching process of a MI is patterned on a switching process of a classical two-level inverter as it is supposed in literature including substantial publications such as (e.g. Corzine and Kou, 2003; Huang and Corzine, 2006; McGrath and Holmes, 2007; Escalante *et al.*, 2002; Meynard *et al.*, 1997; Lai and Peng, 1996). However, theoretically another possibility of switching for MI can be implemented, as was for the first time published in (Kobrle and Pavelka, 2010) for the case of a four-level FCI.

2.4.1 Commutation of Two-level Inverter

For every phase of the two-level inverter here is just one switching pair, as shown in Fig. 4. Thus, if a current is present and the device should get from on-state to off-state or vice versa (simply - transition), there occurs one load commutation; the conducting of one power device is taken over by the second one. As we know from the standard two level voltage inverter

theory, two semiconductor devices must not switch at the same time because of a short-circuit of the voltage source. This is secured by the so called dead time. A dead time is a blank time between the moment when the first switch turns off and the second one turns on. At the moment of the dead time both switches are turned off. If there is a load current, its conducting is taken over by an anti-parallel diode. The duration of the dead time depends on the type of the power devices that are being used and especially on their dynamic characteristics. The situation is depicted in Fig. 34, for detailed description see below.

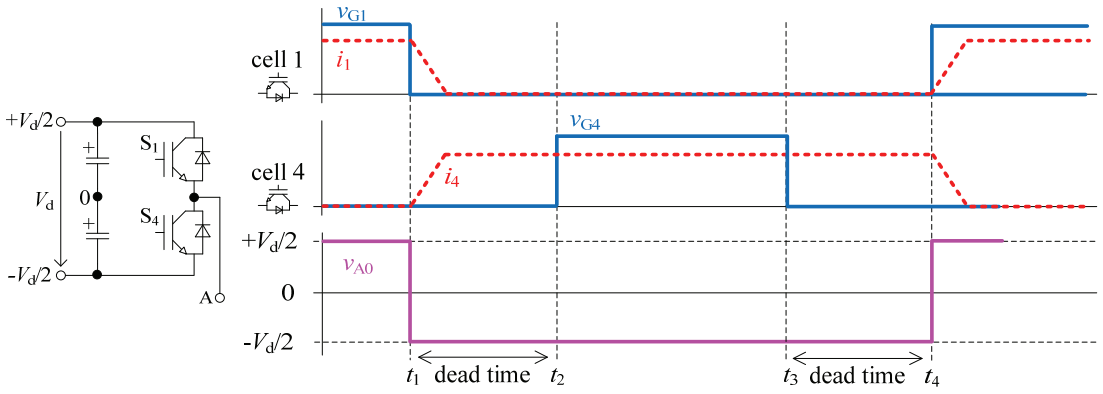


Fig. 34 Switching transitions of two-level inverter.

For a simple and clear analysis we will suppose a frequent state of non-intermitted current. Let us set the load inductance value big enough to maintain the constant current at the moment of the switch. The transient processes appeared by turning on and turning off can be neglected due to their short times of duration. Also the current rising and falling can be considered as linear because its real waveform does not influence the explanation what happens by transitions. Let the load current direction to be positive, V_1 conducting (turned on) and V_4 turned off. Under these conditions, the output terminal is connected to the positive potential of a DC link. With the turn-off control command v_{G1} for V_1, the current commutates from V_1 to D_4, the output terminal is on the negative potential. After a dead time, turn-on control signal v_{G4} for V_4 is got and nothing is changing from current point of view. Reversely, V_4 turns off but switching cell S_4 is still in conducting because only the anti-parallel diode D_4 is conducting in case of positive current. V_1 begins to conduct after a dead time, the current commutates back to V_1 and so the output terminal is connected back to positive pole of the DC link.

2.4.2 1C-transitions of Five-level Flying Capacitor Inverter

There was described in details and explained in chapter 2.1.1 how the three-level FCI switches and what is the complementary switching. Then, it was shown that the principle of the complementary switching is the same also in case of more-level FCI. A switching process of MIs patterned on a switching process of classical two-level inverters mentioned above means that only one complementary switching pair switches in one phase leg by turning over. However, a five-level FCI enables turning over of up to four complementary switching pairs at the same time. It will be kept following marking: under 1C-transition is understood the transition when one commutation occurs (one complementary switching pair turns over); under 2C-transition is understood the transition when two commutations occur (two complementary switching pairs turn over); under 3C-transition is understood the transition when three commutations occur (three complementary switching pairs turn over); under 4C-transition is understood the transition when four commutations occur (all four complementary switching pairs turn over). The similar analysis of switching as for two-level inverter will be performed for all three possibilities of the five-level FCI further.

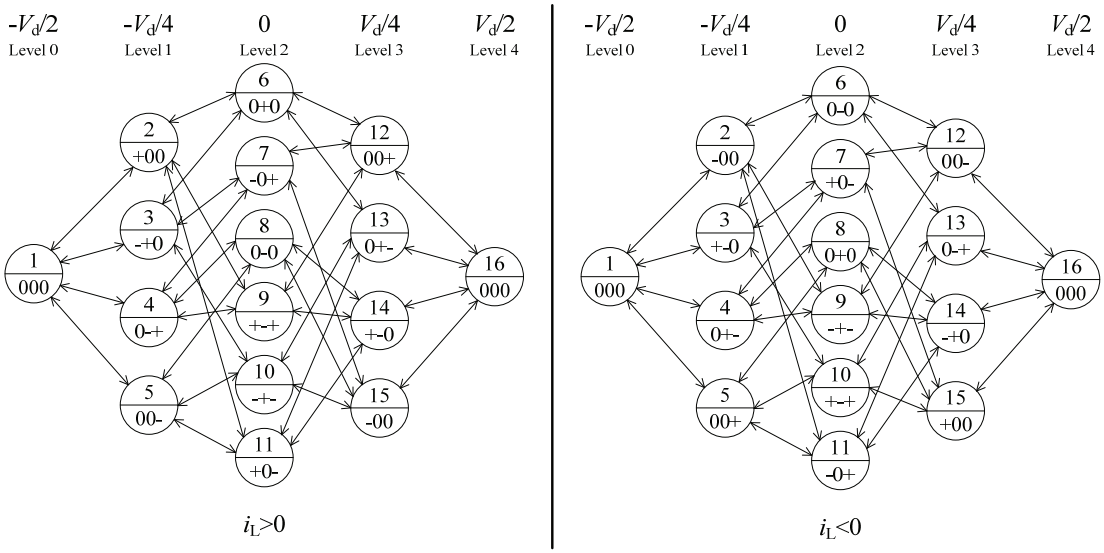


Fig. 35 State diagrams of a five-level FCI for 1C-transitions

All possible 1C-transitions of a five-level FCI (Fig. 17) are depicted in the state diagrams presented in Fig. 35. There are 64 of them for each direction of the load current i_L. Let us select a sample of transitions for one phase and with the help of it explain the principle of the 1C-transition. The sample transition we chose is from the switching state 6 to 2 and back, for a positive load current. The transitions are shown in Fig. 36. The power devices S_{1A}, S_{2A}, S_{5A}

and S_{6A} from Fig. 17 are turned on in the state 6. The load current flows through V_{1A}, V_{2A}, D_{6A} and D_{5A} and the output terminal A is connected to the voltage 0. At the time t_1 the switch S_{2A} turns off, the load current begins to commutate to the diode D_{7A} and the output terminal A is on potential $-V_d/4$. Thanks to this commutation the inverter is transferred directly from the switching state 6 to 2. If the load current does not decrease due to high inductance during the blank time, it no more depends on the time t_2 when the switch S_7 turns on. For a reverse transition, the switching state 2 is the initial state. At the time t_3 the switching cell S_{7A} turns off but the current keep flowing through the diode D_{7A}, so the switching state stays 2. After turning the S_{2A} on at t_4 the current commutates from D_{7A} to V_{2A} and on the output terminal the voltage 0 appears – the inverter is in the switching state 6 again.

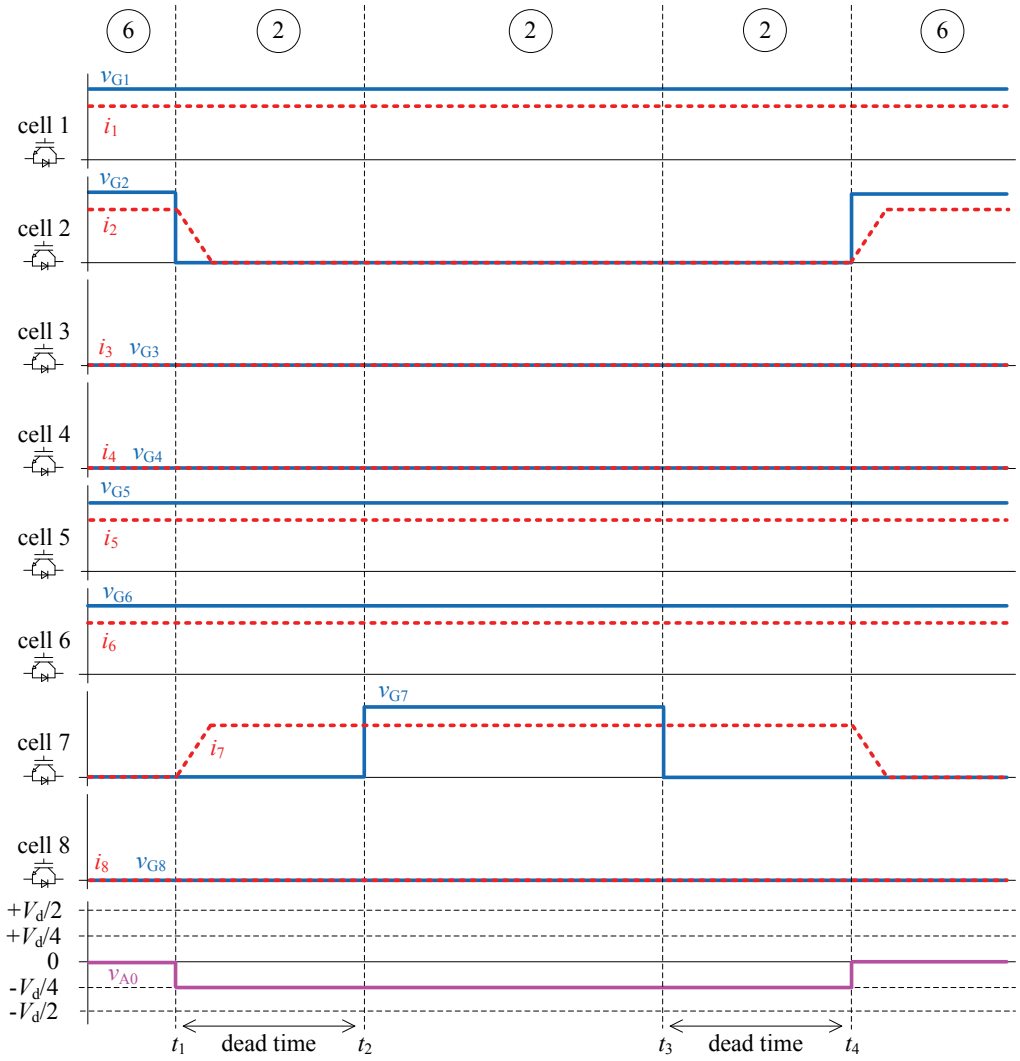


Fig. 36 1C-transitions

2.4.3 2C-transitions of Five-level Flying Capacitor Inverter

All possible 2C-transitions of a five-level FCI (Fig. 17) are shown in the state diagrams presented in Fig. 37. There are 48 of them for each direction of the load current i_L. As an example, the 2C-transitions from the switching state 6 to 7 and back for a positive load current are selected. The transitions are depicted in Fig. 38. The power devices S_{1A}, S_{2A}, S_{5A} and S_{6A} are turned on in the state 6. The load current flows through V_{1A}, V_{2A}, D_{6A} and D_{5A} and the output terminal A is connected to the potential 0. At the time t_1 switches S_{1A} and S_{6A} turn off, the dead time begins and the load current commutates to the diode D_{8A}. This closed circuit corresponds to the switching state 3, so the output terminal A is on potential $-V_d/4$. After the dead time at time t_2 the switching cells S_{3A} and S_{8A} turn on, the load current commutates from the diode D_{6A} to the valve V_{3A} and the output terminal is connected back to the potential 0. The back transition begins with turning the switching cells S_{3A} and S_{8A} off. At the beginning of the dead time at t_3, the load current commutates from V_{3A} to D_{6A}. The state that just passed corresponds to the switching state 3, the voltage $-V_d/4$ appears on the output terminal A. At the end of the dead time t_4 the load current commutates from the D_{8A} to V_{1A} thanks to turning the S_{1A} and S_{8A} on and this ensures the switching state 6 which means there is a 0 potential on the output terminal.

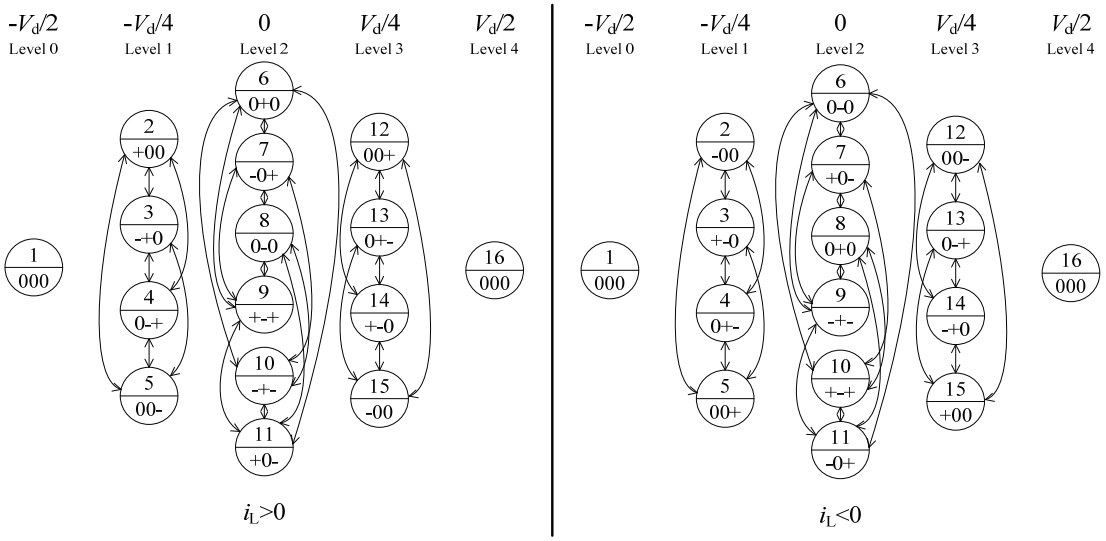


Fig. 37 State diagrams of a five-level FCI for 2C-transitions

The crucial difference between 1C- and 2C-transitions lies in the dead time. Since the voltage stays constant in the case of the 1C-transitions, it alternates between two neighbouring voltage levels in the case of the 2C-transitions. A request for a switching within one voltage level means the increase of switching frequency, practically because of the

possibility to switch in each modulation cycle. However, it does not contradict the core of MIs. In addition, according to the equation (52) better voltage stabilization across the flying capacitors is expected.

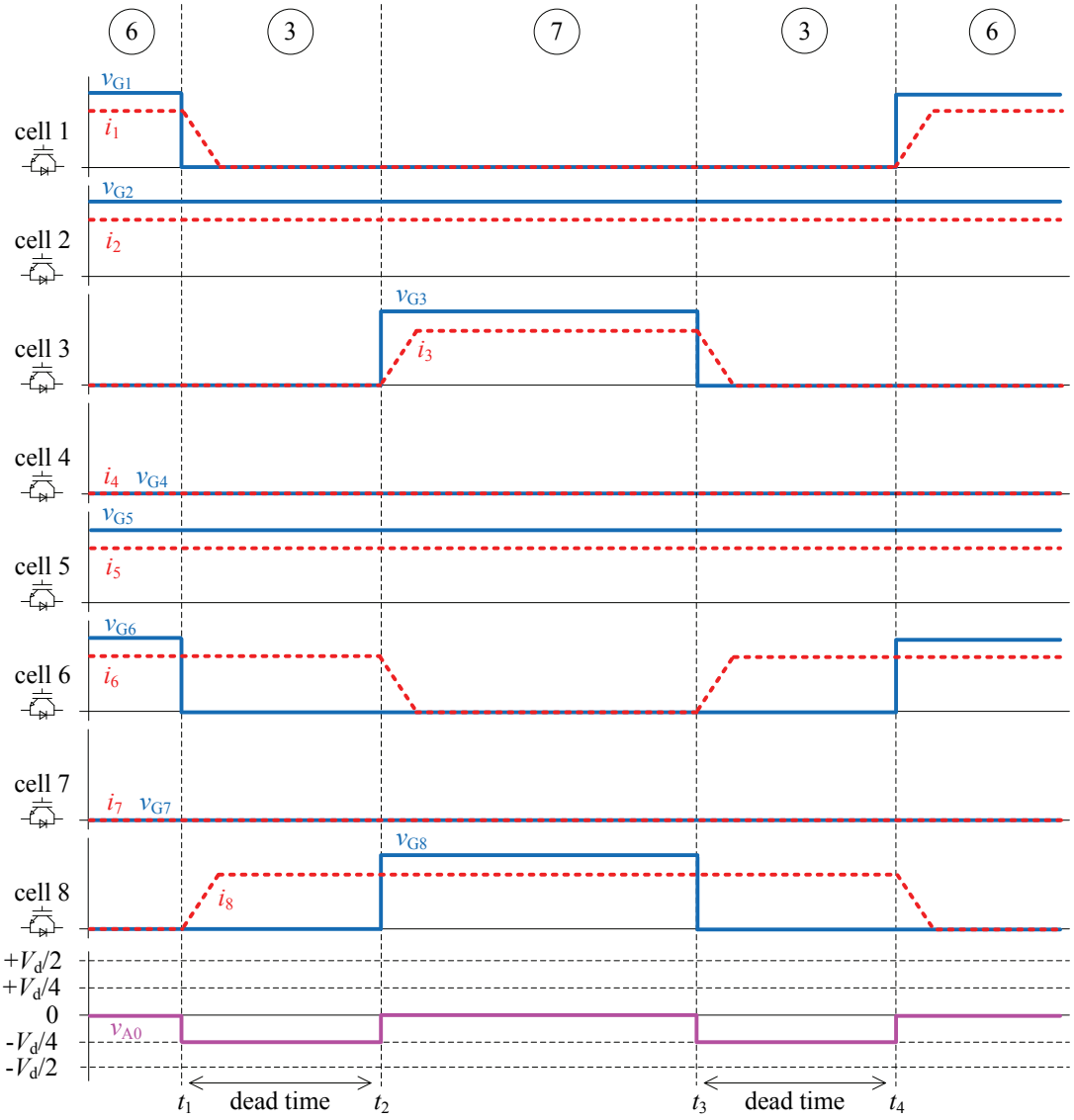


Fig. 38 2C-transitions

2.4.4 3C-transitions of Five-level Flying Capacitor Inverter

All possible 3C-transitions of a five-level FCI (Fig. 17) are shown in the state diagrams presented in Fig. 39. There are 48 of them for each direction of the load current i_L. As an example, the 3C-transitions from the switching state 7 to 2 and back for a positive load

current are selected. The transitions are depicted in Fig. 40. the power devices S_{2A}, S_{3A}, S_{5A} and S_{8A} are turned on in the state 7. The load current flows through V_{2A}, V_{3A}, D_{5A} and D_{8A} and the output terminal A is connected to the voltage 0. At the time t_1 the switches S_{2A}, S_{3A} and S_{8A} turn off, the dead time begins and the load current commutates from V_{2A} to D_{7A} and from V_{3A} to D_{6A} - D_{8A} keeps conducting. This closed circuit corresponds to the switching state 1, so the output terminal A is on potential $-V_d/2$. After the dead time at the time t_2 the switching cells S_{1A}, S_{6A} and S_{7A} turn on, the load current commutates from the diode D_{8A} to the valve V_{1A} and the output terminal is connected to the potential $-V_d/4$, because the inverter is in the switching state 2. The transition back to state 7 begins with turning the switching cells S_{1A}, S_{6A} and S_{7A} off. At the beginning of the dead time at t_3, the load current commutates from V_{1A} to D_{8A}, the diodes D_{6A} and D_{7A} keep conducting. The state that just passed corresponds to the switching state 1, the voltage $-V_d/2$ appears on the output terminal A. At the end of the dead time at t_4 the load current commutates from D_{7A} to V_{2A} and from D_{6A} to V_{3A} thanks to turning the S_{2A} and S_{3A} on and that ensures the switching state 7 which means there is a potential 0 on the output terminal.

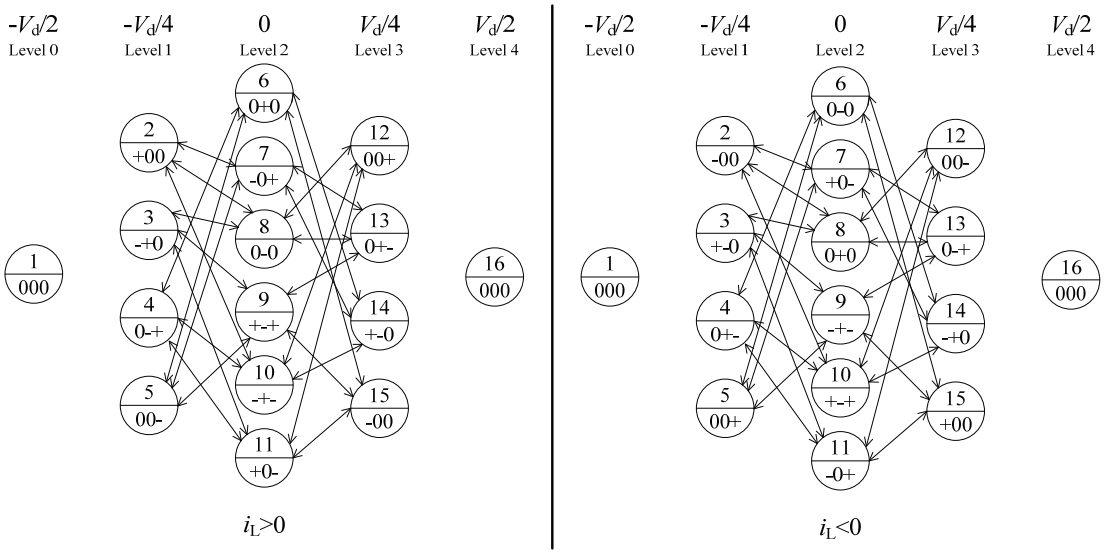


Fig. 39 State diagrams of a five-level FCI for 3C-transitions

The above mentioned description and the Fig. 40 clearly show that between two required neighbouring states another switching state appears. The 3C-transition involves a step over two voltage levels. The reason for this is the dead time. During the dead time, the one pole of the load is connected either to a positive or to a negative polarity of the DC link. According to chapter 1.2.4, a step over two voltage levels is not acceptable because the voltage stress across the semiconductor devices would in such a case be too big and the main purpose of the

multilevel topology was vain. That is why the 3C-transitions are not permitted in proper operation of the FCMI.

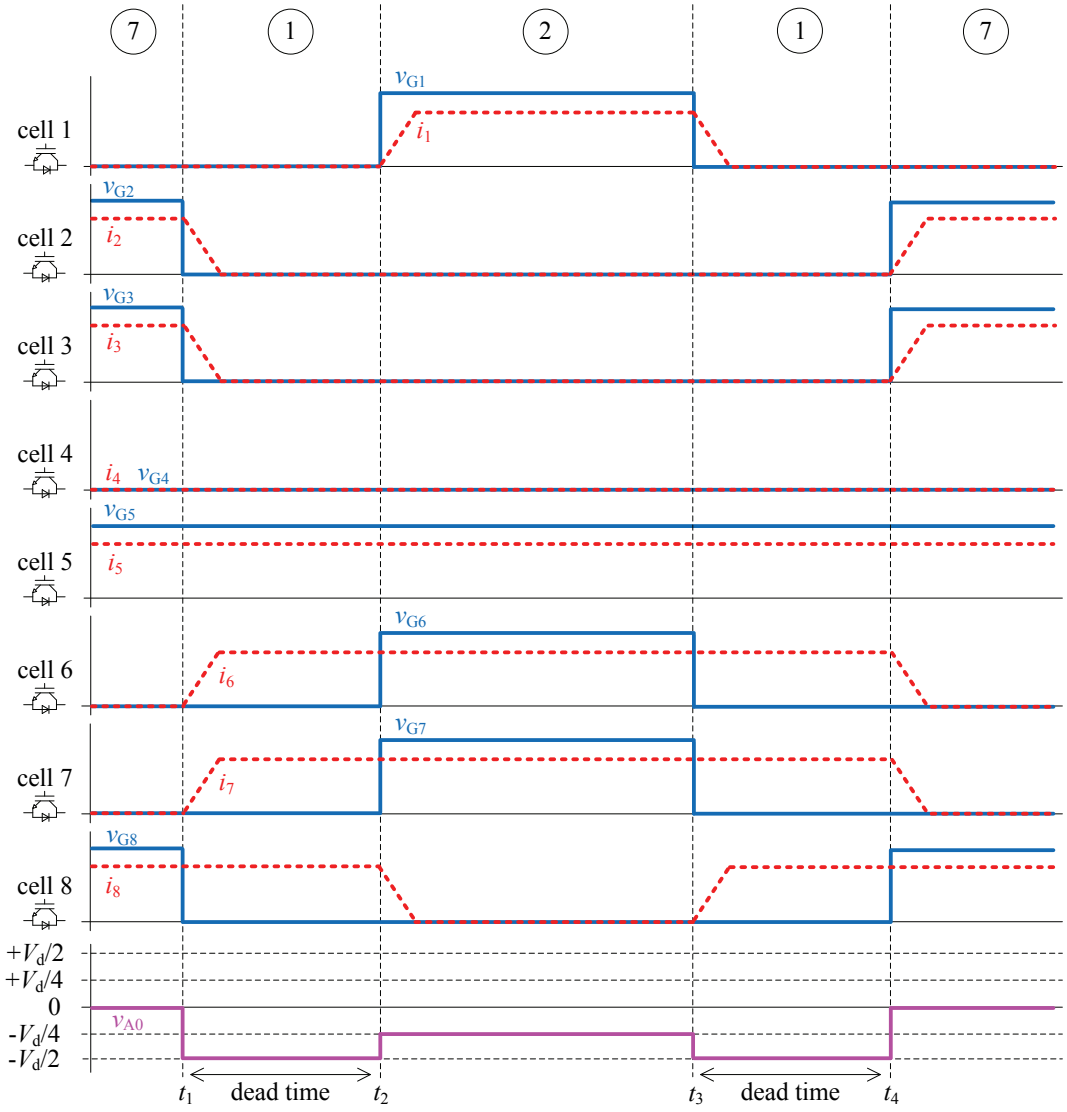


Fig. 40 3C-transitions

2.4.5 4C-transitions of Five-level Flying Capacitor Inverter

In order to make the list exhaustive the transitions with four commutations are mentioned because the 4C-transitions are theoretically possible by a five-level FCI. However, these transitions a priori require a jump over two or more levels. As stated above, these jumps are not acceptable for a correct operation. Therefore, it is not worthwhile to deal with it in more detail.

2.5 Simulation Model of a Three-phase Five-level Flying Capacitor Inverter

A simulation model of the three-phase five-level FCI is realized in this chapter because it belongs to the objectives of this Thesis.

The simulation model was created in the program Matlab-Simulink. For the power part the toolbox SimPowerSystem was used, for the control part the basic toolbox Simulink. A general view of the model is depicted in Fig. 41.

2.5.1 Power Part and Pre-charging

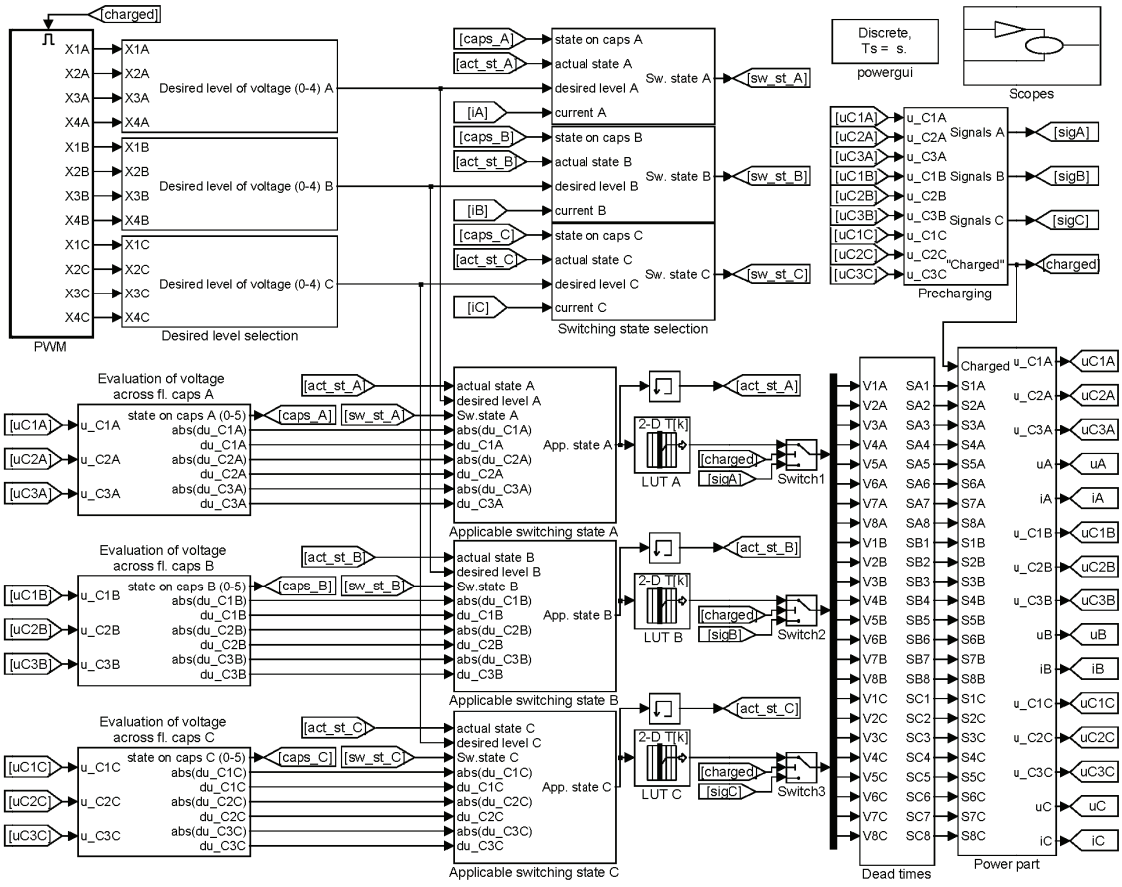


Fig. 41 General view of a five-level flying capacitor inverter - Simulink model

The simulated power part in block "*Power part*" corresponds to the scheme in Fig. 17. There is one phase depicted in Fig. 44. As the semiconductor switch, the offered model of the IGBT was used. All flying capacitors have parallel connected resistors which represent the leakage,

and the voltage across them is measured. Fig. 43 shows how all three phases are connected together – they are supplied from the DC link and their outputs are connected to the three-phase RL passive load in star connection. The phase voltages of the inverter and the load currents are measured. A DC link, comprised of two capacitors and their leakages, is depicted in Fig. 42. They are supplied with the DC voltage from a diode rectifier which rectifiers the voltage from a symmetrical three-phase AC voltage source. At the start of the simulation both of the capacitors have a pre-set initial voltage (a DC link voltage) because the charging process of the capacitors in the DC link was not a part of the simulation. The pre-charging resistors and the electrical contactors in the DC link are also interconnected. They serve as pre-charging devices for the flying capacitors. After all flying capacitors are charged, the electrical contactors bridge the pre-charging resistors. For proper simulation one pre-charging resistor and one electrical contactor have to be interconnected to each pole of the DC link.

Fig. 45 shows the pre-charging logic. From this block, the control signals are transmitted directly to the IGBTs. All IGBTs, except for the two central in each phase (S4x and S5x), are switched on at the beginning. The flying capacitors are charged from the DC link over the pre-charging resistors and the instantaneous voltages are measured across them. After the flying capacitor reaches its nominal voltage, it is disconnected from charging by the appropriate couple of IGBTs. When all flying capacitors are charged, the pre-charging resistors are bridged by electrical contactors and the operating mode of the FCMI can begin by activating the block "*PWM*" and by switching the "*Switch1"* – "*Switch3"* (see Fig. 41). The control signals for all IGBTs are adjusted in block "*Dead times*" to prevent a short-circuit. Dead times are realized by two D flip-flop circuits as depicted in Fig. 46 and the duration is derived from the clock signal.

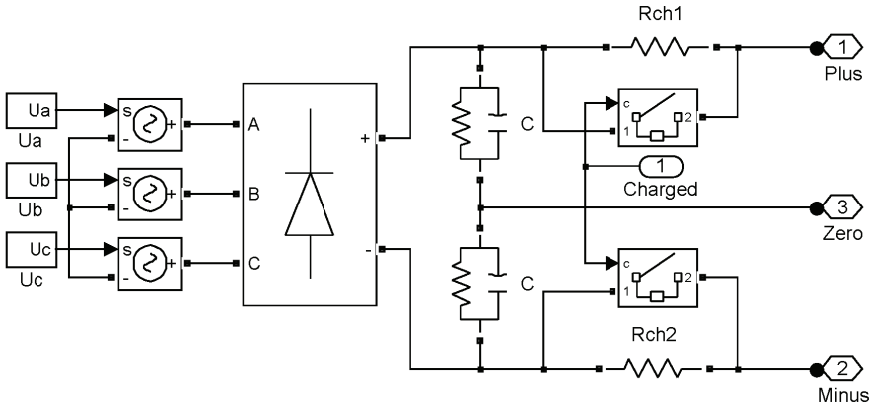


Fig. 42 The block "Supply and DC link": Symmetrical three-phase supply, diode rectifier, DC link and pre-charging– Simulink model

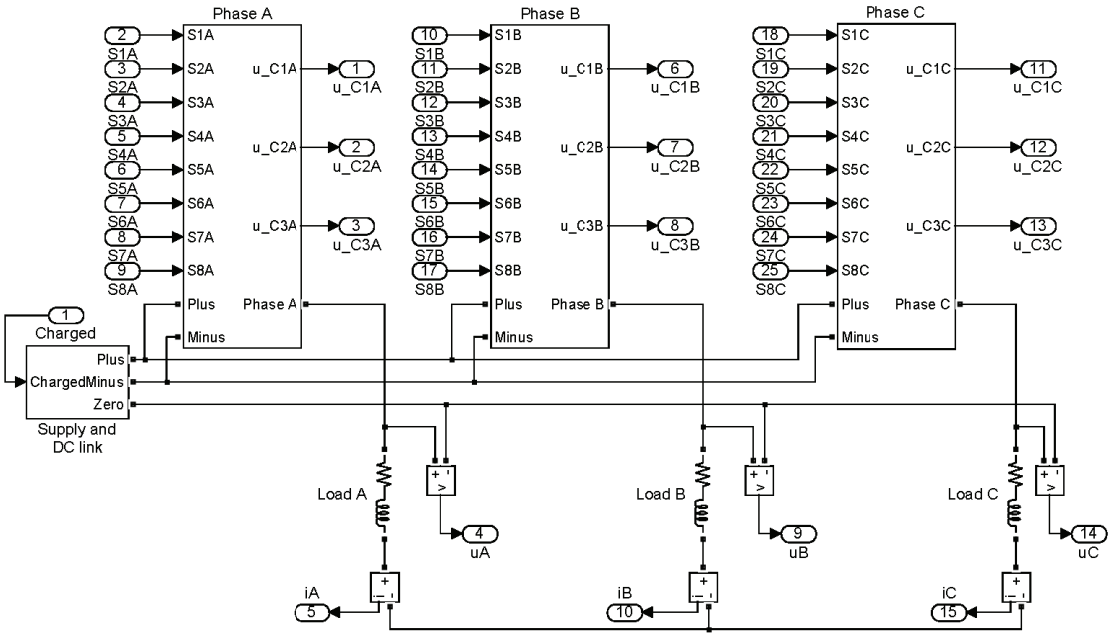


Fig. 43 The block "Power part": power part of a five-level FCI – Simulink model

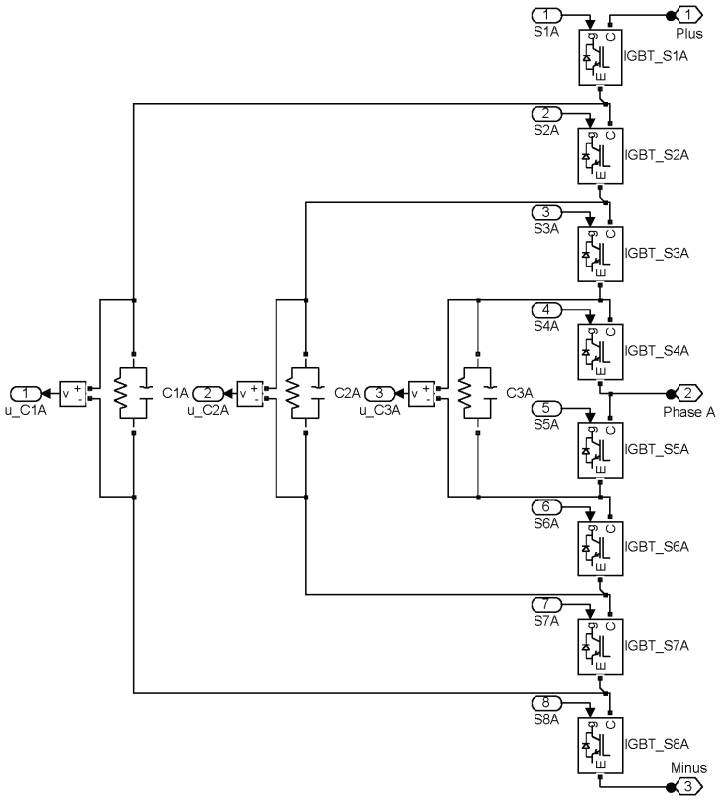


Fig. 44 The block "Phase A": one phase of a five-level FCI – Simulink model

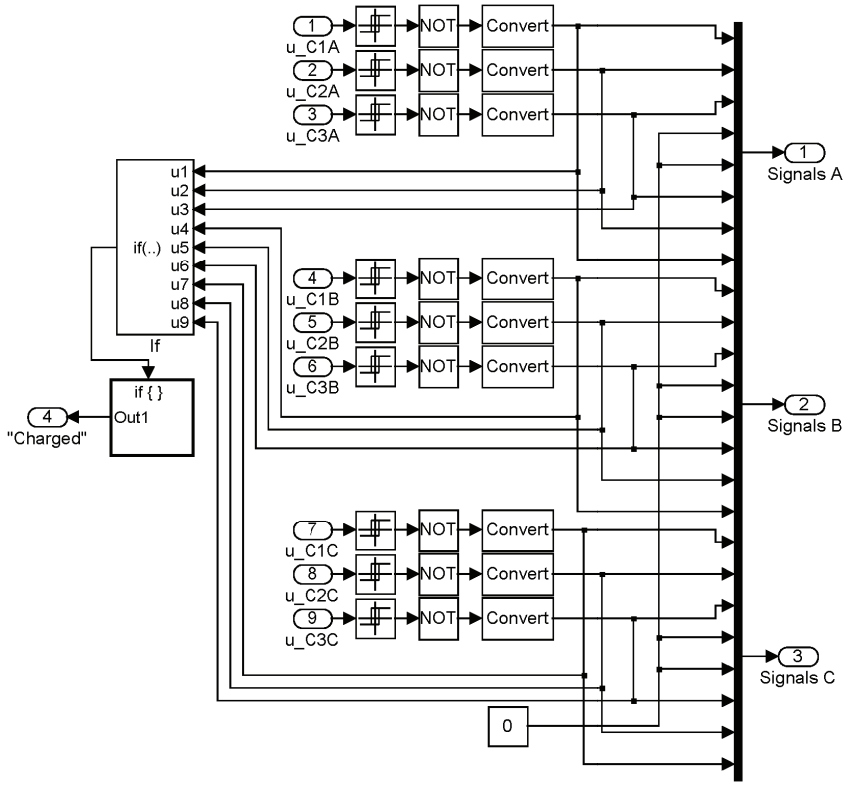


Fig. 45 Pre-charging logic in the block "Precharging"

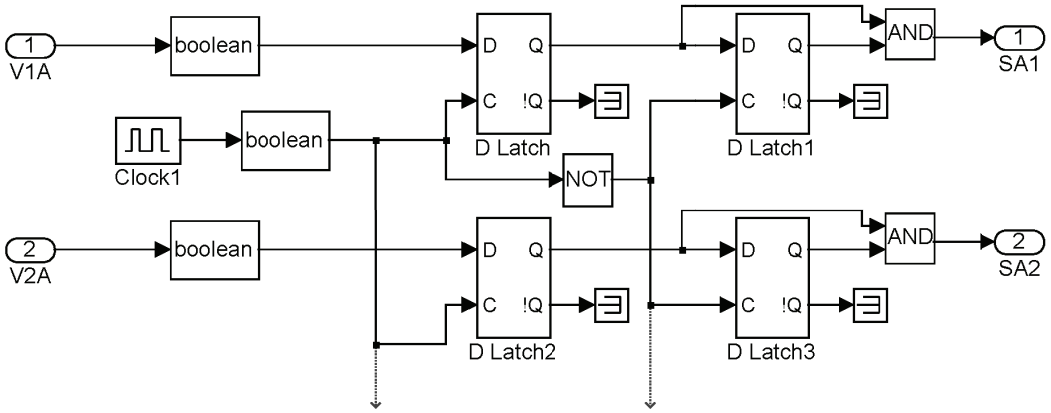


Fig. 46 The block "Dead times": Dead times generation made of two D flip-flop circuits

2.5.2 Control Part

The techniques of the carrier-based PWMs are described in chapter 2.2.2.2. The realization of a regular asymmetrically sampled PD modulation in Simulink can be seen in Fig. 47.

Realizations of other carrier-based PWMs are in Appendix C. There are two discrete-time integrators. The upper integrator generates ωt for sine waveforms, the lower one generates a periodic signal of the switching frequency for the look-up table "*Carrier generation*". The outputs of the block "*PWM*" are the signals for all the 12 complementary couples of IGBTs. These signals would be direct driver signals if no balancing algorithm was used. However, such an algorithm is used, so these signals are further processed in the blocks "*Desired level selection*" which is depicted in Fig. 48. Although, the blocks described in the following text concern the phase A, the same connections are valid for the two remaining phases B and C.

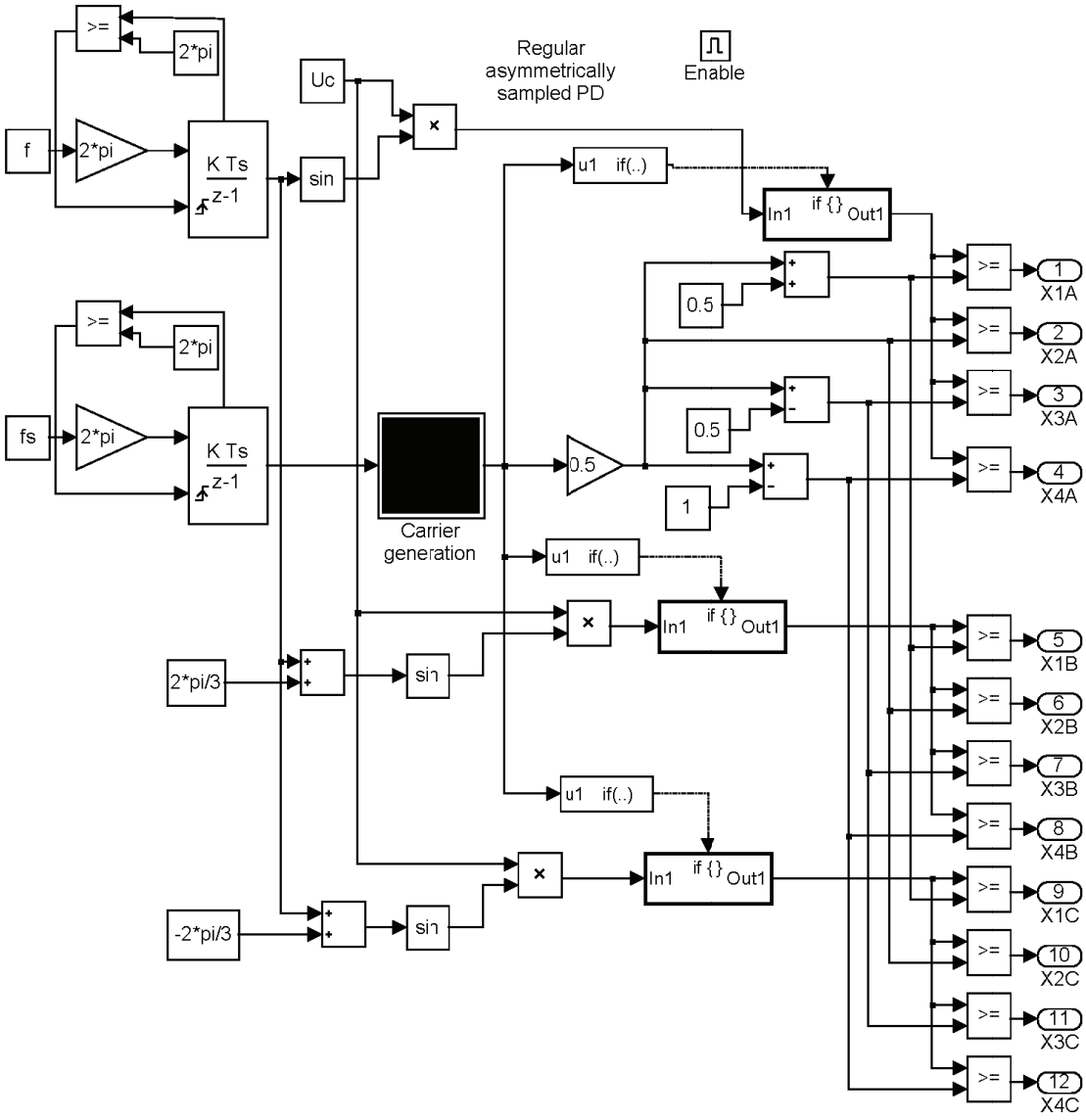


Fig. 47 The block "PWM": Regular asymmetrically sampled PD PWM for a five-level FCI

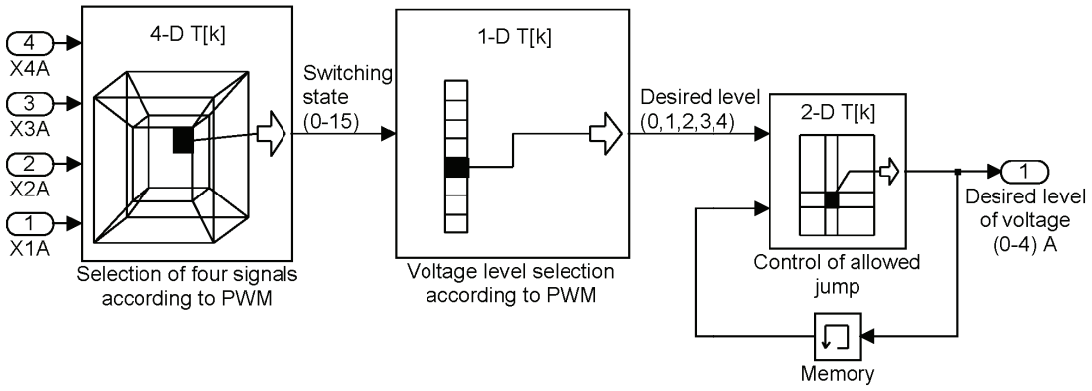


Fig. 48 The block "Desired level selection"

The algorithm of the desired voltage selection is based on selections from three look-up tables of different dimensions as can be seen in Fig. 48. The first 4D look-up table containing a 4D matrix "*signal_dle_PWM*"[1] transforms a foursome of signals from the "*PWM*" to one of the sixteen switching states according to Table 3. Because the look-up tables are zero indexed, the switching states have to be marked from 0 to 15. The number of the desired voltage level (0-4) is decoded from the number of the switching state in a one-dimensional look-up table with the matrix "*level-selection*". The last look-up table containing the matrix "*assurance*" is used in this algorithm just secure that the desired level always is the neighbouring one.

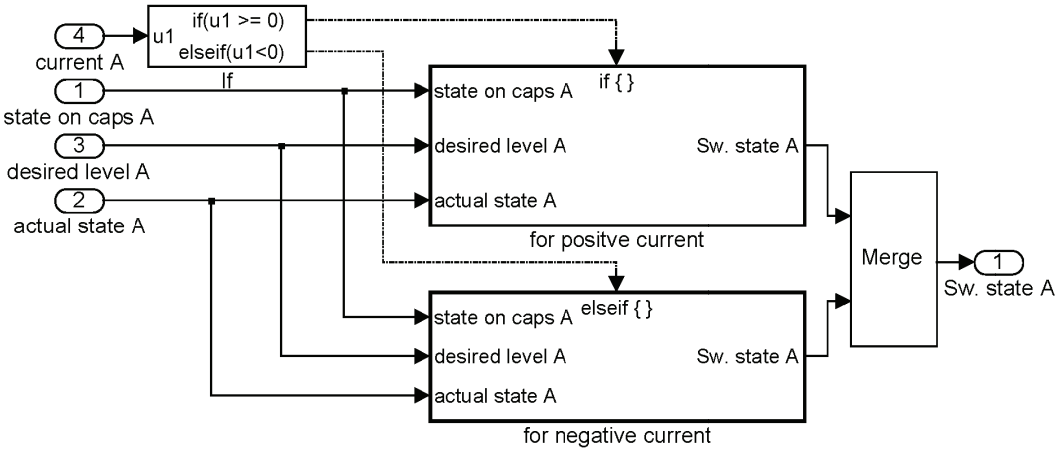


Fig. 49 The block"Switching state selection"

The selection of the most appropriate switching state is under way in the block "*Switching state selection*". There are two three-dimensional look-up tables, the first for the positive

[1] All matrices are stored on the enclosed data medium (Appendix A).

current direction with the matrix "*MATICE*", the second for the negative one with the matrix "*MATICE_m*". The outputs of this matrix would only be switching states in case there are just one or two flying capacitors in the inverter phase, thus, in the case of a three- or four-level FCI. Note that one of the three inputs is the "*state on caps A*" which carries the information about the actual situation across the flying capacitors in phase A. This information is gained from the block "*Evaluation of voltage across fl. caps A*", see Fig. 50, where polarities and absolute values of the relative voltage deviations are evaluated. The output numbers 0–5 indicate which one of the three flying capacitors has the maximum voltage deviation and what its polarity is. The actual values are described in more detail in Appendix A.

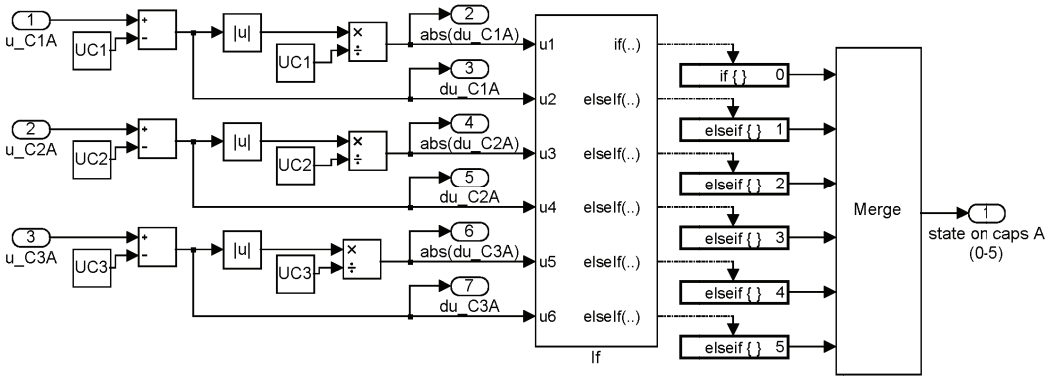


Fig. 50 The block "Evaluation of voltage across fl. caps A"

The block "*Applicable switching state A*", which is depicted in Fig. 51, serves for the selection of the final, applicable switching state. If anywhere across the flying capacitor the situation is detected that the capacitor with the biggest deviation would be charged or discharged, and there is the possibility to simultaneously improve the voltage across some other flying capacitor, the voltage relationships across the two remaining capacitors must be detected. The positive and the negative direction of the current have to be examined separately. An arrangement of blocks which evaluates the situation for the positive current is depicted in Fig. 52. According to the actual situation across all flying capacitors, appropriate "*If Action Subsystem*" is executed. The inner structure of the "*If Action Subsystem1*" from Fig. 52 can be seen in Fig. 53. The other blocks have similar structure. Only the 3D matrices of the 3D look-up tables are different, of course. For positive current, "*If Action Subsystem1*" contains the matrix "*MATICKAN*", "*If Action Subsystem2*" contains the matrix "*MATICKAO*" and "*If Action Subsystem3*" contains the matrix "*MATICKAP*". For negative current, "*If Action Subsystem1*" contains the matrix "*MATICKAN_m*", "*If Action Subsystem2*" contains the matrix "*MATICKAO_m*" and "*If Action Subsystem3*" contains the matrix "*MATICKAP_m*". All the matrices are also presented in Appendix A. The final control signal

sent to the IGBTs is decoded from the applicable switching state found in the 2D look-up table "*LUT A*" with the matrix "*m_sepnuti*". It is also stored by the memory block for the next simulation step as the actual switching state.

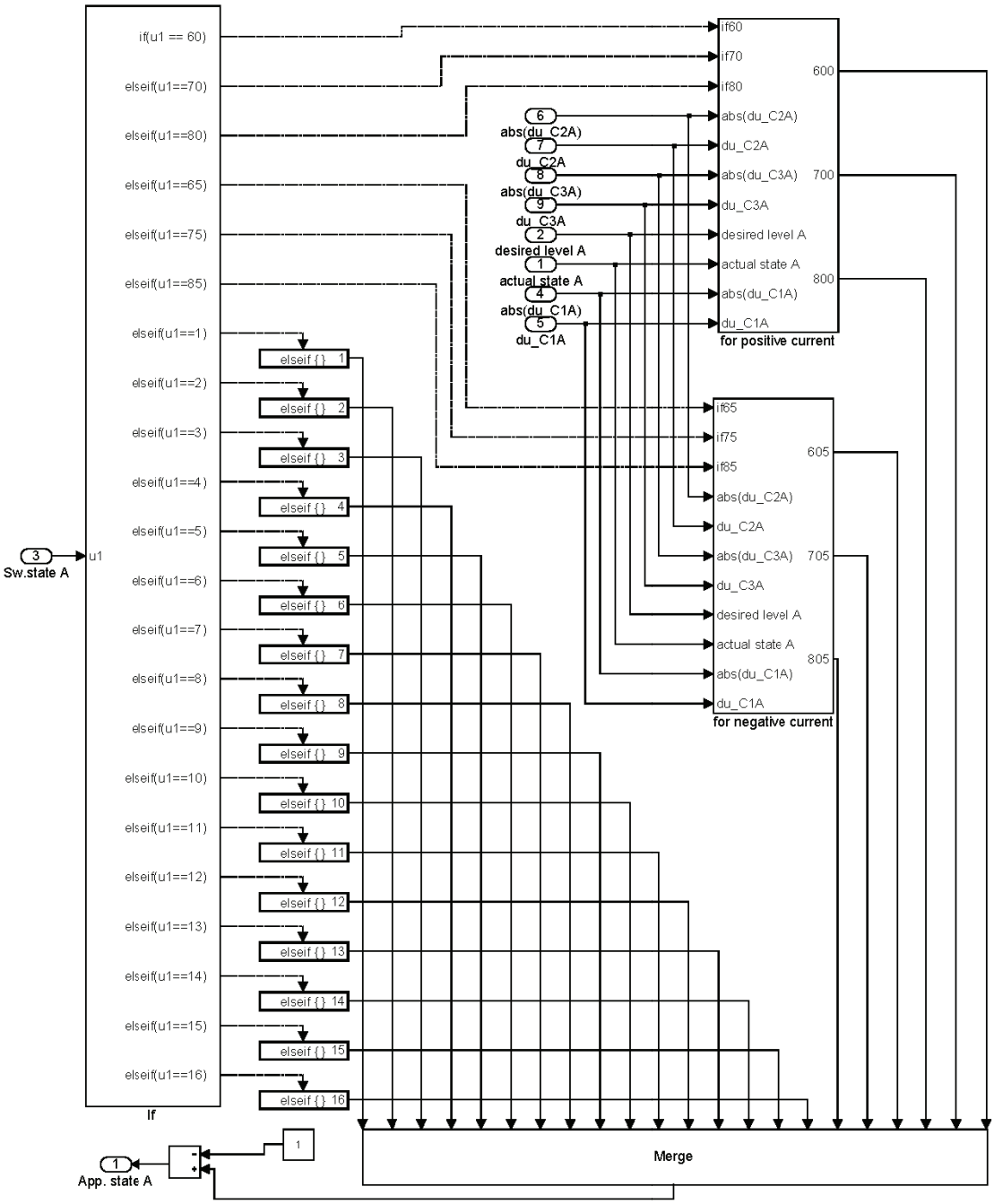


Fig. 51 The block "Applicable switching state A": selection of the final, applicable switching state

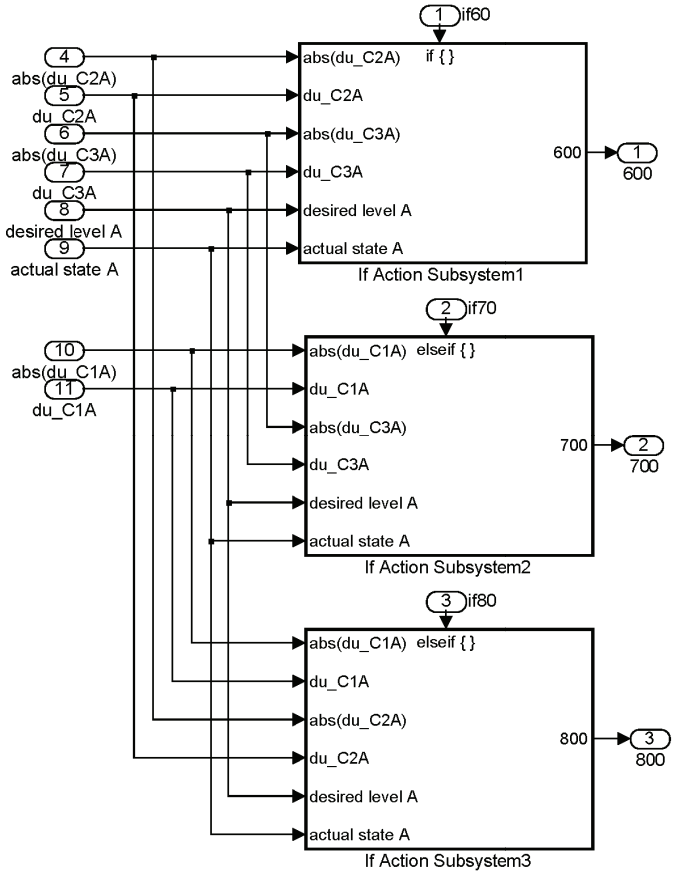


Fig. 52 The block "for positive current" of "Applicable switching state A"

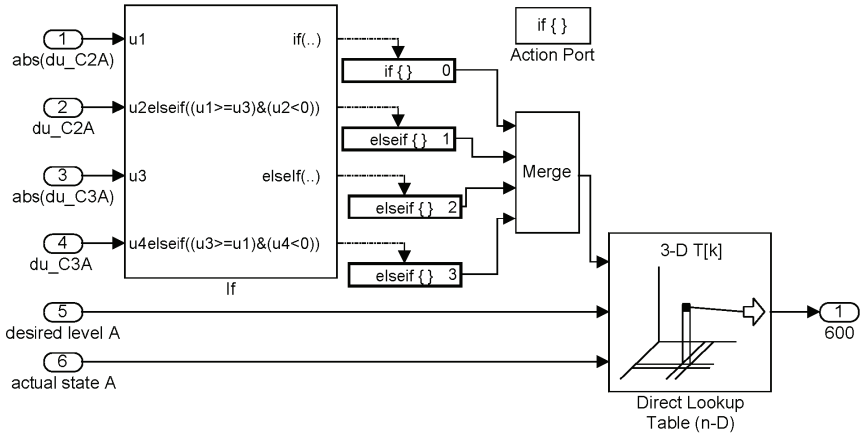


Fig. 53 "If Action Subsystem" for second detection of the voltage relations across the two remaining capacitors in case the flying capacitor C_{1A} has the biggest voltage deviation from its nominal value

2.5.3 Simulation Results

In this chapter simulation results of a three-phase five-level FCI for three different switching processes are presented. The model described in the previous chapter is used with the following parameters:

Three-phase power network and DC link:

U_a = 64 V ..... effective value of the line-to-line supply voltage (V_d = 150 V)

f_{net} = 50 Hz .....frequency of the supply voltage

C = 10 mF .....capacity of the capacitor in the DC link

R_c = 10 kΩ .....capacitors leakage

$R_{ch1} = R_{ch2}$ =25 Ω .....resistance of one pre-charging resistor

Five-level flying capacitor inverter:

f = 50 Hz .....nominal output frequency

f_s = 1250 Hz .....switching frequency

M = 0.95 .....modulation index

C_x = 1 mF.....capacity of each flying capacitor

V_{C1n} = 112.5 V.....nominal voltages of the flying capacitor C_1

V_{C2n} = 75 V.....nominal voltages of the flying capacitor C_2

V_{C3n} = 37.5 V.....nominal voltages of the flying capacitor C_3

R_c = 10 kΩ .....flying capacitor leakage

$t_{DT} = 2\,\mu$s .....dead time duration

regular asymmetrically sampled PD modulation according to chapters 2.2.2.2 and 2.2.2.3

voltage balancing method according to chapter 2.3.2

models of an ideal IGBTs

Load:

R_{Lx} = 20 Ω .....load resistance in one phase

L_{Lx} = 40 mH .....load inductance in one phase

The simulation step size is fixed – it is 1 μs because of the dead time simulation. However, the sample time correlates with one modulation cycle which takes 100 μs. The parameters were chosen with respect to the later comparison with the real FCMI prototype whose superior control system (dSpace) operates in steps of 50 μs integer multiples. An M-file for simulation with all the parameters is in Appendix B.

The start of the simulation is pictured in Fig. 54. It shows how the voltages across the flying capacitors increase. After the last flying capacitor in a phase is charged, the switching according to the modulation begins. While the inverter operates, the voltages across the flying capacitors are balanced.

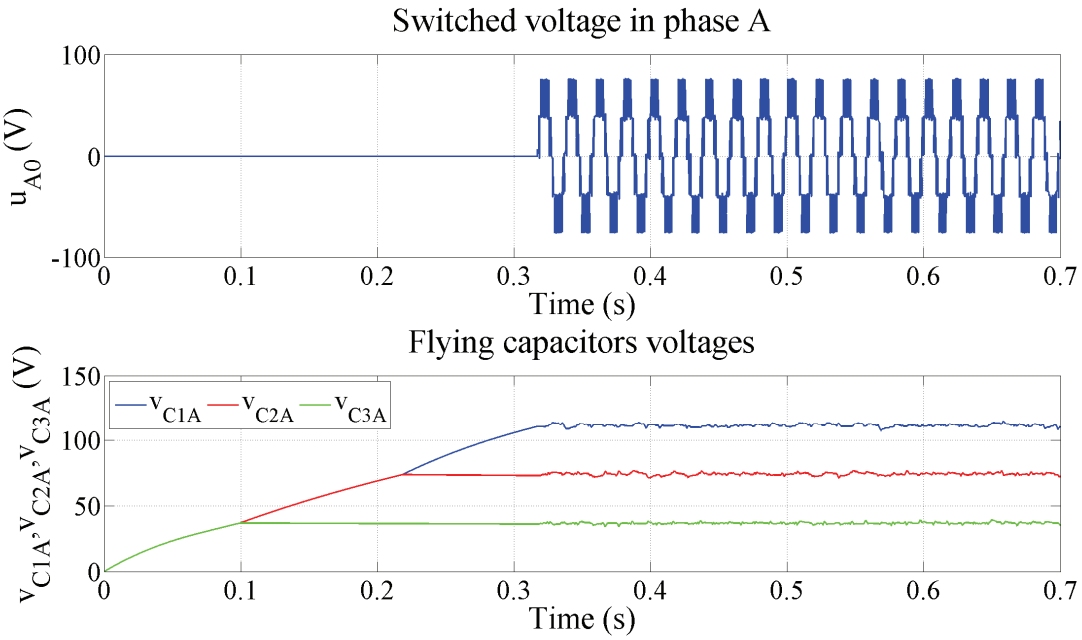


Fig. 54 Waveforms of voltages at the start of the simulation – pre-charging of flying capacitors

2.5.3.1 Simulation Results for 1C-transitions

A detail of two and a half periods of a switched five-level voltage is depicted in Fig. 55. The switching frequency of 1250 Hz is apparent as well as the 150 V in the DC link. From the switched voltage and its switching frequency follows that the switching process corresponds to the process of a 1C-transition described in chapter 2.4.2. A slight fluctuation of voltage levels can also be seen. It corresponds to the voltage ripple of the flying capacitors which can easily be seen in Fig. 56. The value of this ripple depends on the switching frequency, flowing current and capacity as stated in the equation (52). The fluctuation of outer levels depends on

the ripple of the voltage in the DC link. Waveforms of all three load currents are depicted in Fig. 57.

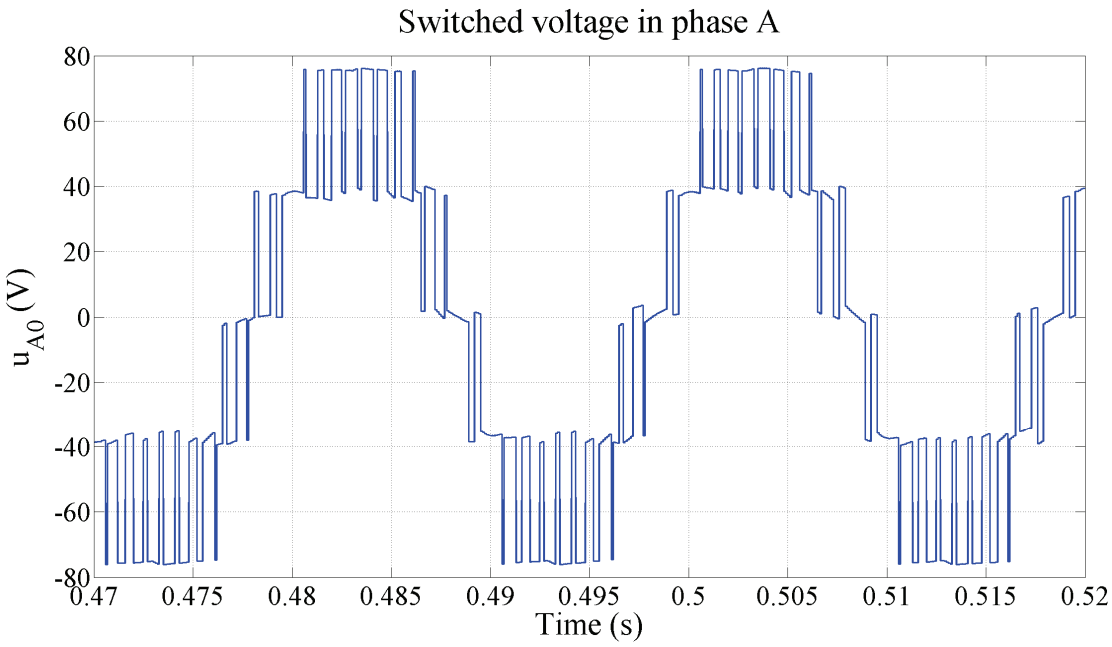


Fig. 55 Waveform of the inverter phase voltage (1C-transitions)

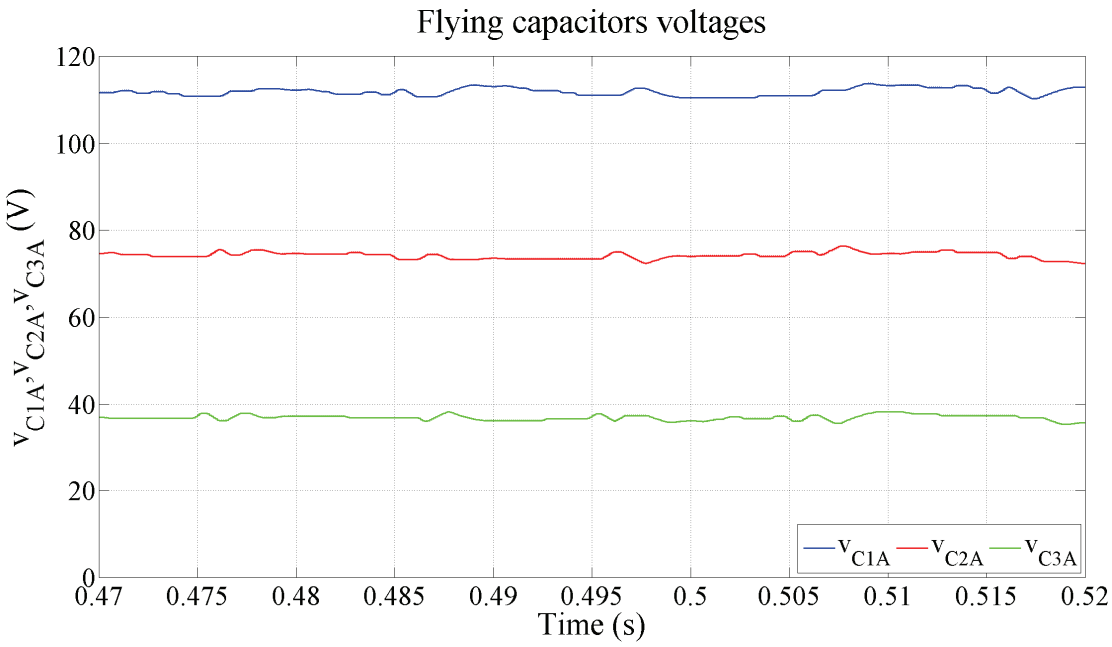


Fig. 56 A detail of voltages across the flying capacitors in phase A (1C-transitions)

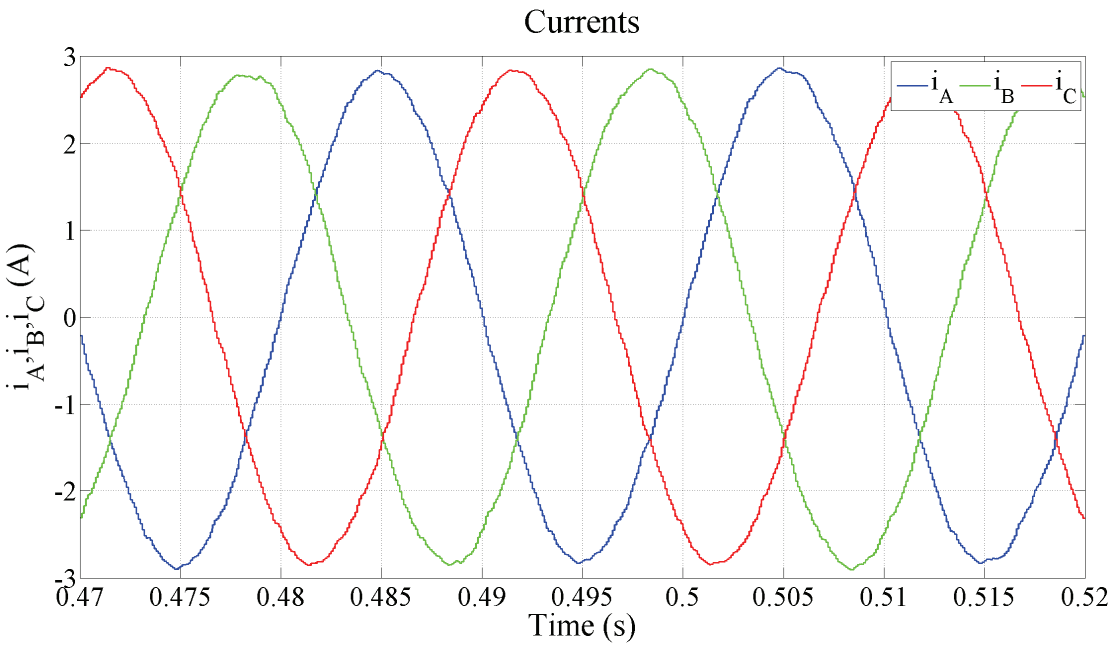


Fig. 57 Detail of load current waveforms (1C-transitions)

2.5.3.2 Simulation Results for 2C-transitions

The core of the 2C-transition is explained in chapter 2.4.3. It follows from the analysis performed there that the output voltage is switched by higher switching frequency than is required and that the stabilization across the flying capacitors is better than in the case of 1C-transition.

Both claims can be inferred from the following figures. In Fig. 58, the five-level inverter phase voltage is depicted in detail. In comparison with a 1C-transition (Fig. 55), the switching frequency of the voltage is much higher. According to the equation (52) the higher the switching frequency, the lower the voltage ripple across the capacitors. Fig. 59 confirms it. This can also be seen (with smaller fluctuations of voltage levels) in Fig. 58.

Waveforms of all the three load currents are presented in Fig. 60.

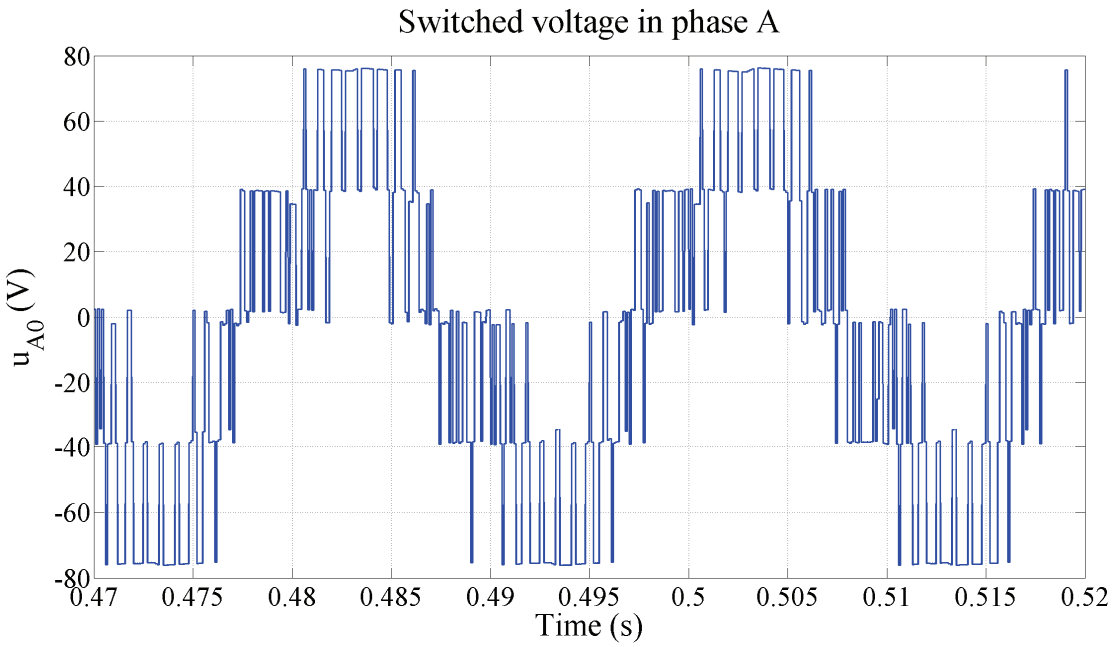


Fig. 58 Waveform of the inverter phase voltage (2C-transitions)

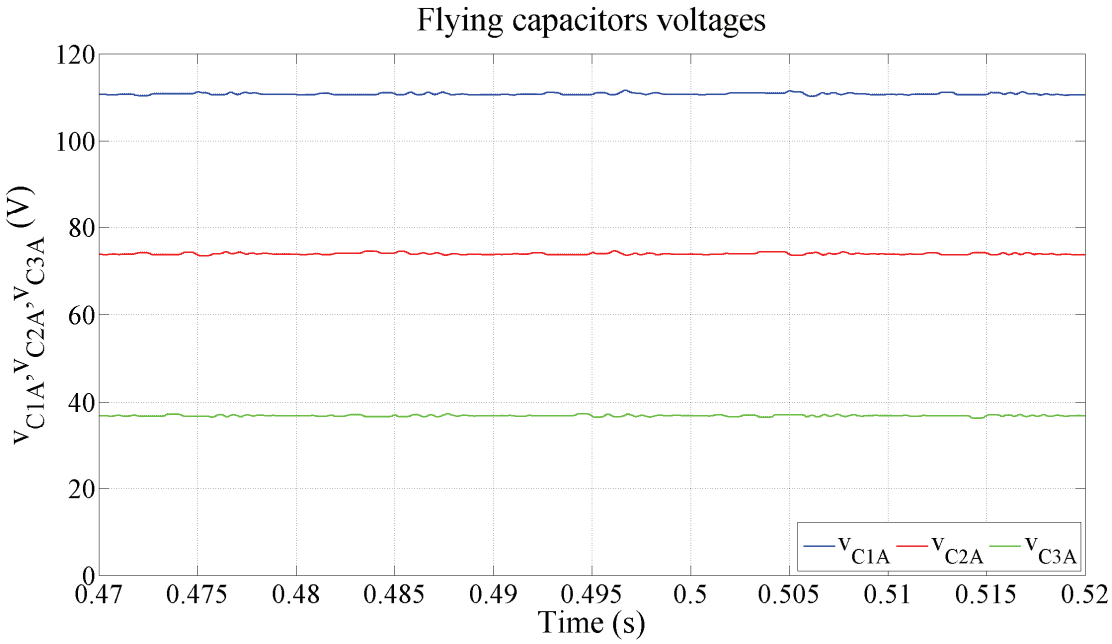


Fig. 59 A detail of the voltages across flying capacitors in phase A (2C-transitions)

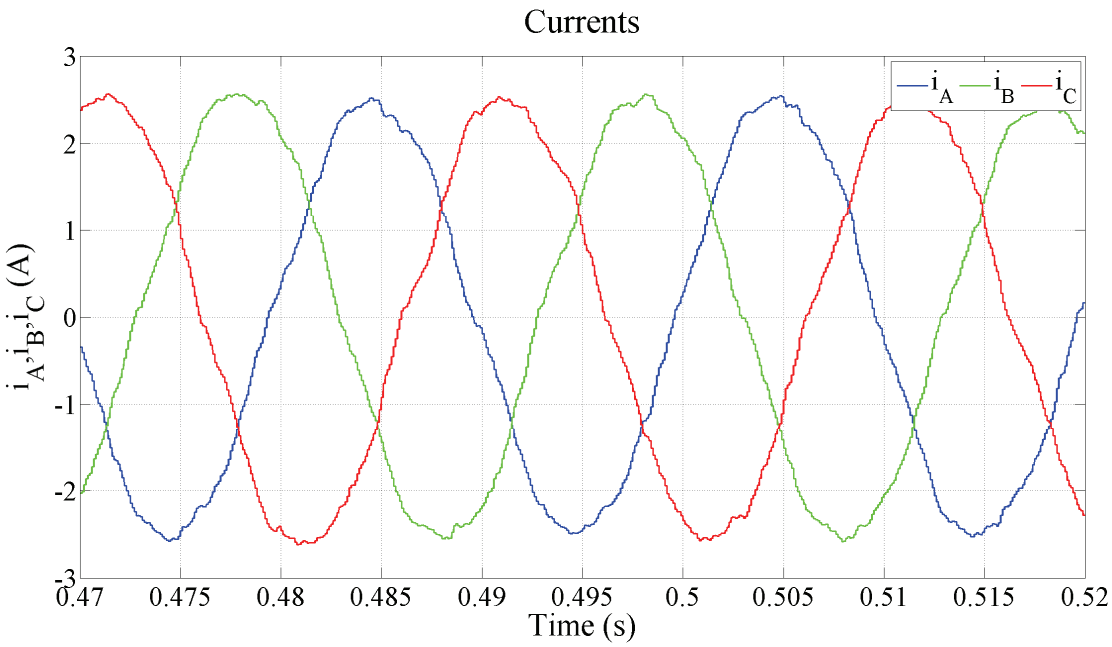


Fig. 60 A detail of load currents waveforms (2C-transitions)

2.5.3.3 Simulation Results for 3C-transitions

The explanation of the 3C-transition is presented in chapter 2.4.4. It follows from the analysis performed there that the change of the voltage level happens with a jump over two voltage levels. This is "forbidden" jump because of the very core of the MI.

The waveform of a five-level voltage is shown in Fig. 61. The "forbidden" transitions are clearly visible; nevertheless, they are depicted in Fig. 62 in detail. Fig. 63 shows the voltages across the flying capacitors. As is apparent at first sight, the voltage fluctuations are comparable with the ones occurring in 1C-transitions.

The waveforms of all three load currents are presented in Fig. 64.

2.5.3.4 Conclusion of This Chapter

The switching processes with different transitions have been simulated with the help of the three-phase five-level FCI model. As the simulation results show the theoretical assumptions regarding the influence of the transition type on the switching process are correct.

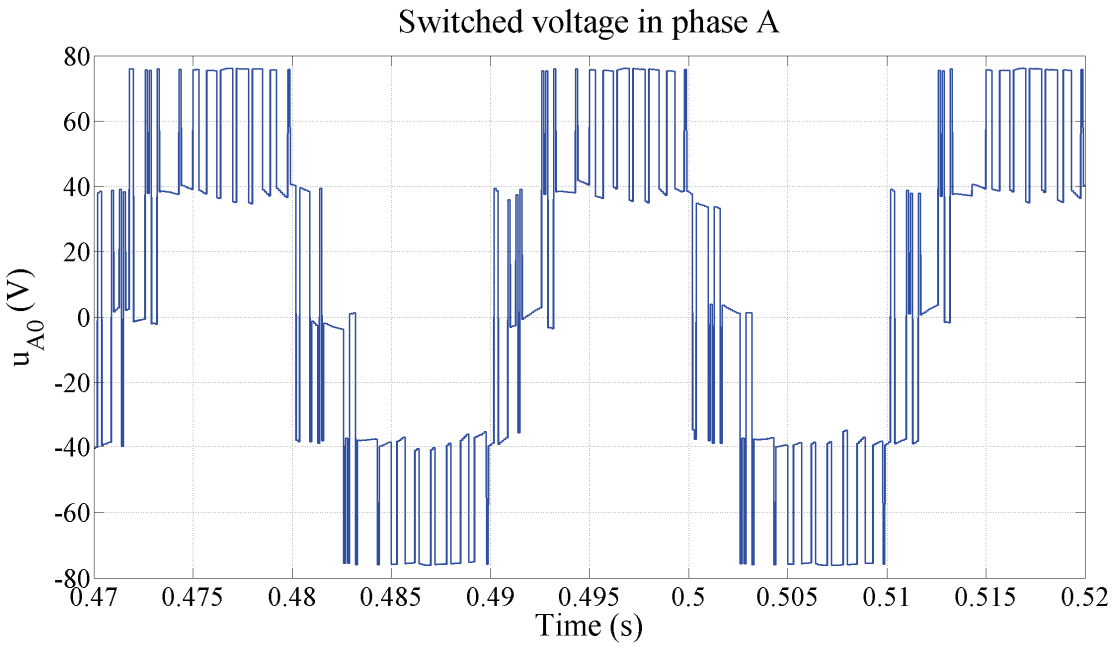


Fig. 61 Waveform of the inverter phase voltage (3C-transitions)

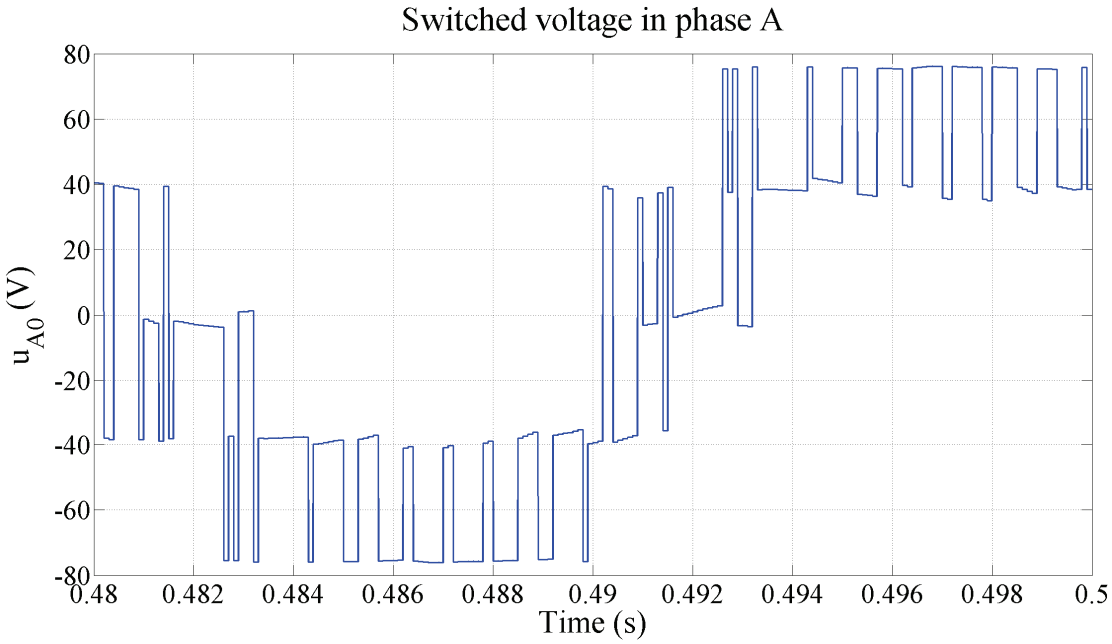


Fig. 62 A deatil of "forbidden" transitions

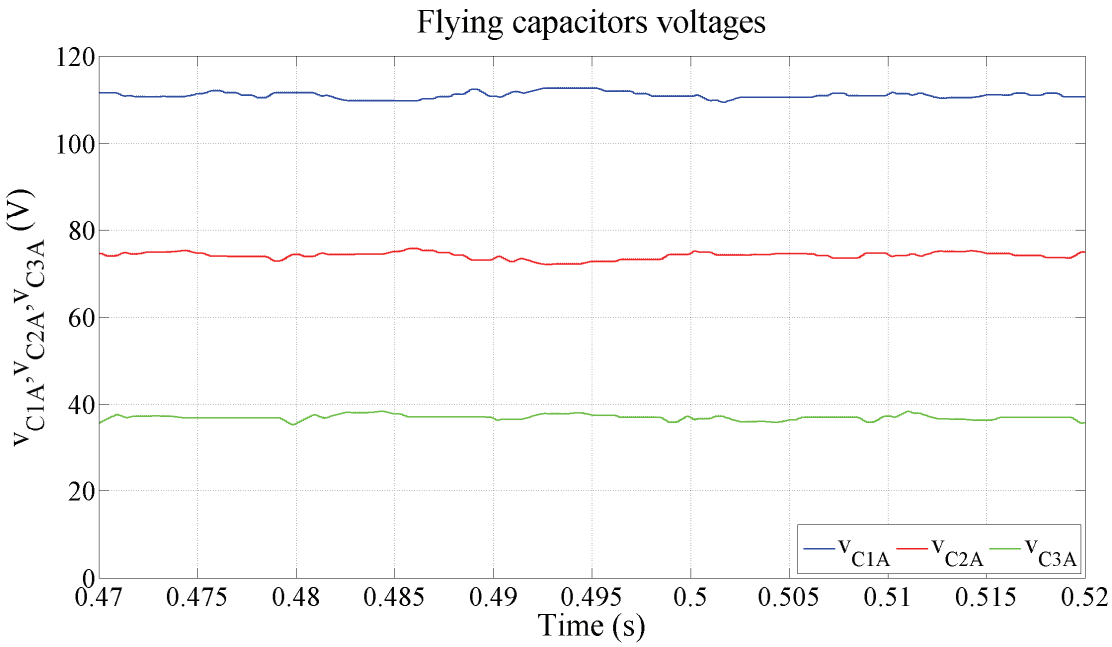


Fig. 63 A detail of voltages across the flying capacitors in phase A (3C-transitions)

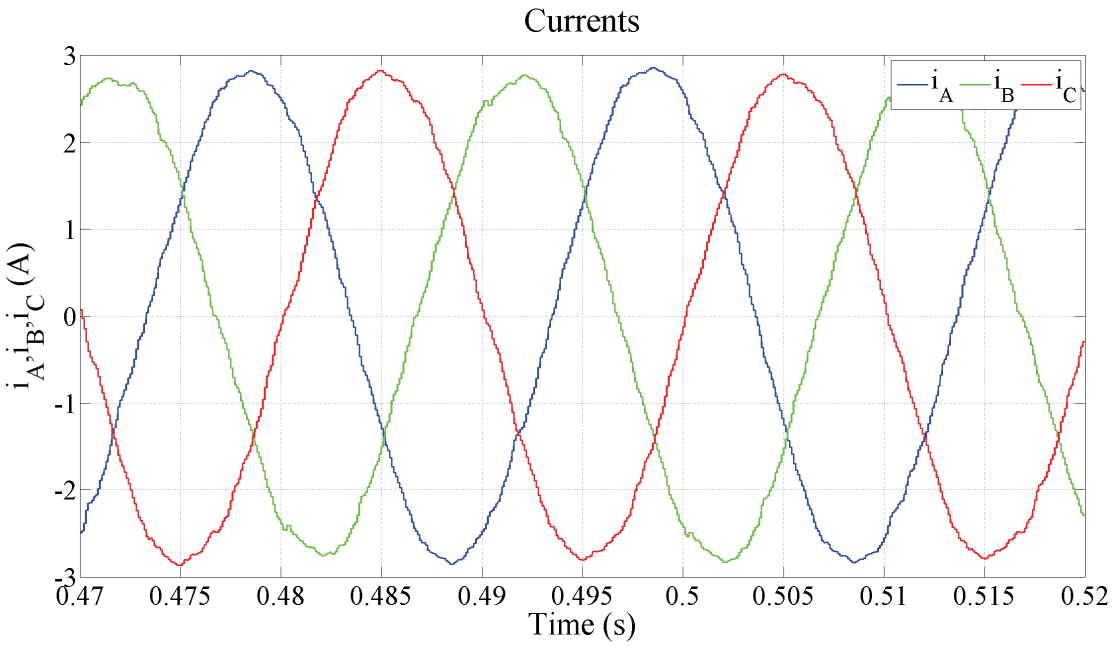


Fig. 64 Detail of load currents waveforms (3C-transitions)

3 The Possibility of Using a Multilevel Inverter as an Active Filter

3.1 The Principal Function of an Active Power Filter

The industry consumers of electrical power are very often supplied by static high power rectifiers and inverters. That means applications such as arc furnaces or e.g. high power adjustable speed drive systems such as magnetic levitation system for urban transport etc. All of these are non-linear loads (Grady *et al.*, 1990; Song *et al.*, 2001). A non-linear load consumes current of non-sinusoidal waveform. If the load consumes a non-sinusoidal current, the current harmonic pollution appears in the electrical network and it degrades the power quality (Song *et al.*, 2001). When it comes to the supply network there are two main ways how to avoid consuming of a non-sinusoidal current: passive and active filtration.

In case of passive filtration, the passive electrical elements (inductors and capacitors) are connected to a suitable point of the network and they are tuned on a particular frequency – this combination secures zero impedance for the currents of this frequency, so this frequency cannot appear in the supply network. However, their performance is limited less effectiveness and low dynamics. The active filtration eliminates harmonic distortion by introducing harmonics of opposite direction into the supply network. This injection is carried out by converters called active power filters, or simply active filters. Note that the terminology in relevant literature is not unified. The term “active power filter” would in fact very often be understood as “active power line conditioner”. An active line power conditioner also reduces the voltage and current distortion but, in addition, it also compensates the reactive power, reduces voltage spikes, transients and flicker (Grady *et al.*, 1990). In this Thesis the term active power filter only refers to the filter of harmonics.

As far as electrical circuit is concerned, the active filter is a three-phase voltage source inverter connected as depicted in Fig. 65. Because the inverter is a voltage source and it is connected to the net in the connection point A, the coupling reactors with inductance L_F must be interconnected between the active filter and the connection point as an impedance separation. For each phase, the inverter is controlled in such a way that it injects the current i_F of the desired value into the connection point before a non-linear load. The non-linear load injects the current i_L. It contains the characteristic harmonics. The current i_N, which should contain the first harmonic only, flows from the power network. The power network with supply voltage v_N is the source of the first (fundamental) harmonic only. The inductance L_N

represents the line inductance. A thyristor rectifier often serves as the non-linear load. It produces the characteristic harmonics, thus, harmonics of order ν:

$$\nu = 6k \pm 1; \quad k \in N^{+} \tag{59}$$

The inverter has to produce exactly these harmonics in the opposite phase.

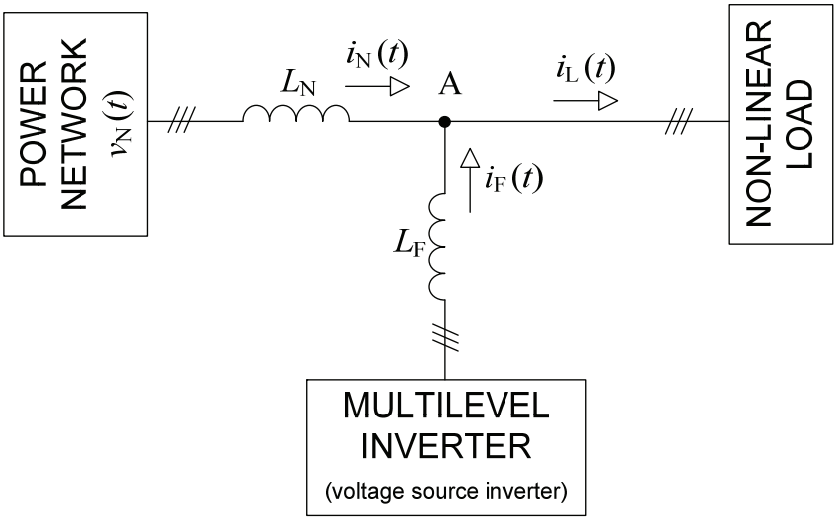


Fig. 65 Block scheme of an active power filter connection

For the currents in the circuit it is true that:

$$i_{\mathrm{L}}(t) = i_{\mathrm{N}}(t) + i_{\mathrm{F}}(t) \tag{60}$$

At the same time, it can be written for ν^{th} harmonic order that:

$$\begin{aligned} i_{\mathrm{L}\nu}(t) &= i_{\mathrm{N}\nu}(t); \quad \nu = 1 \\ i_{\mathrm{L}\nu}(t) &= i_{F\nu}(t); \quad \nu = 6k \pm 1; \quad k \in N^{+} \end{aligned} \tag{61}$$

Thus, the basic task of the control is to get the reference current waveform and switch it:

$$i_{F\nu}(t) = \sum_{\nu} i_{\mathrm{L}\nu}(t); \quad \nu = 6k \pm 1; \quad k \in N^{+} \tag{62}$$

The basic categories of the active filter control are mentioned in chapter 3.3.

3.2 Specific Requirements For Medium Voltage Inverter Operated as an Active Filter

The term medium voltage inverter refers to inverters that for supply of applications in the area above the power of megawatts. It could be generally said that it concerns voltages and currents above thousand volts and hundred amps (Rahimo, 2011). There are four basic requirements that need to be taken into consideration when an inverter for an active power filter is considered (Kobrle and Pavelka, 2012a; Kobrle and Pavelka, 2012b): topology, semiconductor devices, switching frequency and DC supply voltage.

3.2.1 Topology

The classical topology of a low voltage (LV) active filter differs from the MV topology in the interconnection of neutral points. The LV active filter operates with the interconnection of a neutral point and MV without it. The LV active filter requires special inverter topology; MV active filter can be realized with a standard three-phase inverter. In chapter 1.1 the notion was discussed and justified that the multilevel topology is the best and most modern option for MV and HV applications. Therefore, it is reasonable to focus exclusively on that. From now on the flying capacitor topology will be taken into consideration.

3.2.2 Semiconductor Devices

The main limiting parameter is traditionally the blocking voltage of the semiconductor devices that are being used. An overview of contemporary situation is presented in chapter 1.1 where GTO thyristors, IGBTs and IGCTs are discussed. As for energy balance two types of devices are taken into account: IGBTs and IGCTs. The switching-off process of the GTO thyristors requires about 20% of the turning-off power. The blocking voltages of both types are around 6 kV. It is worth noticing that in the case of IGBT it is not the switching device but the companion diode what is the limiting factor (Rahimo, 2011).

3.2.3 Switching Frequency

The non-linear load is a source of current harmonics (Fig. 65). The voltage source inverter operating as an active filter is a source of voltage harmonics. Therefore, some reactors have to be interconnected between the active filter and the network. The active filter has to be controlled to inject load current harmonics. The deciding factor of the upper filtered harmonics order is the switching frequency. Let us suppose the basic frequency is 50 Hz and

the signal filtering goes up to 13th harmonic. If we take into account that the usual frequency distance between the filtered harmonic and its carrier is about 5, we obtain the switching frequency f_s which we are possible to switch the 13th harmonic with:

$$f_s = 50 \cdot 13 \cdot 5 = 3250\,\text{Hz} \tag{63}$$

However, at least a twofold higher frequency is the minimal theoretically possible frequency according to the Shannon-Kotelnikov theorem, thus

$$f_{s\,\min} = 50 \cdot 13 \cdot 2 = 1300\,\text{Hz} \tag{64}$$

Let us look at possible switching frequencies of the MV semiconductor devices. Rahimo (2011) states that the maximum switching frequency of IGCTs comes up to 1000 Hz as depicted in Fig. 66.

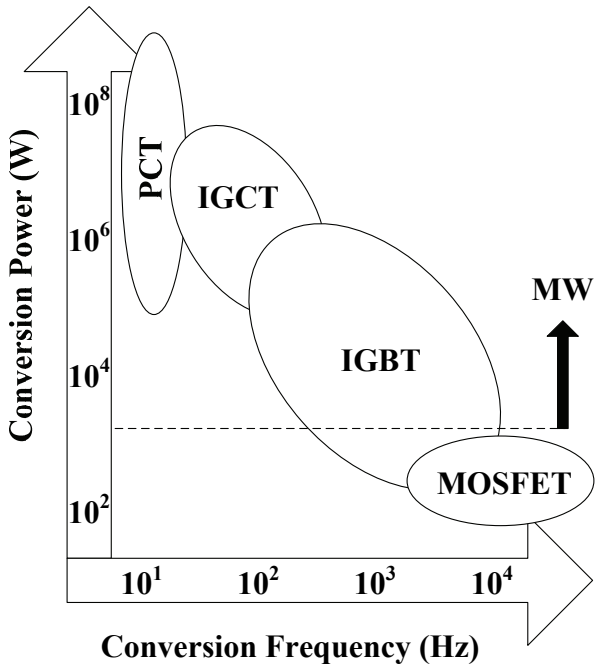


Fig. 66 The dependency of the output power on the switching frequency for switched-off devices (Rahimo, 2011)

Therefore, the IGCTs are not suitable for MV active filters. The achievable switching frequency of IGBT modules is in a different order of magnitude – in kHz. Therefore, only IGBT modules can be used for MV active filters.

3.2.4 The Supply Voltage of a Multilevel Inverter DC link

There is described in details in chapter 2.2.2.4 how the modulation index of the fundamental harmonic can be increased about 15% by an appropriate injection of third harmonic. However, the proper elimination of harmonics requires the higher voltage in the DC link as shown in this chapter.

According to Fig. 65, the active filter supplies currents $i_{\mathrm{F}}(t)$ to the connection point A for the elimination of harmonic currents in the power network. As mentioned above, if the active filter in Fig. 65 is realized by an inverter of voltage type then it operates as a voltage source inverter. In this case, coupling reactors with the inductivity L_{F} must be interconnected between the active filter and network in each phase. Let us assume the pure inductivity without resistance for following consideration. Equation (65) describes the relation between the output phase voltage of ν-order harmonic $v_{\mathrm{F}\nu}(t)$ and the output filter current $i_{\mathrm{F}\nu}(t)$:

$$v_{\mathrm{F}\nu}(t) = j2\pi f_1 \nu L_{\mathrm{F}} i_{\mathrm{F}\nu}(t) = j\nu X_{\mathrm{F}} i_{\mathrm{F}\nu}(t) \tag{65}$$

where f_1 is the fundamental frequency (first harmonic) and X_{F} the reactance of coupling reactor. If the sinusoidal waveforms are considered, it can be written:

$$V_{\max \mathrm{F}\nu} \sin(\nu\omega t) = -\nu X_{\mathrm{F}} I_{\max \mathrm{F}\nu} \cos(\nu\omega t) \tag{66}$$

The relation between the amplitude of the ν-order harmonic and the amplitude of the fundamental component is (Pavelka and Čeřovský, 2002):

$$I_{\max \mathrm{F}\nu} = \frac{I_{\max \mathrm{F1}}}{\nu} \tag{67}$$

Hence, the equation (66) can be re-written as:

$$V_{\max \mathrm{F}\nu} \sin(\nu\omega t) = -X_{\mathrm{F}} I_{\max \mathrm{F1}} \cos(\nu\omega t) \tag{68}$$

For better comparisons and image, this can be transformed into per units (p.u.):

$$v_{\max F\nu}^{\text{p.u.}} \sin(\nu\omega t) = -x_F i_{\max F1}^{\text{p.u.}} \cos(\nu\omega t) \tag{69}$$

Equation (69) describes the relation between the instantaneous values voltage and current of each harmonic across the coupling reactor. However, for the thinking about the voltage in the DC link, the maximal values are important. Thus, it can be written for them:

$$v_{\max F\nu}^{\text{p.u.}} = x_F i_{\max F1}^{\text{p.u.}} \tag{70}$$

The voltage to be switched by a MI comprises of the sum of all n harmonic components to be eliminated. In addition its instantaneous values also have to be summed with the instantaneous values of the supply phase voltage $v_N(t)$, therefore the fundamental current harmonic cannot appear on the filter coupling reactor. Therefore, the inverter has to switch also the fundamental voltage harmonic. Hence, the reference voltage $v_{ref}(t)$ in one phase can be written as:

$$v_{ref}(t) = v_N(t) + \sum_{\nu}^{n} v_{ref\,\nu}(t) \tag{71}$$

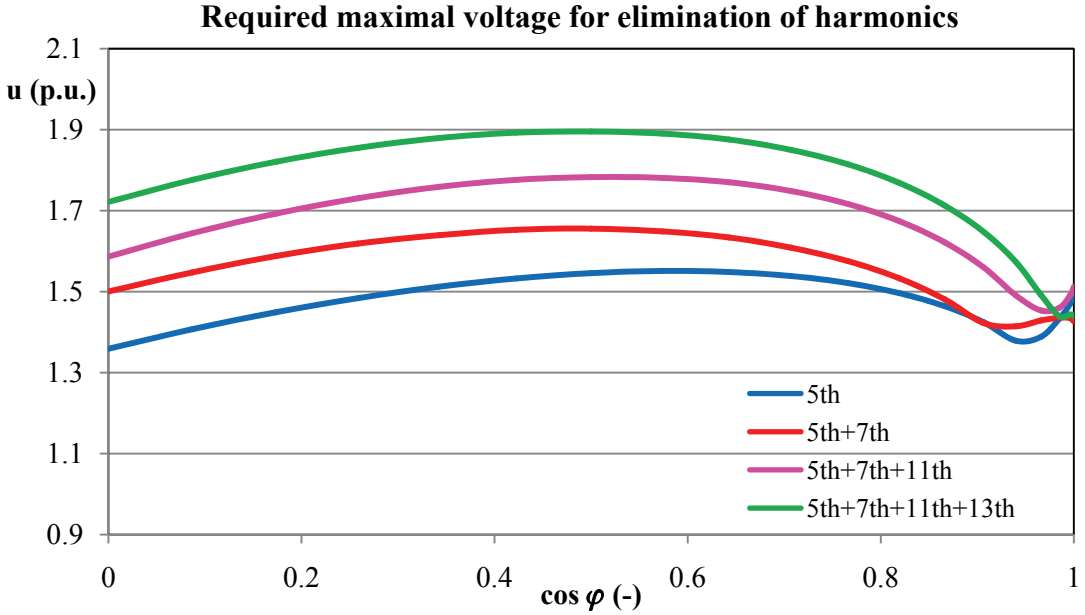


Fig. 67 Required maximal voltage for elimination of different orders harmonics for x_F=10%

The value of the reactance x_F in p.u. is between 5% and 10% of the inverter nominal impedance. According to equation (71), the sum of voltages in instantaneous values determinates the needed maximal value of output inverter voltage. This maximal needed voltage depends also on the phase shift φ between voltage and current of the fundamental harmonic in power line. In Fig. 67, the maximal needed voltages for elimination of different order current harmonics by consumption of nominal current are drawn. They are stated in p.u. as functions of cos φ for x_F = 10 %.

3.3 Possible Control Algorithm of the Flying Capacitor Multilevel Active Power Filter

The control algorithm of flying capacitor multilevel active power filter can be divided into three main parts: formation of a reference waveform, flying capacitors voltage balancing and DC link capacitor voltage balancing. The formation of a reference waveform is usually done in the same way as in the case of a classical two-level active power filter. The control algorithm for flying capacitor voltage balancing does not depend on its use. The voltage across the DC link capacitor will be – for the purposes of this Thesis – constant as this issue was not the subject of our research and it was not solved.

In order to operate an active filter correctly it is necessary to determine the reference current waveforms that should be added to the currents of the non-linear load so that the harmonics could be eliminated. Basically there are two ways how to do it: computation in the time-domain and computation in the frequency-domain.

The computation in time-domain is based on the principle of keeping instantaneous current within a reasonable tolerance of a sinusoidal waveform. An instantaneous error function is computed on-line and it can be e.g. the difference between actual and reference waveform. It means that the fundamental component $f_1(t)$ at 50 Hz of the distorted waveform $f(t)$ is extracted by a 50 Hz filter and the extracted error $e(t)$ is then $e(t) = f(t) - f_1(t)$ (Grady *et al.*, 1990).

The computation in frequency-domain is based on the transformation of periodic distorted waveforms into the frequency-domain and back. The measured phase current continuous signals are transformed into digital signals in the A/D converter. The finite number of quantities for one base period is a result of this transformation and can be stored in a processor memory as a digital representation of one period of the current waveform. This

representation can be transformed into a frequency domain using the Fourier analysis. The output of the Fourier analysis is a complex number for each harmonic. The filtered current harmonics are transformed back into the time domain and into the reference voltage signal for the next period. That implies that the filter process is delayed by at least two basic periods which is the main disadvantage of this method.

Let us go on with the frequency-domain computation. Thanks to the Fourier analysis the reference current waveform is obtained. However, the FCMI is a voltage source inverter, so it is necessary either to use the hysteresis current controller or to re-calculate the reference voltage waveform for PWM modulator. The voltage $v_{\mathrm{ref}}(t)$ corresponding to the desired current $i_{\mathrm{ref}}(t)$ can be calculated from the individual current harmonics components similarly as in equation (65). However, the coupling reactor has in fact both an inductance L_{F} with a resistance R_{F}. Then, the reference voltage can be written as:

$$v_{\mathrm{ref\,v}}(t) = \left(j2\pi f_1 \nu L_{\mathrm{F}} + R_{\mathrm{F}}\right) i_{\mathrm{ref\,v}}(t) \tag{72}$$

As can be seen from the equation (72) the reference voltage depends on the parameters of the coupling choke and its resistance. This poses a problem because the resistance can change during the operation and even a small change can change the reference voltage noticeably.

As mentioned in the previous chapter and as can be seen from equation (71), the reference voltage $v_{\mathrm{ref}}(t)$ is necessary to be produced at the output of a MI. It is possible to switch it by the PWM as described in chapter 2.2.2.3 because the balancing algorithm of the FCMI does not depend on the shape of a reference waveform. This method of reference voltage creation is a direct method without any feedback loop, it is very sensitive to change of parameters and it counts with the operation in a steady state.

Nevertheless, there is much better and much more broadened method: to use the control loop with feedback and control thus the switched current with a multilevel hysteresis current controller. The main principle of this method is explained and described in chapter 2.2.4.2. The desired currents are directly injected into the connection point via the coupling reactors, so that the switched harmonics are “sniffed out” by the filter and they do not get into the power network.

3.4 The Simulation Model of a Multilevel Active Filter

The simulation model of five-level FCI is performed in chapter 2.5. Based on this, the simulation model of multilevel active filter with five-level FCI was created also in program Matlab-Simulink. General view of the system model is in Fig. 68

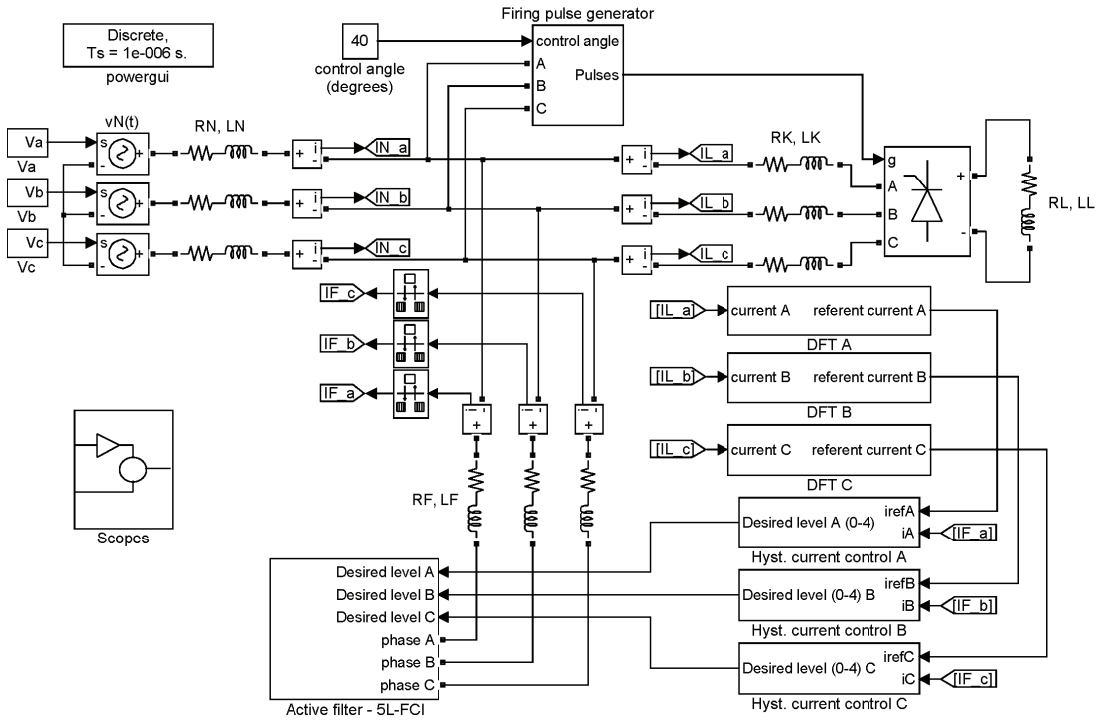


Fig. 68 General view of a multilevel active filter - Simulink model

The simulated power circuit corresponds to the scheme in Fig. 65. In addition, the resistances of reactors and power line are taken into consideration. Thyristor rectifier, which is connected over commutation reactors and operates with RL passive load on DC side, serves as a source of current harmonics. The block "*Active filter – 5L-FCI*" contains the model of the five-level FCI which is described in chapter 2.5. There are only two differences: the first, the inverter is supplied from constant voltage in DC link, the second, the hysteresis current control is used, so the blocks "*PWM*" and "*Desired level selection*" in Fig. 41 are extracted.

The connection of blocks with hysteresis current control is apparent also from Fig. 68. Their inputs are reference current and real current (as the feedback) of each phase, output is desired voltage level. The reference currents are calculated in blocks "*DFT X*" by Discrete Fourier Transformation, as described the in chapter 3.3, for each phase separately. Into the blocks "*Hyst. current control X*" is implemented the algorithm from chapter 2.2.4.2 (Fig. 30),

however, a little bit modified. The change lies in dividing of inner band B into two separate bands. Thus, eight bands and seven boundaries are established. Its inner structure can be seen in Fig. 69. The realization of stated algorithm consists of several steps. First – identification of band where is located the actual current error, second – identification if and which boundary has just been crossing, third – evaluation if one voltage level should be added or subtracted (Fig. 70). The resulting desired voltage levels enter then the voltage balancing algorithm in the same way as described in chapter 2.5.2.

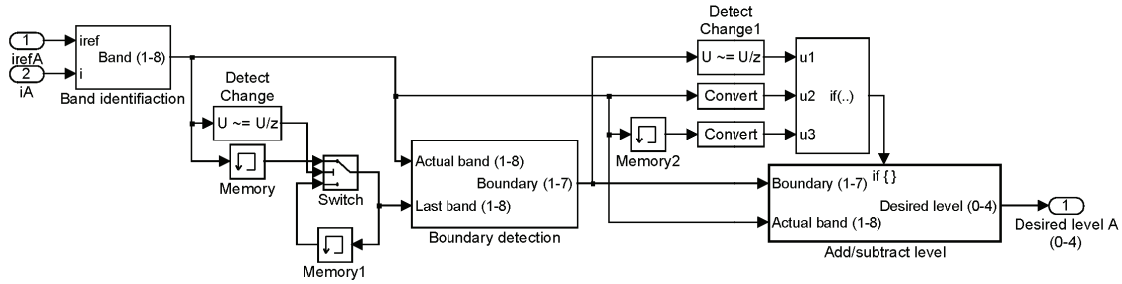


Fig. 69 Inner structure of the block "Hyst. current control A"

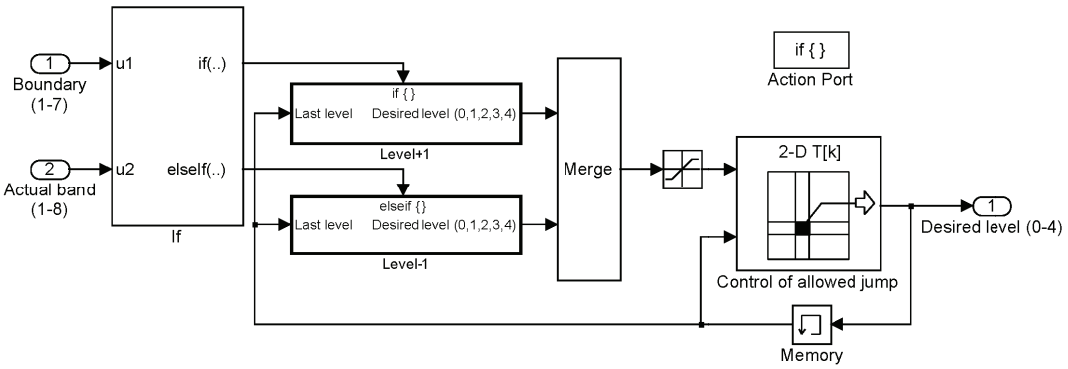


Fig. 70 Inner structure of the block "Add/subtract level"

3.5 Simulation Results

In this chapter the simulation results of multilevel active filter are presented. We use the model described in previous chapter with the following parameters (unless otherwise stated):

Three-phase power network:

v_N = 230 V.....effective value of phase voltage

f = 50 Hz .....frequency of the supplied voltage

R_N = 1 mΩ .....power line resistance of one phase

$L_N = 10\,\mu H$ .....power line inductance of one phase

Multilevel active filter:

$V_d = 800$ V.....voltage in the DC link

$V_{C1n} = 600$ V.....nominal voltages of the flying capacitor C_1

$V_{C2n} = 400$ V.....nominal voltages of the flying capacitor C_2

$V_{C3n} = 200$ V.....nominal voltages of the flying capacitor C_3

$C_x = 1$ mF .....capacity of each flying capacitor

$R_F = 50$ mΩ .....resistance of the coupling reactor in one phase

$L_F = 10$ mH .....inductance of the coupling reactor in one phase

$f_s = 1480$ Hz .....average switching frequency

multilevel hysteresis current control according to chapter 2.2.4.2

voltage balancing method according to chapter 2.3.2

Non-linear load:

$R_K = 30$ mΩ .....resistance of one commutation reactor

$L_K = 3$ mH .....inductance of one commutation reactor

$R_L = 30$ Ω .....load resistance

$L_L = 5$ mH .....load inductance

$\alpha = 0° - 90°$ .....control angle of the thyristor rectifier

Discrete Fourier transformation and solver options:

$NF = 2^9$ .....number of samples (elements of Fourier series)

5^{th}, 7^{th}, 11^{th}, 13^{th} .....filtered harmonics

$T_{samp} = 39.0625\,\mu s$.....sampling period, $T_{samp} = 1/(f \times NF)$

$T_{simul} = T_{samp}/20$ .....simulation step size (fixed)

The parameters of load and supply were chosen according to (Bůbela, 1996). M-file for simulation with all parameters is in Appendix B.

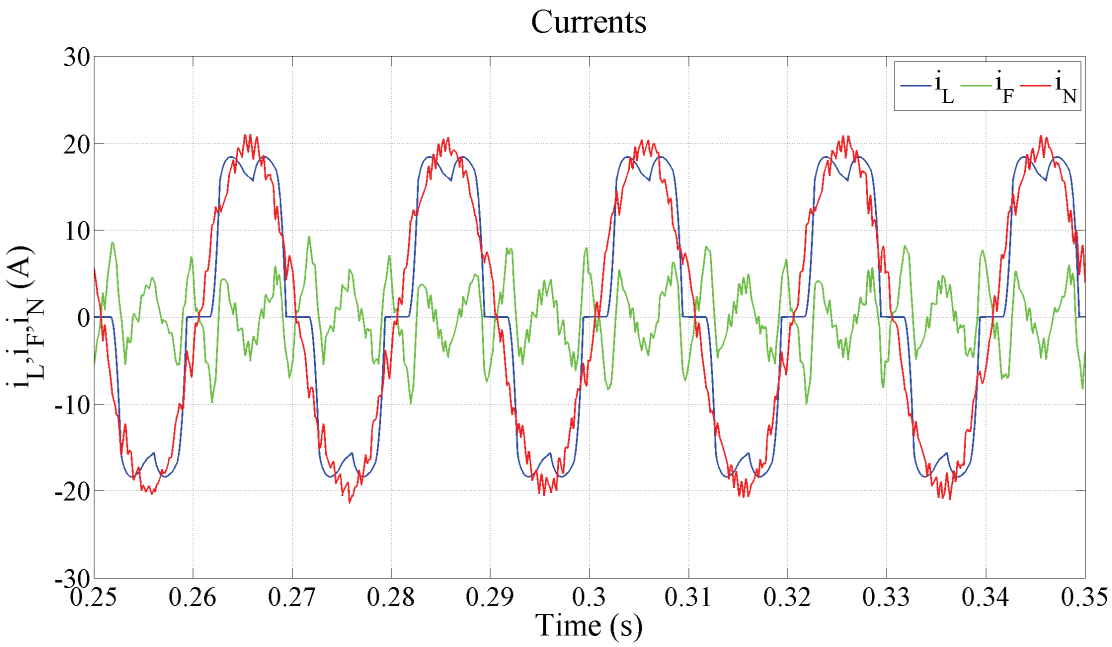


Fig. 71 Current waveforms ($\alpha = 0°$)

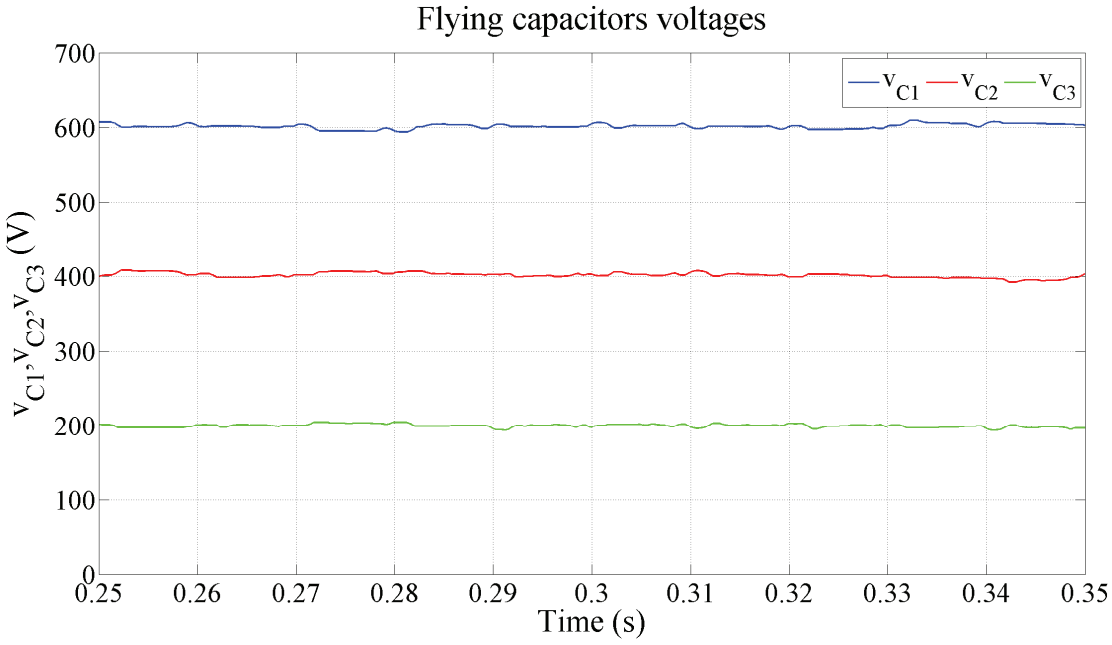


Fig. 72 Voltages across the flying capacitors ($\alpha = 0°$)

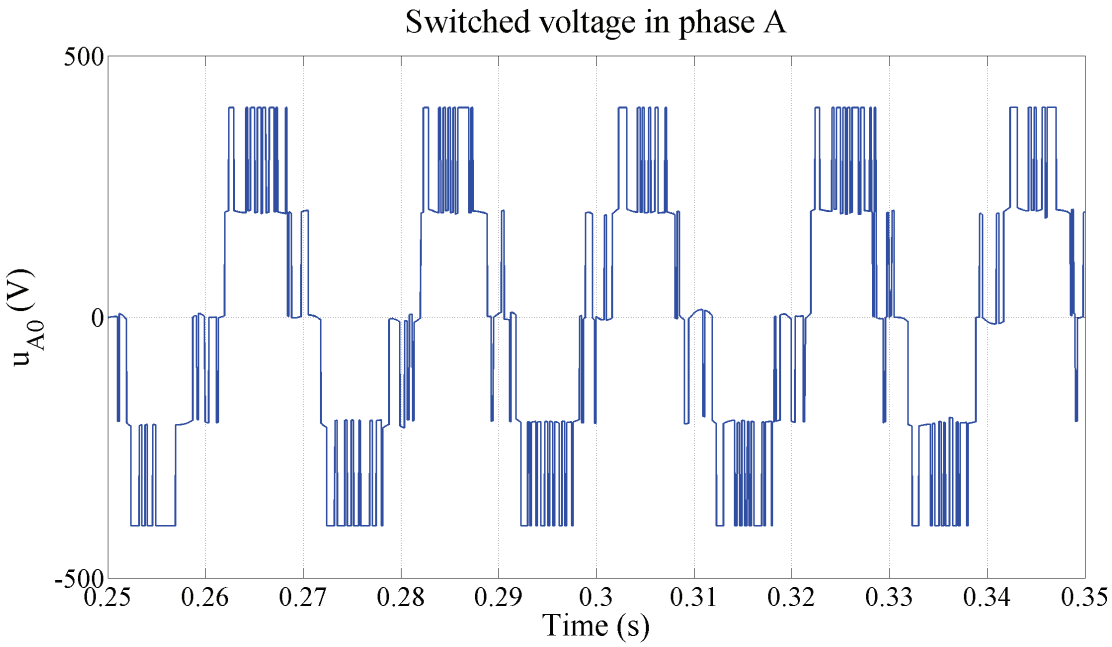


Fig. 73 Switched ouput voltage ($\alpha = 0°$)

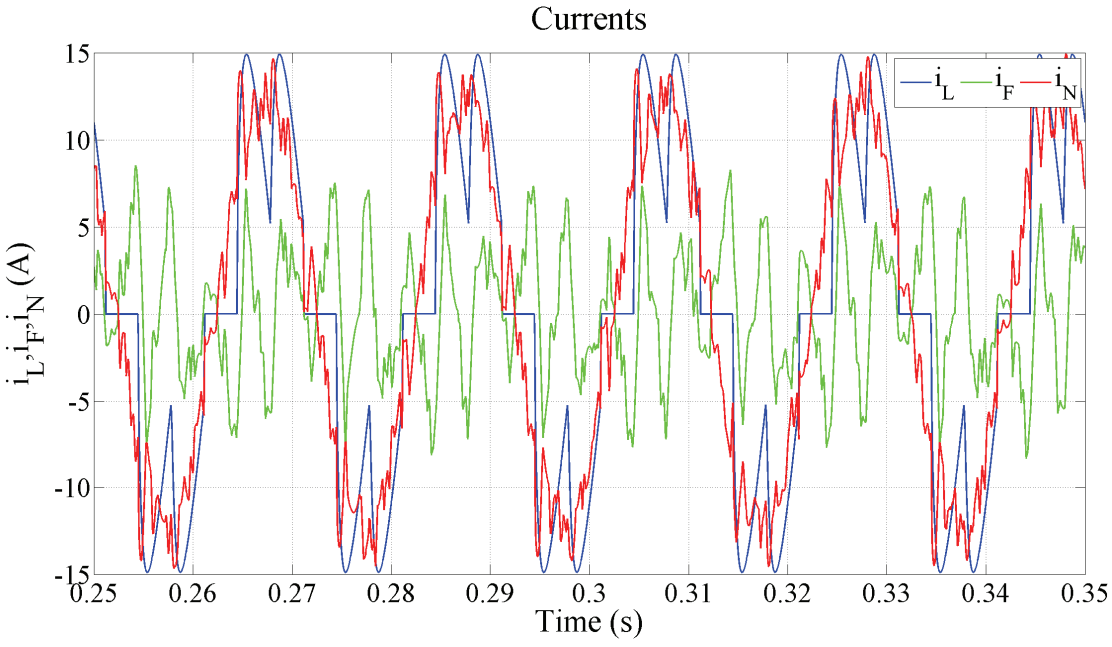


Fig. 74 Current waveforms ($\alpha = 50°$)

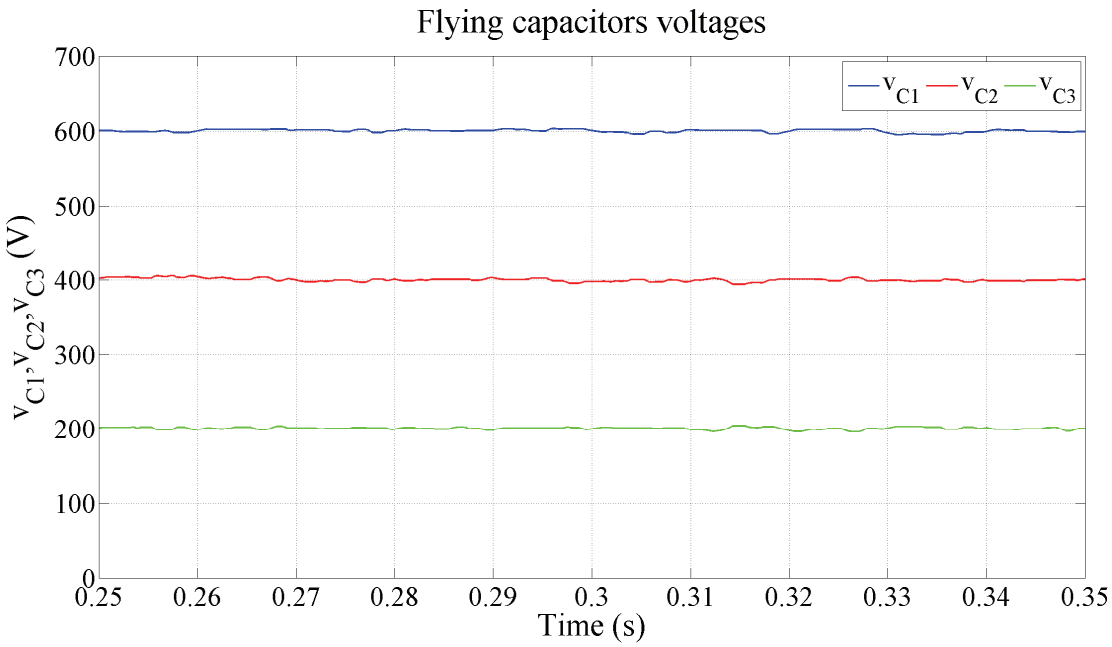


Fig. 75 Voltages across the flying capacitors (α = 50°)

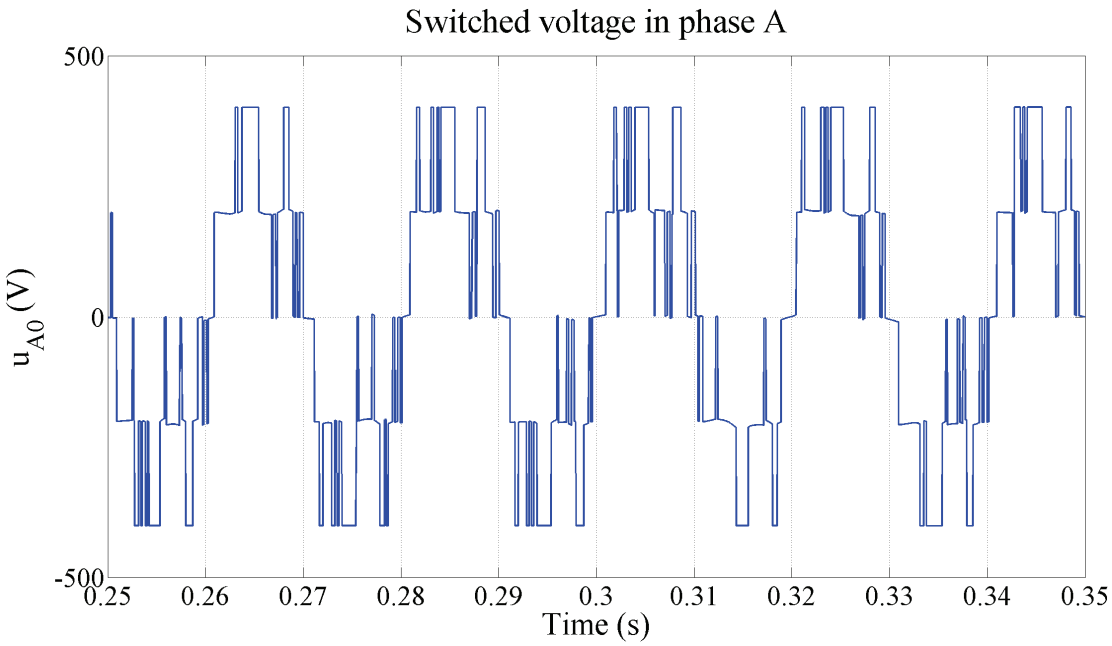


Fig. 76 Switched ouput voltage (α = 50°)

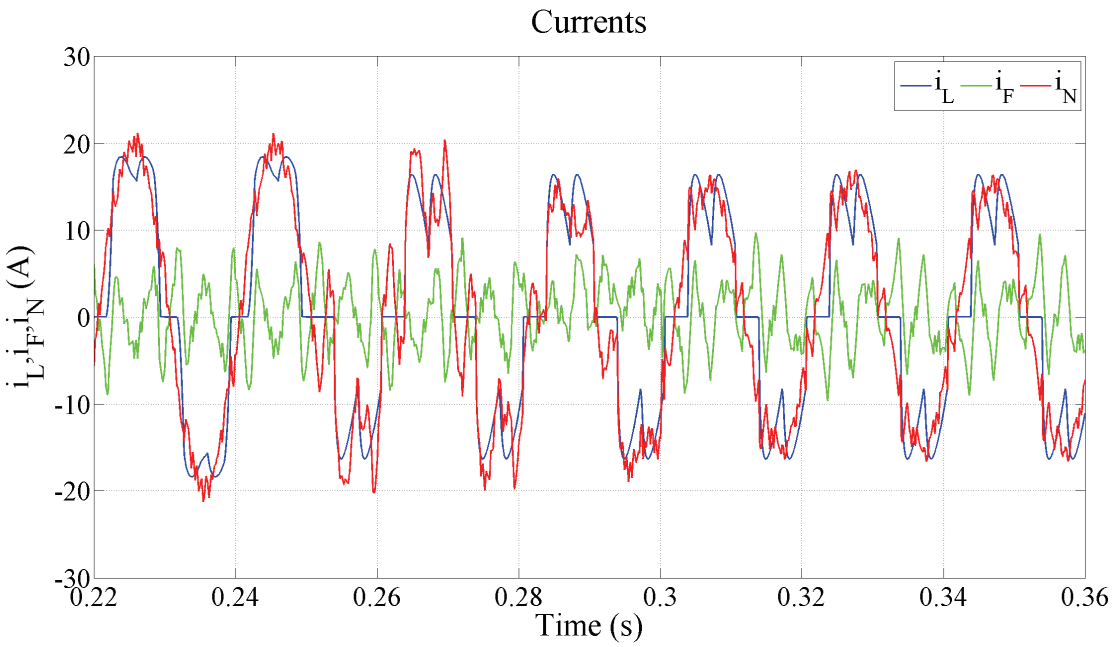


Fig. 77 Current waveform during the transition processs

In the above mentioned figures the waveforms of currents in one phase, flying capacitor voltages and switched voltage for control angle $\alpha = 0°$ are presented. Based on these figures it can be stated that the net current acquires near sinusoidal shape and that the voltage across flying capacitors is well balanced. Fig. 73 shows the five-level switched voltage, the results of the Fourier analysis are displayed in Fig. 78. The chart shows that the THD decreased thanks to filtration to ca 19% of the original value.

The simulation results for the control angle of the thyristor rectifier $\alpha = 50°$ are depicted in Fig. 74 - Fig. 76. According to Fig. 79, the results of harmonic analysis are a little bit worse than in the previous case. The THD decreased thanks to filtration to ca 30% of the original value. The values around 30 % are often considered the boundary value for a proper filter operation.

In both previous examples operates the active filter in a steady state. The transition process - step change of the control angle from 0° to 40° at time $t = 0.25$ sec - is depicted in Fig. 77. It is apparent that it takes two periods for the control to kick in which is in compliance with the claim in chapter 3.3.

Also the hysteresis current control of a two-level inverter and a five-level one was compared from the perspective of the resulting THD. The conditions for both simulations were identical. The results are depicted in Fig. 78 and Fig. 79. The hysteresis controller of the

two-level inverter evinced - in both cases - better THD. Therefore, the conclusion can be drawn that the hysteresis controller for the two-level inverter has a better dynamic.

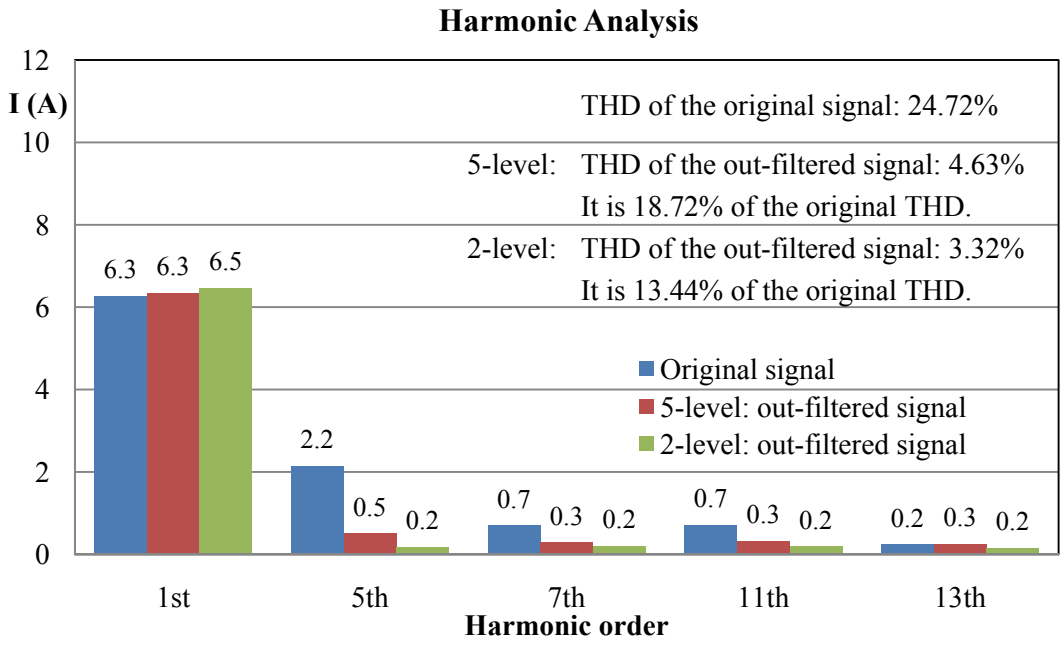


Fig. 78 Harmonics content of load and net currents ($\alpha = 0°$)

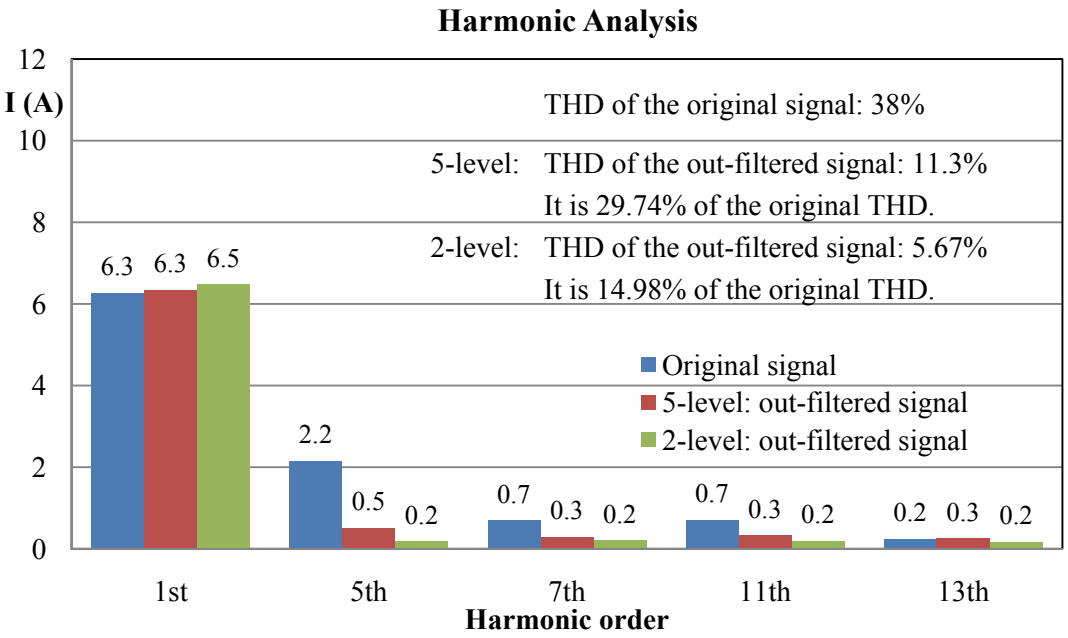


Fig. 79 Harmonics content of load and net currents ($\alpha = 50°$)

4 Laboratory Model of a Three-phase Five-level Flying Capacitor Inverter

In chapter 2 the power scheme, control strategies, simulation model and simulation results of a three-phase five-level FCI were described. Based on this knowledge a laboratory model has been designed, realized and debugged. The laboratory model and all the parts it consists of are described in this chapter.

A block scheme of the whole FCMI is depicted in Fig. 80. The power part includes the power supply with the DC link, the multilevel inverter itself (IGBTs, drivers, flying capacitors) and the electric load. Load current measurement secures the information about the required direction of the load current. It is got together with information about voltages across all flying capacitors into the control system. Adjustment of the received information, pulse-width modulator and voltage balancing algorithm are all implemented in the control system which is realized by dSpace boards. Everything is operated through the PC that the control program runs on. The control signals from dSpace have to be adjusted to proper voltage levels (between dSpace and drivers). The whole inverter is protected by hardware protections. All printed circuit boards (PCBs) need to be supplied by appropriate voltage, often with isolated grounds.

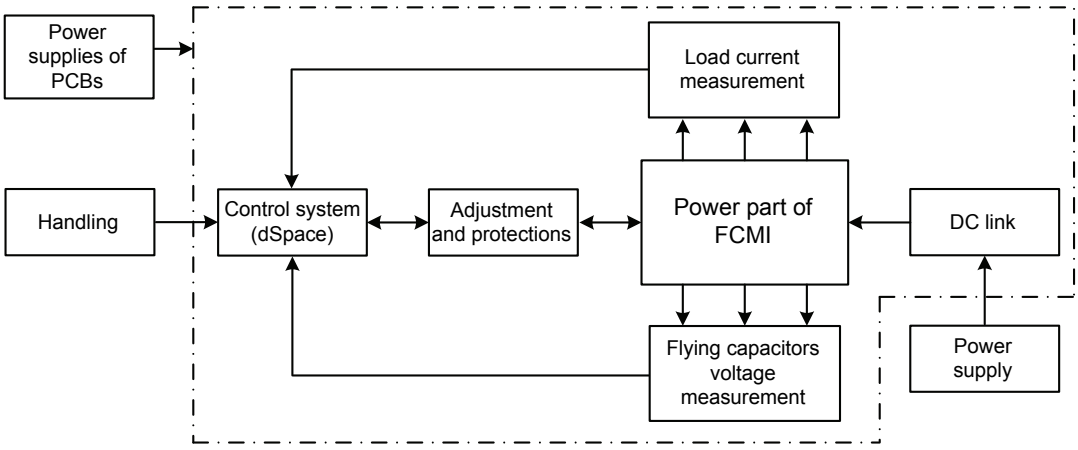


Fig. 80 A block scheme of the whole FCMI

4.1 Power Part

A basic scheme of the whole power part can be seen in Fig. 81.

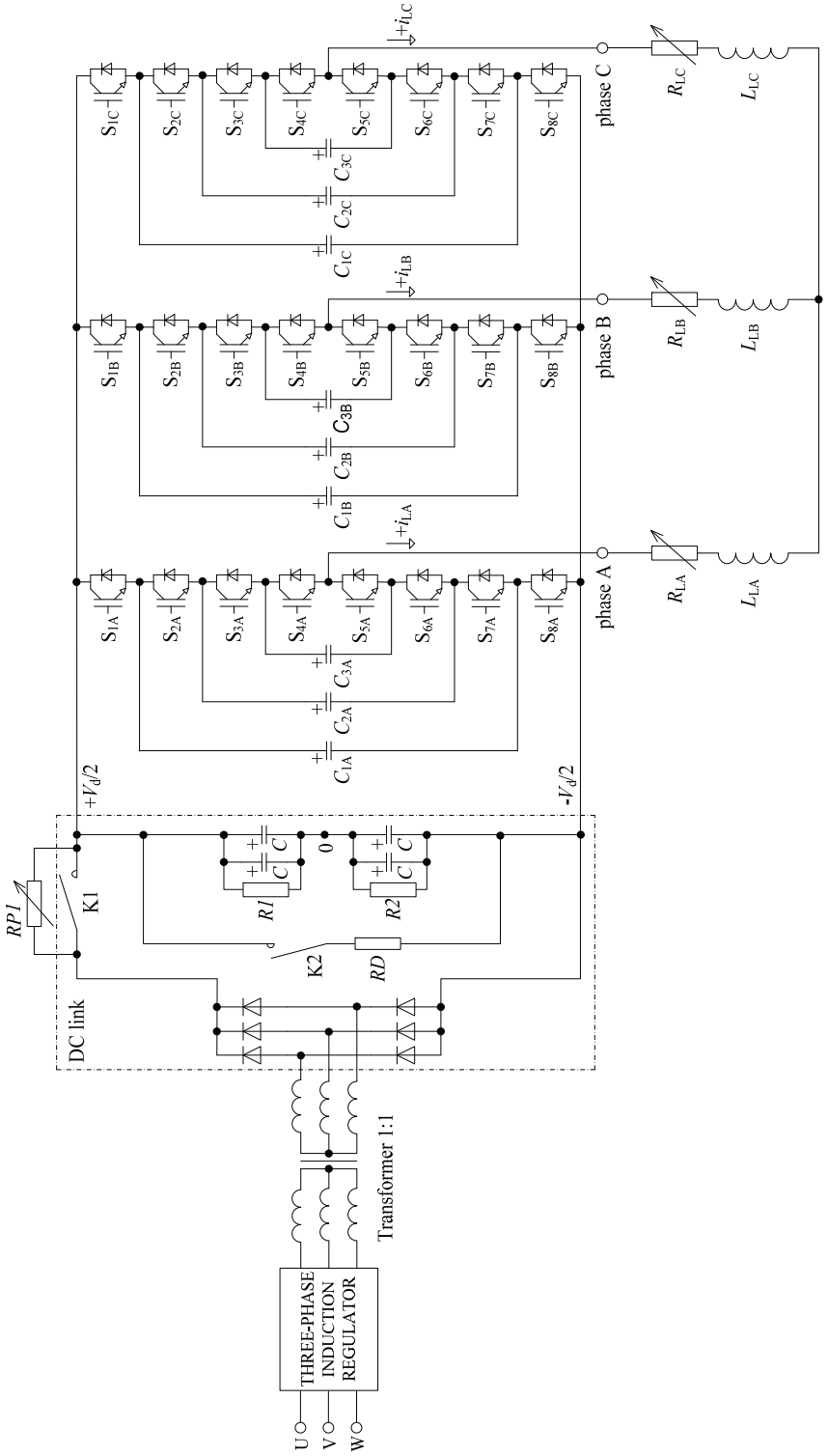


Fig. 81 A five-level FCI – a basic scheme of a power part

4.1.1 DC link

Similarly to the Simulink model, the capacitors in the DC link are connected to a three-phase diode rectifier over a parallel combination of a pre-charging resistor with a variable value *RP1* and an electric contactor K1. The discharging resistor *RD* (in fact several resistors) is connected parallel to the DC link capacitors over a contactor K2 which is actually a solid state relay (SSR). The voltage in the DC link is determined by the voltage of the three-phase induction regulator. Because of safety reasons in the laboratory, the dividing transformer with the transfer ratio 1:1 is connected between the induction regulator and the diode rectifier. As indicated in Fig. 81, the diode rectifier, electric contactor, all capacitors *C* and the discharging circuit comprise one compact unit called the DC link.

This compact unit is realized - besides other things - by two modules on separate PCBs. One is responsible for charging of the DC link capacitors and the other for their discharging. PCBs have been designed in order to reach maximum variability and can be used for DC link voltage up to 500 V. A large amount of terminals enable simple adding of additional components if needed. Their circuit schemes are depicted in Fig. 82. The output from the diode rectifier is connected to terminals X1 (positive) and X7 (negative). RP1 represents the charging resistor connected as an external part. It is bypassed by a contact of the contactor K1. This contactor can be controlled both manually and with a 5 V logic input. Selecting of this operation mode is possible with a SV1 jumper. When the SV1 contacts 2 and 3 are connected, K1 is controlled manually by a switch which is connected to the X11_SWITCH terminal. When the contacts 1 and 2 of SV1 are connected, a 5 volt logic input is responsible for operating the contactor K1. This is realised by the optocoupler OK1, so the 5 volt logic input is galvanic separated from other parts of the module if needed. This logic input can be connected both to the jumper pin terminal XJ2_5V or the screw terminal X13_5V. The state of the contactor can be signalled by a LED connected to the XJ3_LED terminal which glows when the contactor is switched on.

The power line from RP1 and K1 contact continues to X3, X4, X5 and X6 screw terminals, where the DC link capacitors are connected to the module. The same resistors R1 and R2 assure the even dividing of DC voltage between the capacitors. Their midpoint is connected among other terminals to J1 which is well suited for attachment of an oscilloscope probe hook. Between X6 and X3 (positive and negative terminal of the DC link capacitors) are connected the discharging resistors RD1 – RD6 which are switched by phototriac AHQ213 (SSR K2). The input of this SSR operates between 1.2 V and 1.4 V, so when operated at a 24 V supply, the suitable voltage is obtained with a stabilizer 78L05Z and a

resistor R7. The state of the phototriac is indicated by a LED connected to the XJ5_LED terminal which glows when the SSR is on-state. As in the case of the contactor K1, either a manual or a 5 V logic control of the K2 can be chosen, in this case with a jumper on SV2. Similarly to SV1, when contacts 2 and 3 of the SV2 are connected, manual control is selected and K2 is operated by a switch connected to the X10_SWITCH terminal. When contacts 1 and 2 of the SV2 are connected, the 5 volt logic input control is selected and connected through the XJ4_5V or X12_5V terminals. When galvanic separation of the 5 volt logic input is desired, no other supply has to be connected into the X9_24V_IN screw terminal.

Both the charging and the discharging module of the DC link are supplied with a 24 volt input. This voltage has been chosen in order to enable the usage of different power contactors (K1) which operate at coil voltages up to 24 volts in most cases.

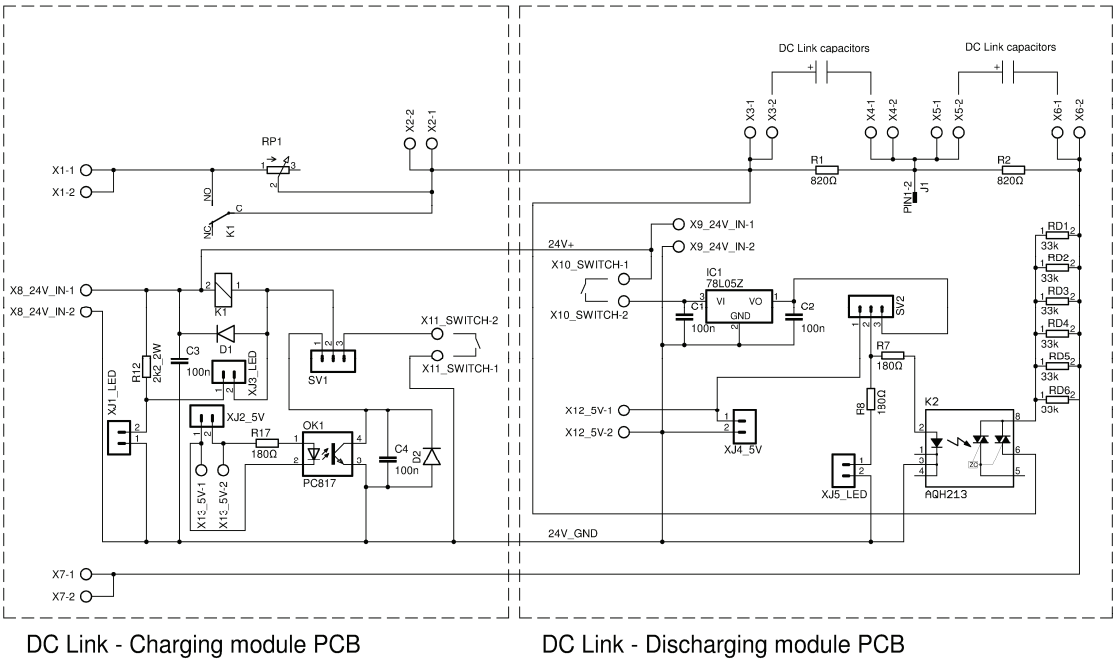


Fig. 82 Circuit schemes of PCBs in the DC link

The PCB layouts can be found in Appendix A and a picture of this construction unit is in Appendix C.

4.1.2 IGBT Drivers

The heart of the power part is the twelve driver boards. One board contains two power transistors, their drivers and a galvanic separation through the optocouplers. A scheme of the

board is depicted in Fig. 83. Two IGBTs on one board switch complementarily, and so, in Fig. 83, the IGBT_H can be S_1, S_2, S_3, S_4 and IGBT_L S_8, S_7, S_6, S_5, respectively. Their emitters are led to the screw terminals E_x and the collectors to C_x. This PCB was designed as a modular part hence it enables easy transformation of five-level FCI to the four- or three-level inverter.

The power supply of the board is taken from screw terminals 24V_x. The obtained switched voltage is rectified in the input Graetz bridge rectifier, so the 15 V_{DC} is produced which is indicated by a green LED light.

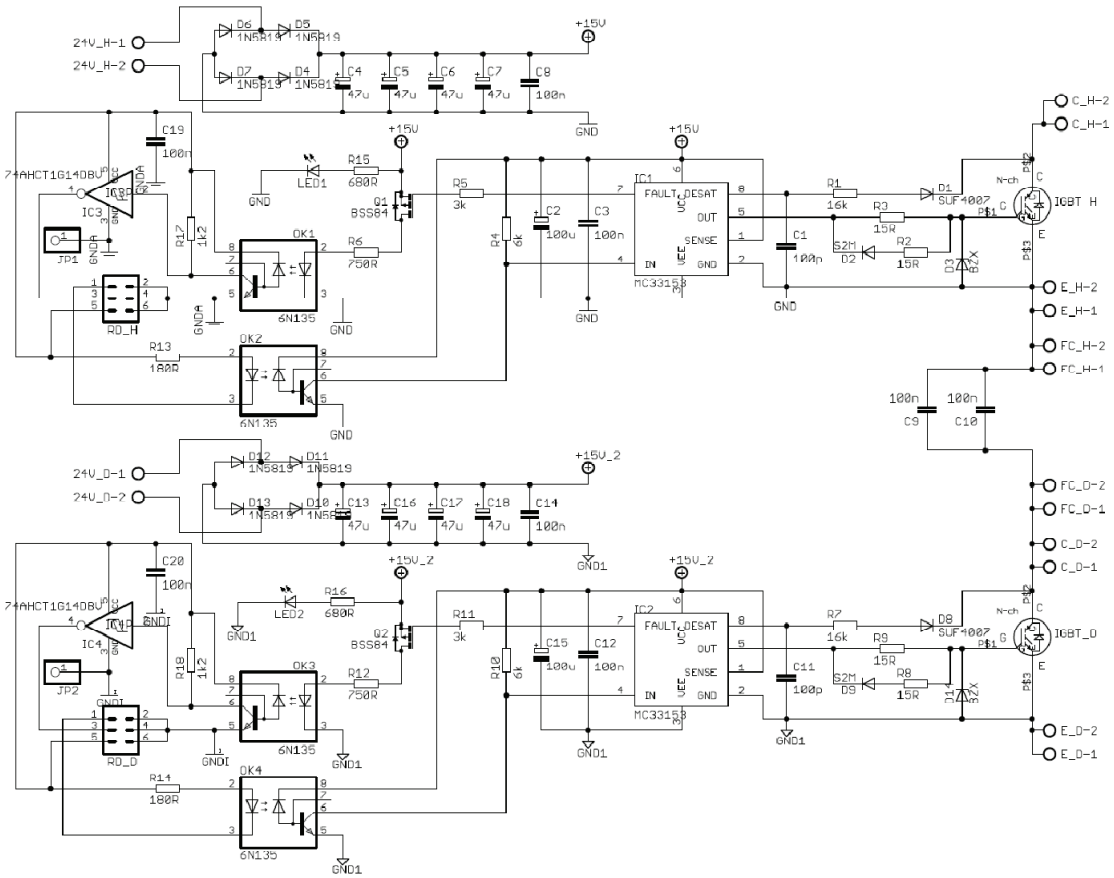


Fig. 83 A circuit scheme of one driver board

For this model, an IGBT for 20 A and 600 V in a TO-247 package has been chosen. This type has an already integrated hyperfast anti-parallel diode and its collector is connected to the bottom side of the package. Therefore the IGBT and its heat sink must be insulated by a mica tape. The selected driver MC33153 has an integrated saturation voltage measuring of the IGBT, so any fault signal is sent out directly from the driver further to the gate of the

P-channel DMOS transistor BSS84. When a fault occurs, the transistor turns off, the photodiode in the optocoupler 6N135 also turns off - because of no voltage - and the fault indication is transmitted further. The fault signal as well as the control signal of each driver are sent to or received by the control part over the optocouplers 6N135, so that they do not have a common ground with the control part. In Fig. 83, GNDA and GNDI are the same control grounds, GND is the ground of the "upper" IGBT and GND1 of the "lower" one. The galvanic separated signals are led to the control part through 6 pin connector RD_x. The fault signal that has been sent is further shaped by the inverting Schmitt trigger 74AHCT1G14.

The flying capacitors are directly connected to the driver board by terminals marked FC_x in Fig. 83. The flying capacitors are connected by very short wires in order to reduce the feeding inductivity. For even bigger reduction, low inductance capacitors are added (capacitors C9 and C10 in Fig. 83).

The whole power part of the converter consists of 24 IGBTs; eight IGBTs in one phase are cooled by the same heat sink and together with it they create one construction unit.

The PCB layouts are stored in Appendix A and the picture of this construction unit can be found Appendix C.

4.1.3 Separated Grounds

Each IGBT driver has to have a separated ground in order to function correctly and safely. There are at least two ways how to achieve it. The first way is to supply each driver from an isolation transformer with an output rectifier. This solution is described in (Thai, 2003) as well as in (Sivkov, 2011). However, as for its space demands this solution is a little less convenient because of the 24 pieces of galvanic isolated sources that are needed.

The other way is to use a common laboratory DC source, an already constructed switched-mode power supply and one little high frequency transformer with a ferrite core. The idea is depicted in Fig. 84. The switched-mode power supply operates on frequency 20 kHz and its output voltage is proportional to its input voltage, so it is easy to tune the desired value of the output voltage. Because the output DC voltage of the Graetz bridge rectifiers on the driver boards should be 15 V, the secondary AC voltage of the transformer should be 16 V. The maximum output voltage of a laboratory DC source is 30 V, so the transfer ratio 3:2 seems to be optimal. Because the power consumption of the drivers is quite small and not continuous, the secondary winding of the transformer can be winded by a flat ribbon cable which is structurally very advantageous.

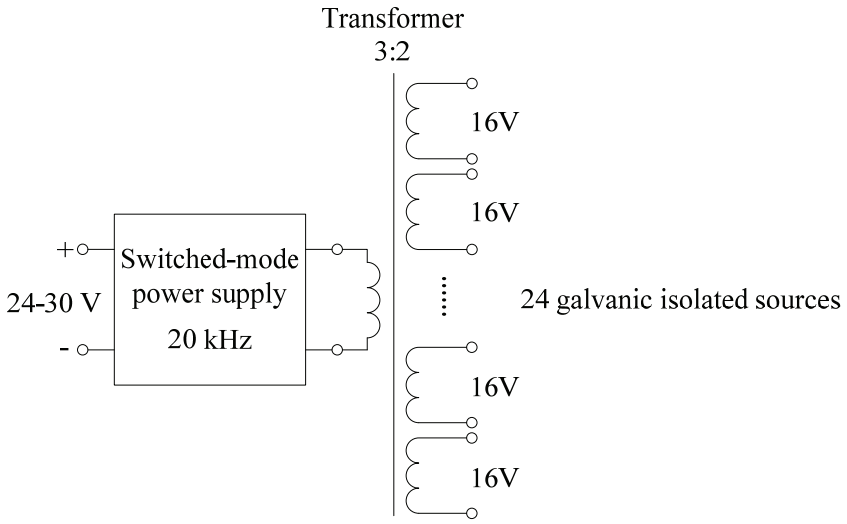


Fig. 84 Realization scheme of the 24 separated grounds

The control signals for the drivers also have to have separated grounds. They are separated from the one common control ground by optocouplers on the driver boards.

The picture of the switch-mode power supply with the transformer is in Appendix C.

4.2 Measuring Part

4.2.1 Measuring of Voltage

Individual voltage levels are clamped by the flying capacitors. The voltage across each flying capacitor, connected by the screw terminals FC+ and FC- in Fig. 85, is measured by a voltage LEM sensor which is capable of measuring voltages from 0 to 500 V. Its advantage is the galvanic separation between the measured and the measuring side. In order to adjust the measuring range, power resistors R1-R8 are needed on the input side. For each of the nine flying capacitors there is an identical PCB, however, the power resistors differs in maximum measured voltage. The operational amplifier UA741 modifies the measured signal for the dSpace system (±10 V) and it is led out on the coaxial connector X3 or on the screw terminal X4. The measuring ranges are set according to Table 6.

The supply symmetrical voltage (±15 V) for operational amplifiers on all measuring boards and LEM sensors is obtained from two identical DC/DC converters for a printed circuit board (PCB). Originally, the DC/DC converter should have been an IT2415S, however, it proved to produce too high a level of distortion. Therefore, two additional small PCBs with

a better DC/DC converter THD 12-2423 and voltage stabilizers 7812 and 7912 were made. Circuit scheme of one such board can be seen in Fig. 86.

Table 6 Relations between the measured voltages and the output ones

Flying capacitor	Output voltage of the operational amplifier	Corresponding measured voltage
C_{1x}	7.35 V	500 V
C_{2x}		350 V
C_{3x}		200 V

The PCB layouts can be found in Appendix A and the picture of the measuring set is in Appendix C.

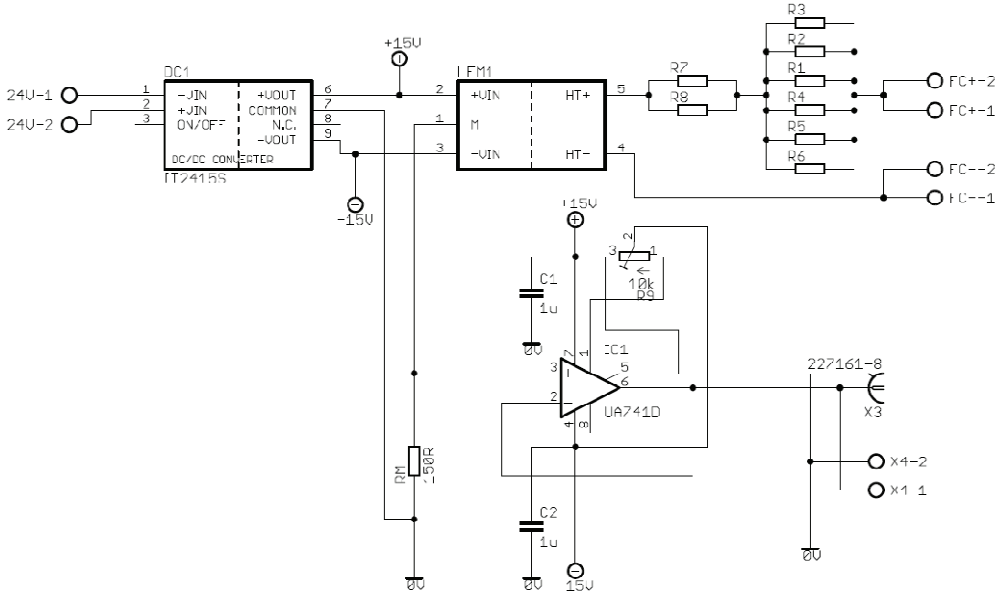


Fig. 85 Measuring of voltage – circuit scheme

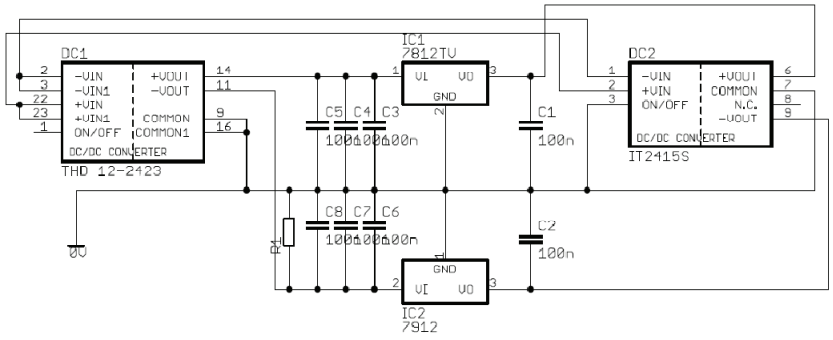


Fig. 86 Power supply for measuring boards – circuit scheme

4.2.2 Measuring of Current

As mentioned above, the information about the load current direction is necessary for the voltage balancing control strategy. Hence, the load current must be measured in all three phases; it means to construct three PCBs. Similarly as in the case of the voltage measurement board, the current measurement board has been designed with a current LEM sensor as can be seen in Fig. 87. The measured current flows into the LEM through the screw terminal +I and out again through the terminal –I. The symmetrical voltage (±15 V) for the supply of operational amplifiers and LEM sensors is gained from one PCB according to Fig. 86, because also the current measurement board was designed with the power source IT2415S that proved to be unsuitable. The load current measurement boards are able to measure currents from -15 A up to 15 A, where 15 A corresponds to 6 V at the output of the operational amplifier. This signal is led out on the coaxial connector X3 or on the screw terminal X4.

The PCB layouts can be found in Appendix A and the picture of the measuring set is in Appendix C.

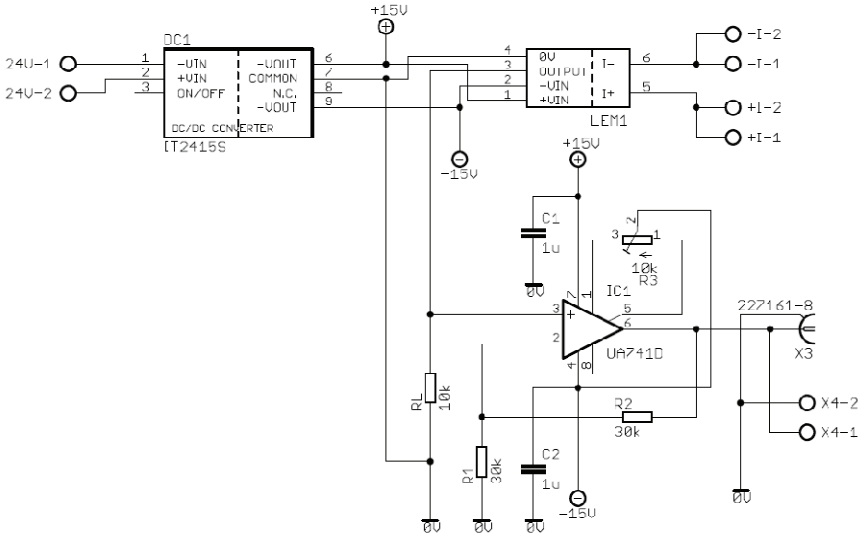


Fig. 87 Measuring of current – circuit scheme

4.3 Control Part

Broadly speaking, the control part can be divided into two sections – a signal adjustment with hardware protections and a dSpace system.

4.3.1 Signal Adjustment and Hardware Protections

The control signal sent to the driver boards or fault signals received from them have to be adjusted for the dSpace system which is in charge of the control. There are two similar types of boards – their circuit schemes are depicted in Fig. 88 and Fig. 89. Each phase has its own board and the main board is always assigned to the phase A (Fig. 88).

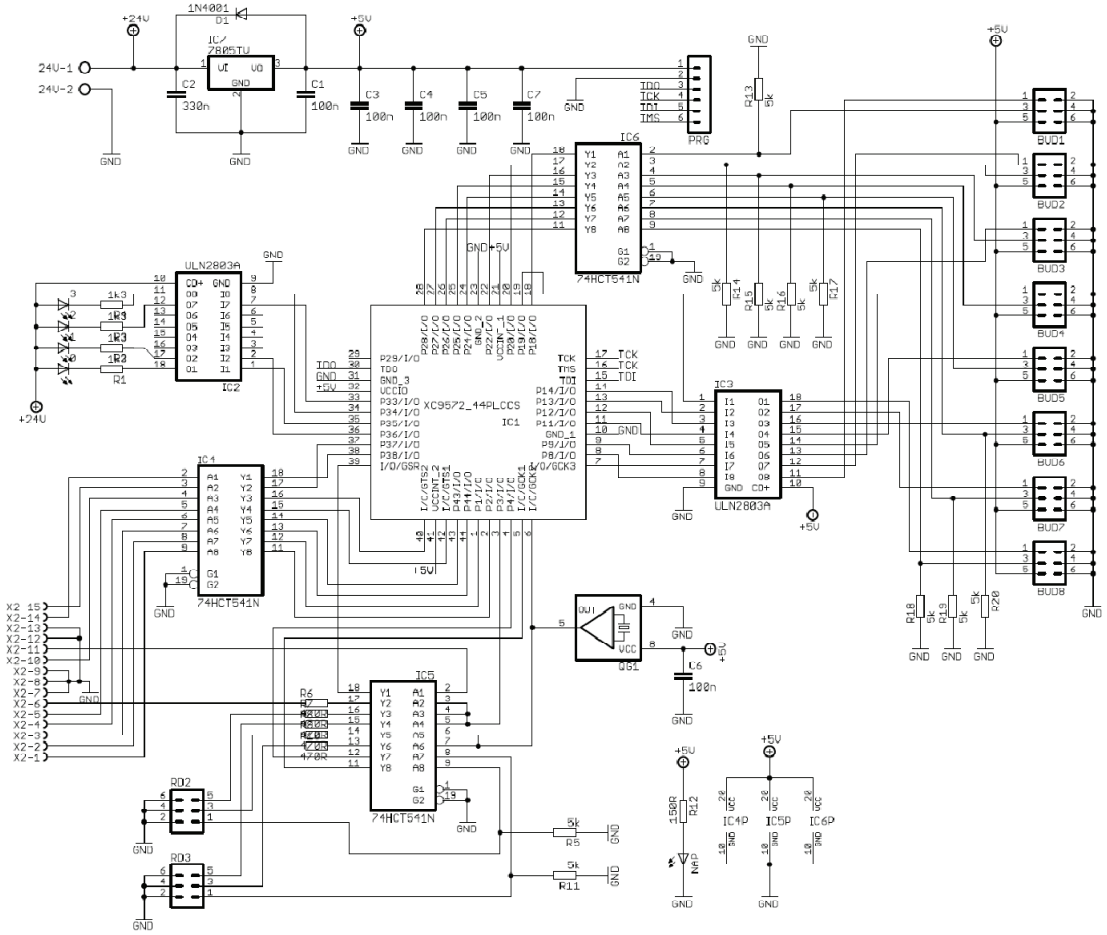


Fig. 88 Main adjustment and hardware protection PCB – circuit scheme

The adjustment is secured by two types of integrated circuits on three PCBs. The first is the octal buffer/line driver 74HCT541N, the second one is the Darlington transistor array ULN2803A. Both of them serve to improve the signal properties of the transmission with long cables. The cables leading to individual driver boards are connected into the sockets BUD1-BUD8 and the cable to the dSpace into the Cannon terminal X2. One transistor array

(IC2) on each board excites four LEDs that visually indicate which driver sent the fault signal. The encoding is in binary code – from 1 to 8.

Except for the adjustment, there are also the hardware protections designed on the boards. The core of each board is the in-system programmable CPLD XC9572 which receives all signals - both the control signals for the IGBT drivers and the fault signals from them. If a fault signal is received by the CPLD, the logic in it sends a turning-off signal to all of the 24 IGBTs immediately. Sending the signals quickly to all drivers requires interconnection between the boards necessary. The main board is connected with two other boards and when a fault signal occurs, a stop signal is sent from the main board to both side boards as well as to the dSpace.

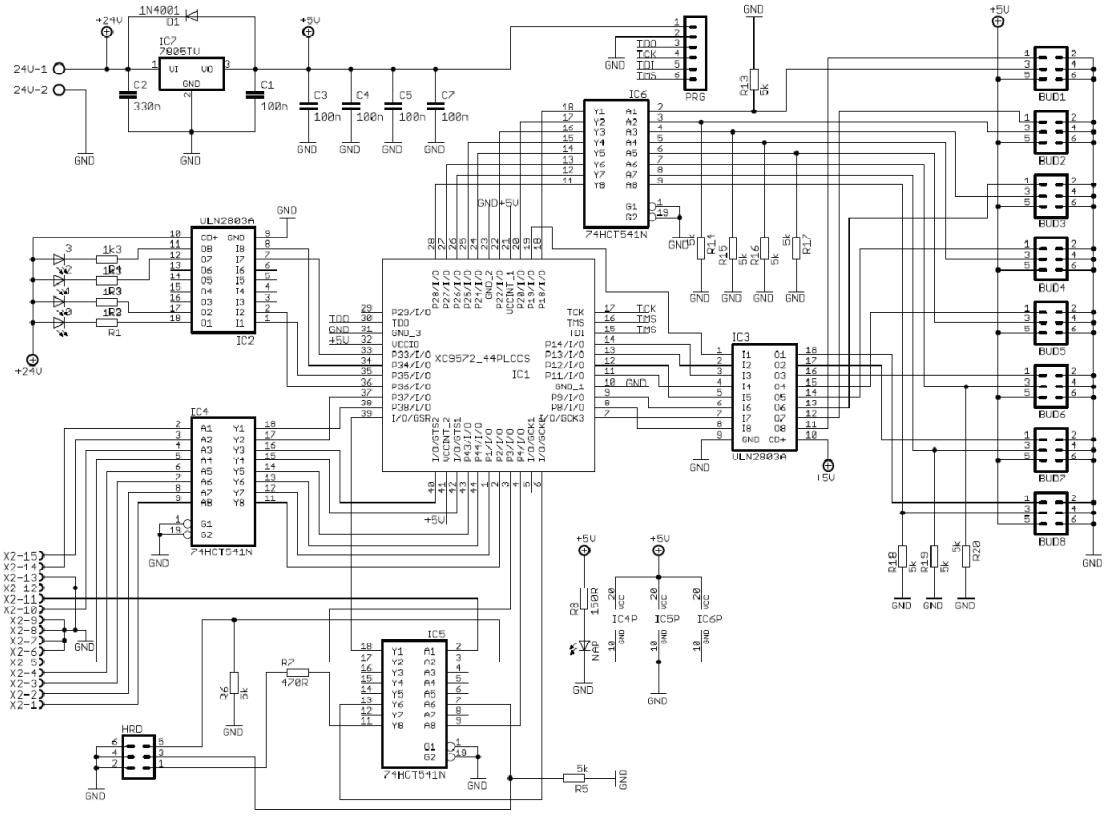


Fig. 89 Side adjustment and hardware protection PCB – circuit scheme

Except for the processing of fault signals, the CPLD on each board generates dead times. The dead time generation is carried out with the help of two D flip-flops as depicted in Fig. 91. The duration of dead times is determined by a clock signal produced by the quartz QG1 on the main board. One clock cycle takes 1 μs. The inner structures of the CPLDs have been

programmed in VHDL language. The source codes of all CPLDs are stored in Appendix A. The programmed structure of the in-system programmable CPLD of the main PCB is drawn in Fig. 90.

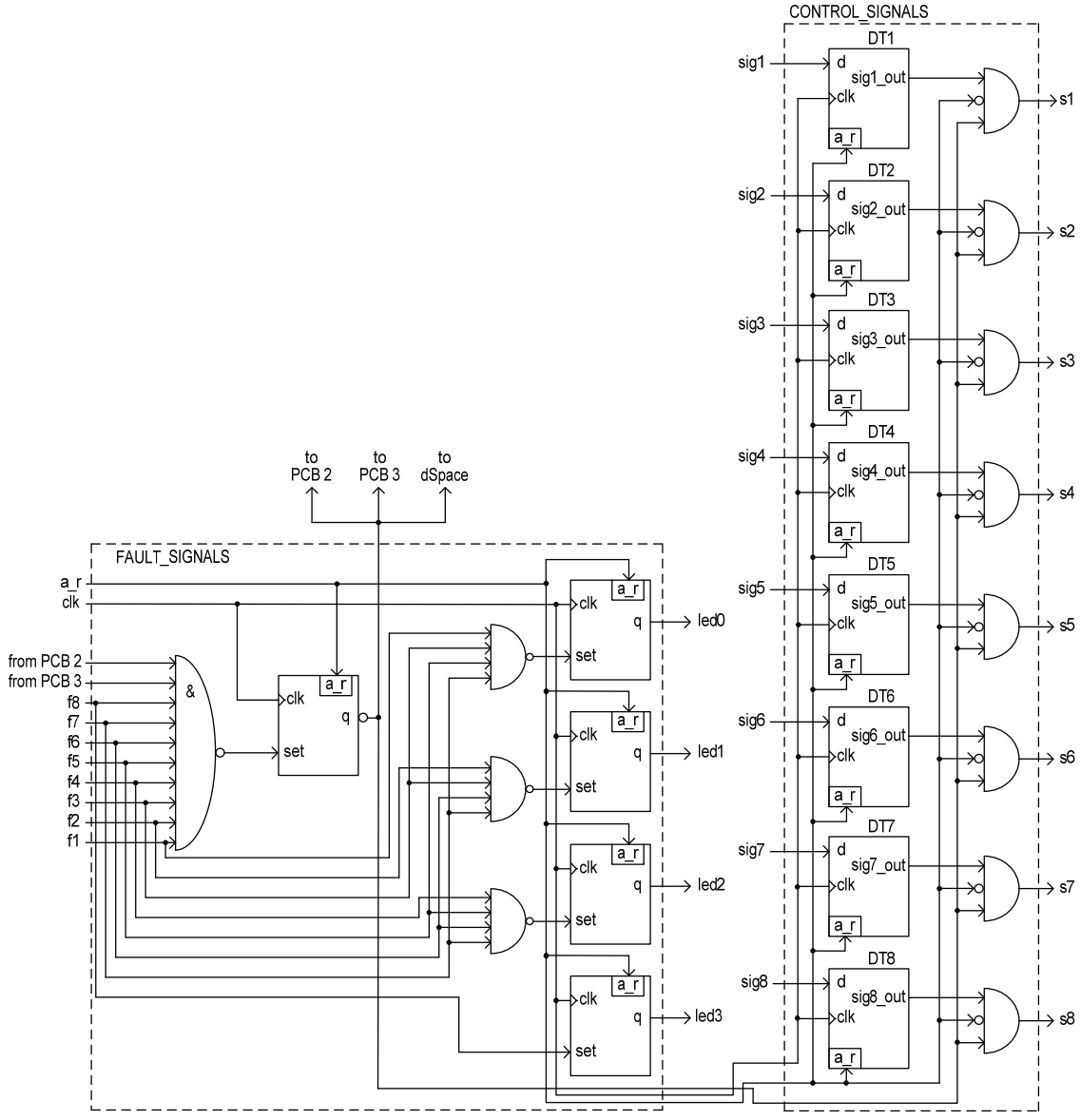


*Fig. 90 Inner scheme of the main in-system programmable CPLD (*a_r = *asyn. reset,* clk = *clock,* fx = *fault signal,* sigx = *signal from the dSpace,* sx = *signal to the IGBT driver,* DTx = *dead time)*

The PCB layouts can be found in Appendix A and the picture of the adjustment boards is in Appendix C.

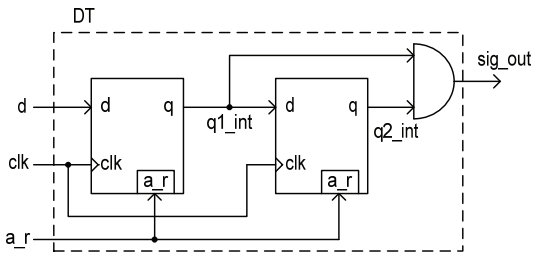


*Fig. 91 Dead time generation in CPLD (*a_r = *asyn. reset,* clk = *clock,* d = *signal from the dSpace,* sig_out = *signal to the IGBT driver,* DT = *dead time generation unit)*

4.3.2 dSpace

The dSpace system is a real-time control system. Sometimes it is called a rapid prototyping tool. It means that the generation of the working prototype should be direct and obviously rapid, so that the developed model could be applied to the actual system with the smallest procedural delay possible (Hedinger and Schär, 2011). The core of the dSpace contains several digital signal processors (DSPs) mounted on a PC board. The big advantage of this system is that it is linked to the Matlab-Simulink. More specifically, the possibility of a C code generation directly in Simulink. It means that the created control scheme in Simulink can be automatically transformed into an optimized code for the DSPs of the dSpace. Therefore, the simulation model described in chapter 2.5 can be further used for the real-time control of the laboratory model. In reality, everything what was done with the help of SimPowerSystem toolbox in the simulation model has to be extracted and all control signal outputs or measuring inputs have to be replaced by appropriate blocks of the dSPACE RTI1103 toolbox which is a toolbox for integration into the dSpace system.

The hardware interface that the dSpace uses with "outer world" is equipped with a dSpace DS1103 card which contains a sufficient number of 16-bit A/D converters multiplexed to 4 channels, of 12-bit one channel A/D converters and control digital I/O units. It is shown in Appendix C. During the work with dSpace, it was found the mistake of this interface that the digital signals transmitted via the I/O unit are sent separately with a period of 500 ns. For 24 signals that should be sent at the same time was it unacceptable. Therefore, the control output signals had to be processed by the function created in Simulink which assured their simultaneous transfer further into the adjustment boards. The code is stated in Appendix A.

The advantage of a real-time system (e.g. the dSpace), is the fact that the parameters of the system can be changed during the operation. Virtually all the parameters in the model can be measured and/or modified on-line. In order to do this, dSpace offers the ControlDesk program. This program reads and writes in the memory blocks reserved for the dSpace

processor and is able to show and change the value of every variable thanks to a memory map generated during the compilation of the program (Hedinger and Schär, 2011).

The program ControlDesk offers a wide choice of visualization and editing tools. A designed layout for the three-phase five-level FCI control can be seen in Fig. 92. The control panel has been assembled and the simulation model has been modified in order to change the on-line the frequency of the output voltage and the modulation index. Further, it also allows you to switch the MI operation on/off or to activate the asynchronous reset and simultaneously stop the next operation. Two warning lights indicate correct charging of all flying capacitors and running of the MI.

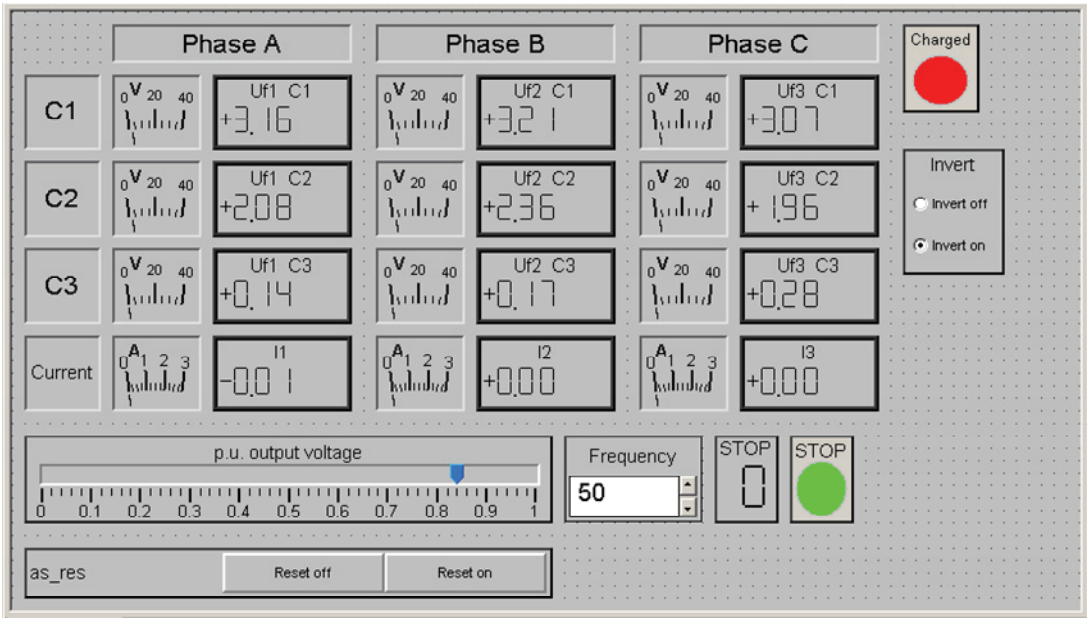


Fig. 92 ControlDesk layout for the three-phase five-level FCI control – design mode

5 Experimental Measurements on Laboratory Model

The simulation results of the three-phase five-level FCI are described in chapter 2.5 and its real design in chapter 4. This chapter presents the results of experimental measurements in order to verify the analysis of switching process from chapter 2.4.

Where it was possible, the parameters of the experiments were identical with the parameters of the executed simulations and there also are some fixed parameters that remain the same for all experiments:

Module of the DC link:

V_d = 150 V.....voltage in the DC link

C = 10 mF .....capacity of the capacitor in the DC link

R_{P1} ≅ 50 Ω (variable).....overall resistance of the pre-charging resistors

R_D = 5500 Ω.....overall resistance of the discharging resistors

$R_1 = R_2$ = 8200 Ω.....resistance of one equalizing resistor

Five-level flying capacitor inverter:

f = variable .....nominal output frequency

f_s = 1250 Hz .....switching frequency

C_x = 1 mF .....capacity of each flying capacitor

V_{Cxn}..... nominal voltages of flying capacitors (Eqs. (11)-(13))

$t_{DT} = 2\,\mu$s.....dead time duration

regular asymmetrically sampled PD modulation according to chapters 2.2.2.2 and 2.2.2.3

voltage balancing method according to chapter 2.3.2

Load:

R_{Lx} = max. 56 Ω (variable).....load resistance in one phase

L_{Lx} ≅ 30 mH .....load inductance in one phase

Step size of the dSpace is fixed – 100 μs.

5.1 Experimental Results of Switching with 1C-transitions

In the upper part of Fig. 93, the voltage v_{A0} between the phase output and the midpoint of the inverter can be seen. Its levels are explicit and rather constant because the electric load is small. The current waveform can be seen in the lower part of the oscillogram. The load is formed by a wire resistor only. It can be said that it is a resistive (R) load, however, the wire resistor has a relatively big parasitic inductance. Therefore, the current waveform resembles the sine curve.

When a bigger load (i.e. smaller resistance) is connected, the parasitic inductance decreases proportionally. The load current is bigger, therefore also the voltage levels are a little bit rippling as is apparent from Fig. 94. The current waveforms also indicate that we are dealing with a three-phase MI.

The waveforms of the resistive-inductive (RL) load are depicted in Fig. 95. The important message of the above mentioned analysis is that the expected transitions are only in the voltage waveform. There are neither any spikes reaching to the neighbouring level nor over one level. Fig. 96 shows it in more detail.

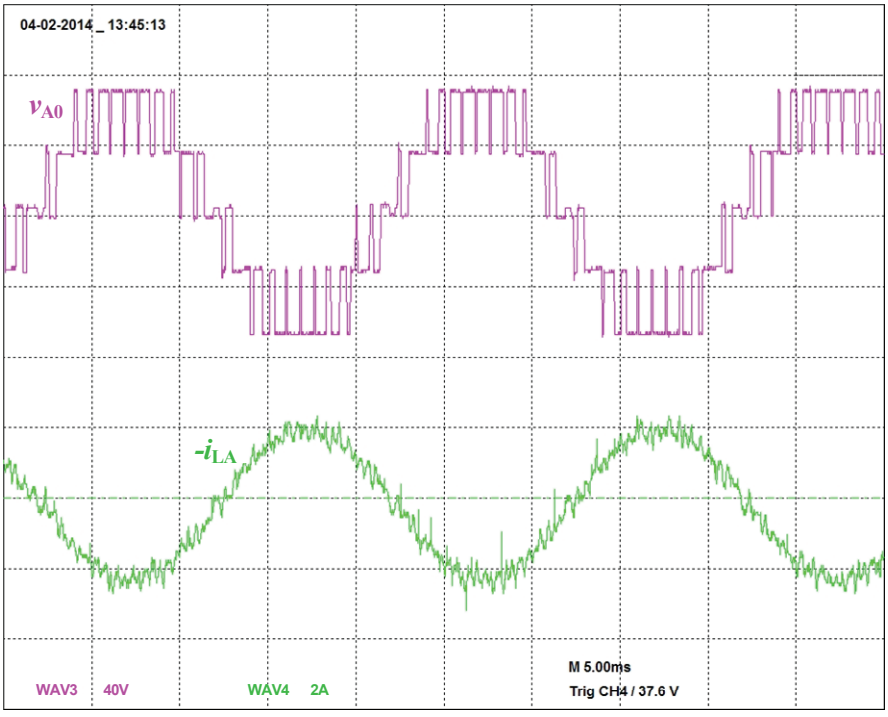


Fig. 93 Waveforms of v_{A0} and i_{LA}; f = 50 Hz, M = 0.95, R load

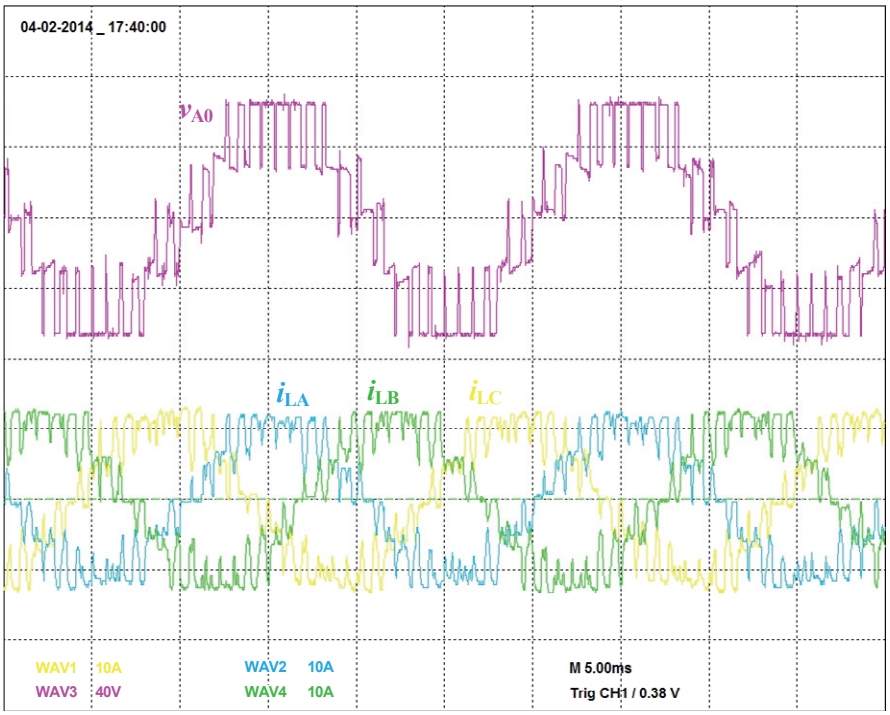


Fig. 94 Waveforms of v_{A0}, i_{LA}, i_{LB} and i_{LC}; f = 50 Hz, M = 0.95, R load

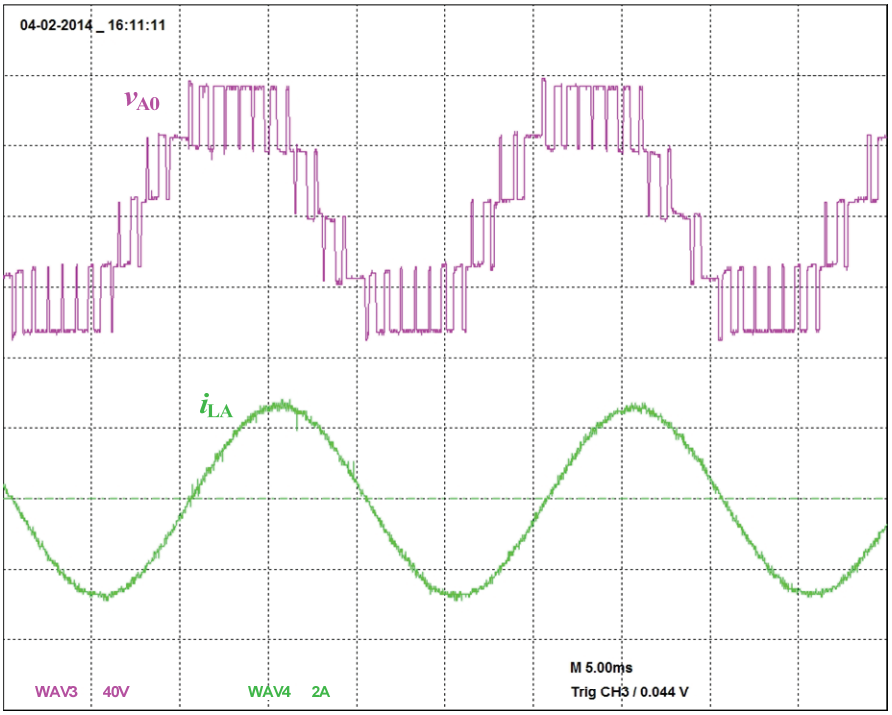


Fig. 95 Waveforms of v_{A0} and i_{LA} in the case of 1C-transitions; f = 50 Hz, M = 0.95, RL load

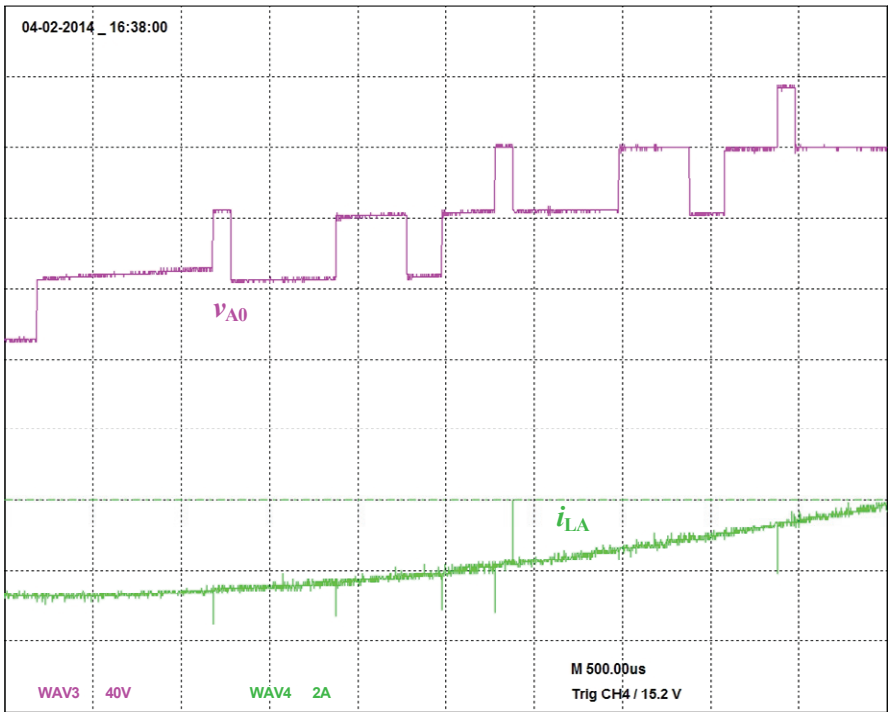


Fig. 96 A detail of waveforms in the case of 1C-transitions; f = 50 Hz, M = 0.95, RL load

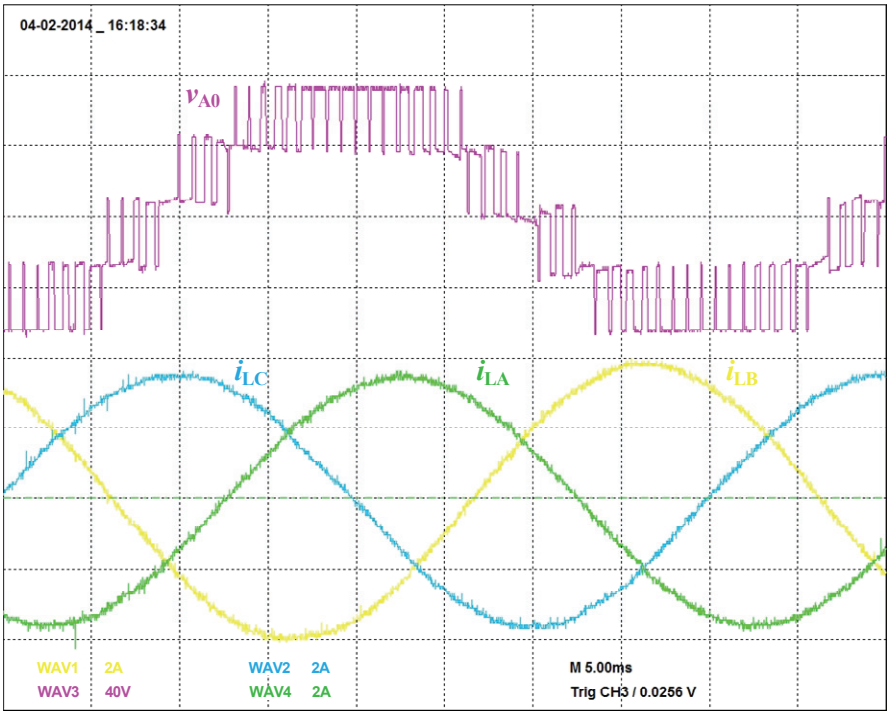


Fig. 97 Waveforms of v_{A0}, i_{LA}, i_{LB} and i_{LC}; f = 25 Hz, M = 0.95, RL load

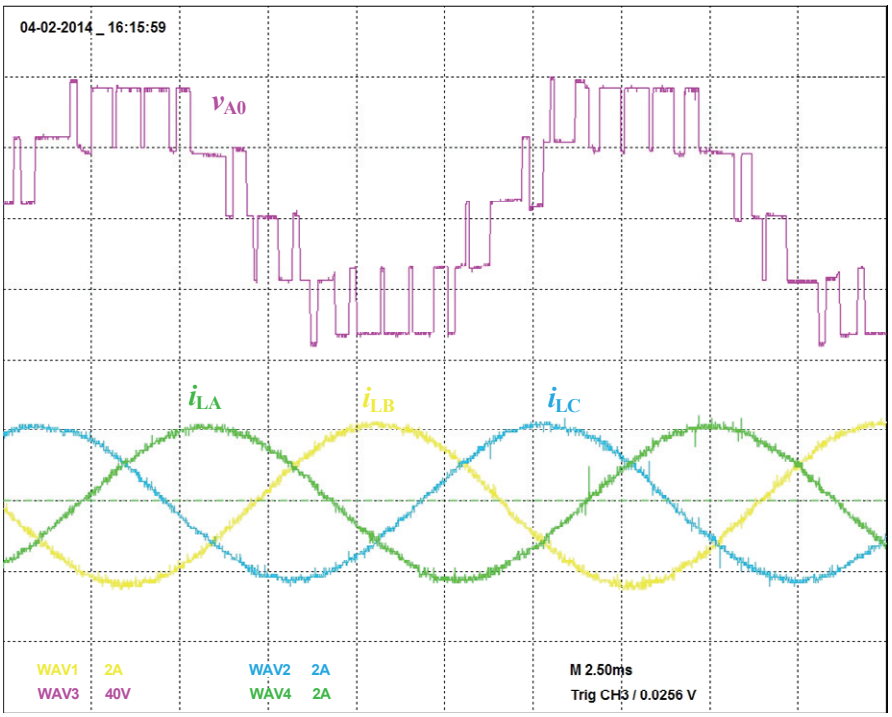


Fig. 98 Waveforms of v_{A0}, i_{LA}, i_{LB} and i_{LC}; f = 70 Hz, M = 0.95, RL load

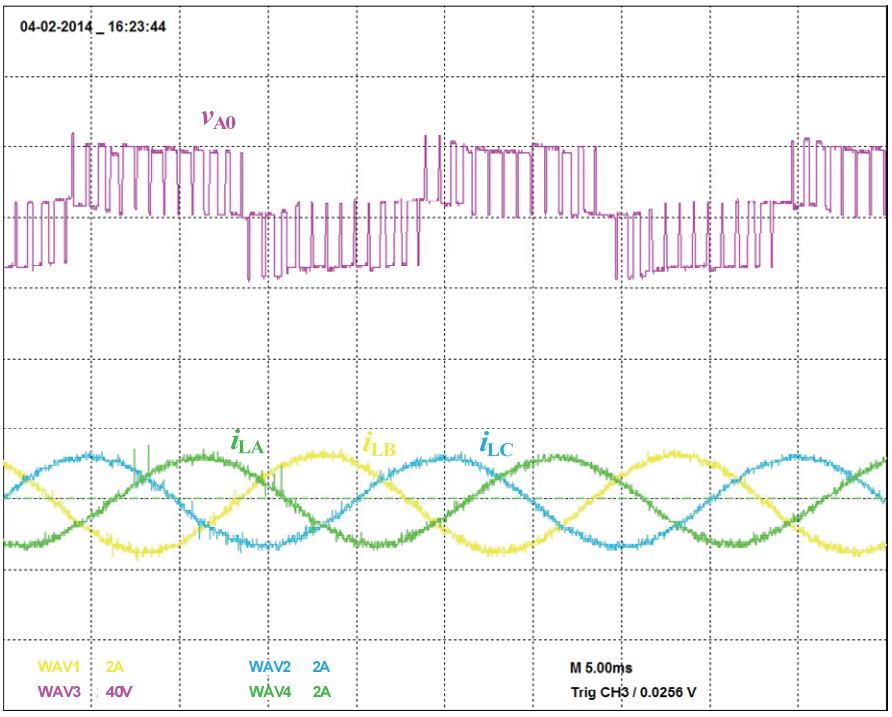


Fig. 99 Waveforms of v_{A0}, i_{LA}, i_{LB} and i_{LC}; f = 50 Hz, M = 0.50, RL load

It was mentioned in chapter 4.3.2 that some parameters can be changed during the operation of the inverter. That is why e.g. the voltage and current waveforms for lower output frequency 25 Hz are depicted in Fig. 97. They were acquired with the same load parameters as in Fig. 95. Analogous waveforms for higher frequency (70 Hz) are depicted in Fig. 98. The different amplitudes of the current waveforms are given by the change of impedance resulting from a different output frequency. The degradation of the five-level operation mode to the three-level one because of $M \leq 0.5$ is shown in Fig. 99.

5.2 Experimental Results of Switching with 2C-transitions

Oscillograms with the five-level voltage and a corresponding current for the switching process with 2C-transitions are depicted in Fig. 100. That the transitions in question are the 2C-transitions is obvious thanks to the short spikes in the voltage waveform whose height does not exceed two neighbouring levels. They are as wide as the dead time (if rising and falling times are neglected). A detail of the 2C-transitions is depicted in Fig. 101. It is quite obvious that the switching appears every 100 μs. This correlates with the duration of one step the dSpace works with. Hence, the switching frequency increases. That corresponds with the conclusions concerning the 2C-trasitions drawn from the analysis in chapter 2.4.3.

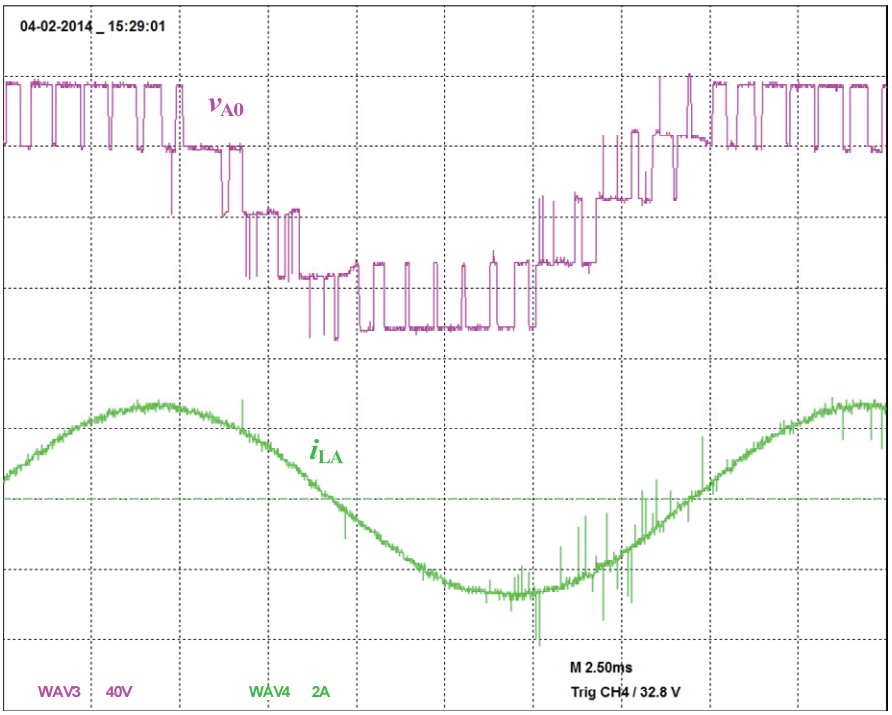


Fig. 100 Waveforms of v_{A0} and i_{LA} in the case of 2C-transitions; f = 50 Hz, M = 0.95, RL load

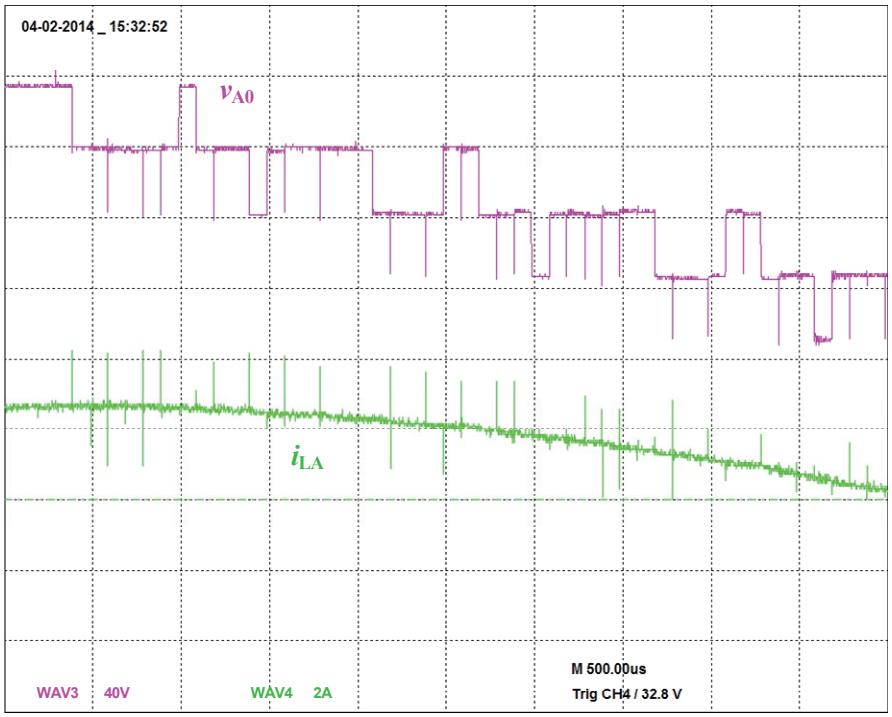


Fig. 101 A detail of waveforms in the case of 2C-transitions; f = 50 Hz, M = 0.95, RL load

5.3 Experimental Results of Switching with 3C-transitions

Oscillograms with five-level voltage and a corresponding current for the switching process with 3C-transitions are depicted in Fig. 102. That the transitions in question are the 3C-transitions is obvious thanks to the short spikes in the voltage waveform that are as high as the extent of three neighbouring levels. A detail of the 3C-transitions is shown in Fig. 103. The "forbidden" transitions reaching over two levels can be distinctly seen. Although these spikes correspond with the period of a dead time, they are unacceptable for a MI operation. The experiment results also confirm the conclusions about the 3C-transitions drawn from the analysis in chapter 2.4.4.

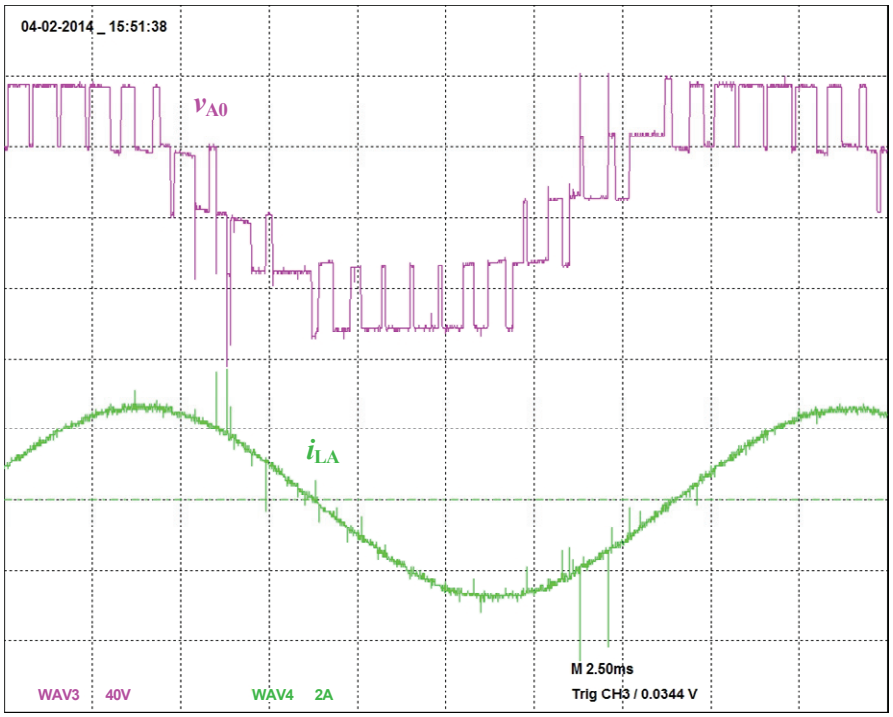


Fig. 102 Waveforms of v_{A0} and i_{LA} in the case of 3C-transitions; f = 50 Hz, M = 0.95, RL load

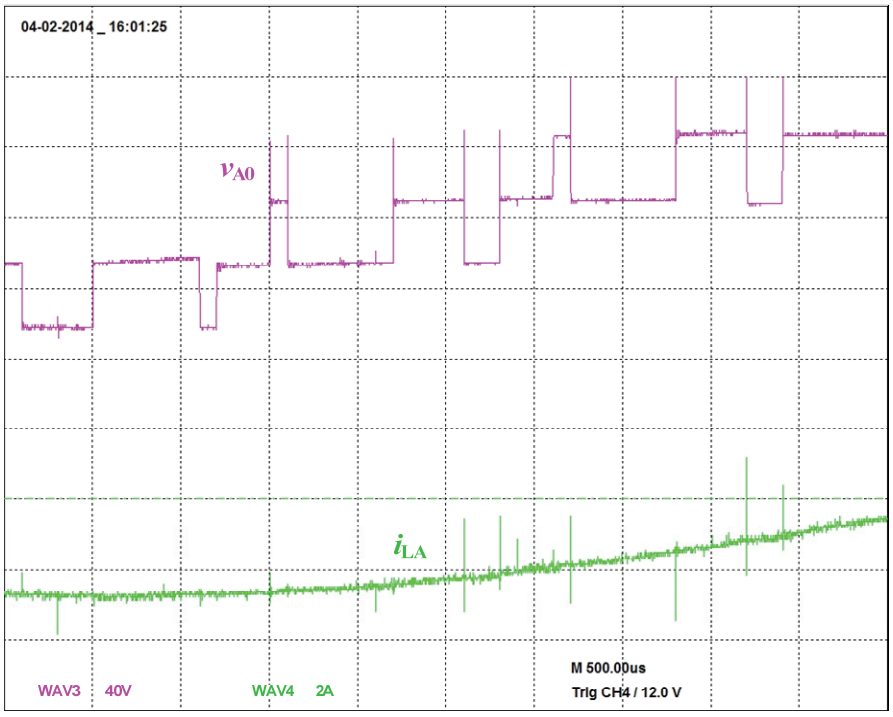


Fig. 103 Detail of waveforms in the case of 3C-transitions; f = 50 Hz, M = 0.95, RL load

6 Conclusion

6.1 Overview of the Results and Contributions

As can be seen from the Table of contents of this Thesis, it yielded both theoretical and practical results.

The pieces of knowledge about flying capacitor multilevel inverters and their control strategies have been presented. The three-, four- and five-level FCIs are described and the five-level FCI has been treated in more detail. It is also shown why, in reality, the FCIs are not used with more than seven levels. The popular modulation strategies are summarized with the emphasis on carrier-based PWM. The topic of flying capacitor voltage balancing without any auxiliary power circuit is explained as well as its control algorithm for the five-level FCI.

Next, the analysis of switching processes is performed, accompanied by particular examples. It is shown why switching over of one complementary switching device pair (1C-transitions) is preferably used. From the analysis follows – apart from other things – that the switching over of two complementary switching pairs (2C-transitions) is also possible, however, it leads to an increase of the switching frequency because the modulator instructs to switch over at each operational step. The performed analysis also considers the switching over of three complementary switching pairs (3C-transitions). In this case, it is shown that this manner of switching cannot be permitted because of the voltage jumps over two levels in the dead time which is an unacceptable transition considering the very core of multilevel inverters.

Furthermore, the dynamic model of the three-phase five-level FCI was created. Both the power part and its control part have been realized in Matlab-Simulink. The control algorithm has been designed with regard to its subsequent implementation into the real-time control system dSpace. Both the balancing algorithm and the performed analysis have been verified thanks to this model which was confirmed by the simulation results that have also been presented. The results show that, according to our expectations, the switching process with the 2C-transitions improves the voltage balancing of the flying capacitors. On the other hand, the switching process with 3C-transitions has no apparent effect on voltage balancing.

Because of the balancing algorithm and the performed analysis a real verification of the compact laboratory model of the three-phase five-level FCI has been realized. Also the compact unit of the DC link for the FCI has been realized because the flying capacitors must

not be clamped by auxiliary resistors. The measured voltage and current oscillograms prove that the laboratory model operates correctly.

All three switching processes have been implemented into the laboratory model of the FCI. The obtained results fully confirm the conclusions following from the performed analysis and simulations.

One theoretical chapter is devoted to the evaluation of the possible use of a multilevel inverter as an active filter. Specific requirements for medium voltage inverters operated as active filters are discussed – topology, semiconductor devices, switching frequency and supply voltage in the DC link. It is explained that for MV active filters the multilevel topology with IGBTs is appropriate. Besides, it is shown that (and in what way) the DC link voltage should be determined with respect to the order of the filtered harmonics and on the power factor. The basic possible control methods are briefly discussed. Also, the simulation model of the five-level FCMI, which is controlled by the hysteresis current control, has been created.

6.2 Fulfillment of Objectives Defined in Part 1.4

The summary of pieces of knowledge about FCMIs and their control strategies is stated as the first objective. It was fulfilled by the elaboration of chapters 2.1-2.3.

The second goal was to analyze and to evaluate the potential switching processes for a five-level FCI. It was fulfilled by the elaboration of chapter 2.4. The subject of this part is the own theoretical contribution of my doctoral thesis.

The third aim was to create a functional simulation model of a three-phase five-level FCI. This model and the simulation results are described in chapter 2.5 which fulfills this aim.

The fourth objective – to design and construct a compact laboratory model of a three-phase five-level FCI – was fulfilled by the designing, construction and debugging of this laboratory model and its description is in chapter 4.

To verify the conclusions drawn from the previous analysis, was the fifth aim and it is fulfilled by elaboration of chapter 5.

The last objective was the evaluation of the possibility to use a multilevel inverter as an active filter. The fulfillment of this goal is in chapter 3.

Based on that I consider all objectives of my doctoral thesis are completed.

6.3 Suggestions for Follow-up Development

One possible way, how to improve the voltage stabilization process, seems to be the on-line changing of flying capacitor nominal voltages according to the actual voltage in the DC link.

For further development, the flying capacitor pre-charging process should stay in focus. The attempt to eliminate the pre-charging resistor and the electric contactor could secure cheaper production because the DC electric contactors for MV applications are (even nowadays) quite expensive and their space requirements are not negligible.

As far as the multilevel active filter is concerned, the control strategy that keeps the voltage in the DC link constant has not been dealt with in this Thesis. However, for the prospective use of the FCMI in practice, it will be necessary to take it into consideration.

Appendix A Matrices, Codes and PCB Layouts

On the enclosed compact disk which is the inseparable part of this Thesis, the following attachments are stored:

A.1 - Matrices common for all simulations in the format of Matlab Workspace

A.2 - Matrices needed for simulations with 1C-transitions in the format of Matlab Workspace + their description

A.3 - Matrices needed for simulations with 2C-transitions in the format of Matlab Workspace + their description

A.4 - Matrices needed for simulations with 3C-transitions in the format of Matlab Workspace + their description

A.5 - Correcting C code for the dSpace interface to sent all digital output signals simultaneously

A.6 - VHDL code for the hardware protections and dead times generation of the CPLD on the main adjustment and hardware protection PCB as the complete project of Xilinx ISE Design Suite 12.3

A.7 - VHDL code for the hardware protections and dead times generation of the CPLD on the side adjustment and hardware protection PCB as the complete project of Xilinx ISE Design Suite 12.3

A.8 - PCB layouts and schemes in formats of the PCB design software Eagle 6.4.0

Appendix B List of M-files

M-file for Simulation of FCMI:

```
clc;                          % clear Command window
clear;                        % clear Workspace
f_net = 50;                   % (Hz) net frequency
Ufef = 64;                    % (V) RMS of supply voltage
nap_max_net = sqrt(2)*Ufef;   % (V) supply voltage amplitude
nabijeci_odpor=50;            % (Ohm) pre-charging resistance
f=50;                         % (Hz) output frequency
Uc=0.95;                      % (p.u.) modulation index
xy = 1;                       % (-) aux. for carrier signal
fs = 1250;                  % (Hz) switching frequency
T=100e-6;                   % (s) sample time
Tsimul=1e-6;                % (s) simulation step size
Vd=Ufef*2.34;               % (V) voltage in the DC link
C=1e-3;                     % (F) capacity of one cap in DC link
R_zatez=20;                 % (Ohm) load resistance
L_zatez=0.04;               % (H) load inductance
svod = 10e3;                % (Ohm) leakage
UC1_0=0;                  % (V) init. voltage of FC1
UC2_0=0;                  % (V) init. voltage of FC2
UC3_0=0;                  % (V) init. voltage of FC3
UC1=0.75*Vd;              % (V) nom. voltage of FC1
UC2=0.5*Vd;               % (V) nom. voltage of FC2
UC3=0.25*Vd;              % (V) nom. voltage of FC3
stav=2;                   % (-)auxiliary; init. state

% dead times simulation
death_time=Tsimul;               % (s) one clk step
death_time_period=2*death_time; % (s) duration of dead time

% assurance
assurance=      [ 0  0  2  3  4
                  1  1  1  3  4
                  0  2  2  2  4
                  0  1  3  3  3
                  0  1  2  4  4];

%sw. states   1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16
m_sepnuti = [ 0  1  0  0  0  1  0  0  1  0  1  1  1  1  0  1
              0  0  1  0  0  1  1  0  0  1  0  1  1  0  1  1
              0  0  0  1  0  0  1  1  1  0  0  1  0  1  1  1
              0  0  0  0  1  0  0  1  0  1  1  0  1  1  1  1
              1  1  1  1  0  1  1  0  1  0  0  1  0  0  0  0
```

```
              1  1  1  0  1  1  0  0  0  1  1  0  1  0  0  0
              1  1  0  1  1  0  0  1  1  0  1  0  0  1  0  0
              1  0  1  1  1  0  1  1  0  1  0  0  0  0  1  0];

% sw. states        0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
level_selection = [ 0 1 1 1 1 2 2 2 2 2  2  3  3  3  3  4];

Further are loaded all needed matrices into the Workspace.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

M-file for Simulation of Multilevel Active Filter

```
clc;                              % clear Command window
clear;                            % clear Workspace
frekvence = 50;                   % (Hz) net frequency
napeti_ef = 230;                  % (V) RMS of supply voltage
napeti_max = sqrt(2)*napeti_ef; % (V) supply voltage amplitude
f=50;                             % (Hz) output frequency
Ud=800;                        % (V) voltage in the DC link
C=1e-3;                        % (F) capacity of one cap in DC link
svod = 10e3;                   % (Ohm) leakage
UC1=0.75*Ud;                % (V) nom. voltage of FC1
UC2=0.5*Ud;                 % (V) nom. voltage of FC2
UC3=0.25*Ud;                % (V) nom. voltage of FC3
UC1_0=UC1;                  % (V) init. voltage of FC1
UC2_0=UC2;                  % (V) init. voltage of FC2
UC3_0=UC3;                  % (V) init. voltage of FC3
stav=2;                     % (-)auxiliary; init. state

R_net = 0.001;     % (Ohm) net resistance
L_net = 10e-6;     % (H) net inductance
narust = 100;      % (V) ramp of voltage
R_kom = 0.03;      % (Ohm) resistance of one commutation reactor
L_kom = 0.003;     % (H) inductance of one commutation reactor
delka_pulzu = 60; % (deg) pulse length for thyr.rect.
R_load = 30;       % (Ohm) load resistance
L_load = 0.005;    % (H) load inductance
R_filter = 0.05;   % (Ohm)resistance of one coupling reactor
L_filter = 0.01;   % (H) inductance of one coupling reactor
SP = 1.3;          % (A) band width of current control
SP2=2*SP;
SP3=3*SP;

fsig = frekvence;           % (Hz) fund. freq. of anal. sig.
Tsig = 1/fsig;              % (s) fund. period of anal.signal
```

```
NF = 2^9;                    % (-) members of Four.ser.
Tsamp = 1/(fsig*NF)          % (s) sample period
T = Tsamp;                   % (s)
Tsimul = Tsamp/20            % (s) simulation step size
Tout = Tsimul;               % (s) because of Scopes
init_sh = 0;                 % (A) init.value for S/H

% dead times simulation
death_time=Tsimul;               % (s) one clk step
death_time_period=2*death_time; % (s) duration of dead time

% Counting for Discrete Fourier transformation
 for n=1:NF
     M_0(n,1)=(cos(2*pi*0*(n-1)/NF)-j*sin(2*pi*0*(n-1)/NF));
     M_1(n,1)=(cos(2*pi*1*(n-1)/NF)-j*sin(2*pi*1*(n-1)/NF));
     M_5(n,1)=(cos(2*pi*5*(n-1)/NF)-j*sin(2*pi*5*(n-1)/NF));
     M_7(n,1)=(cos(2*pi*7*(n-1)/NF)-j*sin(2*pi*7*(n-1)/NF));
     M_11(n,1)=(cos(2*pi*11*(n-1)/NF)-j*sin(2*pi*11*(n-1)/NF));
     M_13(n,1)=(cos(2*pi*13*(n-1)/NF)-j*sin(2*pi*13*(n-1)/NF));
 end

% assurance
assurance =      [ 0  0  2  3  4
                   1  1  1  3  4
                   0  2  2  2  4
                   0  1  3  3  3
                   0  1  2  4  4];

%sw. states   1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16
m_sepnuti = [ 0  1  0  0  0  1  0  0  1  0  1  1  1  1  0  1
              0  0  1  0  0  1  1  0  0  1  0  1  1  0  1  1
              0  0  0  1  0  0  1  1  1  0  0  1  0  1  1  1
              0  0  0  0  1  0  0  1  0  1  1  0  1  1  1  1
              1  1  1  1  0  1  1  0  1  0  0  1  0  0  0  0
              1  1  1  0  1  1  0  0  0  1  1  0  1  0  0  0
              1  1  0  1  1  0  0  1  1  0  1  0  0  1  0  0
              1  0  1  1  1  0  1  1  0  1  0  0  0  0  1  0];

Further are loaded all needed matrices into the Workspace.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix C Additional Schemes and Pictures

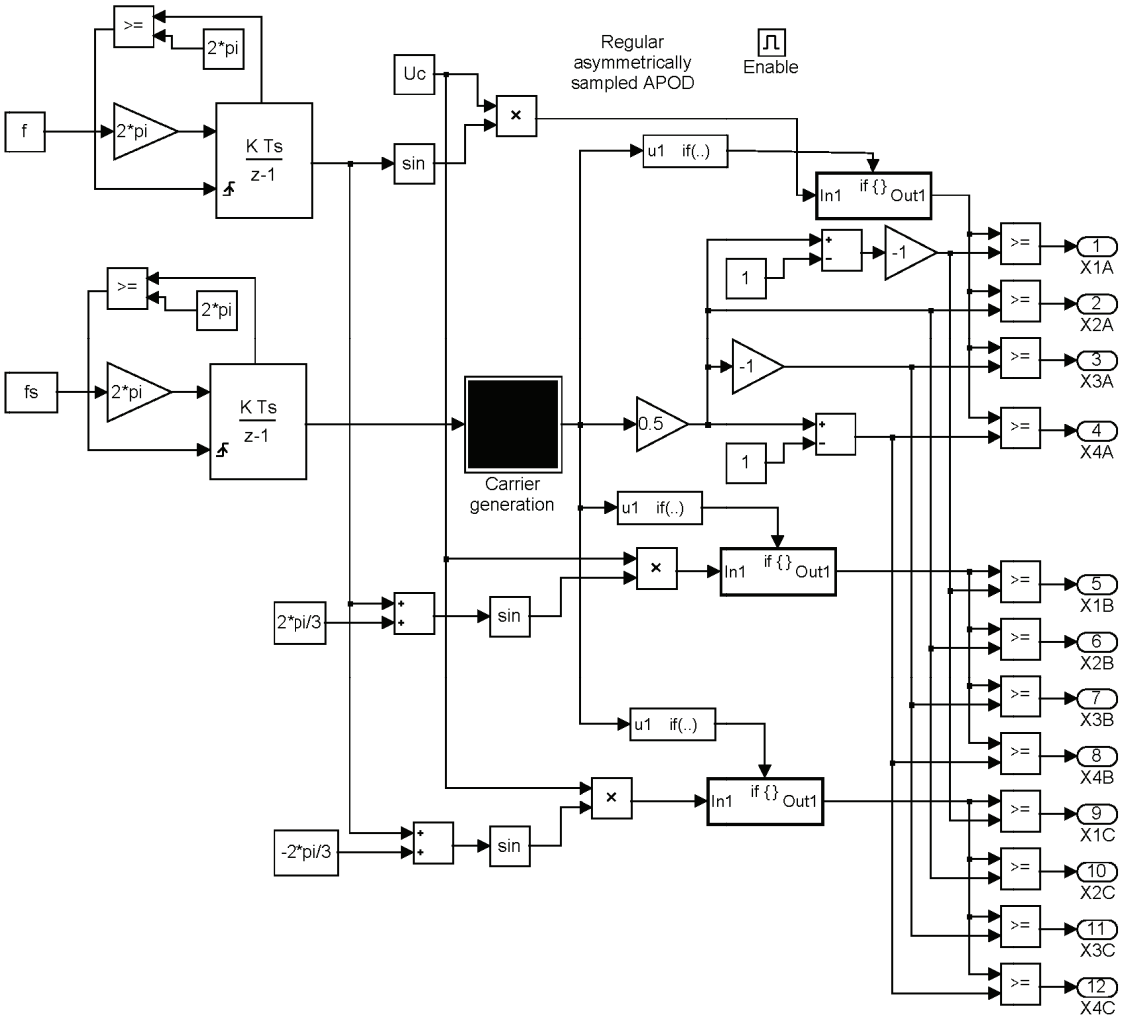


Fig. 104 Block "PWM": Regular asymmetrically sampled APOD PWM for a five-level FCI

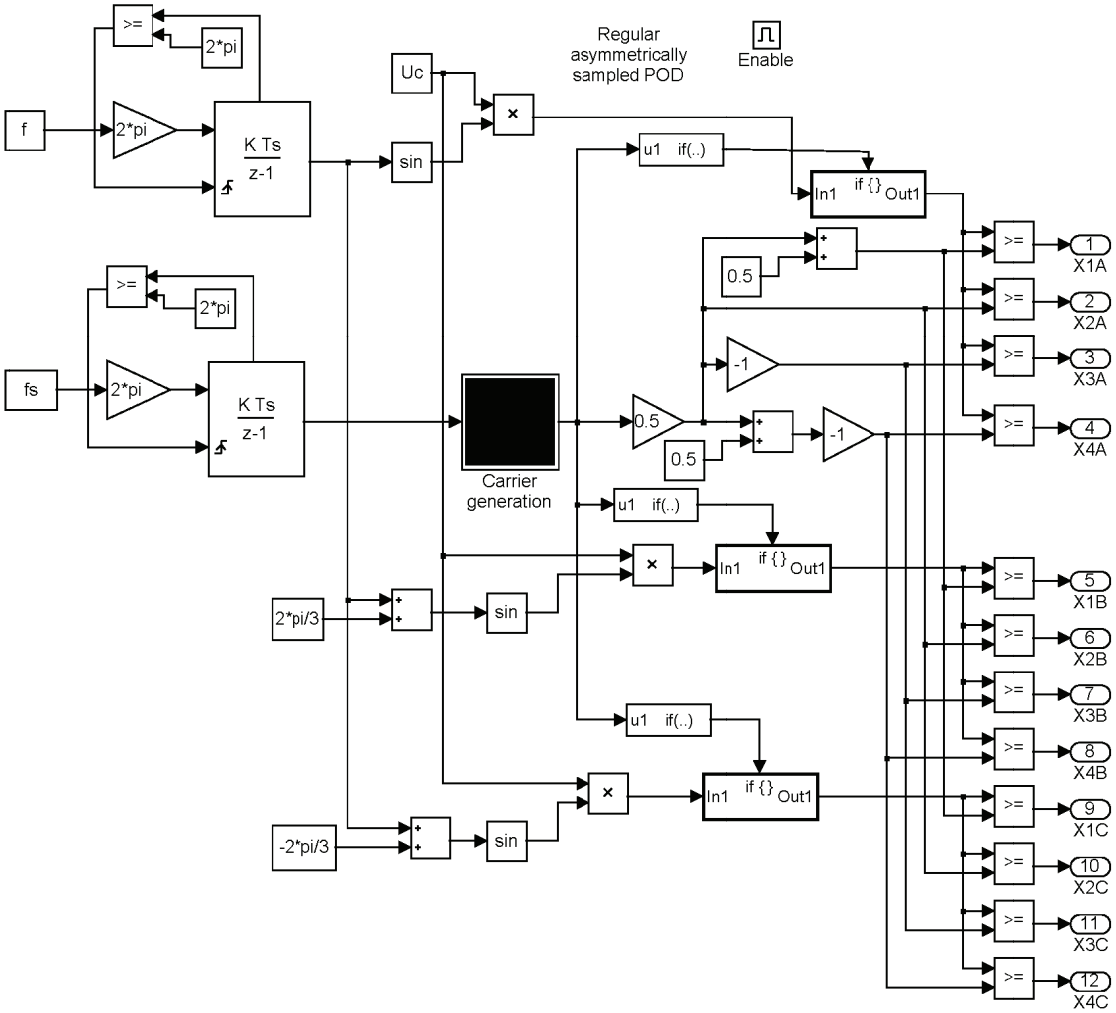


Fig. 105 Block "PWM": Regular asymmetrically sampled POD PWM for a five-level FCI

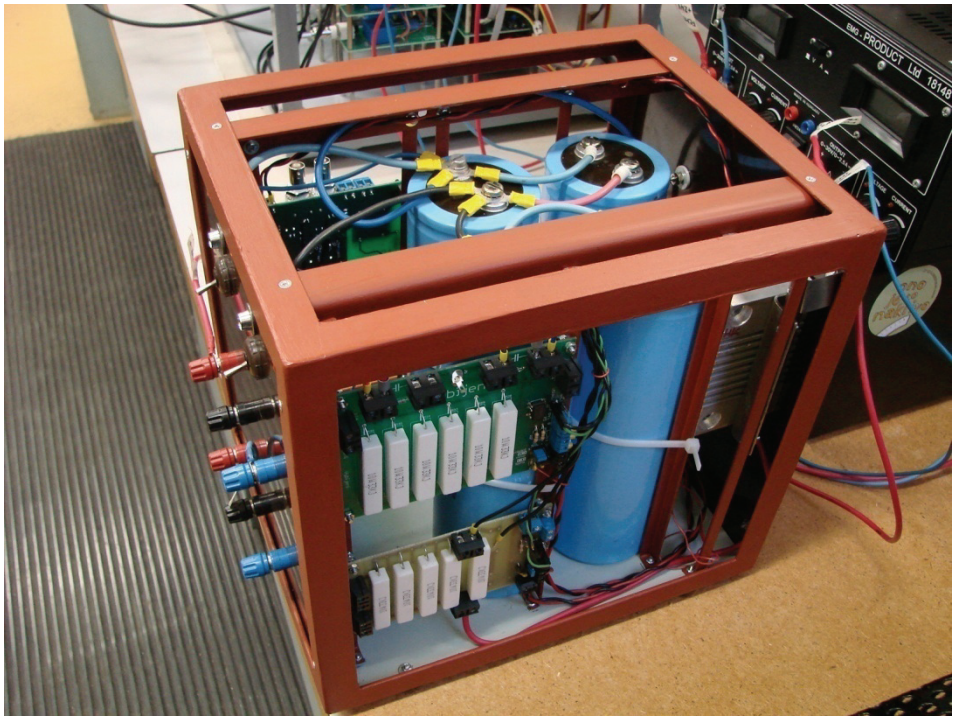


Fig. 106 Compact unit of the DC link

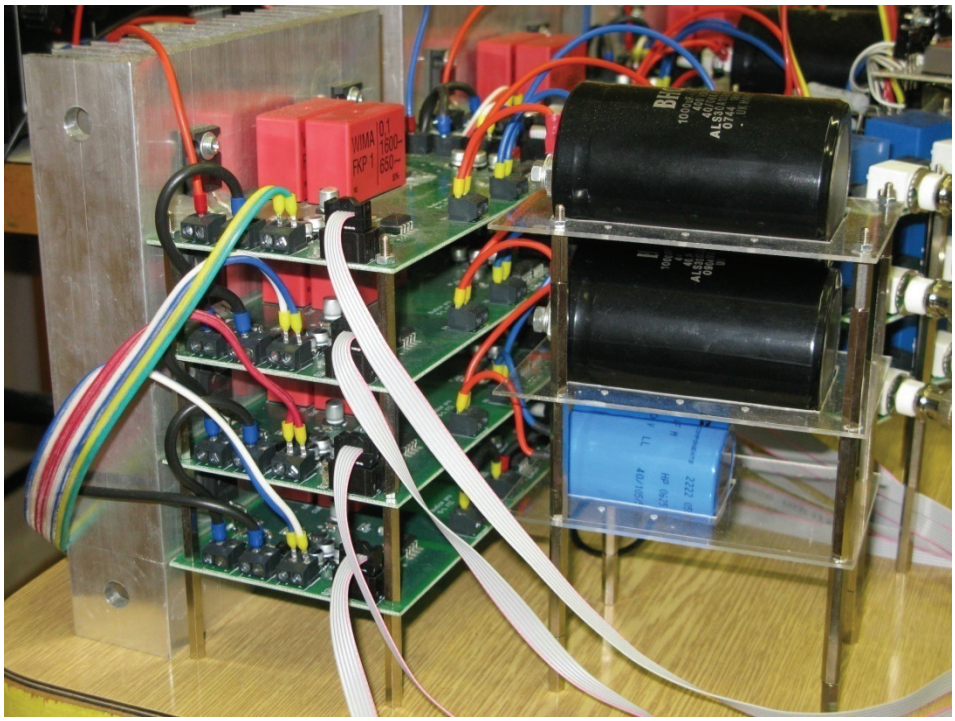


Fig. 107 Driver boards of one phase with connected flying capacitors

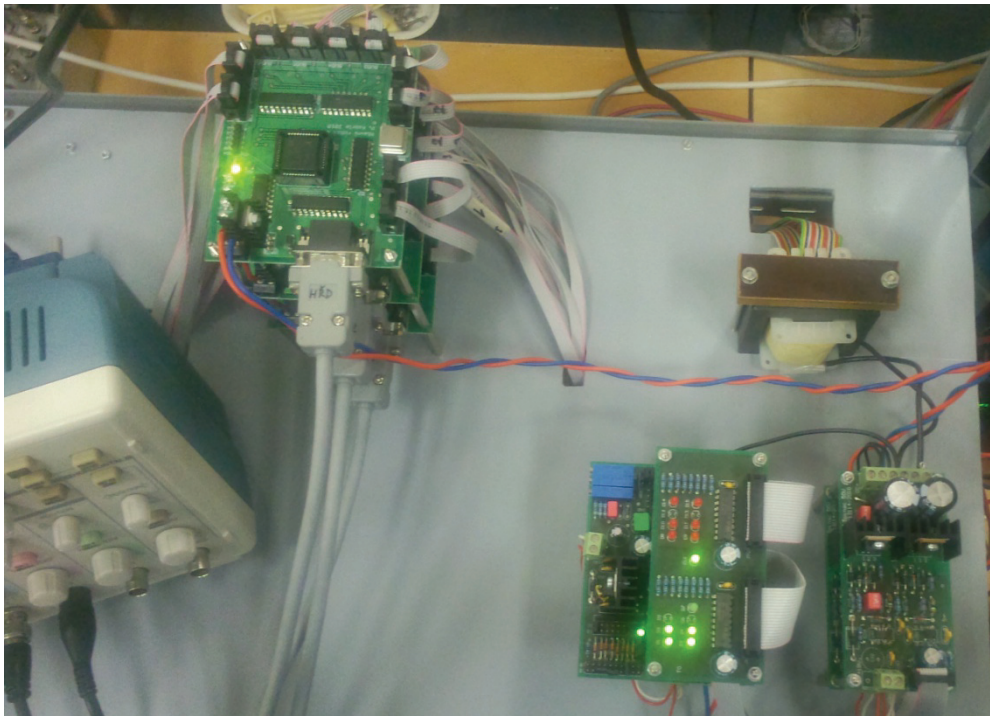


Fig. 108 The switch-mode power supply with the transformer and adjustment boards

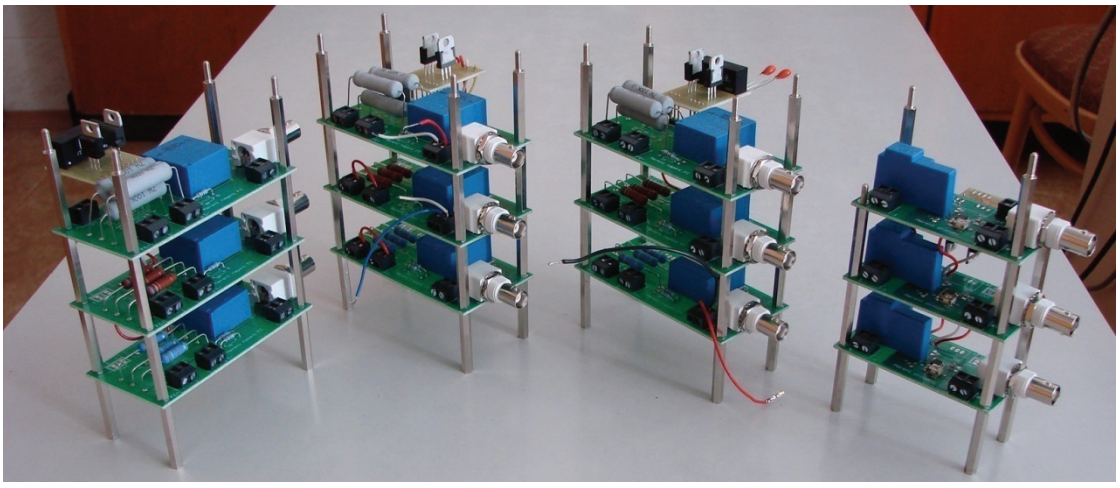


Fig. 109 Voltage measuring boards (9x left) and current measuring boards (3x right)

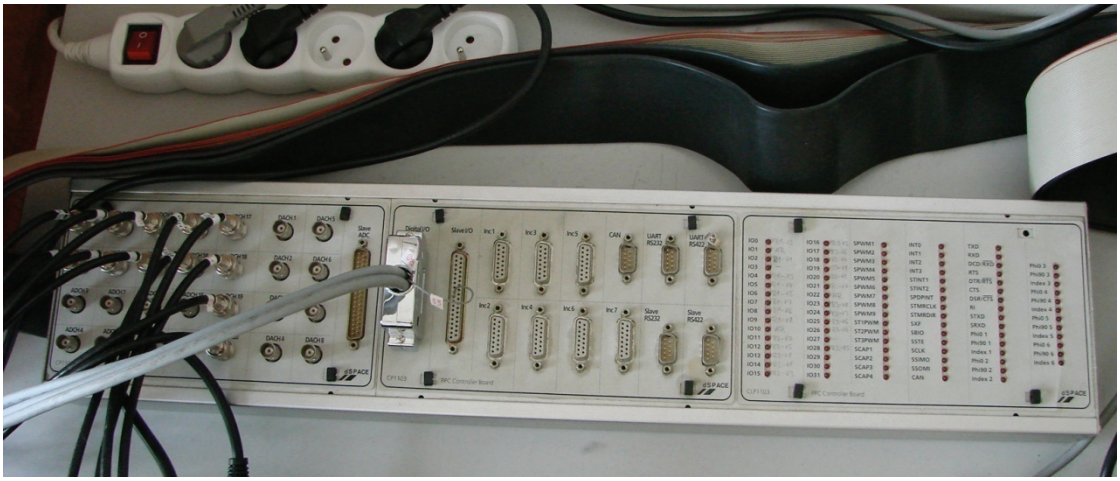


Fig. 110 The dSpace hardware interface

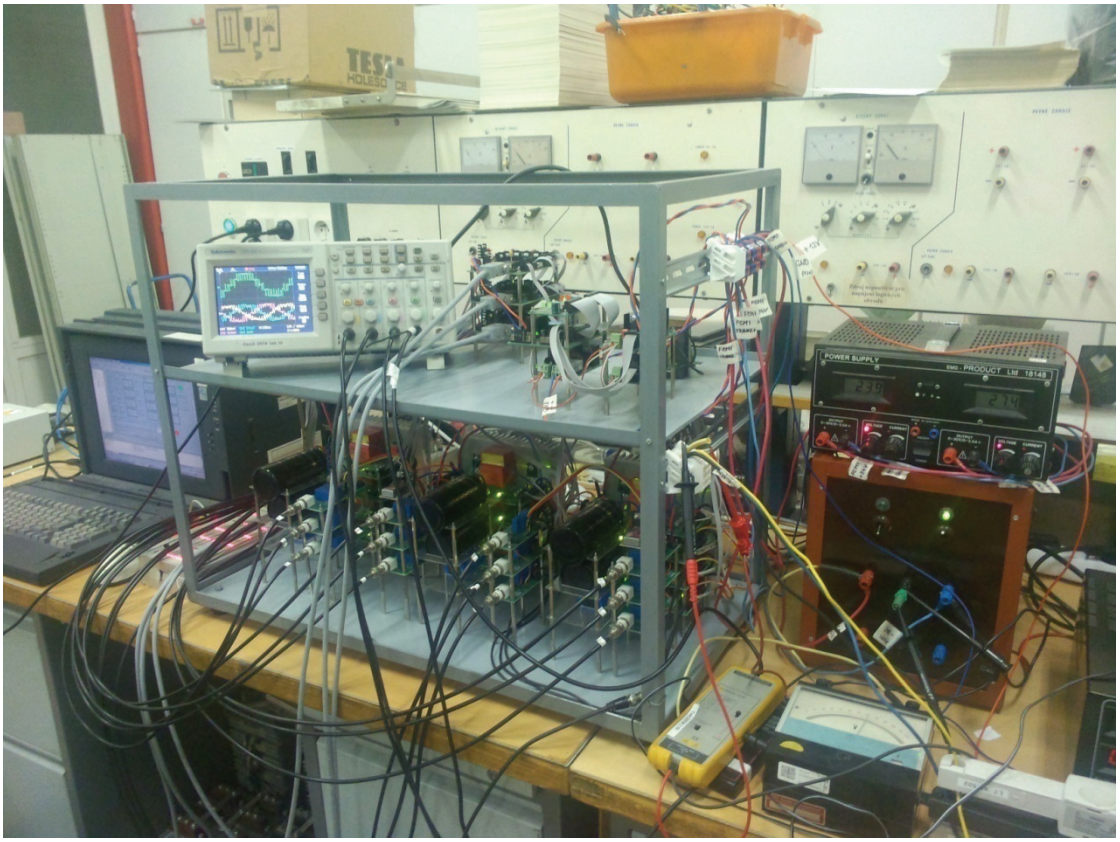


Fig. 111 The view on the whole laboratory model

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