CZECH TECHNICAL UNIVERSITY IN PRAGUE

Faculty of Electrical Engineering

Department of Microelectronics

Habilitation thesis

THERMO-MECHANICAL DESIGN OF ELECTRONIC SYSTEMS

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Prague, 2012

Preface

My very special thanks go to the Prof. Miroslav Husák the head of department who trusted upon my efforts and encouraged me in taking specific research paths, who managed to introduce me into the academic research, which still enormously pleases me. I would like to thank Prof Pavel Hazdra for for valuable advice in writing of this work.

I would like to express my gratitude to all my colleagues at the department of Microelectronics for creating an atmosphere which is at the same time both relaxing and encouraging. In particular, I would like to thank the "Microsystem group", with whom I have had the great privilege of working.

I would like additionally acknowledge all people that share their professional knowledge with me: Tibor Lalinský (SAV Bratislava), Gabriel Vanko (SAV Bratislava), Robert Werkhoven (TNO Eindhoven), Jos Kunen (TNO Eindhoven), Xavier Perpina (CNM Barcelona), Xavier Jorda (CNM Barcelona, Peter Bancken (Philips Eindhoven), Jim Mahon (Cadence San Jose, US), Anand Raman (Cadence San Jose, US) and many others.

Some PhD students have taken the opportunity to contribute to the research described herein. I thank Jan Formánek, for his sincere enthusiasm and persisting work efforts in CSSL project.

Scientific research of any kind is unmanageable without funding. First and foremost, I would therefore like to thank the CSSL ENIAC Project (7-FP EU) – „Consumerizing Solid State Lighting",MorGaN – Project (7-FP EU – 2008-2011) – „Materials for Robust Gallium Nitride", NATO Science for Peace international project, GAČR Intelligent Micro and Nano Structures for Microsensors Realized with Support of Nanotechnology (2009-2013, GA102/09/1601), Miniature intelligent system for analyzing concentrations of gases and pollutants, particularly toxic (2010-2015, MV0/VG - Ministry of Interior).

My family, keeping the most important for the end, I tremendously have to thank them for everything they have meant to me the past years, for their patience and forbearance.

Brief Summary

This work summarises my research results and activities carried out on Czech Technical University, Faculty of Electrical Engineering, Department of Microelectronics over the last seven years. The habilitation thesis has the intention to provide comprehensive work, which is focused on the design, numerical modeling and characterization of temperature affected electronic components and sensors. Relating link in this work is investigation of the thermo-mechanical phenomena in the design and optimization of new electronic systems and sensor structures together with estimation of lifetime and causes leading to failure.

The work describes thermal management design and reliability evaluation and new accelerated testing method of new 806 lumen SSL retrofit lamp that should replace current 400 lumen master LED glow lamp; design, modelling and characterization of new micro machined GaAs and GaN based high temperature hot plate thermal converters for metal oxide gas sensors; design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology and optimization of the dynamic behaviour of the sensor; and design and accurate numerical modelling of Drumskin pressure sensor packaging system with thermo-mechanical evaluation of stresses induced in the solder joints of the pressure sensor chip at high operating temperatures and different applied pressures.

Anotace

Tato práce si klade za cíl přehledně vyzdvihnout moje vědecké výsledky činnosti, kterých jsem dosáhl za posledních sedm let na katedře mikroelektroniky Českého vysokého učení technického v Praze, Fakultě elektrotechnické. Jednotící linií této habilitační práce je teplotně-mechanický návrh, počítačové modelování a charakterizace elektronických systémů a mikro senzorů. Práce se soustřeďuje zejména na modelování a charakterizaci teplotních vlivů z hlediska mechanického návrhu elektronických komponent a mikro senzorů a také problematikou určení životnosti a potenciálních slabých míst návrhu.

Prvé téma práce se zabývá potřebou zavedení moderních technologií výkonných světelných zdrojů, které jsou zejména aktuální po ukončení výroby 60 W žárovek v Evropské unii k 1. září 2011. Dnes jsou k dispozici dvě alternativní technologie: úsporné zářivky nebo světelné zdroje založené na technologii LED. Osvětlení pomocí LED diod je v posledních několika letech velice rychle se rozvíjející alternativou, která představuje díky nízké spotřebě, vynikající účinnosti a vysoké životnosti budoucnost ve svícení nejenom v průmyslu, ale především v domácnostech. Dalšími nespornými výhodami LED osvětlení je možnost inteligentního řízení světelného výstupu jako např. barevné teploty a intenzity, atd. Práce detailně popisuje návrh nové LED žárovky se světelným výstupem 800 lumenů (ekvivalent 60 W), návrh elektronických částí jako je elektronická deska s LED, dále otázkou teplotního managementu a předpovídání spolehlivosti. Světelné zdroje založené na LED technologii se kromě vynikající účinnosti také vyznačují extrémně dlouhou životností (25 – 50 tis. hodin). Testování doby života takových

systémů je velice obtížné právě díky dlouhé době životnosti. Klíčovou problematikou v této oblasti je odhalení potenciálních mechanismů vedoucích k selhání a určení jejich umístění. V práci jsou popsány nové metody pro zrychlené testování elektronických komponent polovodičových světelných zdrojů. Numerické modelování teplotně-mechanických jevů s výpočtem životnosti je konfrontováno s nově vyvinutými systémy pro testování životnosti a spolehlivosti.

Další rozsáhlé téma, kterým se práce zabývá, se soustřeďuje na problematiku využití III-N polovodičů v moderních MEMS senzorech. Polovodičové materiály ze skupiny III-N mohou být velice atraktivní pro návrh MEMS (Micro-Electro-Mechanical-Systems) senzorů. Tyto materiály vykazují vynikající piezoelektrické vlastnosti, jsou přímo kompatibilní s tranzistory s vysokou pohyblivostí elektronů (HEMT), mají velmi dobrou mechanickou stabilitu epitaxních vrstev umožňující integraci s MEMS senzory a jsou použitelné při vysokých teplotách se zachováním piezoelektrických vlastností. Díky těmto vlastnostem jsou předurčeny ke konstrukci miniaturních senzorů, které pracují při vysokých teplotách. V práci jsou popsány návrhy několika druhů MEMS senzorů založených na III-N materiálech (senzory pro detekci koncentrace plynů, tlakové senzory pro vysoké teploty využívající piezoelektrický transdukční mechanismus v HEMT struktuře). Nedílnou problematikou vysokoteplotních senzorů je také problematika návrhu vhodného pouzdra, která je také v práci diskutována.

Poslední téma, zaměřené na návrh analogových integrovaných obvodů, se mírně odchyluje od výše zmíněné problematiky a její jednotící linie. Jelikož však tvoří velice podstatnou část mého vědeckého působení na ČVUT, dovolil jsem si jej zařadit do této práce.

List of symbols and abbreviations

AC	Alternating current
ADC	Analog Digital Converter
AMS	Analog Mix Signal
CFL	Compact Fluorescent Lamp
CMOS	Complementary Metal Oxide Semiconductor
CTU	Czech Technical University in Prague
DC	Direct current
DNL	Differential Non Linearity
EVM	Error Vector Magnitude
FEA	Finite Element Analysis
FEM	Finite Element Method
HALT	Highly accelerated life testing
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
INL	Integral Non Linearity
IR	Infra-Red
LED	Light Emitting Diode
MBE	Molecular Beam Epitaxy
MEMS	Micro Electro Mechanical Systems
MOCVD	Metal Organic chemical vapour deposition
MSPS	Mega Samples Per Second
MTC	Micromechanical Thermal Convertor
P-T	Power to Temperature conversion characteristics
Q	Generated internal heat
RF	Radio Frequency
RFMPS	Radio Frequency Microwave Power Sensor
SSL	Solid State Lightning
TIM	Thermal Interface Material
TS	Temperature sensor
VCO	Voltage Controlled Oscillator
WLAN	Wireless local area network
c_p	Specific heat
E	Young's modulus
H_1	Constant of hyperbolic sine function constitutive model by Schubert at al.
k	Thermal conductivity
k_B	Boltzmann constant
n	Constant of hyperbolic sine function constitutive model by Schubert at al.
T	Temperature
T_j	Junction temperature
α	Constant of hyperbolic sine function constitutive model by Schubert at al.
α_E	Thermal expansion
ε	Equivalent total strain
ε_{cr}	Equivalent creep strain
ε_{el}	Equivalent elastic strain
ε_{pl}	Equivalent plastic strain
ε_{th}	Equivalent thermal strain
λ	Thermal Conductivity
ν	Poisson ratio
σ	Equivalent stress
σ_A	Equivalent alternating stress
σ_M	Equivalent mean stress
σ_{MAX}	Maximum of equivalent stress
σ_{MIN}	Minimum of equivalent stress

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1 Introduction and Author contribution

1.1 Background and Motivation

Since defence of my PhD thesis elaborated in 2004 my professional activities in the field of research and education had been related to the two main activities. The first topic follows a research activities carried out during my PhD that has been with initiation of new projects extended to design and numerical modelling of new thermally based MEMS gas sensors and pressure sensors. Another parallel activity came with design of a new SSL lamp concept. The second activity has been focused on the design of integrated circuits and systems. In this field I made a four-month internship within Cadence Company in 2005 where I worked as a member of R&D team concentrated on development of a new RF CMOS development kit. After the end of internship I become an external contractor for above mentioned R&D team.

The main purpose of this work is to provide a comprehensive summary dedicated to the design, numerical modeling and characterization of thermally affected electronic components and micro sensors. This corresponds to the first activity stated above. Relating link in this work is the investigation of thermo-mechanical phenomena during the design and optimization process of new electronic systems and micro sensor structures (typically based on GaN and GaAs materials) together with estimation of components lifetime and explanation of the effects leading to system failure.

1.2 Organization of the habilitation thesis

The main section of this work is organised to six chapters that describe my research activities over the last seven years. Each chapter begins with a short "Motivation and author contribution" that outlines the main research goals referred to the research presented in the chapter and definition of my own contribution that is related to the working context. This explanation is followed by description of research importance in defined area. Each chapter is concluded and results are discussed together with reflections on possibilities for improvement of the results. Moreover, continuation of the research in that field is added.

Chapter 2 titled "**Solid State Lamp design**" describes design of new 806 lumen SSL retrofit lamp that should replace current 400 lumen master LED glow lamp. The chapter describes my research activities in thermal modelling and validation of master LED glow retrofit lamp, thermo-mechanical evaluation of master LED glow. Design of new LED boards for 806 lumen lamp is described in detail. Development of new accelerated characterization methods for SSL LED boards together with reliability and life time modelling of LED boards is reported in the end.

Chapter 3 titled "**GaN, GaAs and Silicon based Micromechanical Free Standing Hot Plates for Gas Sensors**" has the intention to provide the reader with an outlook on the approaches that have been used to design new micro machined GaAs and GaN based hot plate thermal

converters, which are considered to operate with high temperature metal oxide gas sensors. These sensors can analyse various gases, such as CO, H_2, NOx and hydrocarbons.

Chapter 4 titled "**Design and Characterization of GaAs MEMS thermal converter**" outlines the design and thermomechanical modelling of the new GaAs based RF Microwave Power Sensor (RFMPS) microsystem. The chapter discusses the procedure for performing a thermomechanical analysis of thermal GaAs-based MEMS devices. Main focus is on increasing reliability which requires temperature distribution controlling in single parts of the device and definition of high thermo-mechanical stressed areas that can be critical in relation to the mechanical failure of the device.

Chapter 5 titled "**Thermo mechanical and piezoelectric design of the pressure sensor** " presents numerical modelling of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) designed for new pressure sensor. Thermomechanical behavioural study focusing on the extremely high temperature pressure sensor package is outlined. The study provides accurate modelling and simulation of Drumskin pressure sensor packaging system developed by IVF (Sweden). Research is mainly focused on thermal evaluation of induced stress in the solder joints and in the glass frit that is used to seal the sensor chip at high operating temperatures.

Chapter 6 titled "**IC design**" presents some results of my activities performed in Cadence, San Jose, CA and following activities carried out during next three years with Cadence RF R&D team. This chapter does not belong fully in the main section of presented work, which aims to seamlessly handle the problems of lifetime and thermal design of electronic systems. The chapter has been included because IC design research and teaching activities at the CTU forms an important part of my professional work.

Scientific contributions and general conclusions of this habilitation thesis work are summarized in chapter 7.

1.3 Research Contribution

Habilitation thesis summarises my research results carried out at Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics.

The research work presented in this work could be characterised by a cross-disciplinary approach that brings together theoretical aspects, numerical modelling and experimental techniques of thermal and thermomechanical phenomena which takes place in micro sensors and electronics systems and components. The work has the objective to provide comprehensive summary of research focused on the design, numerical modeling and characterization of temperature affected electronic components and sensors. Relating link in this work is examination of the thermo-mechanical phenomena in the design and optimization of new sensor structures, estimation and calculation of electronic system lifetime and effects that results a failure of the electronic system. Thermomechanical stress induced in an electronic system composed from diverse materials (that have a different coefficient of thermal expansion) could be the main cause of catastrophic failure, especially when the

system operation temperature is high or when the temperature alternate in an extensive range. For the reason that reliability of newly developed electronic systems is one of the major criteria, numerical modelling and optimization of thermomechanical stresses are key issues during new system development. State of the art in numerical modeling of thermo-mechanical phenomena of electronic components is to determine the behavior of the entire system at critical locations. Detailed examination of the physical phenomena leading to the discovery of failure mechanisms have been carried out. In particular cases, where the dimensions of the system are several orders of magnitude larger than examined location, the multi-scale numerical modelling approach has been used.

The main attention of the thesis in particular is given to thermal and thermomechanical numerical modelling and characterization of solid state lightening (SSL) LED Lamp. More insights are observed in the thermal and thermo-mechanical behaviour. Different lamp shapes are also explored (Chapter 2.2.2). The work presents an accurate 3-D modelling of several LED board technologies. More efforts are concentrated on thermal modelling, thermo-mechanical evaluation and lifetime prediction of newly designed LED boards in order to compare their performances. These LED boards are proposed as a possible replacement technology for existing FR4 board used in current 400 lumen retrofit SSL lamp (Chapter 2.4). The advantages of these innovative LED board technologies are discussed. Moreover, innovative approach in modelling and validation of 800 lumen retrofit SSL lamp is proposed. Lifetime numerical analysis have been carried out to study reliability and lifetime limits of each new component, using thermal boundary conditions which was extracted from the thermal simulation of a whole SSL lamp (Chapter 2.3). Additionally, thermal cycling that lead to the LED board failure due to thermal fatigue have been calculated and validated. Elastic-plastic analysis with temperature dependent stress-strain material properties has been performed. The objective of new design is to optimize not only the thermal management by thermal simulation (Chapter 2.3), but also to find potential problems from mechanical failure point of view (Chapter 2.4.3). Development of a new methodology for reliability design of SSL LED boards is discussed (Chapter 2.5). One of the most valuable scientific contributions of this part is development of accelerated characterization testing methods for SSL lamp LED boards. New method replaces traditional thermal cycling or power cycling characterization test, which is very time-consuming (Chapter 2.6). This methodology is based on creep relaxation effects in solder joints (Chapter 2.6.8). Accumulated creep strain (or accumulated energy) in solder joints has to be defined during thermal cycle that is followed by calculation of equivalent mechanical force that imply comparable accumulated creep strain value in solder joint regions of interest. This new accelerated tests can dramatically speed up reliability evaluation process keeping testing accuracy in the range of 20%.

Correct knowledge of mechanical and thermal properties of essential materials used in micro sensors and MEMS is critical for optimum geometric and functional design. The extraction of precise physical properties is rather difficult due to the size effects and the complexity of the assemblies. Further work is intended to present new design, modelling and characterization of micro machined GaAs and GaN based hot plate thermal converters, which are considered to operate with high temperature metal oxide gas sensors that can analyse various gases, such as CO, H2, NOx and hydrocarbons (Chapter 3). New solution increases sensitivity (through the use of new materials as GaAs and GaN) and decreases power consumption, due to the miniaturization and MEMS technology that replaces wide spread screen printing technique on

small ceramics substrates. Newly designed free standing MEMS membrane provides very good thermal isolation between the heated gas sensitive active part and substrate, which remains nearly at ambient temperature. The work discusses needs for sensitivity and selectivity increase that can be realised by higher temperature of active gas sensing parts. However, well developed silicon technology is thermally limited up to 300 ^{0}C, while use of new materials as GaN (Chapter 3.2) brings advantage of much higher operational temperature (up to 1000 ^{0}C). The work focuses on new hot plates design (Chapter 3.3) and compares performance of three hot plate substrate material, e.g. Silicon, GaAs and GaN. State of the art in high temperature MEMS design is correct thermomechanical modelling and optimization of uniform thermal distribution in active sensing area (Chapter 3.4). Thermo-mechanical analyses ware used to simulate steady state and transient thermal performance. The mechanical coupling was included to optimize mechanical integrity of the hot plates. Simulation results were compared with the experiment in the case of GaAs hot plate (Chapter 3.4).

Another work that can be included to this portfolio has the intention to provide with design and characterization of the new GaAs based Microwave Power Sensor (MPS) microsystem (Chapter 4). Transmitted power is the most important quantity considered in RF systems. Usual approach to transmitted power measurement is based on the detection of absorbed power waves (incident and reflected) that requires complicated multiple power meter structures and need complex calibration. An improved method of the absorbed power measurement is based on thermal conversion where, absorbed radio frequency (RF) power is transformed into thermal power inside of a thermally isolated system. This section discusses the micromechanical thermal convertor design (Chapter 4.3) and procedure for performing a thermomechanical analysis of thermal GaAs-based MEMS devices (Chapter 4.3.1). It will provide the general procedure how thermal analysis should be made and model equations used to describe conduction, convection, radiation and mechanical effects caused by inhomogenous temperature distribution. By means of thermo-mechanical simulations, we propose a GaAs Micromechanical Thermal Converter design and a layout of the active sensor elements (HEMT heater and a temperature sensor TS) placed on the MTC structure. Simulation results were compared with the experiment. The main scientific contribution of this session is Design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology in terms of the temperature distribution and optimization of the dynamic behaviour of the RFMPS system with respect to changes of the input RF power dissipation, which is generated by integrated HEMT transistor.

Many industrial applications require electronic devices that can operate in harsh environments such as an extreme heat, high pressure, large electric fields or chemically aggressive environment. For such applications III-Nitrides (III-Ns) are very attractive semiconductor materials that can be used for pressure and stress sensor applications because of their excellent piezoelectric properties

Chapter 5 deals with numerical modelling of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) designed for new stress sensor which can be potentially applied for dynamic high temperature pressure sensing (Chapter 5.3). High temperature devices need special package design that stands for extreme conations. Next section deals with accurate modelling and simulation of high temperature pressure sensor packaging system and thermomechanical evaluation of mechanical stresses induced in the solder joints and the glass frit that is used to seal the pressure sensor chip at high operating temperatures and different

applied pressures (Chapter 5.4). The most critical problem with packaging for high temperature environments is accumulated thermo-mechanical stress induced during thermal cycling process by the different temperature expansion coefficients of materials used for the packaging and interconnect (Chapter 5.5). Evaluation of the package influence on encapsulated sensor structure at high operating temperatures and different applied pressure has been also investigated (Chapter 5.6).

The last part of this thesis is focused on IC design research activities (Chapter 6). I am aware that this chapter does not fit entirely into coherence with previous topic. On the other hand, the IC design constitutes an essential part of my research and teaching activities on CTU. Therefore I decided extend this work by this section. Chapter provides an overview of the most important activities in the last seven years, with couple of examples.

The most valuable scientific contributions:

- *Development of accelerated characterization testing method for LED boards that replaces traditional thermal cycling of power cycling characterization test by LED board mechanical bending method;*
- *Design, modelling and characterization of new micro machined GaAs and GaN based high temperature hot plate thermal converters for metal oxide gas sensors that can analyse various gases (CO, H_2, NOx, hydrocarbons);*
- *Design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology in terms of the temperature distribution and optimization of the dynamic behaviour of the RFMPS system with respect to changes of the input RF power dissipation, which is generated by integrated HEMT transistor;*
- *Numerical modelling of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) designed for new stress sensor to be potentially applied for dynamic high temperature pressure sensing;*
- *Design and accurate numerical modelling of drumskin pressure sensor packaging system and thermomechanical evaluation of mechanical stresses induced in the solder joints and the glass frit that is used to seal the pressure sensor chip at high operating temperatures and different applied pressures*

2 Solid State Lamp design

This chapter deals with design of new 806 lumen SSL retrofit lamp that should replace current 400 lumen master LED glow lamp. The research work has been done in frame of the ENIAC JU project CSSL[1] that aims to develop and demonstrate inexpensive smart solid-state light sources through improvements in technology and application opportunities.

Intention of this chapter is to collect current research results published by the author (see table) into one coherent unit, which is completed by detailed research review, theory basis and new unpublished results describing a new accelerated LED board lifetime calculation and validation methods.

Table 2-1: published works related to the chapter

Paper title	Full reference
Design for reliability of solid state lighting systems	[1]
High power solid state retrofit lamp thermal characterization and modelling	[2]
Thermo-mechanical evaluation and life time simulation of high power LED lamp boards	[3]
Thermal resistance investigations on new leadframe-based LED packages and boards	[4]
Thermal simulation and validation of 8W LED lamp	[5]

2.1 Motivation and author contribution

LED (Light-emitting diodes) lamps are a fast emerging technology which is considered as the true alternative to the Compact Fluorescent Lamp (CFL). At present days we can see many commercial products that are usually available for professional use; however there is not often any LED retrofit lamps that can fulfil traditional expectations of consumers in terms of lamp shape, price, light output and other functionalities.

My own research contribution can be summarized in following research areas:

- *Development of calibrated thermal model of master LED glow retrofit lamp with validation(together with my PhD student Jan Formanek) (chapter 2.2.2)*
- *Design of new 806 lumen retrofit lamp (as a member of design team) (chapter 2.3)*
- *Calibrated thermo-mechanical and reliability model of LED board for master LED glow retrofit lamp (together with my PhD student Jan Formanek) (chapter 2.5).*

[1] The Consumerizing Solid State Lighting (CSSL) project aims to demonstrate affordable Smart Solid State Light sources for consumers via both technology and application routes. The proposed CSSL project works vertically across the entire value chain from embedded electronics, LED die, light source, consumer luminaires, controls and dimmer to partnerships with utility companies in order to bring SSL retrofit products to European consumers with innovative pricing scheme.

- *Design and evaluation of new LED boards from thermal, mechanical and reliability point of view (together with my PhD student Jan Formanek) (chapter 2.5.2)*
- *Development of new accelerated characterization methods for SSL LED boards (together with my PhD student Jan Formanek) (chapter 2.6)*
- *New accelerated validation method of LED boards that replaces traditional thermal cycling test (together with my PhD student Jan Formanek) (chapter 2.6.8)*

2.2 Introduction and state of the art

In the last few years the use of SSL (Solid state lighting) lamps has been increasing almost exponentially. Solid-state lighting has the potential to revolutionize the future lighting industry. It is predicted that the LED replacement lamp market will speed up progresses in commercially available LED performance in the next a few years, as well as cost reduction are expected. SSL technology uses semiconductor light-emitting diodes (LEDs) as sources of lights instead of wildly used incandescent electrical filaments or plasma in fluorescent lamps. The term "solid state" is derived from meaning that light is emitted by solid-state electroluminescence. One of the biggest advantages in comparison to incandescent lighting is that SSL produces a light with reduced heat generation or other parasitic energy dissipation. Other benefits that come with SSL technology are: more than ten times longer life time in comparison with incandescent light technology, better quality of light output (LEDs produce minimum ultraviolet and infrared radiation), smaller volume of light bulb (if needed). Table 2-2 compares SSL lamps to incandescent and fluorescent lamps from power dissipation and life time point of view. The data are related to 800 lumen light output:

Table 2-2: Commercially available lamp comparison

Lamp type	Incandescent	Fluorescent	SSL lamp
			
Input Power (W)	60	18	12
Life time (hours)	~1000	~ 8000	20 000 – 50 000
Retail price	<1€	5-10€	10-35€
Total Radiant Energy	81%	51%	20-30%
Visible light	8%	21%	25-30%
Infra-red emission	73%	37%	~0%

Moreover, a typical SSL lamp is fully dimmable (depends on driver type) like an incandescent bulb, but unlike a fluorescent lamp that has tendency to flicker. SSL lamps also do not emit ultraviolet radiation. That can cause problems to wallpaper and artwork fading. SSL lamps colour can be easily shaded from cool blue to warm yellow to suit all preferences. Further aspect which is very important today is that SSL technology is considered to be "green technology" which means that environmentally harmful materials as mercury, lead, etc., are not used.

On the other hand, SSL lamps cost considerably more than incandescent lamp. However, when life time of SSL lamps and long term energy consumption are taken into account, money saving can be more apparent in behalf of SLL technology. Moreover, the future SSL costs are expected to be reduced dramatically.

2.2.1 SSL lighting technologies, design, life time and reliability

Light emitting diodes historically have been used for indicators at the beginning and produced low quantities of heat. Bob Biard and Gary Pittman found in 1961 that GaAs emit infrared radiation when electric current is applied [6]. The first practical visible-spectrum LED was technologically advanced in 1962 by Nick Holonyak [7]. While the efficacy of these first LEDs was extremely low (~ 0.1 lm/W), research was continued to improve the technology over the next four decades, achieving higher efficiencies and expanding the range of emission wavelengths through the engineering of new III-V semiconductor alloys. Well known Moore's Law predicts the doubling of the number of Si transistors in a chip every 18–24 months. In the same way for LEDs, luminous flux (measured in lm) appears to follow Haitz's Law, which predicts that LED flux per package doubles every 18–24 months for more than 30 years [8]. Today we are seeing even more fast progress.

From the time of invention, LEDs have been used in many industrial applications as for example: displays (outdoor displays, electronic scoreboards), LCD back lighting [9] (mobile phones, notebooks, cameras, monitors, TVs, etc.), automotive lighting [10], in communication technologies. The introduction of high brightness LEDs with white light output have managed to a movement towards general indoor and outdoor illumination applications [11]. The increased electrical driving currents have focused more attention on the thermal management and new designs of LED power packages. The luminous efficiency of LEDs brakes 200 lumens per watt in 2011[2] and the thermal challenges are opening new research areas from LED chip design level to the system level thermal management.

Figure 2.1 shows historical and Predicted Efficacy of Light Sources [12]. Note: today a new LED with efficiency over 200 lumens has been already introduced.

[2] 200 lumens per watt were achieved by CREE LEDs with a colour temperature of 4579k and nominal drive current of 350mA.

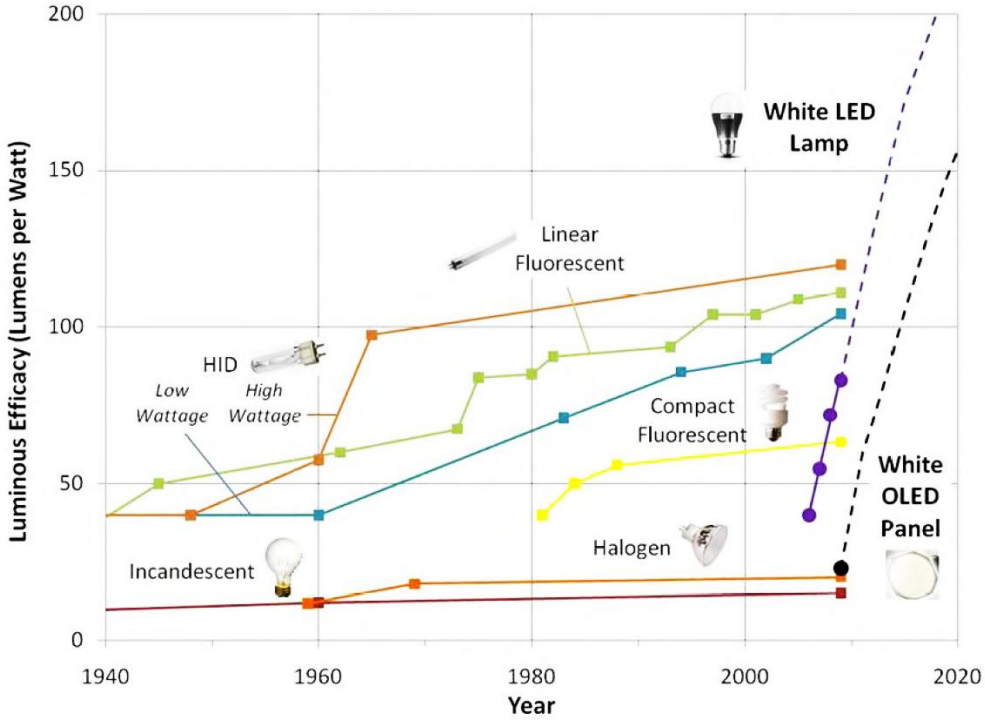


Figure 2.1: Historical and Predicted Efficacy of Light Sources [12]

To generate white light output for general illumination, a narrow spectral band of an LED's must be transformed into white light or more discrete emissions must be mixed. White-light LED conversion is typically based on three common approaches:

- *phosphor-conversion;*
- *discrete colour-mixing;*
- *hybrid consisting of phosphor (white) and monochromatic packages (or different LEDs in a single package).*

The phosphor-converting LEDs produce white light by converting of the blue light (generally around 460 nm) emitted directly from the LED die with light emission converted by a phosphor [13]. Some of this light is emitted directly, and some of it is down-converted by a phosphor from the 460 nm wavelength to longer wavelengths (e.g., green, yellow, red) with wide-band emissions that is mixed with the blue to produce white light. Main disadvantage of phosphor-conversion technology is difficulty of maintaining consistent-quality of white light due to changes of the temperature, thickness of the phosphor layer, variation of the humidity and aging. As a consequence, noticeable discrepancies in output colour can occur from one LED to another.

Discrete colour-mixing create the white light by colour mixing optics to mix the light output from discrete colored sources. The major advantage of the colour-mixing technology is that it does not contain phosphor that eliminates scattering losses in the emitting of white light. The biggest problem is the absence of efficient green light LEDs. Unfortunately this is main factor that significantly limits achievable efficacy. Moreover, mixing of discrete colours requires multi-die mounting and sophisticated optics.

2.2.2 SSL lamp thermal management, thermo-mechanical issues and reliability

This section summarises most important issues that has to be taken into account while designing new high power SSL lamp. Main goal of this text is to review the latest thermal management technologies with respect to SSL lamp lifetime and reliability and show the state of the art in modern SSL lamp design.

2.2.2.1 Thermal management

Almost all modern light sources convert electric power into radiant energy and heat in various proportions. While incandescent lamps emit mostly infrared (IR), with a small amount of visible light, SSL lamps generate little or no IR or UV, but convert only 20%-30% of the power into visible light. The rest is converted to the heat that must be conducted from the LED die and through LED package to the underlying LED board, heat sink and housing. Table 2-3 shows the proportions of input power to heat and radiant energy conversion for various white light sources. Almost all total radiant energy in case of SSL lamp is converted to visible light. This is main advantage above incandescent and fluorescent lamps. On the other hand big portion of the heat is generated here. This is a reason why thermal management is perhaps the most important aspect of successful SLL lamp system design.

Moreover the effectiveness of whole SSL lamp system is not only related to LEDs light conversion, but also to the driver losses, and power dissipation in light conversion element. Most of the input power in an LED converts to heat rather than light (about 70% heat and 30% light).

Table 2-3: Estimated proportions of input power to heat and radiant energy (including visible light) conversion for various white light sources

Lamp type	Incandescent	Fluorescent	SSL lamp
Infra-red emission	73%	37%	~0%
Heat	19%	42%	70-80%
Total Radiant Energy	81%	58%	70-80%
Visible light	8%	21%	25-30%
Total energy	100%	100%	100%

If the heat is not removed, the LEDs run at high temperatures, which not only lower their efficiency, but also make the LED less reliable. The dissipated heat of these components is removed by conduction within the SSL lamp system and by convection and radiation outside the lamp on a heat sink and bulb surface. Thermal management of SSL lamp is a key issue impacting not only efficiency (in lm/W), but also colour consistency and of course, lifetime. The junction temperature of LED components depends on the heat generation caused by loses during light emitting and thermal dissipation within the SSL lamp from the LED die through the LED package, board, heat sink and finally to the ambient (Figure 2.2, [14]). In order to have the junction temperature as low as possible, it is necessary to minimize all thermal resistances, starting with the LED component, itself. In addition, several packaged LEDs are connected in

series on a substrate (LED board) in SSL lamp, increasing the challenges to face during their thermal design.

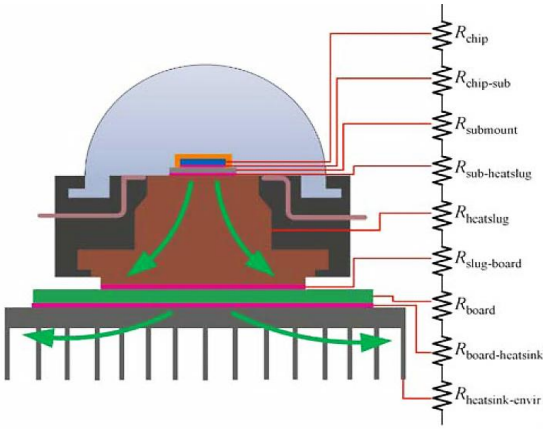


Figure 2.2: Thermal resistance network of Luxeon LED (there are at least four interface resistances. These interfaces are bottlenecks of heat conduction and should be paid special attention) [14]

LEDs are typically encapsulated in a transparent resin, which is a poor thermal conductor. Nearly all produced heat is conducted through the back side of the LED chip. SSL lamp cooling system is composed of many parts. LED chip is usually connected by flip-chip technology to LED package that create a thermal path from LED junction to bottom side of the package solder pads. One or more LEDs packages are typically spread out on LED board which is typically attached by TIM (thermal interface layer) to extension thermal cone that conducts heat to heat sink where the heat is distributed to ambient. Moreover another heat sources in SSL lamp are an electronic driver and phosphorus conversion dome.

In 1998, Lumileds developed the first high-power LED packaging[3] – Luxeon, which embeds a metal large shell size for heat dissipation. This package has been adopted as main packaging type by many corporations such as Osram and Seoul Semiconductor. This packaging method reduces thermal resistance to about 10 K/W and can dissipate heat power up to 5W [15]. In 2006, with the improvement of used materials and attach technologies, the Luxeon K2 package can allow junction temperature up to 150°C for white LED with a driven current up to 1.5 A [16]. To reduce costs and increase the reliability issues, a ceramic based package has been developed by Lumileds (the Rebel component [17]), CREE and others. On the other hand, the thermal resistance of these packages remains typically above 10 K/W. Some of the SSL lamp manufacturers (Osram [18], Nichia [19], Cree [20]) have developed efficient metal based packages which were derived from the Luxeon concept. Those packages are known as leadframe based packages.

LED boards (on which power LEDs are often mounted) technologies that has been developed and used recently uses FR4 boards, metal-core printed circuit boards (MCPCB), IMS (Insulated Metal Substrate). LED board is then attached to a heat sink where TIM (thermal interface layer) that improves heat transfer is used. The TIM's thermal resistance will also vary depending on the type of material used.

[3] Patent no. 6,274,924 "Surface mountable LED package. Filed 11/5/1998, granted 8/14/2001.

Heat and changes of LED temperature directly affects both short-term and long-term LED performance [21]. The short-term performance effects mostly colour shift and reduced light output while the long-term performance results accelerated lumen depreciation and thus shortened useful life. LED operation at higher temperature radically accelerates lumen depreciation and shortened useful lifetime. The Figure 2.3 shows the light output over time for two identical LEDs driven at the same current but with an 11°C difference in LED junction temperature[4]. Estimated useful lifetime (according 70% lumen normative) reduced from about 37,000 hours to about 16,000 hours. A 10 degrees increase in temperature reduces LEDs life by approximately 50% and each following 10 degrees increase will reduce fixture life by another 50%!

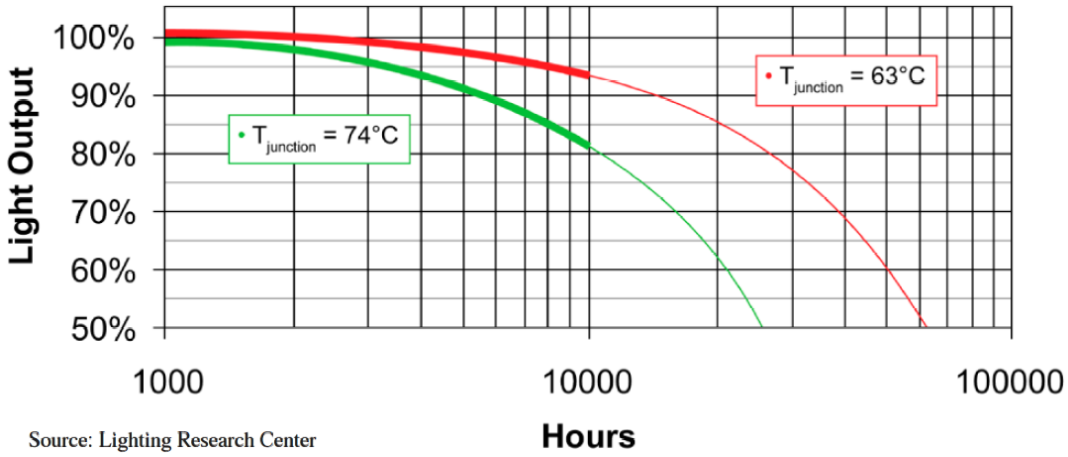


Figure 2.3: Useful life time of high brightness white LEDs at different operating temperatures [22]

In a compact SSL lamp design, the light engine components such as LEDs, drier ICs and electronic components, sensors and phosphor convertor have to be kept in a limited space. Moreover, the required high light output causes high temperatures dissipation inside the limited size of the SSL lamp engine. This can be especially critical for LED junction temperature and driver components temperature. Most of today research works that are dealing with SSL lamp design and thermal management are focusing on the virtual prototyping based on thermal management, thermo-mechanical modelling and reliability predicting, improving of materials selection and fabrication aspects (packaging, connection and integration technologies). Another very important aspect is thermal separation of the LED driver circuitry and phosphor light conversion dome from the LED board. This avoids the heat generated by the driver and light conversion element from raising the LED junction temperature. However, improvement of the lifetime of LEDs at higher operating temperatures has been reached in recent years. Leading manufacturers of high-power white LEDs estimate a lifetime to around 50,000 hours assuming operation at 700 mA constant current at maintained junction temperatures up to 120°C [18] [20]. The LED junction temperature is affected by drive current, thermal path and ambient temperature. Because necessary light output power is given by drive current at given ambient temperature, the LED temperature can be lowered by optimizing of the thermal path.

[4] Experimental data sampled to 10,000 hours and extrapolated beyond

2.2.3 SLL lamp reliability

SSL lamps have properties that difference them from traditional lamps (incandescent, CFL, etc). The most distinguishing features are low power consumption and expected long lifetime. SSL lamps are composed from higher number of diverse components than conventional incandescent lamps. Failure mechanisms are then much different. Conventional incandescent lighting systems fail usually catastrophically, when the filament burns through and no light is emitted anymore. The lifetime of these conventional lamps are usually defined as the time that half of all lamps have failed (B50) [23]. The intensity and change of emitted colour does not play significant role here.

On the other hand, SSL lamps don't usually fail catastrophically. Catastrophic failures can appear when an electronic component or solder join breaks. As an alternative the light output of SSL lamps frequently decreases over time[5]. Lifetime, or "useful life", is defined as decrease of light output power in lumens. The mostly spread normative that has been adopted by many companies is SSL certification which states that an SSL lamp fails when it's light output drops below 70% of the initial light output (L70) [24] [23] [25]. For example the CSSL lifetime specification of 12,000 h (B50L70) indicates that the expected light output of at least 50% of all 60W replacement lamps has to be maintained to a level of 70% (the lumen maintenance level) of the initial 806 lumen light output for a period of 12,000 h[6].

Light degradation in SSL systems can have several reasons and also many different locations: the LEDs themselves, LED package, additional optical sub-systems (LED lens, light conversion dome,…), the driver current output, the connections and interfaces between components, change of operating temperature, etc. [24]. As SSL lighting systems are envisaged to have lifetime (depending on the specific application, thermal management) up to 50,000 h, qualification over the rated lifetime become very problematic before the design of whole SSL system. Unfortunately, up to now there does not exist globally accepted standard tests for SSL lamp reliability issues [26]. One method of LEDs lifetime prediction is accelerated test approach. In this test estimated life time is multiplied by acceleration factor. Therefore, fast and reliable and cost-effective qualification procedures that are based on accelerated tests are required. Some known accelerated tests is based on the simultaneous or sequential application of thermal, mechanical, moisture and electrical loads. Modelling of acceleration factors is usually used to predict long life of SSL lamp components at specific conditions [26]. Chapter 2.6 in this work describes a new "Highly Accelerated Life Testing" (HALT) test methods for LED board testing[7].

[5] Some reasons has been already mentioned in chapter 2.2.2.1

[6] CSSL project specification document

[7] In the semiconductor industry so-called 'highly accelerated stress testing' (HAST) is used combining elevated temperatures, moisture and electrical loads. In electronics industry 'highly accelerated life testing' (HALT) is applied imposing mechanical vibration with temperature increases and electrical loads

2.3 Design of new 806 lumen SSL retrofit lamp

This chapter deals with design of new 806 SSL retrofit lamp that should replace current 400 lumen master LED glow lamp.

SSL (Solid State Lighting) lamps can have a life time up to 50 000 h, but the life time among others effects strongly depends on LED die temperature [23]. Good thermal and thermo-mechanical management of LED lamps is very important and design of all other parts must be optimized for reliability. In this design process thermal and thermo-mechanical issues play a key role.

Heat dissipation and LED temperature were not a problem when low power LEDs were used. However, in today's high power LED applications thermal management issues must be taken into account [27] to not only ensure light maintenance and quality of LED lamps, but also their life time and reliability. Lamp materials and electronics can age at high operational temperature affecting light output [28]. In today's high-power LED applications, these aspects must be taken into account when predicting light quality, life time and whole system reliability. In such applications, the substrate on which LED devices are soldered (LED board) can become critical [2].

The most critical parts of a LED lamp design from the reliability point of view are LED package and LED board [25] [29] [30]. A LED board usually contains several packaged LED dies (6-12). In a LED package a semiconductor die is usually soldered on ceramics and connected by wire or flip-chip bonding. The LED package is then soldered on the LED board.

The most important objective in LED thermal management is to limit the temperature of LED dies and thermal stresses in solder connections, as these parts are the most critical ones for the useful lifetime of the LED lamp [31] [32] [33] [34]. Contrary to the conventional incandescent lighting, LED lamps in general do not fail catastrophically but, as light output is a function of temperature and time, the light output decreases to an unacceptable level in time. ASSIST (Alliance for Solid-State Illumination System) defines life time as the time on which light output has degraded to 70% of the initial output [13].

2.3.1 Retrofit lamp design requirements and components

Most important SSL retrofit lamp requirement is lamp shape (a lot of customers want a "traditional" light bulb shape to replace old incandescent light bulbs). But not only shape is important. Light colours, distributed light angle, dimming possibilities are other very important aspect that must be taken into account.

Figure 2.4 shows a cross-section of retrofit shape SSL lamp with most important parts. Core of the lamp is LED board that include six high powers LED ceramic packages that are soldered on FR4 PCB board. The LED package contains one thermal and two electrical copper pads. Each LED package cover small silicon lens that widening light beam angle. High power LEDs are typically based on GaN solid state semiconductors that emit light in a narrow blue range of the visible spectrum. Blue light has to be converted into white or yellow-white light, comparable to the spectrum of incandescent light bulbs. In this case a remote polycarbonate spherical

conversion dome is used. The dome is mounted on the top of LED board. Another purpose of remote dome is wide angle light distribution. SSL lamp contains also an electronic driver board, which is composed of AC-DC power suppliers, DC-DC converter and current driver controller. The driver maintains the electrical, dimming and optical properties of LEDs [5].

LED board is mounted on top of an alumna thermal cone that dissipates a heat from LEDs and driver (that is embedded in a potting material) to a thermal conductive polymer housing (heat sink). Standard E27 cap is used for lamp mounting. White polyimide reflective cover is attached to thermal cone that reflect the light. A driver support mechanically mounts the driver and thermal interface layer (deposited between LED board and aluminium alloy thermal cone) improve thermal dissipation.

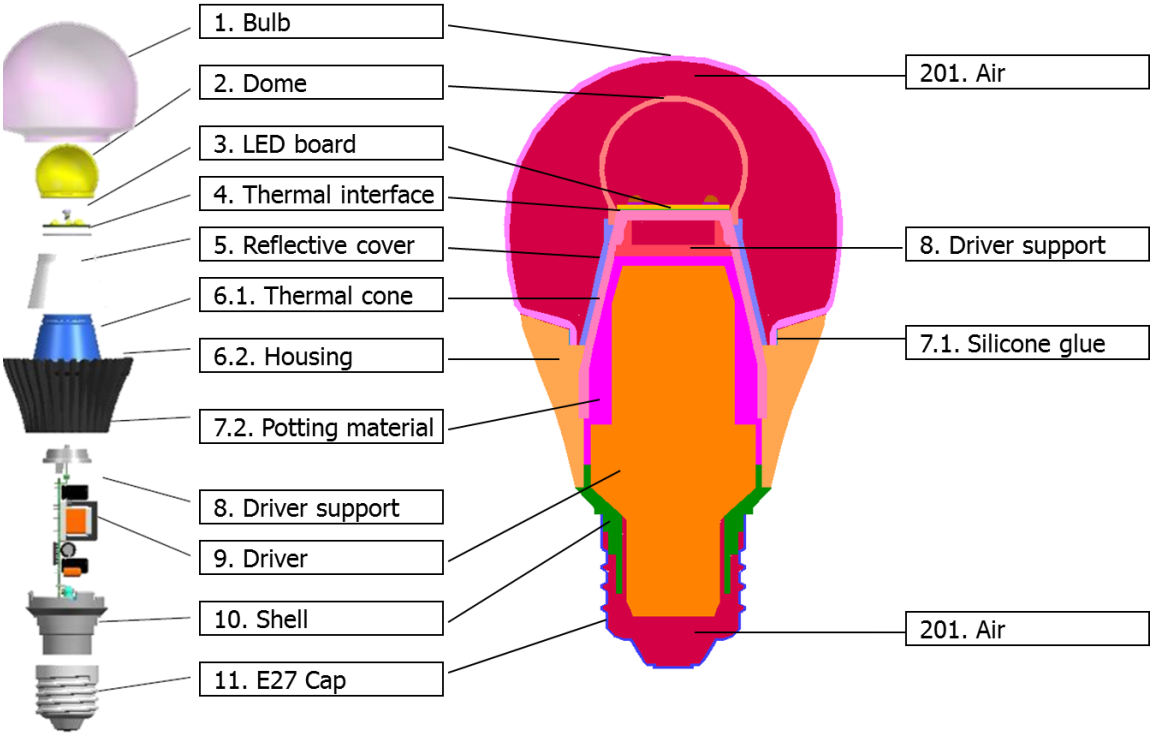


Figure 2.4: Master LED Glow 8 W lamp parts [5]

2.3.2 Methodology for light output improvement

This section proposes a design flow for development of LED lamp models and characterization and validation of the models. The result is calibrated thermal model that can be used for further design and new LED lamp parts development.

LED lamp models development steps

- *Preliminary selection of (existing) LED lamp components, identifying of thermal properties, thermal management possibilities and defining of available packaging materials.*
- *Stepwise modelling of simplified LED lamp concept, incorporating more components until the LED lamp is modelled completely.*
- *Performing simulation on detailed sub-models and thermal boundary conditions transfer from complete model simulated in previous activity. Materials and components data are*

used in to simulate the performance of the conceptual designs; special attention is given to materials interfaces.

- *Variation of heat management in simulations, within the constraints of the simplified model. Parameter study of thermal material properties is carried on to investigate influence of material thermal conductivity to each LED lamp component.*
- *Modification of material properties and simulation software, depending on the results validation from LED lamp models characterization and validation.*
- *Identification of thermal resistances of critical LED lamp components.*
- *Calculation of thermal distribution for new 806 lumen lamp.*
- *Development of the new LED lamp design methodology for 806 lumen lamp.*

LED lamp models characterization and validation steps

- *Physical material properties characterization required for the simulations.*
- *Development of a method for LED board material thermal conductivity measuring; method suited for development purposes as well.*
- *Thermal characterization of the LED lamp.*
- *Software Validation, comparison of measured and simulated results. Identifying of sources of difference.*

The above proposed steps are developed for new 806 lumen lamp, but can be successfully transferred to any other SSL lamp.

2.3.3 Thermal simulation and validation of reference 8W master LED glow

Main purpose of this work has been to get closer to understand thermal phenomena in SLL retrofit LED lamp. For an evaluation Philips 8W master LED glow has been chosen[8]. Thermal management is of critical importance for performance, reliability and life expectancy of a SSL LED lamp. Heat generation and flow inside a lamp will cause a thermo-mechanical loading of the components initiating material and performance degradation and earlier failures. Therefore the multi-target simulation models (such as thermal, thermo-mechanical, reliability and optics) have been integrated to conduct multi-physics simulation of reference master LED glow to provide integrated inputs for new design. Simulations are carried out with ANSYS and CoventorWare software tools to compere not the same simulation methods. The integrated simulation results have been validated experimentally using an existing 8W SSL lamp. Designed simulation models result in new applicable design approach for new 12 W retrofit SSL lamps.

Materials properties (especially thermal conductivity) parametric study has been performed to determine problematical parts that transfer heat from power LEDs to ambient. Solutions for future 12 W retrofit SSL lamp design are proposed. Modelling of SSL lamp has brought more understanding in the design of new lamp shape with new materials. Moreover, explanation of thermal effects inside of SSL lamp can predict light quality, life time and reliability.

[8] The work was done in frame of CSSL project that should develop new 12 W SSL lamp based on Philips 8W master LED glow

2.3.3.1 Thermal model of 8W master glow LED lamp

The conception and design of the geometric model is very significant phase in 3D FEM simulation. The realistic geometry of existing SSL lamp is naturally complex and is composed by many parts and materials. A complete three-dimensional model of retrofit 8W LED Lamp was designed taking into account all essential details (Figure 2.5). The model characterizes a retrofit LED lamp including six blue power LEDs mounted on PCB board. LED GaN wafer is flip-chipped on ceramic package that includes one thermal and two electrical copper pads. Each LEDs chip is covered by a small silicon lens widening a light beam angle (Figure 2.6) [2].

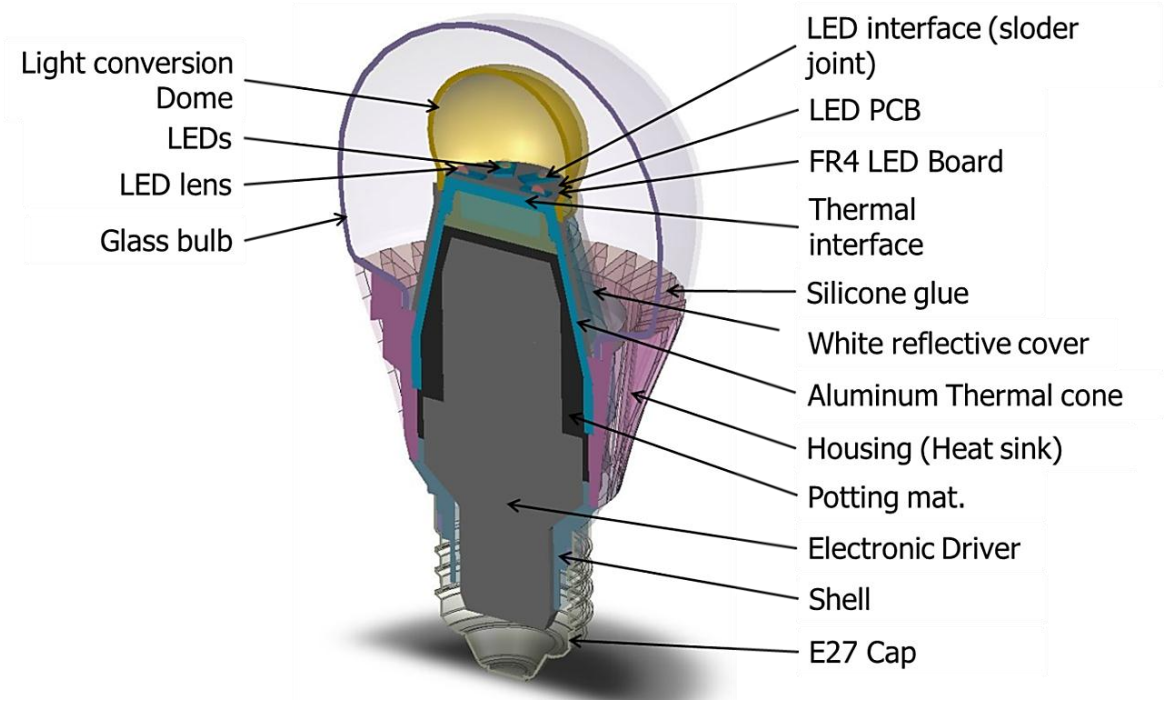


Figure 2.5: SSL Lamp 3-D model includes sixteen different compact parts. Air inside light bulb and inside light conversion dome was included to the model [2]

An essential phase of three-dimensional finite element simulation is definition of the mesh type and mesh generation since it has great impact to the accuracy of the final results. The SSL lamp FEM model mesh has been generated properly detailed to get an acceptable accuracy. Because of the non-orthogonal parts in the model, tetrahedrons elements are used to (which merge and extrude all layers) create a continuous mesh. To keep number of nodes as small as possible, the element distribution is adapted to the shape of the bodies; it means that the number of elements is only increased to capture small features in the model where high heat flus is expected. By this technique we are able to keep computing time at reasonable level. The designed models contain approximately 490,000 nodes depending on the model version [2].

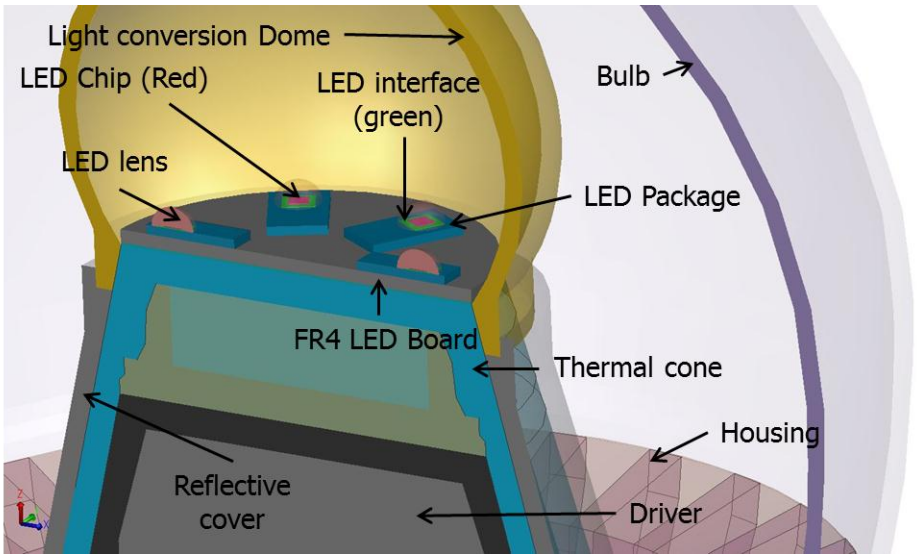


Figure 2.6: Detailed view on LED board placed on aluminium alloy thermal cone. The board includes six LED with Al2O3 package and LED chip [2]

2.3.3.2 Material properties database

One of the most important inputs in FEM modelling that mostly affect validity of simulation results is not only precision of 3D model and its mesh, but also the accuracy of the material properties data. In the SSL lamp simulation model (Figure 2.5) twelve different materials are used. Thermal and mechanical coefficients for each of these materials were collected from different sources [35] [36] [37] [38] [39] [40] [41]. The most problematic issue is identifying component material type properly. For example, some material properties of SSL lamp components are not defined consistently in different sources that refer to not the same values. To resolve this difficulty, the average value of the given material quantities has been used. Another problem arises when some components are simplified as in case of electronic driver. The driver is composed from PCB board and many electronic components. Detail model will be very complex. In current model the driver was simplified to one component where thermal material properties have been estimated[9].

The thermal and mechanical material properties used for the modelling of the LED lamp are summarized in Table 2-4.

[9] This simplification was considered only for the first thermal evaluation. More complex model has been designed for the driver in further simulations

Table 2-4: SSL Lamp thermal and mechanical material properties used for LED lamp simulation [5]

Material	Thermal parameters		Mechanical parameters			References
	Thermal Conductivity λ [W/mK]	Specific heat Cp [J/kgK]	Thermal expansion α [e-6/K]	Young's modulus E [GPa]	Poisson ratio ν [-]	
GaN	130	490	5.6	200	0.4	[25] [37]
Aluminium alloy	100	880	23.4	70	0.3	[42]
Copper	400	385	17.0	110	0.4	[42]
Brass Ni	122	380	20.0	100	0.3	[38] [40]
Glass	1.10	840	8.0	70	0.3	[38] [42]
Polycarbon	0.20	2000	50.0	5	0.3	[36] [39] [38]
Silicone	0.22	1460	220.0	1	0.5	[36] [35] [38]
Silicone filler	2.00	1460	220.0	1	0.5	[41]
PBT	0.27	1700	25.0	9	0.3	[38] [40]
Polyamide6	4.0	1130	40.0	15	0.40	[38] [40]
FR4	4.0	1085	23.4	70	0.3	[42]
LED board	40	1085	23.4	70	0.3	Estimated

2.3.3.3 Thermal modelling

To obtain and compare steady state and dynamic thermal distribution of LED lamp ANSYS, ANSYS-CFX and CoventorWare finite element simulation tools have been used. The steady-state heat conduction equation shown below is solved to obtain temperature distribution for specified thermal boundary conditions, including natural convection and radiation. The Fourier equation for temperature distribution can be written as follows [43]:

$$div(\lambda gradT) = \rho c \frac{\partial T}{\partial t} - p, \tag{2.1}$$

where λ [W m^{-1} K^{-1}] is coefficient of thermal conductivity, ρ mass [kg m^{-3}], c [J kg^{-1} K^{-1}] thermal capacity and p specific heat [W m^{-3}]. Coefficient of thermal conductivity is not constant in wide temperature range. The value of heat flux can be expressed as:

$$q = -\lambda \cdot gradT \quad [\text{W.m}^{-2}], \tag{2.2}$$

If the solid body is heated up by constant power generation and cooled down constantly by surrounding environment then the temperature distribution will reach steady state. For Cartesian coordinate the temperature distribution can be obtained by solving following equation [44]:

$$\nabla^2 T(r,t) + \frac{Q(r,t)}{\lambda} = \frac{1}{\alpha}\frac{\partial T(r,t)}{\partial t} \tag{2.3}$$

Convection

Ambient of SSL lamps is air that can move freely around LED lamp surface and also in the lamp bulb. Natural convection plays dominant role in cooling and heat sink design. It depends on specific dimensions and shapes of the device.

The density of heat flux under the convection is given [44]:

$$q = \alpha \cdot \Delta t = \alpha\left(t_{st} - t_t\right) \quad [\mathrm{W.m^{-2}}], \tag{2.4}$$

where α [W.m^{-2}.s^{-1}] is heat transfer coefficient given by criteria equation (see below), t_{st} is wall temperature of solid body, t_t is gas or liquid surrounding temperature and A contact area.

Criteria equation can be found in literature in following form for instance [44]:

$$Nu = f(Re, Gr, Pr, ...), \quad \text{where} \tag{2.5}$$

$$Nu = \frac{\alpha L}{\lambda_{tek}}, \qquad \mathrm{Re} = \frac{c \cdot L}{\nu},$$

$$\mathrm{Pr} = \frac{\nu}{a} = \frac{\eta \cdot c_p}{\lambda}, \qquad Gr = \gamma \cdot \Delta t \cdot \frac{gL^3}{\nu^2},$$

$$Pe = \frac{c \cdot L}{a} = \mathrm{Re} \cdot \mathrm{Pr}$$

Criteria equation for natural convection can be expressed in the form [44]:

$$Nu = C \cdot (Gr.\mathrm{Pr})^n, \tag{2.6}$$

C and n constants depends on the value of the product Gr.Pr according Table 2-5:

Table 2-5: value of C and n depends on Gr.Pr [45]

Gr.Pr	C	n
$< 1.10^{-3}$	0.45	0.03
$1.10^{-3} \cong 5.10^{2}$	1.18	0.125
$5.10^{2} \cong 2.10^{7}$	0.54	0.25
$2.10^{7} \cong 1.10^{13}$	0.195	0.333

Radiation

Radiation can have significant effect for the devices working close and above 400 K. Some parts of LED lamp are heated up to 380 K. Therefore for such devices the verification of radiation effect should be proved.

Heat loses caused by radiation is given by Stefan-Boltzmann emissive low:

$$P_{Rad} = \varepsilon_{1,2}.C_0.A\sigma T^4 \tag{2.7}$$

where

$$\varepsilon_{1,2} = \frac{1}{\frac{1}{\varepsilon_1} + \frac{1}{\varepsilon_2} - 1} \tag{2.8}$$

ε is emissivity of gray body, A is the body surface and σ is Stefan-Boltzmann constant.

Boundary conditions

The thermal boundary conditions must be specified with care because these conditions can have an excessive influence to calculated results correctness. The essential boundary conditions for SSL lamp modelling are: heat generation caused by Joule heating in all electrical parts (LED chip, driver), heat generation produced by light loses in light conversion dome and in light bulb; heat convection on the outside parts; and radiation. Radiation effect is determined for all model faces that are in contact with the air, it means not only for all external surfaces, but also for LED lamp faces inside the glass bulb and the dome [2].

Heat generation in SSL lamp take place in LED driver 1.2 W (measured value[10]), in six LEDs 4 W (calculated from datasheet) and in polycarbonate light conversion dome 1.5 W (evaluated by optical measurement[11]).

Thermal analysis is performed with ANSYS and CoventorWare to calculate the spatial temperature distribution and steady state heat flux.

In the CoventorWare and ANSYS analysis thermal convection coefficient (5 W/m^2K) was prescribed for all outer parts of SSL lamp that are in interaction with the air. This value can be set for cases, where air velocity is small (under 0.05 m/s) [25]. Radiation affect to ambient (temperature of 22°C) was also taken into account for all inner and outer parts of the lamp which are exposed to the air. It is very important to define emissivity coefficients for all materials of used lamp components. The emissivity coefficients have been evaluated by measurement (Chapter 2.3.3.4).

In the ANSYS-CFX thermal simulation natural air convection is calculated allowing for convective flow. So the simulation was performed taking into account the air flow inside bulb and dome and also around the lamp.

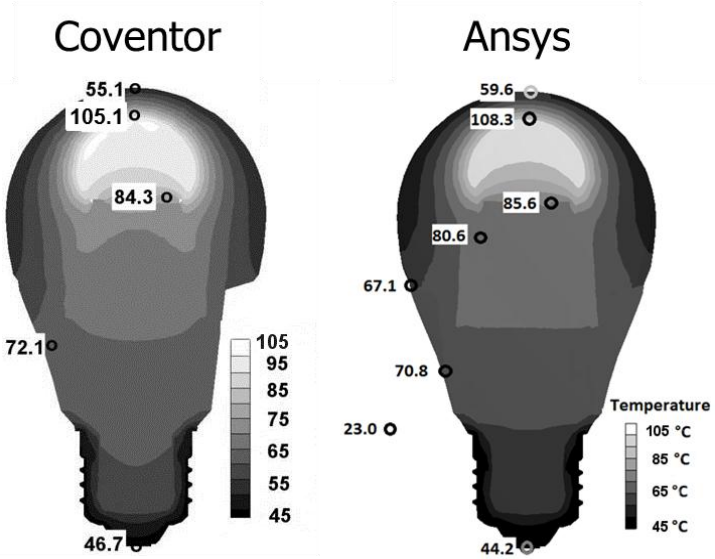


Figure 2.7: Computed steady state thermal analysis temperature distribution. Comparison between Coventor and ASYS simulation tool is shown [2]

[10] Measured by CNM Barcelona. The value has been determined by measuring of input and output power measurement.
[11] Measured by CEA Grenoble.

In Figure 2.7 the temperature distribution results calculated in Coventor and ANSYS are compared. In this analysis natural air convection is not taken into account. Temperatures at defined locations (bulb, dome, LED, thermal cone and housing) were sampled. The LED temperature is defined as the maximum temperature that occurs in the GaN LED die. The model is not complete to be able to calculate the LED junction temperature, but is adequate to calculate a LED GaN die temperature[12]. The calculated LED die temperature is 84.3°C for Coventor simulation and 85.6°C for the ANSYS simulation which shows good agreement. Figure 2.7c shows calculated temperature distribution for ANSYS-CFX thermal simulation with natural air convection.

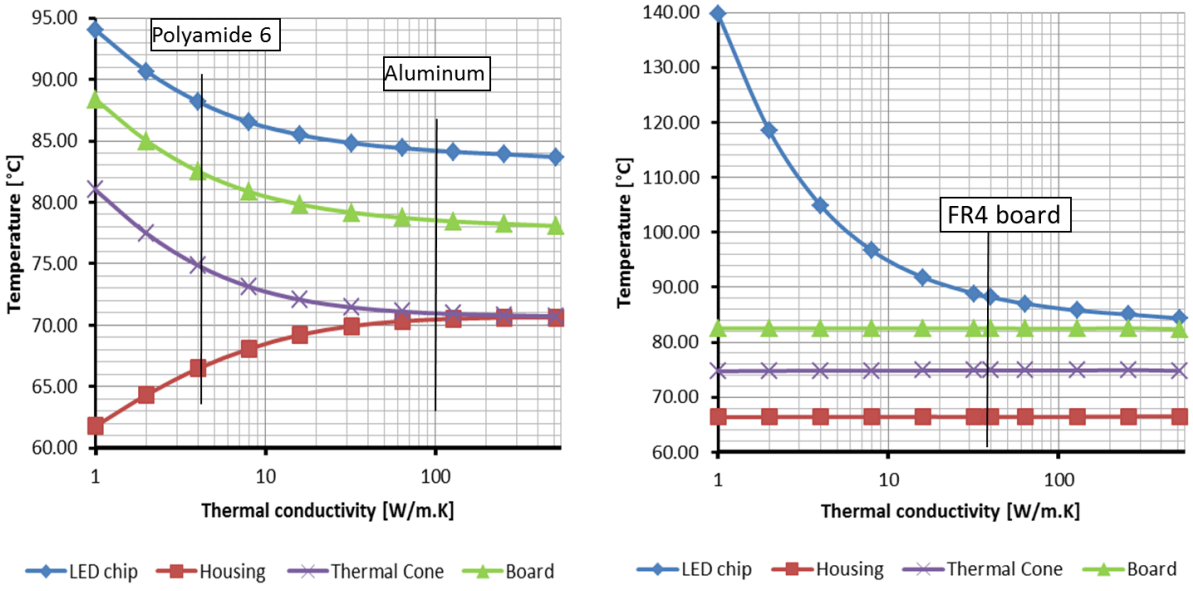


Figure 2.8: Thermal conductivity parametric study that was swept in range 1 – 500 W/mK. a) Housing (heat sink) temperature difference for Polyamide 6 (used in measured LED lamp) and Aluminium; b) LED board where value for current FR4 board is marked [46].

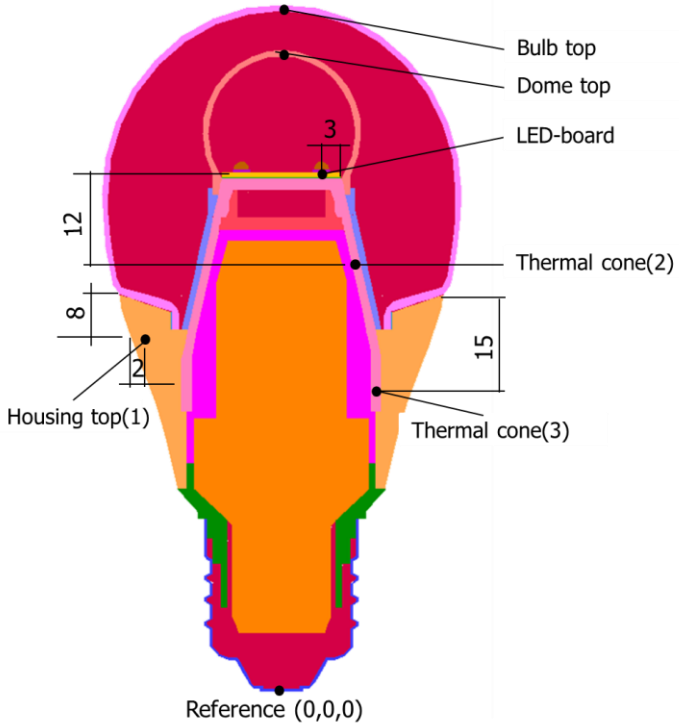
For the reason that reliability and life time of LED chip typically depends on working temperature [30], alternative materials replacement has been proposed to improve heat conduction to ambient. To predict an influence of material thermal conductivity, material parametric analyses was carried out to explore future thermal management improvements with respect to new materials. The influence of thermal conductivity of the housing (heat sink) is depicted in Figure 2.8a. Here LED chip temperature is calculated. It can be seen that if aluminium is used for housing (heat sink) instead of polyamide 6, the LED chip temperature drops about 6°C. The LED die temperature can be also decreased by optimizing of heat sink shape and number of fins[13]. Figure 2.8b shows the influence of thermal conductivity of the LED board that is another critical part from thermal management point of view [46]. The value of current FR4 board is 40 W/m.K. LED board thermal resistance could be improved using leadframe of IMS technology.

[12] More accurate calculation has been done with detailed LED board model where all details of given parts are taken into account
[13] Analysis of number and thickness of heat sink fins has been made by TNO (Nederland) in frame of CSSL project

2.3.3.4 Thermal validation and measurement

The objective was to obtain reliable and accurate temperature values at different points of the reference SSL lamp, by means of IR (infra-red) thermography and direct temperature measurements. Direct temperature measurements were done by thermocouples, in defined monitor points inside the lamp (Figure 2.9). This work has provided a full thermal characterization methodology for new lamp designs. Further objectives of these measurements and simulations are addressed to:

- *Provide data for determining of the thermal input parameters of several SSL lamp components to improve the thermal simulation results.*
- *Study the thermal phenomena of the lamp under working conditions (e.g., internal heat sources and boundary conditions dependence) for further development of new SSL lamp.*



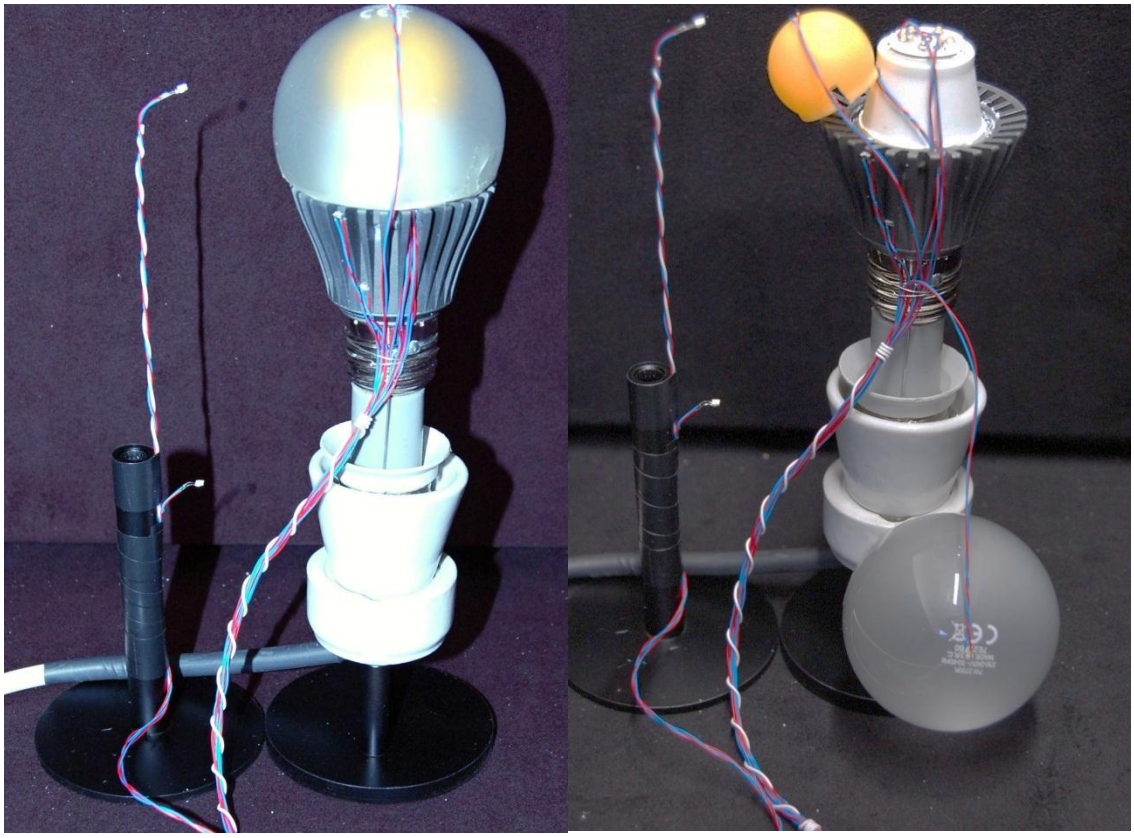
Coordinates to be used in simulation model

	X [mm]	Y [mm]	Z [mm]
Bulb top	0.0	0.0	108.0
T_junction	-3.5	6.1	82.7
LED Board	0.0	8.0	82.0
Thermal cone(1)	-3.5	6.1	81.8
Thermal cone(2)	-6.5	11.2	65.0
Thermal cone(3)	-7.9	13.6	47.5
Housing top(1)	-10.0	20.0	54.8
Housing top(2)	-9.1	17.1	54.8
Shell	-6.5	11.3	29.1
Ambient	0.0	52.0	92.0

Figure 2.9: Measuring points locations [2]

For validation of the thermal modelling a laboratory measurement test set-up methodology was prepared. The SSL lamp is placed in reflection-less thermal chamber (Figure 2.10a). The thermal measurement was performed in a room with air temperature control (23°C)[14]. Thermal measurement was carried out by two independent methods. In the first method the temperature is measured as a function of time at several SSL lamp monitor points inside and outside of the lamp using SMD PT 1000 micro-scale temperature sensors (Figure 2.10b). Temperature sensors are placed on the LED board, thermal cone, heat sink, top of the Dome and top of the lamp. The ambient air temperature in the temperature chamber was measured [2].

[14] The methodology also allows different ambient temperature measurement.



a) b)

Figure 2.10: Measurement setup in reflection-less thermal chamber. a) Assembled SSL lamp. Wires leads to temperature sensors placed inside and outside of the lamp. Temperature sensors measuring ambient temperature are also clearly seen - b) Dismounted SSL lamp [2]

Figure 2.11 shows the results of the direct temperature transient measurement with temperature sensors. A steep temperature growth is observed at the beginning of the test. Within 2 hours the temperature reaches a steady-state condition. In Figure 2.11 the results of the steady-state ANSYS simulation (previous chapter) are presented and marked by symbols at time 6200 s where temperature transient has already reached steady state [2].

The temperatures calculated by ANSYS and Coventor undervalue slightly the measured temperatures of LED board (85.6 °C ANSYS simulation, 88.9 °C measurement). The underestimation might be due to the use of estimated heat generation input and a too high emissivity coefficient. The biggest temperature difference (8.1 °C) between simulation and experiment is detected for the dome temperature (108.3 °C ANSYS simulation, 100.2 °C measurement). The higher calculated dome temperature might be caused by not modelling the air flow inside a dome and inside the bulb, which could in reality cool down the surface of the dome. In additional measurements radial temperature dependence was found in the LED board with the lowest temperature in the middle of the board.

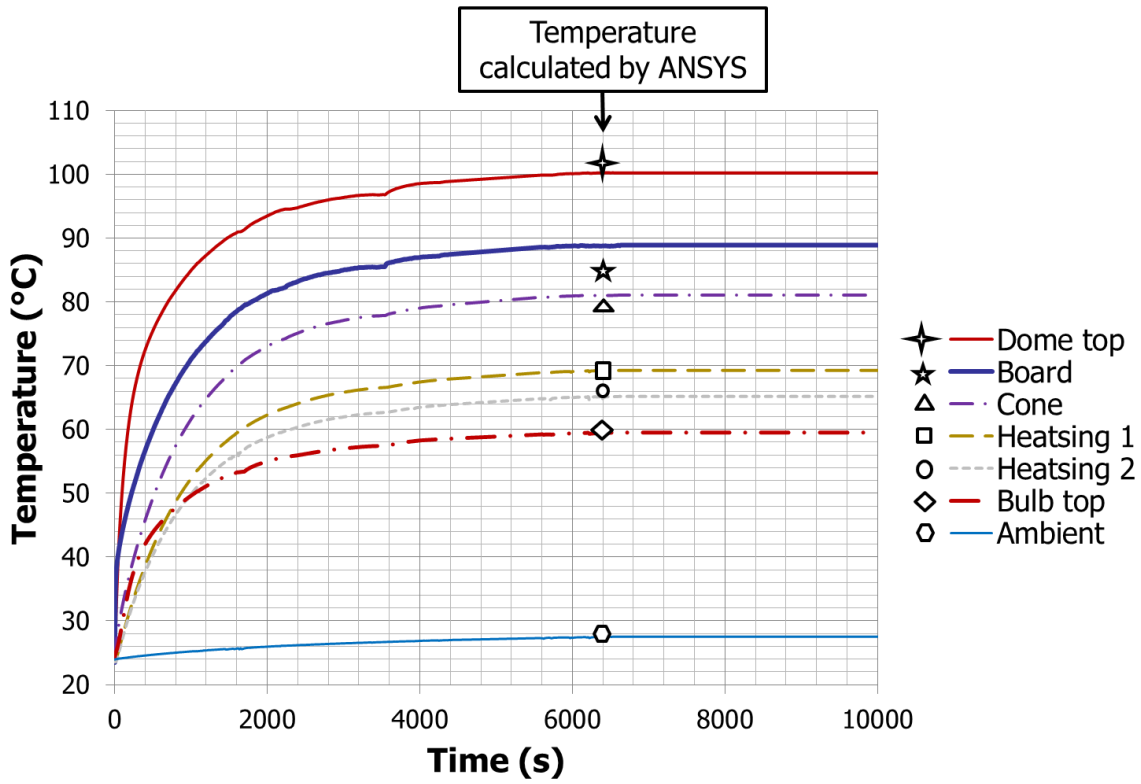


Figure 2.11: Measured (line) and calculated (symbol) temperatures of the SSL lamp [2]

The second measurement method uses an IR (infra-red) camera imaging to obtain temperature distribution of the SSL lamp. In this measurement method, the emissivity coefficients must be known for all materials. The emissivity of all SSL components have been determined by simple methodology where reference object with known emissivity (electrical tape with known high emissivity – 0.95) is heated up to defined temperature together with measured component. The emissivity on IR camera is set to that of the tape (0.95). After heating up to given temperature IR image is taken. Then emissivity can be calculated from Stefan-Boltzmann Law [2].

To overcome a problem with different emissivity of diverse materials, a black strip was made on each part of measured SSL lamp (Figure 2.12). The temperature is at that point sampled on the black strip, which has the same emissivity for all materials. Figure 2.13c shows the temperature distribution sampled by IR camera with marked sampling points. The temperature distribution inside the SSL lamp was obtained when the glass bulb was dismounted Figure 2.13b. The measurement was executed instantly after glass bulb dismounting to keep the temperature that is not affected by air cooling. Compatibly, the light conversion dome was dismounted for LED board temperature distribution measurement Figure 2.13d [2].

Figure 2.12: SSL lamp components with black strip used for IR measurement [2]

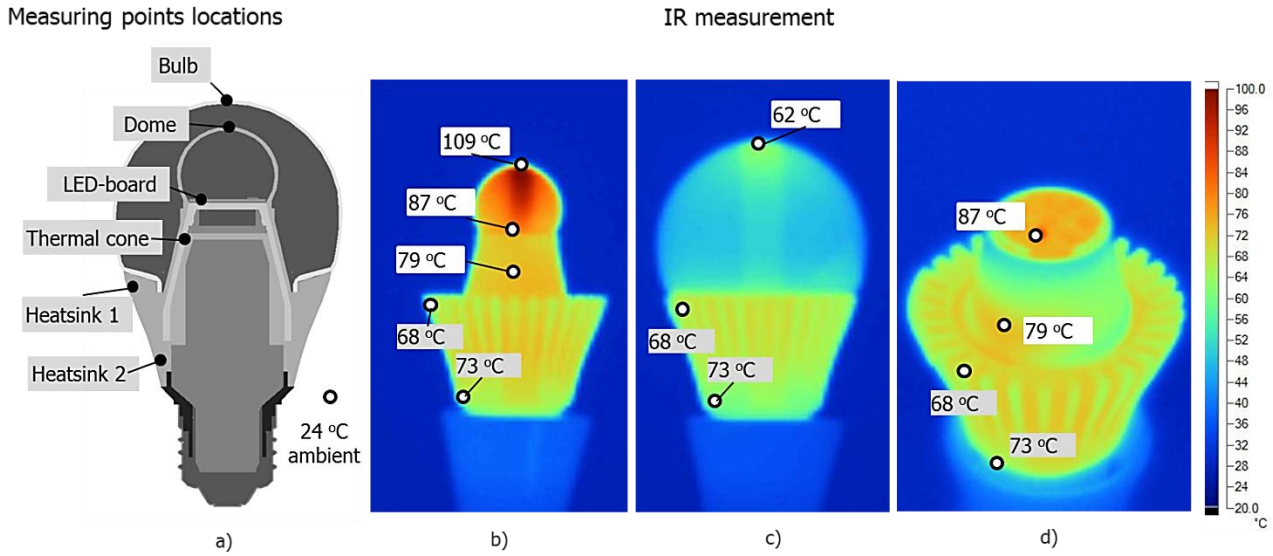


Figure 2.13: Temperature distribution sampled by IR camera. a) Thermal sensors location used for temperature measurement and comparative temperature samples from simulations. b) thermal distribution under glass bulb c) thermal distribution of the SSL lamp surface, d) thermal distribution of the LED board

Table 2-6 shows comparison of calculated and measured temperatures in defined location points (bulb, dome, LED, thermal cone, housing and shell).

Table 2-6: Comparison of measured and calculated temperatures using different methods [2]

	Temperature (°C)						
	Bulb top	Dome top	Board	Cone	Heatsink 1	Heatsink 2	Ambient
Simulation ANSYS	59.6	108.3	85.6	80.6	67.1	70.8	23.0
Simulation COVENTOR	55.1	105.1	84.3	79.8	68.8	72.1	23.0
Measurement PT 1000	59.5	103.2	88.9	81.1	65.2	69.3	24.2
IR Measurement	62.0	109.0	87.0	79.0	68.0	73.0	24.0

2.3.4 Thermal design and management of new 806 lumen SSL lamp

Figure 2.14 shows an expected thermal effect on 60 Watt replacement lamp where new heat dissipation conditions have been applied to an existing SSL lamp topology. The heat dissipation values for driver, LED and Dome was estimated by companies providing new solution of these components for new lamp design. As we can see LED chip temperature rises to 141 °C for room temperature (22 °C) and if the ambient rises to 45 °C the LED chip temperature is even 160 °C. The requirement for maximal LED chip temperature is 120 °C[15]. This LED temperature is not allowed. There are two main aspects that have dominant influence on thermal management of the SSL lamp:

- *Thermal conductivity of used materials*
- *Optimization of heat transport from heat dissipation areas (LEDs, Dome, Driver) to ambient*

Most critical parts from thermal management point of view are LED board with thermal cone and housing (heat sink).

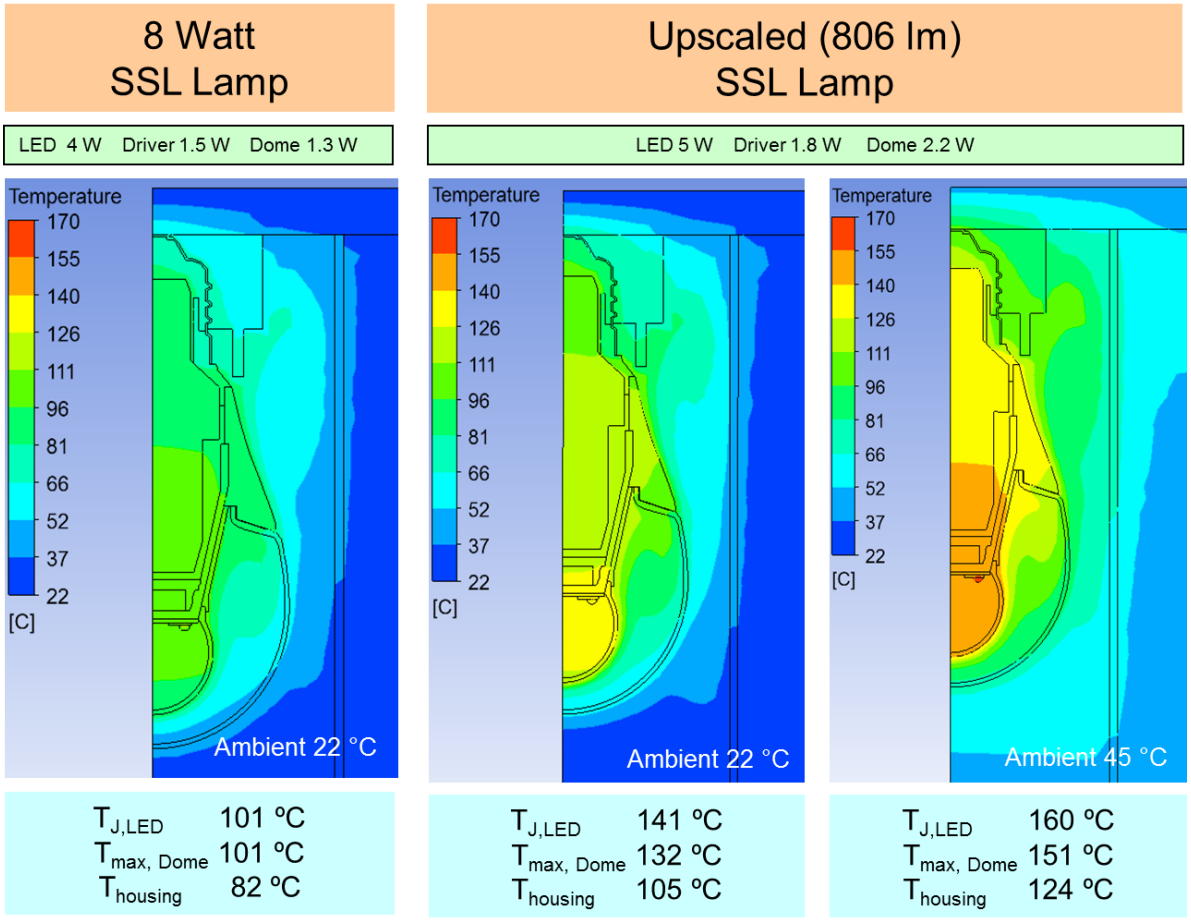


Figure 2.14 - Expected thermal effects on 60 Watt replacement lamp[16]

[15] Luxeon Rebel data sheet
[16] Simulation made by TNO Nederland

An important property of the LEDs board is the heat conductivity (or thermal resistance). Almost all heat generated by the LEDs has to be transported through the substrate conductively. The thermal conductivity of LED board should be as high as possible. The FR4 printed circuit board [PCB] is presently used in SSL lamp (Figure 2.15 [47]). The thermal resistance depends on the thickness of the copper layer and epoxy layer. Changing of the copper layer and of the epoxy layer thickness can change the thermal conductivity dramatically. Another method how to decrease thermal conductivity of the LED board is to use so-called insulated metal sheet [IMS]. Depending on the type of filler used in the dielectric layer, values of the thermal resistance ranges from 2.5 to 5.5 K/W.

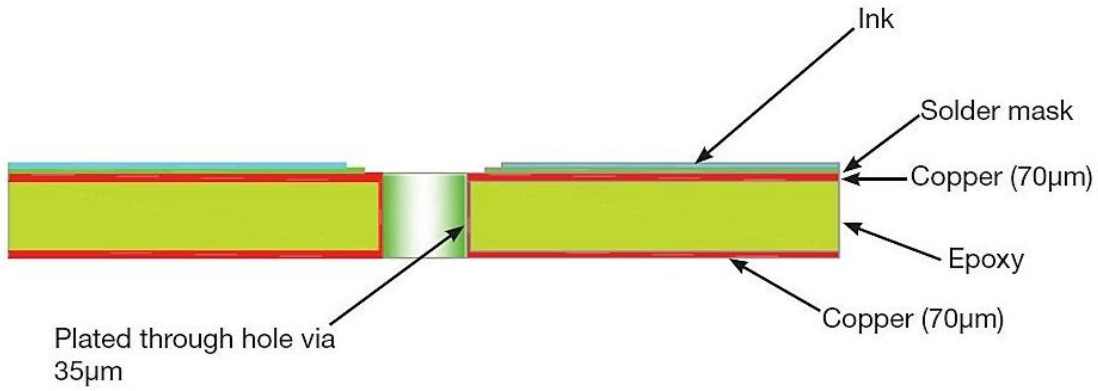


Figure 2.15: Cross section of FR4-based PCB with thermal vias to decrease thermal resistance [47]

The heat sink in reference 8W SSL lamp comprises two components, an internal aluminium cone (thermal conductivity depending on the alloy ranges between 160 – 240 W/mK) that is connected to the LEDs board, and thermoplastic housing that is mechanically connected to thermal cone. To increase an ambient air natural heat convection the housing has a finned surface. The thermal resistance of both components limit heat conduction from cylinder to housing and ambient. Thermal conductivity of thermoplastics is about 0.2 W/mK, The conductivity can be increased to about 1 – 10 W/mK by adding conductive fillers. Thermally conductive compounds of polymers, such as PP, PA46, PBT, PPS and LCP, are available on the market [48] [49]. There exist also PPS and LCP compounds with high thermal conductivity of 20 W/mK [50]. The main backdrop of these materials is the cost-effectiveness.

2.4 Thermal evaluation and characterization of SSL lamp LED board

The objective of this action was design of accurate LED board thermal model and evaluation of the thermal behaviour of reference LED board that proves the thermal simulation results. Thermal performance of LED boards and LED packages can be compared by expressing of the absolute thermal resistance (R_{th} in K/W) which measures the temperature difference across a component when a unit of heat energy flows through the component in unit time. Luxeon Rebel LEDs and the Master LED board structure have been analysed to understand their relationship with the heat conduction phenomena. This allows an accurate thermal modelling and understanding of the experimental data. Calibrated model will be used for new LED board designs.

2.4.1 LED board model

LED board of the master model is composed of 650μm thick FR4 board with 80μm Cu layers implemented on both sides. The top Cu layer makes electrical connection between the LEDs. Thermal vias (500μm in diameter) are placed under and around thermal pad of LED package to increase thermal conductivity of FR4 board. The board includes six Luxeon Rebel LEDs based on ceramic LED package that includes one thermal pad and two electrical copper pads. A LED die is connected by 16 bumps (Flip-chip) on top side of ceramic LED package. Bottom side of LED package is soldered with FR4 top cooper metallization. On each of the LEDs a silicon lens is placed (Figure 2.16). Concerning the thermal management, the heat is dissipated to the PCB via a thermal pad where the die mounted. The PCB used is a via filled FR4 board (Figure 2.16) for improved heat dissipation.

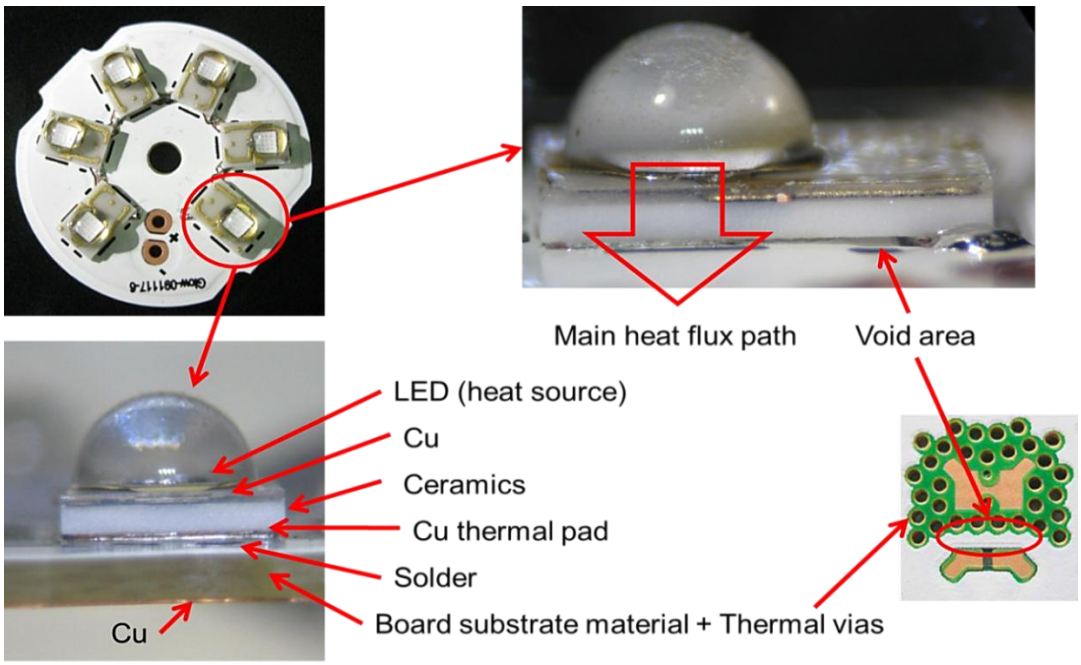


Figure 2.16: Overview of the FR4 board with 6 LEDs and heat conduction mechanism from the LED towards the board and TIM

3-D model of LED board used for thermal modelling is on Figure 2.17. The LED board model is supplemented by a thermal cone that provide the relevant heat flux distribution at bottom side of the LED board as in case of normal operational conditions. This measure is necessary to insure realistic heat distribution at bottom side of the LED board. The heat power dissipation is applied on each LED chip. Additionally, radiation is also taken into account for all surfaces which are supposed to be in contact with air. Material infrared emissivity was determined experimentally (Chapter 2.3.3.4).

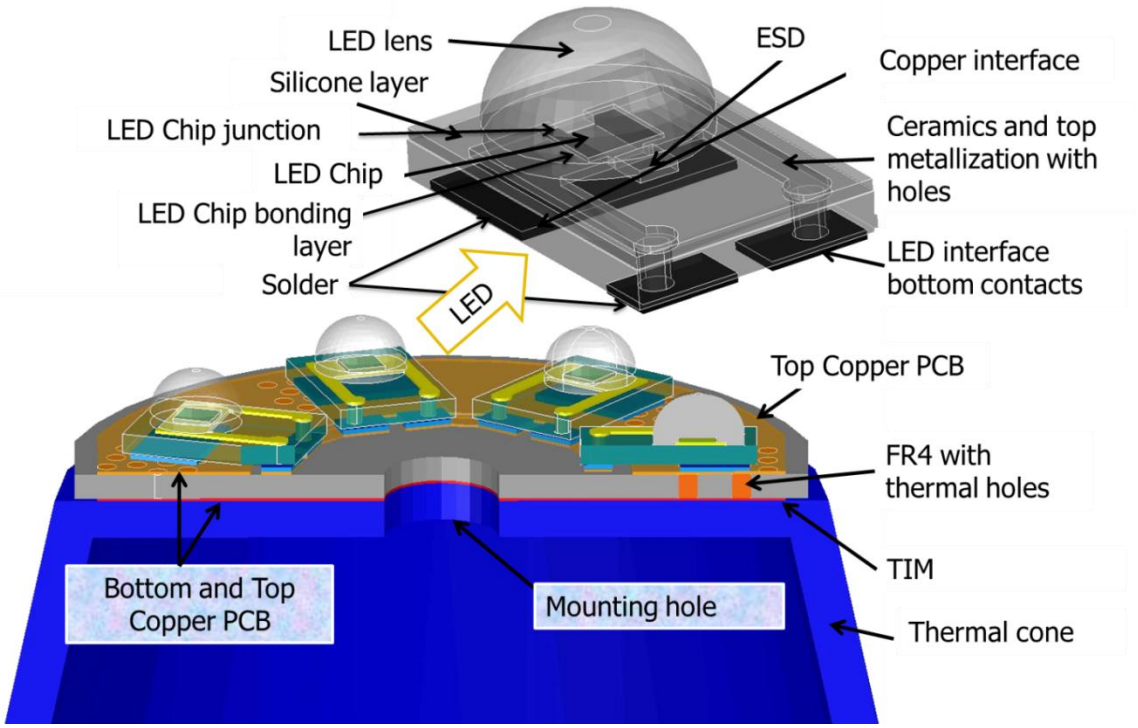


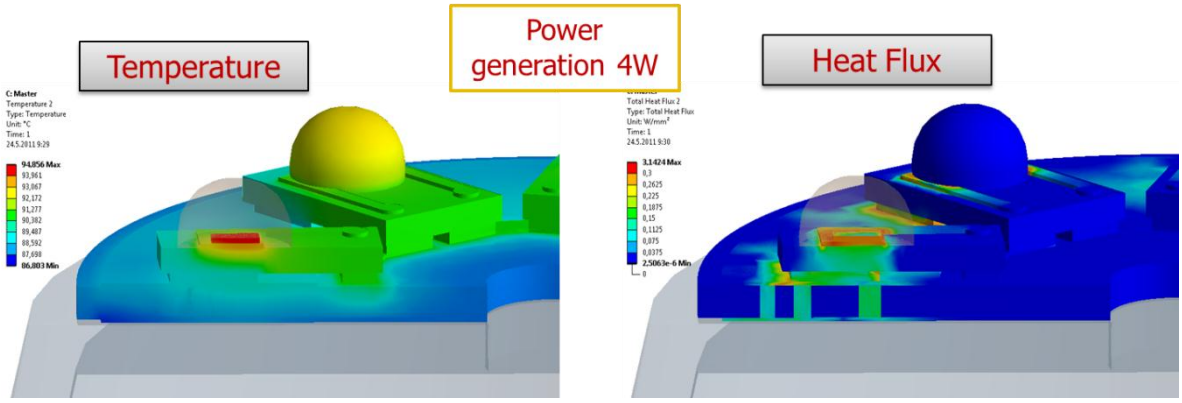
Figure 2.17: 3-D model of LED board used thermal modelling. Board includes six packaged LED packages including LED lens [3]

2.4.2 Thermal simulation and thermal resistance validation

To ensure the same heat flux distribution as in the case of a whole LED lamp, the LED boards are placed on a heat sink that emulates the same heat distribution at the bottom side of the LED board as exists inside the lamp under real working conditions. The total heat power dissipated among the six LED chips of the boards considered in simulations is 4 W. Additionally, radiation is also taken into account for all surfaces which are supposed to be in contact with air. The thermal conductivity and infrared emissivity of all materials involved in this model have been determined experimentally [51]. Thermal performance of LED boards and packages can be compared by expressing of the absolute thermal resistance (R_{th} in K/W) which measures the temperature difference across a component when a unit of heat energy flows through the component in unit time.

Figure 2.18 shows temperature and heat flux distribution of FR4 LED board design. With this simulation result, the thermal resistance has been calculated as the temperature difference between top side of LED die and bottom side of copper thermal pad at the imposed heat

dissipation in the active parts (4W). In the case of the FR4 board, the difference considered was between top and bottom side of copper layers. As a result, 9.44 °K/W and 4.81 °K/W are the thermal resistance values identified for the LED package and FR4 board, respectively. Therefore, the total thermal resistance of FR4 board and LED package is 14.25 °K/W [3]. To validate this result of our model, experimental thermal measurements have been carried out.



a) b)

Figure 2.18: a) temperature and b) heat flux distribution of FR4 LED. Die temperature is 95.2°C [3]

Total thermal resistance of FR4 master LED board was measured[17]. The thermal resistance between LED junction and reference temperature $R_{TH(j-C)}$ defined as:

$$R_{TH(j-C)} = \frac{T_j - T_C}{P_{TH}} \qquad (2.9)$$

The junction temperature T_j is the LED die mean temperature and it is evaluated from the forward voltage drop dependence with temperature at low current ("electrical" T_j determination method). The reference temperature T_C is the backside (or bottom) LED board temperature. Correct $R_{TH(j-C)}$ definition requires T_C measurement in the heat dissipation path. Consequently, this variable has been measured below the LED using a spring loaded K-type thermocouple. P_{TH} is the dissipated thermal power. It is related with the optical power P_{OP} ("radiant flux") and the input electrical power P_{EL}:

$$P_{EL} = P_{TH} + P_{OP} = I_F . V_F \qquad (2.10)$$

where I_F is the LED forward current and V_F the forward voltage drop. The T_j and I_F dependence of P_{OP} are required to determine P_{TH} from P_{EL}. P_{OP} dependence on I_F at 25ºC has been derived from datasheet information. The linear relationship:

$$P_{OP} = 105\text{mW} + 1.1286 \times I_F \qquad (2.11)$$

gives a good approximation in the considered operation range. In order to minimize the experimental errors related with temperature measurements (for both, T_j and T_C), instead of applying directly expression (1.4) for $R_{TH(j-C)}$ determination, we have computed this thermal resistance as the slope of the linear fit between temperature increase ($\Delta T = T_j - T_C$) for different P_{TH}. Figure 2.19 shows experimental results represented in the ΔT vs P_{TH} plane for the reference LED board. 20 points have been measured, showing a significant dispersion. The linear fit (solid line) provides the statistical mean for describing the temperature increase

[17] Measured in Centre Nacional de Microelectrònica, CNM-CSIC, Campus UAB, 08193 Bellaterra, Barcelona, Spain

dependence versus power, with an slope of 12.9 ºC/W and a standard deviation of 1 ºC/W. This value is compared with the mean value of expression (1.4) computed for the 20 experimental points (13.6 ºC/W). We obtain a good agreement between experimental and simulation results (below 5% error). This result validates our simulation approach as well as the thermal conductivity values taken from the literature.

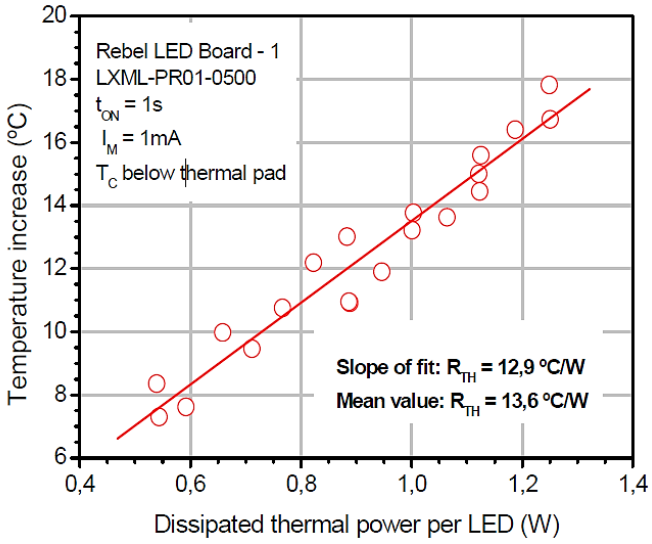


Figure 2.19: Experimental results for the ΔT vs P_{TH} plane[18]

The total thermal resistance obtained by measurement and evaluated by simulation is ~ 14.56 K/W. The experimental results are in good agreement with simulation.

2.4.3 Thermo-mechanical numerical modelling

Calculations of mechanical stresses that are formed by different thermal expansion coefficients of the used materials are very important for the LED board reliability. The most critical parts of an LED lamp design from the thermal path and reliability point of view are LED package, LED board and interconnections.

Thermo-mechanical modelling of LED board has been performed by nonlinear elastic-plastic structural analysis in ANSYS. Material nonlinearities in LED board occur because of the nonlinear relationship between stress and strain. The total strain is defined as summary of three independent strain tensors [43]:

$$\varepsilon = \varepsilon_{el} + \varepsilon_{pl} + \varepsilon_{cr} + \varepsilon_{th} \qquad (2.12)$$

where ε_{el} is elastic strain, ε_{pl} is plastic strain, ε_{cr} is creep strain, ε_{th} is thermal strain.

Elastic strain

Relationship between stress and strain can be expressed by stress-strain curve. The region of the stress-strain curve, where material returns to the undeformed state (when applied forces

[18] Measured by Xavier Perpinya, Centre Nacional de Microelectrònica, CNM-CSIC, Campus UAB, 08193 Bellaterra, Barcelona, Spain

are removed) is called the elastic region. Mechanical stress acting in direction of x-axis depending on the strain can be expressed as:

$$\sigma_x = E\delta_x \tag{2.13}$$

where E is Yang modulus constant, σ_x, is mechanical stress. In linear theory of elasticity, where the dependence between strain and stress tensor is given by generalized Hoock low [52], the deformations are small:

$$\delta_x = \frac{1}{E}\left[\sigma_x - \nu(\sigma_y + \sigma_z)\right] \tag{2.14}$$

$$\delta_y = \frac{1}{E}\left[\sigma_y - \nu(\sigma_z + \sigma_x)\right] \tag{2.15}$$

$$\delta_z = \frac{1}{E}\left[\sigma_z - \nu(\sigma_x + \sigma_y)\right] \tag{2.16}$$

where E is Yang modulus constant, σ_x, σ_y and σ_z are mechanical stresses in the given direction acting perpendicular to wall of the body (Figure 2.20), ν [-] is Poisson coefficient, which indicate the change of the proportions in the directions perpendicular to the vector of acting mechanical stress. Typical values are between 0 and 0.5. τ in Figure 2.20 is shear stress affecting along the plates.

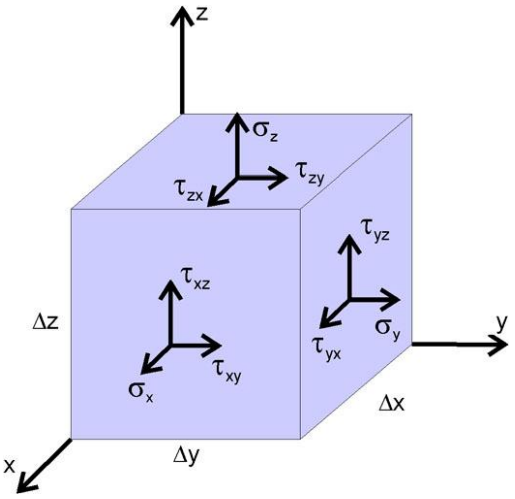


Figure 2.20: Mechanical stresses and shear stresses affecting the solid body [45]

Mechanical structures in the case of linear theory of elasticity have idealized some its physical properties by following assumptions: homogenous body, isotropic, linearly elastic in all points.

By affecting of external forces and no homogenous temperature distribution, the elastic body is deformed and internal forces then arise. In linear elastic continuum appear displacements which are defined by Lamé equation:

$$(\varphi + \psi)grad(div\delta) + \psi\Delta\delta - (3\varphi + 2\psi)\alpha_T gradT + f - 0 \tag{2.17}$$

where $\varphi \geq 0$ and $\psi > 0$ are so called Lamé coefficients, which are given by material properties:

$$\psi = \frac{\nu \cdot E}{(1+\nu)\cdot(1-2\nu)}, \qquad \psi = \frac{E}{2(1+\nu)}, \tag{2.18}$$

where E (r, T) [MPa] is Young modulus, ν (r, T) Poisson coefficient, $\delta(r)$ [m] vector of displacement and f (r, ...) [N m^{-3}] is vector of internal volume forces.

Plastic strain

The region in which the material deforms permanently is called the plastic region. Plastic strain is strain in which the distorted body does not return to its original size and shape after the deforming force has been removed. If the deforming force makes stress that exceeds a critical value, the material will undergo plastic deformation. This critical stress can be tensile or compressive. The value of stress where material becomes plastic is called Yield stress. The yield strength of a material cannot be calculated for any material. It must be arrived experimentally and proved by statistical analysis.

The relation between stresses and induced strains is expressed by constitutive equations or material's Stress-Strain curve that describes the relationship between the stress and strain and is unique for each material. Stress-Strain curve is measured by recording the amount of strain deformation at distinct intervals of tensile or compressive loading (stress).

Creep strain

Some solid material has tendency to slowly move or deform permanently under the influence of mechanical or thermal stresses. This phenomenon is called creep. It occurs as a result of long term exposure to levels of stress that are below the yield strength or ultimate strength of the material. Creep is more severe in materials that are subjected to heat for long periods, and near the melting point

The creep strain can be calculated by implicit constitutive relation [53]:

$$\varepsilon_{cr} = A_1[sinh(\alpha\sigma)]^n exp\left(\frac{-H_1}{kT}\right) \tag{2.19}$$

More information describing creep behaviour can be found in chapter 2.6.

2.4.4 LED board thermo-mechanical simulation

To calculate accurately deflection and stresses of the LED board and its components in the thermo-mechanical analyses, parabolic 10-node elements are used [43]. In this case inner face nodes of the central hole are mechanically fixed (Figure 2.21). This boundary condition reflects on the fact that the LED board is fixed to the thermal cone by a central screw connection. All other nodes can freely move in all directions. Heat generation of 4 W is applied in the LEDs. The heat flux through the bottom face of the LED board has been taken from the thermal analysis of the LED lamp model. Convection (5 W/m^{2}K to air) and radiation (emissivity experimentally measured) has been prescribed on the top surface of board and LEDs. Figure 2.22 shows the calculated residual stress distribution based on a linear elastic approach.

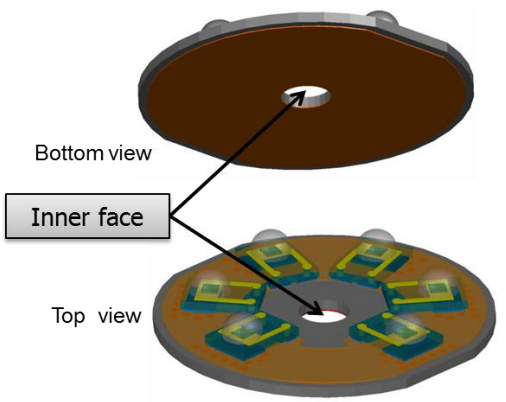


Figure 2.21: Mechanical boundary condition for master LED board. Inner face of the board was mechanically fixed; all other faces was mechanically free

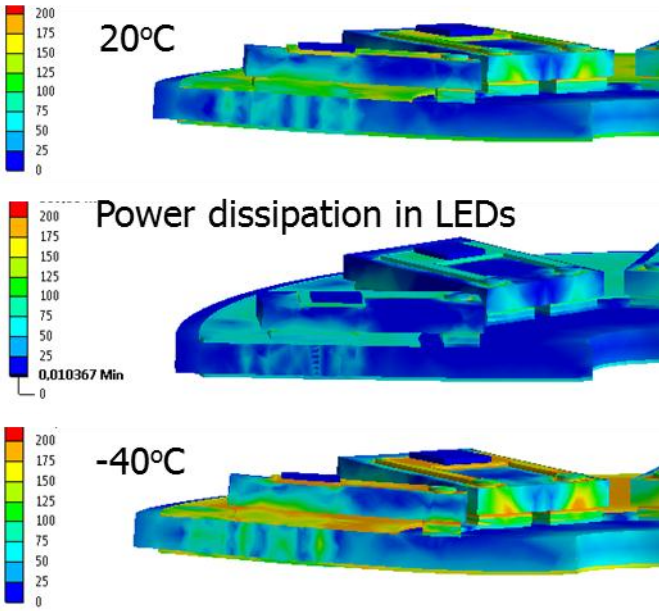


Figure 2.22: Distribution of residual stresses (in MPa) of the LED board for different temperatures

Very high residual stresses can be found for lowest temperature (-40°C). The reason for that is zero stress temperature that has been defined according soldering and moulding fabrication process. Highest thermal stresses are located in LED board and LED package top copper layer. The value reaches up to 190 MPa. In this simulation only linear elastic approach was used which not takes into account material yields stresses and material plastic behaviour. The value of the yield stress for copper is about 70 MPa for example.

To overcome this inaccuracy the simulation has been improved by adding elastic-plastic material properties that are usually defined by stress-strain curves. The temperature dependent stress-strain curves for copper are on Figure 2.23 [54]:

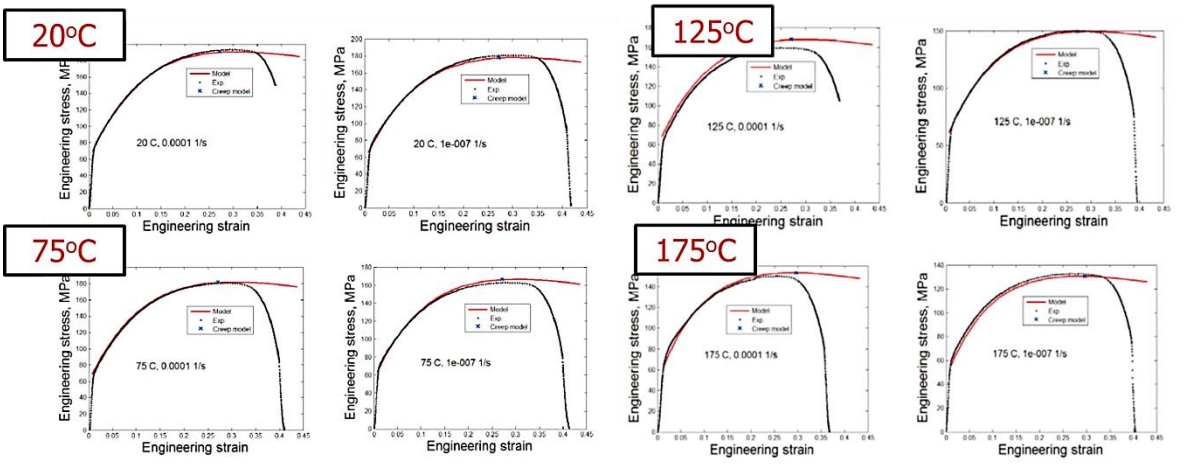


Figure 2.23: The temperature dependent stress-strain curves for copper [54]

Stress-strain curves for other materials as FR4, epoxide via filer, solder material and gold has been also taken into account [55] [37]. Figure 2.24 shows the calculated residual stress distribution based on the elastic-plastic approach. Because of plastic deformation residual stress of the copper layer is dramatically decreased in comparison with linear elastic approach results.

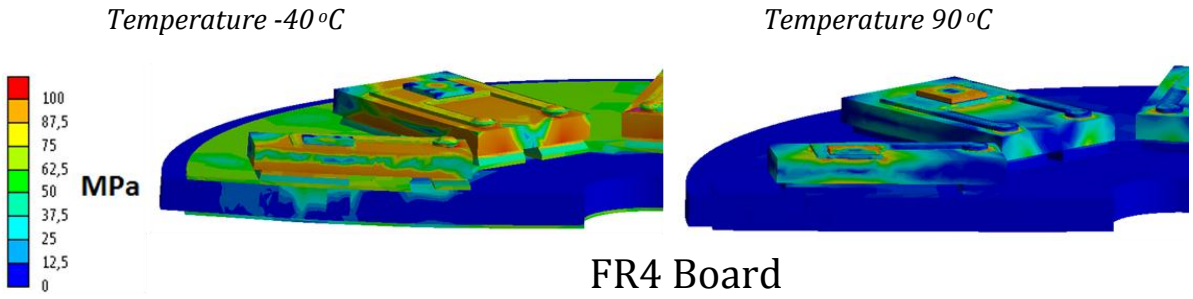


Figure 2.24: Thermal stress distribution master FR4 LED board based on the elastic-plastic approach for minimal storing temperature -40°C and operational temperature 90°C [3].

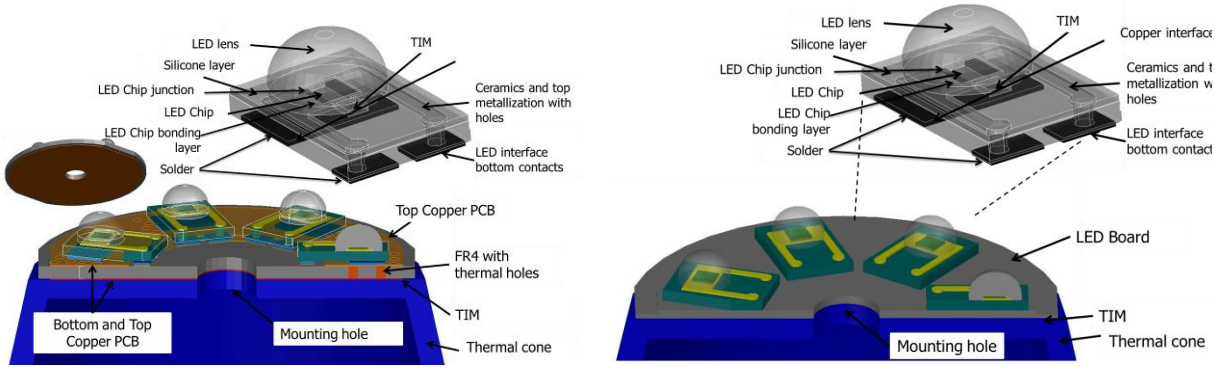
2.5 New LED board designs

The main goal of this work has been to improve thermal management of LED board and evaluate thermal stresses in LED board and LED package to investigate reliability. As has been already shown, one of the main critical parts in SSL lamp thermal management is proper thermal design of the LED board. Main role of each LED board is to transport heat from LED die to heat sink and keep the thermal stresses in all layers as low as possible. The thermal resistance between LED chip and LED board bottom side has to be lowered as much as possible. Very important aspect regarding reliability is keeping thermal stresses and accumulated creep strains in solder joints as low as possible. Thermal stress has been inspected for the widest temperature range that can affect the LED boards (-40 to +125°C given by specification). Simulations have been completed with ANSYS structural analysis where temperature dependent stress-strain material properties have been taken into account. The objective of the analysis is to optimize not only the thermal management by thermal simulation of LED boards, but also to find potential mechanical fatigue problems. The most critical parts of a LED lamp design from the reliability point of view is usually solder interface between LED package and LED board or LED package and LED die [25] [29]. In this work five new LED boards have been designed using two new technologies (IMS and Leadframe)[19]

2.5.1 LED Boards design and models

Performance of five new LED boards (Figure 2.25) was compared to reference LED board from thermal and thermo-mechanical point of view. An essential aspect in 3D FEM simulation is the conception of the geometric model. The geometry and shape of LED lamp is intrinsically complex. Six detailed models were built:

- ***Design A*** - *FR4 board of existing 8W retrofit LED lamp (reference model)* – Figure 2.25*a*
- ***Design B*** - *New LED board concept 1 with Luxeon Rebel LEDs*– Figure 2.25*b*
- ***Design C*** - *New LED board concept 2 with Luxeon Rebel LEDs* Figure 2.25*c*
- ***Design D*** - *Insulated Metal Substrate (IMS) board with Luxeon Rebel LEDs* –Figure 2.25*d*
- ***Design E*** - *IMS board with a new LED package design.*- Figure 2.25*e*
- ***Design F*** - *New LED board concept 3 with the new LED package design* Figure 2.25*f*



a) b)

[19] The design of new LED boards has been done with cooperation of Philips Lighting, CEA LETI and Boschmann

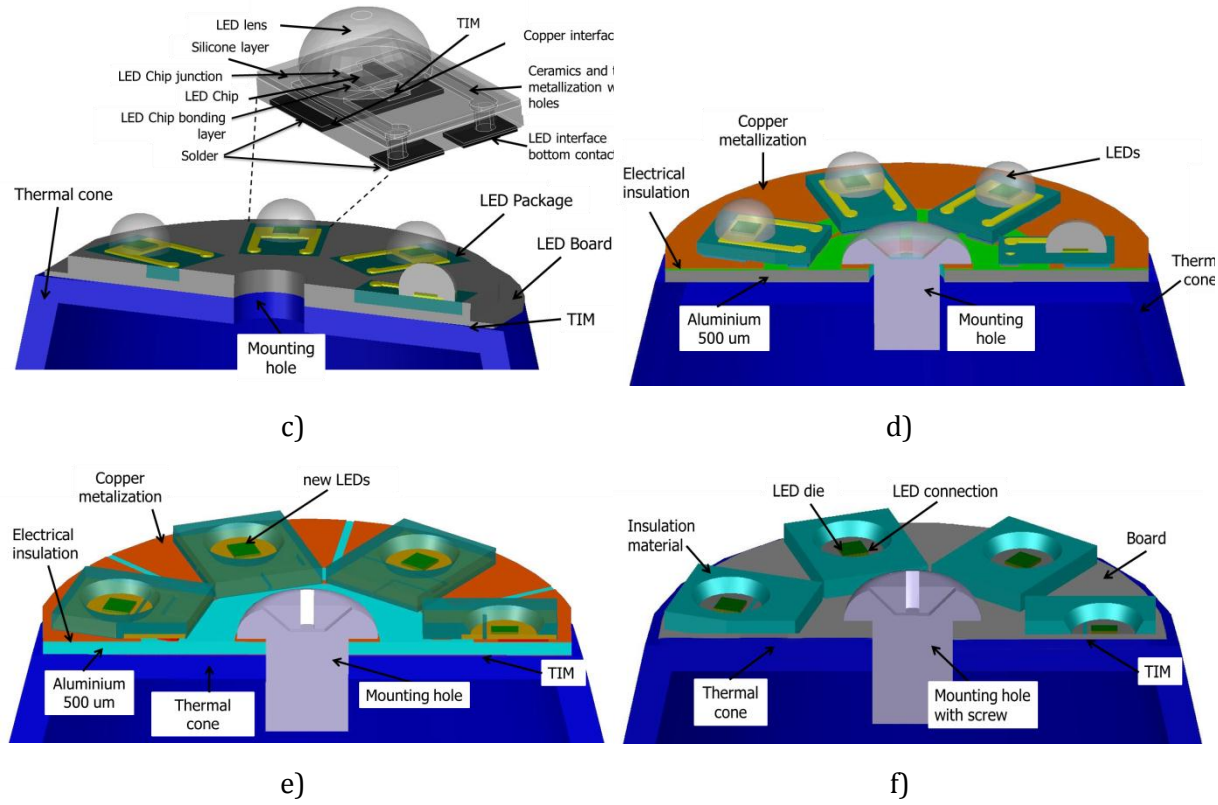


Figure 2.25: Design of new LED board models[20] [3]

For each technology, a detailed 3D model has been built, including six packaged high power LEDs on the LED board. The LED board diameter and placement of LEDs on the board are the same for all cases [3].

In FEA simulation meshing is an important step since it affects the accuracy of the final results. Because of many non-orthogonal parts in the model, tetrahedron elements are used. The element distribution is adapted to the shape of the model parts. Small features, where high stress is expected, were meshed with more detail. Designed models contain approximately 600,000 nodes.

The validity of simulation results is limited by the accuracy of the material properties data. Thermal coefficients for all used materials has been summarised in Table 2-4. To obtain realistic plastic deformation behaviour of the LED boards, mechanical properties of all materials have been described by temperature dependent stress-strain curves [37].

2.5.1.1 New LED Boards thermal evaluation

The new boards were designed as possible replacement of the reference LED board. Their performance is evaluated by comparing thermal and mechanical properties. Thermal and thermo-mechanical modelling of LED boards was completed by ANSYS finite element simulation tools.

[20] Some details are not shown because of CSSL project confidentiality

One way how to determine thermal properties of LED boards is to compare their thermal resistance. In this case thermal boundary conditions must be defined in the same way for all LED boards. Thermal resistances are calculated as temperature difference between two defined points at specified heat dissipation in active parts. For example, the thermal resistance of LED package in is our case defined between top side of LED die and bottom side of copper thermal pad [3].

To ensure the same heat flux distribution as in case of whole lamp modelling, the LED boards are placed on a heat sink (thermal cone with housing) that emulates the lamp real working conditions. By this arrangement we can insure same heat distribution at bottom side of the LED board. The total heat power dissipation of 4 W is considered in six LED chips. Free convection and radiation that take place on all surfaces of LED board which are supposed to be in contact with air (material infrared emissivity was determined experimentally) ware correspondingly considered. Figure 2.26 shows a temperature comparison, among other parts, for the LED chip where we find the lowest temperature for Design F (new LED board concept 3 with the new LED package). As we can see, the LED chip temperature is almost five degrees lower than the temperature at Design A (Reference model). More detailed analysis of the material results can be derived from thermal resistance values (Table 2-7), computed separately for each LED package including soldering layer and for each LED board. We can see a big difference between the reference LED board with thermal resistances between 9.01 and 9.94 K/W (Design A-D), and the new LED package design where computed thermal resistance dropped to values between 2.18 and 2.83 K/W. The lowest LED board thermal resistance is calculated for the IMS board (1.89 K/W) which is more than two times lower that in case of reference model (4.81 K/W) [3] [56].

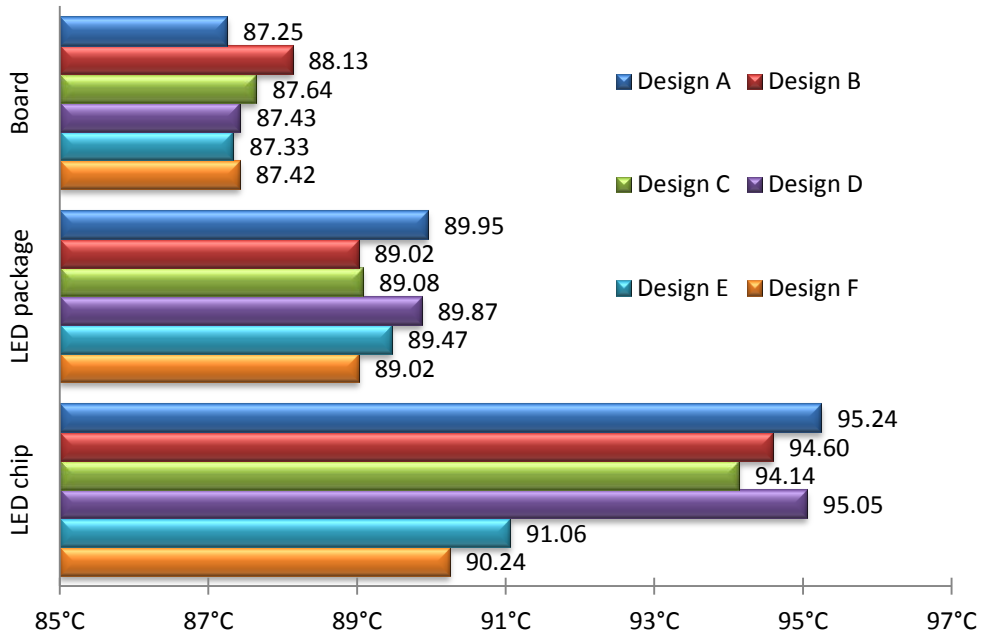


Figure 2.26: LED boards temperature comparison sampled at LED chip, LED bottom side of the package and LED board [3].

Table 2-7 LED boards thermal resistances comparison [3]

Thermal resistances					
Board type	**LED package+ solder**	**LED Board + TIM**	**LED + solder + board**	**Aluminium cone**	**Total**
	(K/W)	(K/W)	(K/W)	(K/W)	(K/W)
Design A	9,44	**4,81**	14,24	12,88	27,12
Design B	9,94	**1,58**	11,52	14,43	25,95
Design C	9,01	**2,56**	11,57	13,58	25,15
Design D	9,35	**1,89**	11,24	13,56	24,80
Design E	2,18	**2,85**	5,03	13,23	18,26
Design F	2,83	**3,79**	6,62	13,07	19,71

Leadframe LED board thermal resistance depends heavily on used moulding material. The market offers moulding compounds with thermal conductivity from 0.7 – 10 K/W. Figure 2.27 shows influence of compound moulding material thermal conductivity on LED board thermal resistance of two leadframe designs. For new leadframe LED board's two new moulding materials are considered with thermal conductivity of 2 W/m.K and 9.8 W/m.K. In case of Design B the difference in whole LED board and LED package thermal resistance is rather small (0.18 K/W) but in case of Design A the difference of thermal resistance is quite high (1.8 K/W). This difference can make a LED chip temperature change more than 3°C. Thermal resistance of leadframe LED boards without LED package is summarized in Table 2-8.

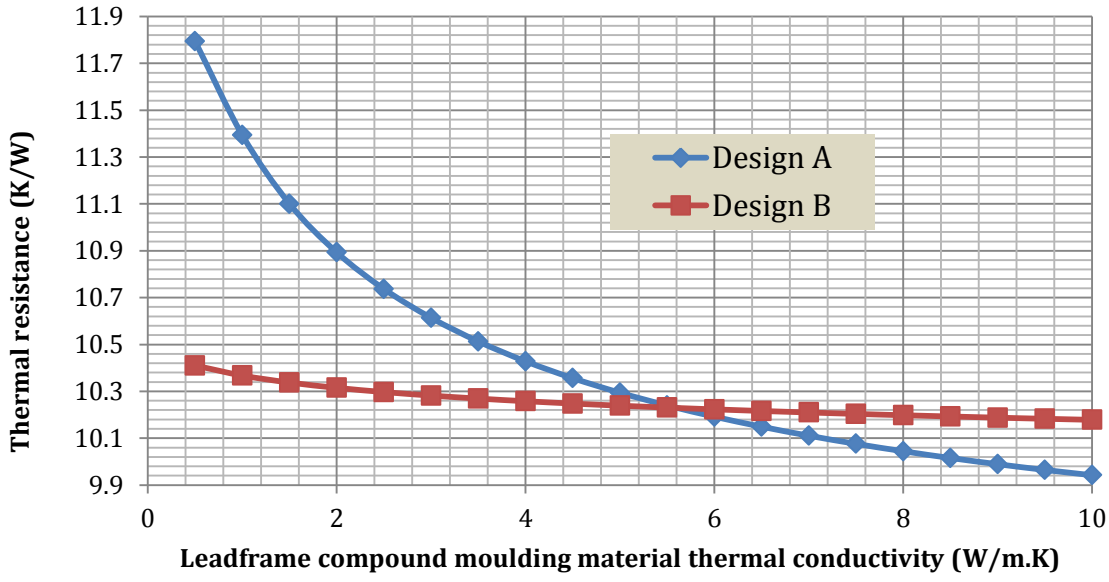


Figure 2.27: Influence of compound moulding material thermal conductivity on LED board thermal resistance of two leadframe designs

Table 2-8: Thermal resistance of leadframe LED boards designs for three values of moulding compound thermal conductivity

Moulding compound thermal conductivity	0.5	2	10
Leadframe Design A R_{TH}	1.5	1.6	1.7
Leadframe Design B R_{TH}	1.6	2.5	3.4

2.5.2 Thermo-mechanical evaluation of designed LED boards

Calculations of mechanical stresses that are produced by different thermal expansion coefficients of the used materials are very important for the LED board reliability. LED board models were designed with all LED package details, mounting pads, TIM, metallic leads and thermal vias placed under each LED package (Figure 2.25).

Calculations of mechanical stresses that are produced by different thermal expansion coefficients of used materials are very important for the LED board reliability. The same LED board models (Figure 2.25) were used for calculation of mechanical LED board deflection and stress distribution by ANSYS thermo-mechanical structural analysis. Mechanical boundary conditions mechanically fix an inner face node of the central hole. This boundary condition reflects the fact that the LED board is fixed to the thermal cone by a central screw. All other model nodes can freely move in all directions. Thermal boundary conditions are set differently for two cases. The first represents LED boards in real operational temperature distribution. For that case the heat flux at the bottom face of the LED boards has been derived from the thermal analysis of the LED lamp model [46]. Convection (5 W/m^2K to air) and radiation has been prescribed on the top surface of the board and LEDs. The total heat power dissipation of 4 W has been considered for six LED chips. The second case represents LED board stored in limit temperature -40 ^oC where uniform temperature distribution has been applied on all parts of the LED model. Zero stress temperature for all materials has been defined according to assumed moulding and soldering fabrication processes. Thermal stresses were calculated by Static structural analysis for three most interesting temperature cases, e.g. an extreme storing temperature (-40^oC), for room temperature (22^oC) and for operating temperature (as the board is heated by power dissipation in the LED chips) [3].

Figure 2.28 shows the calculated residual stress distribution comparison of all models which is based on an elastic-plastic approach. Figure 2.29 shows the comparison of calculated maximum residual stresses of all LED boards. The maximal value of residual stress in all new LED board designs is found for the temperature of -40 ^oC. Mechanical stresses generally reduce when temperature is increased. This is caused by the initial stress formed when LED package is soldered on the LED board [3].

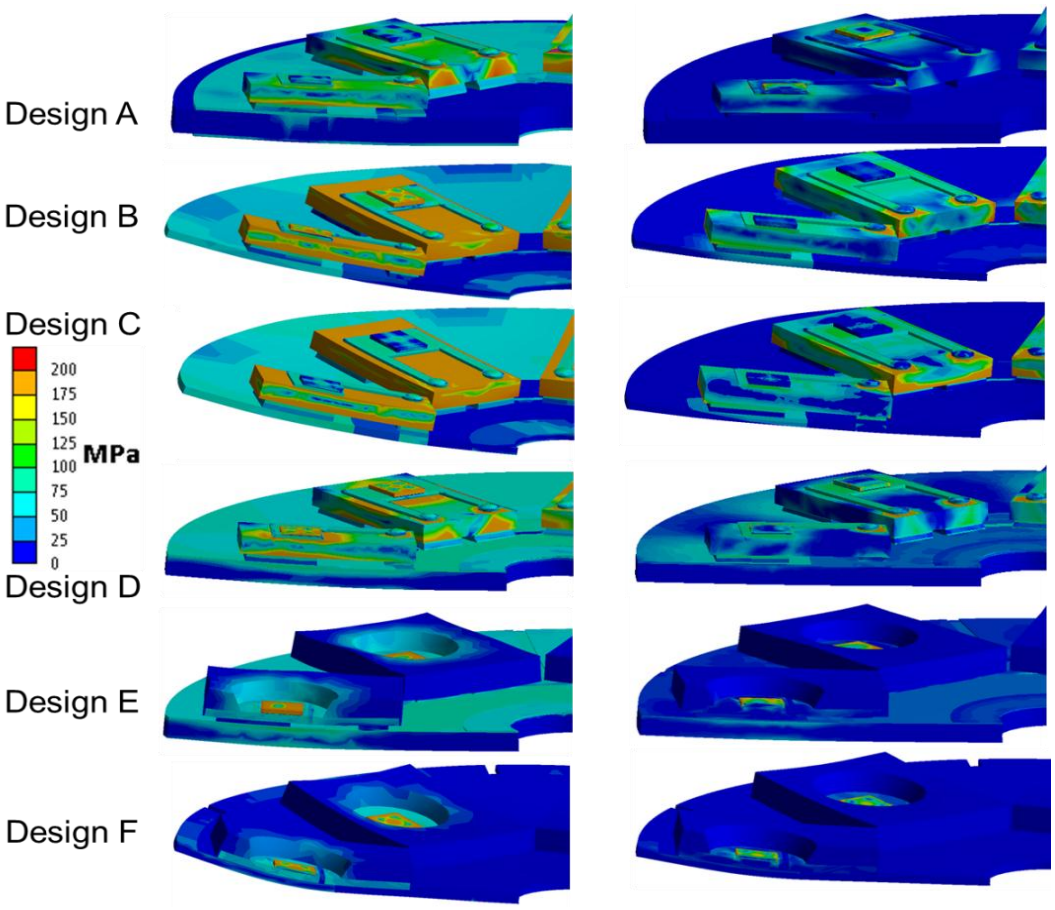


Figure 2.28: Thermal stress distribution in LED boards. Deformation is 5x magnified. for a) Master LED board Design A, b) Leadframe Design B, c) Leadframe Design C, d) IMS Design D, e) Leadframe Design E f) IMS Design F

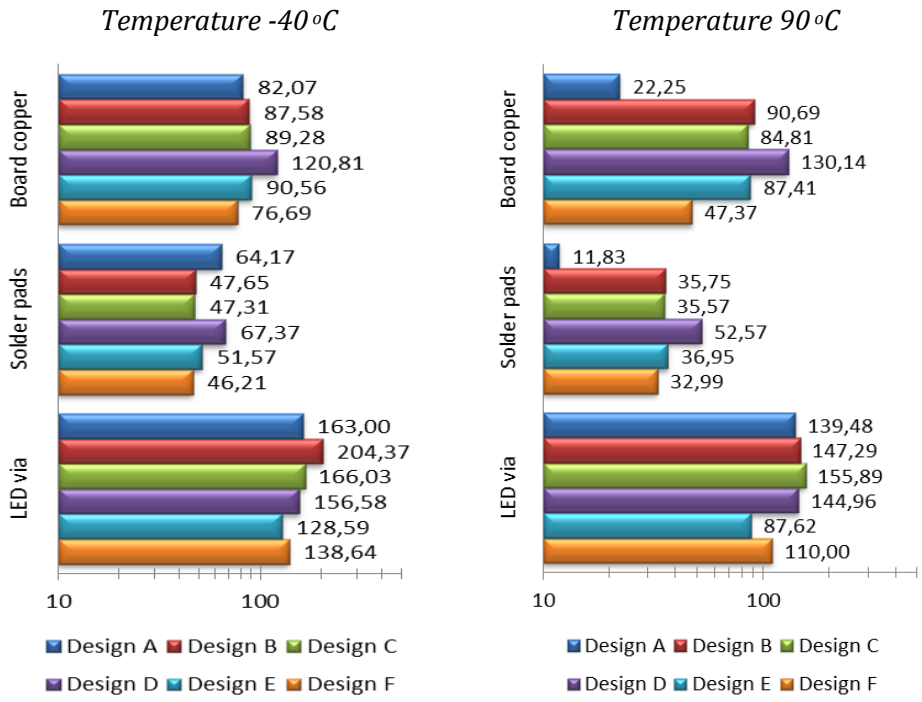


Figure 2.29: LED boards maximum residual stress sampled at LED via, Solder pads and LED board copper

2.6 Accelerated characterization methods for SSL LED boards

Main goal of the work presented in this chapter is development of an innovative accelerated LED board testing method based on mechanical load cycling that could be an alternative replacement of currently used thermal cycling test. The results of on-going research activities of alternative accelerated ageing and characterization tests are reported in this chapter.

2.6.1 General description and work motivation

Some of the main advantages of solid state lighting [SSL] systems are the high efficiency and (expected) long lifetime. As has been already shown in previous chapters, one of the most critical parts of the SSL lamp from life time and reliability point of view is LED board including soldered LED package [57]. To ensure lifetime and good light quality, a lamp design is needed to meets strict requirements in terms of heat dissipation, electrical insulation and light conversion.

New accelerated testing methods are based on the calculation of thermo-mechanical stresses in the LED board, which are caused by thermal cycling, and the computation of an equivalent mechanical force. Corresponding force is assumed to yield very similar residual stresses distributions and mechanical deflection of the LED board as thermally induced stresses does. Mechanical force is enforced on the LED board in a pneumatic shaker test set-up. It allows managing of a creep rate in solder joints (as a test parameter) as well. New method under development could simplify and significantly speed up mechanical and thermal cycling lifetime evaluation.

Accelerated lifetime testing (e.g. thermal, mechanical and electrical) is carried out in order to study the failure behaviour of current and newly developed LED boards. Among others the tests will help in further refinement of the failure models of LED boards.

2.6.2 Methodology of acceleration testing method for LED boards

Solder bonds and electrical metallic lines failure caused by thermo-mechanical stress is a wear-out mechanism in electronic systems design. Relatively small number of thermal cycles (in order of thousands) can lead to rapid failure especially in solder joints [58]. The mismatch of thermal expansions of LED package materials and LED board materials can induce very high mechanical stresses especially in small solder joints that connect component package with PCB board [57]. Solder joint failure occurs when thermal stress drives the periodical repetition of thermal expansion contraction of applied materials. When thermo-mechanical stress becomes higher than value of yield stress a local plastic deformation occurs in certain areas. Moreover accumulation of creep strain can play a dominant role in such a case. These accumulated strains can initiate cracks in material propagating further in each next thermal cycle.

Reliability of thermally stressed electronic devices is usually tested by thermal cycling or power cycling test in a thermal chamber. The same test is provided to predict lifetime of LED boards. Main disadvantage of this method is very long testing time (often several months). Typical thermal cycle setup is 30 min at high temperature (120 °C for LED boards) and 30 min at low temperature (-40 °C for LED boards). Usual number of cycles that lead to LED board failure is between 3000 and 8000 cycles [59]. The total time for this test could be in the range of hundreds of days! Moreover, high energy consumption is another disadvantage of thermal cycling tests.

Proposed accelerated testing method under development could simplify and speed up thermal cycling test. Mechanical cyclic forces imposed on LED board could result in very similar residual stress and mechanical deflection shape as thermal stress does (range of temperature change from -40 to 120°C). This can be especially true for symmetrical board structures as for instance circular LED board. Key issue here is precise computation of mechanical force, which deflects the LED board. This mechanical deflection is put in confrontation with deflection caused by thermal stress. Calculated equivalent force can be than applied in mechanical bending test. Two types of mechanical bending tests are proposed.

First method applies a high speed periodical mechanical loading to LED board. Deflections of the LED board impose a mechanical stresses in LED board assembly. This so called vibrational fatigue test causes failure mainly in solder joint between LED package and LED board [60]. The duration of this test can be very short, because vibration frequency range is set between 10 and 2000 Hz and typical number of cycles that cause a failure is in order of hundreds of thousands. It should be pointed out that some failure mechanisms are suppressed here. Mechanical excursions are without time to induce creep relaxation effects in solder material. This test investigates the effects of different material properties of soldering material to different failure modes. The vibration test could not fully replace power or thermal cycling test (Chapter 2.6.4).

The second method was proposed as accelerated method which could replace thermal or power cycling test. The main idea of accelerated testing methodology is based on computer calculation of thermal residual stresses and forces in solder joints during power or thermal cycling test. In this analysis accumulated creep strain in solder joints has to be defined during a thermal cycle. The second step is and finding of equivalent mechanical force that will imply comparable accumulated creep strain value in solder joint of interest. More details can be found in (Chapter 2.6.9).

Figure 2.30 shows flowchart of proposed lifetime prediction methodology. Left flow chart shows computer calculations of elastic, plastic and creep strains in the model of interest. In this step we should decide if thermal cycling induces only elastic and plastic strain or if a creep strain plays dominant role. The right flow chart shows steps needed for accelerated fatigue test.

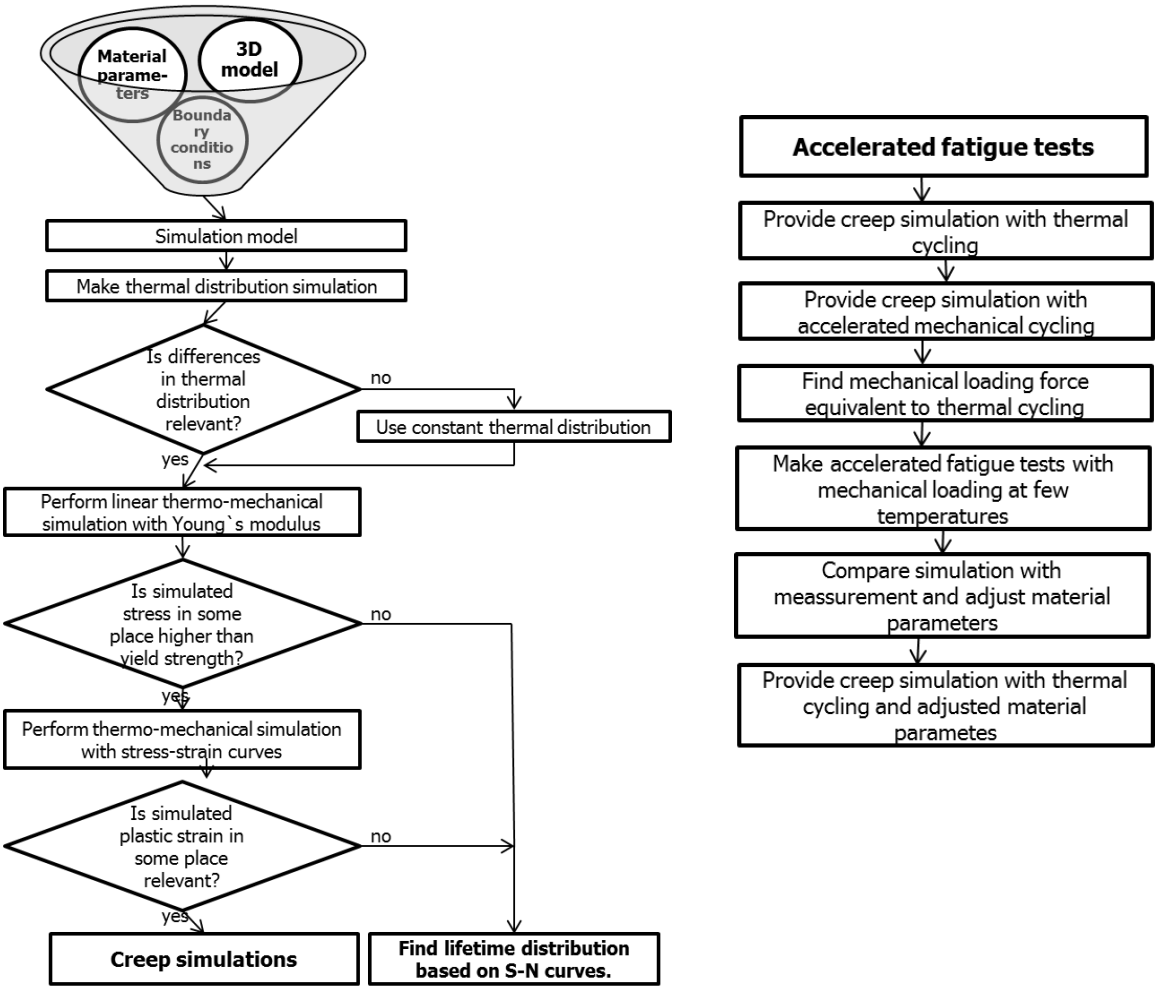


Figure 2.30: Flowchart of lifetime prediction

2.6.3 Lead less solder joints fatigue models - theory

One of the most important factor concerning thermally stressed (or thermally cycled) electronics devices systems from the reliability point of view is mechanical and electrical bonding between electronic device packages and PCB board [61]. Thermal expansion coefficients and stiffness mismatch between PCB board and electronic component package results high thermal stress in solder joints during thermal cycle. Life time prediction models for solder joints fatigue requires four major constituents [53]:

- *Definition of constitutive equation;*
- *Determining of methodology of the damage mechanism;*
- *Experimental data measured on real component; and*
- *FEM simulation can calculate thermal or mechanical stress distribution in solder joint.*

A number of papers have been published recently on lead less solder joints fatigue models [58] [57] [61] [53] [62]. There are generally five models categories [61]:

- *Mechanical stress-based,*
- *Plastic strain-based,*

- *Creep strain-based,*
- *Energy-based, and*
- *Damage-based.*

All of these models are established on constitutive equations for given solder material and thermal cycling fatigue data on actual solder joint type (that means shape and thickness of solder join layer). After defining right constitutive equation and its constants, a finite element modelling techniques are used for mechanical stress and strain distribution (in LED board in our case) and for life time calculation.

Table 2-9 below summarises classification of the most important models and coverage of effects.

Table 2-9: classification of the most important component bonding models and coverage of related effects

Model	Model class	Needed parameters	Coverage	Note and Ref
Coffin-Manson	Plastic strain	Plastic strain	Low cycle fatigue	[63]
Total strain (Coffin-Manson-Basquin)	Plastic strain + elastic strain	Strain range	High and low cycle fatigue	Bending test [62] [64]
Solomon	Plastic shear strain	Plastic shear strain	Low cycle fatigue	[65]
Engelmaier	Total shear strain	Leaded and leadless, TSOP	Low cycle fatigue	[65] [61]
Miner	Superposition (plastic and creep)	Plastic failure and creep failure	Plastic shear and matrix creep	[66]
Knecht and Fox	Matrix creep	Matrix creep shear strain	Matrix creep only	[66]
Syed	Accumulation of creep strain energy	Accumulated energy	Implies full coverage	Slow creep Test [53]
Heinrich	Energy density based	Energy	Hysteresis curve	[67]
Darveaux	Energy density based	Damage + energy	Hysteresis curve	[68]

2.6.3.1 Mechanical stress based models

Stress based models typically applies periodical stress vibrations on the sample. These models are not used much for solder joint bonding evaluation. Main reason for that it is difficult application of mechanical stress directly to the solder joints.

2.6.3.2 Strain based models.

The better method is applying of mechanical deflection or strain on whole PCB board. Deflection results mechanical stress within solder joints. Coefficients of thermal expansion TCE which induce thermal stresses can be also included to this category. Up to now many different models has been published. Most relevant to proposed accelerated characterization

method for LED board evaluation are Coffin-Manson, Solomon and Engelmaier models that are based on plastic stain fatigue [53]. These models calculate number of cycles to failure based on experimental determination of the plastic strain. Coffin-Manson model computes the total number of cycles to failure N_f in dependence on plastic strain amplitude $\Delta\varepsilon_p$, fatigue ductility coefficient and ductility exponent c [63]:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_f(2N_f)^c \qquad (2.20)$$

Ductility coefficient and exponent in equation 2.20 must be for required material determined experimentally. For lead fee solders (as SAC305 that are has been used in proposed LED boards) those coefficients has determined by Schubert at al [62] and Hong at al [64].

Coffin-Manson equation is usually combined with Basquin equation to take into account elastic deformations as well [63]:

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f}{E}(2N_f)^b + \varepsilon_f(2N_f)^c \qquad (2.21)$$

$\Delta\varepsilon$ is the strain range, σ_f is the fatigue strength coefficient, E is the elastic modulus, ε_f is the fatigue ductility, b is the fatigue strength, and c is the fatigue ductility exponent. Figure 2.31 explains relationship between low cycle and high cycle region which results the total strain equation.

Equation 2.21 is used for high speed mechanical loading calculation of LED board.

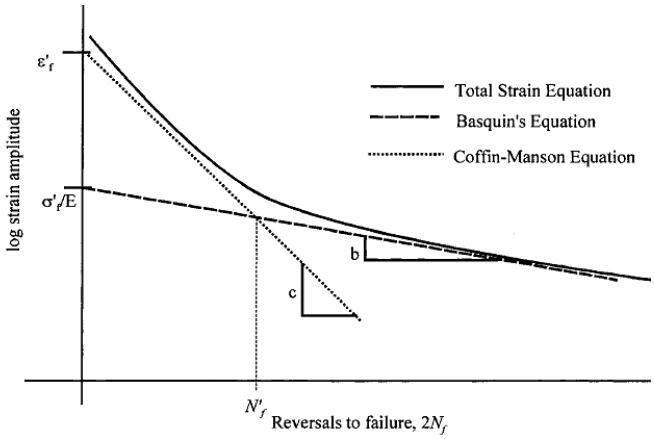


Figure 2.31: Coffin-Manson-Basquin total strain versus number of cycles to failure [61]

Solomons constitutive low cycle model [65] describes fatigue behaviour to the plastic strain and requires experimental determination of plastic strain range:

$$\Delta\gamma_p N_p^{\alpha} = \theta \qquad (2.22)$$

$\Delta\gamma_p$ is the plastic shear strain range, N_p is the number of cycles to failure, θ is the inverse of the fatigue ductility coefficient, and α is a material constant. Disadvantage of this model is that describes only low cycle fatigue without creep effect that is usually dominant especially in thermal or power cycling tests [62]. Solomon model use for solder joints is then limited. Moreover, the constants Θ and α depends on solder joint geometry.

Engelmaier fatigue model [65] [61] improves Coffin-Manson and Solomon model taking into account frequency and temperature effects. Unfortunately, the main disadvantage is that all

constants are dependent on solder joint shape and solder material. The constants must be measured for specific solder joints and are hardly transferable to other solder joint type [62].

2.6.3.3 Creep strain based models.

Addition of creep strain into above mentioned fatigue models provides a more complete approach. The most important creep strain based models above others are represented by Miner, Knecht and Fox [66] and Syed model [53]. Creep can be separated into two possible mechanisms. The first mechanism is matrix creep and the second is so called grain boundary creep. Creep mechanism in solder joints may be caused due to grain boundary sliding and by dislocation movement which cause the matrix creep [62].

The model that describes the Matrix creep is proposed by Knecht and Fox [66] where number of cycles to failure N_f can be expressed:

$$N_f = \frac{C}{\Delta\gamma_{mc}} \qquad (2.23)$$

Constant C is dependent on failure criteria and solders microstructure. $\Delta\gamma_{mc}$ is the strain range due to matrix creep.

Accumulated creep strain based model for SnAgCu solder joint taking into account the grain boundary sliding creep is well described by Syed model [53]. The lifetime prediction methodology is established on calculating of accumulated creep strain during one temperature cycle. Number of cycles to failure can be expressed as [53]:

$$N_f \left(\frac{\sum_{i=1}^{n} \Delta t_i \varepsilon_{cri}}{\varepsilon_f} \right) = 1 \qquad (2.24)$$

Where ε_{cri} is the steady state creep rate for stress level σ_i, Δt_i = time spent at stress level σ_i within a cycle, ε_f constant gives the "creep ductility" or the strain at the onset of failure. Numerator term within summation sign in equation 2.24 is the creep strain accumulated during Δt time. Summation for all n steps in thermal cycle gives [62]:

$$\varepsilon_{acc} = \sum_{i=1}^{n} \Delta t_i \varepsilon_{cri} \qquad (2.25)$$

Where ε_{acc} is the accumulated creep strain per cycle. Then the equation 2.24 can be simplified as:

$$N_f = (C' \varepsilon_{acc})^{-1} \qquad (2.26)$$

Where N_f is number of cycles to failure C' is inverse of creep ductility.

For two creep mechanisms (grain boundary sliding and the matrix creep) the above equation becomes:

$$N_f = (C_I \varepsilon_{acc}^{I} + C_{II} \varepsilon_{acc}^{II})^{-1} \qquad (2.27)$$

ε_{acc}^{I} is the accumulated equivalent creep strain per cycle for grain boundary sliding and ε_{acc}^{II} is the matrix creep. The constants C^I and C^{II} in the above equation have been determined for SnPb solders by Sayed in [53]:

$$N_f = (0.022 \varepsilon_{acc}^{I} + 0.063 \varepsilon_{acc}^{II})^{-1} \qquad (2.28)$$

And for SnAgCu solders (SAC305) [53]:

$$N_f = (0.106 \varepsilon_{acc}^{I} + 0.045 \varepsilon_{acc}^{II})^{-1} \qquad (2.29)$$

The limitation of Syed model is the absence of plastic strain effects. Plastic strain can be neglected only if the plastic strain rate is much lower than creep strain rate. However this can be proved by FEM simulation. More discussion on this problem is on 2.6.9. Syed model is one of the most suitable for LED board solder joint life time evaluation because experimental data was collected for the same solder joint type (SAC305) [62].

If the grain boundary sliding is much smaller in comparison with matrix creep, the total accumulated creep strain can be expressed taking into account only one creep effect. This simplifies the number of cycles to failure calculation. The number of cycles to failure equation using the total accumulated creep strain is then [53]:

$$N_f = (0.0468\varepsilon_{acc})^{-1} \qquad (2.30)$$

This shortens the post-processing calculations in FEM simulator because hyperbolic sine constitutive model for creep calculation can be used.

Miner's model combines the Solomon and the Knecht and Fox model [62]:

$$\frac{1}{N_f} = \frac{1}{N_p} + \frac{1}{N_c} \qquad (2.31)$$

N_p is the number of cycles to failure due to plastic fatigue and is obtained directly from Solomon's fatigue model. N_c is the number of cycles to failure due to creep fatigue and is obtained from Knecht and Fox's creep fatigue model.

A lot of different factors have to be taken into account applying above mentioned models. One of the most important is solder joint geometry and cycling temperature. Solder joint geometry specific data can be evaluated by experimental work or by FEM calculation.

2.6.3.4 Energy based fatigue models

Those models predict the accumulated energy which is required to initiate crack propagation in solder joint. Failure is predicted by energy hysteresis that is typically calculated by some correlation to energy under stress-strain hysteresis loop. There are many papers today reporting the energy based models [67] [68] [69]. All these models are very strictly dependent on solder type and geometry. For example Wu at al [68] reported study of BGA package using Heinrich's energy fatigue model to calculate number of cycles N_0 to initiate the crack:

$$N_0 = 18083\Delta W^{-1.46} \qquad (2.32)$$

ΔW is the viscoplastic strain energy density per cycle.

The main drawback of energy based model is not possible direct calculation of the number of cycles to failure. Only crack initiation is predicted [62].

To complete this short review a damage failure models should be also mentioned shortly. They are based on either fracture mechanisms or creep and fatigue mechanisms. Because microstructure is not directly addressed in fracture mechanisms, the main focus is on constitutive theoretical level dependent on FEA calculations [62].

2.6.4 LED board life time calculation - high speed mechanical cycling

The thermally induced mechanical forces acting on LED boards can be calculated using mechanical "Transient structural (Plastic)" analysis and Fatigue analysis. The corresponding mechanical force can be applied to mechanically deflect the LED board in the so-called "shaker" test set-up, as shown in Figure 2.32. The testing apparatus is made of an electromagnetic actuator (vibrational shaker), a mechanical lever that increases periodical force applied on LED board and a clamping support for LED board. The LED board is mechanically fixed on the on the outside perimeter of FR4 board at top and bottom side. Internal mounting hole of the FR4 board is mechanically coupled to a shaft which imposes the force of the shaker Figure 2.32b.

The value actuated mechanical force is calculated by FEM analysis (ANSYS simulation tool) to impose same LED board deflection as thermal stress does in temperature range -40 to 120°C. The reference LED board model (Figure 2.17) was designed according Philips LED board for 8W retrofit LED lamp.

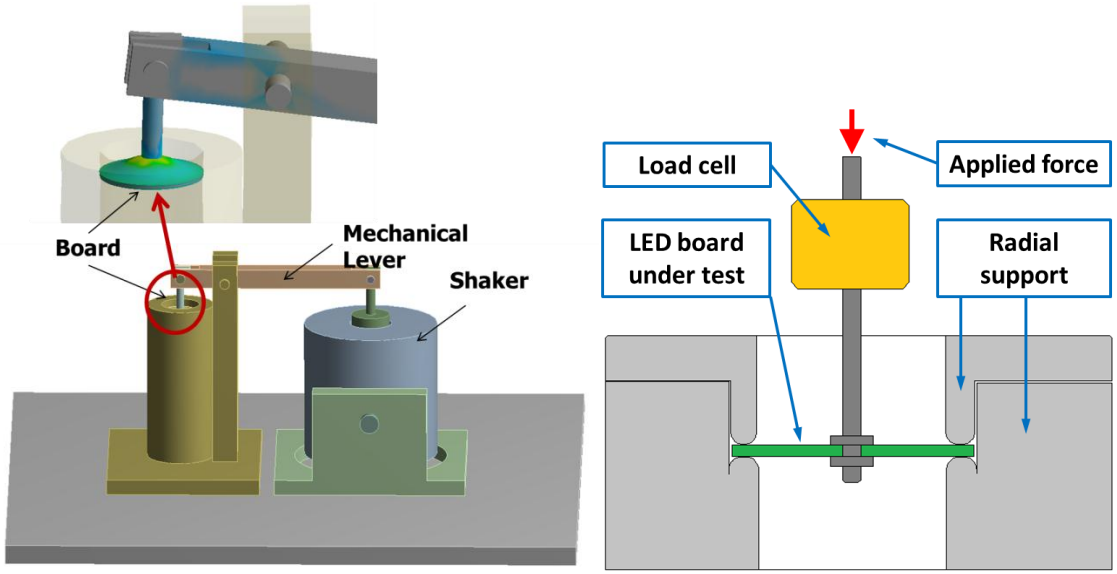


Figure 2.32: Measuring equipment: a) 3D model for FEM analysis b) detail of LED board mechanical fixation

To obtain corresponding force for mechanical bending test the thermo-mechanical analysis is carried out in two steps. The first one calculates the stress distribution and LED board deflection for temperature range that LED board may be exposed (-40°C and 120°C). In the second analysis the mechanical force that imposes the same mechanical deflection and similar stress distribution on the LED board as occurs in case of temperature cycling is found. This mechanical force is applied as mechanical load in the mechanical bending test set up. The simulation take into account an initial intrinsic stress induced in LED board. This is done by defining zero stress temperature for all board materials. This temperature corresponds to moulding and soldering fabrication processes. Mechanical boundary condition sets all inner mesh vertexes of the LED board FEM model of the central mounting hole to be mechanically fixed, since a central screw attaches this point to the thermal cone. All other nodes of the model can freely move in all directions.

Figure 2.33a shows residual stress distribution on the top and bottom side of the FR4 LED board calculated for a temperature of -40°C compared with the stress distribution when a mechanical force of -20 N is applied. The stress distributions are almost identical in this case. Figure 2.33b shows the comparison between LED board deflection caused by thermal stress at -40°C and mechanical load of -20 N. Given thermal stress result slightly smaller mechanical deflection then mechanical loading does. The same analysis was carried out for temperature 120°C. The comparative results are summarised on Figure 2.33c) and d).

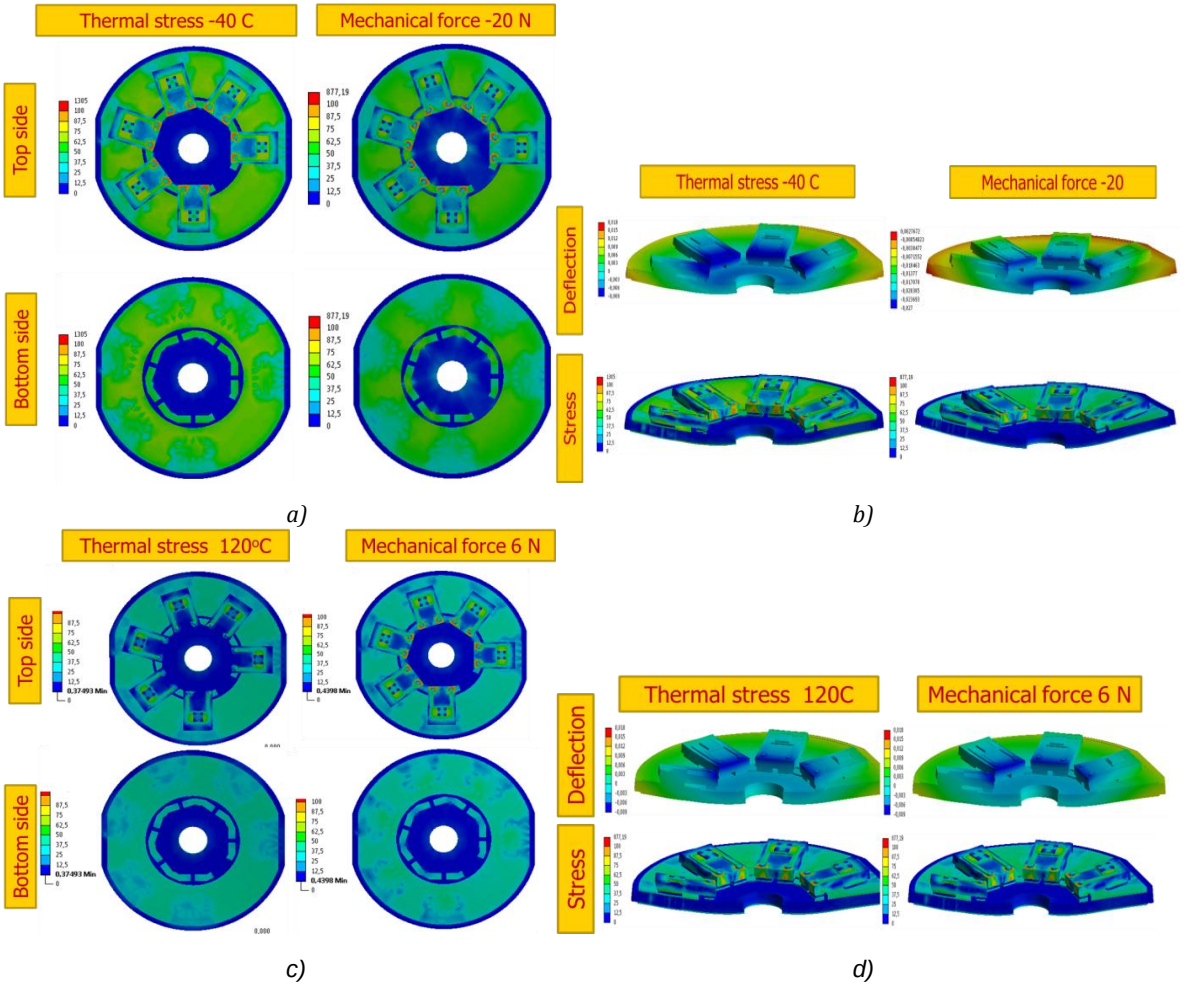


Figure 2.33: Stress distribution for LED board at temperature of -40ºC and stress distribution of applied mechanical force of -20N; b) comparison of LED board deflection caused by thermal stress at temperature of -40ºC and mechanical force -20N; c) Stress distribution for LED board at temperature of 120ºC and stress distribution of applied mechanical force of -20N; d) comparison of LED board deflection caused by thermal stress at temperature of 120ºC and mechanical force -20N

High speed mechanical load cycling life time prediction has been calculated by plastic strain based Coffin-Manson-Basquin model (equation 2.21). The analysis has taken into account the elastic and plastic behaviour of the LED board materials (defined by stress-strain curves is chapter 2.4.3) and life time S-N curves (Figure 2.34) [37]. This analysis shows the probability of initiation and propagation of cracks in the most mechanically stressed areas and possible failure with respect to thermo-mechanical stresses that are induced by thermal cycling of LED boards.

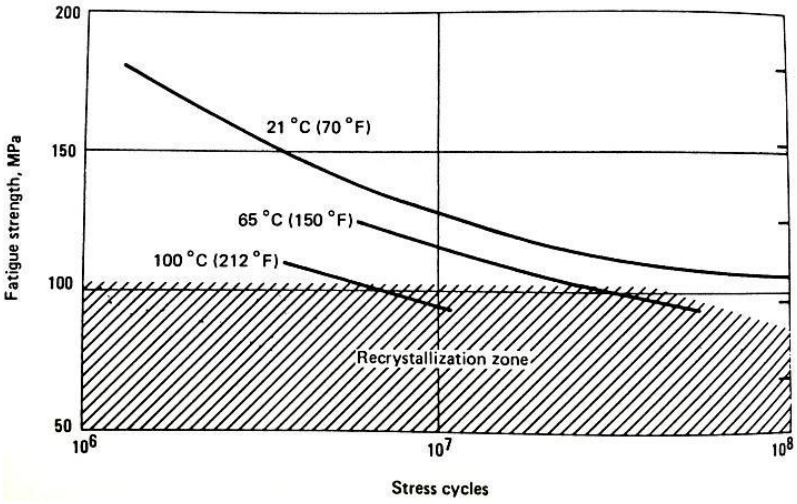


Figure 2.34: S-N curve for SAC305 solder [37]

2.6.4.1 Master LED board Lifetime evaluation and validation

Solder bonding and electrical metallic lines failure caused by mechanical and thermal stress is a wear-out mechanism in thermally affected electronic system designs [70]. One of the most important factors concerning mechanically or thermally stressed (thermally cycled) LED boards from the reliability point of view is electrical bonding between LED packages and PCB board. At these locations very thermal stresses usually appear [71].

The advantage of high speed mechanical bending test of LED boards is simplicity and fast testing time. Some failure mechanisms are not considered using this approach. Fast mechanical cycling does not allow incorporate creep relaxation effects, which can especially occur in solder material. Nevertheless, this method is good for determining of the weakest spots of the structure. Qualitative comparison between different LED board technologies is then possible. In particular, our lifetime prediction method calculates the response of high speed periodical mechanical loading. The loading deflects the LED board, which, in turn, imposes mechanical stresses in LED board assembly (i.e., LED package and board).

Strain based models is good choice for the calculation of the number of cycles to failure. As has been already shown, the most relevant method for LED board evaluation is the Coffin-Manson-Basquin model (see chapter 2.6.3), that is based on a plastic-strain fatigue approach. The model calculates the number of cycles to failure based on experimental data of the plastic-strain curve of the used materials.

To obtain the appropriate force for the mechanical bending test, the thermo-mechanical analysis is carried out in two steps. The first one calculates the stress distribution caused by temperature change (-40°C and 120°C). The second step calculates mechanical force that imposes the same mechanical deflection and stress distribution in the LED board as in the first case. Calculated equivalent mechanical force is then applied as a mechanical load in the mechanical cycling test set up. The simulation takes into account an initial intrinsic stress induced in the LED board due to the manufacturing process (e.g., due to moulding and soldering processes).

Mechanical boundary condition prescribes all inner mesh vertexes of the LED board model of the central mounting hole to be mechanically fixed, since a central screw mechanically fixes this face to the thermal cone. All other nodes of the model can freely move in all directions.

In this study, high speed cycling mechanical loading is considered; therefore creep material behaviour has play a minor effect. Figure 2.35 shows that plastic deformation of solder (SAC 305) is more predominant at bending frequencies faster than 1 Hz. The accumulated creep strain is three order smaller then accumulated plastic strains. The creep strain was calculated by implicit constitutive relation [53]:

$$\varepsilon_{cr} = A_1[sinh(\alpha\sigma)]^n exp\left(\frac{-H_1}{kT}\right) \qquad (2.33)$$

where σ is mechanical stress and constants for solder are [53]: A_1 = 277984 s^{-1}, α = 0.02447 MPa^{-1}, n = 6.41, H_1/k = 6500.

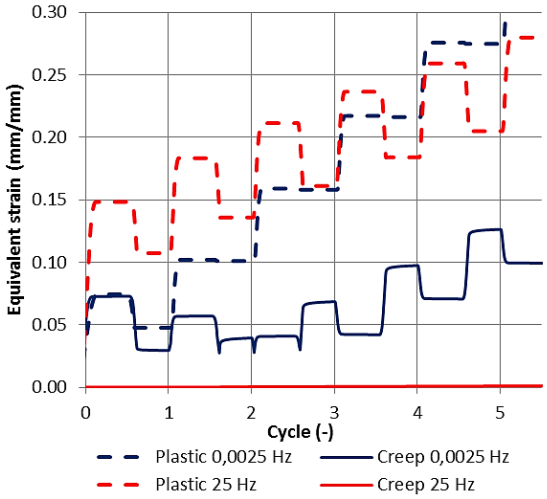


Figure 2.35: Simulation of maximum value of accumulated equivalent creep and plastic strain in solder pads at different mechanical loading frequencies.

Life time simulation shows the probability of initiation and propagation of cracks in the mechanically most stressed parts.

Figure 2.36 shows the lifetime distribution (number of cycles to failure) for most interesting LED board parts. As we can see more problematic parts are solder joints and vias. The graph on Figure 2.37 summarises the calculated lifetime of the most stressed parts (the metal vias in the LED board and the interconnection area that contacts the LED package with the copper metallization on that board).

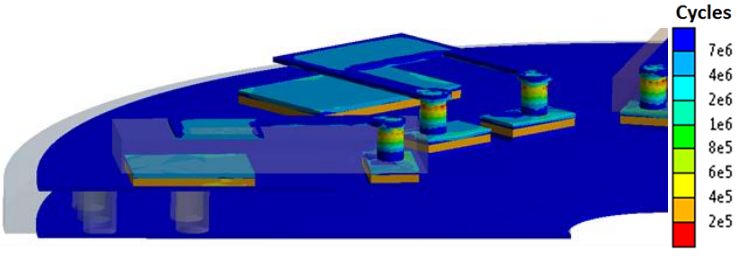


Figure 2.36: Distribution of calculated lifetime in the metallic connection of the LED board.

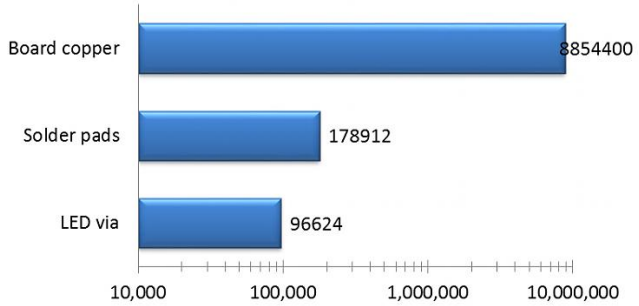


Figure 2.37: Calculated lifetime for LED board copper layer, solder pads between LED board and LED package, and LED package via.

2.6.4.2 LED board life time validation by high speed cycling

Initially, bending test is carried out to verify the solder joint life time and reliability of LED board. For this purpose a shaker mechanical assembly has been constructed for LED boards bending. In this test the testing machine apply periodical mechanical load to LED board using 25 Hz sinusoidal wave with amplitude 15 N (value derived from modelling of thermal behaviour of LED board, see previous chapter). Figure 2.38 shows schematic model of newly developed bending test and Figure 2.39 realization of bending test assembly. The equipment consists of electromagnetic shaker, lever that increase force acting on LED board and strain gauge load cell measuring value of applied force. The failure detection system is based on electrical conductivity measurement (see Chapter 2.6.5.1).

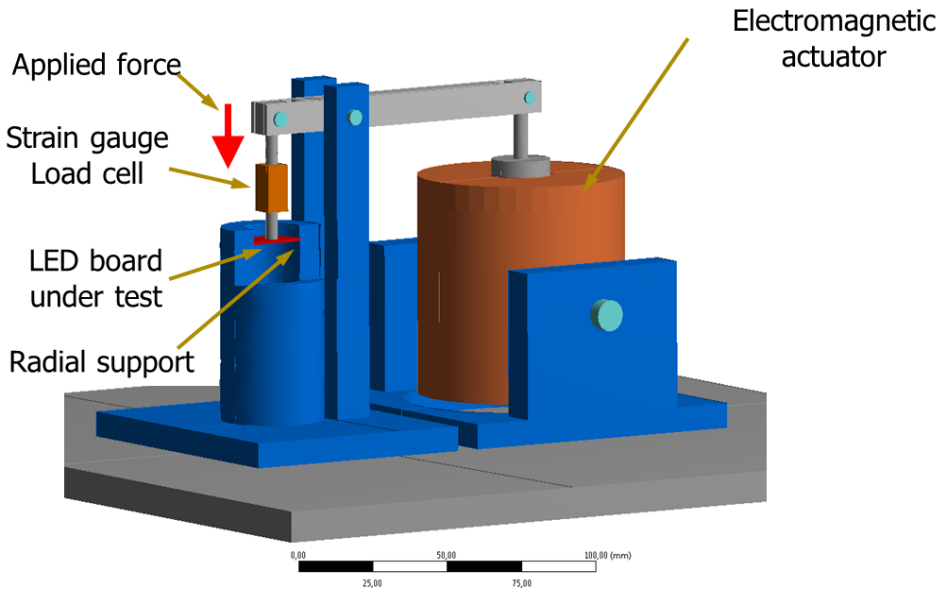


Figure 2.38: Schematic model of newly developed bending test

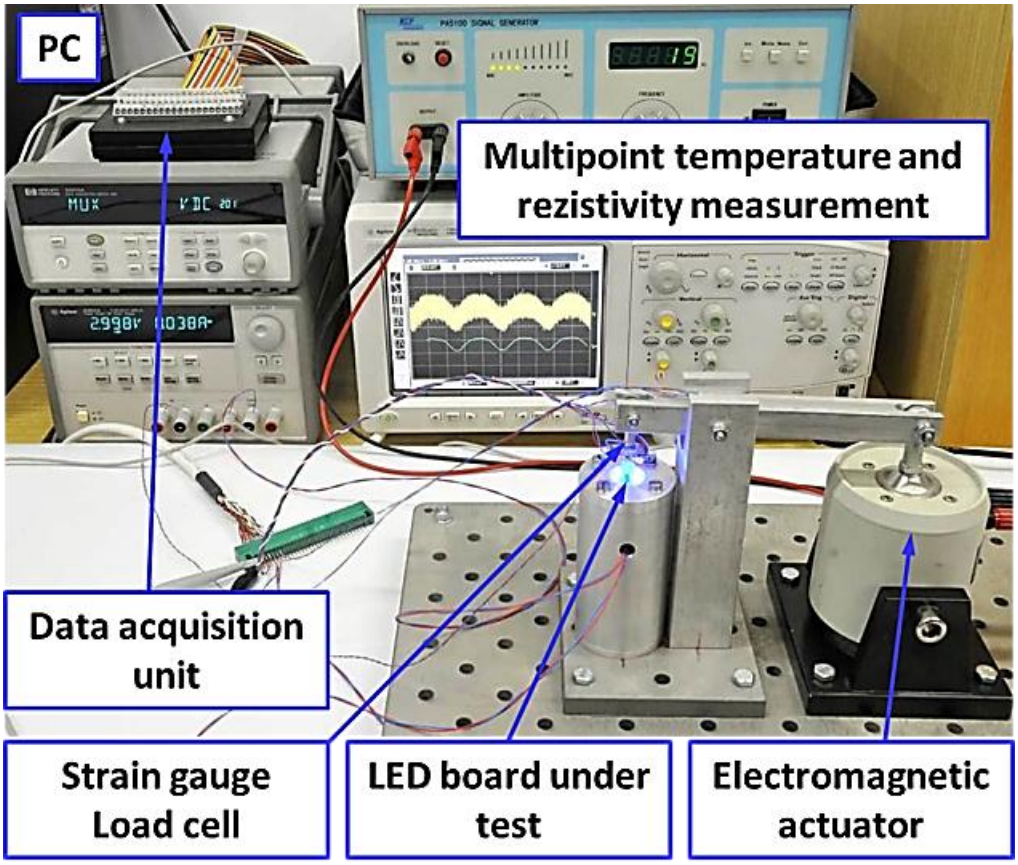


Figure 2.39: Bending test assembly for LED board life time validation[21]

The applied force has been measured by strain gauges mounted on a (mechanically stretched) beam with known cross-section area and Young modulus (Figure 2.40 and Figure 2.41).

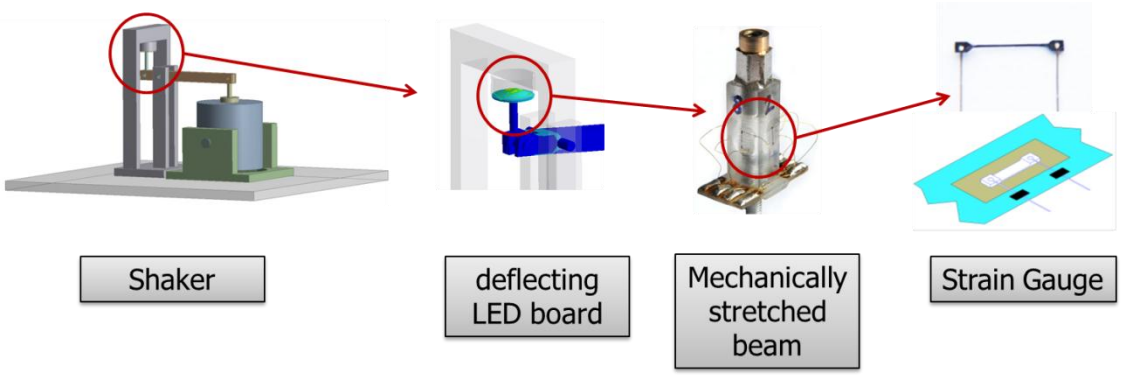


Figure 2.40: Construction of load cell for force measurement

[21] Assembly was made by my PhD student Jan Formanek

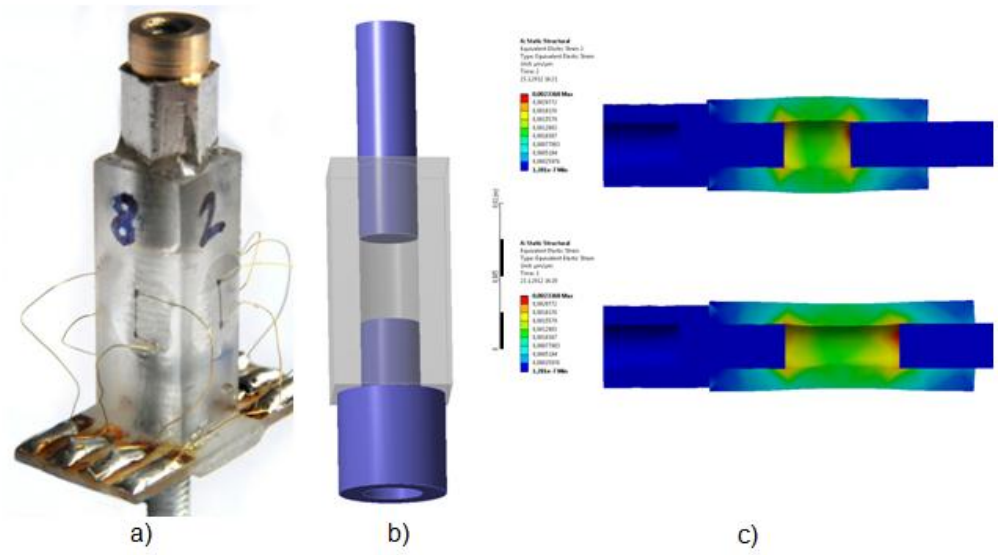


Figure 2.41: a) Realized deflecting beam with strain gauges, b) the model for simulation, c) mechanical strain numerical simulation

The applied force measured by strain gauges is proportional to strain ε, the Young modulus E and the cross-section area S of the beam:

$$F = E.\varepsilon.S \tag{2.34}$$

Plexiglas (S = 28.9 mm^2) has been chosen as deflecting beam. The Young modulus of Plexiglas is 1.949 GPa. The strain is measured by strain gauges applied on all four sides of deflection beam (Figure 2.41).

The dependence of resistance to deformation of used strain gauge is described by formula:

$$R_{\varepsilon,25} = R_{0,25}.(1 + C_1.\varepsilon + C_2.\varepsilon^2) \tag{2.35}$$

C1 and C2 are the linear coefficient of deformation rate and the quadratic coefficient of deformation rate respectively, $R_{0,25}$ is the electrical resistance of the unstressed gauge (without support) at 25°C and $R_{s,25}$ is the electrical resistance of the deformed free gauge at 25°C. Coefficients C1, C2 $R_{0,25}$ are determined experimentally by manufacturer.

Rewriting equation (2.35) we can get the strain:

$$\varepsilon = \frac{-C_1 R_{0.25} \pm \sqrt{(C_1 R_{0.25})^2 - 4.C_2 R_{0.25}.(R_{0.25} - R_{\varepsilon.25})}}{2.C_2 R_{0.25}} \tag{2.36}$$

The unknown variable $R_{s,25}$ is measured using the Wheatstone bridge method (Figure 2.42). For the measured voltage can be written:

$$V = V_{cc}.\left(\frac{R_3}{R_3 - R_1}\right) - \left(\frac{R_2}{R_{\varepsilon,25} - R_2}\right) \tag{2.37}$$

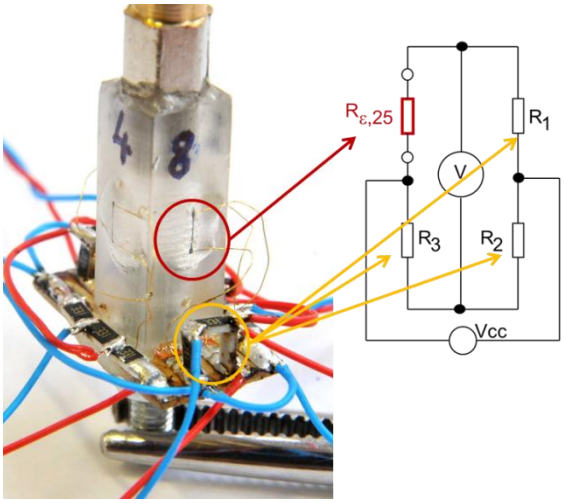


Figure 2.42: Strain gauge implemented on bridge a) realization b) schematics

And the resistance of mechanically stressed strain gauge becomes:

$$R_{\varepsilon,25} = \frac{R_2}{\frac{R_3}{R_3+R_1}\frac{V}{V_{cc}}} - R_2 \qquad (2.38)$$

Finally we have all unknown quantities and we can use equation (2.34) to calculate acting force.

2.6.5 Failure detection

Cracks and fatigue in conductive materials applied within the LED board can be characterized by electrical resistance measurement. Changes in resistance can indicate an interconnect-related failure. Thermal resistance measurement can be used to characterize isolating materials parts, and changes to detect thermal resistance degradation.

2.6.5.1 Electrical characterization of interconnect-related failure mechanisms

Interconnect related failure is caused by thermo-mechanical stress (different thermal expansion of materials). Thermal stress caused by thermal expansion can result initiation of crack that can propagate further during thermal and mechanical cycling. These cracks can be characterized by electrical resistance measurement. Cracks propagation changes active wire or solder joint cross-section, which leads to increase of resistance.

Figure 2.43 shows an electrical equivalent circuit of Master LED board interconnection. Interconnect-related failure can be detected by measurement of the resistances.

The proposed characterization procedure begins with initial measurement of selected resistances before cycling process. After this initial procedure mechanical force is applied on the LED board by the shaker. The resistance is measured again after each cycle in three different LED board deflections. First for the low temperature equivalent force, secondly for room temperature (no applied force) and last for the high temperature equivalent force

(operational temperature of LEDs). This is important because cracks can open and close depending on actual LED board deflection.

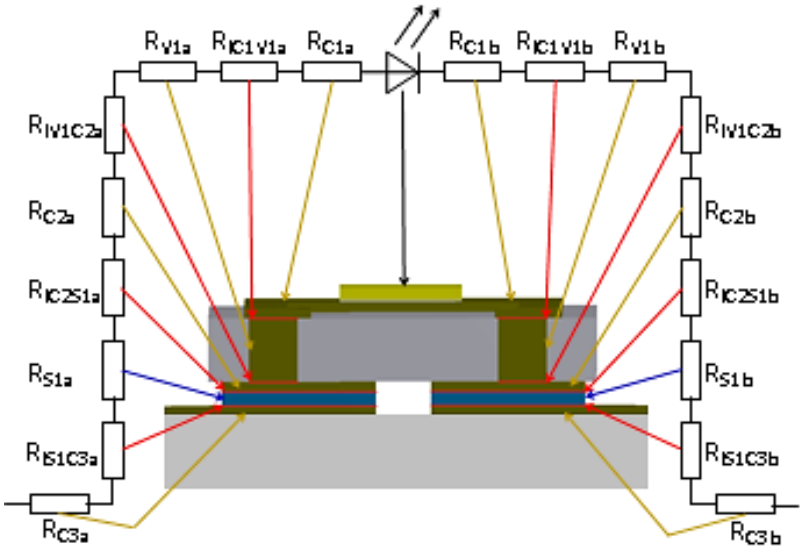


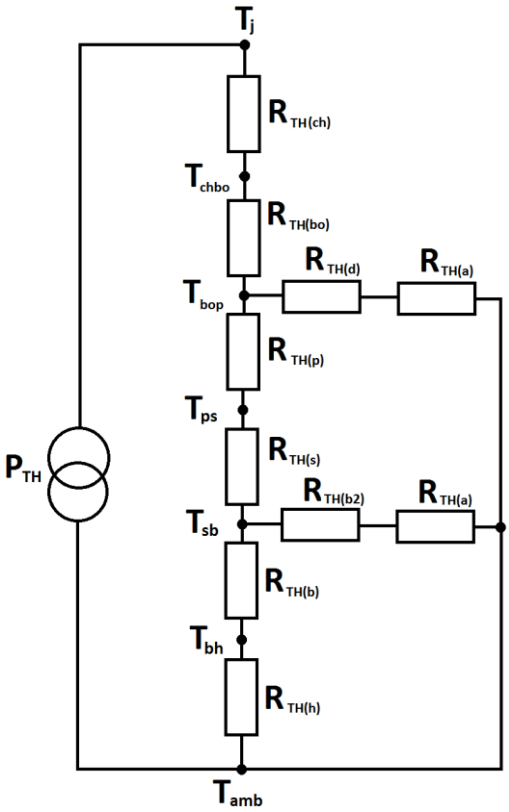
Figure 2.43: Electrical equivalent circuit of Master LED board.

Rc1a *– Electrical resistance of top Cu layer of LED package*
RIc1v1a *– Electrical resistance of interface between top Cu layer of LED package and LED package via*
Rv1a *– Electrical resistance of via of LED package*
RIv1c2a *– Electrical resistance of interface between bottom Cu layer of LED package and LED package via*
Rc2a *– Electrical resistance of bottom Cu layer of LED package*
RIc2s1a *– Electrical resistance of interface between bottom Cu layer of LED package and LED board via*
Rv1a *– Electrical resistance of LED board via*
RIs1c3a *– Electrical resistance of interface between bottom Cu layer of LED board and LED board via*
Rc2a *– Electrical resistance of bottom Cu layer of LED board*

During characterization process the total resistance is measured by detecting a voltage drop when all six LEDs are supplied from reference current source. When an increase of resistance is detected, all indicated resistances are measured to detect the location of the crack. Here it must be noted that the interface resistance between a particular via and the Cu metallization is not measurable because separate vias are not accessible for resistance measurements. Only total resistance of via and top and bottom resistance is detected.

2.6.5.2 Thermal characterization of thermal resistance degradation

Electrical characterization is suitable only for electrically conductive materials. It cannot be used for electrically nonconductive materials. The cracks propagation in non-conductive materials (in LED package ceramics and FR4 epoxy) can be detected by measurement of the change of thermal resistance. A thermal equivalent model of the Master LED board is shown in Figure 2.44. Another method is to use CT scanner.

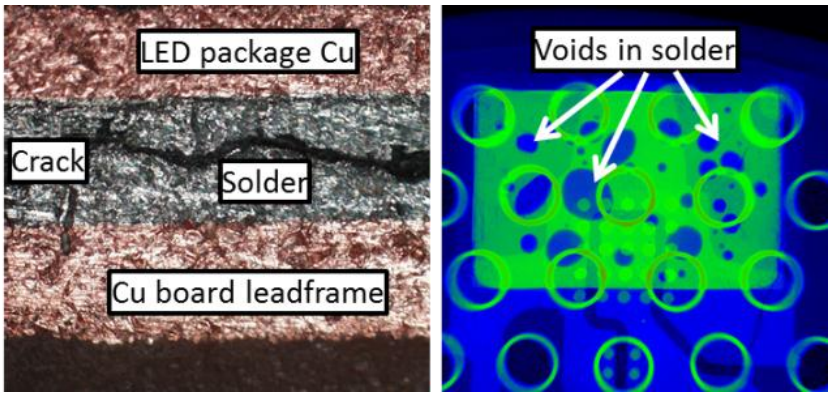


P_{TH} is the power dissipated by the device
T_J is the junction temperature in LED diode
T_{chbo} is surface temperature where the LED chip is attached to the LED chip bonding material
T_{bop} is surface temperature where the LED chip bonding material is attached to the LED package
T_{ps} is surface temperature where the LED package is attached to the solder pads
T_{sb} is surface temperature where the solder pads is attached to the LED board
T_{bh} is surface temperature where the LED board is attached to the heat sink and other components of Light bulb
T_{amb} is the ambient temperature
$R_{TH(ch)}$ is the thermal resistance of the LED chip
$R_{TH(bo)}$ is the thermal resistance of the LED chip bonding material
$R_{TH(d)}$ is the thermal resistance of the transparent LED dop
$R_{TH(p)}$ is the thermal resistance of the LED package
$R_{TH(s)}$ is the thermal resistance of solder pads
$R_{TH(b)}$, $R_{TH(b2)}$ is the thermal resistances of LED board
$R_{TH(h)}$ is the thermal resistance of heat sink and other components of Light bulb
$R_{TH(a)}$ is the thermal resistance of air

Figure 2.44: Master LED board thermal resistance equivalent circuit

2.6.6 Measurement results

Validation results performed on two LED boards (more LED boards will be measured in the future) show the weakest point is located in solder joint between LED package and FR4 board. The mechanical fatigue life was 86 500 and 97 800 respectively. Simulated life time value has a 2.07 and 1.83 times longer life (178 912). Figure 2.45a shows the optical microphotograph of the crack in the solder joint between electrical pad and FR4 board. X ray photography of mechanical pad solder joint shows a fact that during soldering process many voids appears (Figure 2.45b). This could explain differences between simulation and validation results. Voids can initiate cracks a bit earlier due to bigger local mechanical stress around the void and failure can appear sooner [1].



a) b)

Figure 2.45: a) Optical micrograph showing the crack in the solder joint. b) X-ray photograph of thermal pad showing voids in solder [1]

Life time tests have been proved on two LED board for applied force 15 N. However more tests for different applied force are needed to get statistical data in the future. Another very important aspect is to simulate and validate slow bending test where creep effect play a dominant role (Chapter 2.6.9).

2.6.7 Different LED board technologies life time comparison

An accurate 3-D modelling of several LED board technologies mainly focusing on thermal, thermo-mechanical evaluation and lifetime prediction to compare their performances was performed. This chapter discusses the advantages of these new LED board technologies from their lifetime and reliability limits (see models on Figure 2.25). Thermal stress has been inspected on all LED boards considering the widest temperature working range according to standards (-40 to +125^{o}C). Thermo-mechanical and lifetime analysis have been performed to study reliability and lifetime limits of each board technology, using thermal boundary conditions extracted from the thermal simulation of a whole LED lamp. Additionally, thermal stress cycles that lead to the LED board failure due to thermal fatigue have been calculated. Elastic-plastic analysis with temperature dependent stress-strain material properties has been performed [3].

Figure 2.28 shows the calculated residual stress distribution in LED boards. Figure 2.29 shows the comparison of calculated maximum residual stresses of all LED boards. The most problematic part can be found in reference LED package metallic vias that connect bottom contact of the package and top LED package metallization. Second problematic part is found at solder joints which connect LED package with LED board electrical routing.

Figure 2.46 shows the calculated lifetime distribution in detail for the place where LED package is soldered on the LED board. Some parts (LED package ceramic, FR4 and insulation layer) are intentionally hidden to view the most interesting parts: the electrical and thermal pads of LED package, soldering layer, metallization vias through ceramic LED package, LED chip and LED chip bounding layer. Simulation results show that the most critical parts are LED vias and solder joints [3].

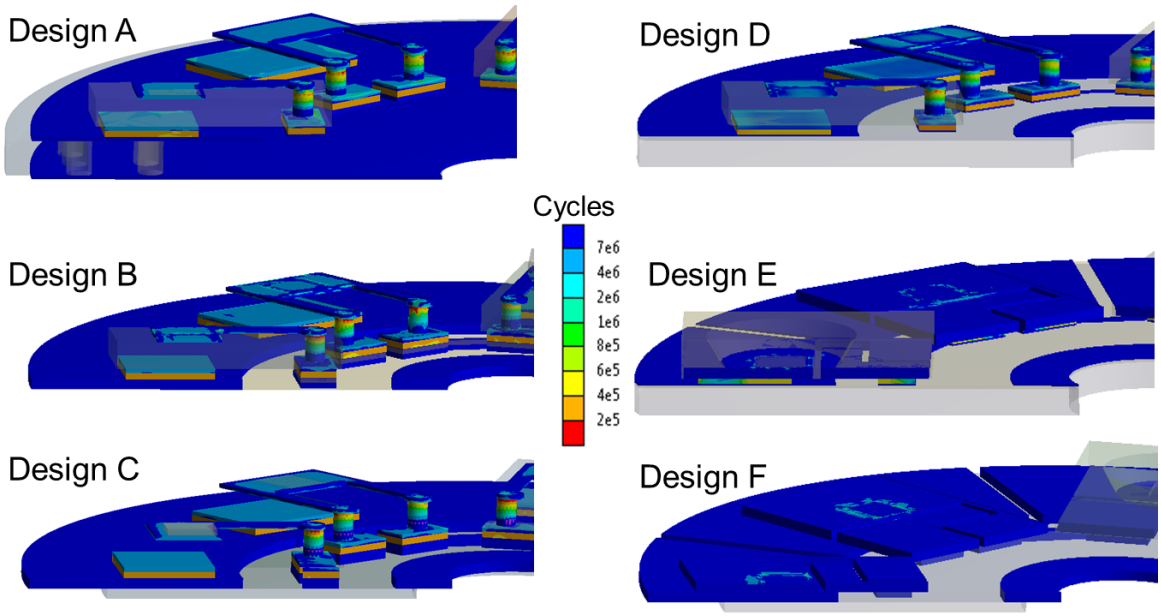


Figure 2.46: Distribution of calculated life time in the place where LED package is soldered

Figure 2.47 shows the comparison of the lifetime calculated for each LED board. The most problematic part can be found in the metallic vias of the reference LED package that connect bottom contact of the package and top LED package metallization (Design A: 96 624 cycles – Design D: 164 640 cycles). Longer lifetime has been calculated for the new LF package (Design E: 796 600 cycles and Design F: 584 740 cycles). Second problematic part is found at solder joints which connect LED package with LED board electrical routing. The worst performance has been observed for Design D (IMS board) 170 414 cycles. The best performance has been obtained for Design E (248 453 cycles) [3].

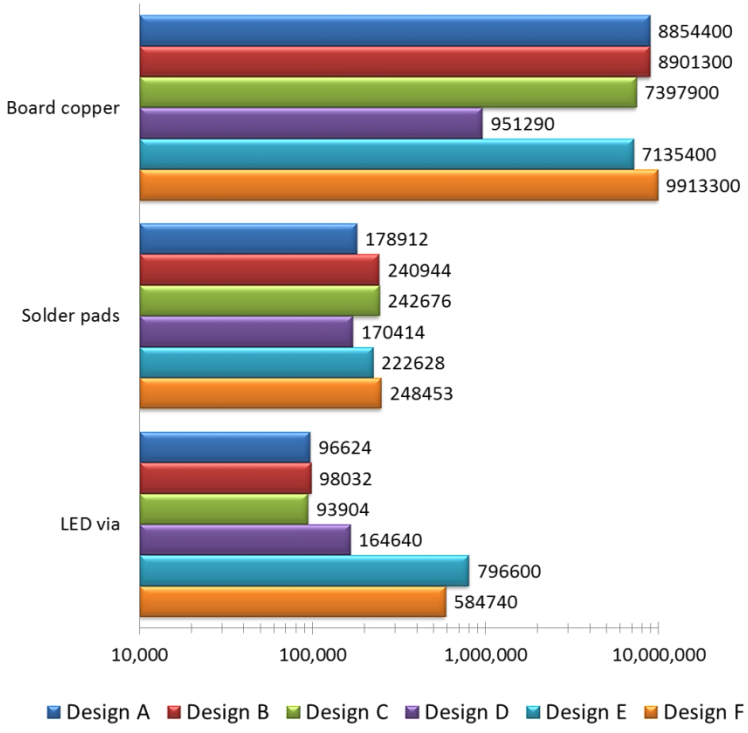


Figure 2.47: Calculated life time comparison [3]

2.6.8 LED board life time calculation - low speed mechanical cycling including creep effect

Many electronic devices works under thermal cycling through two temperature extremes, that is typically at relatively high rates of change. LED board temperature changes from room temperature (when SSL lamp is switched on) to operational temperature which is typically around 90°C and back to room temperature (when SSL lamp is switched off). These thermal cycles cause a high thermal stresses imposed in LED board materials. Ability to withstand cyclical exposures to these temperature extremes are usually tested by temperature cycle test. Temperature cycling test determines the ability of LED board to resist extremely low and extremely high temperatures at cyclical exposure to these temperature extremes. Failure mechanisms accelerated by temperature cycling typically cause die cracking, solder joint and package cracking, wire breaks and bond lifting. However, main disadvantage of temperature cycling tests is long time of testing. One temperature cycle (temperature range -40 °C to +120 °C) typically takes one hour and number of cycles needed to device failure is in the order of thousands of cycles.

Our new testing method can dramatically speed up testing process keeping testing accuracy in the range of 20%.

Imposing mechanical loads cyclically to a device under test might mimic thermal stresses. Mechanical cycling can be applied at much higher frequency, which on the other hand must be slow enough to take into account material relaxing effects and creep. When cycling is applied at too high a frequency, a possible effect of creep will be vanished but if mechanical bending of the board under the test is slow enough, the creep effect become dominant. The frequency, where creep plays dominant role can be calculated by expressing and comparing accumulated creep strain and accumulated elastic and plastic strain for given material. If accumulated creep strain rate at given mechanical loading frequency is much higher than accumulated plastic strain and/or elastic strain rate, then the creep effect is dominant. The same rule can applied when power cycling or thermal cycling is used. It is well documented that creep plays an important role at slow mechanical bending, especially in materials where homologous temperature (ratio of operating and melting temperature) is above 0.5 [53]. This is true almost for every soldering material used in electronic assembly. The melting point of SAC305 (used in tested LED boards) is typically observed as 217 °C. This means that the homologous temperature is about 0.47 to 0.81 for temperature range -40 °C to +120 °C. Because measured and simulated dynamical thermal constant of the SSL lamp is more than 30 min (see chapter 2.3.3), the thermal cycling of LED board is very slow. Solder joints are expected to deform primarily due to creep effect.

To calculate number of cycles to failure N_f, we use the Syed model is most suitable for SSL LED board life time prediction (explanation is given in chapter 2.6.3). The only unknown parameter in equation (2.27) is value of accumulated creep strain.

The creep rate deformation is a function of the material properties, time, temperature and the applied structural load and is described by creep strain rate function (Figure 2.48). Three main regions can be found on creep strain rate function. In the first region (I), the primary

creep forms. The strain rate is high and slows with increasing time because of material hardening. In the second region (II) the strain rate reaches a minimum and becomes almost constant. This is caused because of the sense of balance between hardening and annealing effect. Most models typically refer to the creep rate in first and second region. In tertiary region (III), the strain rate exponentially increases with stress and ends in rupture (at time t_r with a fracture strain ε_f).

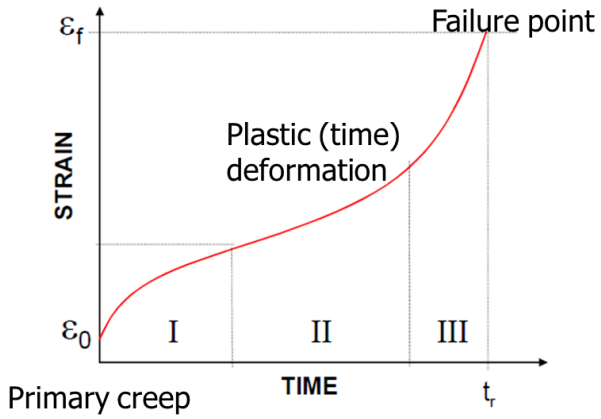


Figure 2.48: Creep strain rate as a function of time due to constant stress

Creep strain rate is usually described by creep constitutive equation. Most of the constitutive equations are obtained by means of the generalization of the simple and classic time and strain hardening laws. A wide range of creep model equations are in use today. Many of these equations include behaviour which represents of primary, secondary, and/or tertiary creep deformations. The proper selection a constitutive equation is a major task in description of creep behaviour. This can be completed by associating of experimental data with the selected creep strains constitutive equation.

Two most important and widely used constitutive model equations are Norton- Power Law (or double power law) and Hyperbolic sine function model (Chapter 2.6.3).

Wiese at al. [72] published constants for double power law constitutive model for PCB and Flip Chip solder joints of SAC 405. Constitutive equation for double power law can be written as:

$$\varepsilon_{cr} = A_1 \left(\frac{\sigma}{\sigma_n}\right)^{n1} exp\left(\frac{-H_1}{kT}\right) + A_2 \left(\frac{\sigma}{\sigma_n}\right)^{n2} exp\left(\frac{-H_2}{kT}\right) \qquad (2.39)$$

where ε_{cr} is an equivalent creep strain, σ is equivalent stress, T is temperature (absolute), k is Boltzman constant, A_1 , H_1, n_1 and A_2 , H_2, n_2 are constants defined by the measurement. Constants published in [72] are following:

double power law model parameters for SAC 305 solder joints					
A_1	H_1/k	n_1	A_2	H_2/k	n_2
0.4 μs^{-1}	3223	3.0	1 ps^{-1}	7348	12

Constants for Hyperbolic sine function constitutive model has been published Schubert at al [62]. Material data were collected for different solder composites (SAC 305, SAC 307 and SAC 3075) from different sources. The model covers two regions for stress-strain rate. The equation for hyperbolic sine function constitutive model is:

$$\varepsilon_{cr} = A_1 \left[\sinh(\alpha.\sigma)\right]^n exp\left(\frac{-H_1}{kT}\right) \qquad (2.40)$$

where ε_{cr} is an equivalent creep strain, σ is equivalent stress, T is temperature (absolute), k is Boltzman constant, α, n and H_1 are constants defined by the measurement. Constants published in [62] are following:

Hyperbolic sine function constitutive model parameters for SAC 305 solder joints					
A_1	α	n	H_1/k	E (MPa)	CTE
277984 s^{-1}	0.02447 MPa^{-1}	6.41	6500	61251 – 58.5T(K)	20 ppm/K

The above constitutive models and constants has been used in FEM modelling of solder joint life time of the SSL LED boards.

A stress-strain analysis of the LED board (model in Figure 2.49) was calculated taking into account nonlinear thermal dependent elastic-plastic material behaviour. The analysis must be calculated in time domain taking into account creep constitutive model for SnAgCu solder. Because these calculation is very time intensive, the models of LED board was slightly simplified to reduce the number of nodes and 1/4 model has been used.

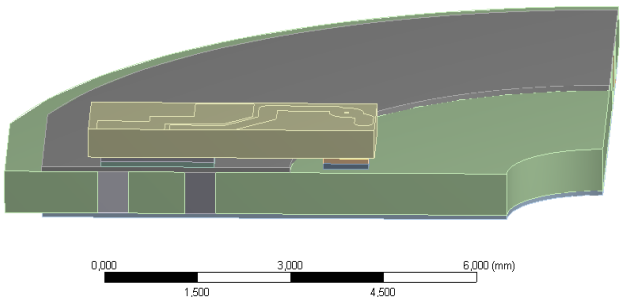


Figure 2.49: simplified 1/4 model to reduce the number of nodes

Thermo-mechanical boundary condition for FEM simulation is following: all inner face vertex of the FEM model mesh of the central mounting hole is mechanically fixed, since a central screw attaches this point to the thermal cone. All other nodes of the model are mechanically free and can move in all directions. A temperature profile (as depicted on Figure 2.50) has been applied on all parts of the LED board model. Thermal cycling simulation temperature starts at temperature 180 °C which is considered as zero stress temperature for SAC 305 (the melting point of SAC305 is typically observed as 217 °C, but thermo-mechanical stresses start to form at lower temperature). Then periodical thermal cycling is applied with period 480 s where rump time 60 s was set up. Period time was set shorter then thermal constant of SSL lamp (chapter 2.3.3) to speed up simulation. The period shod be long enough to make creep effect dominant.

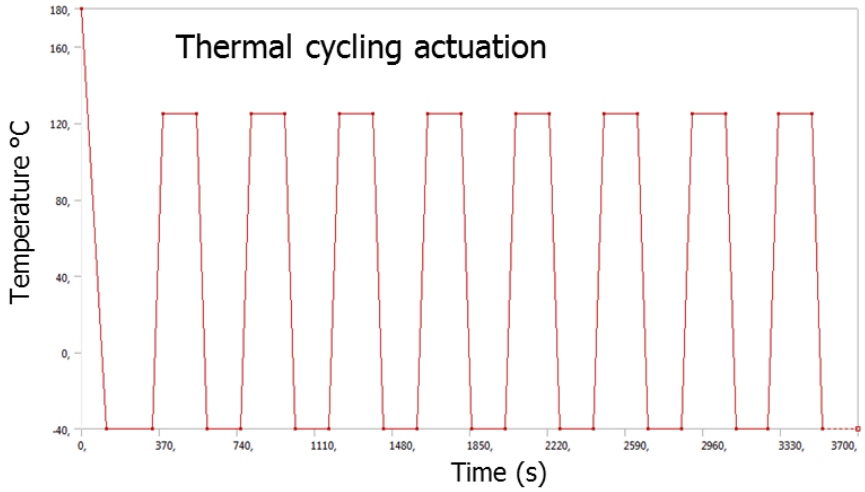


Figure 2.50: Applied temperature profile

The analysis computes residual stresses distribution based on elastic-plastic nonlinear approach at each time increment for whole LED board model. Then creep strain is calculated using double power law or hyperbolic sine constitutive model. The value of accumulated creep strain can be calculated as a difference of creep value at given point in one thermal cycle. Figure 2.51 shows creep strain distribution in electrical solder join (solder joint between FR4 LED board top copper and bottom side of electrical pad of the LED package) after five and six cycles. Green line represents maximal value and red line minimal value of the creep strain. The value of accumulated creep strain can be identified in all mesh points of the model by post-processing script.

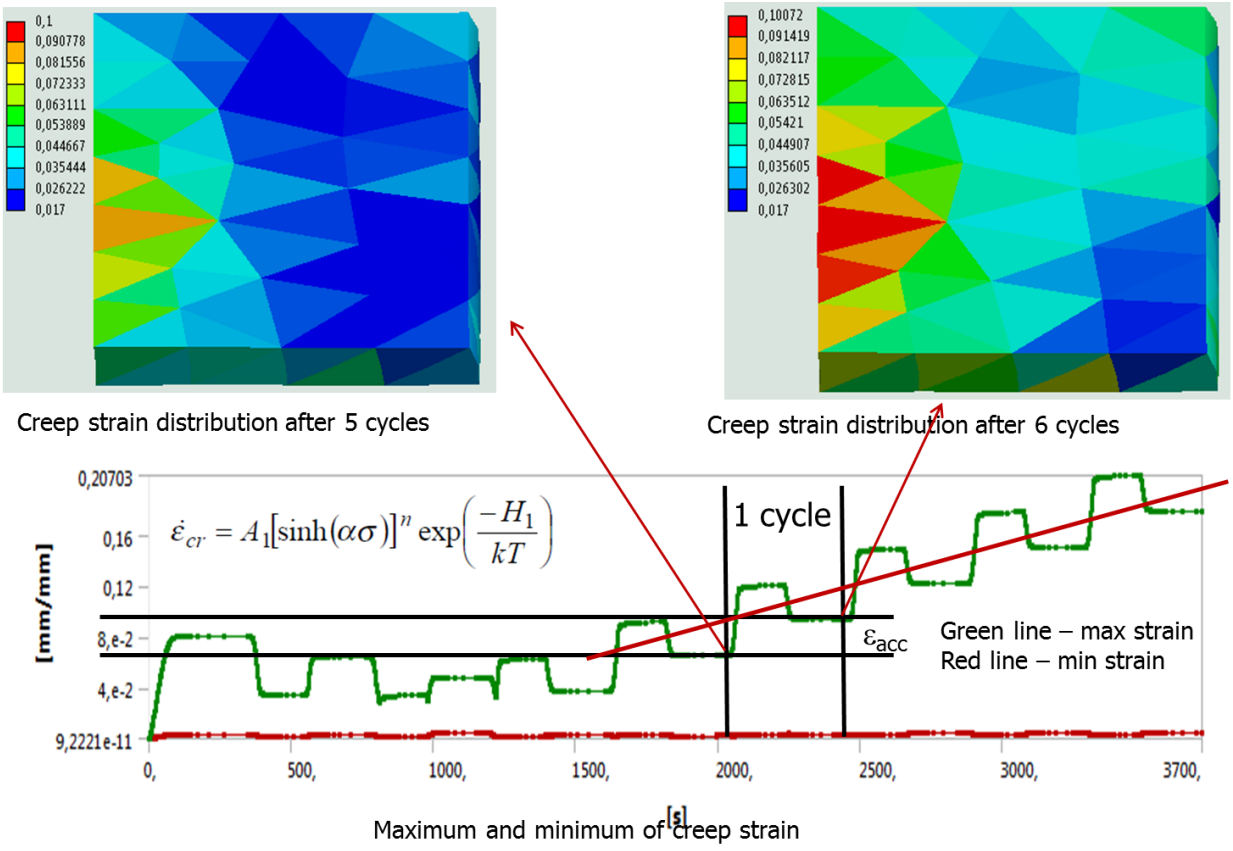


Figure 2.51: Determination of equivalent accumulated Creep strain rate in electrical solder joint

Equation (2.29) that uses total accumulated strain has been used for number of cycles to failure calculation. By post-processing script distribution of number of cycles to failure can be obtained. Figure 2.52 shows the distribution of number of cycles to failure in electrical solder join. Minimum value of cycles (788) is located in red area. Possible crack will be probably initiated in this area. Maximal number of cycles (8799) is located on bottom right corner. Note: this simulation is not capable to perform dividing of the mesh and simulation of crack propagation is not possible to observe here. This is very interesting research topic for the future.

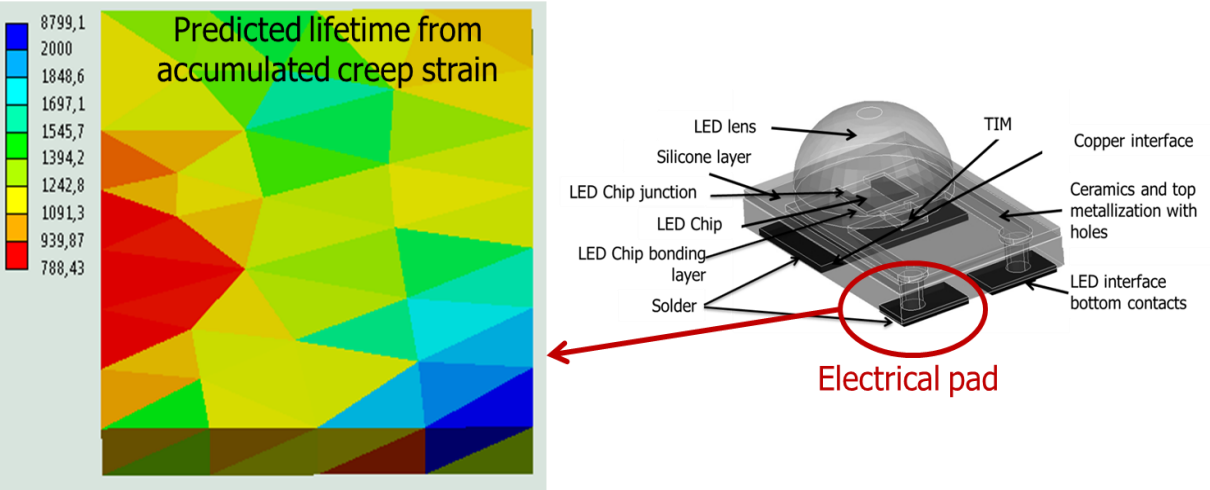


Figure 2.52: Distribution of number of cycles to failure in electrical solder

It could be possible to replace thermal cycling test that is very slow by much faster mechanical bending test. Mechanical actuation force that creates LED board bending must be identified. The force magnitude must results the same value of accumulating creep strain in solder joint as in case of thermal cycling. If the thermal cycling accumulated strain value will be consistent with mechanical cycling accumulated strain, then also number of cycles to failure must be the same.

Figure 2.53 shows creep strain rate comparison for thermal (-40 °C to 120 °C) and mechanical cycling for actuation force +80 to -80 N at temperature 70 °C. Here the value of accumulated creep strain is almost identical. The higher temperature for mechanical actuation has been chosen, because creep rate is higher at high temperature and then the actuation force is lower.

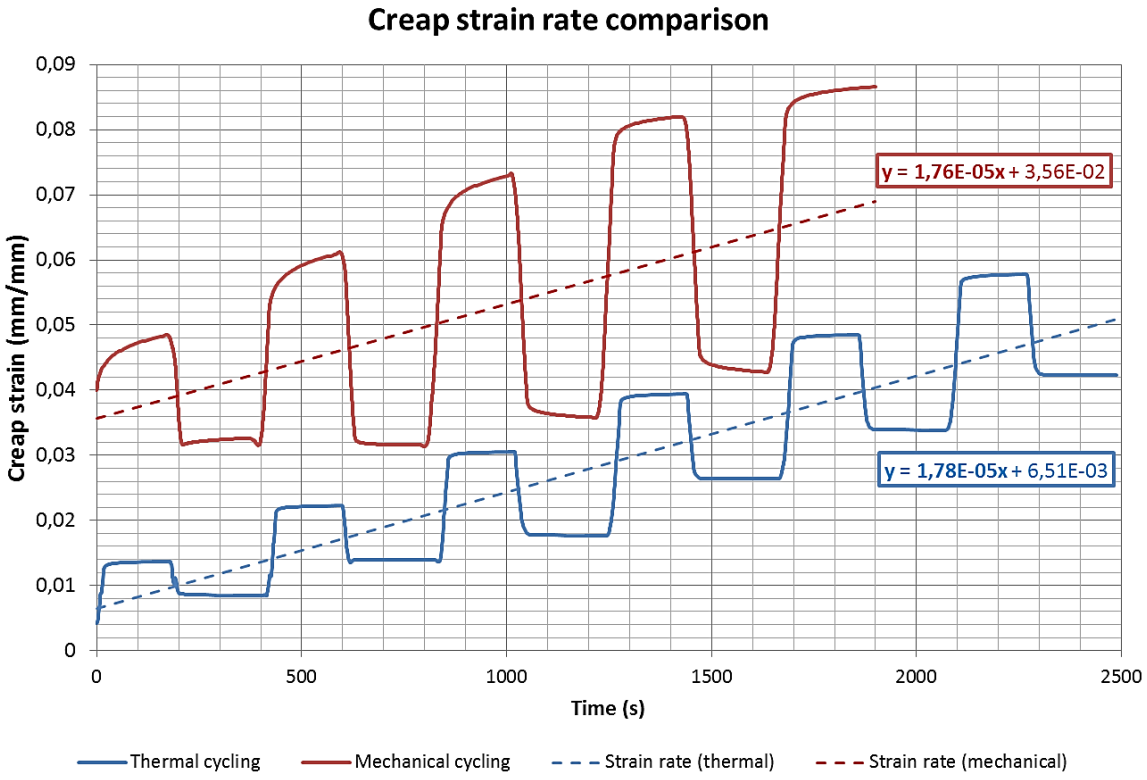


Figure 2.53: Distribution of number of cycles to failure in electrical solder

2.6.9 Low speed mechanical cycling measurement

Electromagnetic actuator used for high speed cycling test is limited by low frequency range which is 10 Hz. In the low speed mechanical loading testing system we need frequency range 1 – 0.001 Hz. Figure 2.54 shows designed pneumatic loading system that is able to mechanically deflect LED boards by applied force in the range 0 – 150 N and frequency 3 – 1.10^{-4} Hz. Another advantage of proposed system is controlling of ramp time that can be adjusted by flow control valve. This is especially important while we want to emulate thermal cycling test, which has usually ram time in order of minutes.

The testing apparatuses shown on Figure 2.54 consists LED board under test holder that mechanically fix LED board on outer side by radial support which fixes LED board only in direction of actuating force. Actuated mechanical force is transmitted from compact pneumatic cylinder through load cell to the shaft that is mounted on central hole of LED board. The direction of applied force is controlled by control valve and blow off silencer. The vale is then controlled directly by pressure control valve. Measurement setup with pneumatic actuation is shown on Figure 2.55.

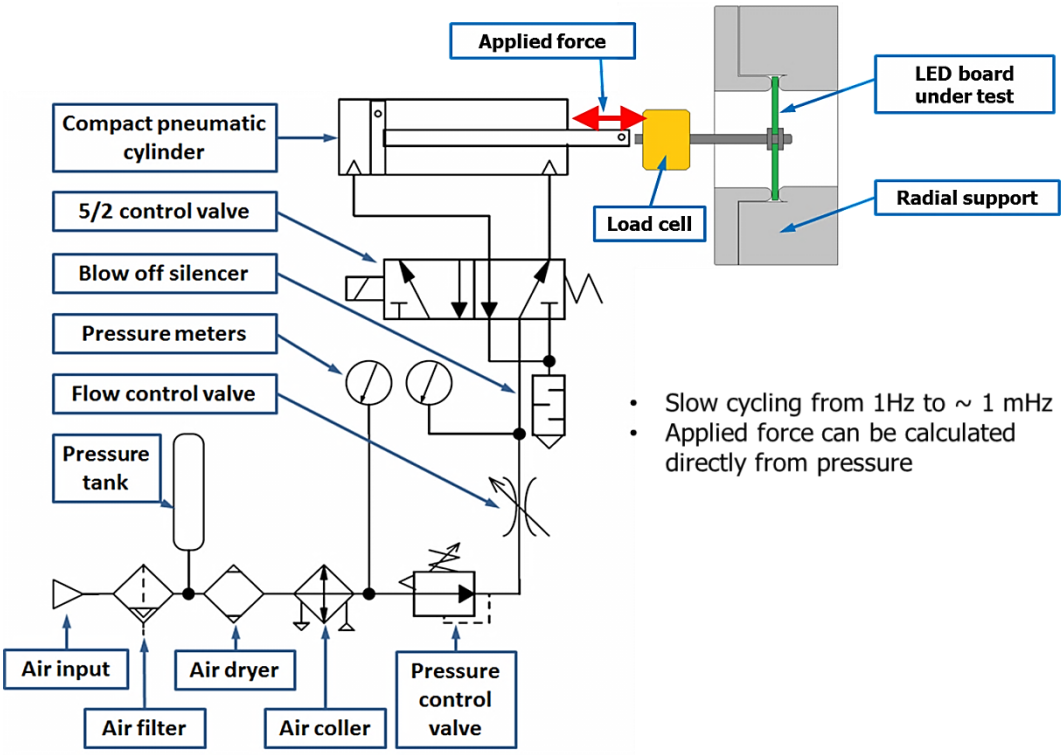


Figure 2.54: Schematic view of pneumatic shaker system.

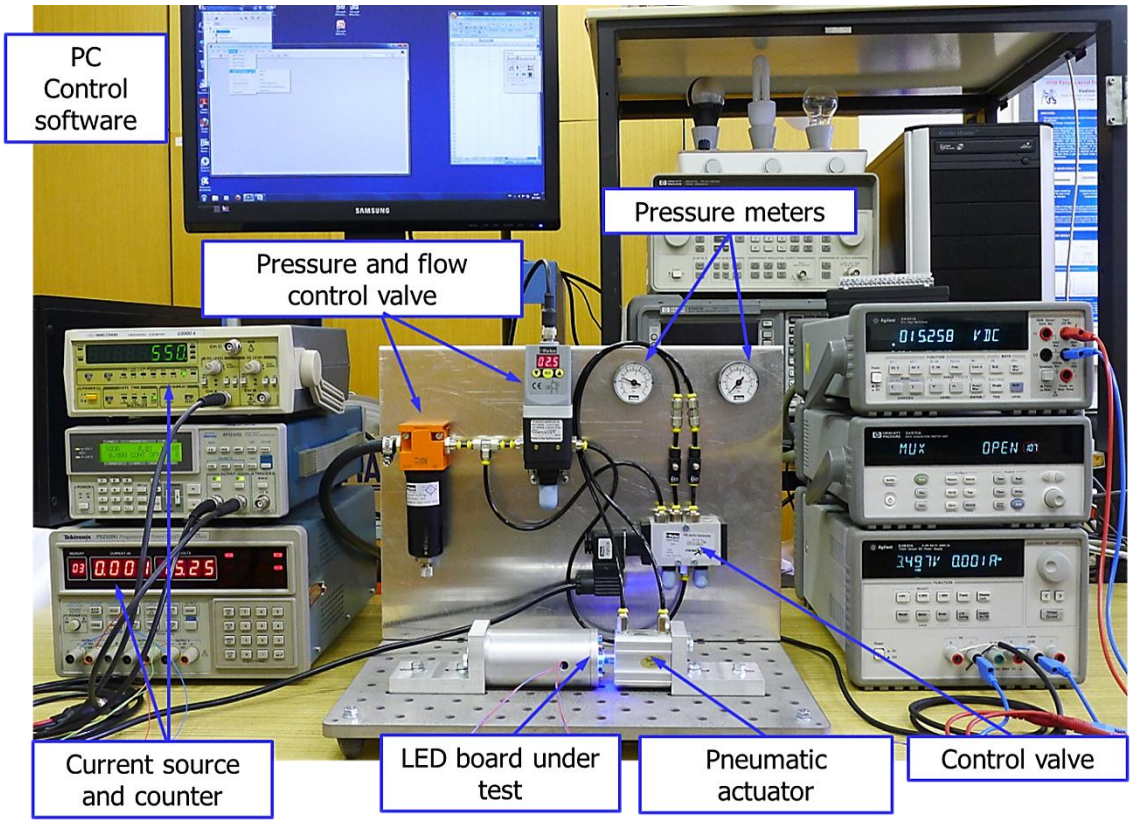


Figure 2.55: Measurement setup with pneumatic actuation[22]

[22] Measurement setup was constructed by my PhD student Jan Formanek

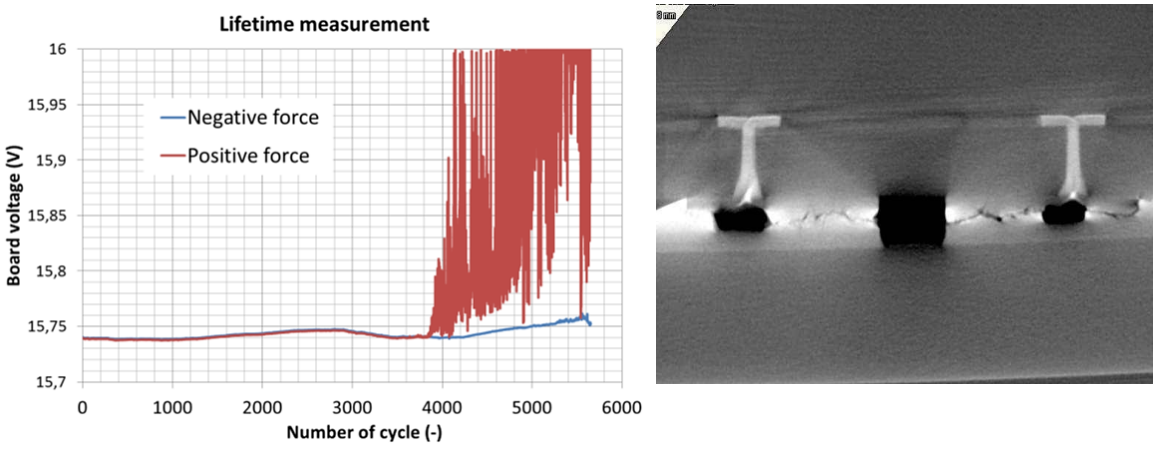
2.6.9.1 Measurement results

The characterization procedure begins with initial measurement of voltage drop on six LEDs before the cycling process. After the initial procedure the mechanical force is applied on the LED board by the pneumatic actuation system. The voltage drop is measured over again each cycle at positive and negative LED board deflection. This is important because cracks can open and close depending on actual LED board deflection.

Figure 2.56a shows the voltage drop measured on six LEDs. It can be clearly identified that after 3870 cycles a crack appears on electrical contact of the LED package. Disadvantage of this crack detection method is inability of location of the solder joint where the crack appears. This disadvantage will be solved in future by measuring of electrical resistance on each solder joint

Figure 2.56b shows the crack in solder joint detected by CT.

At the time of submission of this work only one sample was measured. Unfortunately we have no statistical data which is need for proper evaluation of measured data. These measurements are ongoing. Another aspect that should be noted here is that only one measurement setup was performed with one actuation frequency and one actuation force. Ongoing measurements will be performed at different frequencies and actuation forces.



a) b)

Figure 2.56: a) Voltage drop measured on six LEDs, b) Crack in solder joint (CT detection)

2.7 Summary and conclusions

This chapter presents results achieved with the design of new 806 lumen SSL retrofit lamp that should be an alternative replacement of current 400 lumen master LED glow lamp. My own research contribution can has been summarized in chapter 2.1. The chapter collets published (see Table 2-1) and new unpublished scientific results that was mainly summarised in chapter 2.6.

The work that has been done can be summarised by following conclusions:

- *Thermal performance of an 8 W LED Lamp was analysed by two independent simulation tools (Coventor and Ansys) and validated by thermal measurement. Acquired results are in good agreement; however, improvement of the simulation model and prescribed heat generation will results in a better prediction of the measured temperatures. The simulated LED temperature was 90°C for the Coventor simulation and 86°C for the ANSYS simulation; a temperature of 91°C was measured on the board close to the LED die. Results were published in [5] and [2]*
- *Critical parts has been determined for new higher power LED lamp design (LED board and LED driver)*
- *Five new of LED boards designs including two different LED packages have been compared to an existing LED board of a 40 W equivalent LED lamp from thermal, mechanical and lifetime point of view. All new concepts have been improved from thermal point of view. The lowest LED chip temperature has been achieved with the Design F (new LED board concept 3 with the new LED package) with almost five degrees lower temperature then Design A (Reference model). Results were published in [3]*
- *LED package and LED board thermal resistance has been calculated and compared for all newly designed boards. Results were published in [56]*
- *Comparison of calculated residual stress distribution and life time simulation for all models has been realised. The most problematic part can be found in LED package metallic vias together with solder joints which connects LED package with LED board. Results were published in [3] and [2]*
- *The lifetime model, life time boundary conditions and S-N curve material properties has been be verified by actual lifetime tests. Results were published in [3]*
- *Validation results performed on two reference RF4 LED boards show the weakest point is located in solder joint between LED package and FR4 board. The mechanical fatigue life was 86 500 and 97 800 respectively. Simulated life time value has a 2.07 and 1.83 times longer life (178 912). Differences between simulation and validation results can be explained by voids in solder joints. Life time tests have been proved on two LED board for*

applied force 15 N. However more tests for different applied force are needed to get statistical data in the future. Results were published in [1]

- *New accelerated characterization methods for SSL LED boards solder joint have been developed. The method includes creep effect into account. Theoretical calculation of solder joint life time is in good agreement with lifetime measured on real sample. However, more samples has to be measured to get some statistical data. These very promising results were not published yet.*
- *New accelerated validation method of LED boards can replace traditional thermal cycling test.*

2.7.1 Future work:

New accelerated characterization methods for SSL LED boards seem to be very promising. However, more work has to be carried out to measure more LED board samples not only of existing reference RF4 board, but also on newly designed LED boards. Moreover, it would be very interesting to find a relationship between mechanical cycling frequency, applied force and traditional thermal cycling that is given by accumulated creep strain in solder joints.

3 GaN, GaAs and Silicon based Micromechanical Free Standing Hot Plates for Gas Sensors

Main objective of the presented work deals with design, modelling and characterization of new micro machined GaAs and GaN based hot plate thermal converters, which are considered to operate with high temperature metal oxide gas sensors, that can analyse various gases, such as CO, H2, NOx and hydrocarbons.

3.1 Motivation and author contribution

Typical micromachined hotplates are based on thin membranes made of silicon nitride and silicon oxide. However, the operating temperature of these hotplates is limited to a maximum of about 350°C.

High sensitivity and low power consumption are expected for present metal oxide Gas sensors, which generally works in high temperature mode that is essential for chemical reactions to be performed between molecules of the specified gas and the surface of sensing material. Because of a low power consumption is required, even for operation temperatures in the range of 200 to 500 °C, high thermal isolation of these devices are necessary. The thermal and mechanical properties of GaAs and GaN based hot plates are compared with Silicon based hot plate. A new GaN based suspended membrane-type hot plate MEMS processing technology was developed for operating temperature range up to 1000°C. The processing technology is also well-suited with the GaAs and GaN MESFET or HEMT devices, which enable integration of signal processing electronics into one chip with the MEMS gas sensors.

The following text is based on published papers summarised in Table 3-1 where I am main author or co-author.

Table 3-1: Main published works related to the chapter:

Paper title	Full reference
GaN, GaAs and Silicon based Micromechanical Free Standing Hot Plates for Gas Sensors	[75]
GaAs based micromachined thermal converter for gas sensors	[76]

My own research contribution can be summarized in following research areas:

- *Thermal modelling of three new MEMS metal oxide gas sensors based on GaN, GaAs and Si substrate), optimization of the thermal distribution on free standing hot plate and thermal resistance R_{th} extraction (chapter 3.3 and 3.4)*
- *Thermo-mechanical numerical modelling of free standing MEMS structure (chapter 3.42.5)*
- *Micromachined concept of GaN based micro-hotplate device to be designed for high temperature metal oxide gas sensors, to our knowledge, is introduced for the first time.*

3.2 Introduction and state of the art

The use of compound semiconductors (such as GaAs) for fabrication of MEMS addresses several problems. These materials are monocrystalline, have atomically flat interfaces, due to the technology of epitaxially grown layers, and extremely well controlled thickness, unlike polycrystalline materials. Also by controlling the lattice mismatch, the mechanical stress of epitaxial films is much more accurately controllable than in polycrystalline materials, which is usually controlled by annealing cycles. Performance and reliability are strongly affected by temperature causing thermal stress in multilayer structures. As temperature increases, physical changes within the device are accelerated. This seldom causes immediate, catastrophic failure; instead it brings about slow deterioration in the internal elements of the device, such as metallization areas, transistor junctions, temperature sensors, etc. The effect is cumulative, so failure rates could depend on the entire thermal history of the device. Temperature changes must therefore be analysed carefully when designing a MEMS working on thermo-mechanical principle, not only for sensitivity optimization but also for reliability purposes [73].

Present industrial metal oxide gas sensors are usually made by screen printing technique on small ceramics substrates. Typically require power consumption in the range 1- 2 W and response time is several seconds [77]. That could be usually too much for battery-driven diagnostic systems. There is a need for cheap, small and battery powered user-friendly gas sensing devices with high sensitivity, selectivity and stability. A power decrease and complexity of the gas sensing can be achieved through the design of semiconductor free standing MEMS micro hot plates. The gas sensitive layer is deposited on thin semiconductor free standing membrane of low thermal conductivity. Free standing membrane provides very good thermal isolation between the heated gas sensitive part and substrate, that itself remains nearly at ambient temperature. The power consumption of these hot plates can be less than 100 mW and the thermal time response can be within a range under 10 ms [77].

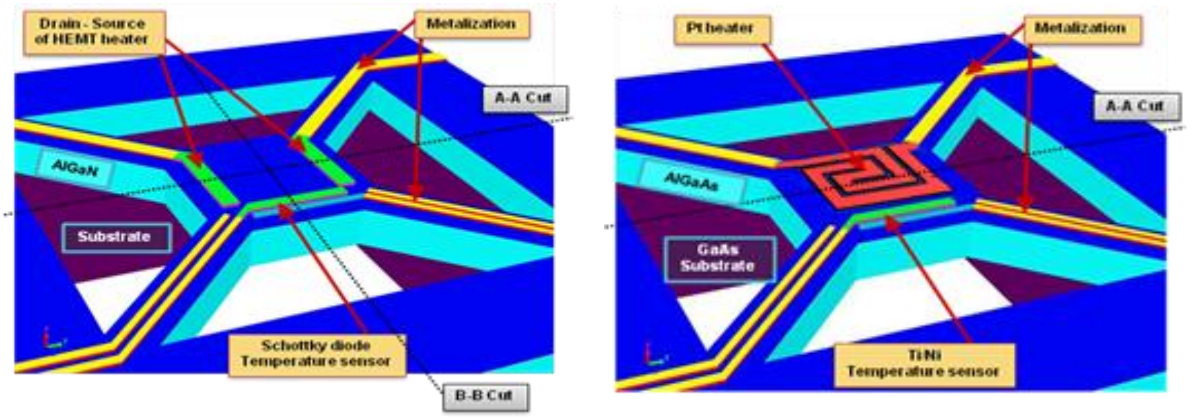
Typical micro hotplates are based on membranes made of silicon nitride and silicon oxide. Silicon technology is cheap and well developed, but silicon based hot plates maximum operating temperature is limited to only about 300 - 500°C [78]. To increase sensitivity, selectivity and response time of metal oxide gas sensors, we require much higher operating temperature of the gas absorption layer. Beside SiC, which was introduced as excellent candidate for these applications, the group of III-Nitrides can fulfil these requirements. MEMS hotplates based on GaAs and GaN can be very attractive for gas sensor micro hotplates design. The thermal performance of GaN hot plates can reach 1000°C [73].

In this paper we confront the performance of a new GaN MEMS hot plate design with silicon and GaAs based counterparts.

3.3 Hot plates design

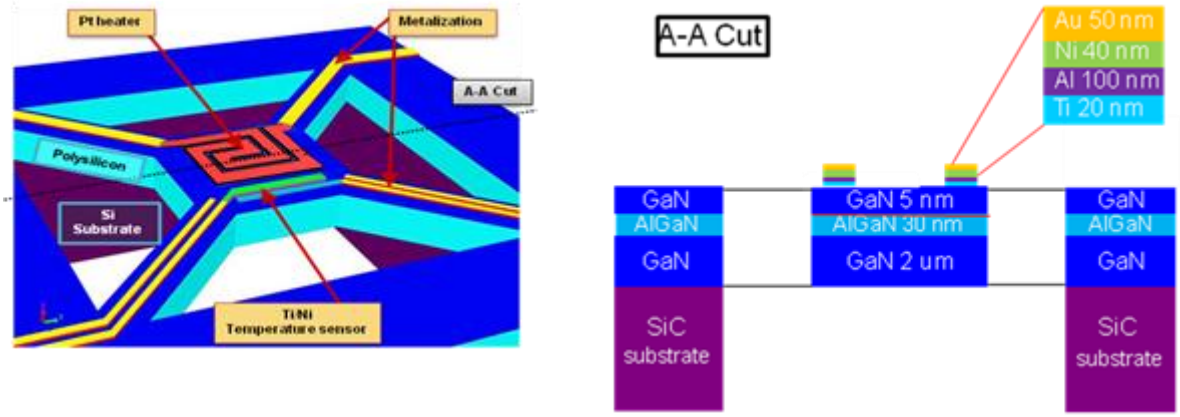
Thermally isolated hot plate was designed as free standing 2 μm thin MEMS island (150 x 150μm) supported only by four 20 μm wide cross bridges. Three different design

concepts were considered to confront thermo-mechanical performance of different materials. Figure 3.1a shows 3-D model of the suspended GaN/AlGaN heterostructure hotplate concept, including HEMT heater (High Electron Mobility Transistor), source and drain metallization and Schottky diode as temperature sensor. Two dimensional electron gas induced in AlGaN/GaN heterostructure by spontaneous and piezoelectric polarization forms an active conduction channel in the HEMT heater. SiC barrier layer and gas sensitive NiO layer is not shown. Composite layer system of the GaN hot plate is shown on Figure 3.2b. Conformable 3-D models were designed for GaAs and Si based hot plates with the view to compare their mechanical and thermal properties. In the case of GaAs and Si based hot plates a Ti-Pt heater and Ti-Ni temperature sensor was integrated within MEMS hot plate to heat up and control the sensor operation temperature Figure 3.1b and Figure 3.2a. The hotplate proportions are exactly the same for all three cases. For FEM numerical simulation 3-D model substrate has been designed 10 μm thick and 100 μm wide.



a) b)

Figure 3.1: a) Model of the GaN/AlGaN HEMT suspended hotplate structure. SiC barrier layer and gas sensitive NiO layer is not shown. Z axe dimensions are 30 times magnified; b) Model of the GaAs/AlGaAs hotplate concept. SiC barrier layer and gas sensitive NiO layer is not shown. Z axe dimensions are 30 times magnified [73]



a) b)

Figure 3.2: a) Model of the Si/PolySi suspended hotplate structure. SiC barrier layer and gas sensitive NiO layer is not shown. Z axe dimensions are 30 times magnified; b) Composite layer system of GaN HEMT hot plate (see A-A cut on Fig.3.1). [73]

Top view mask layout of MTHP hotplate is shown on Figure 3.3. Active devices (temperature sensor and heater) are covered by 500 nm thick SiC barrier layer that electrically isolates the 100 nm thick NiO gas sensitive layer and Pt interdigital electrodes.

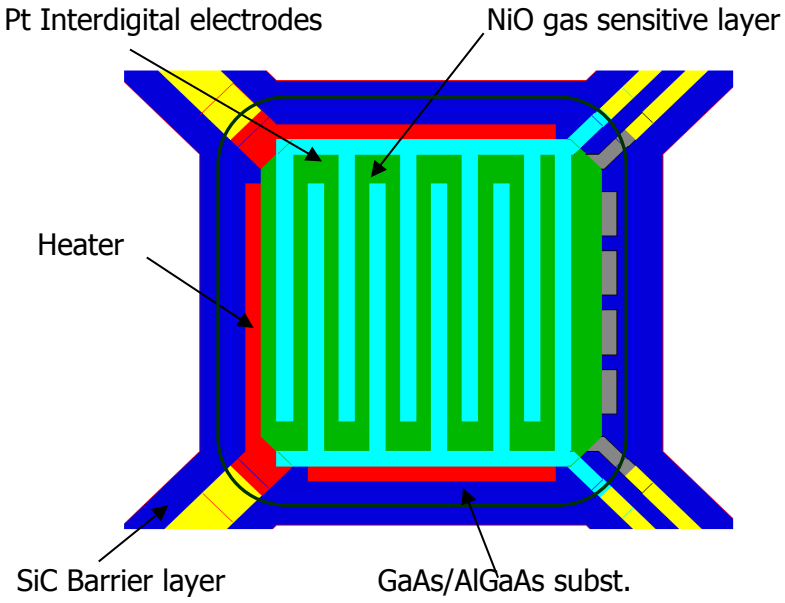


Figure 3.3: Top view mask layout of MTHP hotplate [73]

The MTHP fabrication process begins with the front-side processing technology of the micro-heater and temperature sensor. The process must be combined with surface and bulk micromachining of GaAs and should be fully compatible with the processing technology of microelectronic integrated circuits.

The multilayer GaAs/AlGaAs heterostructure active MTHP layers are grown by MBE (Molecular Beam Epitaxy) on GaAs substrate. After this technology step the double-sided aligned photolithography is carried out to define the etching masks on the both sides of the substrate. Highly selective reactive ion etching (RIE) of GaAs from the front side defines the lateral dimension of the hotplate structure while vertical dimensions are defined by deep back side RIE through a 300 μm thick GaAs substrate to the AlGaAs etch-stop layer [73]. Therefore the hotplate thickness (vertical dimension) is precisely defined by the thickness of MBE grown GaAs layer over AlGaAs etch-stop layer. As the final step AlGaAs etch stop layer is selectively etched. More technological details can be found in [77].

3.4 Hot plate modelling

Thermo-mechanical analysis has been performed to optimize the temperature distribution and determine the thermal resistance of micro hot plates.

For an isotropic homogenous material the steady state heat equation can be written [79]:

$$\nabla^2 T \equiv \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = -\frac{1}{k} Q(x, y, z) \tag{3.1}$$

where Q represents generated internal heat, k denotes the thermal conductivity, c_p its specific heat and T its temperature. The steady state temperature analysis has been performed to determine the temperature distributions and thermal resistance of the MTHP device.

Precise thermal analysis that includes the conduction, convection, and radiation effects is necessary to properly predict the behavior of thermo-mechanical devices. Not only quantitative but also qualitative performance can change if thermal boundary conditions are not set correctly.

In many cases convection and radiation losses from the device could be negligible and heat dissipation is entirely due to the heat lost to the substrate. In depends on the shape and dimensions of the device. This is modeled as a constant ambient temperature condition at the base of the substrate or on the side parts and patches of the 3-D model. These boundary conditions are known as Dirichlet [80].

Above mentioned assumption may not be true when the thermal mass of the substrate is not large enough to preserve the ambient temperature or the working temperature is relatively high. At that moment a natural boundary condition (Neumann boundary condition) must be chosen. After completing the thermal analysis we can get no uniform temperature distribution at the base substrate.

The technology process, environment, and the packaging of the MEMS device conclude which boundary condition is suitable. The choice of the type of boundary condition could significantly affect the device behavior.

Because of high temperature operation of MTHP we have used natural boundary condition. For the thermal analysis problem, the essential boundary conditions are prescribed temperatures. The spatial temperature distribution and steady state heat flux were calculated taking into account the heat transfers to infinity. In the current analysis, accordingly to the application requirement, the fixed thermal boundary is defined for the all side walls of the substrate. These sides were kept at the room temperature while other sides were adiabatic.

3D graph as shown in Figure 3.4 gives good overall visualization of the temperature distribution in the suspended island structure of the MTHP device, which is caused by the power dissipation generated in the thin film resistive Pt heater. The thermal analyses were performed for both vacuum ambient and gaseous air around the hotplate. The heat losses, due to radiation, were also taken into account.

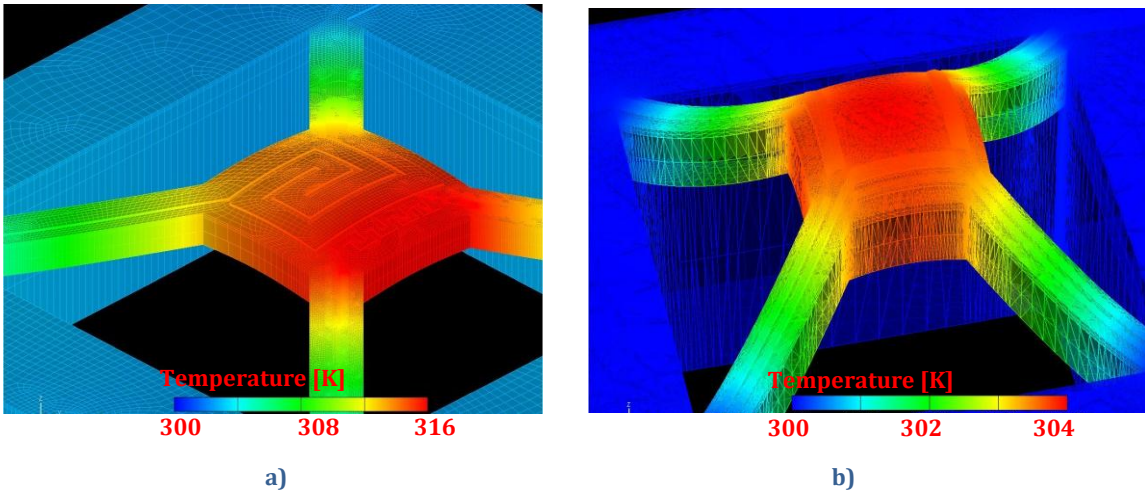
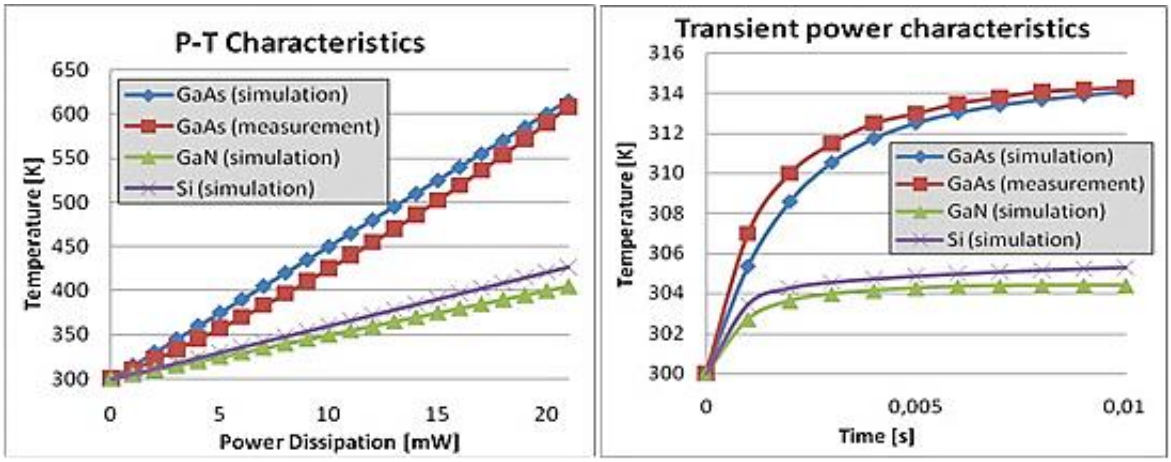


Figure 3.4: a) Temperature distribution of the GaAs/AlGaAs hotplate concept (Dissipated power in the heater was 1 mW); b) temperature distribution of the GaN/AlGaN HEMT suspended hotplate for 50 mW dissipated power in HEMT heater

Figure 3.5a shows simulated and measured power to temperature conversion characteristic. GaAs based hot plate shows the best thermal conversion efficiency with extracted thermal resistance R_{th} = 13.2 mW/K (measurement) and R_{th} = 15.1 mW/K (simulation). GaN and Silicon hot plate concepts reflect nearly the same thermal resistance: R_{th} = 5.1 mW/K for GaN and R_{th} = 6.05 mW/K for Silicon structure.

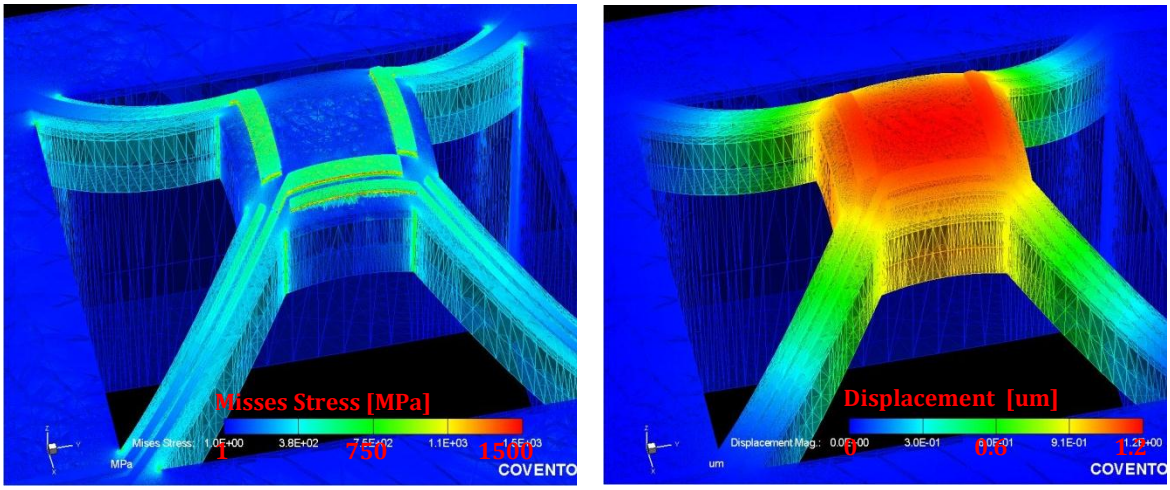
Transient power characteristics for 1 mW power dissipation in the heater are shown on Figure 3.5b. There is comparison between simulated and real measured characteristic of fabricated GaAs hot plate and simulated GaN and Silicon based hot plate. The boundary conditions were set as for steady state analysis. The power dissipation was generated either in the 2DEG volume of HEMT heater in the case of GaN based hot plate or in the volume of Ti-Pt heater for Silicon and GaAs hot plate concepts.



a) b)

Figure 3.5: a) Power to temperature characteristic. The comparison of various materials is shown. Ambient temperature was 300 K. Dissipation power in the heater 1-20 mW; b) The simulated thermal time response for 1 mW power dissipation in the heater for GaAs real structure and simulated GaAs, GaN and Silicon hot plates [73]

Composite MEMS hot plates design is also challenge with respect to mechanical design. There are many effects which must be considered during the hot plate design, including induced membrane thermal and intrinsic stresses, stresses in the metallization and HEMT composite layers. The final hot plate topology was carefully designed with respect to above mentioned problems. Figure 3.6a shows the simulated mechanical stress distribution that corresponds to HEMT heater power dissipation 50 mW. Z axe dimensions are 30 times magnified. Displacement is also shown and its magnitude is 4 times exaggerated. The peak value of thermally induced mechanical stress as large as 750 MPa is predicted mainly on the metallic interfaces and GaN cross-bridges. The mechanical boundary condition fixes all side walls of 3-D model. Table 3-2 summarize the material properties of used materials. Figure 3.6b shows displacement magnitude in μm for 50 mW dissipated power in the HEMT heater. Z axe dimensions are 30 times magnified. Displacement is also shown and its magnitude is 4 times exaggerated. Mechanical stress in the structure does not exceed yield stress and sensor structure is deformed only elastically.



a) b)

Figure 3.6: a) Mechanical stress in MPa for 50 mW dissipated power in the HEMT heater; b) Displacement magnitude in μm for 50 mW dissipated power in the HEMT heater. Z axe dimensions are 30 times magnified. Displacement is also shown and its magnitude is 4 times exaggerated

Table 3-2 – Material properties

Material	GaN	AlN	GaAs	Gold	Nickel	Platinum	Titanum
E (GPa)	330	392	71	80	220	145	110
Poisson	0,202	0,505	0,25	0,35	0,3	0,35	0,33
Density (kg/m3)	6150	3230	5320	19300	8910	21400	4510
TCE (1/K) * $1E^{-6}$	3,17	5,27	5,39	14,30	15,20	9,50	8,60
Thermal Cond (W/mK)	130	285	55	297	90,5	71,6	21,9
Specific Heat (J/kgK)	490	0	351	128	443	133	528

3.4.1 Hot plates fabrication

Fabrication process of GaN and GaAs micro-hotplates combines the front-side processing technology of AlGaN/GaN HEMT heater or Ti-Pt heater and Schottky diode temperature sensor with surface and back side bulk micromachining techniques. The details of the HEMT process technology can be found in [81] [82]. Figure 3.7 shows a real view of fabricated GaAs and GaN micro-hotplate devices[23]. The large HEMT or Ti-Pt heater and Schottky diode or 2DEG resistor as a temperature sensor can be clearly recognized.

[23] Hot plates were fabricated in IEE SAS Bratislava

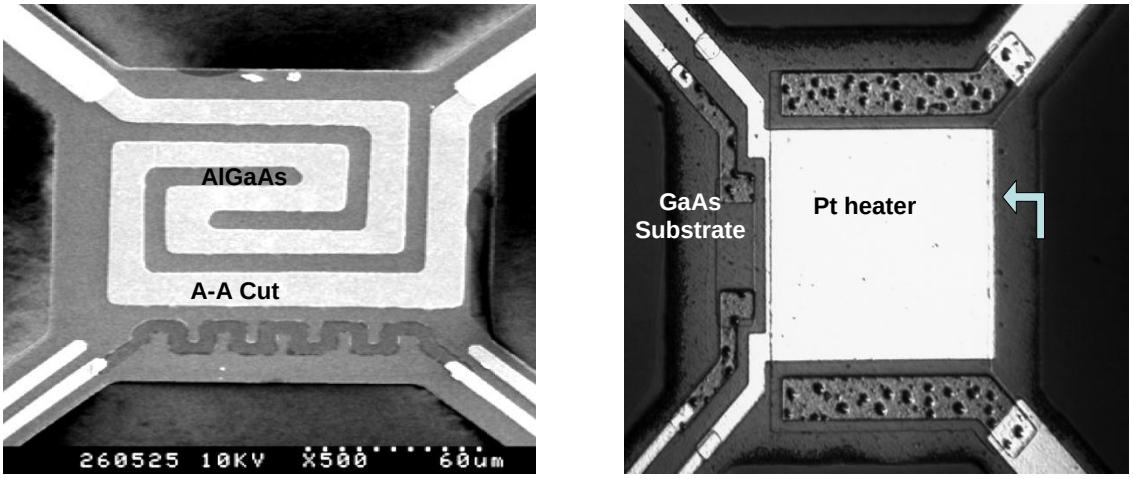


Figure 3.7: a) The real view of fabricated GaAs hot plate with Ti-Pt heater and Ti-Ni temperature sensor; b) Photograph of fabricated GaN micro-hotplate with HEMT heater and resistor as temperature sensor. [73]

3.5 Summary and Conclusion

In this chapter, the results achieved with the design of new GaN and GaAs based MEMS hot plate thermal converter has been shown. My own research contribution has been summarized in chapter 3.1. These section collets published scientific results that was summarised in Table 3-1.

Performance confrontation of the new GaN MEMS hot plate design with silicon and GaAs based counterparts that are considered to operate with high temperature metal oxide gas sensors are presented. The hot plates are based on a 2 μm thick suspended island with an integrated HEMT heater or Ti-Pt heater and Schottky diode (or 2DEG resistor) as a temperature sensor.

Thermo-mechanical numerical modelling has been carried out to optimize steady state and transient thermal performance. The mechanical coupling analysis was included in the simulations in order to control mechanical integrity of the hot plates.

Simulation results were compared with the experiment in the case of GaAs hot plate. GaAs based hot plate shows the best thermal conversion efficiency with extracted thermal resistance R_{th} = 13.2 mW/K (measurement) and R_{th} = 15.1 mW/K (simulation). GaN and Silicon hot plate concepts reflect nearly the same thermal resistance: R_{th} = 5.1 mW/K for GaN and R_{th} = 6.05 mW/K for Silicon structure. As compared with the experiment, the thermal resistance values are in good agreement. MEMS concept of GaN based micro-hotplate for high temperature metal oxide gas sensors has been introduced for the first time.

This work has been published in [73] and [74].

4 Design and Characterization of GaAs MEMS thermal converter

Main goal of is design and characterization of the new GaAs based RF Microwave Power Sensor (RFMPS) microsystem. The main criteria of the RFMPS optimisation are to keep the stable thermal distribution and minimise the thermal stress in multi-layer MEMS structure.

The chapter discusses the procedure for performing a thermomechanical analysis of thermal GaAs-based MEMS devices. It will provide the general procedure how thermal analysis should be made and model equations used to describe conduction, convection, radiation and mechanical effects caused by nonhomogenous temperature distribution. It also gives the values for thermal conductivity, heat transfer coefficients, emissivity, and reviews factors for various materials combined with GaAs technology. Increasing reliability requires both to control the temperature distribution in single elements of the device and to choose elements with high thermo-mechanical stress ratings adequate for the given application. The general doubt on the mechanical properties of compound semiconductors is largely speculative. While not as strong as silicon, compound semiconductors are sufficiently robust for most MEMS applications and are in fact stronger than the highest quality steel [45].

4.1 Motivation and author contribution

Transmitted power is the most important measure considered in RF systems. Usual approach to transmitted power measurement is based on the detection of absorbed power waves (incident and reflected) that requires complicated multiple power meter structures and need complex calibration.

An improved method of the absorbed power measurement is based on thermal conversion where, absorbed radio frequency (RF) power is transformed into thermal power inside of a thermally isolated system.

The conception of absorbed power measurement is based on thermal conversion, where absorbed RF power is transformed into thermal power, inside a thermally isolated system. Micromechanical Thermal Converter (MTC) spatial temperature dependences, thermal time constant and power to temperature characteristics are calculated from the heat distribution. The temperature changes induced in the MTC by electrical power dissipated in the HEMT (High Electron Mobility Transistor) are sensed by the integrated temperature sensor (TS). The temperature distribution over the sensing area and mechanical stress was optimized by studying different MTC sizes, and topologies of the active HEMT heater and temperature sensor [81].

The following text is based on published papers summarised in Table 4-1 where I am main author or co-author.

Table 4-1: Main published works related to the chapter:

Paper title	Full reference
GaAs Thermally Based MEMS Devices - Fabrication Techniques, Characterization and Modelling	[45]
Design and characterization of new GaAs micromechanical thermal converter developed for microwave power sensor	[83]
Optimization of GaAs MEMS structures for Microwave Power Sensor	[84]

My research contribution:

The main scientific contribution of this session is design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology in terms of the temperature distribution and optimization of the dynamic behaviour of the RFMPS system with respect to changes of the input RF power dissipation, which is generated by integrated HEMT transistor. Another contribution can be seen in modeling of mechanical properties (stress and strain) depending on the temperature changes caused by heating MTC structure.

4.2 Introduction and state of the art

The Gallium Arsenide based Micro-Electro-Mechanical Systems have some advantages over the well-understood Silicon micromachined microsensors. The most considerable advantages are some intrinsic material properties such as lower thermal conductivity, high temperature performance, heterostructure quantum effects, etc. The HEMT technology is compatible with GaAs based MEMS structures.

Thermal conversion element needs perfect thermal isolation. It should be also designed as small as possible to reduce thermal capacity and thus thermal time constant and power consumption. High thermal isolation of the MTC (Micromechanical Thermal Convertor) structure can be reached by the very thin free micromechanical plate. We have developed a new GaAs based MTC technological process, which creates optimal conditions for both, the monolithic integration of active HEMT heater and thermal isolation of the microwave sensor elements. Thermo-mechanical numerical modelling and temperature distribution optimization have a significant influence on the performance of the Micromechanical Thermal Converter. MTC structures with a diverse sizes and arrangements of the heater and the temperature sensor were studied [81].

The thermoelectric AC power sensor and microwave power sensor were firstly analysed by Jaeggy and Kopystinski [85] [86] by using CMOS IC technology. The heater was defined with a polysilicon resistor and a Polysilicon/ Aluminium thermopile was used as temperature sensor. Unfortunately, these sensors cannot be integrated with III-V compound semiconductors.

4.3 Micromechanical Thermal Converter design and models

The MTC structures used in the thermally based MEMS devices are mostly designed as free space standing structures. To increase the thermal resistance values, they have to be designed with the thickness as thin as possible. A new processing technology of GaAs micromechanical island structure has been developed[24]. The technology process begins with the MBE or MOCVD growth of GaAs heterostructure on semi-insulating substrates (SI-GaAs) (Figure 4.1). A front-side processing technology is performed to define Source (S), Drain (D) and Gate (G) of the HEMT. The GaAs surface is completed by Ti (50 nm) / Au (150 nm) metallic transmission lines, which allow connections to the heater and TS [82].

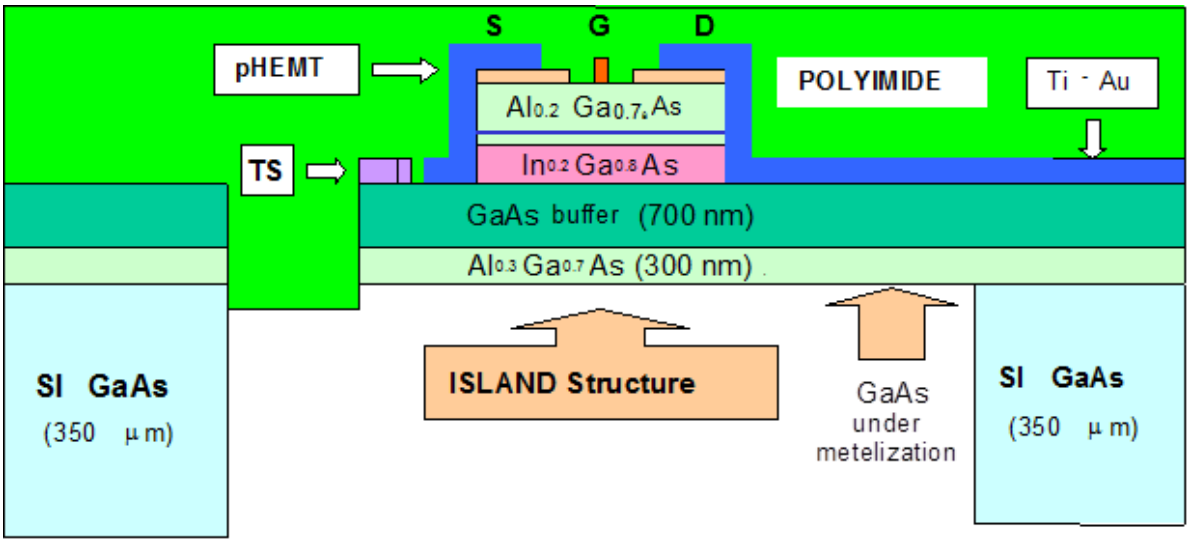


Figure 4.1: Schematic cross-section through the polyimide-fixed MTC structure to be integrated with HEMT as heater and poly-Si/Pt thin film resistor as temperature sensor TS [81]

Next step is a surface micromachining of cantilever, bridge or island by a masked non-selective wet or plasma etching of the heterostructure up to semi-insulating (SI) GaAs. A surface micro-machining is followed by deposition and subsequent thermal forming of a thin top polyimide layer. Finally, a three-dimensional patterning of the micro-mechanical structures is defined by a deep back-side selective reactive ion etching of SI-GaAs through the openings in mask, using AlGaAs together with the polyimide as an etch-stop layer [81].

Thin polyimide layer is deposited after the bulk GaAs micromachining and enables the micromechanical structures to be mechanically fixed and thermally isolated in a fee space.

Schematic cross-section is shown on Figure 4.1. Silicon delta-doped layer is formed for HEMT design in the $Al_{0.22}Ga_{0.78}As$ barrier layer. This layer is separated by 3 nm thick undoped $Al_{0.22}Ga_{0.78}As$ spacer from the $In_{0.2}Ga_{0.8}As$ channel. $GaAs/Al_{0.3}Ga_{0.7}As$ (700 / 300 nm) heterostructure buffer layer under channel was designed to define the thickness of the MEMS structure [81].

Subsequent benefits of this technology is that microwave controlled circuit can be also integrated within the MTC microstructure

[24] Technology of MTC was developed by IEE SAS Bratislava

The design criteria to assess the general performance and considerations of the sensor are given below [82]:

- *Reduced maximum stress in both GaAs substrate and Ti/Au metallization layers, in particular in the heated active area of the MTC device.*
- *Uniform temperature distribution over the sensing element (meander-like temperature sensor).*
- *Increase sensitivity (dissipating power to temperature conversion, Rth).*
- *Quick time response (change of the temperature as a result of change of input power)*

According to the above criteria extensive 3-D models of the MTC structure have been designed and numerical simulations have been carried out to evaluate the performance of the sensor.

The three following MTC device types have been investigated to compare their thermal and mechanical behavior:

- *Fixed Cantilever Beam device*
- *Fixed Island device*
- *Fixed bridge device*

The temperature distribution over the sensing area and device mechanical stresses were optimized by studying different MTC formations, and layouts of the heater and temperature sensor.

Figure 4.2 demonstrates the model of GaAs island structure which has been proposed to increase a sensor thermal resistance. The GaAs island (175 μm x 125 μm) floats in 1 μm thin polyimide membrane (225 μm x 360 μm) that mechanically fixes and thermally isolates the GaAs MTC plate. For numerical simulation purposes GaAs substrate rim has been designed 10 μm thick and 50 μm wide. These dimensions ensure sufficient mass for simulator boundary condition setting while keeping number of simulation nodes at reasonable level.

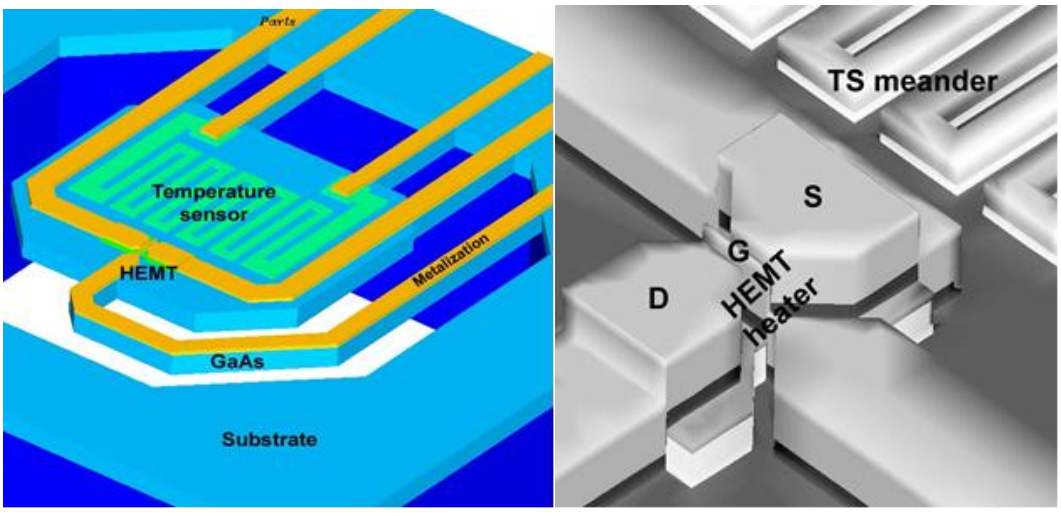


Figure 4.2: Model of the Island MTC structure. GaAs island is floating in Polyimide 1 um thick layer (not visible). The meander-shaped TS is also shown. Z-direction is 20times magnified. The Detail of HEMT heater is on the right [81].

Optimized island structure design reduces the maximal stress caused by temperature changes; minimize the temperature losses that were caused by too short supplying metallization to HEMT transistor. The 3-D model is depicted on Figure 4.2. Gate supplying metallization was led around the island order to lengthen it as much as possible. The temperature losses are minimized by this solution [81].

Another advantage is that all metallization are entering the substrate surface in the same location and there are no other metallization on the opposite site. The mechanical compressions are minimized by this solution.

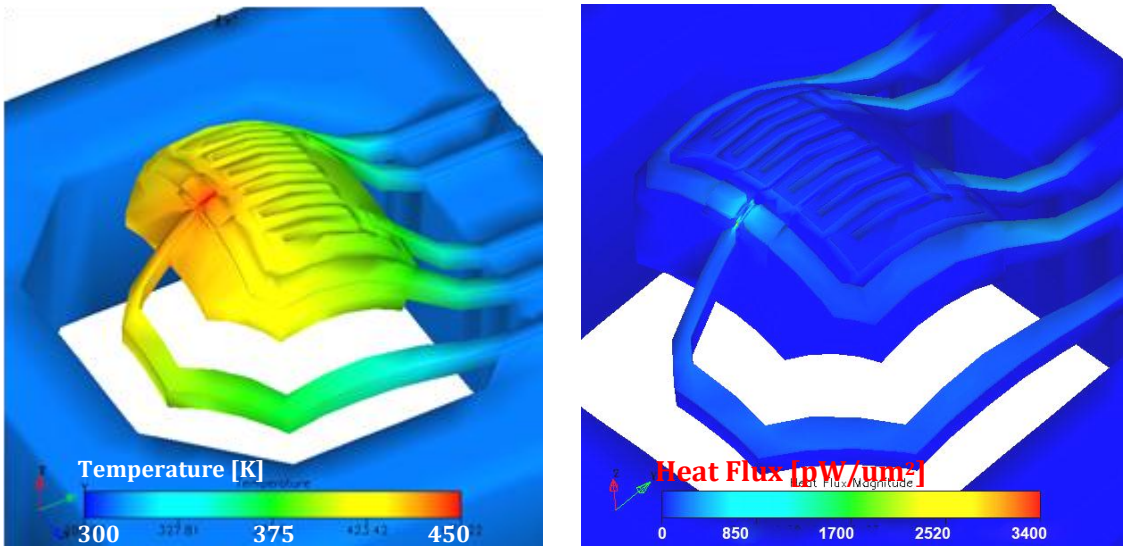
4.3.1 Thermal analysis

The steady state temperature analysis has been performed to propose the sensibility and thermal resistance of the structure. The temperature distribution caused by power dissipation in the heater and thermal time response as a result of power changes were evaluated by the MemTherm module of Coventor software.

The input power dissipation in the heater was defined as heat flux coming through the HEMT gate area (10 μm x 0.5 μm). We can use this approximation because the heat dissipation in HEMT structure is generated in very thin conduction layer which formed under the gate area.

The spatial temperature distribution of the MTCs and steady state heat flux were calculated taking into the account the heat transfers to infinity. In the current analysis, according to the application requirement, the fixed thermal boundary is defined for the all side walls of GaAs substrate. These sides were kept at the room temperature of 300 K while other sides were adiabatic.

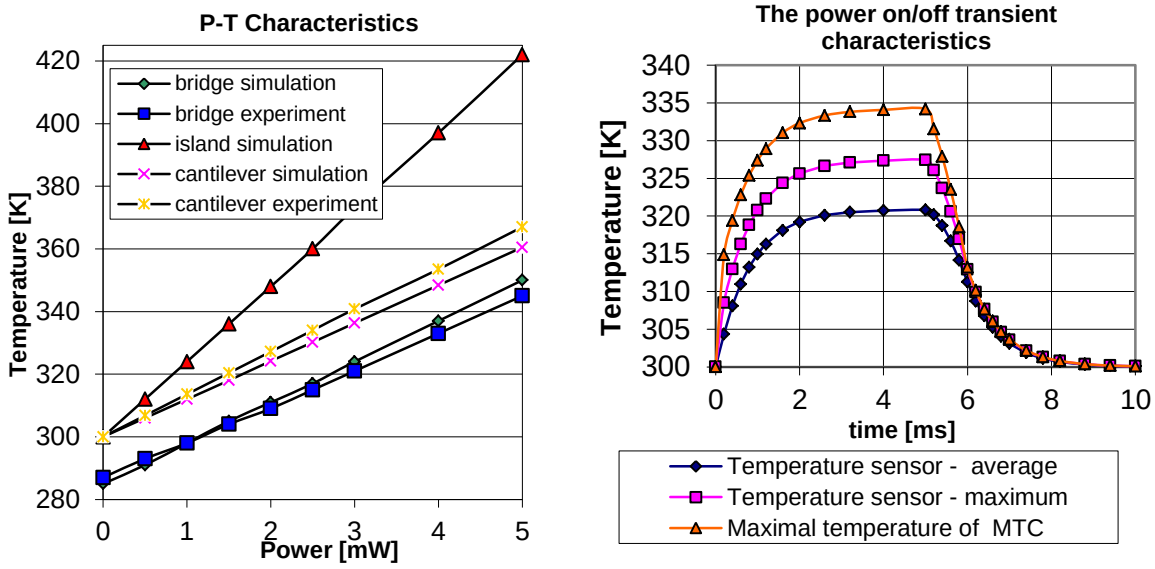
3-D diagram gives good overall visualization of the temperature distribution (Figure 4.3) in the island MTC structure caused by the power dissipation generated by the HEMT heater. Thermal boundary conditions were defined for side walls of GaAs substrate. These sides were kept at the room temperature of 300 K while other sides were adiabatic. The island is "floating" in the polyimide layer that mechanically fixes and thermally isolates the MTC structure. Polyimide layer is not shown on the figure, but was considered in the simulation [81].



a) b)

Figure 4.3 a) 3-D plots of temperature distribution of the island MTC structure. The island is "floating" in polyimide layer that mechanically and thermally isolates the MTC structure. Polyimide layer is not shown. The scale factor in the z direction was multiplied by 10. b) 3-D plots of heat flux (μW/μm2) of the island MTC structure. Polyimide layer is not shown. The scale factor in the z direction was multiplied by 10 [73]

The thermal analyses were performed for both vacuum ambient and non-convective gaseous medium around the MTC structure. The heat losses, due to radiation, were viewed as negligible. Derived power to temperature characteristic is on Figure 4.4. From the angular coefficient we can express thermal resistance R_{th} of the structure which is summarized for different topologies of the MTC structure on Table 4-2 [81].



a) b)

Figure 4.4: a) Simulated island, cantilever and bridge Power to Temperature characteristics. Comparison with real micro-machined MTC device. Ambient temperature for bridge MTC was 285 K whereas other two MTCs ambient were 300 K. b) The power on/off transient characteristics for island MTC structure for power ON of 2mW. At the beginning there was power of 2mW switched ON. In the time of 5ms the power was switched OFF [81].

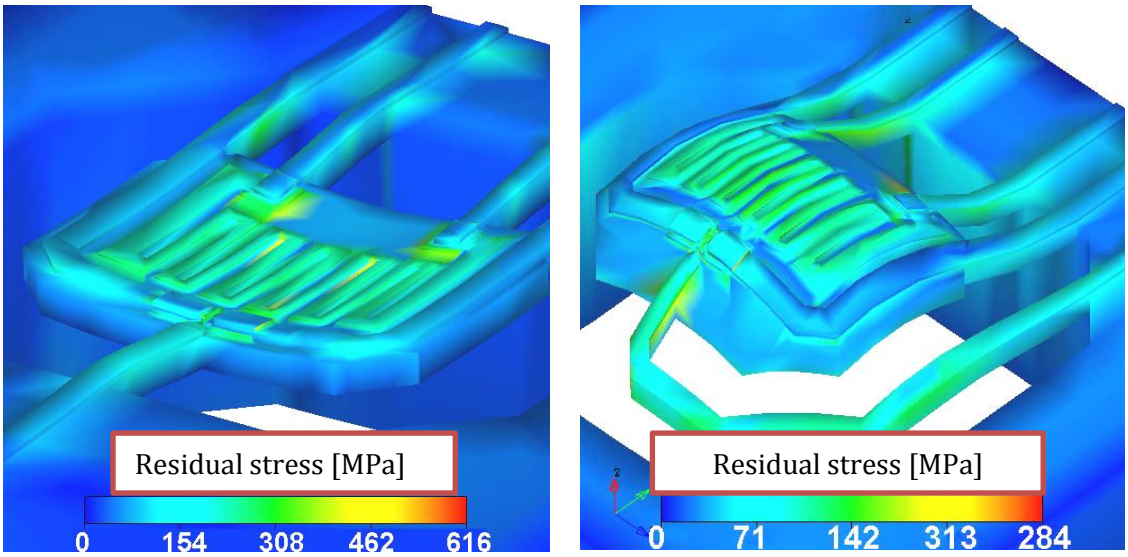
Transient on/off power characteristics for island structure are depicted on Figure 4.4b. At the beginning there was power of 2mW switched ON. In the time of 5 ms the power was switched OFF. Thermal time constant of the island structure arrangement is 1.9 ms. There are three transients on the Figure 4.4b. Upper is the maximal temperature of the heater and the bottom dependence reflect average temperature of TS [73].

4.3.2 Thermal stress and displacement evaluation

The mechanical and thermal boundary conditions were defined for side walls of GaAs substrate. These sides were kept at the room temperature of 300 K while other sides were adiabatic and were set as rigid e.g. non moveable. The initial stress was set in each material according the analytical calculation.

The stress and displacement magnitude evaluation were simulated using MemMech simulator. Figure 4.5 shows the plot of residual stresses and a deformation of the island structure and optimized island structure caused by heating up. The shading represents residual stress for 1 mW power dissipation in the heater. The biggest stresses (616 MPa) are located in the place of the meander-shaped PolySi temperature sensor. The stress is significantly reduced in the optimized island structure design (284 MPa).

The MTC structure is fixed by polyimide layer that is not shown in the figure, but was taken into account during the simulation. The scale magnifications in Z-direction being X10 and the displacement magnification being X2.



a) b)

Figure 4.5: Residual stresses and deformation of the island structure caused by heating up with power dissipation of 1mW in the heater. a) island structure b) optimized island structure. Polyimide layer was investigated in simulation (not visible). Values of stress are in MPa.

Table 4-2: MTC simulation results summary [81]

	Island without GaAs	Island with GaAs	Optimized island with GaAs
R_{th} simulation [K/mW]	*24*	*13*	*26*
R_{th} measurement [K/mW]	-	*14*	-
τ simulation [ms]	*0.9*	*0.9*	*0.8*
τ measurement [ms]	-	*0.8*	-
Max. temperature [K] (1mW)	*332*	*320*	*336*
Max. displacement [μm] (1mW)	*2.74*	*0.26*	*5.28*
Max. mechanical stress [MPa] (1mW)	*540*	*434*	*284*

4.3.3 Influence of the gate width on maximal temperature of MTC structure

The influence of the gate width on maximal temperature of MTC structure has been simulated. Temperature distribution in the HEMT and in the MTC structure for different gate width (5 μm, 10 μm, 15 μm, 20 μm) has been obtained.

From the simulation results follows that the maximal temperature of the MTC microstructure which is located in the gate of the HEMT is inversely proportional of the gate width Figure 4.6

The analysis also proved that the temperature sensed by temperature sensor remained the same. It can be concluded that the HEMT gate width does not have any influence to the resulted sensitivity, only maximal temperature changes. In order to minimize maximal temperature of the sensor it is desirable to increase the HEMT gate width as soon as possible. The dissipated power is then generated in greater volume. Due to maximal temperature reduction the sensor structure could be used for wider field of measured power while the sensitivity remains the same [81].

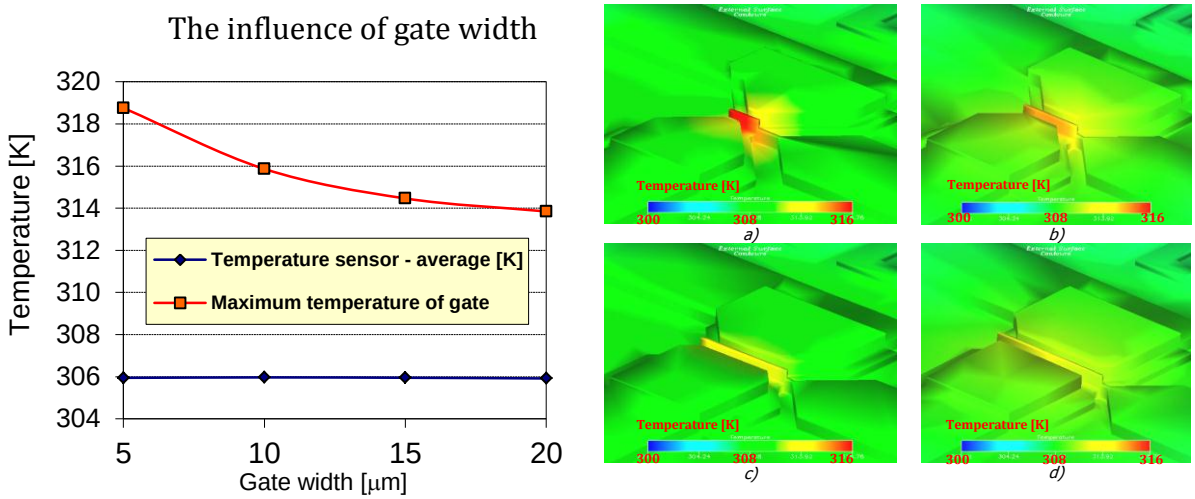


Figure 4.6: Left) Maximal and average temperature – HEMT gate width dependence. Dissipated power was 0.5 mW. [73] Right) Temperature distribution in the HEMT and in the MTC structure for different gate widths: a) 5 μm, b) 10 μm, c) 15 μm, d) 20 μm. Dissipated power in the HEMT was 0.5 mW. From the simulation results follows that the temperature of the MTC structure remains the same

4.4 Summary and conclusions

In this section, main results achieved with the design of new GaAs MEMS thermal converter have been presented. My own research contribution has been summarized in chapter 4.1. These section collets published scientific results that was summarised in Table 4-1.

The most important scientific contribution of this session is design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology and modeling of mechanical properties (stress and strain) depending on the temperature changes caused by heating MTC structure. Spatial temperature dependences, thermal time constant, thermal stress and displacement and power to temperature characteristics were calculated from the heat distribution. Topology of HEMT transistor, temperature sensor and MTC shape has been optimized.
Power to temperature (P-T) conversion characteristics of the MTC devices was simulated and compared with measurement of real micromachined structures. The high electro-thermal conversion efficiency, defined by extracted thermal resistance values (R_{th}) 24 K/mW, was achieved for island structure. As compared with the experiment, the thermal resistance values are congruent.

The work was published in [45], [81] and [82]

5 Thermo mechanical and piezoelectric design of the pressure sensor for harsh environment

Many industry applications require electronic devices that can operate in increasingly harsh environments e.g.: extreme temperature, pressure, large electric fields or chemically aggressive substances. This work summarises results of thermo-mechanical and piezoelectric simulation of the new pressure sensor and its package. The research work was done in frame of the MORGAN[25] project which addresses the need for new materials for electronic and sensors devices that operate in extreme conditions, especially high temperatures. Advantage of the excellent physical properties gallium nitride (GaN) based heterostructures plays a key role in design of new sensor structures. The work also report on piezoelectric response investigation of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) as a new stress sensor that can be potentially applied for dynamic high-pressure sensing in extreme conditions. The piezoelectric performance simulation and packaging issues of the device are discussed (Chapter 5.3).

Chapter 5 is divided to two sections. The first one denote on modelling and simulation of mechanical and electro-mechanical behaviour of the GaN and AlGaN/GaN based sensor structures with integrated High Electron Mobility Transistor (HEMT) as piezoelectric element for pressure sensing. The sensor was evaluated by mechanical load (applied force) analysis, harmonic analysis and piezoelectric response. Simulation results are in good agreement with measurement done by SAS IEE Bratislava. The second part focuses on suitable packaging of the sensor that has to withstand high temperature and pressure (Chapter 5.4 to 5.6).

5.1 Motivation and author contribution

The most essential aim of this work has been to apply new semiconductor materials which are stable especially at high temperature. III-Nitrides (III-Ns) are very attractive for pressure and stress sensor applications because of their excellent piezoelectric properties [87]. New design of ZnO-passivated AlGaN/GaN-based circular HEMT (C-HEMT) structures can be utilized for new stress and dynamic pressure sensors [86].

Increased attention must be paid to design of suitable package that have to enable the capability to withstand high temperature and pressure. An accurate modelling and simulation of Drumskin pressure sensor packaging system developed by IVF (Sweden)[26] has been carried out. New package design is optimized by thermal evaluation and calculation of induced stress in the solder joints and the glass frit, which is used to seal the sensor chip at high operating temperatures and different applied pressures.

The following text is based on published papers (Table 5-1) where I am co-author and new unpublished results describing modelling of influence of the pressure sensor package on encapsulated sensor structure.

[25] MORGaN is a project supported by the European Commission's Seventh Framework Programme to develop new materials for Robust Gallium Nitride applications

[26] Swerea IVF, Argongatan 30, SE-431 53 Mölndal, Sweden

Table 5-1: Main published works related to the chapter:

Paper title	Full reference
Piezoelectric response of AlGaN/GaN-based circular-HEMT structures	[74]
Impact of ZnO gate interfacial layer on piezoelectric response of AlGaN/GaN C-HEMT based ring gate capacitor	[73]
Simulations of a high temperature pressure sensor packaging and interconnection	[88]

My research contribution can be summarized in following research areas:

- *Numerical modelling of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) designed for new stress sensor to be potentially applied for dynamic high temperature pressure sensing;*
- *Evaluation of pressure sensor in terms of applied mechanical load, harmonic analysis and piezoelectric response. Calculation of specific mechanical and piezoelectric response of III-N based structures;*
- *Evaluation of the performance of new package design and its optimization for Drumskin pressure sensor packaging system; evaluation of the package influence on encapsulated sensor structure at high operating temperatures and different applied pressure;*
- *Understanding of mechanical failure effect during thermal cycling and reduction of alternating stress at the interface between nano-Ag and Pt layer.*

5.2 Introduction and state of the art

Numerous papers have recently been published on the capabilities of a new III-N semiconductor material system [89] [90]. Wider band-gaps make these materials more suitable to operate in a high temperature environment. For example GaN systems could operate up to 1000°C. Dramatic increase of these semiconductors materials that can be exposed to harsh environments might be seen in recent years. Harsh environment (extreme temperature, pressure, large electric fields or chemically aggressive substances) requires not only development and research in new semiconductor materials, devices and sensors but also design of reliable packaging system which is extremely important. Regarding to new semiconductor materials, III-Ns have some significant advantages:

- *Compatibility with HEMTs technology;*
- *High mechanical stability of epitaxial films, which gives the possibility to integrate III-Ns into MEMS mechanical sensors;*
- *High temperature performance including their piezoelectric properties are preserved in a wide temperature range.*

These properties give possibility to change the conductivity of a HEMT directly through external stress. AlGaN/GaN-based HEMT devices contain a highly conductive two-dimensional electron gas at the interface that is sensitive to mechanical load. This effect can be used for novel sensors [87].

However, not much research effort has been given to packaging of these semiconductor materials operating in extremely high temperature. Okoije et al [91] have reported on a SiC pressure sensor encapsulated in an AlN based package for operation up to 600 °C and Guo et al [92] have demonstrated SOI based sensor in a similar package and Platinum wire bond.

The most critical problem for high temperature packaging is accumulated thermo-mechanical stress and strain induced by the different temperature expansion coefficients of used materials for the packaging and interconnect. Moreover, creep effect could be dominant during periodical thermal cycling of the sensor system. Creep effect appears when absolute temperature of metal is above half of melting point.

The proposed packaging technology for Drumskin pressure sensor is based on the green-state milling of alumina to the desired geometry and via channels for the electrical electrodes. Technology use sintering of the ceramics on the electrically conductive metals placed inside. The electrical interconnections are based on silver[27].

5.3 GaN and AlGaN/GaN -based structures with HEMT as piezoelectric sensing element

Modelling and simulation of mechanical and electro-mechanical behaviour of the GaN and AlGaN/GaN -based structures with integrated High Electron Mobility Transistor (HEMT) as piezoelectric pressure sensing element is shown in this session. Different approaches were proposed to describe the behaviour of the sensing unit.

Sensor structures:

1) Cantilever sensor structure
3) Circular HEMT (C-HEMT) sensor structure

5.3.1 Cantilever sensor structure

The main goal was to understand how mechanical stress is distributed in AlGaN/GaN heterostructure based cantilever and investigate piezoelectric response in circular HEMT (C-HEMT) when mechanical load is applied. C-HEMT exhibits some advantages over that of a conventional rectangular HEMT. There is no need of "MESA" etching step that define the C-HEMT. Additionally, the ring gate shape can be easily patterned.

5.3.1.1 Simulation conditions

To calculate specific mechanical and piezoelectric response of fabricated AlGaN/GaN based circular HEMT structures, finite element analysis simulations using CoventorWare were performed. The sensor structure (Figure 5.1) consists in a multilayer cantilever composed of

[27] Developed by colleagues from Swerea IVF, Argongatan 30, SE-431 53 Mölndal, Sweden

SiC substrate, AlN cantilever, GaN and AlGaN active layers. An undoped AlGaN/GaN heterostructure on SiC substrate was used to define a C-HEMT sensing device. The AlN layer is used as a nucleation layer. The thickness of GaN layer was 1,5 µm and thickness of AlGaN layer was 25 nm. Detail of the simple C-HEMT structure consisted of circular source/drain ohmic contacts is shown on Figure 5.2.

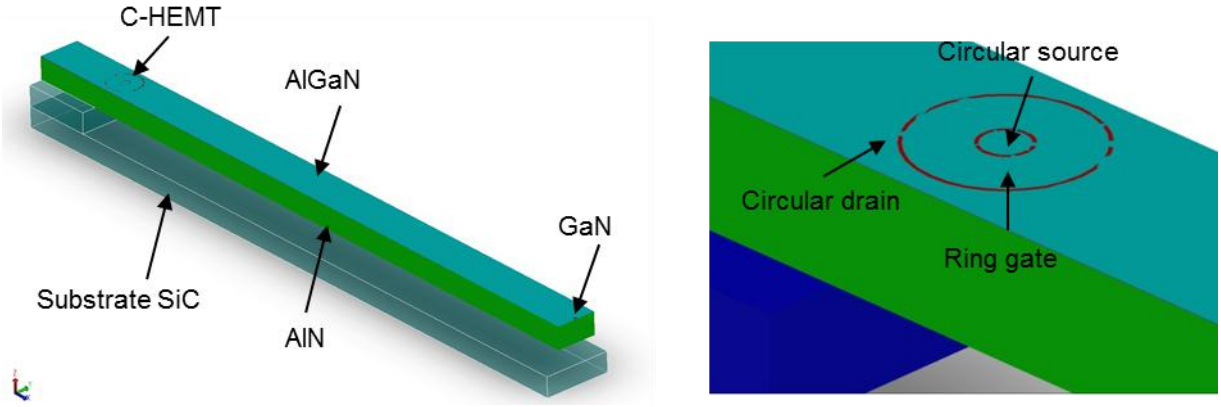


Figure 5.1: Cantilever sensor structure with C-HEMT sensing element. a) The cantilever b) zoom to area of C-HEMT

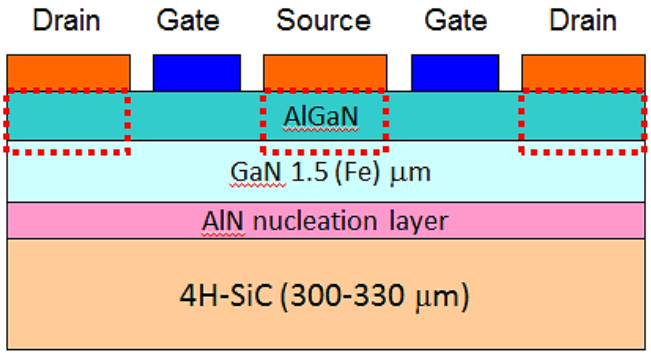


Figure 5.2: C-HEMT Structure cross-section[28] [86]

As boundary conditions bottom layer of testing anchor was mechanically fixed; all other model faces were mechanically free. To calculate intrinsic stress a deposition temperature of AlGaN/GaN layers was set according fabrication process to 1300 K. Mechanical load was applied as force acting in z axis direction on the end of cantilever. Source electrode was grounded and piezoelectric potential was measured on Gate electrode.

Material parameters used for the modelling are shown in Table 5-2. For thin piezoelectric layers (under 500 nm), piezoelectric coefficient d_{33} is strongly dependent on layer thickness. F. Martin at all in [93] has shown that if AlN film thickness increases from 35 nm to 250 nm, the d_{33} rapidly increases from 2.75 to 4.6 pm/V and gradually flattens to reach maximum value of 5.15 pm/V for thickness of 2 µm. In the simulation d_{33} was set to 2.5 pm/V for layer thickness 25nm [87].

[28] C-HEMT fabrication technology and layer system was designed in SAS IEE Bratislava

Table 5-2: Material properties used in Coventor Ware models

	SiC	GaN	AlGaN	AlN
Young's modulus (GPa)	410	315	315	392
Poisson's ratio	0.14	0.202	0.204	0.505
Density (kg/m^3)	3100	4300	5430	3230
TCE a_0 (10^{-6}/K)	4.00	5.59	5.51	5.27
TCE c_0 (10^{-6}/K)	-	3.17	3.41	4.15
Piezoelectric stress coefficient e_{13} (C/m^2)	0	-0.49	-0.51	-0.57
Piezoelectric stress coefficient e_{33} (C/m^2)	0	0.73	0.67	0.97
Dielectric constant	0	10.4	8.8	8.55

5.3.2 Mechanical analysis

Finite element analysis (FEA), using a CoventorWare simulation tool, was performed to confirm that the C-HEMT device with a thin piezoelectric ZnO layer on the gate interface exhibits an increased stress detection sensitivity. FEA 3-D model was build according to real device topology (a bulk SiC cantilever with the integrated real topology of C-HEMT device placed near to the cantilever clamped area). To calculate initial stress in all layers, the deposition temperature of the AlGaN/GaN layers was set to 1300 K, according to the fabrication process, and the mechanical response was calculated at 300 K. The simulation tool computes piezo-electric strain (strain-charge constitutive relation). The solved piezoelectric equation can be written in strain-charge form [94]:

$$[\varepsilon] = [D]^{-1}|_{[E]=0}\,[\sigma]+[d]^t[E] \qquad (5.1)$$

where $[\varepsilon]$ is the strain matrix, $[D]^{-1}|_{[E]=0}$ is the material compliance matrix when there is no electrical field, $[\sigma]$ is the stress matrix, $[d]$ is the PZE-strain coupling matrix and $[E]$ is the electric field vector.

Mechanical load was applied as force acting in the *z* axis direction at the end of the cantilever. The source electrode was grounded and drain electrode can remain unconnected (The source in fact electrically connect the bottom layer of AlGaN piezoelectric layer by ohmic contact) and the Piezoelectric potential was calculated on the ring gate electrode for harmonic loading at frequency of 20 Hz.

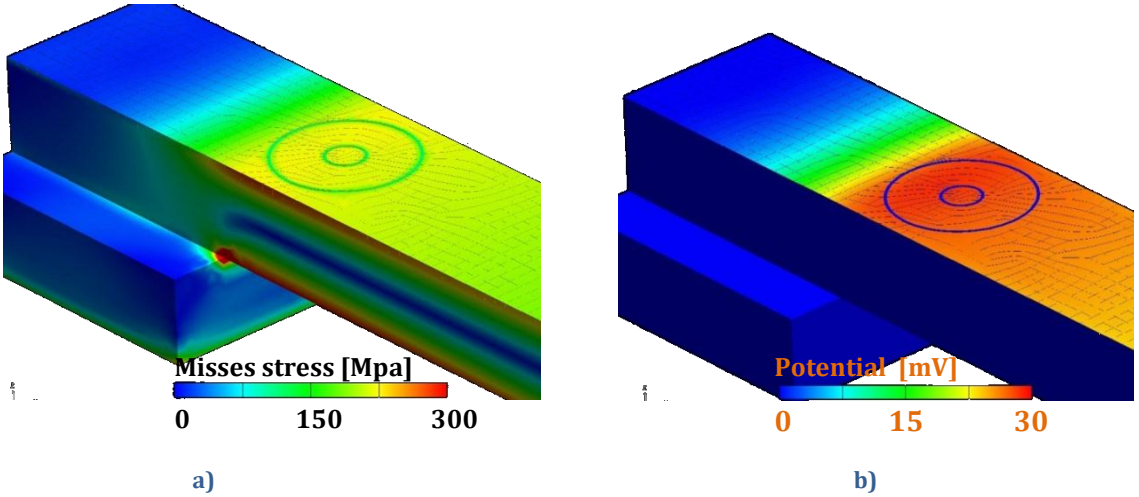
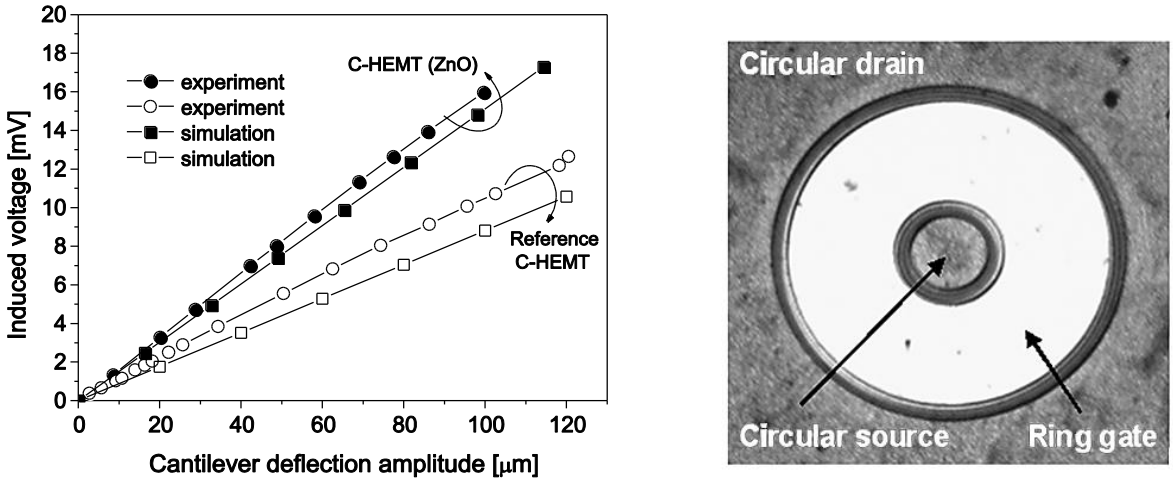


Figure 5.3: a) Simulated mechanical stress distribution of the cantilever for deflection 249 µm caused by loading force 0.8 N. b) Piezoelectric potential caused by initial stress - load 0.8 N

Figure 5.3b shows calculated piezoelectric gate potential (between top and bottom of AlGaN layer) in gate area for linearly increasing cantilever deflection caused by applied force (on the end of cantilever). Bottom layer of AlGaN has zero potential. Simulated mechanical stress distribution of the cantilever for deflection 249 μm caused by loading force 0.8 N is shown on Figure 5.3a.

The calculated piezoelectric potentials induced on the ring gate electrodes of both types of C-HEMT (with and without ZnO) were also compared with those measured in Figure 5.4. It shows a very good correlation with the experiment.



a) b)

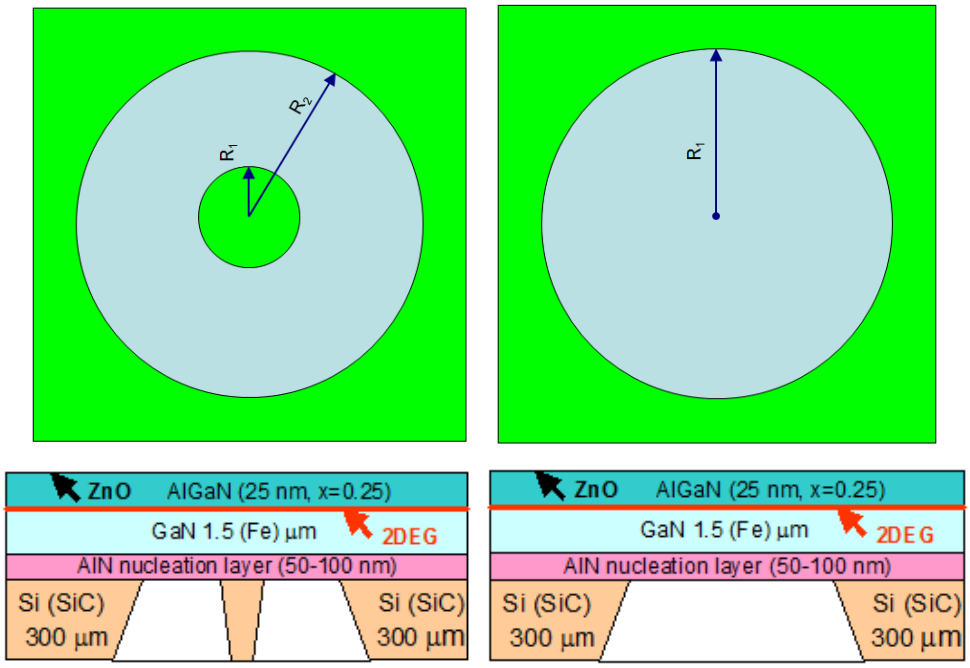
Figure 5.4: a) Simulated and measured sensor voltage as a function of cantilever deflection amplitude b) Real view of C-HEMT device (right)[29] [86]

Experimental results show that a very thin piezoelectric ZnO layer grown by PLD on the AlGaN barrier layer of a C-HEMT stress sensor yielded over a 60 % increase in the piezoelectric detection sensitivity of the device. This improvement was also supported by a three-dimensional CoventorWare simulation. The new ZnO passivated C-HEMT stress sensor is promising for dynamic high-pressure sensing applications in harsh environments [86].

5.3.3 Circular HEMT (C-HEMT) sensor structure

Simulation and experimental results shown in previous section are promising for pressure sensor construction. Two types of new pressure sensors with C-HEMT was designed and simulated. Figure 5.5 shows two types of designed pressure sensor topologies.

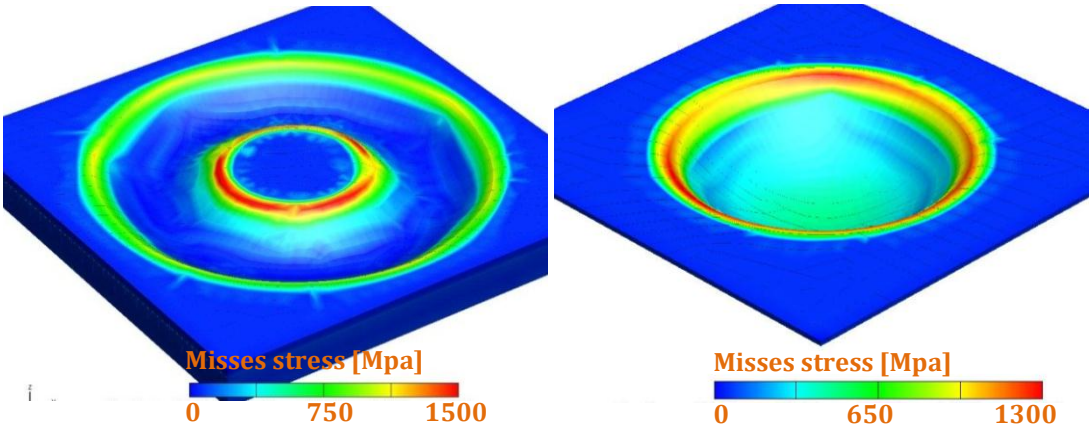
[29] Cantilever MEMS with C-HEMT was fabricated in SAS IEE Bratislava



a) b)

Figure 5.5: a) C-HEMT based ring membranes and b) C-HEMT based circular membranes; and cross-section view

Mechanical analysis was done for applied pressure 1 MPa to the membrane of the sensor in direction of z-scale. Maximum deformation of 9. 7 µm was calculated for membrane type and deformation of 5.1 µm was calculated for memrane with support in the centre. Z-scale displacemetn is 10 times exaggerated. Figure 5.6 shows results of mechanical stress distribution.



a) b)

Figure 5.6: Distribution of mechanical stress for applied pressure 1 MPa. a) C-HEMT based ring membranes and b) C-HEMT based circular membranes

Next research on these types of pressure sensor is on-going to calculate piezoelectric response.

5.4 Pressure sensor package 3D model

As I already mentioned in chapter 5.2, proper packaging of such pressure sensor is very important. The package design assembly consist of a ceramic holder and electrical leads enclosed within the structure connecting to a lid. 3-D model of pressure sensor package is on Figure 5.7. The electrical interconnections to the active electronics chip are made using a nano-silver die attach which consists of nano-sized silver particles

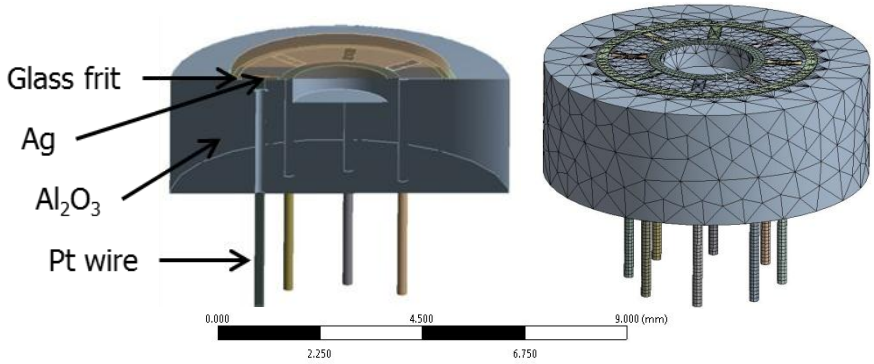
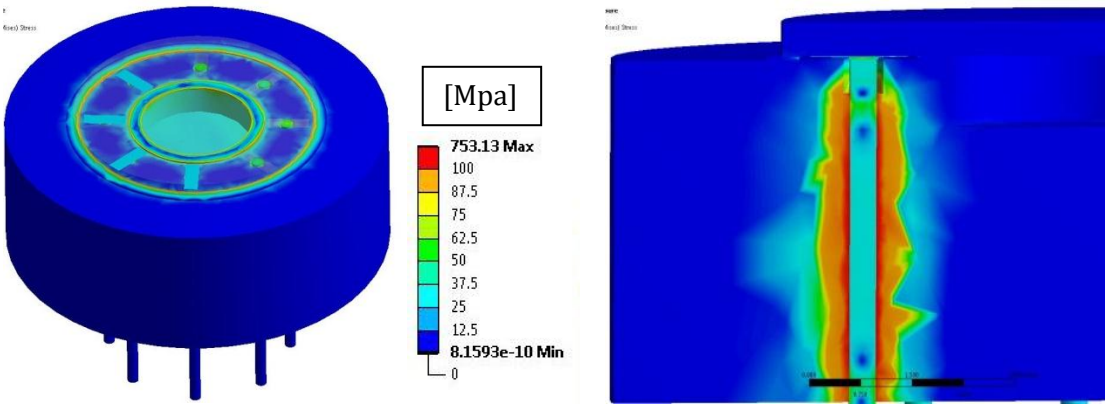


Figure 5.7: Packaging structure - 3D image of whole and cross-section isometric view

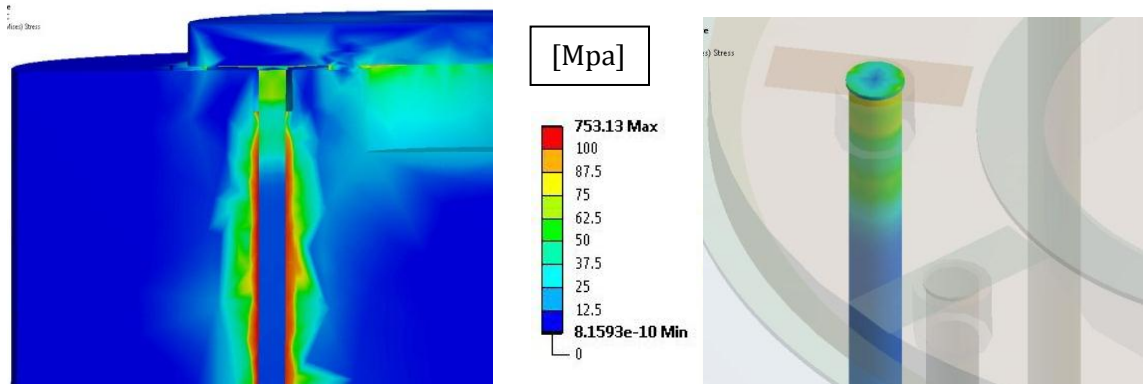
5.5 Thermo-mechanical simulation and thermal cycling

ANSYS workbench finite element method (FEM) simulator with the static and dynamic structural module has been used to evaluate thermally induced stress and strain in the solder joints and the glass frit which is used to seal the lid at high operating temperatures and different applied pressures. Figure 5.8a shows stress distribution in the package at 20 ^{0}C and 650 ^{0}C for applied pressure to membrane 10 MPa. The stress-free temperature was set to 850 ^{0}C since this is the temperature during the glass sealing process. The highest stress is located in glass frit and in interface between Ag and Pt wire. Figure 5.8b shows detail of stress distribution in cross-section view in the package at 20 ^{0}C and 650 ^{0}C for applied pressure to membrane 0 MPa and Figure 2.85.9a for applied pressure to membrane 10 MPa



a) b)

Figure 5.8:a) Equivalent stress at 20 °C and 650 °C, applied pressure to membrane 10 MPa; b) Cross-section view showing equivalent stress at 20 °C and 650 °C, applied pressure to membrane 10 MPa



a) b)

Figure 5.9: a) Cross-section view showing equivalent stress at 20 °C and 650 °C, applied pressure to membrane 10 MPa; b) Detail view of silver interconnect showing equivalent stress at 20 °C and 650 °C, applied pressure to membrane 0 MPa [95]

Figure 5.9b shows a close-up of strain in the Ag interconnects and Pt wire at 20 ^{0}C and 650 ^{0}C. The maximum strain in the Ag increases from 2.3×10^{-3} to 4,6×10^{-3}. Figure 5.10 indicates the stress distribution in a fictional contour through the package in the middle of an interconnect. Z=0 mm is at the top surface of the lid and Z=5.5 mm is the bottom of the Al_2O_3 holder. The highest stress is found in areas close to interfaces between Alumina, Platinum and Silver solder.

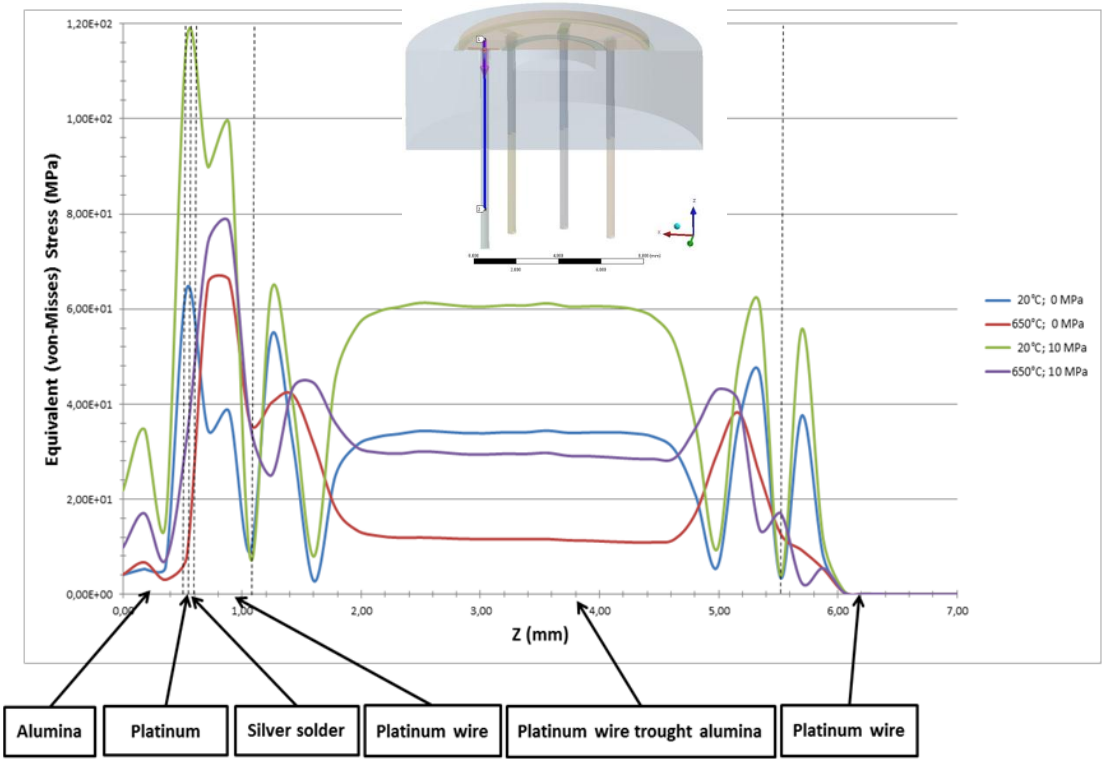
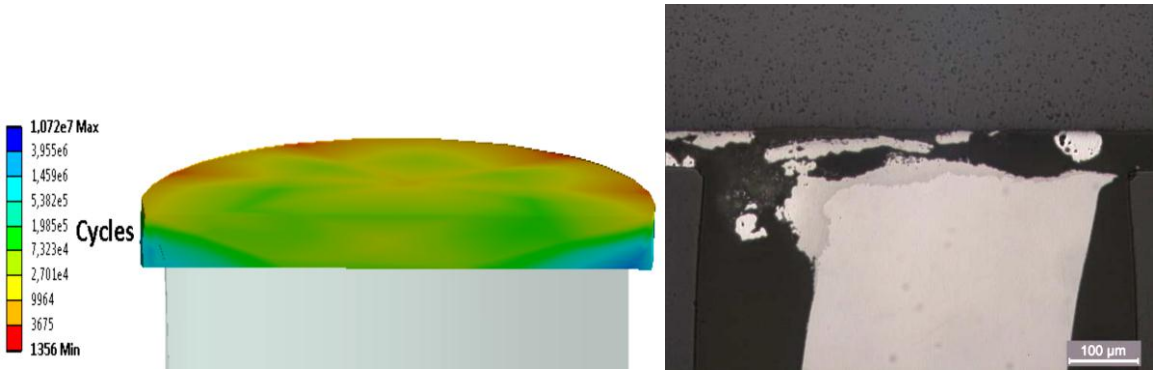


Figure 5.10: Modelled stress in the package along the z-direction of the centre of the platinum wires [95].

Life time of the package was calculated from thermal cycling simulation which was performed for temperature range 20-650 °C.

Figure 5.11a shows modelled lifetime distribution in the nano-Ag joints. The simulation model does not include porosity of the nano-Ag material, directional properties and temperature dependence because, to the best of our knowledge, these properties are not available in the literature. The simulation was calibrated by correction factors which were derived from the measurement results [95].



a) b)

Figure 5.11: a) Lifetime distribution in nano-Ag pad; b) Cross-section view of one of the interconnects after N=1250 cycles [95].

A test package was manufactured and thermally cycled to 650 ^{0}C (with the interval 30 min at 650 ^{0}C, 30 min at 20 ^{0}C, total time of one cycle 80 minutes)[30]. More details about measurement and life time validation can be found in [95]. Thermal cycling simulations indicate relatively high alternating stress at the interface between nano-Ag and Pt (64.91 MPa), which in the real structure leads to the delamination. This effect occurs after relatively small number of thermal cycles. Figure 5.11b shows cross-section view of one of the interconnects after N=1250 cycles[31]. Our simulation shows that minimum number of cycles when the cracks appear is around 1356.

5.6 Simulation of influence of the whole package on encapsulated sensor structure

Very important issue that must be considered in high temperature applications is the influence of the package on the sensor itself. The main aim of this work was numerical modelling of pressure sensor packaging system and evaluation of the package influence on encapsulated sensor structure at high operating temperatures and different applied pressures. Another objective was to understand how the mechanical stress and strain is distributed at elevated temperatures and investigate the reaction forces on the encapsulated sensor structure.

[30] Measured in Swerea IVF, Argongatan 30, SE-431 53 Mölndal, Sweden
[31] Photograph done in Swerea IVF, Argongatan 30, SE-431 53 Mölndal, Sweden

5.6.1 Pressure sensor packaging

Pressure sensor packaging assembly contain pressure sensor chip placed on ceramic holder attached within stainless steel main nut, copper distance ring placed between the ceramic holder and assembly nut to seal all parts (Figure 5.12).

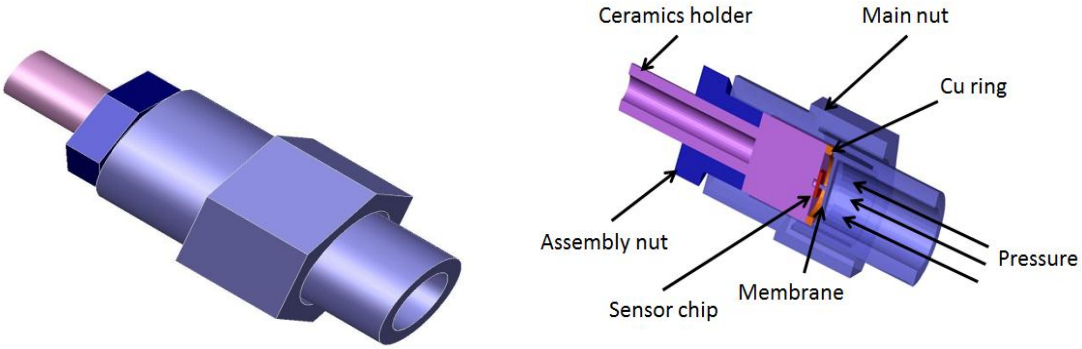


Figure 5.12: Packaging structure - 3D image of whole and cross-section isometric view

5.6.2 Simulation conditions and linkage connections

For mechanical simulations two types of models part interface connection have been used. Fixed connection was set between the main nut and the assembly nut crossing point, where the assembly is strong enough not to allow the mechanical movement of interface slices. The main nut and the assembly nut can be seen as one part. As well as mechanical interface between the sensor chip and the ceramic holder has been assumed to be bonded. All other part interfaces have been defined as free connection (frictionless). It means that these connected parts can move consecutively, and frictional forces are negligible. The linkage boundary conditions are shown on Figure 5.13.

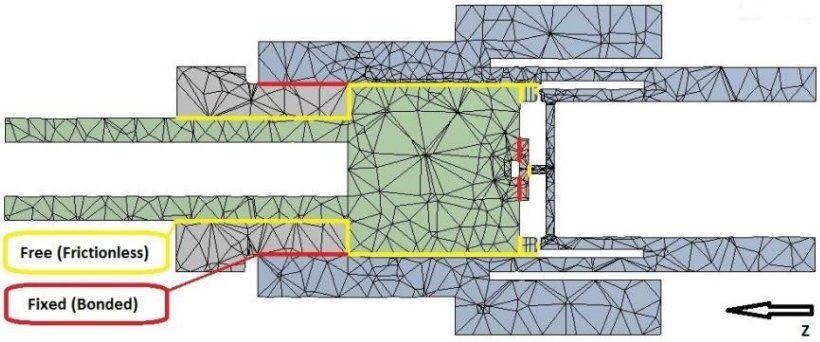


Figure 5.13: Types of linkage connections

Related displacement of sensor system free parts has to be taken into account. Every surface on free interface can be deformed independently. On the other hand some parts as ceramic

holder and the main nut must move together. The ceramic holder can be lifted by heating and may create a gap between the sensor chip and the main nut.

5.6.3 3D model and material properties

To decrease the number of nodes in simulation mesh, and therefore the computing time, the element distribution is adapted to the shape of the bodies. The number of elements is increased to capture small features in the model and also in place where high gradient of mechanical stress is expected. The designed model contains approximately 450,000 nodes. Material properties linked to used materials are summarised in Table 5-3.

Table 5-3: Material properties used in models

	Ceramic **Alumina**	Chip **Sapphire**	Nuts **Stainless steel**	Cu ring **Copper**
Density (kg/m^3)	3 890	3 980	7 750	8 300
Young's modulus (GPa)	375	370	193	110
Poisson's ratio (-)	0.220	0.275	0.310	0.340
Yield strength (MPa)	260		207	280
Therm exp. coef. TCE (10^{-6}/K)	8.40	6.60	1.70	1.85
Specific heat (J/kg.K)	880	761	434	385
Thermal conductivity (W/m.K)	35.0	41.9	60.5	400

5.6.4 Thermo-mechanical simulation

Figure 5.14 shows equivalent stress in the chip which is caused by different thermal expansion coefficients of the chip and ceramic when the sensor system is heated up to 1000 ^{0}C. Deformation is increased tenfold. We can see a gap between sensor chip and membrane, which may cause a problem detecting low value of pressure. Big value of thermal stresses on the interface between sensor chip and ceramics holder is caused by taking into account perfect contact between these those two part faces. In reality, TIM (Thermal Interface Material) layer is applied on the interface.

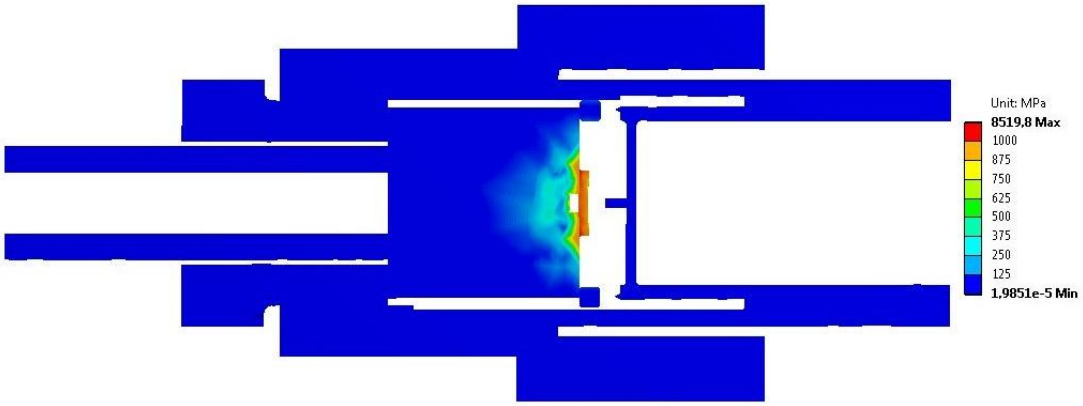


Figure 5.14: Equivalent stress 1000 °C, applied pressure to membrane 0 MPa

Thermo-mechanical parametric simulation has been used to find behaviour recognition of the sensor system in different body temperatures and pressure conditions. Few significant cases are shown on next figures. Figure 5.15 and Figure 5.16 shows an equivalent stress which acts on the chip and the membrane.

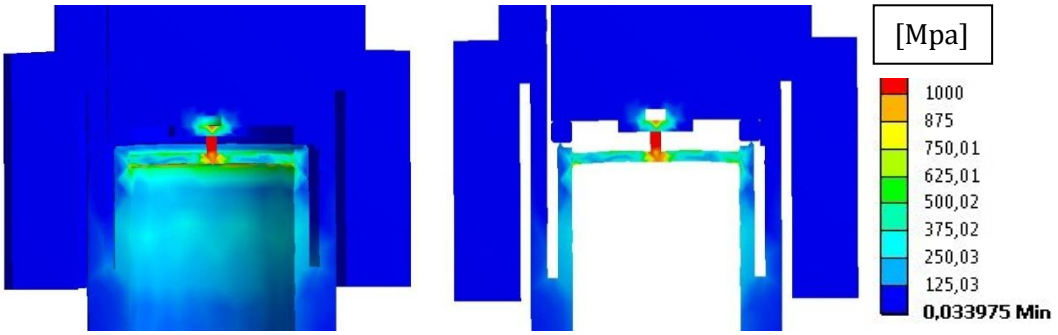


Figure 5.15: Equivalent stress 20 °C, Applied pressure to membrane 50 MPa

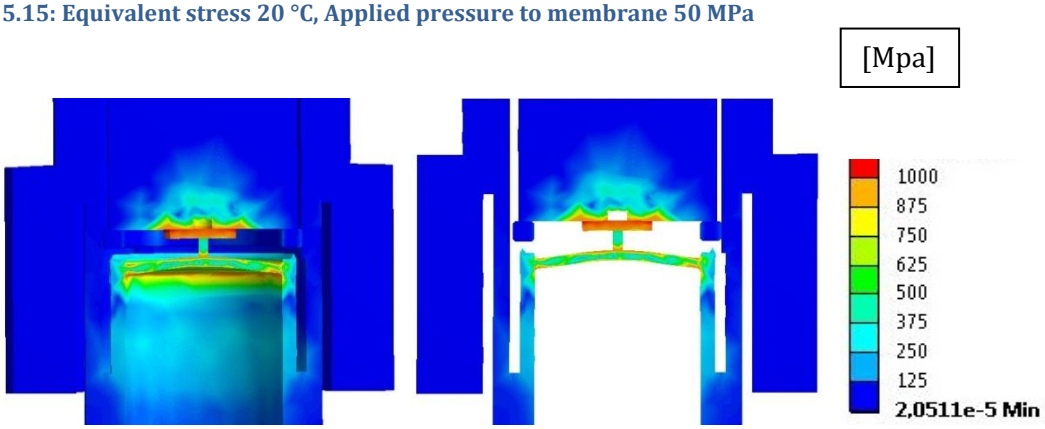


Figure 5.16: Equivalent stress 1000 °C, Applied pressure to membrane 50 MPa

The behaviour of the sensor system has been evaluated for different operating temperatures. The aim of this parametric simulation was to find the value of the gap between chip and tip of the membrane for different temperatures. Reaction force between the chip and the membrane at various thermal and pressure conditions has been also found. Results are shown on Figure 5.17.

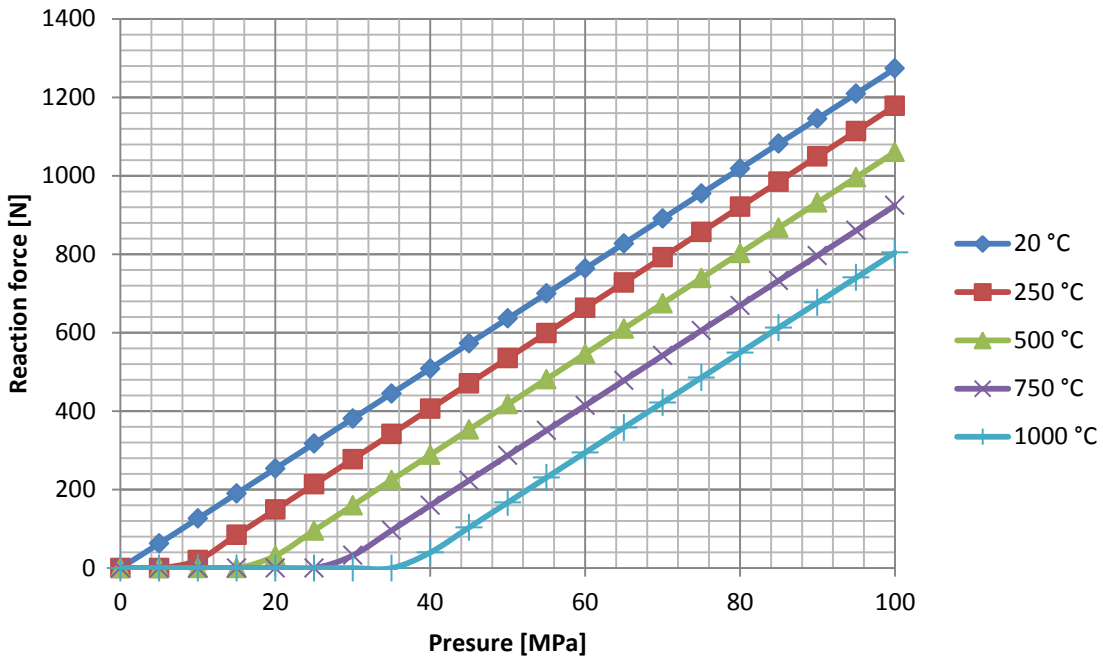


Figure 5.17: Graph of reaction with respect to pressure for different operating temperatures

When we apply a pressure to the membrane, the gap between chip and tip of the membrane is reduced. At 1000 °C the gap dismiss when the pressure of 38 MPa is applied to the membrane. We can conclude in this case that pressure in range 0 – 38 MPa will not be sensed by pressure sensor chip. When higher pressure than 38 MPa is applied, then the tip of the membrane is pressing the sensor chip. At present we are designing new package that will have not the dead zone of pressure sensing.

5.7 Summary and Conclusions

This section presents results achieved with the design of new high temperature robust pressure sensor and its package. My own research contribution has been summarized in chapter 5.1. These section collets published scientific results that was summarised in Table 5-1.

Electro-mechanical simulation of circular HEMT (C-HEMT) sensor structure was performed together with calculation of intrinsic stress, deflection, stress distribution and piezoelectric potential under mechanical load for different geometrical configurations. Influence of ZnO layer has been evaluated by simulation and also by experiment. The result show good agreement. Design of new Drumskin sensor has been introduces. This work was published in [87] and [86].

Evaluation of thermal and mechanical properties of new high temperature package design was performed. Thermo-mechanical simulations indicate that the maximum stress are located in

the interconnects and reaches 60 – 80 MPa, which exceeds the yield strength of silver. Metal interconnect have experienced a plastic deformation and creep during the cycling. Thermal cycling simulations shows relatively high alternating stress at the interface between nano-Ag and Pt (64 MPa), which in the real structure causes the delamination. Numerical modelling of thermal cycling shows minimum number of cycles is around 1356 (initiation of the cracks). This statement is supported by the thermal cycling measurement. For applications that have a short sensor life time this packaging approach well enough in its present state. This work was published in [95].

Influence of the package on the encapsulated sensor itself was evaluated. Simulation indicate possible problem of the package in the gap forming between chip and tip of the membrane when high temperatures are applied. Moreover, the gap size is a function of the temperature. This can be explained by the fact that ceramic sensor holder is expanding less than the main nut. The gap is formed between these initially clamping parts. The problem can be solved by replacing of the copper ring by a stainless steel ring, which has the same thermal expansion coefficient as the rest of the package.

Future work:

The results of thermal cycling are promising, however, further research will focus on new design where maximum stress in interconnects and between nano-Ag and Pt wire will be decreased.

6 IC design

This section presents my activities in the field of IC design. This additional chapter does not belong in the main section of presented work, which aims to seamlessly handle the problems of lifetime and thermal design of electronic systems. I've included this section for the reason that IC design research and teaching activities at the CTU belongs to an important part of my professional work. The main content of presented work was carried out during four months internship in Cadence, San Jose, CA and following three years design cooperation with Cadence RF R&D team (chapter 6.1).

A substantial part of my activities in IC design is leadership of PhD students with a focus on design of analog integrated circuits. In this field, we have close cooperation with companies as ST Ericsson, ASICentrum and ST Microelectronics that support our designs by technological realization. Brief summary of these activities is presented in chapter 6.2.

6.1 Wireless Design Flow for RF development Kit - R&D for Industry

This part has the objective to briefly summarize my internship activities performed in Cadence, San Jose, CA and next three years design cooperation with Cadence RF R&D team. An overview of the research activities with particular focus is given. Due to some confidentiality of R&D work for Cadence, not all details are shown.

6.1.1 Motivation and author contribution:

RF IC designs turn into more complex systems today and also contain AMS circuits as well. There is a need to have a complex design flow which begins on system design at a top level and move down to the circuit block level. To follow such a flow, RF IC must be built not only from circuit blocks but each designed block must have also behavioral model representation. Development of such design flow kit for RF circuits is today missing link in the chain.

My research and engineering contribution can be summarized in following research areas:

- *Design and development of Verilog A precise models for WLAN 802.11b/g transceiver. I designed several dozens of universal Verilog-A models for most of 802.11b transceiver blocks (VGA, LNA, VCO, Prescaler, DC cancelation block, Filters, Track & Hold amplifier,* Dual I/Q 8-bit pipeline ADC, *Phase Detector, Charge pump, Mixcer, DAC, etc.), testbenches for simulation in AMS environment, obtaining parameters from circuit simulations for behavioral model, etc.*
- *Co-working on the development of new design methodology for Wireless Design Flow (member of the six-member team)*

- *PLL Calibrated Behavioral Models generation using VCME (*Virtuoso Characterization and Modelling Environment) *templates, which enables to bridge transistor level simulations by automatically generated and calibrated Verilog-A models.*
- *Creating of functional verification for Top-down WLAN 802.11b/g transceiver design, on Development of new test benches system level and specifications set for RF ICs*
- *New VGA block design in 90 nm CMOS technology and development of characterization testbench*
- *ADC and DAC Verilog-AMS models (including 40 MSPS, INL, DNL, Pipeline delay, Track & Hold amplifier delay, gain error, clock booster)*
- *EVM Processing Verilog-A model*

6.1.2 State of the art

No longer does the traditional "bottom-up" design approaches of doing detailed transistor level design work well for large and complex designs. As the complexity increases a flow requires more organization and planning. This means an effective design flow has to have some connection from system level design to chip top-level and then down to specific circuit design together with IC layout and all its verification. Final layout needs parasitic extraction and re-simulations are necessary for RF design before final chip tape out.

This work was focused on development of Wireless Design Flow used to demonstrate the RF development Kit. A WLAN 802.11b/g transceiver was designed as the reference design. The design contains a 2.4GHz WLAN transceiver designed in Cadence's 90 nm CMOS Generic Process Design Kit (GPDK090). The transceiver is designed with the radio specifications set for the IEEE 802.11b and 802.11g standards. The core of the radio architecture consists of a direct conversion receiver and a direct I/Q up-conversion transmitter. The CMOS RF architecture is fully integrated and does not require any external RF passive devices. It means that IC includes also integrated inductors and capacitors. Active I/Q mixers provide a gain and necessary linearity for both Tx and Rx paths. An on-chip Voltage Controlled Oscillator (VCO) oscillates at harmonic frequencies of twice of desired channel frequency, to diminish DC offset issues due to direct conversion. A divide-by-2 prescaler subsequently divides the produced signal. A DC offset cancellation circuit is employed in the receive chain to dynamically filter out unwanted DC offsets, and programmable, analog baseband filters and VGAs complete the transceiver chain. The block diagram is depicted on Figure 6.1.

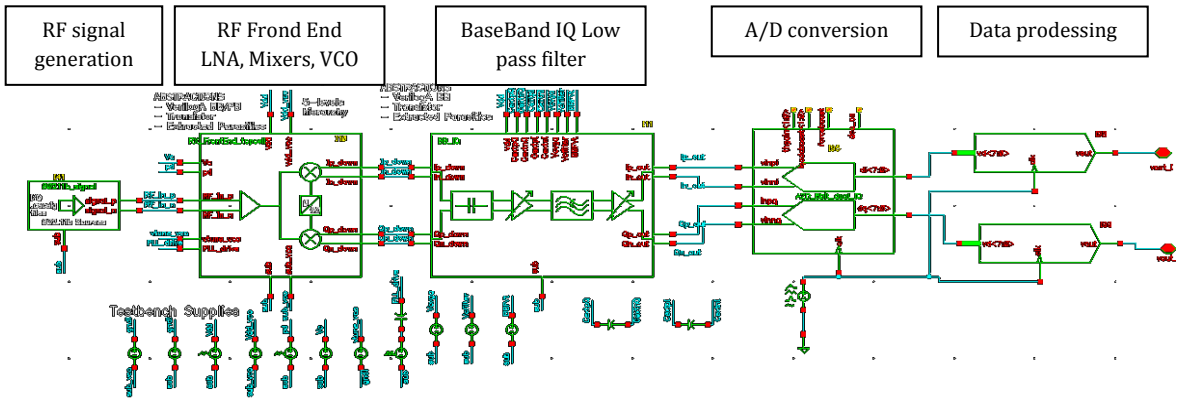


Figure 6.1: Top level schematic of 2.4GHz WLAN transceiver designed in Cadence's 90 nm CMOS Generic Process Design Kit

Top-down IC design (especially for the large designs) need a functional verification. This is the reason why behavioral modeling becoming very important in this process. Especially when is used early in the design and if behavior models are pin-to-pin compatible with the actual transistor-level circuit blocks. Models are integrated in simulations where mixed representation of both behavioral models and transistor-level abstractions are present. The main advantage is the usage of behavioral models for well-characterized circuits, while critical or newly created circuit blocks can be left on transistor-level for the best accuracy. This approach requires an analog mixed signal simulator such as Analog Mixed Signal Designer and Verilog-AMS modeling.

Simulation and verification process begins by setting up a simulation plan to what needs to be done. Usually it starts from specification which is transferred to the system design and functional modeling. This procedure is followed by top-level chip organization and block-level circuit design. Especially in case of large RF designs, transistor level simulation of whole circuit could take very long time. Where possible, behavioral models should be employed to speed up simulation time and minimize convergence.

As already has been mentioned above, Verilog-AMS modeling is one of the key steps in system level and top-down modeling. Behavioral AMS models that are pin compatible have been designed for all functional blocks of WLAN 802.11b/g transceiver described above (Figure 6.1) and for fully functional PLL blocks (Charge pump with differential inputs, Voltage controlled oscillator, Divider, Phase detector). PLL Calibrated Behavioral Models was designed in Verilog AMS environment and also generated using VCME (Virtuoso Characterization and Modelling Environment) templates which enable to bridge transistor level simulations by automatically generated and calibrated Verilog-A models. The main issue was to compere performance of new VCME environment with customized Verilog models. VCME uses custom templates for creation of analog model cells and generated model possibilities are sometimes limited. On the other hand Verilog-A models can be calibrated to capture nonlinear behavior into the model. Cell templates can be configurable for different block designs including inverted multi-stages outputs, reset inputs, reference voltages and currents, etc. Unfortunately, non-standard driving inputs cannot be usually taken into account.

Pin compatible Verilog-A models was also developed for whole PPL block. The PLL block diagram and test bench is illustrated below on Figure 6.2. VCO produces an output frequency that is divided by the Prescaler_Counter block in the feedback path producing divided signal for Phase-Frequency detector (PFD). The PFD continuously evaluates the phase difference between the reference signal and the divider output. This phase difference is transformed to an average charge pump current in Charge_Pump block. The loop filter transforms this current to vtune_vco signal which controls the VCO output frequency. When reference signal equals the divider output, the PLL is locked and output frequency of the VCO equals reference signal multiplied by division ratio of the Prescaler_Counter block. By varying the division ratio of the Prescaler_Counter block, the VCO can generate different output frequencies.

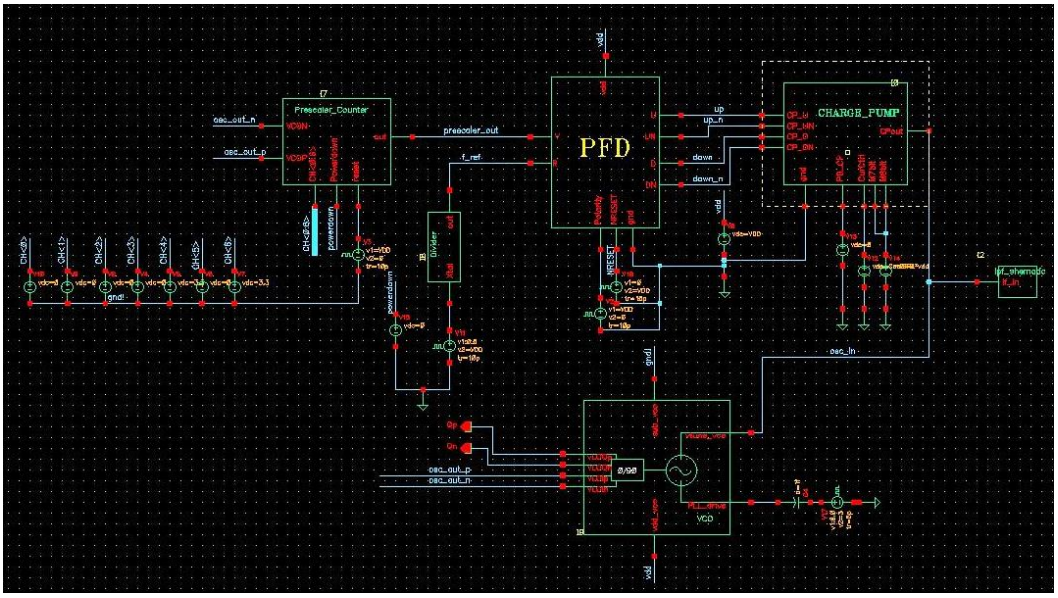


Figure 6.2: Schematic of PLL model Test benche

Pin compatible Verilog-A models were created for these blocks, which can be used as true replacement of transistor level blocks. The performance of all models was tested and calibrated according transistor level simulation result. Among all Verilog-A models mentioned above one example is described[32]

6.1.3 Dual I/Q 8-bit pipeline ADC Verilog-AMS model

Designed dual I/Q ADC consists from two 8-bit pipeline ADC connected in parallel. ADC has programmable output gain function integrated to its topology. The gain is set by *thgain* bus that allows setting of output amplifier gain to 0, 3.5, 6 and 9.5 dB. Clock signal can be internally boosted to higher level than Vdd for low voltage operation by setting *iqadcboost* signal. The boosted ration can be set from 1.1 to 1.4. The schematic of pipelined ADC is on Figure 6.3 including above mentioned signals. The Verilog-A model was designed to provide all non-idealities, which has been obtained from transistor level. On the other hand, the model is designed to be universal for further designs. Only input parameters have to be changed.

ADC Verilog AMS model Specifications and requirements:

- *40 MSPS, input dual I/Q differential signals*
- *Integral nonlinearity - INL*
- *Differential nonlinearity - DNL*
- *Pipeline delay*
- *Track & Hold amplifier gain*
- *gain error*
- *clock booster*
- *DC offset*
- *Rin, Rout*
- *Parameterized latency*

[32] Because of cconfidentiality reason, schematic on transistor level are not shown

Two differential ADCs have been used to ensure two dual channels for I and Q signal. Figure 6.3 shows Schematic of dual differential pipelined ADC.

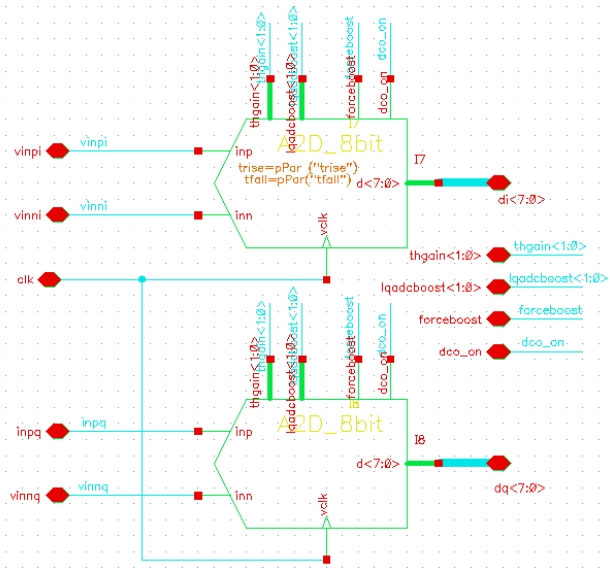


Figure 6.3: Schematic of dual differential pipelined ADC

ADC Verilog-AMS Model has following programmable parameters:

- ***DNL_min*** *minimal value for random DNL generation [LSB]*
- ***DNL_max*** *maximal value for random DNL generation [LSB]*
- ***INL*** *Incremental non Linearity [LSB]*
- ***INL_correction*** *parameter corrects the error caused by imprecise function approximation caused by 45 degrees tilting*
- ***dif_inp*** *differential voltage range [V]*
- ***tdel, trise, tfall*** *transitions times of the output digital signal [ns]*
- ***vlogic_high*** *Digital output voltage level – log 1 [V]*
- ***vlogic_low*** *Digital output voltage level – log 0 [V]*
- ***vtrans_clk*** *clock high to low transition voltage level [V]*
- ***TH_gain*** *Track & Hold Amplifier Gain [dB]*
- ***gain_error*** *Gain error of T&H amplifier [dB]*
- ***ICM_low*** *Minimal Input Common Mode Voltage [V]*
- ***ICM_high*** *Maximal Input Common Mode Voltage [V]*

These parameters can be derived from transistor level modeling.

6.1.3.1 Differential Nonlinearity Error Modelling:

Differential Nonlinearity Error (DNL) is defined as the maximum deviation between actual steps and the ideal steps. Here 'ideal' is not for the ideal transfer curve but for the resolution of the ADC. Ideally analog input voltage change of 1LSB should cause a change in the digital code. If an analog input voltage greater than 1LSB is required for a change in digital code, then the ADC has the differential nonlinearity error. DNL thus corresponds to additional maximum voltage that is required to change one digital code to the next digital code (Figure 6.4).

Parameters:

- ***DNL_min*** *= minimal value for random DNL genereation [LSB]*
- ***DNL_max*** *= maximal value for random DNL genereation [LSB]*

The value of DNL is computed by following equation that use random generation:

$$V_r[i] = \sum_{i=1}^{256} i \frac{V_{IR}}{256} Rand(-DNL/2, DNL/2) \qquad (6.1)$$

where V_{IR} is Input Voltage Range and $V_r[i]$ is New value of input voltage affected by DNL

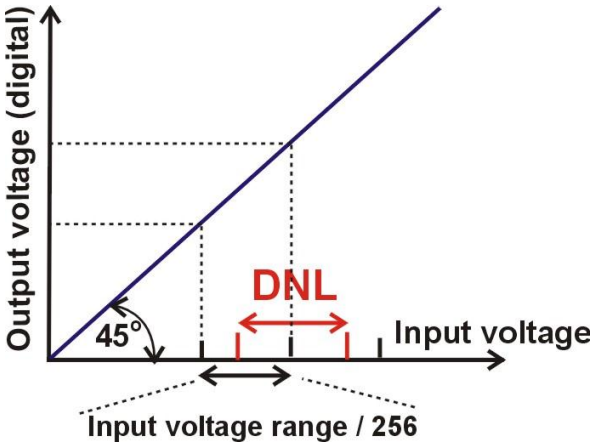


Figure 6.4: Differential Nonlinearity Error (DNL) is defined as the maximum deviation between actual steps and the ideal steps

Following list shows computing of DNL:

```
@ ( cross(V(vclk) - vtrans_clk, 1)) begin
   for (i=0; i<=255; i=i+1) begin
      rand_DNL = $rdist_uniform(seed, DNL_min/2, DNL_max/2);
      Vr[i] = (Vin_bit*i)+rand_DNL*Vin_bit+y *Vin_bit*INL_correction;
   end
```

Note: Input DNL is divided by 2 to ensure max DNL according specification. For example DNL spec=0.5LSB. If random function generates 0.5 for current state and the previous state was -0.5, then the DNL in this case in equals 1LSB.

Figure 6.5 shows ADC DNL test bench. Instance I1 (on the right) measures 8 bit ADC's DNL using a histogram method. 'vout' is sequentially set to 4096 equally spaced voltages between 'vstart' and 'vend'. At each different value of 'vout' a clock pulse in generated causing the ADC to convert this 'vout' value. The resultant code of each conversion is stored. When all the conversions is done, the DNL is calculated from the recorded data.

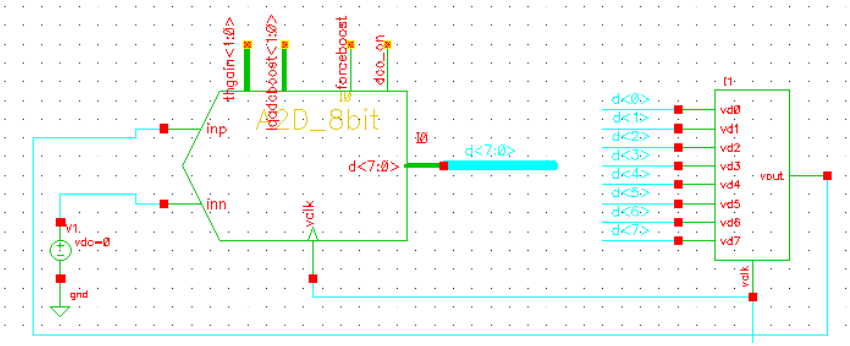


Figure 6.5: ADC DNL test bench

6.1.3.2 Integral Nonlinearity Error Modelling

Integral Nonlinearity Error is maximum deviation between any actual transition and the endpoint correlation line. The endpoint correlation line can be defined as the line on the A/D transfer curve that connects the first actual transition and last actual transition. INL is the deviation from this line for each transition. The endpoint correlation line thus corresponds to the actual transfer curve and has no relation to the ideal transfer curve (Figure 6.6).

Parameters:

- ***INL*** *= Incremental non Linearity [LSB]*
- ***INL_correction*** *= Actual INL value tends to be slightly larger than input INL. This is due to the error introduced by a simplifying approximation used in the calculation of the transfer function curve. The correction parameter allows the user to adjust for this error if needed.*

INL calculation theory:
The voltage transfer characteristic is approximated by parabolic function which has vertex in the middle of input voltage range and the y value of the vertex equals INL value. The value of DNL is computed by following equation that uses random generation:

$$Vr[i] = -\frac{n}{m^2}x^2 + \frac{2n}{m}x = -\frac{INL}{V_{IR}^2}\left(\sum_{i=1}^{256} i\frac{V_{IR}}{256}\right)^2 + \frac{2INL}{V_{IR}}\left(\sum_{i=1}^{256} i\frac{V_{IR}}{256}\right) \qquad (6.2)$$

where V_{IR} = Input Voltage Range and $V_r[i]$ = New value of input voltage affected by DNL

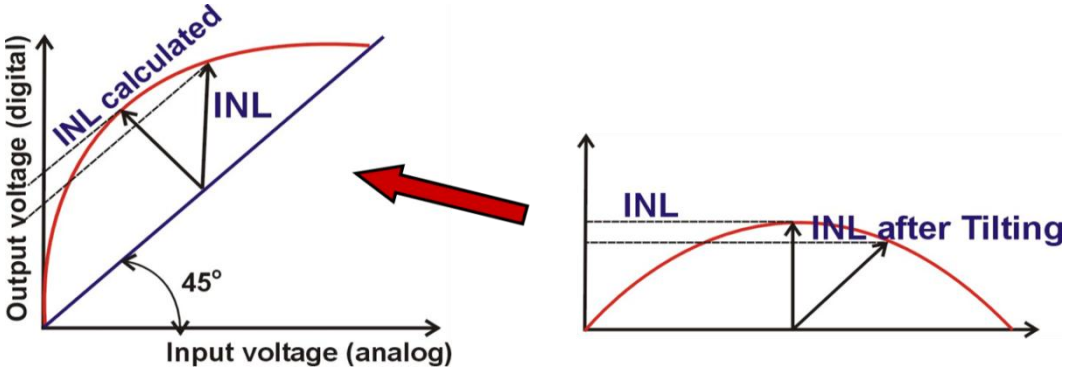


Figure 6.6: Integral Nonlinearity Error is maximum deviation between any actual transition and the endpoint correlation line

The INL value is affected by DNL because DNL randomly change the input voltage for each point of conversion. Following list shows computing of INL:

```
@ ( cross(V(vclk) - vtrans_clk, 1)) begin
    for (i=0; i<=256; i=i+1) begin
     x = i;
     y = -(n/(m^2))*(x^2)+((2*n)/m)*x;
     Vr[i] = (Vin_bit*i) +rand_DNL*Vin_bit+ y*Vin_bit*INL_correction;  end
```

Figure 6.7shows ADC INL test bench. Instance I6 (on the right) measures an 8 bit ADC's INL using a histogram method. 'vout' is sequentially set to 4096 equally spaced voltages between 'vstart' and 'vend'. At each different value of 'vout' a clock pulse in generated causing the ADC to convert this 'vout' value. The resultant code of each conversion is stored. When all the conversions have been done, the INL is calculated from the recorded data.

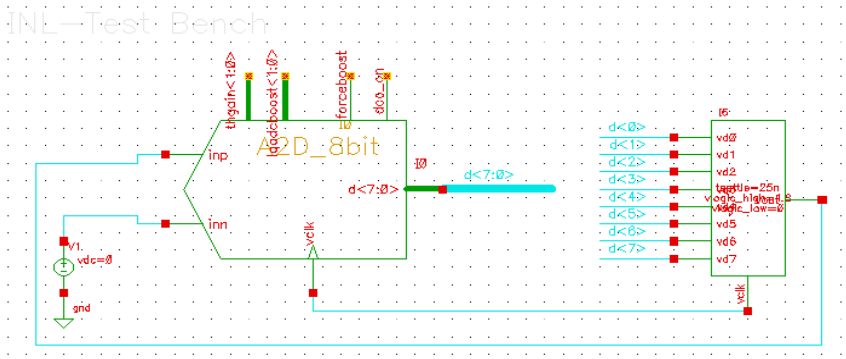


Figure 6.7: ADC INL test bench

6.1.3.3 Programmable gain and gain error of ADC

Many ADCs have programmable output gain function integrated to its design that is usually set by programmable inputs. In this design the gain is set by *thgain* bus (Figure 6.3) that allows setting of output amplifier gain to 0; 3.5; 6 and 9.5 dB. Differential analog inputs signal can be amplified by input Track & Hold Amplifier.

Another ADC error is caused by Gain error which is defined as deviation between the last actual transition and the last ideal transition. Following list shows application of gain error:

```
@ (cross (V(thgain[0]) - vtrans_clk, 0) or cross (V(thgain[1]) - vtrans_clk, 0)
        if ((V(thgain[0]) < vtrans_clk)&&(V(thgain[1]) < vtrans_clk)) begin
                $strobe ("Track & Hold Amplifier Gain = 0 dB");
                TH_gain_dB = 0;
        end
        if ((V(thgain[0]) < vtrans_clk)&&(V(thgain[1]) > vtrans_clk)) begin
                $strobe ("Track & Hold Amplifier Gain = 3.5 dB");
                TH_gain_dB = 3.5;
        end
        if ((V(thgain[0]) > vtrans_clk)&&(V(thgain[1]) < vtrans_clk)) begin
                $strobe ("Track & Hold Amplifier Gain = 6 dB");
                TH_gain_dB = 6;
```

```
        end
        if ((V(thgain[0]) > vtrans_clk)&&(V(thgain[1]) > vtrans_clk)) begin
                $strobe ("Track & Hold Amplifier Gain = 9.5 dB");
                TH_gain_dB = 9.5;
        end
```

6.1.3.4 ADC - Clock booster

Clocks can be internally boosted to higher level than V_{dd} for low voltage operation by setting *iqadcboost* signal. The Verilog AMS model display value of clock booster at any change of *iqadcboost* or *forceboost* signal. The boosted ration is set from 1.1 to 1.4.

```
@ (cross (V(lqadcboost[0]) - vtrans_clk, 0) or cross (V(lqadcboost[1]) - vtrans_clk, 0) or cross (V(forceboost) - vtrans_clk, 0) or initial_step("static") ) begin
if (V(forceboost) < vtrans_clk) begin
        if ((V(lqadcboost[0]) < vtrans_clk)&&(V(lqadcboost[1]) < vtrans_clk)) begin
                $strobe ("ADC Clock boost enabled - ratio 1.1");
        end
        else if ((V(lqadcboost[0]) < vtrans_clk)&&(V(lqadcboost[1]) > vtrans_clk)) begin
                $strobe ("ADC Clock boost enabled - ratio 1.2");
        end
        else if ((V(lqadcboost[0]) > vtrans_clk)&&(V(lqadcboost[1]) < vtrans_clk)) begin
                $strobe ("ADC Clock boost enabled - ratio 1.3");
        end
        else if ((V(lqadcboost[0]) > vtrans_clk)&&(V(lqadcboost[1]) > vtrans_clk)) begin
                $strobe ("ADC Clock boost enabled - ratio 1.4");
        end
else $strobe ("ADC Clock boost not enabled...");
end
```

6.1.3.5 Data latency computation- 5 cycles

There are five registers to store converted output data to simulate data latency. Each clock cycle the data are shifted from lover register one upward:

```
@ ( cross(V(vclk) - vtrans_clk, 1)) begin
  generate i(`HIBIT,0) begin
        reg5[i] = reg4[i];                      // Data latency computation
        reg4[i] = reg3[i];
        reg3[i] = reg2[i];
        reg2[i] = reg1[i];
        end
end
generate i(`HIBIT,0)                           // analog to digital conversion
reg1[i] = transition( vlogic_high*(!(!(adcout&(1<<i)))) +vlogic_low*(!(adcout&(1<<i)))
                , tdel, trise, tfall );
 generate i(`HIBIT,0)                           // Output voltage assignment
 V(d[i]) <+ reg5[i];
```

The ADC model uses more than ten parameters that have to be set. Values of these parameters could be obtained from transistor level testbench when the model is used to replace the transistor level circuit. The model could be used also in system level behavioural modelling. Here the designer can play with defined parameter in order to get more insights whole system behaviour.

6.1.4 Summary of Wireless Design Flow

Using developed behavioural models we can dramatically speed up design verifications of new blocks for RFIC design where simulations on transistor level run for very long time and sometimes become more difficult to converge. Verilog-AMS models were created to achieve a desired external circuit behaviour which corresponds to transistor level. Models are used to represent a certain circuit block on top-level behaviour. However, they can also replicate transistor device level characteristics. Models can be as complex as necessary but more complicated models can tend to have the same simulation overheard as regular transistor device models. It is always important to consider what trade-offs are important and necessary before constructing the model. At this point we were quite successful. Designed model has to be checked and compared with transistor level simulations. Model placed in the same testbench runs approximately two of three orders faster than transistor level does.

6.2 IC design – PhD students leadership

At this point I would like to mention my PhD student leadership activities in the area of IC design that form at the moment a significant part of my work on CTU. This session shows a brief description of interesting PhD themes that were created on the commercial IC companies R&D requirements. Most significant cooperation at this level has been established with ST Ericsson, ST Microelectronics and ASICentrum companies. Following text states ongoing activities.

6.2.1 Optimization tool for analog circuit design

PhD student Ing. Miroslav Kubař (fourth year)

The research in this field is focused on development of a new optimization tool for analog circuit design. Proposed tool is based on the robust version of the differential evolution optimization method. Technology corners as temperature, voltage and current supplies drifts are taken into account during the optimization that certifies robust "ready for the layout" circuit. New optimization tool has been implemented into the Cadence analog design environment to achieve very short setup time of the optimization task. The tool is universal and can optimize most of basic analog circuits as OTAs, voltage regulators, current sources, operational amplifiers, etc. The design automation procedure has been enhanced by optimization watchdog to control optimization progress. The optimization shall be usable in IC research and industry design work to save most of the design time of generic circuits. The optimization algorithm was successfully tested on several design examples (various OTA and voltage regulator architectures).

Integration of the optimization tool to Cadence analog design environment was implemented by SKILL language. Ocean scripting language has been used to perform algorithms of the optimization tool and to run simulations of the optimized circuit. The proposed optimization tool uses the simulation approach with real device models (AMIS 0.35 um technology) but any other design kit can be used. Developed optimization tool is very universal and can be used to optimize circuits of many types and architectures.

6.2.2 Design of capacitor-less LDO regulator in CMOS technology

PhD student Ing. Vladimír Molata (second year)

Good power management design of modern ICs is one of the main research topics today. Increasing priority of optimized power management and consequently prolonging battery life of mobile devices is one of key reasons for chip design modifications towards SOC (System on Chip) solutions where power management is critical.

This research work provides solution for Low Drop Out (LDO) voltage regulator designed for System on Chip (SOC) applications. A voltage regulator of Low Drop Out (LDO) type makes a small family of circuits that fit in to power management. Its main usage is in power supply

where low noise and high accuracy of voltage are extremely essential. LDO regulator produces constant output voltage, independent of change in load or change of battery voltage.

Classic power management system contains several LDO regulators, which provide specific voltage required by individual subsystems. For conventional regulators external capacitors (in the order of microfarads) are used. Main disadvantage of external capacitor is occupation of valuable space and requires additional pins of a chip.

This work is focused on capacitor-less LDO regulator development in the field of SOC applications, which brings solution for reduction external capacitor. The other research goal is decreasing of LDO regulator's consumption to levels below 50mA. In order to achieve the good transient characteristics of capacitor-less regulator, the circuit must be improved to compensate lack of capacity of eliminated external capacitors. This can be achieved by realized by extremely fast feedback loops that become critical for capacitor-less regulators. Final design should be robust enough to be widely applicable.

6.2.3 Design and validation of an SMPS power distribution network

PhD student Matthieu Thomas, MSc (second year)

For modern RF Power Amplifier SMPS (switched mode power supply), size and number of pins has become one of the main constraints. Common practice in Step-Down DC-DC converter is to split the control and power part supplies by having dedicated pin/ball for each part. This research work is focused on reduction of the number of required pins. New IC design solve that problem and show that it is possible to share a single supply pin for powering both the output stage and the sensitive control part of a Step Down converter. Sharing of the positive supply pin allows the circuit to fit in a WLCSP 9 balls package of 1.2mm x 1.2mm.

There are many problems that have to be solved. An SMPS circuit is a main source of noise for itself and the components around it. By sharing the supply pin for control and power, the noise immunity becomes even more critical. The target of this this research work is to propose an original on-chip supply filtering strategy. This strategy allows the analog control part to keep its performances despite the noisy supply environment.

By careful partitioning of analog and digital blocks, it is possible to apply an RC filtering on the internal supply of an integrated circuit. This filtering allows sharing the same ball for the supply of sensitive analog control part and noisy power stage. This approach has been validated in silicon chip. In order to validate the stability of the SMPS on its whole operational range an original measurement method has been developed. This method allows first to get a picture of the stability on a large operational range and second to make comparative study when changing measurement parameters. This tool has been for us the key in identifying the issue in the first version of the silicon. The research work at this field shows very promising results.

6.2.4 ESD MOSFET model fitting by differential evolutionary optimization

PhD student Ing. Tomáš Nápravník (second year)

The electrostatic charge creates a major danger for ICs reliability and lifetime since the beginning of history of a high integration. The rapid development of IC technologies pushes the dimensions of CMOS devices into deep-submicron area, where especially gate oxides of input buffers are extremely thin and can be easily damaged by high electric field. The goal of ESD protection designers is to develop countermeasures, able to divert the charge away from the sensitive internal circuits and to clamp the resulting over-voltage bellow oxide-breakdown level.

However, standard model libraries of MOS transistors based on Berkeley short-channel IGFET Model (BSIM) or EKV (initials of its developers C. C. Enz, F. Krummenacher, and E. A. Vittoz) models are unable to simulate appropriate behavior of ESD protection devices. Research in this field is very relevant. The main goal of this work is to develop an optimization algorithm based on Differential Evolution method to automatically fit the measured data from test chip to the appropriate electrostatic discharge (ESD) model without the need of manual model-parameters tuning. In contrast with proposed method this traditional approach can be very time and resource consuming. Proposed method brought the first success by ability to fit generic the model to the piece-wise linear I-V characteristic to be able to simulate HBM pulse response and resulting snapback of the model connected as gate-grounded NMOST. The process lasted less than 5 hours of fully automatic optimization process. This shows that this approach is feasible and can be used as alternative for time and resource consuming manual model calibration. Future development will be focused on optimizing the differential evolutionary optimization algorithm parameters. Using additional optimization methods we can increase optimization efficiency. NMOST model will be modified to comply with technology used for fitting and amended by additional effects that were omitted during optimization method development.

7 General conclusions and future perspectives

The research work presented in this habilitation thesis is characterised by a cross-disciplinary approach that brings together experimental, theoretical, and computer modelling techniques. The work provides a wide-ranging summary dedicated to the design, modeling and characterization of thermally affected electronic components and sensors. It gives a comprehensive view of thermo-mechanical phenomena, design aspects and optimization of new electronic systems and sensor structures together with estimation of system lifetime and effects leading to a failure.

For the scientific community, the most important contributions of this research can be summarised in following points:

- *Thermal and thermomechanical numerical modelling and characterization of solid state lightening (SSL) LED Lamp(published in* [2] *and* [5]*);*
- *Accurate 3-D modelling of several LED board technologies mainly concentrating on thermal, thermo-mechanical evaluation and lifetime prediction of LED boards, definition of critical parts from reliability point of view and proposal for new designs (published in* [3]*);*
- *Development of accelerated characterization testing methods for LED boards. New method should replace traditional thermal cycling of power cycling characterization test. The method is still under development, but first promising results have been published. This new testing method can dramatically speed up testing process keeping testing accuracy in the range of 20% (estimation that will be proved by testing of LED board samples (published in* [1]*);*
- *Design, modelling and characterization of new micro machined GaAs and GaN based high temperature hot plate thermal converters, which are expected to be used for metal oxide gas sensors that can detect various gases (CO, H_2, NOx, hydrocarbons). New solution increases sensitivity (through the use of new materials as GaAs and GaN) and decreases power consumption, due to the miniaturization using MEMS technology (published in* [73] *and* [74]*);*
- *Design and optimization of micromechanical GaAs based Microwave Power Sensor thermal converter topology in terms of the temperature distribution and optimization of the dynamic behaviour of the RFMPS system with respect to changes of the input RF power dissipation, which is generated by integrated HEMT transistor. Numerical modelling results were compared with the experiment and are in good agreement (published in* [82] *and* [81]*);*
- *Modelling of ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) as a new stress sensor to be potentially applied for dynamic high-pressure sensing (published in* [87] *and* [86]*);*
- *Design and accurate numerical modelling of Drumskin pressure sensor packaging system and thermomechanical evaluation of mechanical stresses induced in the solder joints and*

the glass frit that is used to seal the pressure sensor chip at high operating temperatures and different applied pressures (published in [95]*);*

- *Design and development of Verilog-A precise models for WLAN 802.11b/g transceiver;*
- *Co-working on the development of new design methodology for Wireless Design Flow and Creating of functional verification for Top-down WLAN 802.11b/g transceiver design, and development of new test benches on system level and specifications set for RF ICs.*

7.1 Future research and possibilities for improvements

A lot of efforts have been made to achieve the research results described herein with thoroughgoing drive. The research and development of new things are encouraging specifically because it never ends. There always appears a new unexplored path. And so it is with this work.

CSSL project focused on development of new 806 lumen LED lamp is still on going. As I've already pointed, new accelerated characterization methods for SSL LED boards (Chapter 2.6) seem to be very promising. Nevertheless, there is still a lot of work that continue to measure more LED board samples (not only of existing reference RF4 board, but also on newly designed LED boards). Another very promising research result that should be exploited more is to find a relationship between mechanical cycling and traditional thermal cycling that is given by accumulated creep strain or accumulated energy in solder joints.

Another progressing issue is the work on thermo mechanical and piezoelectric design of the new pressure sensor for harsh environment. We have shown that ZnO-passivated AlGaN/GaN-based circular high electron mobility transistor (C-HEMT) designed for new stress sensor has very good potential to be applied for dynamic high temperature pressure sensing. The pressure sensor has been evaluated in terms of applied mechanical load, harmonic analysis and piezoelectric response. First mechanical calculations have been performed on newly designed C-HEMT pressure sensor. Nevertheless, much more effort has to be paid to piezoelectric modelling of proposed structures. This should lead to design of final demonstrator, which will be technologically processed and measured. Further attention will be paid to the design of relevant packaging. The results of thermal cycling simulation and test of designed package are promising, however, further research is required to focus on new improved design where maximum stress in interconnects and between nano-Ag and Pt wire will be decreased.

In the field of IC design four research projects pointed in chapter 6.2 are on-going. These are carried out by team of my PhD students.

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Appendix I: Curriculum Vitae

Jiří Jakovenko

October 20, 2012

Department of Microelectronics
Faculty of Electrical Engineering
Czech Technical University
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Born on 10th July 1972 in Prague, Czech Republic

Work experience

Since 1999	**Assistant Professor and Research fellow** at the Czech Technical University, Faculty of Electrical Engineering, Department of Microelectronics Main responsibilities: Teaching (lectures, supervising and preparation of courses, PhD student supervision, etc.), research (work on several international projects, scientific papers writing, reviving, etc.),
Since 2000	**Computer administrator of the SUN Workstations and servers** at Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics Main responsibilities: Hardware and software installation and administration, Sun Solalaris, EDA software (Cadence, Synopsys, TCAD, Coventor Ware, …)
2005 - 2008	**External consultant and RF and Analog-Mix signal IC design engineer** at CADENCE Design Systems, Seely Ave., San Jose, CA, USA (Microelectronic, EDA Software developer) Main responsibilities: Design of analog and mix-signals circuits for 802.11 b, g transceiver
2005	**Wireless IC design engineer** at CADENCE Design Systems, Seely Ave., San Jose, CA, USA (four month internship) Main responsibilities: Development of RF design kit and design of Verilog-AMS models for 802.11 b, g transceiver
1990-1991	**Technical services for Building industry** at North Brick company, Tzaneen, South Africa Main responsibilities: Installing and servicing of processing machines

Education

1999-2004	**PhD degree in Microelectronics** at Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics, with thesis MEMS Structures for RF Power Measurement.
1991-1997	**MSc degree in Microelectronics** at Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics, with thesis Non-invasive Flow monitoring system.
1998	**International Business Program** - Six month study in under the frame European TEMPUS programme - European Business and Management at Hogeschool, Gent, Belgium

Research interests and scientific achievements

Microsensors and MEMS design (GaN, GaAs based Micromechanical Free Standing Hot Plates for Gas Sensors, thermo mechanical and piezoelectric design of the pressure sensor for harsh environment); Solid State Lamp design (design of new 806 lumen SSL retrofit lamp, thermal and thermo-mechanical numerical modelling of LED glow, design of new LED boards, development of new accelerated characterization methods for SSL LED boards, reliability and life time modelling); Analogue and Mix-signal Integrated Circuit design.
J. Jakovenko is author and co-author of many scientific publications: 7 journal papers with impact factor, co-author of chapter in Springer book (MEMS/NEMS), 30 publication are registered in WoS.

Language skills

Czech (native), English (fluent), Russian (good), German (elementary).

Professional activities

Research activities in the frame of several international and national projects in the area of applied electronics, MEMS and Microsystems design. Some selected projects: CSSL ENIAC Project (7-FP EU) – „Consumerizing Solid State Lighting“ – Design and thermal management of LED light bulbs; MorGaN – Project (7-FP EU) – „Materials for Robust Gallium Nitride“; NATO Science for Peace - development of RF Power Sensor Microsystem; PolyApply Project (6-FP EU) – Design of polymer based sensors and electronics circuits; Target Project (6-FP EU) – “Top Amplifier Research Groups in a European Team“, - microwave amplifier research; IMINAS Project GAČR GA102/09/1601 – „Intelligent micro and nano structures for micro-sensors; and many others.
Reviewing for scientific journals like Microelectronics Reliability, Radioengineering, Electron Device Letters, Reviewer for conferences like IMAPS EDS
Since 2004 Leader of IC and MEMS design laboratory at CTU FEE, Department of Microelectronic
Organization of European IC Design course IDESA and European MEMS Design course STIMESI
Member of the management board of department of Microelectronics, member of CTU FEE committee for instrumentation; 2001-2004 member of academic senate at CTU FEE

Pedagogical activities

Undergraduate and postgraduate level courses in IC design and Microelectronics (VLSI design and technologies, Design of integrated systems, Integrated system on Chip, Practice in IC design, Design of VLSI, IC design for informatics, Integrated design structures, New trends in electronics, Microelectronic, Electronics a microelectronics, Sensor systems).
Deputy of board for defence theses and final state examination in Electronics, CTU; Member of board for defence theses and final state examination, University of Technology Brno.
Member of the committee for PhD degree defence board in "Electronics" - CTU Prague
Currently supervisor of 7 PhD students, leader of about 20 Master students that have successfully defended the final thesis.

Appendix II: List of publications related to the habilitation work

[1] Jakovenko, J. - Formánek, J. - Janíček, V. - Husák, M. - Werkhoven, R.: High Power Solid State Retrofit Lamp Thermal Characterization and Modelling. Radioengineering. 2012, vol. 1, no. 21, p. 231-238

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[3] Perpina, X - Werkhoven, R. - Jakovenko, J. - Formánek, J. - Vellvehi, M. - Jordà, X. - Kunen, J. - Bancken, P. - Bolt, P.J.: Design for reliability of solid state lighting systems. Microelectronics Reliability. 2012, vol. 9-10, no. 52, p. 2294-2300. ISSN 0026-2714

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[8] Jakovenko, J. - Formánek, J. - Perpina, X - Werkhoven, R. - Kunen, J. - et al.: Thermo-mechanical evaluation and life time simulation of high power LED lamp boards. In EuroSimE 2012 - Proceedings of the conference www.eurosime.org. Porto: IEEE, 2012, vol. 1, p. 1-4. ISBN 978-1-4673-1511-1.

[9] Brinkfeldt, K. - Formánek, J. - Laposa, A. - Jakovenko, J. - Adolfsson, E. - Johander, P.: Simulations of High Temperature Pressure Sensor Packaging and Interconnections. In EuroSimE 2012 - Proceedings of the conference www.eurosime.org [CD-ROM]. Porto: IEEE, 2012, vol. 1, p. 1-4. ISBN 978-1-4673-1511-1.

[10] Pardo, B. - Gasse, A. - Fargeix, A. - Jakovenko, J. - Werkhoven, R. - Perpiñà, X.- Van Weelden, T.- Bancken, P.: Thermal Resistance Investigations on New Leadframe-Based LED Packages and Boards. In EuroSimE 2012 - Proceedings of the conference www.eurosime.org. Porto: IEEE, 2012, vol. 1, p. 1-4. ISBN 978-1-4673-1511-1.

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Appendix III: Projects

The following list summarises main projects where I have been working on

EU Projects:

- **CSSL ENIAC** - Project (7-FP EU) – „***Consumerizing Solid State Lighting***"; Period: 2010 - 2012; Ext. No: 120219 – The project aims to demonstrate affordable smart SSL light-sources for consumers via both technology and application routes. The proposed CSSL project works vertically across the entire value chain from LED die, lightsource, consumer luminaires, controls and dimmer to partnerships with utility companies in order to bring SSL retrofit product to European consumers with a substantial cost reduction.

- **MorGaN** – Project (7-FP EU – 2008-2011) – „***Materials for Robust Gallium Nitride***" – Research in the field of new robust pressure sensors for extreme conditions especially high temperature. The project takes advantage of the excellent physical properties of diamond and gallium nitride (GaN) based heterostructures.

- **NATO Science for Peace** international project focused on ***development of RF Power Sensor Microsystem***. Within this project he carried out research in 3D thermal and thermo-mechanical design and modelling of Micromechanical Thermal Converter MEMS device.

- **PolyApply** Project (6-FP EU) – simulation and modelling of polymer based sensors and electronics circuits.

- **Target Project** (6-FP EU) – "***Top Amplifier Research Groups in a European Team***", microwave amplifier research.

GAČR:

- ***Intelligent Micro and Nano Structures for Microsensors Realized with Support of Nanotechnology*** (2009-2013, GA102/09/1601)- The project is targeted on research in the field of new types of microstructures with carbon diamond layers and promising materials from $A^{III}B^{V}$ group, for using in industry, living environment protection, biomedicine and measurement systems.

- ***Micro and Nano Sensor Structures and Systems with Embedded Intelligence*** (MINASES) (2006-2008, GA102/06/1624)

- ***Smart Microsensors and Microsystems for Measurement, Control and Environment*** (2003-2005, GA102/03/0619)

- ***Integrated Intelligent Microsensors and Microsystems*** (2000-2002, GA102/00/0939)

CTU Projects and grants

- ***Development of Smart Devices and Systems in the Field of Microelectronics, Nanoelectronics and Optoelectronics*** - SGS10/280/OHK3/3T/13 2010-2012 - The project supports selected expert activities sold by doctoral and master students in the field of micro and nanostructures, microsystems and microsensors, chip integration, the use of new materials, including optoelectronic integrated systems. Development of optimization tools for designing analog integrated circuits in CMOS technology in Cadence design environment. Activities are focused on design of the voltage comparator with very low-power consumption, design capacitor-less DC-DC converters, design of intelligent sensor chip for wireless sensor data transfer and linearization, design of MEMS structures for autonomous power supply for microsystems and further optimized design of analog integrated circuits.

- ***IBAD (Ion Beam Assisted Deposition)*** *Project of CTU*

Other

- ***Miniature intelligent system for analyzing concentrations of gases and pollutants, particularly toxic*** (2010-2015, MV0/VG - Ministry of Interior) – Project deals with research and development of intelligent miniature analyzing system of gases concentrations and hazardous substances with sensor matrix arrangement. The solution is based on smart sensors and electronics, MEMS technology. Wireless communication allows information transferring; system is designed to protect people and assets, helps to increase safety. The novelty of the project is the application of emerging sensor technologies with smart decisions, variability and compactness.

- ***Cadence tutorial.*** MŠMT – project of FRVŠ - 2008; Ext. No: 2566 G1.

- ***EDA laboratory for IC design and Electronics*** – Project of FRVŠ, 2009; Ext. No: 1193Ab

- ***CEMIS – Centre of microsystems*** - 1997-2000, Project of MŠMT; Ext. No: VS 97046

Appendix IV: Internships

1998 - International Business Program - Six month study in under the frame European TEMPUS programme; European Business and Management, Hogeschool, Gent, Belgium

2005 - Three month post-doctoral intern; IC Design, CADENCE Design Systems, Seely Ave., San Jose, CA, USA