Master Thesis

Czech
Technical
University
in Prague

F3

Faculty of Electrical Engineering
Department of Measurement

Software Support for Parallel ADAS Applications on Pre-development Version of the Aurix TC4

Bc. Lukáš Bielesch

Supervisor: Ing. Radek Olexa
Subfield: Cybernetics and Robotics
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MASTER‘S THESIS ASSIGNMENT

I. Personal and study details

Student's name:	**Bielesch Lukáš**	Personal ID number:	**465960**
Faculty / Institute:	**Faculty of Electrical Engineering**		
Department / Institute:	**Department of Measurement**		
Study program:	**Cybernetics and Robotics**		
Branch of study:	**Cybernetics and Robotics**		

II. Master’s thesis details

Master’s thesis title in English:

Software support for parallel ADAS applications on pre-development version of the Aurix TC4 microcontroller

Master’s thesis title in Czech:

Softwarová podpora pro paralelní ADAS aplikace na vývojovém vzorku mikrokontroléru Aurix TC4

Guidelines:

1. Familiarise with pre-development samples of Infineon AURIX™ TC49A MCU and its new Parallel Processing Unit (PPU).
2. Develop basic software support (boot code, IRQ handling, …) for the Infineon AURIX™ TC49A microcontroller.
3. Explore the standalone computing cluster with vector processing capabilities (PPU). Demonstrate the advantages/disadvantages of offloading the tasks from TriCore to the vector processor.
4. Provide integration of the PPU capabilities with other tools such as MATLAB/SIMULINK with MetaWare toolbox, the Neural Network Software Development Kit (NN SDK) etc. The aim is to speed up the development process of PPU applications.
5. Develop a set of automotive-related applications demonstrating effective application vectorisation. The applications will use both the basic software and the PPU support. The applications will work on the virtual model of the CPU and the actual pre-development hardware samples.

Bibliography / sources:

[1] AURIX™ TC49x User manual V0.73. Infineon Technologies AG. 01-12-2021
[2] Effective Vector Programming Guide MetaWare for AURIX™ TC4x. Version 4222-013. Synopsys. September 2021
[3] Machine Learning and Embedded Computing in Advanced Driver Assistance Systems (ADAS). September 25, 2019. ISBN 978-3-03921-376-4 [online]. Available from WWW: https://www.mdpi.com/books/pdfview/book/1573

Name and workplace of master’s thesis supervisor:

Ing. Radek Olexa HighTec EDV-Systeme GmbH

Name and workplace of second master’s thesis supervisor or consultant:

Date of master’s thesis assignment: **10.02.2022** Deadline for master's thesis submission: ___________

Assignment valid until:
by the end of summer semester 2022/2023

Ing. Radek Olexa Supervisor’s signature	Head of department’s signature	prof. Mgr. Petr Páta, Ph.D. Dean’s signature

III. Assignment receipt

The student acknowledges that the master’s thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the master’s thesis, the author must state the names of consultants and include a list of references.

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Date of assignment receipt	Student’s signature

Acknowledgements

I would like to express my sincere gratitude to HighTec EDV Prague headed by my supervisor Ing. Radek Olex, for the willingness and time he gave me during the development of this thesis as well as the opportunity to work with state-of-the-art technologies. Secondly, I would like to thank my colleagues whose expertise greatly facilitated the process of understanding the automotive AURIX architecture. Special thanks go to my brother Marek and my parents for their unconditional support throughout my studies.

Declaration

I declare that the presented work was developed independently and that I have listed all sources of information used within it in accordance with the methodical instructions for observing the ethical principles in the preparation of university theses.

Signature:

In Prague, May 20, 2022

Abstract

To meet the combination of performance, ASIL safety standards and cost-effectiveness, many new architectures in the automotive industry are adopting a heterogeneous design combining scalar, and vector DSP processors. The aim of this thesis is to create a set of tools and functions to support the new TC4xx family of microcontrollers adopting the heterogeneous design. Furthermore, high-level tools are analyzed and used to enable accelerated development processes.

The scope of this thesis further includes an implementation of basic software support consisted of multi-core booting, initialization of essential peripherals, easy-to-use registration of interrupt service routines and printing to UART with multi-core synchronization. Further it contains, the inter-processor communication allowing data exchange between individual cores, and thus offloading computationally intensive operations on a parallel computing unit.

To demonstrate the capabilities of the vector processor, two experiment applications were developed - a Kalman filter-based application to estimate the speed of the lead vehicle and a convolutional neural network trained to recognize the drowsy driver.

The correct functionality was verified by running the programs in a simulation environment and subsequently on the first prototype of the evaluation board.

Keywords: Aurix TC4xx, Pre-development, BSP, SIMD, ADAS, Model-based design, Embedded code generation, Kalman filter, Convolutional neural network

Supervisor: Ing. Radek Olexa

Abstrakt

V mnohých nových architektúrach v automobilovom priemysle sa vyuºíva heterogénny dizajn kombinujúci skalárne a vektorové DSP procesory s cie©om splni´ výkonové kritériá, bezpe£nostné normy ASIL a kompetitívnu cenu. Cie©om tejto práce je vytvori´ súbor nástrojov a funkcií na podporu novej rodiny mikrokontrolérov TC4xx s heterogénnym dizajnom. Okrem toho sa analyzujú a vyuºívajú vysokoúrov¬ové nástroje, ktoré umoº¬ujú zrýchli´ vývojové procesy.

Táto práca ¤alej zah¯¬a implementáciu základnej softvérovej podpory pozostávajúcej z bootovania viacerých jadier, inicializácie základných periférií, ©ahko pouºite©nej registrácie funkcií obsluhy preru²enia a výpisu do UART so synchronizáciou viacerých jadier. „alej implementuje medziprocesorovú komunikáciu umoº¬ujúcu výmenu údajov medzi jednotlivými jadrami, a tým aj od©ah£enie výpo£tovo náro£ných operácií na paralelnej jednotke.

Na demon²tráciu moºností vektorového procesora boli vyvinuté dve aplikácie - algoritmus zaloºený na Kalmanovom filtri na odhad rýchlosti vedúceho vozidla a konvolu£ná neurónová sie´ natrénovaná na rozpoznávanie ospalého vodi£a. Správna funkcionalita bola overená spustením programov v simula£nom prostredí a následne na prvom prototype evalua£nej dosky.

Klí£ová slova: Aurix TC4xx, Pre-development, Základná softvérová podpora, Paralelné výpo£ty, Asisten£né systémy vodi£a, Generovanie kódu, Kalmanov filter, Konvolu£ná neurónová sie´

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Chapter 1

Introduction

The pressure to improve driver safety through neural network-based algorithms in driver assistance systems is forcing automotive microcontroller manufacturers to create new architectures satisfying the latest safety and security standards while delivering adequate performance to utilize complex algorithms.

This is also the case with Infineon's new TC4xx family of microchips, which has adopted a heterogeneous architecture consisting of TriCore safety microcontrollers and an ARC71 Parallel Processing Unit optimized for compute-intensive operations. Currently, TC4xx is in an early development phase where support is being gradually built up. A simulation environment is provided to speed up SW development before the hardware availability and can be used to perform the initial tests. The same code is reused on hardware later on.

This thesis focuses on developing a set of software tools and features allowing to boot the platform, provide basic run-time capabilities, establish communication between computing modules, and explore the capabilities of PPU using parallel algorithms. Another objective is to use modern high-level approaches to model complex algorithms and generate optimized code for the PPU unit, replacing the hand-written code.

After the analysis of TC4xx architecture in Chapter 2, requirements for the essential software tools are listed in Chapter 3. Their correct functionality is verified by a multi-core application that properly initializes all cores and utilizes interrupts for LED flashing.

The following Chapter 4 describes en early development process of the TC49x device, analyses the simulation environment, and depicts encountered problems and their workarounds for the first hardware samples.

The processing capabilities of a Parallel Processing Unit unit for offloading computationally intensive operations and algorithms are provided in Chapter 5. It also builds support for booting PPU and notifying TriCores using inter-core interrupts. Chapter 6 specifies an inter-processor communication between scalar and vector cores using shared memory and software mailboxes and creates an application demonstrating the use of a vector processor for offloading tasks. Following on from this, several experiments are carried out to demonstrate the advantages and disadvantages of using a vector processor within the TC4xx architecture in Chapter 7.

Last but not least, the possibilities of speeding up development with the use of high-level tools that enable code generation are studied in Chapter 8. The following Chapter 10 specifies the requirements of modern ADAS on embedded devices and compares frequently used architectures. A model-based approach using Matlab Simulink is applied to model and deploy the estimation algorithm using a Kalman filter. The neural network mapping tool is used to tailor CNN for the target embedded implementation.

1.1 Motivation

This thesis was created in cooperation with HighTec EDV company, a supplier of Toolchain for AURIX Tricore architecture. This cooperation allowed us to use the prototype of the development board, draft versions of other development tools, and documents currently unavailable to the general public. The following projects have been developed and documented in details and are available to HighTec's customers as a support for TC49x compiler:

- tc49x-bsp-example [7]
- tc49x-uart-example [9]
- tc49x-ppu-base-example [8]