Czech Technical University in Prague
Faculty of Electrical Engineering
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Doctoral Thesis

Column-parallel Sampling for a Monolithic Pixel Detector

by

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Declaration

I hereby declare I have written this dissertation thesis independently and quoted all the sources of information used in accordance with methodological instructions on ethical principles for writing an academic thesis.

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Abstrakt

Tato dizertační práce se věnuje vývoji převodníku analogového signálu na digitální (ADC) s postupnou aproximací (SAR) a využitím plně diferenciální architektury pro monolitický pixelový detektor (MAPS) Spacepix-2 v technologii 180 nm SoI CMOS. MAPS detektory představují aktuální trend ve fyzikáních experimetech detekce částic o vysokých energiích (HEP). Kromě fyzikálních experimentů jsou tyto detektory hojně využívány v lékařských a kosmických aplikacích. ADC umístěné pod pixelovou maticí v MAPS detektoru se nazývá sloupcové ADC. Ve standardní architektuře pixelový detektor využívá pro každý sloupec jedno sloupcové ADC a analogové signály z pixelů jsou digitalizovány řádek po řádku. Hlavním problémem při návrhu diferenciálního sloupcového SAR ADC je jeho limitovaná šířka, která je dána šířkou pixelu. Spacepix-2 má šířku pixelu 60 µm. Při řešení tohoto problému byla navržena nová architektura v 8-bit a 10-bit verzi,ve které jedno sloupcové SAR ADC je použito pro vzorkování signálů ze dvou sloupců. Plocha SAR ADC se tedy zvětší na 120 µm. Tato nová architektura přispívá ke zlepšení rychlosti vzorkování, linearity, zmenšuje šum a dokonce i snižuje spotřebu SAR ADC. Navržené řešení jednoho sloupcového SAR ADC v 8-bit verzi dosahuje rychlosti vzorkování 4 MSps a spotřeby 200 µW při napájecím napětí 1.8 V. 10-bit verze dosahuje stejných parametrů s vyšší spotřebou 250 µW.

Klíčová slova:

SAR, ADC, MAPS, sloupec, pixel, vyčítací, elektronika

Abstract

This thesis concerns the development of a fully differential analog to digital converter (ADC) with successive approximation (SAR) for a monolithic pixel detector (MAPS) Spacepix-2 in 180 nm SoI CMOS technology. MAPS detectors represent the actual trend in high-energy physics experiments (HEP). Besides HEP experiments are MAPS detectors often used in medical and space applications. ADC placed under the column of the MAPS pixel matrix is called column ADC. A single ADC for a single column is used in standard architecture. Analog signals from pixels are digitized row by row. The main problem of the differential column SAR ADC design is a limited width determined by the pitch of the pixel. The Spacepix-2 pixel pitch is 60 µm. This thesis proposes a new SAR column ADC architecture in 8-bit and 10-bit versions, where each ADC has multiplexed input to two columns. The layout area is doubled to 120 µm. This new architecture helps achieve higher speed, linearity, low noise, and low power consumption of the proposed SAR ADC. The 8 bit column ADC reaches sampling rate 4 MSps, average power consumption is 200 µW from a 1.8 V power supply at ten frames per second readout frequency. The 10 bit version achieves the same parameters with the higher power consumption of 250 µW.

Keywords:
SAR, ADC, MAPS, column, pixel, read-out, electronics

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Abbreviations

ADC	Analog to digital converter
CDAC	Capacitor analog to digital converter
CMOS	Complementary metal oxide semiconductor
ASIC	Application specific integrated circuit
DCC	Differential common centroid
DD	Displacement damage
DNL	Differential nonlinearity
FPGA	Field programmable gate array
FSM	Finite state machine
FURRY	Fast read-out interface
HEP	High energy physics
HCPD	Hit counting pixel detectors
HVT	High voltage threshold
INL	Integral nonlinearity
LET	Linear energy transfer
LED	Light emitting diode
LVT	Low voltage threshold
LVDS	Low-voltage differential signaling
MAPS	Monolithic active pixel sensor
MBU	Multiple bit upset
MoM	Metal oxide metal
MSPS	Milion samples per second
PCB	Printed circuit board
RHDB	Radiation hardening by design
SAR	Successive aproximation register
SEE	Single event effects
SEFI	Single event functional interrupt
SEGR	Single event gate rupture

SEL	Single event latch-up
SET	Single event transient
SEU	Single event upset
SPI	Serial peripheral interface
SoI	Silicon on insulator
TID	Total ionising dose
TNID	Total nonionising dose
ToT	Time over threshold
USB	Universal serial bus

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Introduction

Pixel detectors have been used in high energy physics experiments (HEP) for the last three decades. The first hybrid pixel detectors were developed in the 1980 at CERN. These ionizing radiation detectors composed of an array of diodes and adjacent electronics are based on semiconductor technology. The hybrid detector forms two main elements, the semiconductor sensor and the read-out chip manufactured independently and connected by a bump-bonding process. The sensor part is principally made of doped silicon or cadmium-telluride. The read-out chip, also segmented to pixels, contains electronics to process an incoming electrical signal from the sensor. The advantage of the hybrid concept is in the use of an arbitrary sensor. The disadvantage is a higher cost and complexity.

Nowadays, semiconductor technologies offer ways to integrate the sensor part with high voltage reversely biased diodes and read-out electronics on the same substrate. These detectors are called monolithic active pixel sensors (MAPS). This approach has several advantages compared to the hybrid sensors: missing problems with bump bonding resulting in lower cost, the pixel can shrink with used technology maintaining functionality, low power consumption and low number of input/output pins.

The pixel detector technology was initially invented for experiments in the field of high-energy physics in CERN. However, this technology has extended to many commercial activities in widely differing application areas with ongoing development.

In medical applications, especially radiotherapy and CT scans, pixel detectors are used to measure X-ray in single-photon counting mode. The CT scan field trend is to visualize full-color images with a high resolution and provide a fast read-out interface.

Another application where a pixel detector takes its place is a chemical, physical and structural analysis of a material. It helps better understand a variety of materials, from proteins, polymers to metals and building materials.

Space dosimetry experiments use pixel detectors for radiation monitoring, particle tracking, and recognition. These detectors must be able to work in extreme radiative environments. In this application are often the sensors integrated with an ADC to sample the incoming signal information. Data are then sent and analyzed on Earth. It allows researchers to study the radiation environment in space.

Typically, a MAPS detector consists of a pixel matrix and readout electronics on the same substrate. The pixel matrix has some rows and some columns. Analog signals from pixels are digitized row by row using ADCs placed under each column. Such ADC is called column ADC. This thesis proposes a new fully differential column SAR

ADC architecture for Spacepix-2 MAPS detector in 8-bit and 10-bit versions in 180 nm SoI CMOS technology. Spacepix-2 has pixel pitch of 60 µm. The problem is that the pixel pitch limits the width of the ADC layout. Internal capacitive DAC layout in SAR ADC is significantly complicated. This thesis provides the new solution where a single ADC digitizes signals from two columns doubling the layout width to 120 µm. This approach permits to use of fully differential SAR ADC architecture that improves linearity, speed and decreases the noise of ADC.

Motivation

A current converted to a voltage is generated when a particle hits the sensor in a pixel. Two ways exist how to process this voltage signal. The first is the time over threshold method (ToT), where the deposited energy of the particle in a sensor is proportional to the time when the voltage is over the threshold. The second is the ADC method, where the peak voltage signal of deposited energy of a particle left in a sensor is measured. These principles are explained in the first chapter 1. The ADC method provides more information about radiation environment than the ToT method. The disadvantage of the ADC method is in more complexity. The primary motivation is to design low power, fast enough, and linear ADC with a moderate resolution for MAPS pixel detector dedicated for space applications. MAPS detector combining sensor, ADC, and fast digital readout allows a user to study radiation environment in space, creating opportunities for interesting scientific experiments in space missions. Regardless of the space missions, this concept may also be helpful in other applications like CT scans, radiotherapy, and structural analysis of a material. A differential SAR ADC architecture provides several benefits compared to a single-ended design. However, the differential architecture needs two CDAC causing the problem to implement only in 60 µm width. Another challenge is to use a minimum unit capacitance in CDAC and reach proper linearity. The secondary motivation is to successfully solve these design challenges.

Aims of the Thesis

Aims of the thesis are following:

1. Design fully differential column-parallel SAR ADC (8-bit and 10-bit) for a monolithic pixel detector in 180 nm SoI CMOS technology.
2. Reach conversion speed at least 2 MSps.
3. Use a low power asynchronous architecture.
4. Decrease capacitive DAC capacitance to minimum.
5. Provide a high input impedance.
6. Convert single-ended signal from a pixel to fully-differential signal at the ADC inputs.

Structure of the Thesis

Chapter 1 provides necessary theoretical background for better understanding the rest of the thesis. It addresses the difference between hybrid and MAPS detectors, the importance of the ADC measurement in HEP experiments, primary SAR ADC working principle, comparison ADC architectures, problem statement, design parameters, and state of the art (related work).

The following two chapters 2 and 3 describe the new proposed design of column SAR ADC for Spacepix MAPS detector in 8-bit and 10-bit versions. Designing the 8-bit version is more accessible because there are lower requirements for the comparator design and CDAC layout design. For this reason, the 8-bit column SAR ADC is designed first, and then the same architecture is extended by two more bits to the 10-bit version.

Chapter 4 describes the necessary electronics, measurements methods, design of PCBs, and software tools for data transfer and processing from Spacepix-2 MAPS detector ASIC.

Chapter 5 shows measured ADC characteristics, integral and differential non-linearities, power consumption, sampling rate and compares the proposed solution with another existing column ADCs. This chapter also shows measuring spectra with the implemented Spacepix-2 MAPS ASIC.

Chapter 1

Theoretical Background

A simplified block diagram of the Spacepix MAPS detector ASIC is illustrated in Fig. 1.1. Each pixel contains the sensor diode reversely biased by a high voltage (HV) in a magnitude of 100-150 V. A particle hitting the sensor generates a current pulse converted to voltage pulse by a charge summing amplifier (CSA). Then the signal is connected to peak detector hold (PDH) if the detector works in ADC mode or to discriminator (DIS), assuming that the sensor operates in counting mode (HC).

In the hit counting mode, the CSA output voltage goes up when a particle hits the sensor. If this peak voltage value is over a certain (adjustable) threshold, the counter (CNT) starts counting. Data are then stored in the fast shift register (FSR) and finally read out digitally using SPI or LVDS. The hit counting mode is primarily dedicated to soft X-ray radiation imaging.

In the ADC mode, the CSA output voltage goes up to the maximum value proportional to the energy left by the detected particle in the detector. Peak detector hold (PDH) holds the maximum peak voltage value. This value is sampled by the ADC and stored in the FSR. All ADCs are placed under each column. For this reason, it is called column ADC. Sensor peak voltage signals are sampled row by row, and data are read-out digitally in the same way as in the hit counting mode. The ADC mode provides information about the energy of particles useful for dosimetry applications.

Spacepix-2 ASIC is controlled external signals that allow the user to perform row shifting, reset, load configuration, test individual blocks, and read data from the detector.

Fig.1.2 illustrates a frame detector readout of the Spacepix MAPS detector. At the beginning of the frame, the reset signal occurs to set the detector to its initial state - the reset pulse width of around 200 ns. Then the exposition time takes place, getting the sensor diodes on. A particle hitting the sensor creates voltage proportional to energy left by the detected particle in the detector at the PDH output (ADC input). After the exposition time, the first rising edge of the row shift signal selects row 63. At the falling of the row shift signal is PDH voltage output of pixels from row 63 sampled. Sampling takes some time, and then the data are stored in the shift register. The second row shift rising edge selects row 62, and row 63 data are sent out from the detector. Single row readout time depends on the readout frequency. At 50 MHz it is 20.48 µs. At the second falling edge of the row

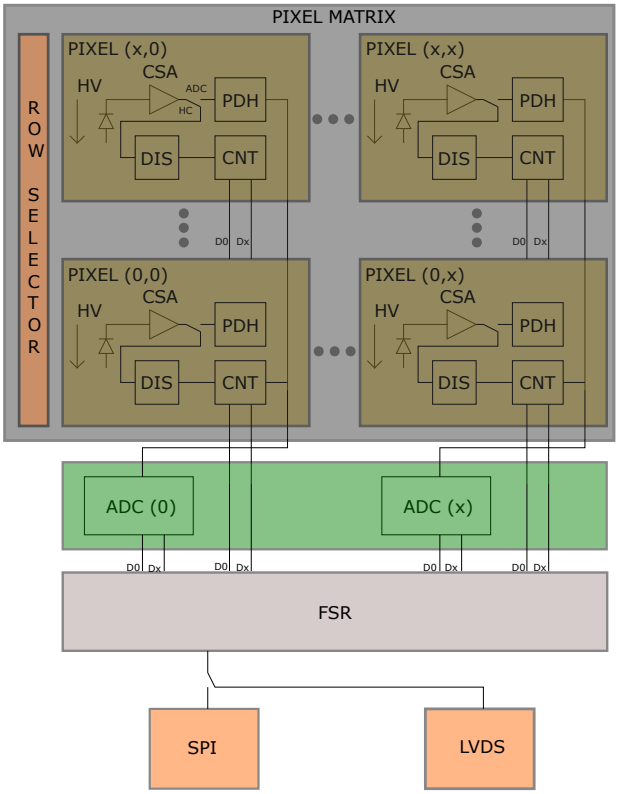

Figure 1.1: The principal illustration of a MAPS detector ASIC.

shift signal are sampled voltages of pixels in row 62. The readout continues in the same manner up to row 0. The time for sampling should be as short as possible to cut the readout time to a minimum. However, concerning the time duration of the other signals is one µs reasonable compromise.

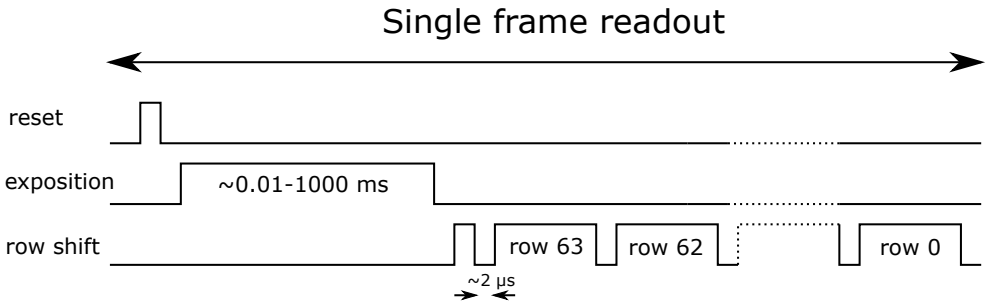

Figure 1.2: The timing diagram of the Spacepix MAPS detector readout.

Table 1.1: The comparison of existing ADC architectures.

ADC architecture	Power consumption	Speed	Area	Resolution
Sigma-delta	low	low	low	very high
SAR	very low	high	moderate	moderate
Flash	high	very high	large	low
Integrating	low	low	low	low
Pipeline	high	very high	moderate	high

1.1 Choice of the ADC Architecture

The first step to the realization of sampling in the proposed Spacepix architecture is to answer question where to place the ADC. One option is to place ADC in the pixel. However, this choice has two disadvantages. The first is the limited pixel size of 60×60 µm^2 used in Spacepix-2 ASIC. The second disadvantage is increased power consumption. A better way to place the ADCs is under columns and sample signals from pixel row by row. This approach is called column-parallel sampling. It reduces power consumption and the layout constraints only in width, not in length.

The second step in column-parallel ADC design is choosing the most suitable ADC architecture. This choice is the crucial step as it determines the complexity and performance of the entire solution. Three basic requirements for column-parallel ADC for MAPS detector are low power consumption, moderate resolution (8-10 bits), moderate layout area, and high speed. The following table 1.1 compares the existing ADC architectures.

According to table 1.1 is the most suitable SAR ADC architecture. It provides low power consumption, sampling rates up to 5 MSPS, moderate layout area, and sufficient resolution. Sigma-delta and integrating converters are slow for the given application. The flash converter has high power consumption and low resolution. The pipeline ADC also has higher power consumption in comparison with SAR ADC architecture.

1.2 SAR ADC Architecture

Fig. 1.3 illustrates a simplified SAR ADC block schematic. The ADC circuit consists of a digital to analog converter (DAC), comparator, and SAR control register. Transistors or resistors can be used for the CDAC realization. However, to maintain a low power consumption is the DAC preferably implemented using capacitors, called CDAC. Such SAR architecture is called SAR ADC with charge redistribution because the charge stored in CDAC capacitors is redistributed between capacitors within an approximation cycle resulting in an effective low power ADC design.

In Fig. 1.3A is shown a single-ended architecture with one of the comparator inputs connected to a reference voltage. When the sampling period occurs, the top plates of all capacitors in CDAC are switched to the ground, and the bottom capacitor plates are connected to the input voltage. The control SAR algorithm then switches the MSB ca-

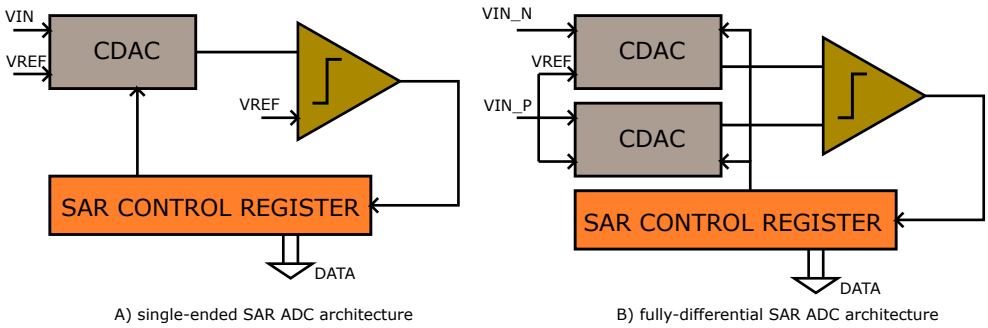

Figure 1.3: The SAR ADC block diagram.

pacitor to the reference voltage. According to the comparison result, the output leaves MSB changed to the reference voltage or the ground. The algorithm continues in the same manner up to LSB. A three-bit example single-ended approximation cycle is illustrated in Fig 1.4A. The one of problems of the single ended architecture is that any voltage noise presented at the reference voltage higher in peak value than 1 LSB affects accuracy of ADC. A power supply fluctuations also deteriorate a proper ADC operation. The preferred choice is to use the fully differential architecture that effectively suppress these difficulties.

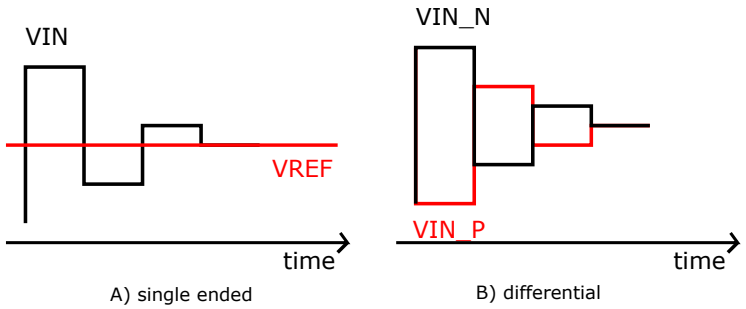

Figure 1.4: The single-ended and differential successive approximation cycle.

The fully differential architecture, principally illustrated in Fig. 1.3B, employs the same control algorithm with the difference that the input voltage is connected differentially to two CDACs and capacitors in both CDACs are switched inversely. This architecture has benefits in higher noise immunity and low process variability. Another advantage is the two times larger voltage magnitude of LSB. The comparator design of the fully differential architecture is more relaxed because charge injection does not affect ADC performance. It allows the designer to use low power dynamic comparator architecture. On the other hand, fully differential design takes over more layout areas. Fig. 1.4B illustrates the differential approximation cycle.

1.3 Problem Statement

The purpose of this thesis is to design SAR column ADC for the Spacepix MAPS detector ASIC. The differential SAR ADC architecture, briefly described in section 1.2, provides essential ADC performance benefits. Therefore, the task is to design a fully-differential SAR column ADC.

The first problem in designing such architecture is to convert a single-ended signal from the sensor to a fully differential signal at the ADC inputs. The column ADC thus must contain a single-ended to differential voltage converter. Such converter has to be fast enough to accomplish a fast sampling rate (at least 2 MSPS) parameter. The power consumption of the converter has to be as low as possible to maintain low power operation. A compromise between speed and power consumption has to be made.

In the case of the proposed MAPS detector is the pixel width 60 µm. Therefore, ADC layout width is limited to 60 µm. The major problem is to design fully differential column SAR ADC with 60 µm width and maintain speed, linearity, and low power consumption. This problem is illustrated in Fig. 1.5.

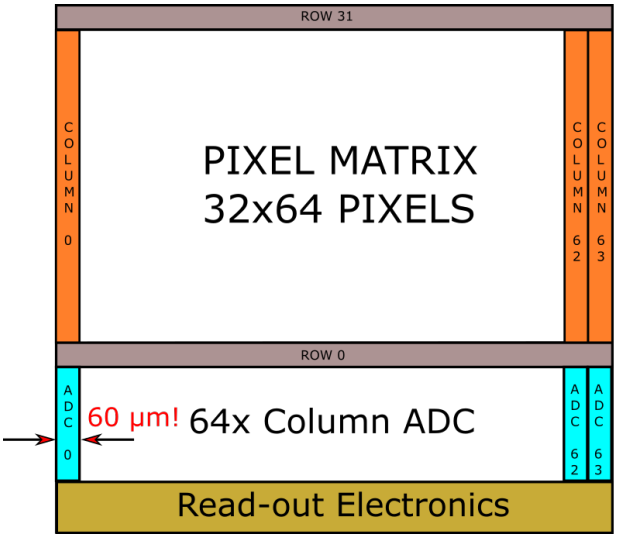

Figure 1.5: An illustration of the major problem solved in this thesis.

The largest area in the SAR ADC with charge redistribution takes the CDAC layout. The CDAC can be realized using a split capacitor method or binary scaling method [2]. The binary-weighted DAC architecture is preferable because it provides better linearity with a smaller unit capacitor. The 8-bit version contains 256 unit capacitors. The 10-bit version contains unit 1024 capacitors. Therefore, the unit capacitor has to be as small as possible to shrink the area. Capacitance has to be also as low as possible to reduce power. The combination of the small unit capacitors and parasitic capacitances between them and substrate complicates the CDAC design. Furthermore, the pixel with is the limit. For fully differential architecture are needed two CDACs. Moreover, the comparator layout has to

Design Parameter	Value	Units
ADC architecture	SAR ADC with charge redistribution	
Number of bits	8-10	
Power consumption	<300	µW
Speed	2	MSPS
Layout width	60	µm
Layout length	1000	µm

Table 1.2: The design parameters.

be perfectly symmetrical in the differential architecture. These problems solve this thesis. The table 1.2 summarize the column ADC design parameters.

1.4 Related Work

From a historical perspective, the first 11-bit, 20 kSps vacuum tube successive approximation ADC was patented in 1963 [3]. The internal DAC represents the first known use of equal currents switched into an R/2R resistor ladder. The first CMOS SAR ADC was published in 1975 [4]. Internal DAC is implemented as capacitive DAC (CDAC) containing the sample and hold circuit. Comparator reference is ground, and a slightly different approximation algorithm is used. An input signal is sampled to the entire DAC capacitance and efficiently re-used. This technique is today known as charge redistribution, making SAR ADC popular in low power applications.

In table 1.3 is shown comparison of properties between McGreary [4] and original SAR ADC method. Green table fields are preferred properties defining SAR ADC development from the past to the present. Below is the list of preferred properties:

1. Avoid needs for resenting; it wastes energy.
2. DAC voltage should be able to go up and down.
3. Common mode level comparison at the mid-scale.
4. DAC should not go outside from supplies.
5. Top plate sampling

A differential DAC solves the first and the fourth problems since DAC voltage can go up and down easily and cannot go outside from the supplies. In the original differential SAR ADC architecture [5] are, during the sampling phase, all capacitors connected between ground (top plate) and input voltage (bottom plate). However, the input voltage can be sampled at the top plate, and the bottom plates are grounded as well [6]. The top

Method	V_{IN} shift	Comparison	CM-level	V_{DAC} out of range	V_{DAC}	Overshoot
Original	No	V_{DAC} to hold	Variable	No	Up/Down	No problem
McGreary	Yes	V_{DAC} to 0	Fixed	Yes (negative)	Down	Needs reset

Table 1.3: The comparison of original and McGreary SAR ADC properties

plate sampling uses inverters at the bottom plates of capacitors that are switched between ground and a voltage reference.

In the original differential SAR ADC architecture goes common-mode too low, making the comparator design difficult. This problem is solved by switching MSB to ground and other bits to reference voltage during the top plate sampling [1]. Then the approximation algorithm always converges toward reference voltage mid-scale. It simplifies the comparator design.

Liu et al. [6] first presented a customized Metal-oxide-Metal (MoM) capacitor for CDAC that they called a cage capacitor with capacitance 4.5fF. A similar CDAC design is used in the proposed 8-bit SAR ADC in chapter 2. Harpe et al. [1] propose an even smaller value of the unit capacitor in CDAC, only 0.5 fF and effective CDAC layout. This approach is used for the proposed 10-bit SAR ADC in chapter 3.

Besides the column-parallel sampling approach exists another ways of signal digitization used in FE-14 [7], [8], or Timepix [9] chips. However, these pixel detectors do not measure the signal amplitude by an ADC but rather use the Time over Threshold (ToT) method for charge digitization in each pixel. ToT relies on a small current discharging a charge-sensitive amplifier with a constant rate. It isn't easy to keep the discharge current uniform and stable across the pixel matrix. Therefore, the ADC approach has been chosen for Spacepix detectors.

SAR ADC with charge redistribution in SoI processes was published by Culurciello et al. [10], and Dasgupta et al. [11]. However, these designs are not column-ADC's and consume a lot of power, not suitable for space applications. One of the first attempts to implement a column SAR ADC with charge redistribution is the XCHIP03 chip [12], [13]. The XCHIP03 design used a single-ended 10-bit SAR ADC.

Chapter 2

8-bit Column SAR ADC

This chapter describes the 8-bit version of column-parallel SAR ADC[A.1] design used in the SpacePix-1 MAPS detector [14].

2.1 Proposed 8-bit column ADC architecture

The proposed asynchronous column SAR ADC is used in the Spacepix-1 MAPS detector. The size of the pixel matrix is 32 rows and 64 columns. The novelty of the proposed solution, published in 2020 [A.1], is that a single ADC converts signals from two columns, odd and even. Data from the ADC are moved to the row shift register (RSR) and then read out serially from the chip with a fast digital interface. An illustration of the Spacepix-1 pixel detector is depicted in Fig. 2.1.

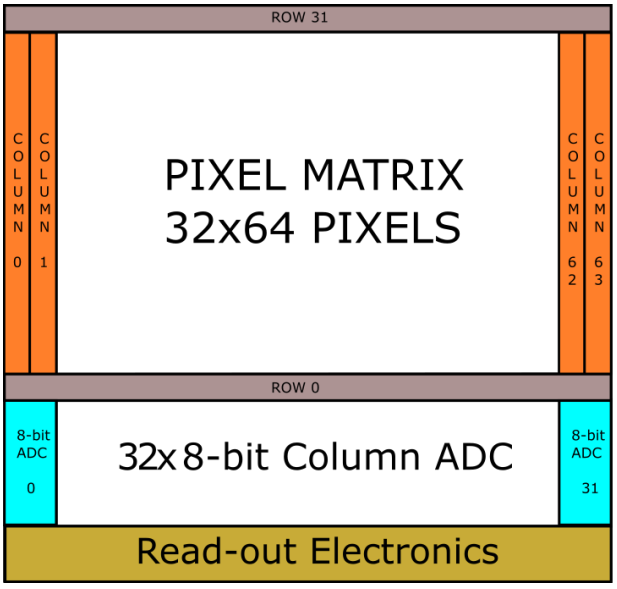

Figure 2.1: The Spacepix-1 MAPS detector illustration.

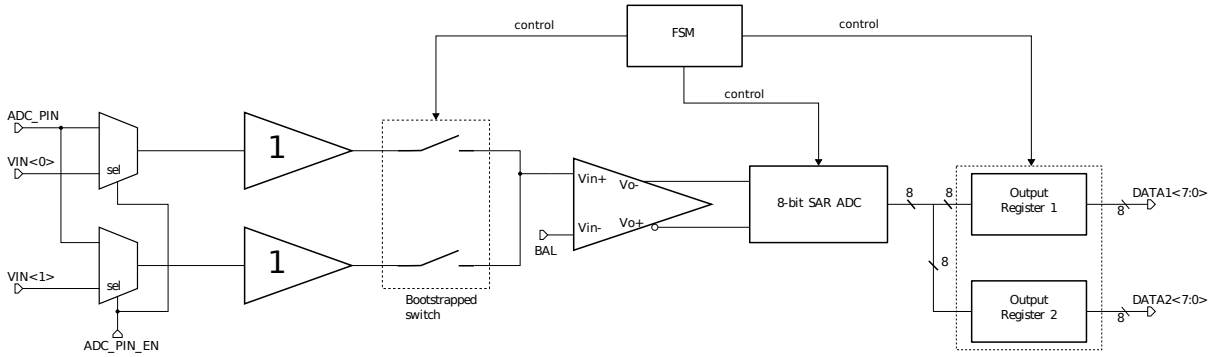

Figure 2.2: The proposed column ADC architecture.

A simplified block diagram of the proposed 8-bit column ADC is shown in Fig. 2.2. Input signals from odd and even columns are connected to VIN<0> and VIN<1>. These inputs are fed through the input demultiplexers where the signal ADC_PIN_EN selects VIN<1:0> or the external pin ADC_PIN. This external pin serves for testing purposes. The input buffers are used to increase the input impedance of column ADC. In the proposed design, the buffer was realized by a standard two-stage operational transconductance amplifier (OTA) with input capacitance 220 fF.

Two bootstrap switches [15] serve as a multiplexer controlled by the finite state machine (FSM). The output from the bootstrap switches is connected to the ADC driver. The FSM selects one of the inputs. The bootstrap switch design is used in order to maintain good linearity resulting in low distortion. The bootstrap switch is described in Section 2.1.1.

The ADC driver is a fully differential amplifier that drives the differential SAR ADC inputs. The main task of this block is to convert a single-ended signal to a differential signal with a fast settling time. The BAL signal sets the common mode. The ADC driver is described in detail in Section 2.1.2.

The 8-bit asynchronous SAR ADC with charge redistribution is described in Section 2.1.3. The output data from the ADC are latched into one of the output registers. The SAR ADC and output registers are also controlled by the FSM.

The FSM was implemented by standard digital cells and is described in Section 2.1.4. The FSM turns on the bootstrap switch at input VIN<0> in the initial state. A conversion cycle is initiated at the falling edge of an external that perform row shifting, principally illustrated in Fig. 1.2. An analog value of the signal VIN<0> is digitized and latched to the output register 1. Immediately after conversion VIN<0>, the FSM switches off VIN<0> and turns on VIN<1>, waits some time to settle the ADC driver output and initiate the second conversion. After the second conversion, is data latched into the output register 2. The individual circuits are described in the following subsections.

2.1.1 Bootstrapped switch

CMOS switches suffer from several imperfections that can be alleviated by bootstrapping. A single transistor switch suffers from a limited input range as input voltage approaches to V_{DD} - V_{TH}. It can be alleviated by a complementary switch topology where NMOS and PMOS transistors provide the whole input voltage range. However, R_{ON} resistance of the complementary structure varies with V_{IN} distorting the signal. The bootstrapped switch preserves R_{ON} constant as the voltage at the node X varies according to V_{IN}, it improves linearity.

The bootstrapped switch uses a standard circuit [15]. The modified design is shown in Fig. 2.3. The used technology, 180nm silicon on insulator (SoI) process, provides NMOS and PMOS transistors with break down voltage of 1.98 V and 5 V. The node X in Fig. 2.3 reaches a voltage level of up to 2.8 V. Therefore, there are used transistors with thicker gate oxides with a breakdown voltage of up to 5V.

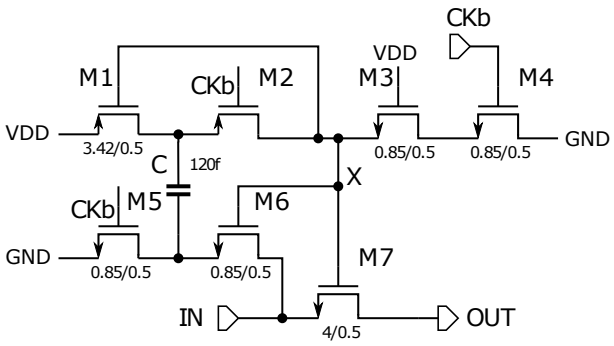

Figure 2.3: The bootstrapped switch.

2.1.2 ADC Driver

The proposed fully differential operation amplifier in Fig. 2.4 [16], drives fully differential SAR ADC inputs. The input stage forms the PMOS transistors M0, M1, cascodes M6, M7, current source M8 and current mirrors M2, M3 stabilized by a common-mode feedback. The common-mode feedback is composed of transistors M15, M16, M11, M13, which set a common mode level and the resistors R2, R3, capacitors C6, C7 senses the output voltage and cancel out differential signals. The transistors M12, M13, M26, and M30 are class AB output stage at output Vo+. Vo- is identical to Vo+. Resistors R7, R6, R8, R9 and capacitors C0, C5, C8, C9 form a frequency compensation. The remaining transistors are for biasing purposes. The advantage of this circuit is a large output swing of the class AB stage, fast settling time, and low output impedance. Using a fully differential amplifier with common-mode feedback for single-ended to differential signal conversion also has the advantage of small sensitivity to process variations.

Voltage Vb1 is connected to the ground. The BAL voltage sets the common mode. The output voltage versus input voltage of the ideal characteristic is depicted in Fig. 2.5

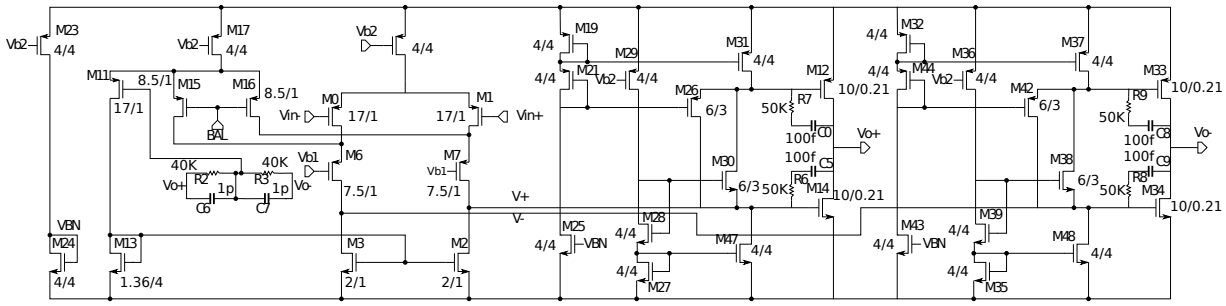

Figure 2.4: The proposed ADC driver.

on the left. Note that the output voltage is equal to -1.024 V for the zero input voltage and +1.024 V for the maximum reference input voltage, which is also 1.024 V. Driver output deviation from ideal characteristic shows Fig. 2.5 on the right. The maximum deviation is 300 µW or 0.3 LSB. The Output settling time is less than 100 ns. Power consumption is 160 µW from 1.8 V power supply. The layout area is 50 × 115 µm^2.

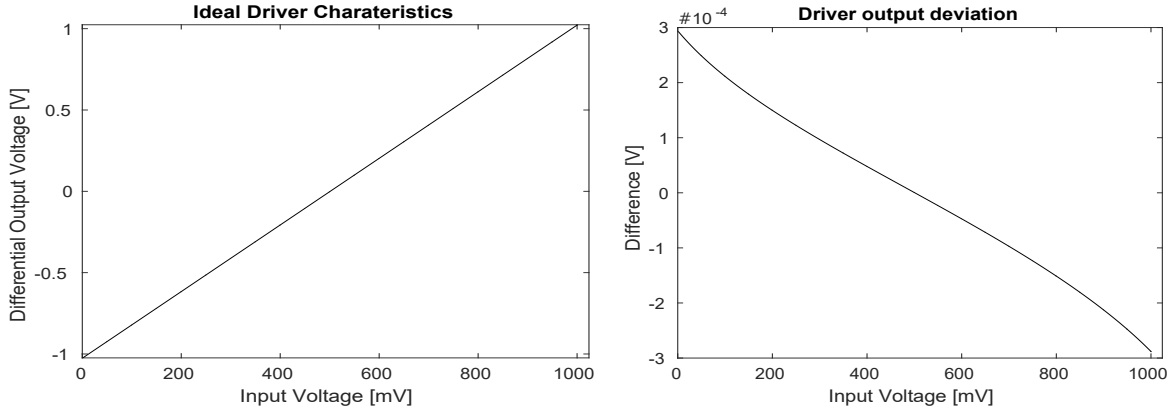

Figure 2.5: The input and output voltage characteristics of the proposed ADC driver.

2.1.3 8-bit SAR ADC

A block diagram of the proposed asynchronous 8-bit SAR ADC [A.2] is depicted in Fig. 2.6. Input or output pins are signed in capital letters and internal nets in italics. The primary switching principle, SAR logic, and comparator are identical with Harpe et al. design [1]. The switched capacitor DAC (CDAC) is different, explained below. A new pulse generator is added to generate the *mclk* signal at the falling edge of the SAMPLE signal. The *mclk* signal is used to sample the input analog voltage to CDACs through bootstrapped switches. A new reset circuit is added to generate a SYNC signal that is needed for the asynchronous AD conversion of signals from the left and the right column. The individual blocks different in comparison with [1] are explained below.

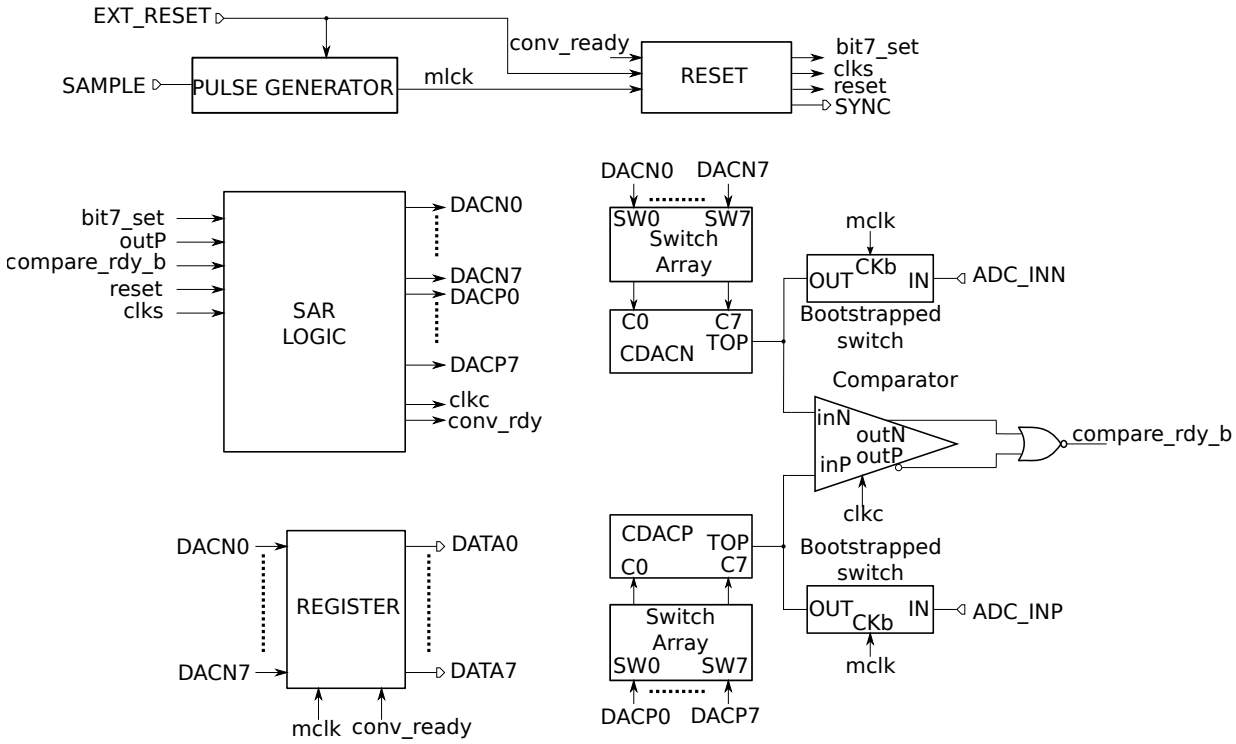

Figure 2.6: The 8-bit SAR ADC block diagram.

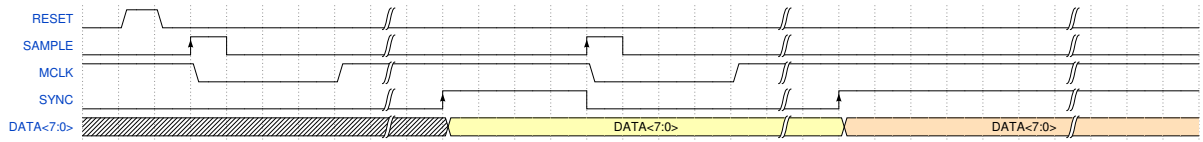

Figure 2.7: The SAR ADC Timing diagram (not to scale).

The asynchronous operation is depicted in Fig. 2.7. Before a conversion cycle takes place, the RESET signal goes high to set asynchronous logic to its low initial state. The ADC converter is in standby mode after reset. Another reset signal is generated internally by the signal *conv_rdy* when a conversion cycle has been completed. The converter goes on standby mode after every conversion. The pulse generator is a monostable circuit that generates a pulse *mclk* at the rising edge of the signal SAMPLE. An input differential signal is sampled to the CDACs when *mclk* is low. The SAR logic begins successive approximation when the *mclk* goes high. The SYNC signal goes high when the ADC finishes a conversion cycle. DATA are latched into the output register at the rising edge of SYNC. The SYNC signal goes low when the next conversion is required by the SAMPLE signal.

2.1.3.1 Capacitive DAC

The Proposed switched capacitor DAC contains 256 customized MoM capacitors. Each unit capacitor has the dimensions 4.24x4.24 µm^2, with capacitance of 4.5 fF [A.3]. Details of the unit capacitor is shown in Fig. 2.8. The metal 3 forms one pole and metals 1 or 4, the second pole of the capacitor. All metals including vias, except for gaps for the metal 3 pole, form a box structure that highly decreases parasitic capacitances. The CDAC layout area is 195x57.5 µm^2, overall capacitance of switched capacitor DAC is 1.174 pF.

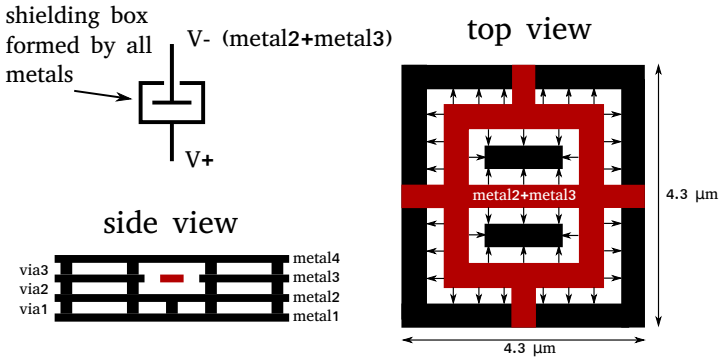

Figure 2.8: The proposed MoM capacitor.

2.1.3.2 Asynchronous Dynamic SAR Logic

This asynchronous logic architecture is based on Harpe et al. [1] design. The proposed algorithm of the SAR ADC asynchronous controller performs a binary search algorithm in eight identical cycles. Fig. 2.9 shows state and timing diagram pro the single SAR bit. To achieve consecutive asynchronous operation, self-synchronization is used. Before each transition, a specific condition is checked to ensure that the previous step is finished before starting the next. First, the bit is set (1). When the bit is ready (2), the comparison is initiated (3). After some time the comparator is valid, which indicates by ready signal (4). Then, the next bit is initiated (5). The value of the bit decision is stored in the SAR register.

To implement logic in Fig. 2.9 is the operation split into two parts illustrated in Fig. 2.10. The main control starts in state 10. When the bit is set, the state changes to 00 where *compare_b* requests comparison. The condition *compare_rdy_b* test if the comparator is ready. Then the state changes to 01 to hand over the next bit iteration by enabling *next_bit_set*. The DAC control starts in state 1 where the DAC bit is turned off. When the *bit_set* is requested and the comparison is active, the state changes to 0 in which the DAC bit is set. Based on the comparator result and conditions *next_bit_set* and *compare_rdy_b*, the state changes back to 1 or remains in the state 0.

Different approaches can realize both state machines in Fig. 2.10. Interesting realization by Harpe et al. [1] illustrates Fig. 2.11. This is effective and low-power solution.

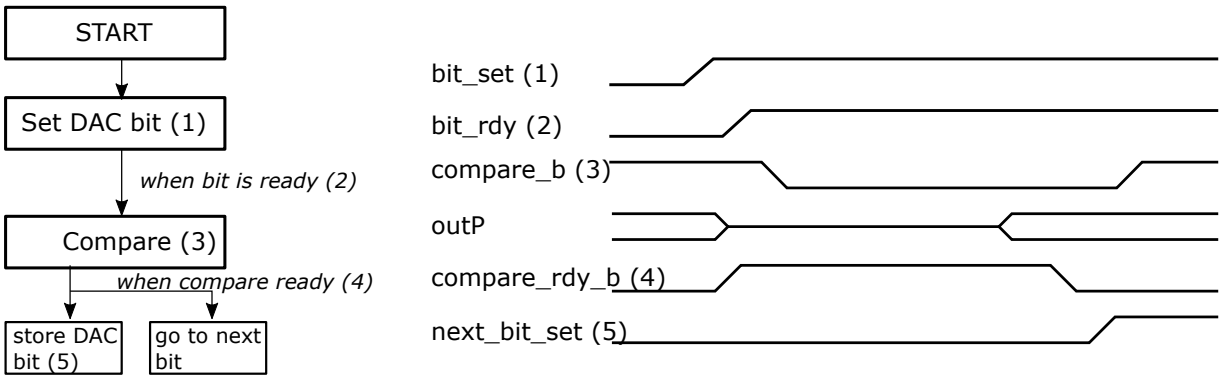

Figure 2.9: The conceptual state and timing diagram of single SAR bit operation.

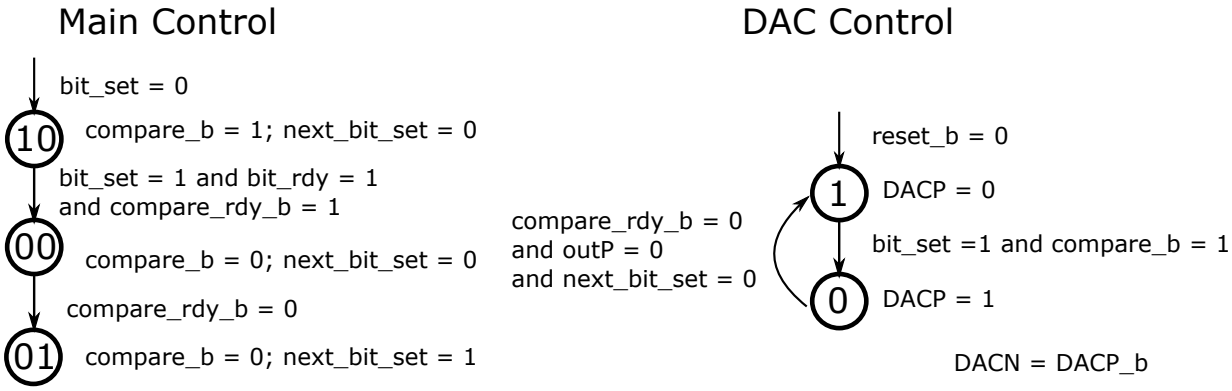

Figure 2.10: The state diagram of the main control and the DAC control.

On the other hand, this realization is problematic in the MAPS detector application because the reset signal sets capacitors C1, C2, and C3 at the beginning of the frame readout. Sampling takes place right after the acquisition time. C1, C2, and C3 are based on parasitic capacitances verified by simulation. As the detector's acquisition time is variable in time, it is complex to set these capacitances properly. Therefore, the realization in Fig. 2.11 is not guaranteeing the reset state of the state machines because the sampling does not occur immediately after the reset, and a leakage current influences parasitic capacitances.

Another more robust approach to realize the main control and the DAC control is with standard cells in the used technology. This realization is shown in Fig. 2.12. The benefit is the stability of signal states after reset with no dependency on time. This implementation is more robust for the target application.

The modular asynchronous logic concept is illustrated in Fig. 2.13. The signal *mclk* initiates the 10-bit conversion. Each module generates clock pulses (*clkc*) for the comparator through OR gates. The comparison is allowed by *compare_rdy_b* signal from the comparator. The *compare_rdy_b* generates a NOR gate connected at the differential comparator output (not illustrated). The result of a comparison, the signal *outP*, is sampled in each bit. When a conversion cycle is finished, the *conv_rdy* signal latches data in the

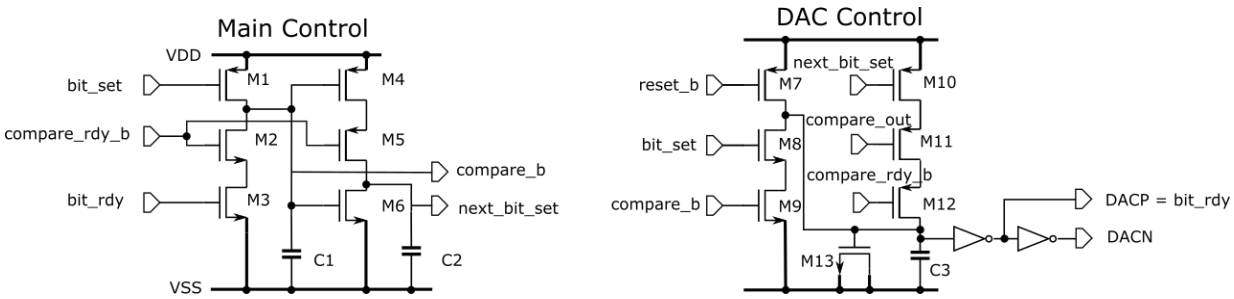

Figure 2.11: The realization of state machine by Harpe et al.

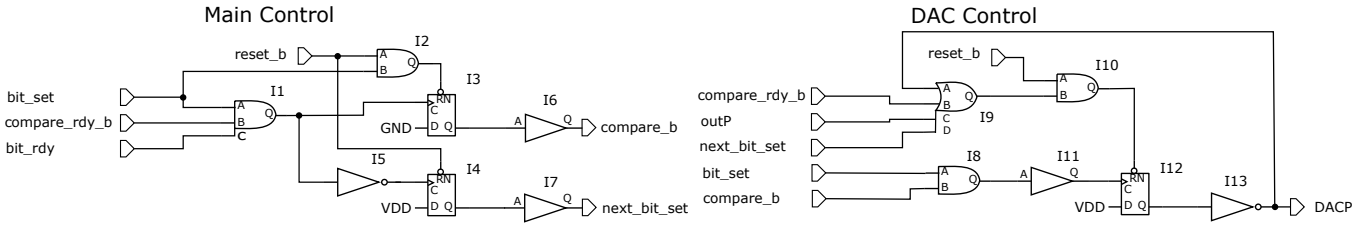

Figure 2.12: The DAC control realization using standard cells.

10-bit register.

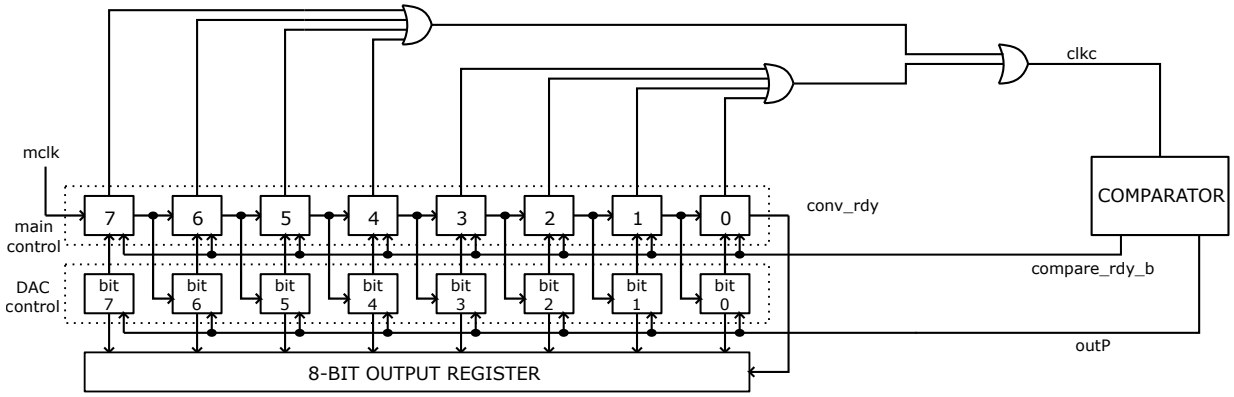

Figure 2.13: The simplified block diagram of the asynchronous SAR logic.

2.1.3.3 Dynamic comparator

The design of the comparator also uses Harpe et al. [1] architecture. A combination of low threshold (LVT) and high threshold (HVT) transistors is used. In each current branch is at least one HVT transistor used to avoid leakage current. The difference of the proposed comparator design is only in the transistors sizing as illustrated in Fig. 2.14.

The simulated offset of the comparator reaches almost 30 mV. However, in the differential architecture, the comparator offset causes only the ADC transfer function offset and has no impact on ADC linearities. The noise of the comparator is simulated using

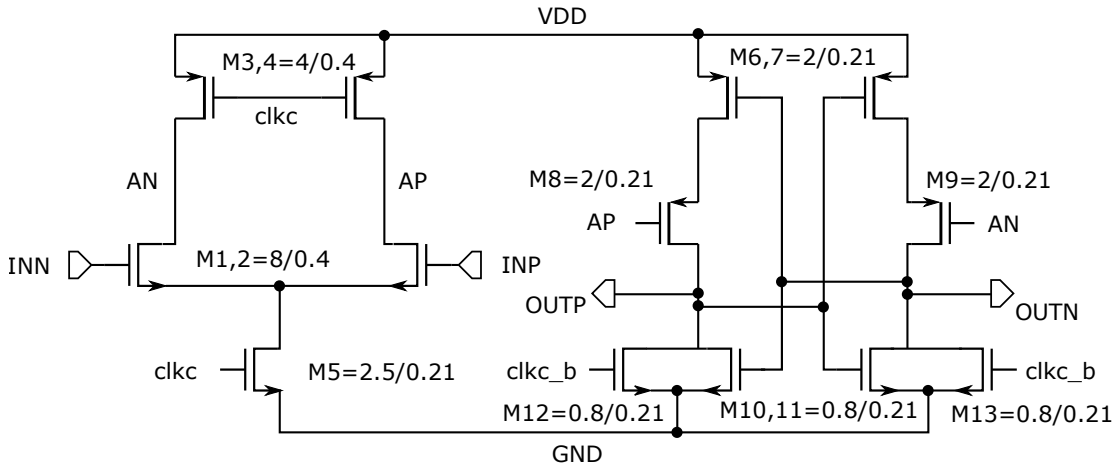

Figure 2.14: The dynamic comparator design.

Differential voltage [µV]	Wrong decisions
100	64
200	45
300	35
400	21
500	12
600	7
700	6
800	4
900	2
1000	1

Table 2.1: The simulated transient noise of the comparator.

transient noise analysis. The differential input voltage is swept from hundred microvolts up to tens of millivolts. In each step, some wrong decisions occur. The bad decisions are counted. The total number of decisions in each voltage level is one hundred. The number of wrong decisions at a particular voltage level shows Tab. 2.1.

The comparator noise can be calculated using the following formula 2.1 [17],

$$V_{n_{RMS}} = \sqrt{k_1 v_1^2 + k_2 v_2^2 .. + k_n v_n^2} \tag{2.1}$$

where v_m is differential DC voltage at which k_m wrong decisions occur. The calculated comparator noise is 475 µV. That is for 8-bit ADC approximately 1/8 LSB if the voltage reference is 1.024 V.

2.1.3.4 Reset circuit

The reset circuit is an additional part of the SAR logic. The RESET signal is generated if the EXT_RESET or *conv_rdy* signal is received. This circuit also generates the signal BIT7_SET on the *mclk* rising edge and SYNC when the conversion is finished. The signal SYNC is needed for the asynchronous double column conversion. The reset circuit is shown in Fig. 2.15 and a timing diagram in Fig. 2.16.

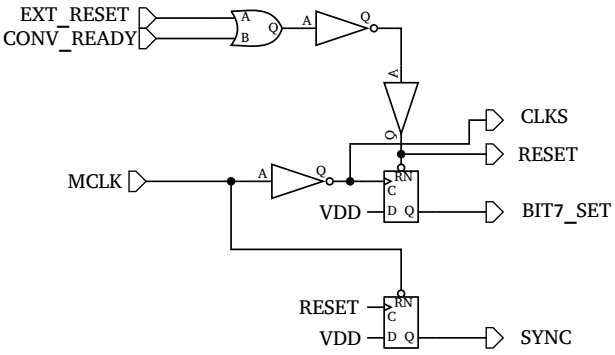

Figure 2.15: The reset circuit.

2.1.3.5 Pulse Generator

The pulse generator is a monostable circuit that generates an *mclk* pulse of defined length. The *mclk* signal is active low, used for sampling analog voltage to swithed capacitor DAC. The proposed pulse generator is illustrated in Fig. 2.17.

First of all, the *mclk* signal has to be initiated by EXT_RESET. It turns on the transistor M4 to discharge MOS capacitor M1. M1 is charged by a constant current from current source M0 when the *mclk* is low at CLKIN rising edge (CLKIN is SAMPLE signal). The M0 current is adjusted by VPS voltage. I1 output goes low when the voltage at the M1 capacitor reaches a threshold voltage of the inverter. In this time, I24 Q output goes high and the short reset signal is generated by a delay line I8, I26 in order to reset I22, I24. *mclk* is low and circuit waits for next CLKIN rising edge. The timing diagram is shown in Fig. 2.18.

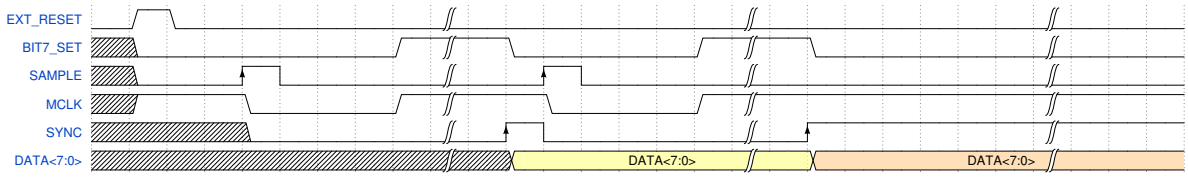

Figure 2.16: The reset circuit timing (not to scale).

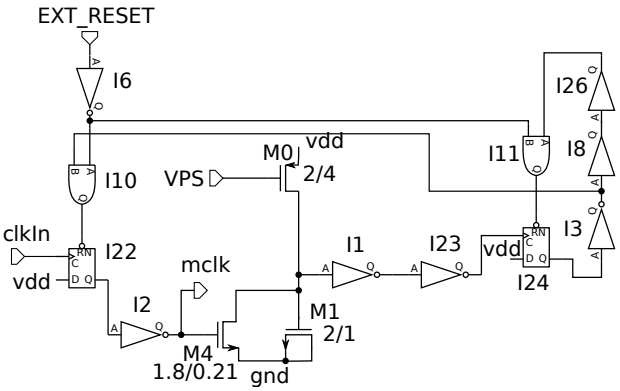

Figure 2.17: The pulse generator.

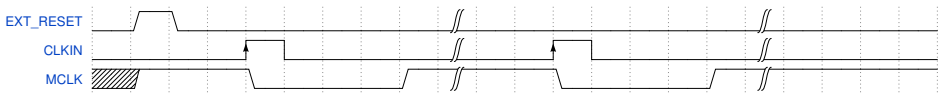

Figure 2.18: The pulse generator timing (not to scale).

2.1.4 Column Control FSM

This simple finite state machine (FSM) controls AD conversion of the left and the right column. It controls the bootstrapped switches at the ADC driver input, latches output data into registers and also drives the SAMPLE signal of the SAR ADC. The circuit diagram is shown in Fig. 2.19 and the time diagram in Fig. 2.20. At first, the EXT_RESET goes low to initiate the FSM to its state. The REG_SET signal is low and turns on the even column connected by the bootstrapped switch. The first row of the pixel detector is selected at ROW_SHIFT rising edge. The ROW_SHIFT signal is held high until a voltage level is steady at the output of the input buffers. The first conversion cycle is initiated at ROW_SHIFT falling edge by SAMPLE signal, generated by I8. The delay loop, composed of I12-I14, reset I8 when the SAMPLE signal goes low. I12 and I13 are delay buffers. The SYNC signal goes high when the first (odd column) conversion has finished. The ADC data are latched into both registers at the rising edge of SYNC and REG_SET. At the same time, the second SAMPLE signal is generated and the second (even) bootstrapped switch is turned on (the odd bootstrapped switch is turned off) by the REG_SET signal. At SYNC rising edge, the second (even) conversion cycle is initiated. The ADC data (even) are latched into one register by the rising edge of the SYNC when the second conversion cycle is finished. Data latched in both registers are moved to a shift register and are ready to be read out. The next conversion cycle can be initiated by ROW_SHIFT when the data are moved into the shift register.

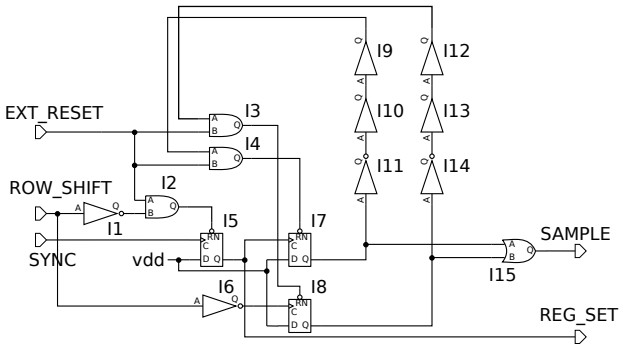

Figure 2.19: The FSM circuit diagram.

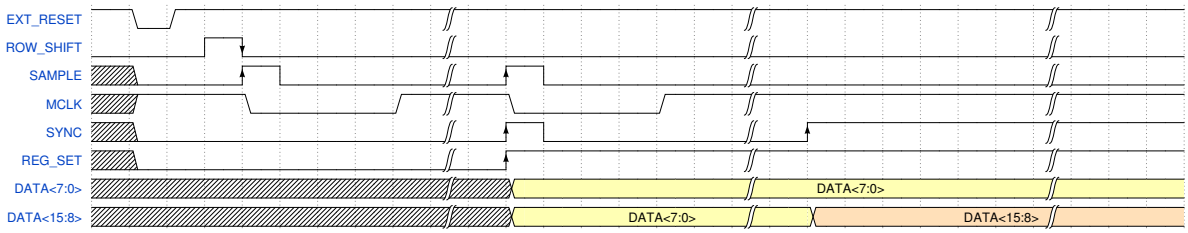

Figure 2.20: The FSM timing diagram (not to scale).

2.1.5 Layout

The layout is shown in Fig 2.21. A common centroid technique [A.5] is used for transistors in the comparator circuit of the SAR ADC and for transistors in the ADC driver. The common centroid technique helps to improve matching properties and eliminates analog single event transients invoked by impinging particles [18], [19]. The layout is kept as symmetrical as possible. At the bottom of the layout the output registers are placed for a simple connection of the readout circuits. A free place in the symmetrical structures are filled with decoupling capacitors. Driving signals, bias and power are connected on top of the layout by top metal in the used technology. The dimensions of the layout are 445×115 µm^2. All 32 column ADCs are placed next to one another.

2.1.6 Bandgap Voltage Reference

The Spacepix-1 ASIC has integrated an on-chip bandgap reference with output voltage 1.024 V. In the case of 8-bit ADC is 1 LSB voltage step equals 4 mV. The bandgap voltage is decoupled by a large off-chip capacitor (10 µF). When a conversion cycle occurs, the current charging the capacitors in CDAC is drained from the voltage reference and the associated capacitor. The bandgap's output resistance has to be low enough to supply sufficient current for all 32 ADCs without a significant voltage drop. This is verified by simulation.

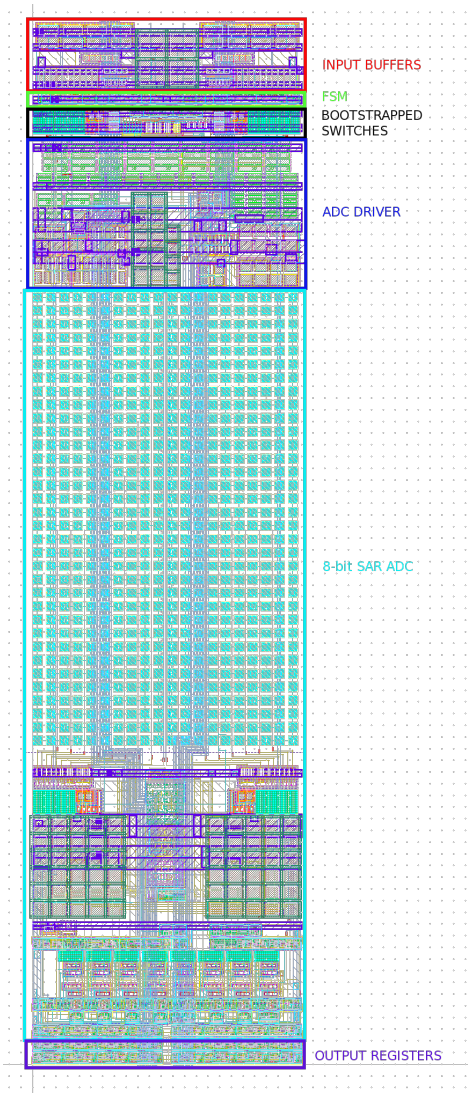

Figure 2.21: The 8-bit column ADC layout.

2.1.7 Layout of all 32 Column ADCs

This chapter so far described the design of the single 8-bit column ADC. However, placing all column ADCs one to the next brings other challenges that have to be solved. The layout design of single column ADC has to tie up the other as explained in section 2.1.5. Then is possible to place all 32 ADCs one to the following other as illustrates Fig. 2.22.

Single column ADC requires connecting power, bias signals, bandgap voltage reference, and control signals (reset and row shift) with the associated circuits in the chip. These connections realize thick top metals placed under the column ADCs leading through all 32 ADCs. Then is possible to connect signals with the related circuits in the chip from the left or the right side of the 32 ADC layout. Required metal thicknesses are calculated and verified by simulation. At the bottom, power lines at the bottom supply the SAR

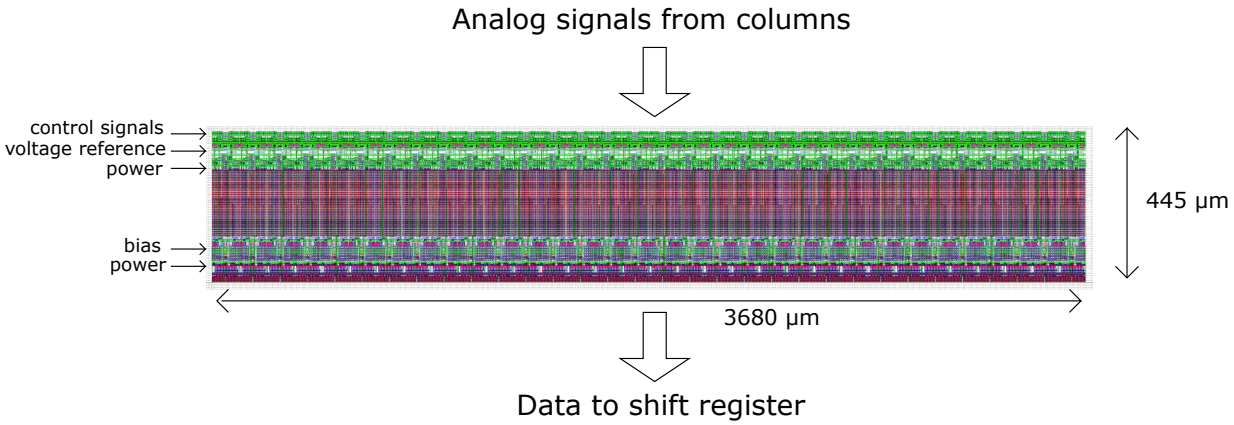

Figure 2.22: The layout of 32 column ADCs.

ADCs, and power lines at the top supply the analog front-end (ADC driver, buffers, FSM). Analog signal from pixels coming for the top of the ADC input. Output data from ADCs to fast shift registers are connected from the bottom. The total layout length is 3680 µm, and the high is 445 µm.

Chapter 3

10-bit Column SAR ADC

The problem to adequately design the 10-bit SAR column ADC for MAPS detector is the limited width of the layout and simultaneously to maintain the linearity of internal switched capacitor DAC (CDAC). The 8-bit SAR ADC architecture [A.1] provides doubled width of the ADC layout because the single ADC digitizes signals from two columns. This double sampling method is also used in this 10-bit version, and therefore the CDAC layout is more relaxed. However, to reduce the CDAC layout's height, the unit capacitor size in the 10-bit version has to be smaller in area because 1024 unit capacitors are needed instead of 256 capacitors in the 8-bit version. Design described in this chapter solves this problem and provides a 10-bit CDAC layout with a unit capacitor capacitance of only 0.5 fF and novel foldback architecture that reduce the layout height by half. The CDAC layout is even narrower than pixel size; therefore, it is possible to lead analog and digital pixel power supply through the ADC.

In comparison with the 8-bit version [A.1] are two more problems solved. The first is the comparator design with rescaled transistors and improved symmetrical layout. The second is the SAR logic redesign with extension by two more bits.

The chapter is organized as follows: Section 3.1 is a brief overview of the 10-bit column ADC architecture, section 3.2 describes design problems of CDAC, comparator, and SAR logic, and section 3.3 discusses layout design.

3.1 10-bit column ADC architecture

The 10-bit column SAR ADC architecture, depicted in Fig. 3.1, exploits the same double-sampling method described in the 8-bit ADC version [A.1]. On the left side of the Fig. 3.1, input signals for odd and even columns are shown. The input multiplexers allow the user to connect signals from columns to ADC or an external pin for ADC testing purposes. The double sampling is initiated by a signal that performs row shifting. The input buffers provide high input resistance of the column ADC. The FSM successively controls the asynchronous AD conversion of the left and right column, and data are latched into output registers. The fully differential amplifier drives the fully differential SAR ADC inputs.

The 64 × 64 pixel matrix needs only 32 ADCs. This double-sampling architecture is described in detail in [A.1]. The 10-bit SAR ADC contains the following differences: Complementary metal-oxide-semiconductor (CMOS) switches instead of bootstrapped switches are used at the input of the fully differential amplifier (ADC driver); SAR logic and registers are extended by two more bits to 10-bits.

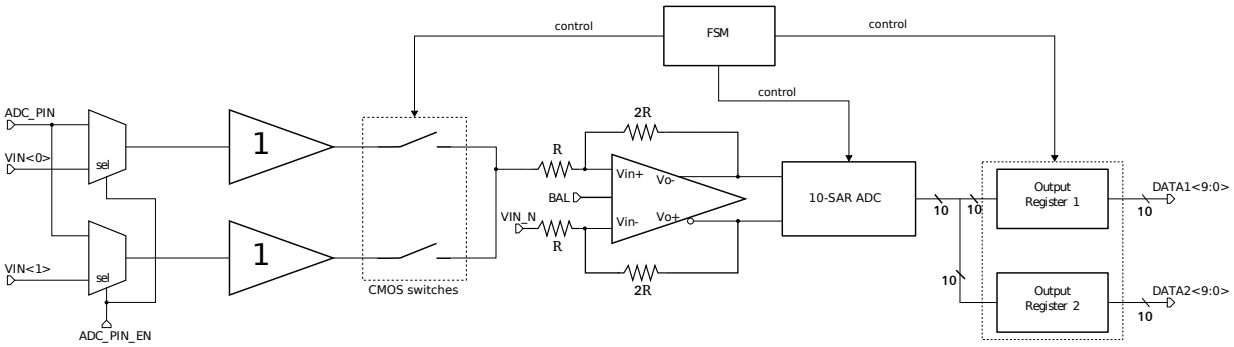

Figure 3.1: The 10-bit column ADC block diagram, the input signals on the left side going though buffers to ADC driver. FSM controls the asynchronous conversion and data are stored in the output registers.

Adjustable BAL and VIN_N signals bring improvement compared to the 8-bit version design [A.1]. The VIN_N signal allows the user to shift the input voltage range according to the following relation:

$$ADC_{vout} = V_{in} + (V_{IN\_N} - \frac{V_{ref}}{2}), \tag{3.1}$$

where V_{in} is the voltage at the buffer input (VIN<0> or VIN<1>), V_{IN_N} is the adjustable voltage at the negative input of the ADC driver, V_{ref} is the ADC reference voltage and ADC_{vout} is the ADC value in volts. It is also possible to calculate ADC value in volts:

$$ADC_{vout} = \frac{V_{ref} ADC_{code}}{ADC_{maxcode}}, \tag{3.2}$$

where ADC_{code} is 10-bit code of the sampled input voltage and $ADC_{maxcode}$ is 1023 for a 10-bit ADC resolution. If the V_{IN_N} input is set to 512 mV and V_{ref} is 1.024 V, then the 10-bit binary approximation of input signal (ADC value) is equal to V_{in}. If the V_{IN_N} is set, for example, to 612 mV, then the ADC value is 100 ADC units (1 ADC unit = 1 LSB) lower then the V_{in}. The signal V_{IN_N}, if needed, is possible to make use for shifting the ADC transfer characteristic by a constant value.

The BAL signal control has also a significant benefit in this architecture. The BAL signal sets the common-mode level as depicted in Fig. 3.2. The differential input voltage shown as a sine wave is sampled to CDAC through bootstrapped switches inside of the SAR ADC (shown in Fig 3.3). Then, the approximation algorithm, also shown in Fig. 3.2, takes place.

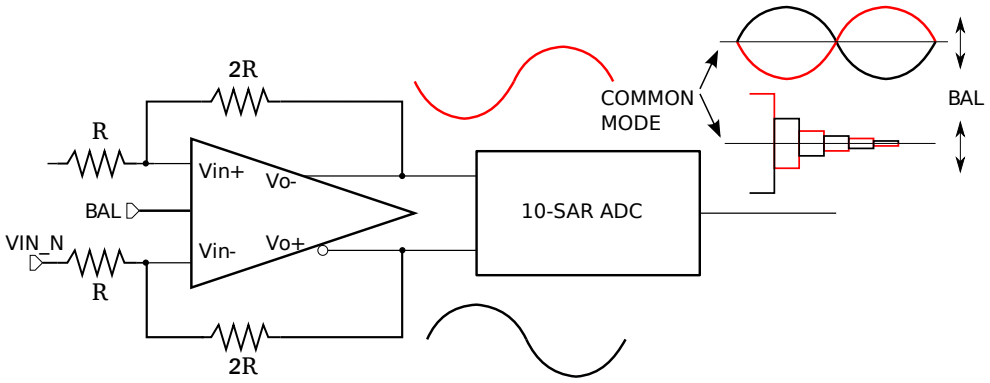

Figure 3.2: The influence of the adjustable BAL signal on common mode.

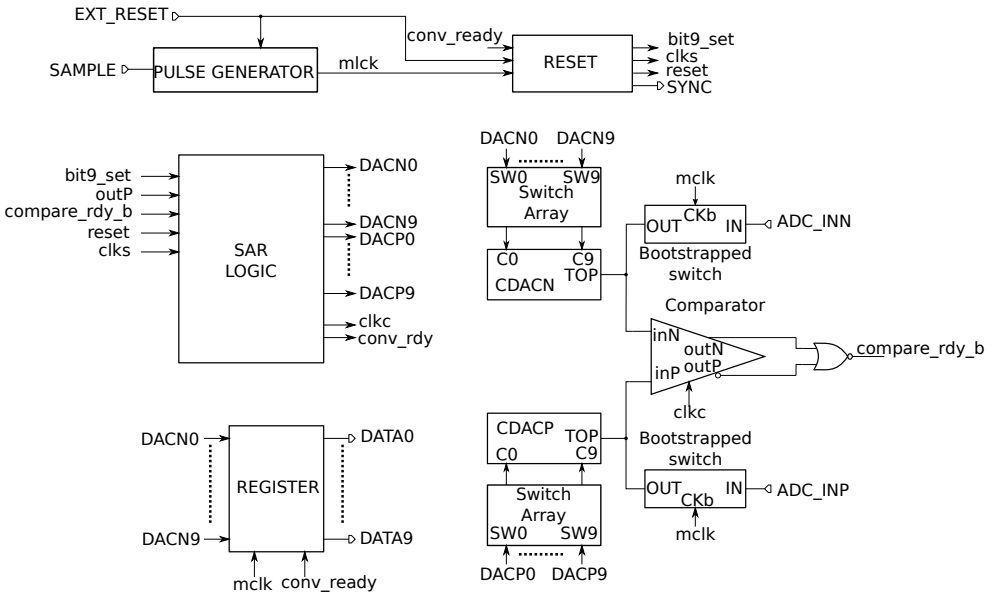

Figure 3.3: The 10-bit SAR ADC block schematic.

The top plates of all CDAC capacitors are connected to the input differential pair of the comparator. The approximation algorithm converges toward the common-mode that is set by the BAL signal. The comparator, shown in Fig 3.4, has a high voltage threshold (HVT) N-type metal-oxide-semiconductor (N-MOS) transistors at the differential pair input. The threshold voltage of HVT N-MOS in used technology is approximately 0.6 V.

When the comparator clock signal is at the low state, parasitic capacitances in the nodes AP and AN (shown in Fig. 3.4) are charged, and voltage at these nodes is equal to VDD. The output of the comparator resets transistors M12 and M13. When the clock goes high, M12 and M13 are switched off, AP and AN nodes start to discharge, and voltage at these nodes decreases according to the V_{GS} of M1 and M2. At the end of the successive approximation, the differences between V_{GS} of M1 and M2 are small, but the comparator has to

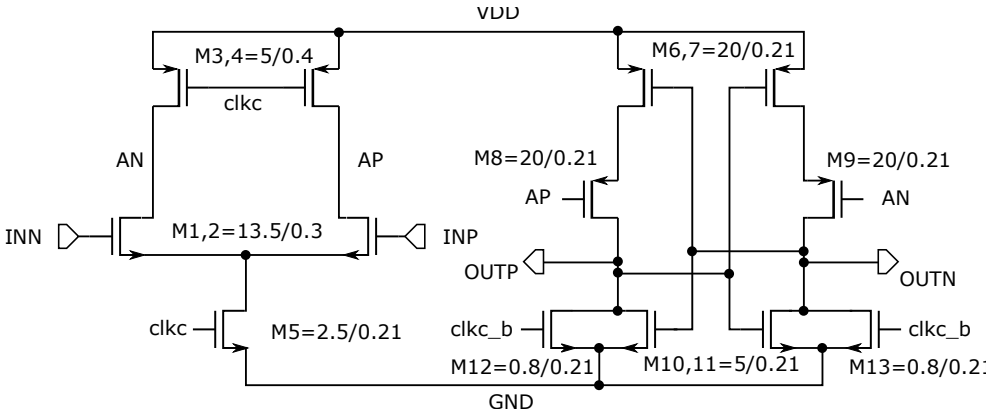

Figure 3.4: The 10-bit version comparator design.

decide correctly to reach the 10-bit resolution. When the BAL signal is set around the HVT N-MOS threshold voltage, the discharging of AP and AN nodes is slow, and the output latch has more time to decide correctly. On the other hand, when the BAL signal is set 200-300 mV above the HVT N-MOS threshold voltage, discharging capacitances in the AP and AN nodes is fast, and the latch may decide incorrectly. Therefore, the BAL control signal directly affects the accuracy and speed of the proposed SAR ADC architecture.

3.2 10-bit SAR ADC

Block schematic of the proposed 10-bit SAR ADC is illustrated in Fig. 3.3. The pulse generator, reset, and bootstrapped switches remain identical to ones in the 8-bit version [A.1]. Capacitors in CDAC are switched to the voltage reference or ground using inverters. The largest capacitor uses an inverter with N-MOS W/L ratio 8/0.21 and P-MOS W/L ratio 24/0.21. The remaining switches are scaled-down by a factor of two up to the minimum value. The register is also easily extended using two more standard D-type circuits available in the used technology. The comparator, CDAC, and modified SAR logic are described in the following subsections.

3.2.1 10-bit foldback CDAC

The CDAC used in the 10-bit SAR ADC is entirely different in comparison with the previous 8-bit version. The unit capacitor, shown in Fig. 3.5 right, is designed using only one metal layer with the capacitance of 0.5 fF. The 10-bit binary-weighted version has 1024 capacitors in total. The common centroid layout technique is used. A principal illustration of the CDAC structure is shown in Fig. 3.5 left.

A standard CDAC design [1] interconnects unit capacitors from one side of CDAC and the capacitors on the other side connected to the ground compensate parasitic capacitances. The proposed folded CDAC architecture interconnects unit capacitors from both sides as is shown in Fig. 3.5. This approach reduces the CDAC height by half. The node

leading from CDAC to the comparator is connected by metal 1 and capacitor interconnections by metal 3 to decrease parasitic capacitances between these sensitive nodes.

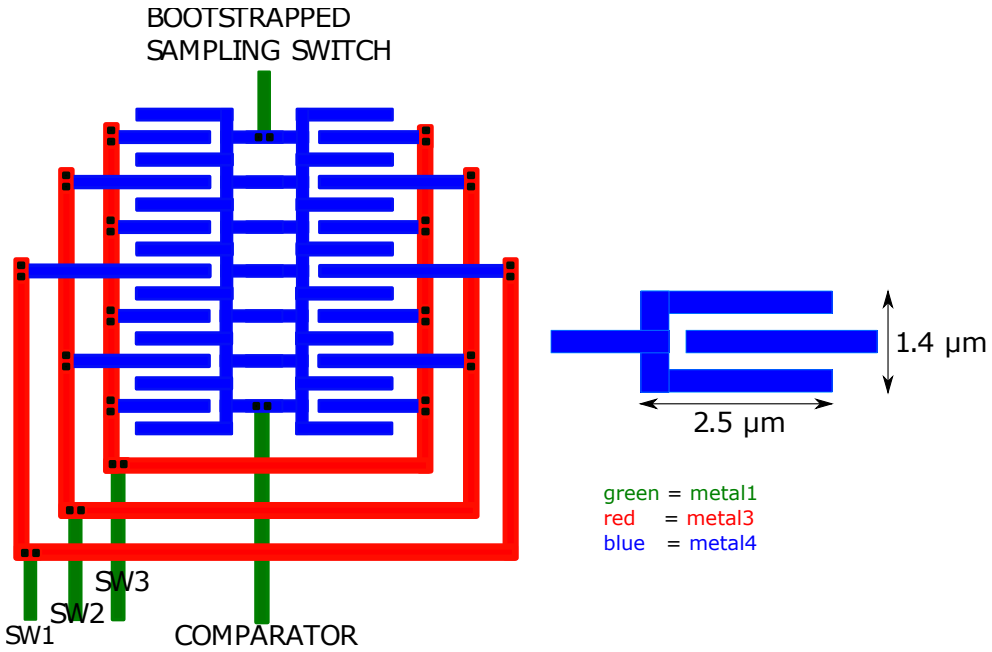

Figure 3.5: An example of 3-bit folded CDAC design.

Parasitic capacitances at the top plates of capacitors in CDAC have to be compensated because CDAC's height is around 800 µm. This compensation is done by adding a Metal-insulator-Metal (MIM) capacitor to the comparator node and by increasing ADC reference voltage as illustrated in Fig. 3.6.

The capacitance of the MIM capacitor is calculated as

$$C_{MIM} = V_{REF}\frac{C_{DAC}}{V_{OUT}} - C_{DAC} - C_{PAR}, \tag{3.3}$$

where V_{REF} is set to 1.5 V (bandgap reference voltage), V_{OUT} is the comparator input voltage, C_{DAC} is the total capacitance of CDAC equal to 512 fF, and C_{PAR} is the parasitic capacitance at the comparator input. The C_{PAR} is an unknown parameter that has to be determined by post-layout simulation. The C_{MIM} value is then easily calculated.

The second way to eliminate the parasitic capacitance at the comparator node is to leave C_{MIM} fixed and precisely adjust V_{REF} to get the linear transfer characteristic of the ADC. The capacitor mismatch was verified using Matlab software. Normalized standard deviation is calculated as

$$\frac{\sigma(C)}{C} = \frac{A_m^2}{WL}, \tag{3.4}$$

where C is the nominal unit capacitance 0.5 fF, A_m is Pelgrom coefficient found in the documentation of the used technology, and WL are dimensions of the unit capacitor.

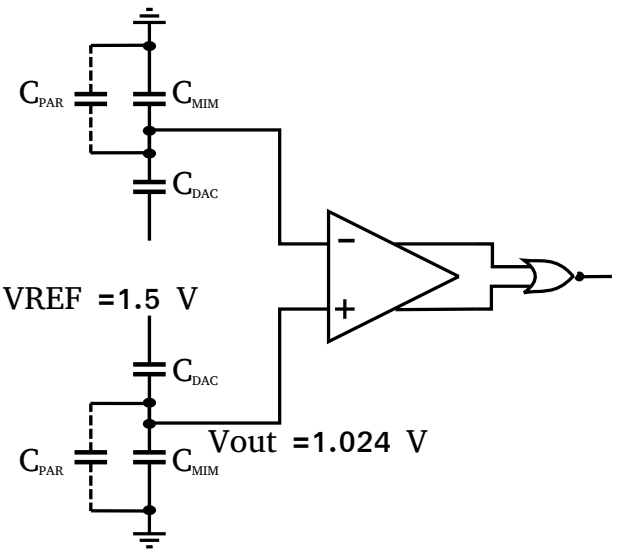

Figure 3.6: The compensation of parasitic capacitances of CDAC.

A calculated denormalized standard deviation was used for generating a set of all 1024 capacitors of both CDACs. Then the linearity was tested. Results, shown in Fig. 3.7, confirmed the ability of the capacitor design to reach desired 10-bit resolution.

3.2.2 Dynamic Comparator

The comparator design is shown in Fig. 3.4. The differential pair gain is around 9, and the latch transistor sizes are properly selected by simulation. The input-referred noise, calculated according to normal distribution method [17], is estimated to be 245 µV RMS (root mean square).

The comparator layout is shown in Fig. 3.8. Transistors are divided into odd fingers to connect dummy transistors and keep the same capacitance at the AP and AN nodes. The symmetry of the layout is essential in order to keep the same metal lengths of the critical nodes, AP, AN, and latch. The comparator output is buffered, because one of the outputs is connected to the SAR logic with a long metal with a large parasitic capacitance.

3.2.3 Asynchronous SAR logic

Based on the reference [1], the asynchronous SAR logic utilizes a modular concept easily extendable from 8-bits to 10-bits. The used switching scheme is illustrated in Fig. 2.5. In the sampling phase is differential voltage connected to the capacitors top plates through switches S1 and S2. At the same time is MSB switched on VREF and other bits to the ground. The benefit of switching the MSB in the sampling phase is that successive approximation converges toward to common-mode V_{CM}. In the second step, switches are S1 and S2 off, and the comparator decides MSB bit. Then the algorithm tests individual bits

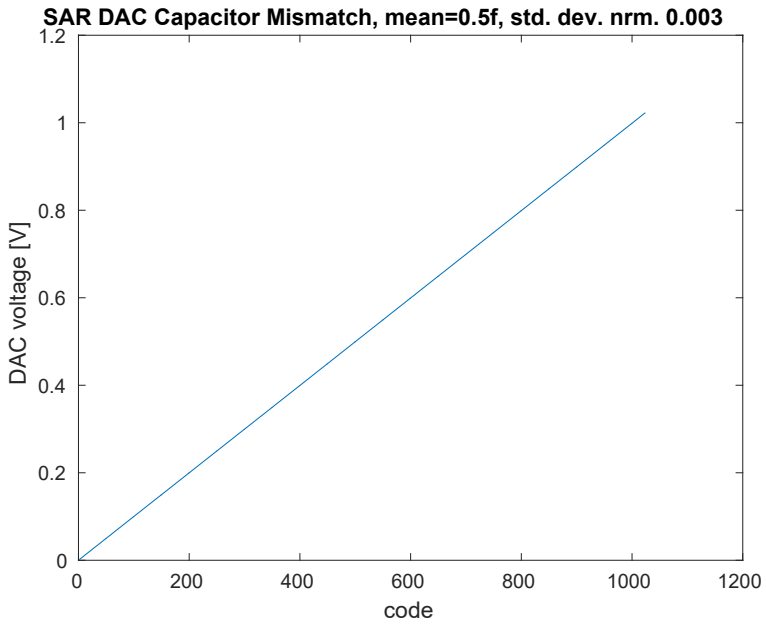

Figure 3.7: The capacitor mismatch simulation in Matlab

as illustrated in Fig. 2.5. Advantages of this low power switching scheme are convergence to common mode, no redundant switching, and simple components (inverters are used for the bottom plate switching.

The modular asynchronous logic concept is illustrated in Fig. 3.10. The signal *mclk* initiates the 10-bit conversion. Each module generates clock pulses (*clkc*) for the comparator through OR gates. The comparison is allowed by *compare_rdy_b* signal from the comparator. The *compare_rdy_b* generates a NOR gate connected at the differential comparator output (not illustrated). The result of a comparison, the signal *outP*, is sampled in each bit. When a conversion cycle is finished, the *conv_rdy* signal latches data in the 10-bit register.

Single bit operation shows Fig. 3.11. The particular bit is set (1) with the signal *bit_set*. The delay between signals *bit_set* and *bit_rdy* ensures voltage setting on CDAC (2). This delay has to be set by simulation. A comparison is initiated when the bit is ready with *compare_b* (3). The comparator output *outP* is sampled when the signal *compare_rdy_b* goes low (4). The *compare_rdy_b* signalizes valid data on the comparator output. The next bit is operation is initiated by *next_bit_set* (5).

The main control and the DAC control in each of bit are simple state machines that can be specified using state diagrams shown in Fig. 3.12.

Harpe et al. [1] built DAC control and main control using few transistors and parasitic capacitances. SAR logic is initialized by a reset signal that charges the parasitic capacitances in their design. However, in the Spacepix-2 detector application, when a long period between samplings is used (a long acquisition time), these small capacitances are discharged by a leakage current that may result in an error in the SAR register. Therefore,

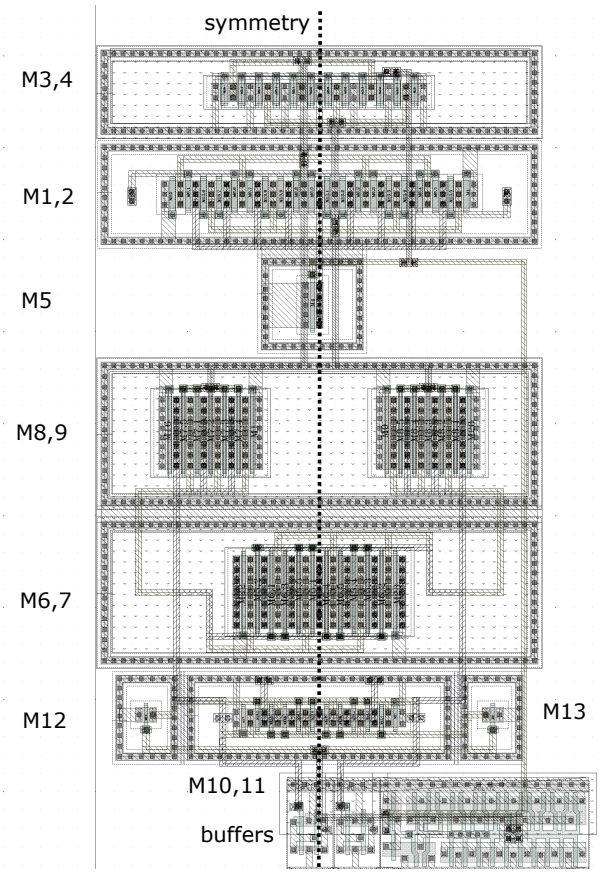

Figure 3.8: The layout of the comparator.

the DAC control in Fig. 3.13 and the main control in Fig. 3.14 are redesigned using standard cells in the used 180 nm SoI technology. The delay cells I6, I7 in the main control, and I11 in the DAC control are validated by a simulation to ensure the proper operation and settling time of CDAC switches.

3.3 Layout

Individual column SAR ADCs are placed one next to the other. The total length of the layout is 923 µm and the width is 120 µm (2 × pixel size). The new column 10-bit ADC layout is shown in Fig. 3.15. On the top, analog front-end is placed consisting of the ADC driver, input buffers, CMOS switches and asynchronous FSM that drives successive conversion of the left and right columns. Two CDACs are in the middle of the layout. Above the CDACs, the sampling bootstrapped switches are placed to decrease the parasitic sensitive node length to a minimum. The bootstrapped switches connect the input voltage on the top of both CDAC's as illustrated in Fig. 3.5. Under the CDAC is placed the comparator and inverters for CDAC capacitors switching. The SAR logic and output registers are at the bottom.

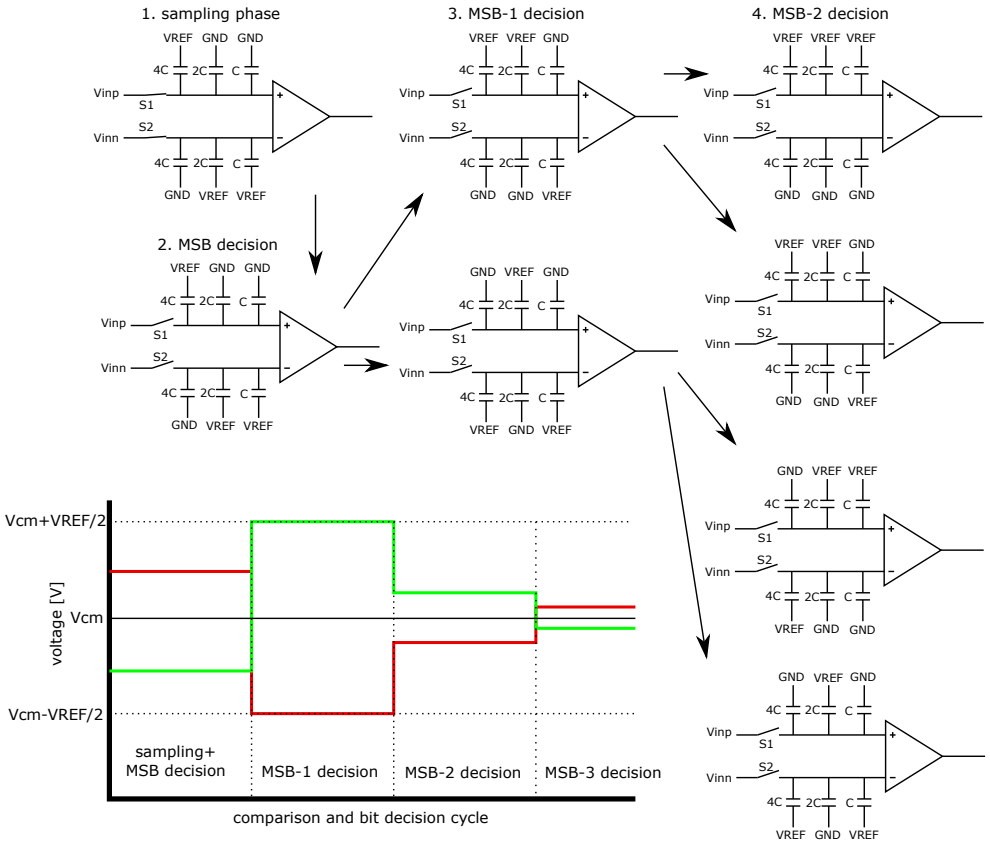

Figure 3.9: The used switching scheme.

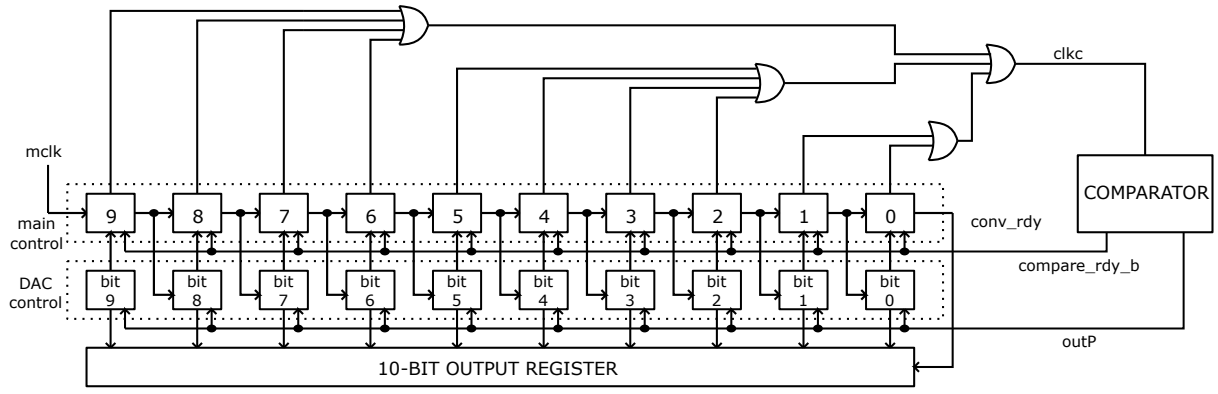

Figure 3.10: The simplified block diagram of the asynchronous 10-bit SAR logic.

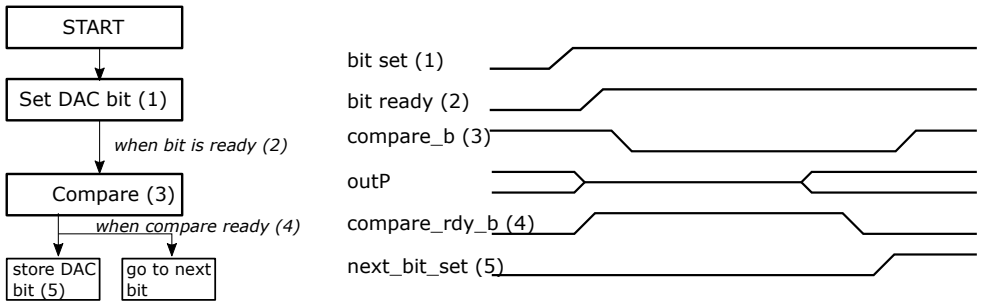

Figure 3.11: The timing diagram of single SAR logic bit (not to scale) [1].

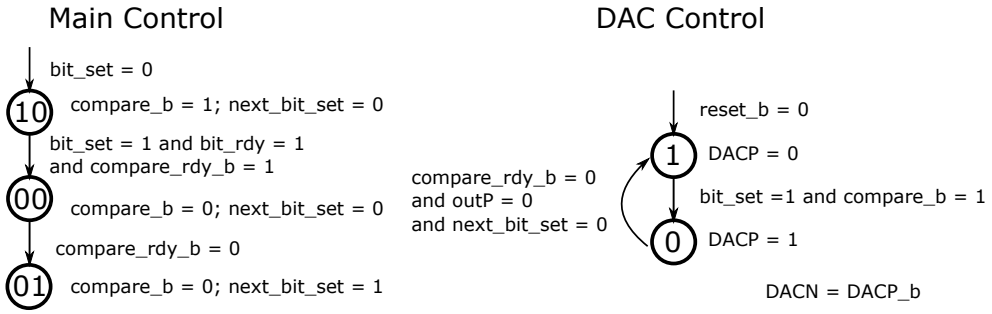

Figure 3.12: The main control and DAC control finite state diagrams [1].

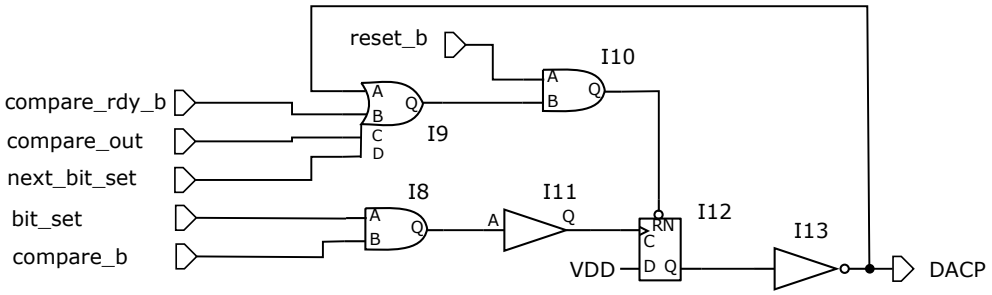

Figure 3.13: The DAC control

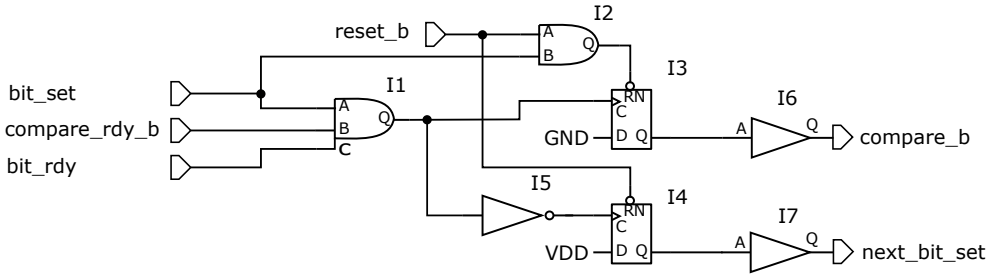

Figure 3.14: The main control

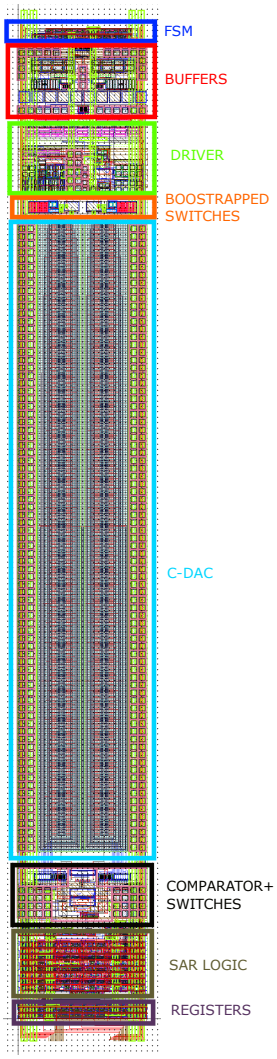

Figure 3.15: The 10-bit column ADC layout

A detailed illustration of the layout is shown in Fig. 3.16. On the top, the inputs from the left and the right columns are connected to the analog front-end (buffers, ADC driver and FSM). Then, the differential input signal is switched to CDAC through bootstrapped switches when sampling occurs. On the top of CDAC, the MIM capacitors are used for CDAC parasitic capacitance compensation as explained in Fig. 3.6. The bottom of the capacitor top plates is connected to the comparator by the lowest possible metal. The highest metal makes the interconnection between unit capacitors in order to reduce parasitic capacitances in these critical metals crossings. Along the left and right side, power lines for digital and analog column power supply are lead without an interruption of ADC performance.

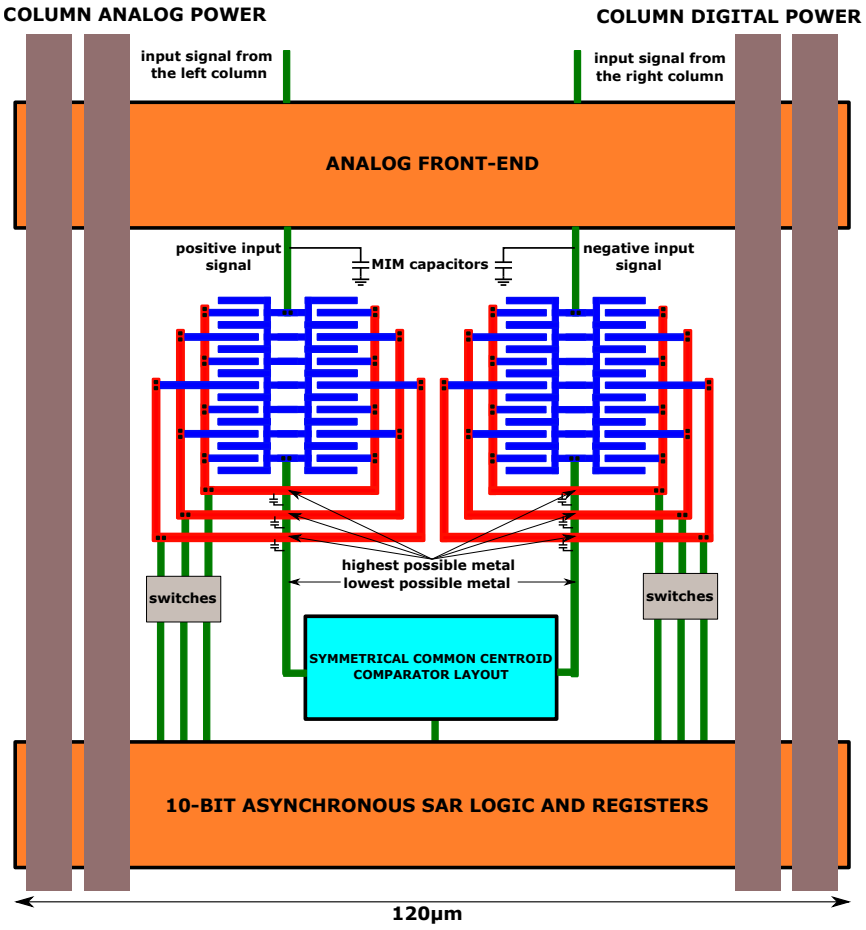

Figure 3.16: The 10-bit column ADC layout in detail.

Chapter 4

Software and Electronics for Spacepix Detector Read-out

This chapter briefly describes tools, designed PCBs, and software for the Spacepix detector read-out. The Spacepix ASIC is controlled using SPI or LVDS interface. A software and read-out electronics have to be developed to receive data from the detector and test the proposed column ADC design in chapters 2, 3. The read-out electronics and software, functionally illustrated in Fig. 4.1, were previously developed for XCHIP03 MAPS detector [20]. As described in this chapter, the same hardware and software were modified to control and send data from/to the Spacepix detector.

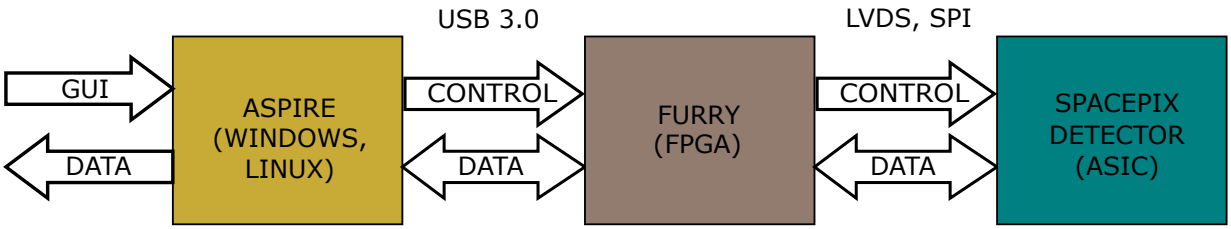

Figure 4.1: The functional illustration of the read-out flow for XCHIP03 and Spacepix MAPS detectors.

The left block in Fig. 4.1, named ASPIRE, is the application for Windows and Linux operating systems. ASPIRE communicates with a fast read-out interface (FURRy) using USB 3.0. FURRy controls the Spacepix detector and sends or receives data from/to the sensor with SPI or LVDS interface. Spacepix ASIC is fixed and wire-bonded on daughter-board PCB. These individual blocks in Fig. 4.1 describe the following subsections.

4.1 Spacepix Daughter-boards

The daughter-board purpose is to fix the Spacepix ASIC on the PCB, interconnect chip pins with FURRy connector, and provide additional circuitry for proper chip functionality.

There are two different daughter-board PCBs for the 8-bit and the 10-bit column ADCs. The 8-bit version is used in Spacepix-1 ASIC, and the 10-bit is used in Spacepix-2 ASIC. Each of ASICs has a different pin-out and dimensions.

Spacepix-1 has a pixel matrix with 32 rows and 64 columns, and chip dimensions are 3.03×3.98 mm^2. Fig. 4.2 shows the daughter-board PCB. Dimensions of the PCB are 70×40 mm^2. A schematic diagram is attached in appendix A. On the top PCB side is a wire-bonded Spacepix-1 ASIC and also temperature sensors U2 and U6. On the bottom PCB side is 40-pin FURRy connector, LVDS buffer U4, and chip noise filtration circuits.

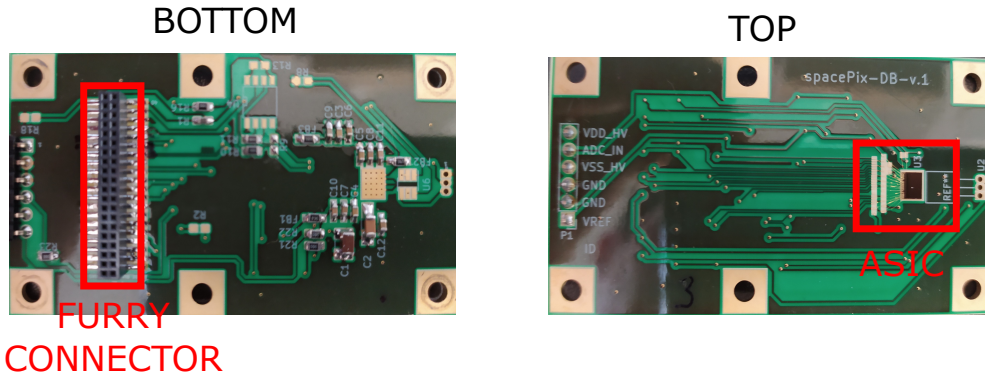

Figure 4.2: The Spacepix-1 daughter PCB.

Spacepix-2 has the pixel matrix with 64 rows and 64 columns, and chip dimensions are 4×5.64 mm^2. Fig. 4.3 shows the daughter-board PCB. Dimensions of the PCB are 50×40 mm^2. A schematic diagram is attached in appendix B. On the top PCB side is wire-bonded Spacepix-2 ASIC, LEDs D1-D3 signalizing power at all thee power domains, and connectors for control measurements J2, J3, J5. On the bottom PCB side are placed temperature sensors U2, U4, bandgap reference for ADCs U3, LDO regulator for the bandgap reference U5, power filtration circuits, and the 40-pin FURRy connector.

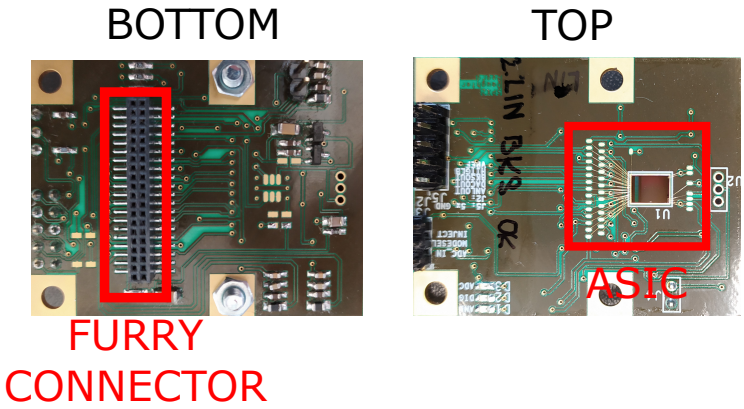

Figure 4.3: The Spacepix-2 daughter PCB.

RO4350B material is used for manufacturing of both PCB's for a low deflection during wire-bonding.

4.2 Fast Read-out Interface (FURRy)

The FURRy, shown in Fig. 4.4, interconnects the Spacepix daughter PCB with ASPIRE application. FURRy perform these important tasks:

- Receives commands and configuration data from ASPIRE with USB 3.0
- Sends the configuration to the Spacepix chip
- Performs read-out tasks from the detector
- Sends data from the detector to ASPIRE by USB 3.0
- Provides 3 x 1.8 V power supply domains for Spacepix ASIC

Figure 4.4: The Fast Read-out Interface (FURRy).

FURRy uses Spartan 6 FPGA for generating control signals and LVDS data transmission from/to Spacepix ASIC. FURRy is primarily designed for the XCHIP-03 chip [20]. Necessary modifications were performed in the Verilog firmware code to communicate and read-out the data from Spacepix detectors. Details about firmware modifications are out of the scope of this thesis.

4.3 ASPIRE

As shown in Fig. 4.5, ASPIRE is an application for Windows and Linux operating systems. The main task of ASPIRE is to control the MAPS detector and store or visualize incoming data from the detector. For the proposed both column ADCs testing are important the following features:

- Set appropriate exposition time
- Load and modify the chip configuration (including ADC configuration)
- Visualise measured data from the detector

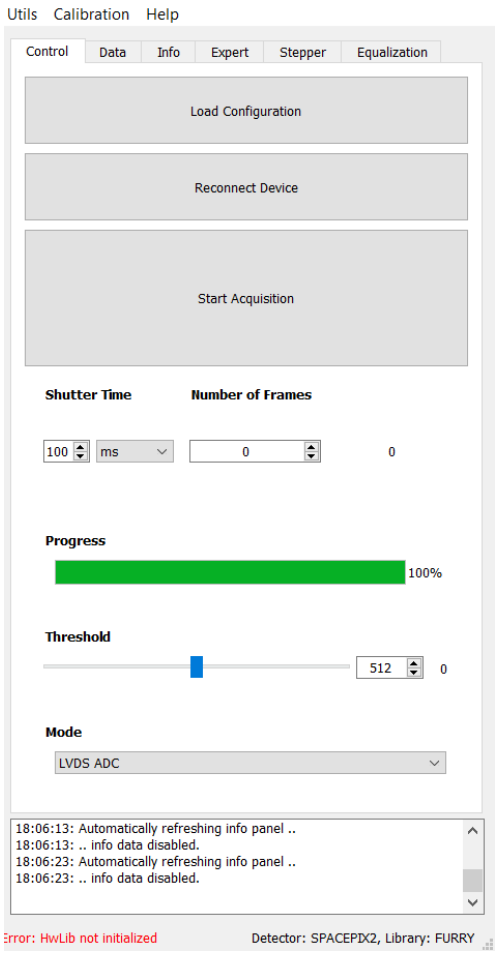

Figure 4.5: ASPIRE

- Store data from the detector in a file. The created file is then possible to process with, for example, Matlab and plot ADC characteristics.

The detector requires to load configuration before measurements. Spacepix chips have two configurations, global and local. The local configures the pixel matrix, and the global configure the rest of the chip, including the column ADC. Tab. 4.1 shows the global configuration settings for the 10-bit ADC version. In the 8-bit ADC version are the VIN_N and the BAL settings merged into a common setting. It is shown to be impractical, and these settings are separated in the 10-bit version.

4.4 ADC measurement setup

The Spacepix MAPS detectors in all submitted version allow the user to test column ADC using the external pin depicted in Fig. 3.1. With this chip pin is possible to connect

Settings	Default Value	Description
SAMPLE LENGTH	128	Time when the boostsrapped switches are opened. This time has to be large enough to settle voltage at the CDAC
BUFFER BIAS	128	Sets bias current of the input buffers. It is 5 µA by default
DRIVER BIAS	128	Sets bias current of ADC driver. It is 15 µA by default
VIN_N	731	This voltage DAC is able to shift ADC charateristics by a constant value. By default is set to 512 mV, where the input voltage corresponds to the output ADC value with zero offset.
BAL	731	Sets DC voltage value of common mode of the ADC driver. This voltage DAC influence the speed of the comparator and thus has an impact to ADC accuracy as desribed in Chapter 3

Table 4.1: The ADC setting of the global configuration of the Spacepix-2 detector.

a the same external voltage to all 32 ADCs in the chip. The measurement setup used for 8-bit and 10-bit column ADC testing is shown in Fig 4.6.

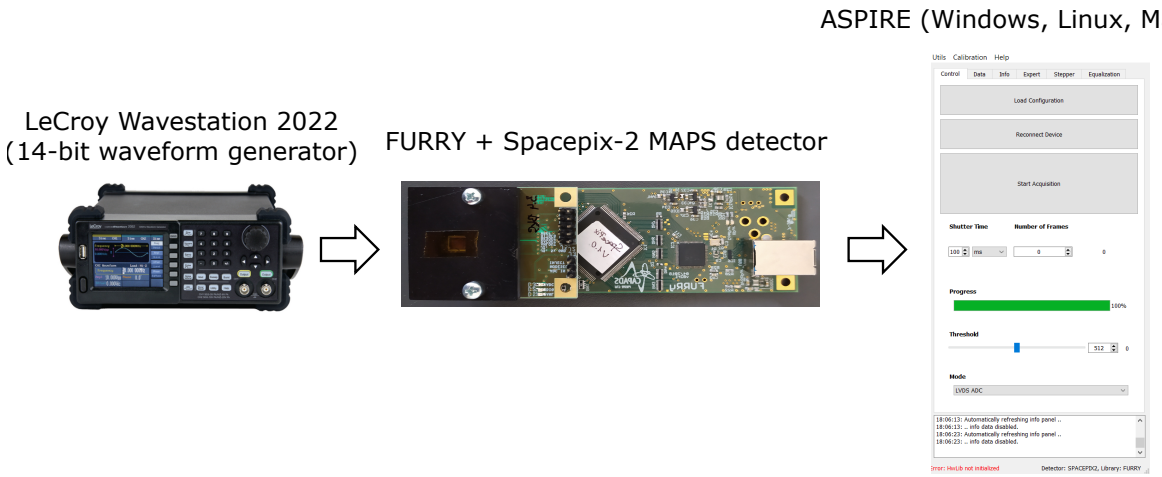

Figure 4.6: The used ADC measurement setup.

The principle of ADC measurement is the following: The LeCroy Wavestation 2022 generates a slow triangle type waveform to ADC input. The increment of the triangular waveform is 125 µV per sample (1/8 LSB in the 10-bit ADC). Data from the detector are collected by ASPIRE application and stored in a text file. The file is then processed by a Matlab code to analyse an ADC performance.

4.5 Inject

The Spacepix-2 MAPS detector allows the user to test and calibre a pixel front-end electronics using a testing pin called inject. All of the pixels in the pixel matrix can be calibrated and tested independently. In injecting mode, a DC voltage level at the ADC IN pin is set, and when the acquisition takes place, the INJECT pin goes from high (1.8 V) to low (0 V). By this way is injected charge to the charge summing amplifier without the need of activating the associated sensor.

Chapter 5

Results

This chapter shows achieved results from simulations and measurements of the manufactured ASICs Spacepix-1, in section 5.1, and Spacepix-2, Spacepix-2-lin-a, in section 5.2. In Spacepix-1 is used 8-bit column ADC version described in chapter 2. In Spacepix-2 and Spacepix-2-lin-a is used 10-bit column ADC version described in chapter 3. All Spacepix ASICs were implemented in a 180 nm SoI CMOS technology.

5.1 8-bit column ADC results

This section provides the simulated and measured results of the implemented prototype of the 8-bit column ADC, used in the Spacepix-1 MAPS detector. Simulated integral and differential nonlinearities (INL, DNL) in proposed corners in used technology are shown in Fig. 5.1 and Fig. 5.2. These nonlinearities have been extracted from the transfer function with a gradually increased 1 mV (0.25 LSB) step at the buffer input. The worse case DNL is held within 1 LSB and -0.5 LSB and INL between 1 LSB and -2 LSB.

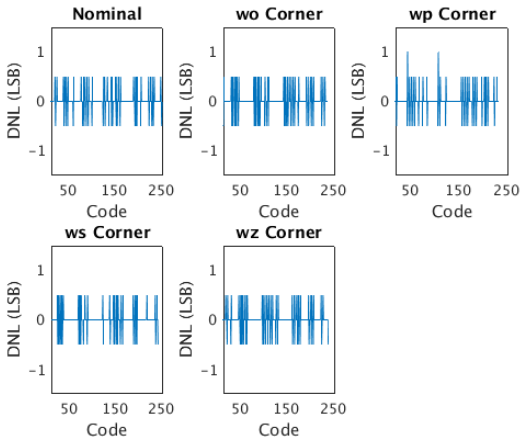

Figure 5.1: The simulated DNL.

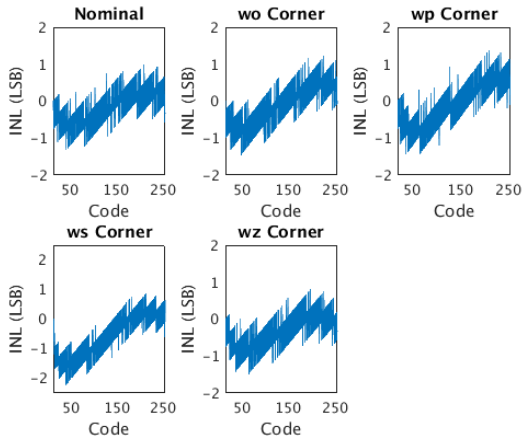

Figure 5.2: The simulated INL.

The measurement method described in section 4.4 was used to test the 8-bit column ADC functionality and linearities. The voltage step of 1 mV (1/4 LSB) per ADC conversion was used for testing the 8-bit version.

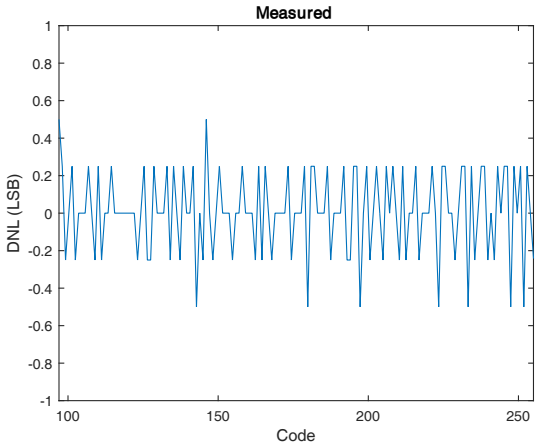

Figure 5.3: The measured DNL.

The measurements have revealed a problem with limited input range of the ADC. ADC does not react to input voltages below the code 100. The problem is caused by the incorrect layout of a PMOS voltage divider which sets 512 mV from the ADC voltage reference for the BAL input of the fully differential amplifier. The BAL signal is lower than 512 mV resulting in a limited output voltage range. However, the problem occurs outside of the presented design; therefore, it does not influence the presented solution. The problem was understood and will be eliminated in future circuit re-designs. The limited range is shown in Fig. 5.5. Measured and calculated DNL and INL are shown in Fig. 5.3 and Fig. 5.4 respectively. These nonlinearities are calculated from the transfer function shown

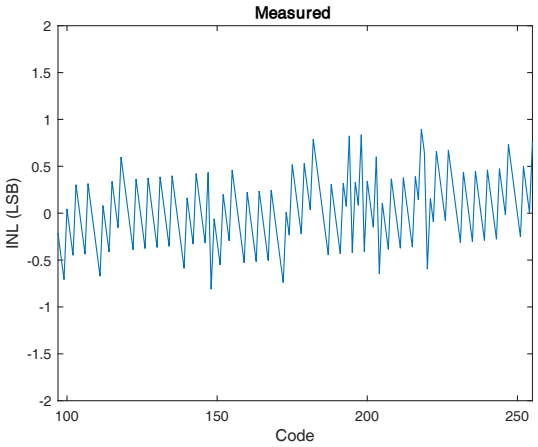

Figure 5.4: The measured INL.

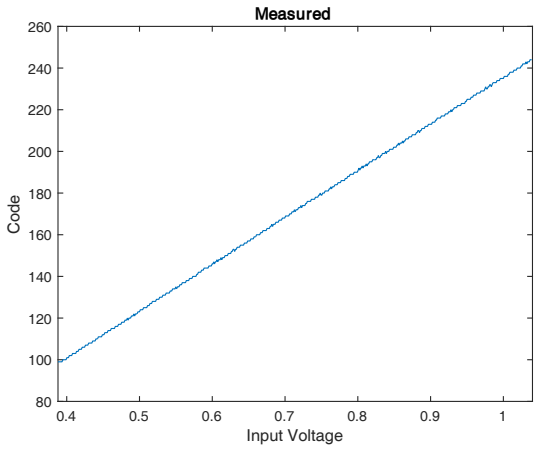

Figure 5.5: The measured transfer function.

in Fig. 5.5 at the range in which the ADC is working. All 32 column ADCs of the single monolithic pixel detector were measured. Their DNL is held within 0.5 LSB and - 0.75 LSB and INL are held within 1 LSB and -1 LSB. The results of one column ADC in Fig. 5.3, Fig. 5.4 and Fig. 5.5 are shown because nonlinearities from other column ADCs are also held at the same range. This indicates a low process variability of the proposed solution. Comparing simulated and measured results shows that the proposed design works as expected at the limited range.

The overall power consumption for all 32 8-bit SAR ADCs, including ADC drivers, is 3.1 mA from 1.8 V power supply. One SAR ADC with a ADC driver consumes 180 µW from 1.8V at 10 frames per second readout speed. The sampling frequency is 4 MSps. It means that within 1 µs are sampled voltages from odd and even columns.

Tab. 5.1 compares the proposed 8-bit column ADC with other solutions. The benefit of the proposed design is low power consumption, speed and differential architecture.

	Dasgupta 2014 [11]	Culurciello 2006 [10]	Havranek 2019 [12]	This work
Architecture	differential	single-ended	single-ended	differential
Bit	10	8	10	8
Speed (MS/s)	20	1.23	0.25	4
INL (LSB)	-	0.87	1.5	1
DNL (LSB)	-	0.18	1	0.75
Power (µW)	900	770	150	200
Area (μm^2)	310 × 190	450 × 315	57.5 × 480	115 × 445

Table 5.1: The comparison of the proposed 8-bit design with other column SAR ADCs.

Cell	Spacepix-2	Spacepix-2-lin-a
Comparator	the same as in the 8-bit version Fig. 2.14	resized transitors Fig. 3.4
SAR logic	the same as in the 8-bit version Fig. 2.11	redesigned usign stadard cells, Fig. 3.13 and Fig. 3.14
Other cells	the same as described in section 3 in both versions	

Table 5.2: The design differences between Spacepix-2 and Spacepix-2-lin-a ASICs.

5.2 10-bit column ADC Results

Two versions of the 10-bit column ADC were manufactured in the 180 nm SoI technology. This section describes the results obtained from the measurements. For more clarity, the versions are divided to individual subsections 5.2.1 (the first submission) and 5.2.2 (the second submission). Both Spacepix-2 detector versions allow the user to test ADC characteristics using the external pin that is connected to the inputs of all 32 ADCs in the chip as depicted in Fig. 3.1. The measurement setup is explained in section 4.4. The following table 5.2 shows differences between Spacepix-2 and Spacepix-2-lin-a ASICs.

5.2.1 The Spacepix-2 ASIC measurement

The Spacepix-2 10-bit column ADC exploits the same comparator design and the SAR logic asynchronous controller architecture as in the 8-bit version. The SAR logic is only extended by two bits. Three MAPS detector samples were measured from one part of the area on the wafer. One MAPS detector sample was measured from another area on the wafer.

Several different approaches can be used to test ADC performance. Typically, integral and differential nonlinearities, monotonicity, missing codes, or signal to noise ratio. During the first submission measurements, the dominant problem with missing codes was found. The problem with missing codes is critical for the MAPS detector performance because it precludes an user to distinguish adjacent peaks in a spectrum. Therefore, only missing codes and linearity are preferably examined in the first submission testing. DNL and INL characteristics are not calculated because they are useless in this case.

The Spacepix-2 10-bit ADC measurement is shown in Fig. 5.6. Three horizontal plots belong to three different tested chips, sample 1.1 to sample 1.3, respectively. The right plot is the transfer curve of all 32 columns ADCs in the chip when a ramp signal with the increment of 125 µV is applied at the ADC inputs.

The first difficulty is that there are no codes under code 170 and below. It is known from performed simulations that the input buffer does not reach zero voltage on the output when it is applied to the input. However, in the simulations were no codes from 100 and below. This difficulty has proven to be solved in the second submission described in the following section 5.2.2. The nonlinearity at the lower end of the transfer characteristic is also problematic. These difficulties cause that is not possible to see particles with a lower energy spectrum, such as Plutonium-238 or Iron-55.

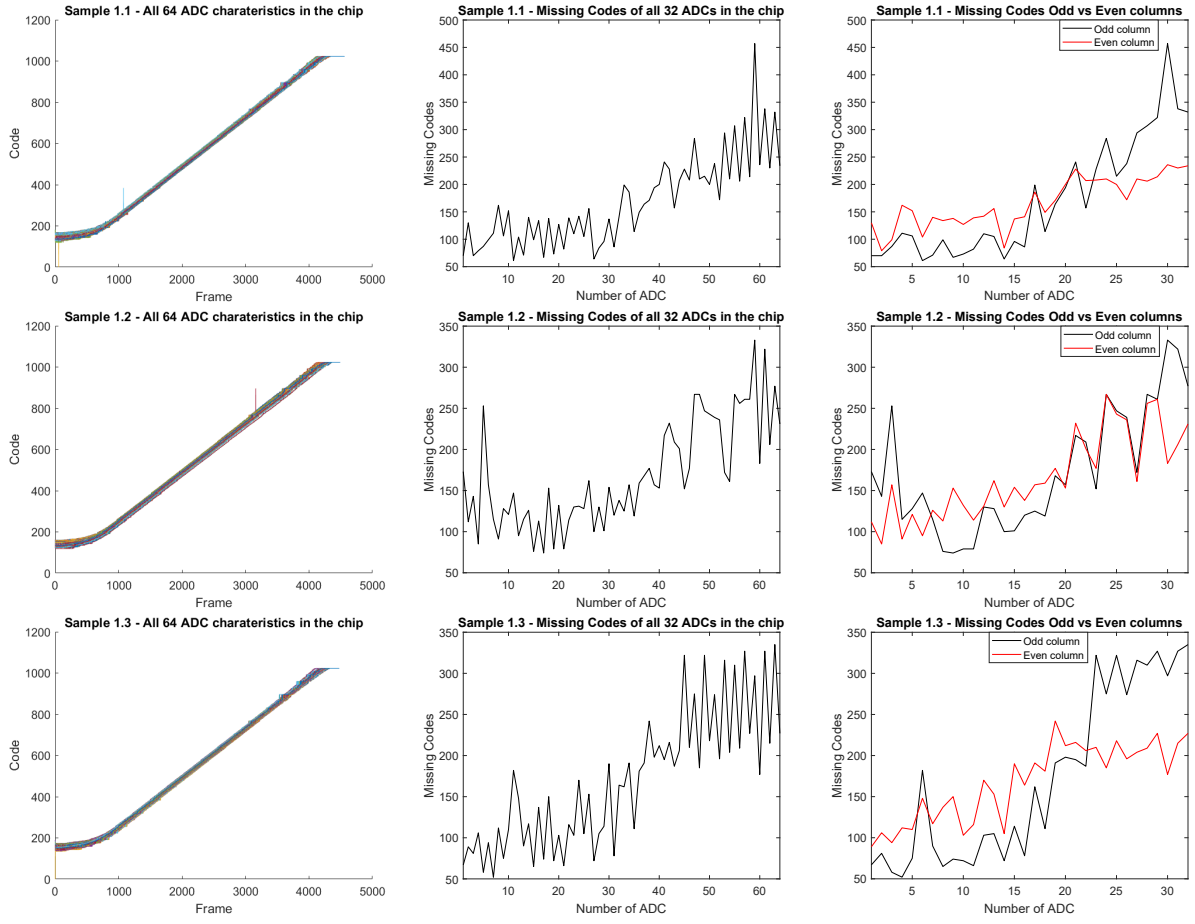

Figure 5.6: The missing codes measurement of chip samples 1.1-1.3.

Besides chip redesign, it is possible to solve this difficulty with shifting ADC power supply. The Spacepix-2 has three power supply domains: the analog, ADC and digital power supply domains. The ADC power supply can be shifted by 100 mV down with respect to analog and digital domains. The codes are than also shifted by 100 codes

down and it is possible to see particles with lower energies. This procedure was applied in Plutonium-238 measurement shown in Fig 5.8.

The second difficulty seen in the transfer curve of samples 1.1 and 1.2 is the peaks in one ADC transfer curve. The most probable reason for these unwanted peaks is an error in the asynchronous controller.

The third and more serious difficulty found during measurements are missing codes that can be seen in the middle plots for all of three samples. On the horizontal axis is the number of ADC from left to right on the chip. A single column ADC samples signals from two columns. The missing codes are on the right three plots divided in the odd column (the black curve) and the odd column (the red curve). From ADC number 1 to approximately ADC number 16 shows fewer missing codes than the rest. Another interesting observation is that the number of missing codes is slightly different for the same ADC. It means that in each measurement is obtained a different number of missing codes for the same ADC. This behavior is, to some extend, random. However, with a real measurement with the detector, this problem causes gaps in a spectrum. A single peak in a spectrum may appear as two different peaks.

Another Spacepix-2 detector from different part of the wafer was measured. The results are shown in Fig. 5.7. The transfer characteristics from all 64 columns look very similar as in Fig 5.6. The missing codes are more concentrated in the left half of the column ADC array.

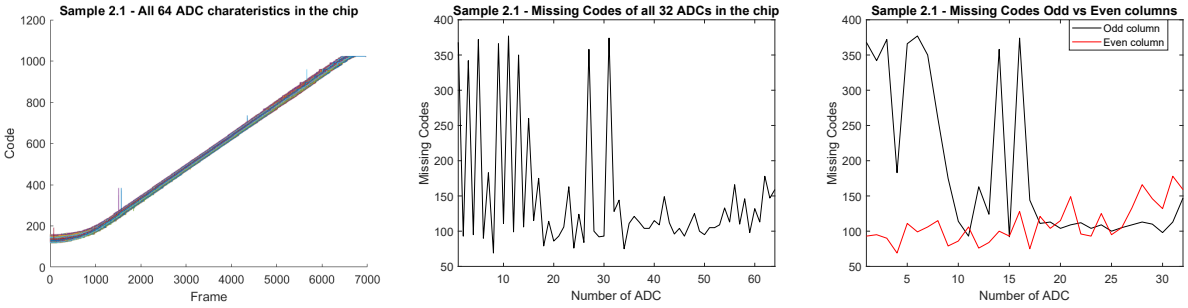

Figure 5.7: The missing codes measurement of chip sample 2.1.

The real measurement of Plutonium-238 with the Spacepix-2 MAPS detector is shown in Fig. 5.8. One hundred thousands samples were collected with an acquisition time of 1 ms. The ADC power supply was shifted by 100 mV (-100 mV / 1.7 V), as explained higher in this section, to obtain better resolution at the lower energies. Fig. 5.10 shows a measurement of various particles with XCHIP-03 MAPS detector [20] for comparison. Examination of Fig. 5.8 and Fig. 5.10 shows ability Spacepix-2 detector with proposed 10-bit column sampling to visualize Plutonium-238 (Pu-238) spectrum. This ability is also confirmed by injecting a current in a pixel. This testing method is described in section 4.5. The yellow curve in Fig.5.8 shows inject into pixels with energy spacing similar to Pu-238 spectrum. The inject confirms that the Spacepix-2 detector can differ three different peaks with spacing near Plutonium-238.

Each pixel and each ADC have a process variability. It means that each pixel gives a bit different value to the same inject level. Therefore, it is important to correct their variances using an equalization. Firstly, the mean ADC value from all pixels is calculated, and then a value is added or subtracted from individual pixels. In the measurement of Pu-238, was equalization performed at 40 ke (the blue curve in Fig. 5.8) and 16.4 ke (the red curve in Fig. 5.8). From Fig. 5.8 it is well visible that both equalizations provide similar results.

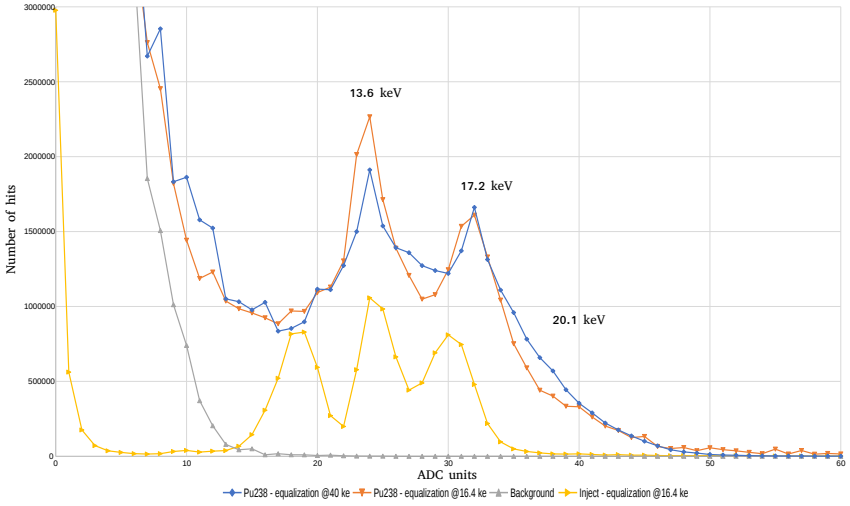

Figure 5.8: The Plutonium-238 spectrum measurement with the Spacepix-2 detector.

Another example of measurement with the Spacepix-2 detector in shown in Fig. 5.9. This time, an isotope of americium, Americium-241 (Am-241), was measured. Am-241 has a typical peak at 60 keV that is well visible at the measured spectrum in Fig. 5.9. Before the measurement, the equalization at 40 ke was performed.

5.2.2 The Spacepix-2-lin-A ASIC Measurement

The purpose of designing Spacepix-2-lin-a was to fix difficulties with missing codes and improve sensitivity at the lower energies. The Spacepix-2 measurement discussed in section 5.2.1 addressed these difficulties. Additional simulations reveal three problems in the 10-bit SAR ADC design. At first, the comparator design was improved by transistor resizing, and the comparator layout was modified to be more symmetrical. The second, in the asynchronous controller, certain states in the state machines DAC control and main control depend on parasitic capacitances. They are set by reset. However, a long reset period may cause the asynchronous controller to fail because a leakage current discharges these parasitic capacitances. For the above-stated reasons, the comparator and the asynchronous register were redesigned. The new comparator design is shown in Fig. 3.8 and the re-

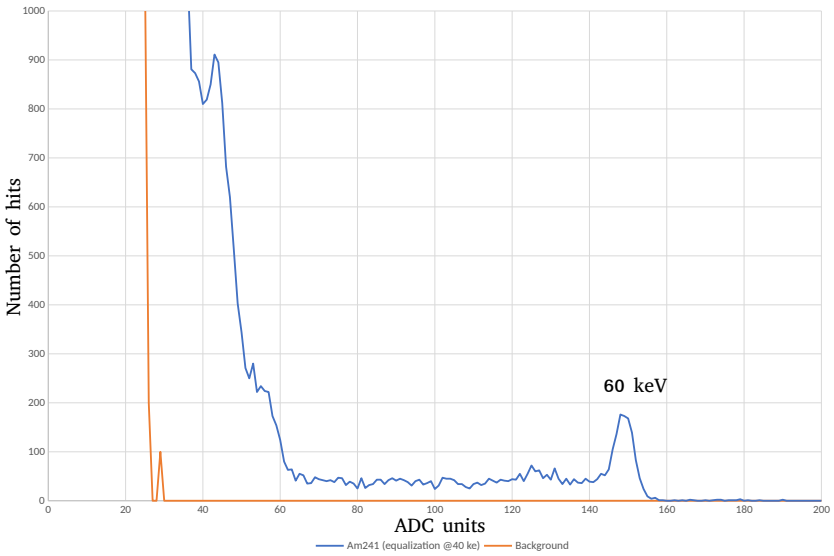

Figure 5.9: The Americium-241 spectrum measurement with the Spacepix-2 detector.

designed SAR logic in Fig. 3.13 and Fig. 3.14. Finally, the input op-amp buffer was redesigned to improve the detector's sensitivity to particles at the lower energy range.

Three samples of the Spacepix-2-lin-A were measured by the same method as the previous measurement of the Spacepix-2 described in section 4.4. The results are shown in Fig. 5.11. At first sight, missing codes are even worse than the Spacepix-2 version. On the other hand, performed simulations of the Spacepix-2-lin-a do not reveal any problem. The reason why measurements and simulation give different results is explained later in this chapter. Despite difficulties with the missing codes, the input buffers had improved linearity at the lower end of the ADC characteristic was reached. ADC works linearly from codes 75 to 1023 without the rounding at the lower transfer function that was seen in Fig. 5.6 in the left.

When the measured characteristics in Fig. 5.11 are exterminated more carefully, it can be seen that the missing codes of individual ADCs are different. The number of missing codes is from 800 to 80. While in the Spacepix-2 measurements in Fig. 5.6 it was from 300 to 80. For example, the ADC 11 of the sample chip 3.2 exploits the minimum number of missing codes compared to the rest ADCs of the sample chip 3.2. The results of the ADC 11 are shown in Fig. 5.12. On the left side of Fig. 5.12 is shown measured transfer function of ADC 11 of the 3.2 sample. It looks much better in comparison with the other ADCs in the chip. In the middle of Fig. 5.12 is shown calculated differential nonlinearity (DNL) of ADC 11. This DNL was calculated by a histogram method [2]. The right side of Fig. 5.12 shows calculated integral nonlinearity (INL) of ADC 11. The INL is calculated by the best fit method [2]. INL and DNL characteristics are not worth figuring for the ADCs where missing codes are the dominant factor.

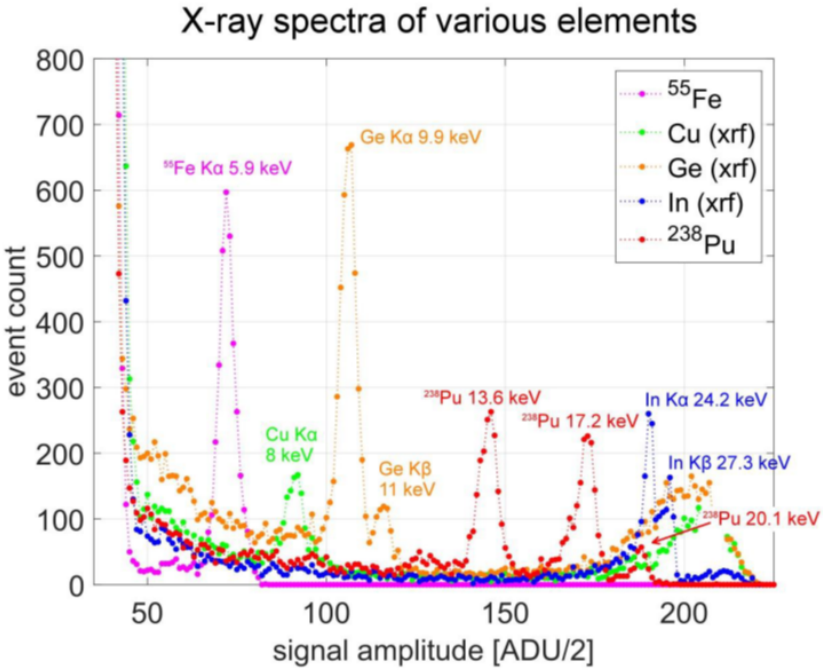

Figure 5.10: The measured spectra of different particles with the XCHIP-03 MAPS detector.

Spectrum measurement examples are not possible to perform with the Spacepix-2-lin-a because missing codes have large spaces in the ADC characteristics. These large spaces between codes precludes to obtain any reasonable spectra.

The MAPS detector ASIC architecture allows the user to adjust control voltages VIN_N, BAL, and bias for ADC driver and buffers. The measurement that may help to figure out the difficulty with missing codes is shown in Fig. 5.13. What happened is explained below.

In the Spacepix-2, ASIC is 10-bit DAC that sets VIN_N and BAL control voltages. A non-inverting op-amps buffer these voltages. This 10-bit DAC is connected between ground and power supply of 1.8 V. The following expression easily calculates the voltage value of 1 LSB

$$V_{LSB} = \frac{1.8}{1024} = 0.00176. \tag{5.1}$$

The 10-bit DAC works inversely. When the high code is set, the lower voltage at the DAC output is. The voltage at the DAC output is calculated as

$$V_{DAC_{out}} = 1.8 - DAC_{code} V_{LSB}, \tag{5.2}$$

where DAC_{code} is the value from 0-1023 set by user. In the case of the BAL settings of 954 is $V_{DAC_{out}}$ equal to 120 mV. It was verified by simulation, Fig. 5.14, that common-mode DC level when BAL 954 setting is 430 mV. The differential signal V_{o+} and V_{o-}

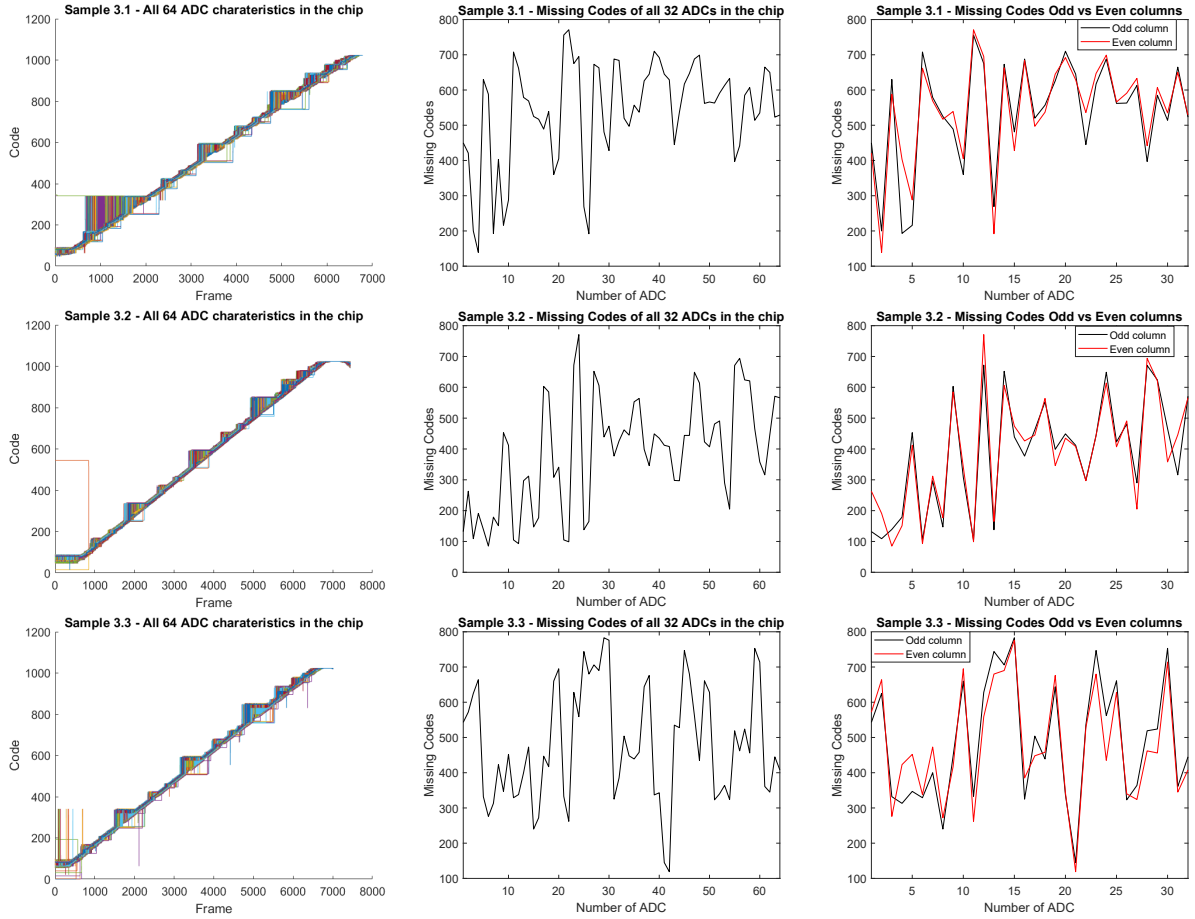

Figure 5.11: The Missing codes measurement of chip sample 3.1-3.3.

from the ADC driver is connected directly to the comparator input trough CDACs. When the successive approximation takes place, the differential voltage between V_{o+} and V_{o-} at the comparator input converges to the 430 mV common-mode set by the BAL signal. A differential successive approximation illustration is depicted in Fig. 3.2. It means that the comparator has to differ small-signal voltage differences (below 1 LSB) to reach a 10-bit resolution.

The comparator input NMOS transistors have, in used technology, the threshold voltage 0.6V. When the successive approximation converges to 430 mV, then the overdrive voltage of the NMOS transistor is -170 mV. This large negative overdrive voltage puts the NMOS transistor in the comparator in a deep sub-threshold regime where the drain current I_D is exponentially related to the voltage between gate and source V_{GS}. It means that a small change of V_{GS} causes a large change of I_D makes the comparator more sensitive to subtle V_{GS} changes.

However, another effect occurs in the proposed SAR ADC architecture when the BAL signal is set to the voltage level of 430 mV. Because of the NMOS transistors at the comparator input are in the deep sub-threshold region, their drain to source resistance R_{DS}

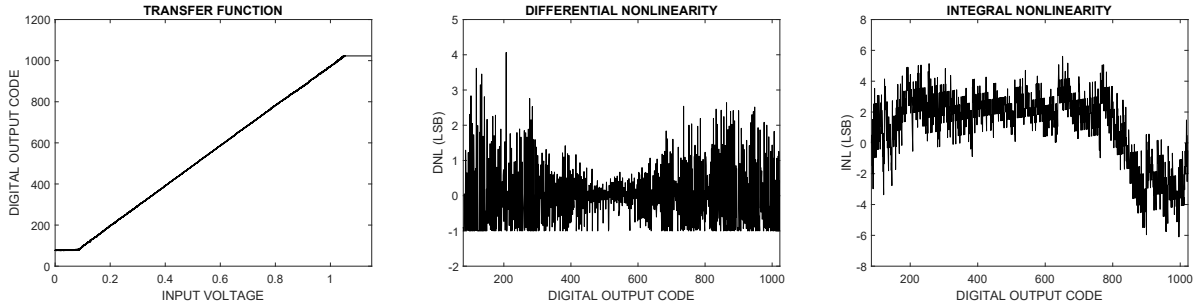

Figure 5.12: The measured transfer function and calculated INL, DNL of ADC 11 in the Spacepix-2-lin-a ASIC.

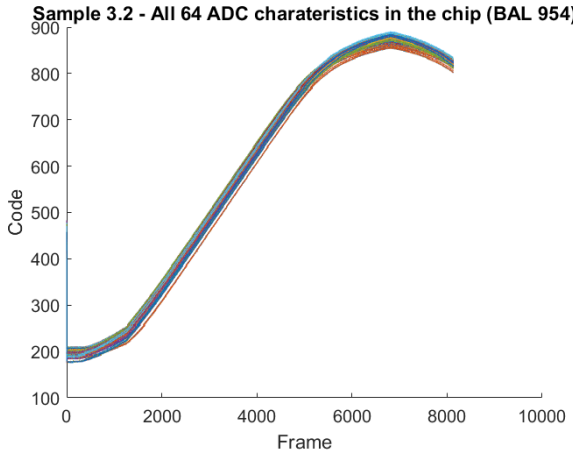

Figure 5.13: The measurement of the sample 3.2 with BAL control voltage settings at the level 954.

is significant. The working principle of the dynamic comparator is explained in sections 3.2.2 and 2.1.3.3. A Discharging speed of the nodes AP and AN in the dynamic comparator depends on R_{DS} of the differential pair NMOS transistors. When the R_{DS} of the NMOSs is small, then the comparison is faster. On the other hand, when the R_{DS} the NMOSs is high, then the comparison is slowed down. The slower comparator operation also causes a slower operation of the DAC control and the main control state machines depicted in Fig. 3.13 and Fig. 3.14. It means that the whole successive approximation algorithm is slowed down. Therefore, the most probable reason for the missing codes in the Spacepix-2-lin-a version is the inappropriate functionality of the SAR asynchronous register consisting of DAC control and main control in each of 10-bit. The Spacepix-2 version uses the transistor logic in the DAC control and the main control depicted in Fig. 2.11. In the Spacepix-2 are not observed these large skips in the ADC transfer characteristic.

By comparison, Fig. 5.13 and Fig. 5.14 is a well visible reduction of ADC dynamic range and camber at the ends of ADC transfer characteristic. In the normal operation, when the BAL signal is set to the DC level of 600 mV are signals from the ADC driver

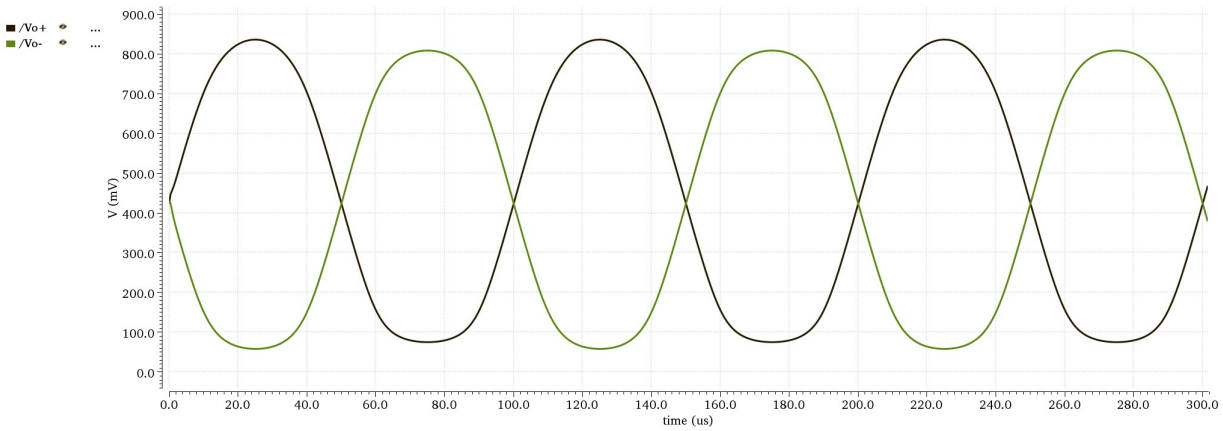

Figure 5.14: The simulation of the ADC driver output when 954 BAL settings.

linear as shown in Fig. 2.5.

The above-described symptoms signalize a failure of the proposed asynchronous logic. To examine the operation of the asynchronous controller, the DAC control in Fig. 3.13 and the main control in Fig. 3.14 were again carefully analyzed. A simple Verilog stimulus of the timing diagram in Fig. 2.9 was modelled to test the DAC control FSM. The state diagram of the DAC control is shown in Fig. 2.10.

In Fig. 5.15 is shown a comparison of the DAC control simulation between the standard cells design in Fig. 2.12 (on the left) and the transistor logic design in Fig. 2.11 (on the right).

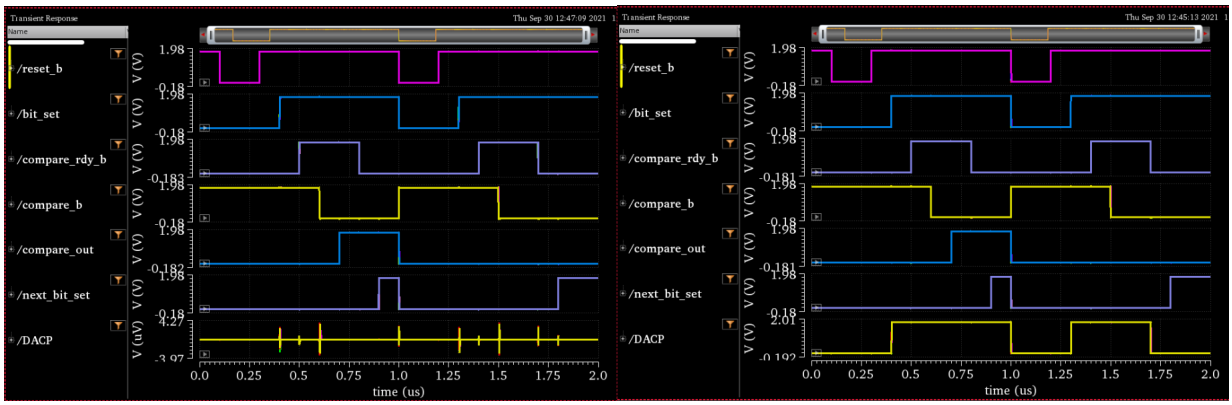

Figure 5.15: The comparison of the DAC control FSM simulation between the standard cells design in Fig. 2.12 (on the left) and the transistor logic design in Fig. 2.11 (on the right).

In Fig. 5.15 it is well visible that the DACP output of the DAC control is not set in the case of standard logic design in Fig. 2.12. The DAC control in Fig. 2.10 explains the reason why the DACP is not set. The FSM has to go from state 1 to state 0 when

the signals *bit_set* and *compare_b* are in the high state. In the transistor logic, is this transition possible because transistors M8 and M9 are on and the input of the inverter is pulled down; thus, DACP is set. In the case of standard cells logic, the flipflop (DFF) should be set at the rising edge of the signal *bit_set*. However, it is not because the DFF is still held in the reset state by signals $next_bit\_set$, *compare_rdy_b* and *compare_out* in the low state. The conclusion is that the logic proposed by the standard cells is inappropriately designed, and it does not provide the same logic function as the transistor logic design.

The standard cell DAC control design problem is that the I12 resets itself; it is an unacceptable logic concept. The delay I11 partially eliminates the error. However, there are tens of picoseconds between the case when the DACP output is set or not. PVT variations, noise, mismatch causes that some ADCs work better or worse than others. It is what we see in the performed measurements described above. These picoseconds fluctuations and the wrong DAC control design causes the large missing codes that we see in the measured ADC characteristics. Surprisingly, simulations in corners, Monte Carlo, and post-layout at the top level have not revealed the problem. The problem was seen only after a detailed examination of the DAC control FSM.

The last time Spacepix-2-lin-a post-layout simulations of the proposed 10-bit ADC has revealed the problem with missing codes. Cadence spectre APS simulator allows the user to set post-layout optimization. When the optimization option is enabled in simulation with settings 150 GHz (capacitors and resistors above this frequency are filtered out from netlist), the missing codes starts to appear in ADC characteristics. When the optimization is disabled, the missing codes disappear from the ADC characteristic. It means that the parasitics optimization intently deteriorate result of parasitic extraction. A mismatch between manufactured ASIC and used extraction tool causes that the missing codes are not seen in simulations but are visible in real measurements. The solution is to increase the unit capacitance. Fig. 5.16 shows a comparison of simulated missing codes with 0.5 fF (80 missing codes) and 1 fF (22 missing codes) unit capacitor in CDAC. Increasing the CDAC capacitance two times reduces the missing codes four times according simulation with enabled post-layout optimization.

Some of the ADCs in the Spacepix-2-lin-a were working, and the measured characteristics shown in Fig. 5.12 can be compared with other existing solutions of the MAPS detector columns ADC. The comparison is shown in the Tab. 5.3. This design is a faster sampling speed, and differential in comparison with Havranek's design [12] with similar power consumption. Design by Rarbi et al. [21] provides faster sampling speed but for the cost of higher power consumption and single ended architecture.

The overall power consumption for all 32 10-bit SAR ADCs, including ADC drivers, is 4 mA from 1.8 V power supply. One SAR ADC with a ADC driver consumes 225 µW from 1.8V at 10 frames per second readout speed. The sampling frequency is 4 MSps. It means that within 1 µs are sampled voltages from odd and even columns.

The part of the manufactured Spacepix-2-lin-a ASIC with a focus on column ADC is shown in Fig. 5.17. The detail shows some of the ADCs in the array under the pixel matrix. In the black frame, it is visible the proposed single column 10-bit ADC as shown in Fig. 3.15.

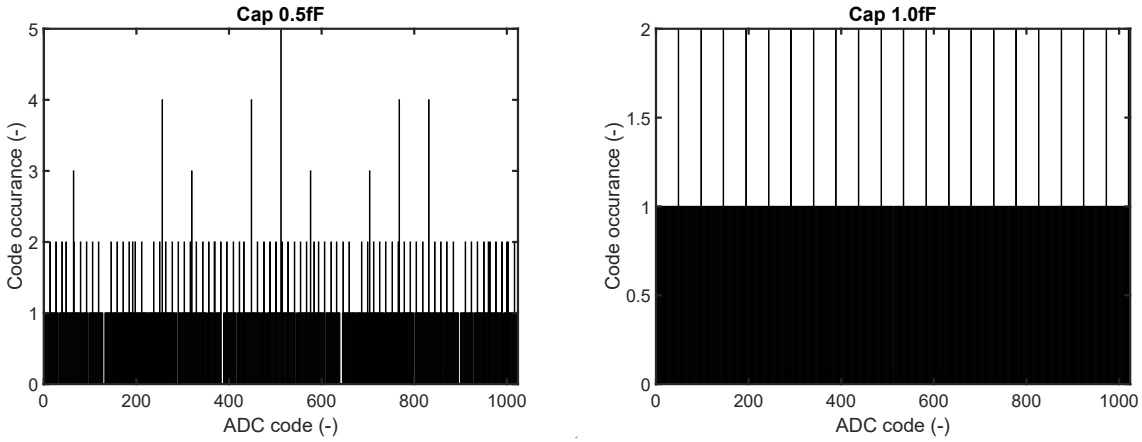

Figure 5.16: The missing codes comparison of post-layout simulation with enabled 150 GHz optimization of proposed 10-bit SAR ADC with 0.5 fF capacitor in CDAC (on the left) and 1 fF capacitor in CDAC (on the right).

	Rarbi 2017 [21]	Havranek 2019 [12]	Vancura 2020 [A.1]	This work
SAR architecture	single-ended	single-ended	differential	differential
Nubmer of bits	8	10	8	10
Max. INL (LSB)	-	1.5	1	5
Technology (nm)	65	180	180	180
Max. DNL(LSB)	-	1	0.75	5
Max. speed (MS/s)	100	0.25	4	4
Power (µW)	1550	150	200	225
Area (μm^2)	208.6×103.6	57.5×480	115×445	120×923

Table 5.3: The comparison of the proposed 10-bit design with other column SAR ADCs.

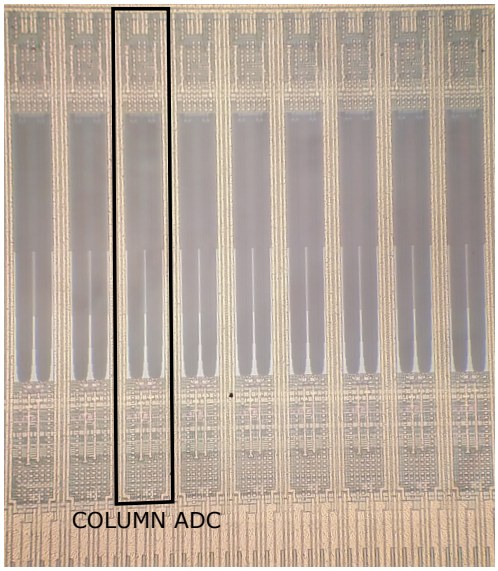

Figure 5.17: The microphotography of manufactured 10-bit column ADC used in the Spacepix-2-lin-a ASIC.

Conclusion

In this thesis is proposed a fully differential SAR column ADC design for a MAPS detector designed in 180 nm CMOS SoI technology. The primary difficulty in this design is the pixel width of 60 µm that complicates layout and deteriorates ADC linearity. Notably, the switched capacitor DAC (CDAC) layout design is complex since the fully differential architecture needs two CDACs. The unit capacitor in the CDAC array has to be sized as small as possible to maintain fast speed and low power consumption. On the other hand, the small unit capacitance more suffer from parasitic capacitances and deteriorates SAR ADC linearity. Another problem is converting a single-ended signal to a fully differential signal and maintain 2 MSps sampling rate.

These problems solved new architecture, published in 2020 [A.1], where the single column ADC has multiplexed input to two columns. In the Spacepix MAPS detectors, only 32 ADCs are needed for 64 columns pixel matrix. This new approach doubles the layout width. Therefore, the CDAC layout is more relaxed with good linearity. This unique design also reduces power consumption.

Two versions of column SAR ADC have been implemented, the 8-bit (Spacepix-1) and the 10-bit (Spacepix-2) version. The 8-bit version, published in 2020 [A.2], exploits 4.5 fF unit capacitors with the cage structure in CDAC design. This CDAC design was presented at the TWEPP conference in 2018 [A.3]. The total capacitance of a single CDAC is 1.152 pF. The method for matched layout structures assessment [A.5], [A.4] was used in comparator and CDAC designs. Differential and integral nonlinearities, for all 32 columns ADCs placed at the same chip, are held within 0.5 LSB, - 0.75 LSB, and 1 LSB, -1 LSB, respectively. It indicates a low process variability of the proposed solution. The problem with a limited range of ADC was detected during the testing of the implemented prototype. The limited range is caused by the incorrect layout of the PMOS voltage divider. The PMOS voltage divider is not part of the presented design; thereby, the presented work's relevancy is maintained. The maximum sampling rate is 2 MSps with power consumption 200 µW from 1.8 V power supply. The layout area occupies 445×120 μm^2.

The 10-bit column SAR ADC design, manufactured in 2021 [A.6], is an extended version of the 8-bit design. The asynchronous modular logic and registers were easily extended by two more bits. The double sampling concept remains the same. However, the CDAC design is entirely different in comparison with the 8-bit version. Only 0.5 fF MoM unit capacitors are used. The total capacitance of CDAC is only 512 fF, improving speed and lowering

power consumption. Two Spacepix-2 ASIC versions were designed. In the Spacepix-2, ASIC is used the 10-bit column ADC with the same comparator design and the same transistor SAR logic as in the 8-bit version, only extended by to bits. In the Spacepix-2-lin-a ASIC, transistors were resized in the comparator design to increase sensitivity needed for the 10-bit resolution. The new comparator layout improves the comparator symmetry. The asynchronous controller was redesigned with standard cells in used technology.

The Spacepix-2 ADC suffers from missing codes and insensitivity of the detector at the lower energy range. The Spacepix-2-lin-a ASIC should improve these difficulties. However, the 10-bit ADC characteristics were even worse than in the Spacepix-2 version because of the inappropriately designed asynchronous controller. However, several of the ADCs in the Spacepix-2-lin-a ASIC are working correctly. It was possible to measure differential and integral non-linearities and compare the design to other existing column ADCs. The latter version improved the sensitivity of the detector at the lower energy range. Despite difficulties with the 10-bit ADC design, it was possible, with the Spacepix-2 sensor, to measure spectra of Pu-238 and Am-241.

The maximum sampling rate is 4 MSps with power consumption 250 µW from 1.8 V power supply. The layout area occupies 923×120 µm^2.

Another essential part of this thesis was to prepare hardware and software for testing the implemented prototypes. For the 8-bit and the 10-bit versions, two daughterboards were designed (PCBs). The fast readout interface (FURRy) and ASPIRE application were originally intended for XCHIP03 MAPS detectors. To read data out from the Spacepix MAPS detector, it required to modify FURRy firmware and ASPIRE software. The FURRy platform was Verilog firmware for SPARTAN-6 FPGA was modified to read measured data and configure the sensor. ASPIRE windows application was adapted to the size of pixel matrix and global configuration settings.

It was proved by the spectrum measurements that the 8-bit resolution is not sufficient for recognizing impinging particles in the detector. The only way to do a serious experiment in high-energy physics is to use the 10-bit resolution. It is necessary to redesign the asynchronous controller properly and improve ADC characteristics with the minimum missing codes in future work. The latter post-layout simulations imply that increasing the unit capacitance in CDAC significantly reduces the problem of the missing codes. After that, the proposed column ADC design will provide a fast sampling rate of 4 MSps with low power consumption 225 µW and all benefits of the used differential architecture.

Summary of Scientific Contribution of this Thesis

The primary scientific contribution of this thesis is in new proposed column ADC architecture shown in Fig. 2.2 for 8-bit version [A.1], [A.2] and in Fig. 3.1 for 10-bit version [A.6]. A single column-ADC has multiplexed input to two columns. The layout width is doubled, and thus differential SAR ADC layout design is better feasible. The secondary scientific contribution of this thesis is in the improvement of noise immunity, better speed, and accuracy of the proposed column ADC resulting from using differential SAR ADC architecture. A new CDAC layout was proposed [A.3]. A new method for assessment of pre-arranged layout topologies was proposed in cooperation with STMicroelectronics [A.5] and used in the comparator layout design. These scientific contributions improve the SAR column-parallel ADC knowledge in the monolithic active pixel sensors domain.

Completed Aims

All aims of the thesis were fulfilled.

1. **Design fully differential column-parallel SAR ADC (8-bit and 10-bit) for a monolithic pixel detector in 180 nm SoI CMOS technology.**

   The 8-bit column-parallel SAR ADC was implemented in 180 nm SoI CMOS process and published in 2020 [A.1], [A.2]. The 10-bit column-parallel SAR ADC was implemented in 180 nm SoI CMOS process and published in 2021 [A.6]. Both versions use novel double sampling architecture, where the single column ADC samples signals from two columns. In the Spacepix MAPS detector, only 32 ADCs are needed for 64 columns pixel matrix. This new approach doubles the layout width from 60 µm to 120 µm. Therefore, the CDAC layout is more relaxed with good linearity. This unique design also reduces valuable power consumption.

2. **Reach conversion speed at least 2 MSps.**

   Both of ADCs versions can sample with speed 2 MSps. ADC speed is limited by the ADC driver that has to react to signals from odd and even columns. There is needed some time for voltage settling at the differential ADC inputs. Single ADC without the driver samples with speed up to 5 MSps.

3. **Use a low-power asynchronous architecture.**

   Asynchronous architecture is used in both ADC versions. The 8-bit uses transistor SAR logic [1] and the 10-bit uses re-designed SAR logic using standard cells published in 2021 [A.6].

4. **Decrease capacitive DAC capacitance to a minimum.**

   The 8-bit version exploits 4.5 fF unit MoM capacitors with the cage structure in CDAC design. This CDAC design was presented at the TWEPP conference in 2018 [A.3]. The total capacitance of a single CDAC is 1.152 pF.

The 10-bit version exploits 0.5 fF unit MoM capacitors with the cage structure in CDAC design. The total capacitance of a single CDAC is 512 fF.

In cooperation with ST Microelectronics (during master thesis), a method for matched layout structures assessment was developed. This method was published in 2020 [A.5], [A.4] and used for comparator and CDAC designs matched layout design.

5. **Provide a high input impedance.**

   The input buffers are used in both of the presented column ADC versions. These input buffers provides input capacitance 220 fF, [A.1], [A.6].

6. **Convert single-ended signal from a pixel to fully-differential signal at the ADC inputs.**

   For single-ended to fully differential converter at the SAR ADC inputs was implemented two stage fully-differential amplifier. The second stage uses class AB amplifier with small output resistance and high swing. This amplifier provides needed fast settling time and works within whole ADC voltage range.

Future Work

Above mentioned aims of the thesis were all fulfilled, but there is still space for future improvement of the proposed solution. In the next submission planed at the end of 2021 is needed to improve the following:

1. **Solve the problem with missing codes.**

   Based on post-layout simulations performed after the Spacepix-2-lin-a chip, it seems that the missing codes are caused the deficient value (0.5 fF) of the unit capacitor in CDAC. Interestingly, the missing codes cannot be seen in the post-layout simulation until the post-layout optimization at 150 GHz and below is enabled. When the post-layout optimization is enabled, there are visible missing codes in ADC characteristics. It seems that the extraction tool provides better results than in reality are. The solution is to increase the unit capacitance to 1 fF and test the design with enabled post-layout optimization at 150 GHz and below.

2. **Re-design 10-bit SAR logic**

   Inappropriately designed SAR logic (especially DAC control FSM) used in Spacepix-2-lin-a ASIC must be re-designed in the next submission.

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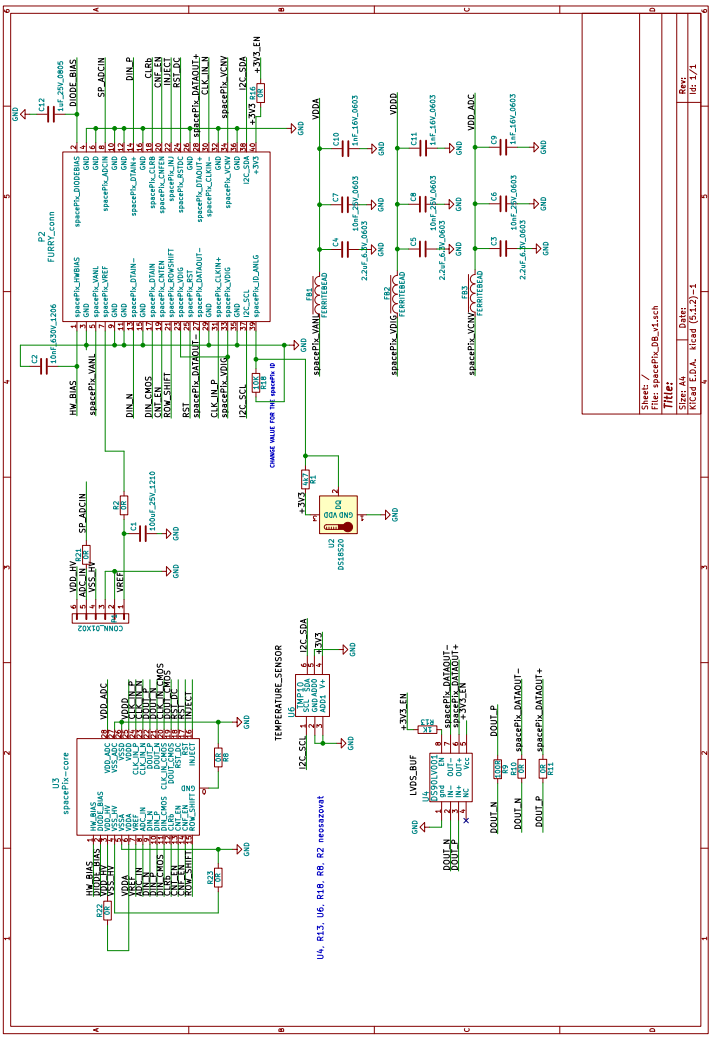
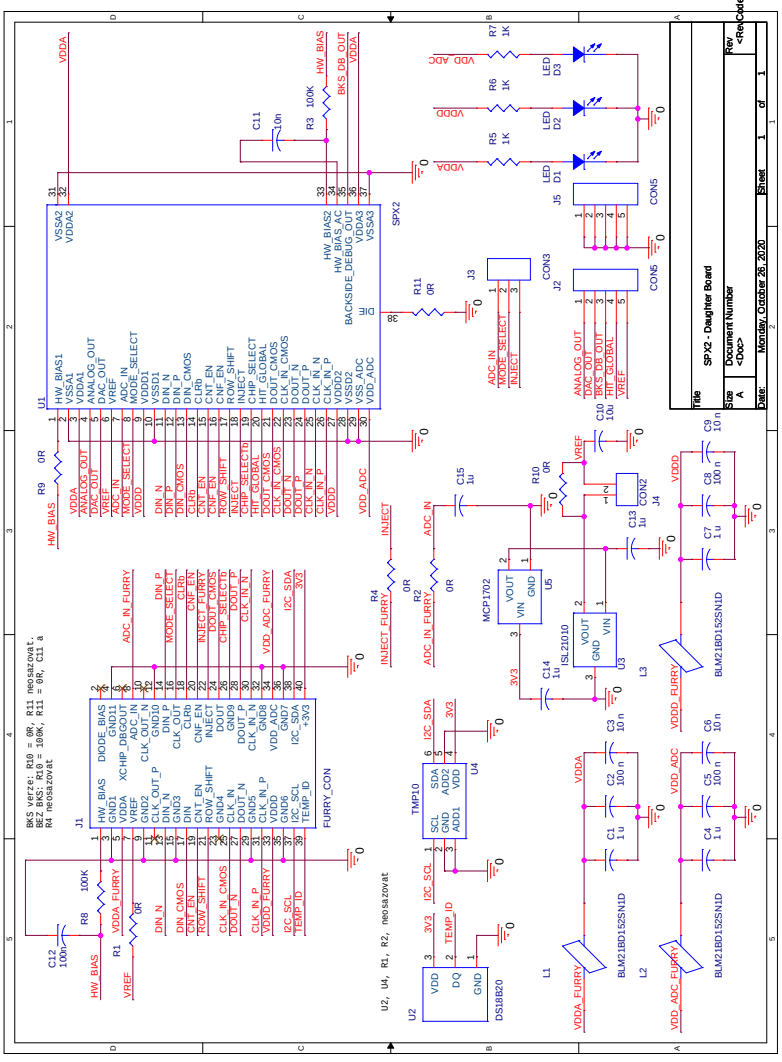
Appendix A

Spacepix-1 Daughterboard PCB



Appendix B

Spacepix-2 Daughterboard PCB



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Improvement of column-parallel sampling for a monolithic pixel detector

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Abstract: Monolithic pixel detectors often use an on-chip analog to digital converter (ADC) with successive approximation register (SAR) to digitize the signal amplitude of the pixels. This paper solves the challenges of column-parallel sampling with respect to the layout, power consumption, process variability, speed, and the integration of fully differential ADC architecture with ADC driver. To save power and area, a single column ADC digitizes the signals from two columns. A fully differential amplifier (ADC driver) is used to convert a single-ended signal from a pixel to the differential signal for driving the fully differential SAR ADC inputs. An implemented prototype occupies $445 \times 115\,\mu m^2$ and achieves 4 MHz sampling frequency. The overall power consumption is 200 µW from a 1.8 V power supply at 10 frames per second readout frequency.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

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Radiation Tolerant 8-bit Analog to Digital Converter with Successive approximation

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Abstract. *This paper brings implementation of 8-bit asynchronous analog to digital converter with successive approximation (SAR ADC) in 180 nm CMOS SoI technology. Radiation tests have proven that used technology is radiation tolerant up to 1 kGy. Layout in the used technology occupies 319 × 115 μm^2. The proposed SAR ADC consumes 295 μW from 1.8 V power supply at 4 MHz sampling frequency. Achieved ENOB is 7.81 bit and calculated figure of merit is 163 fJ/conversion-step.*

Keywords

radiation tolerant, SAR ADC, low power, asynchronous, fully-differential

1. Introduction

Modern electronics for special applications such as space applications, X-ray monolithic detectors, avionics, CERN experiments, etc. needs to be working in a radiation environment. Electronics in integrated circuits can be hardened by design, technology or layout techniques. This paper brings 8-bit SAR ADC in 180 nm SoI technology working in radiation environment up to 1 kGy. This maximum radiation value limits used technology [1]. The proposed design brings innovation of Harpe at al.[2] with improvements for radiation environment. The first improvement is the used SoI CMOS technology which is more radiation tolerant than classic bulk technologies [1]. The second improvement is using layout matched structures in combination with differential design which helps to eliminate single event effects (SEE). The third improvement is own customization of metal-oxide-metal (MoM) capacitor used in capacitor DAC of the SAR ADC. The figure of merit of the proposed design is 163 fJ/conversion step which is competitive value in comparison with existing published results, for example with references [3], [4], [5].

2. 8-bit SAR ADC circuit description

The 8-bit SAR ADC circuit design is described in detail by Harpe et. al [2]. In this section, only brief circuit description is provided and modifications are emphasized. A block diagram is shown in Fig. 1.

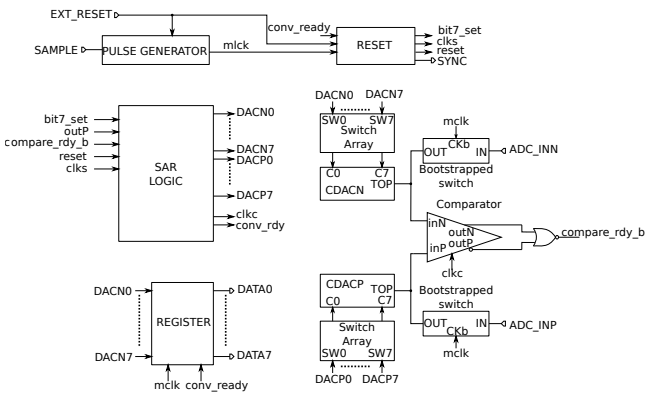

Fig. 1: 8-bit SAR ADC block diagram

The proposed design contains in comparison with [2] a pulse generator circuit which generates sampling pulse with adjustable length at rising edge of the SAMPLE signal. A bootstrapped switches [6] are used instead of transfer gates to improve the linearity of sampling signal into top plates of capacitor arrays. The output register latches data when conversion is finished. Data are latched until the next SAMPLE signal is received. Both of capacitor DAC's uses customized MoM capacitor shown in Fig. 2. Each of unit capacitor has dimensions 4.24x4.24 μm^2 with capacitance 4.5 fF. The proposed unit capacitor acts as a shielding box which improved linearity. A common centroid layout in the comparator is used. The common centroid layout in combination with fully differential ADC design mitigates SEE [7].

3. Results

Differential and integral non-linearities (DNL, INL) of the SAR ADC from simulations are shown in Fig. 3 and Fig. 4. These nonlinearities have been extracted from transfer

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A Capacitor DAC for Charge Redistribution Analog to Digital Converter with Successive Approximation

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The recent analog to digital converters, with the successive approximation (SAR ADC), are widely used for their high speed, low power operation and accuracy. SAR ADC demands precise internal digital to analog converter (DAC). To save power, the DAC is mainly implemented using capacitors (CDAC). Its precision depends mostly on layout implementation which must minimize the various parasitic effects. This paper presents two new layout design approaches of CDAC for SAR ADC used in a pixel detector implemented in 180 nm SOI technology. The various types, topology, size of the capacitors, power consumption, layout area, speed, and any nonlinearities are discussed. First is a new layout design of the 10-bit split capacitor DAC with Metal-Insulator-Metal capacitors, and, the second, is a 8-bit binary-weighted DAC with Metal-Oxide-Metal capacitors. The new layout of the metal-oxide-metal capacitor topology provides better accuracy of the DAC. The layout styles for each of CDAC, with low parasitic capacitances, are shown. The post layout simulations confirm that both capacitor arrays have an integral, differential nonlinearity, less than one least significant bit without a calibration scheme.

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Spatial systematic mismatch assessment of pre-arranged layout topologies

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ABSTRACT

A spatial systematic mismatch, occurring in the integrated circuit manufacturing process, leads to differences in parameters for two or more identical devices. It is widely accepted that placing devices into symmetrical patterns reduces the spatial systematic mismatch between their parameters. In this paper, a novel method based on linear and nonlinear parameter gradient modeling for the assessment of pre-arranged matched structures has been proposed. The direction of a parameter gradient against a layout topology on a wafer is unknown. The pre-arranged layout pattern is rotated against the modeled parameter gradient. In each step of the rotation, for example, with a 1-degree resolution, the mismatch between parameters is calculated. The peak mismatch value is then used for the comparison of the different pre-arranged patterns. The proposed method is independent of technology.

1. Introduction

Continuous improvement in Complementary Metal Oxide Semiconductor (CMOS) technology implies higher requirements for both analog and digital integrated circuits. For example, faster and more accurate Analog to Digital Converters (ADC), precise voltage references, current mirrors, comparators, amplifiers and other analog circuits require more sophisticated design and layout approaches. The mismatch between parameters of identical devices causes e.g. an offset in a differential pair, errors in current mirroring, or integral and differential non-linearity in Digital to Analog Converters (DAC) arrays [1]. These non-idealities directly affect the performance of an analog circuit [2].

The mismatch between parameters of identical devices is divided into the random and the systematic part. While the random part of mismatch can be improved by increasing the size of a device according to Pelgrom's model [3], the systematic part of mismatch can be improved by a proper layout technique [4]. A well-known technique for elimination of the systematic spatial mismatch is, for example, a common centroid pattern [5]. In a simple common centroid layout, matched devices are split and placed symmetrically in order to cancel out the linear order gradient. These small patterns are known and can be immediately used. However, a pattern may also contain nonlinear parameter gradients. The problem is to assess and design patterns with the minimum spatial systematic mismatch. Other problems are to take into account nonlinear order of the gradient with unknown direction of the spatial systematic mismatch.

Several models dedicated to mismatch modeling have recently been published. One of the first attempts to model mismatch is the Lakshmikumar model [6]. A statistical model has been published in [7]. However, generally known is Pelgrom's model [3] describing random and systematic parts of the mismatch of two identically designed devices using spectral analysis. Lan et al. [8], used a spatial systematic mismatch modeling method with continuous gradient rotation for classification of the current mirror and of the differential pair patterns respecting the linear order gradient. Another technique for modeling of systematic mismatch was presented in [9]. The advantage of this method is a parameter gradient modeling with a two-dimensional function, which can be easily extended from linear order to higher-order gradient. Xin Dai et al. focused their work [9] on the elimination of *n*th order gradients for symmetrical layout patterns.

The proposed method uses the parameter gradient model published by Dai et al. [9]. The orientation of the layout pattern always has a fixed reference, but the parameter gradient direction is unknown. Therefore, in the proposed method, the assessed pre-arranged layout patterns have to be rotated upon the same parameter gradient model. The step of 1 degree of the rotation provides enough resolution. In each step the mismatch between parameters is calculated. Each pre-arranged

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A Low Power Asynchronous Column-parallel 10-bit Analog to Digital Converter with a High Input Impedance

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Abstract: This paper proposes a low power 10-bit asynchronous fully-differential column analog to digital converter (ADC) with successive approximation (SAR) and charge redistribution in a 180 nm SoI technology. The ADC is designed for use in Spacepix-2 monolithic active pixel sensor. A novel folded architecture of internal capacitive digital to analog converter (CDAC) is proposed. The total capacitance of CDAC is 512 fF, with a single unit capacitor capacitance only 0.5 fF and a size of 2.5×1.4 μm^2. The total input capacitance of the proposed column ADC is only 220 fF. Two columns of a pixel matrix share a single ADC to double layout width. The layout area is 120×923 μm^2. The sample rate is 4 MSps with power consumption of 225 μW from 1.8 V power supply.

Keywords: SAR, ADC, pixel, MAPS, detector, asynchronous, design

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