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Doctoral Thesis

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Frequency response analysis in high voltage machines diagnostics

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Declaration

I declare that I worked out the presented work independently and I quoted all used sources of information in accord with Methodical instructions about ethical principles for writing academic thesis.

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Abstrakt

Táto dizertačná práca sa zaoberá návrhom prístrojovej platformy pre nedeštruktívne testovanie vysokonapäťových napájacích transformátorov alebo testovanie točivých strojov pomocou metódy analýzy frekvenčnej odozvy (FRA). Hlavným cieľom je vyvinúť a navrhnúť kompletný prístrojový systém, ktorý zlepší parametre stávajúcich systémov a poskytne operátorovi vyššiu mieru pohodlia a ergonómie pri používaní takéhoto systému. Navrhnuté prístrojové vybavenie bolo vytvorené vrámci širšej výskumnej snahy. Meracia platforma sa skladá z niektorých častí, ktoré boli vyvinuté v spolupráci s ostatnými členmi tímu. Táto práca sa zaoberá predovšetkým plne digitálnym jadrom FPGA pre účely vysokonapäťovej diagnostiky spolu s finálnym overením a validáciou pre samotnú metódu FRA. Práca sa týka aj vývoja akupacku, ako aj ďalších častí.

Vybavenie elektrární ako aj zariadenia celej napájacej sústavy vyžadujú moderné diagnostické metódy testovania s možnosťou predikcie závad pre lepší manažment ich životného cyklu a pre včasnú detekciu neočakávaných závad. V práci je možné nájsť popis a pripomenutie spoločných a základných princípov napájacích transformátorov spolu s priblížením typických konštrukcií týchto zariadení. Na týchto teoretických základoch pracujú takmer všetky používané diagnostické metódy.

FRA algoritmus je zástupcom tzv. skupiny elektrických metód diagnostiky, ktoré sú používané k monitoringu transformátorov. V nadväzujúcich častiach dizertačnej práce sa nachádza popis najznámejšie používaných elektrických metód, pričom pri každej z týchto metódy je možné nájsť jej základný blokový popis spolu s typickou aplikáciou danej metódy. Metóda FRA, jej teoretický základ a aktuálny stav techniky je ďalej detailne uvedený v práci. Popis aktuálne používaných prístrojov spolu s identifikáciou ich parametrov je možné nájsť v závere úvodnej časti. Ďalšie sekcia tejto práce pozostávajú z koncepčného návrhu prístrojového vybavenia, ktorý obsahuje identifikovanie požiadaviek a výber kľúčových súčiastok a ďalších komponentov. Kompletný dizajn a návrh hardvéru od schematických podkladov cez plošné spoje až po testovanie a prípravu firmvérových a softvérových blokov je možné nájsť v praktickej časti tejto dizertačnej práce. Túto časť práce je možné považovať za najdôležitejšiu, nakoľko celkový výsledok návrhu prístroja je závislý najmä na precíznej návrhrajskej práci. Všetky tieto kapitoly obsahujú veľmi špecifickú a detailnú informáciu o vedeckých a návrhársky postupoch, ktoré stoja za úspešným návrhom kompletného prístrojového vybavenia. Softvérová časť práce obsahuje rozbor a implementáciu číslicového spracovania signálu pre potreby diagnostických metód. Kapitoly obsahujú popis vlastnej práce v rámci VHDL jazyka ako aj dizajn system-on-the-chip systému (SoC) mikroprocesora spolu s jeho ovládacím programovým vybavením. V rámci VHDL jadra sa systém opiera hlavne o lock-in-amplifier (LIA) blok. Okrem samotného systému pre spracovanie signálu je ďalej popísaná príprava laboratórneho testovania spolu s vyhodnotením presnosti a výkonu navrhovaného riešenia. Prepojenie systému s nadradeným systémom a komunikačný protokol sa nachádza v závere kapitoly, ktorá sa venuje softvérovému vybaveniu.

Navrhnutá a vyvinutá prístrojová platforma bola testovaná v reálnych podmienkach a výstupy tohto testovania je možné nájsť v závere práce spolu s ich zhodnotením. Vďaka tomuto výskumu a vývoju tejto novej prístrojovej platformy pre metódu FRA ponúka tento systém širší pracovný rozsah frekvencií spolu s presnými výsledkami a použitím moderných komunikačných rozhraní. Ďalším benefitom tohto prístrojového vybavenia je mobilná prevádzka takéhoto systému.

Kľúčové slová: Analýza frekvenčnej odozvy, nedeštruktívna diagnostika, FPGA, lock-in-zosiľňovač.

Abstract

This doctoral thesis deals with designing an instrumentation platform for frequency response analysis (FRA) testing for non-invasive diagnostic purposes such as high-voltage power transformer testing or rotary machines inspections. The main objective of this work is to develop the complete instrumentation, which will operate with better parameters and provide a higher level of operator convenience together with robustness and ergonomy. This thesis is part of the larger research group effort. The proposed instrumentation consists of some parts, which were designed in collaboration with other team members. This work deals mainly with the fully digital FPGA core for high-voltage diagnostics purposes together with final verification and validation for the FRA method by itself. Work also covers the accupack developments as well as other parts.

Power-plant devices and the whole power infrastructure require modern diagnostic and predictive methods of testing and monitoring for better life-cycle maintenance management and to prevent unexpected failures. The common principles of the power transformer theory and power transformer construction are described at the beginning of this thesis to remind the basics, which directly influence almost all diagnostic methods.

The FRA testing is the member of the electrical methods, which could be used for the monitoring. In the following parts of the work, there is a description of each of the major electrical methods. Each method's principle is shown together with the typical applications. The frequency-response-analysis and its state-of-art types and facts are summed up in the following chapters with the contemporary instruments available on the market. The following chapters consist of the conceptional design of the future instrumentation platform, including the specific hardware requirements definition and selection of the correct parts and hardware components. The complete hardware design from the schematics via printed circuit board design up to the testing and firmware and software preparation could be found in the practical part of the work. This part is the most important of this work because the complete instrumentation depends on the precise designer's work. This stage includes the design of the field-programmable-gate-array (FPGA) board, the accumulator board, and the excitation (interconnect) analog board. All these chapters include very specific and detailed information of the scientific and designer's work which is behind the whole instrumentation. There is a software and signal-processing oriented part after the hardware design. This stage consists of the digital domain signal processing core description. The VHDL code blocks together with the soft-core system-on-the-chip (SoC) microprocessor runtime codes are presented. The signal processing part relies mainly on the lock-in-amplifier (LIA) core. Its specific VHDL design can be found here. Moreover, the complete laboratory performance testing is presented as well. Interconnection in-between the computer and other diagnostic devices could be found in the control software and communication protocol description part.

The designed and developed instrumentation platform was tested in the real environment, and the outputs of these tests could be found in the closing parts of this work. Thanks to this complete research and development of the FRA method instrumentation, this system could offer a wider frequency range together with more precise results and a modern communication interface. The remote power-independent operation is another benefit of this design and the result of this doctoral thesis research.

Keywords: Frequency response analysis, non-invasive diagnostics, FPGA, lock-in-amplifier.

Contents

Abbreviations

FRA	Frequency response analysis
SFRA	Swept frequency response analysis
PD	Partial discharge
HV	High voltage
WND	Weighted nominal difference
OWA	Objective winding asymmetry
FFT	Fast Fourier transform
DSP	Dielectric spectroscopy
DUT	Device under test
FPGA	Field programmable gate array
FBGA	Fine ball grid array
SoC	System on the chip
DSP	Digital signal processing
SAR	Successive approximation
HSMC	High speed mezzanine connector
ALM	Adaptive logic module
TCP	Transfer control protocol
SPI	Serial peripheral interface
MAC	Medium access control
DDR	Double data rate
QDR	Quad data rate
LVDS	Low voltage differential signalling
LVTTL	Low voltage TTL
JTAG	Joint test action group
PLL	Phase locked loop
PCB	Printed circuit board
GPIO	General purpose input/output

1 Introduction

Increasing reliability and keeping the economic aspect at low levels is one of the upcoming trends in high voltage power machinery maintenance. Investments into the diagnostic processes could be returned rapidly, especially when these steps avoid cost-ineffective repairs. Periodical inspection and the correct data representation is the fundamental approach to increasing the life cycle of the high voltage machinery. Electricity infrastructure relies mainly on the failure-free service of the high-power transformers. Thus the correct maintenance timing and inspection with several well-known methods are necessary. Any failure or unexpected system shutdown is very costly.

Nowadays, there are several diagnostic methods widely used. They can be divided into two groups: invasive methods and the second is more effective, non-invasive. Invasive methods have significant limitations, and they can not be used for online or periodic testing on-site. On the other hand, the non-invasive methods could be used directly in a particular place without uncomfortable moving. The main advantage is that non-invasive testing could be done several times in the regular cycles at the same device under test. These steps allow comparing all the tests from the past months or years. Diagnostics could be further divided into the electrical-based and non-electrical, where no additional testing voltage is connected and the devices are inspected differently. Acoustic and mechanical testing could be performed in addition to classical electrical testing to achieve better accurate results. Defects in the insulation could cause excessive heating, material changes, and other impacts. For instance, the existence of partial discharges inside the windings causes ionization of surrounding air. These methods are classified only as additional because of their lower repeatability and accuracy. Electrical testing nowadays relies on several methods, which have been classified by tests and long-term data analysis as proper for maintenance. Widely used methods are:

- partial discharge measurement, localization - PD
- capacitance and dissipation factor measurement - $tg\delta$
- frequency response analysis - FRA
- dielectric spectroscopy - DSP

Mentioned methods are performed by specialized instruments, which could be done fully analog or fully digital in more modern devices. From the complexity point of view, they can be designed as an online measuring system or as a standalone diagnostic system for periodical maintenance visits. It is common to build a poly-phase diagnostic instrument to produce complete data set of measured values at one time. This is very common for the PD measurement, specialized algorithms for processing data underlying all these methods. Except for real-time data visualization and representation, more problematic is the long-term data comparison and estimation. In other words, some momentary critical value could not cause any failure, but trends in whole datasets could predicate defects more accurately. To illustrate, some of the devices under test (DUTs) have a lifetime of more than tens of years. To support this estimation, all measurements have to be done strictly in the same way in regular intervals with systematic data management for long time usage.

1.1 Transformer and transformer construction theory

This chapter is the key theoretical background for the further description and implementation of diagnostic methods like frequency response analysis. This chapter will try to describe the types of transformers used and also describe the construction details, which directly implies the results of the high voltage diagnostics applied to the particular device under test (DUT) units. First of all, the very basic theory behind the transformer device must take place.

1.1.1 Ideal transformer - principles

To describe the principles, the features of the ideal transformer should be mentioned in the first place. An ideal transformer is only a theoretical model. The real transformers are only trying to match the ideal parameters of the model. The model connection is shown in Fig. 1. This shows the ideal transformer connected with source V_P on the primary winding and load impedance Z_L on the secondary. This impedance match the following criteria $0 < Z_L < \infty$, according to the [1]. The ideal transformer model and

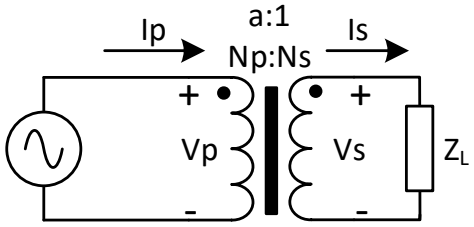


Fig. 1 Ideal transformer

its principles are based on the Faraday's law of induction [1], see Eq. 1 and Eg. 2.

$$V_S = -N_S \frac{d\Phi}{dt} \tag{1}$$

$$V_P = -N_P \frac{d\Phi}{dt} \tag{2}$$

where V is the instantaneous voltage, N is the number of turns in the winding and $\frac{d\Phi}{dt}$ is the derivative of the magnetic flux Φ through one turn of the winding over time t. The p and s determines the primary and secondary part of the transformer. Easily connecting these two equations, the equation for the ratio is as follows (Eq. 3).

$$\frac{V_P}{V_S} = \frac{N_P}{N_S} = a \tag{3}$$

In other words, the varying current in the transformer's primary windings creates a varying magnetic flux in the transformer core. This magnetic field induces the output voltage in the secondary winding. The current direction shown in Fig. 1 is applicable when the input winding is fed from the voltage source, and the output is loaded with generic impedance Z_L. By the law of energy conservation, the power at each side of the transformer is conserved as follows in Eq. 4.

$$S = I_P V_P = I_S V_S \tag{4}$$

To describe the inductance of the windings, the Eq. 3 and 4 could be connected to get Eq. 5. This identity is applicable because the ideal transformer's winding inductances are each infinitely high, the square root of winding inductances ratio is equal to the turns ratio (according to the [2]).

$$\frac{V_P}{V_S} = \frac{N_P}{N_S} = \frac{I_S}{I_P} = \sqrt{\frac{L_p}{L_S}} = a \tag{5}$$

The key features of the ideal transformer are full **linearity**, **lossless** and **perfectly coupled**.

1.1.2 Real transformer

The real transformer has few deviations from the ideal type, mentioned earlier. To sum up the main deviations:

- **Core losses, magnetizing current losses**

  There are two basic types [3]. The first one is the hysteresis loss, which is the result of the magnetization process inside the core material due to the defects inside the crystal structure. The second group of losses is the eddy-current losses, especially when the core is electrically conductive. The alternating magnetic field also induces a current inside the core. Then the energy is dissipated in the form of heat because of the resistance of the core material. This phenomenon could be eliminated with the usage of the core, which has large electrical resistance, for instance.

- **Windings resistance and inductance**
  Simple said, the resistance of the primary and secondary winding produces another heat dissipation due to the current, which flows through the wires. Moreover the leakage flux that escapes the core, will affect the primary and secondary winding in form of reactive impedance. The leakage flux is shown in. Fig. 2. The main

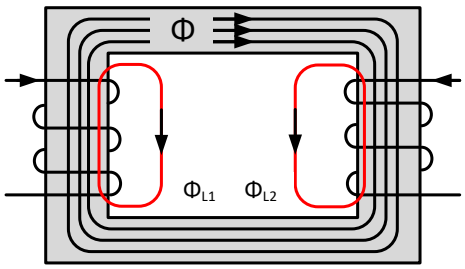


Fig. 2 Flux leakage

  flux is shown as Φ, while the flux, which escapes are Φ_{L1} and Φ_{L2}.

- **Parasitic capacitance**
  The most important part of the real transformer features are parasitic capacitances, which are developed in three parts of the transformer construction
  - capacitance between adjacent turns in any layer of the winding
  - capacitance between adjacent layers
  - capacitance between the core and layer adjacent

1.1.3 Equivalent circuit

Based on the previous facts of the real and ideal transformer model, the equivalent circuit of the transformer could be built up [4]. The basic equivalent circuit is shown in Fig. 3. The primary winding resistance is shown as R_P, while its reactance is denoted as

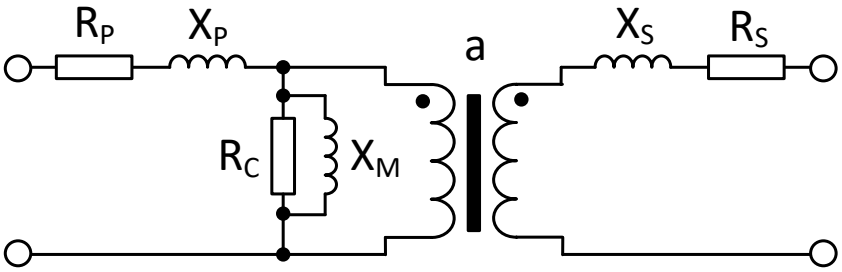


Fig. 3 Equivalent circuit of transformer [4]

X_P. The very same parameters R_S and X_S are present also at the secondary side of the transformer. Losses in core is schematically implemented as R_C and the magnetizing reactance as X_M. In the middle of the circuit is the ideal transformer with ratio a.

1.1.4 Constructions

There are several types of windings and core types. In case of closed-core transformers, there are two construction concepts the "core form" and the "shell form". When the winding is inside the cores the type is shell type, while if the winding is accessible from outside and it surrounds the core, the type is core form. For better understanding the core constructions are shown in. Fig.4 On the left side, there are single-phase

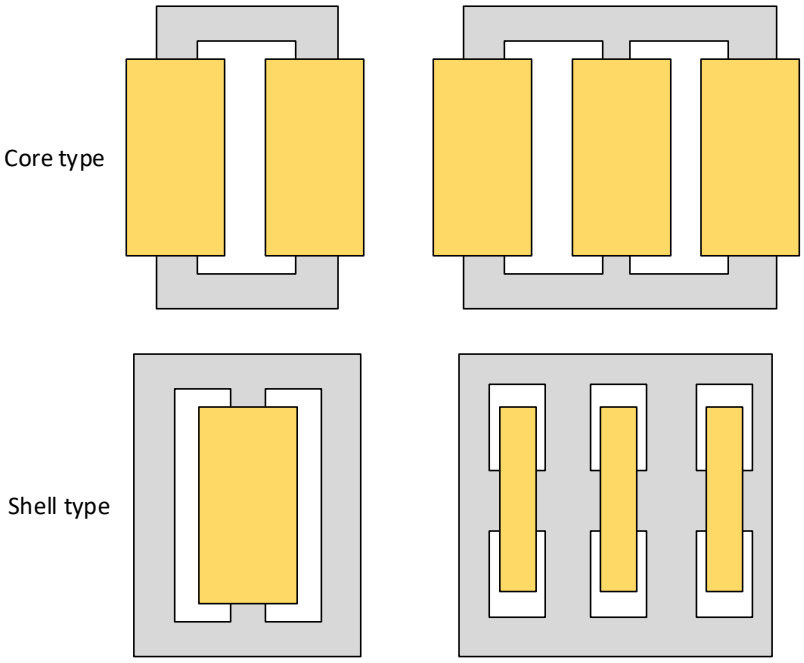


Fig. 4 Core and shell form types [5]

transformers, while on the right side, there are three-phase transformers. The core

form type is typically cheaper construction, and typically the usage is in low rating power transformers [5]. The shell-type core construction is better for easier winding stacking. Also, the higher voltage and power rating applications rely on the shell-type transformers. The transformers, by their core construction, could be then grouped as follows:

- laminated steel cores
- solid cores
- toroidal cores
- air cores

The laminated steel concept is widely used in power transformers (which are the main suspect of the HV diagnostics). This core uses high permeability silicon steel [6]. This material has larger permeability than free space, so the magnetizing current in the core becomes reduced. The lamination process was necessary for the eddy-current losses elimination. The core is not typically manufactured from the single iron plate because the intersection of the core will be too large. The area which is closely related to the eddy-currents is eliminated as shown in Fig. 5. The laminated core structure is shown

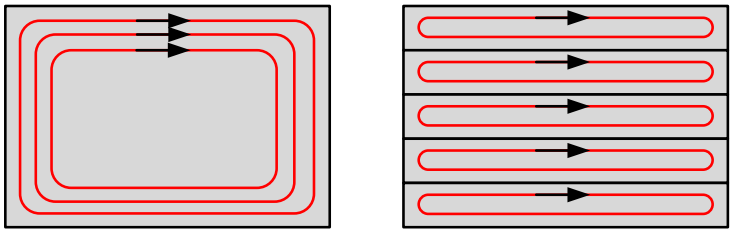


Fig. 5 Steel core lamination and eddy current losses

on the right side. The separate iron plates are laminated together with coating layers. The other groups are solid cores which are mainly used in switching-mode supplies in the higher frequency range. The next large group of transformer core types is toroidal cores. The toroidal core is a ring-shaped object. The construction is also eliminating the air gap of the classical E-I construction. Another aspect is the relatively more complicated manufacturing process of the winding because this winding must be passed through the ring with every one wire turn. The main disadvantage of these cores is their limited power capacity. Because of this, the main appliances are low powerpoints of load voltage conversion [5]. The last group of cores is the "no-core" concept. The core is formed by the surrounding air next to the primary and secondary winding. Transformers based on this type of cores are typically used in the high-frequency band (radio-frequencies). The magnetizing inductance is smaller because of the non-magnetic core, which is an issue for higher power transfer. Enlargement of the primary and secondary winding turn count could solve the issue, but the final resistance of the winding will rise too.

1.2 Power transformer construction

This section is most important for the further proposed high-voltage diagnostic frequency response analysis testing. The power transformers are the main suspect of the tests so the construction of the winding together with its simulation model should be discussed. The very good start for this theory could be found in [10]. For proper understanding the construction and its circuit simulation the winding structure of the typical high-voltage transformer must be included at first. The typical picture of the

Fig. 6 Distribution transformer example 33 kV 100 kVA (electricmall.com)

power distribution transformer is shown in Fig. 6. The shown transformer has rating of 100 kVA. For the next text, the typical power transformer will be described as a

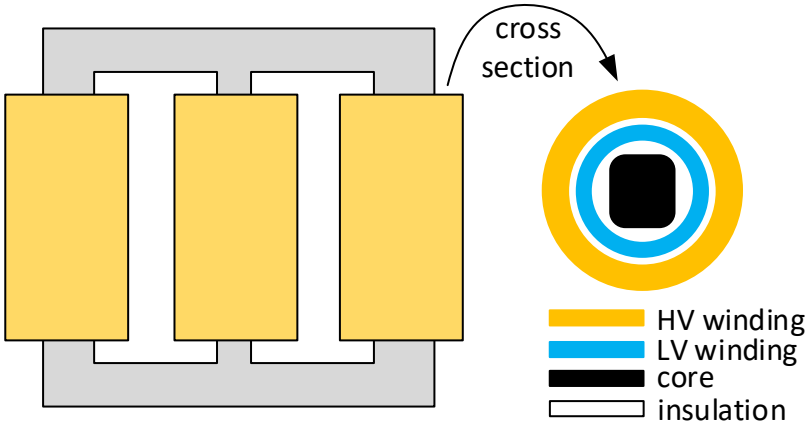


Fig. 7 Winding structure of the power transformer

three-phase transformer. Inside the power transformer, there is typically a core type concept construction (mentioned in 1.1.4). Inside the case of the transformer, the main part is the core together with the winding structure. To better understand the construction of the winding structure, the typical physical structure is shown in Fig. 7. Each of the phases is shown in cross-section with the core material in the middle. The insulation material is in-between the core material and both windings. The low-voltage winding is typically underneath the high-voltage winding. The real placement of the windings inside the high-voltage transformers could vary from the transformer to the transformer. Typically, the transformer windings are divided into **discs**. For better

understanding the Fig. 8 The winding discs could be in the way that the low voltage

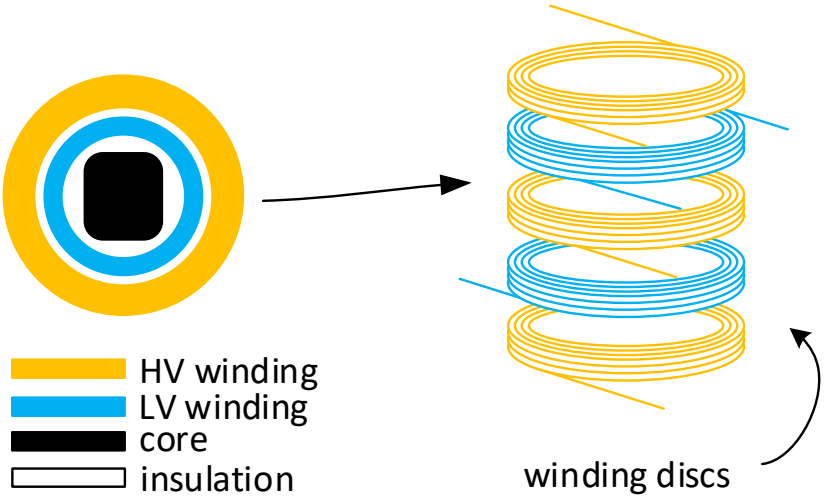


Fig. 8 Winding discs

winding is hidden under the high voltage winding or interleaved (as shown in the figure). The low voltage winding and high voltage winding are put on the core one by another. The important fact is that the winding could be divided into some parts, and it is not manufactured somehow in one piece. The failures which could affect the transformer are typically connected with the winding discs according to the [10]. The [10] tries to show the schematic representation of the disc type power transformer.

The Fig. 9 shows the model equivalent of the disc transformer. The yellow background shows the high voltage winding part, while the blue part shows the low voltage winding. As the construction consists of discs, these parts are graphically shown as three rows on the figure (separated by the grey lines named disk boundaries). To better understand the all schematic parts could be described according to the real construction. The high voltage winding parts are symmetrically placed as the low voltage winding parts, so only one side of the transformer is described more in detail. Naturally, each disk consists of the inductance L_S together with parasitic series resistance R_S. This combination is in each disk on both sides. This part is shorted with the C_{SH} and dielectric conductance G_{SH}. The connection between the two windings should be isolated in the case of a real transformer, but the real power transformer (as all kinds of transformers) has the capacitance binding C_{HL} between windings together with the dielectric conductance G_{HL}. The next parasitic feature is the coupling between the chassis of the transformer via the dielectric material (typically oil). This is simulated with the conductance G and the capacitance C_G. For complete design also the mutual inductance between the inductors should be stated as well. The M is the inductance between primary and secondary winding, while the M_H (M_L) are mutual inductances between the discs.

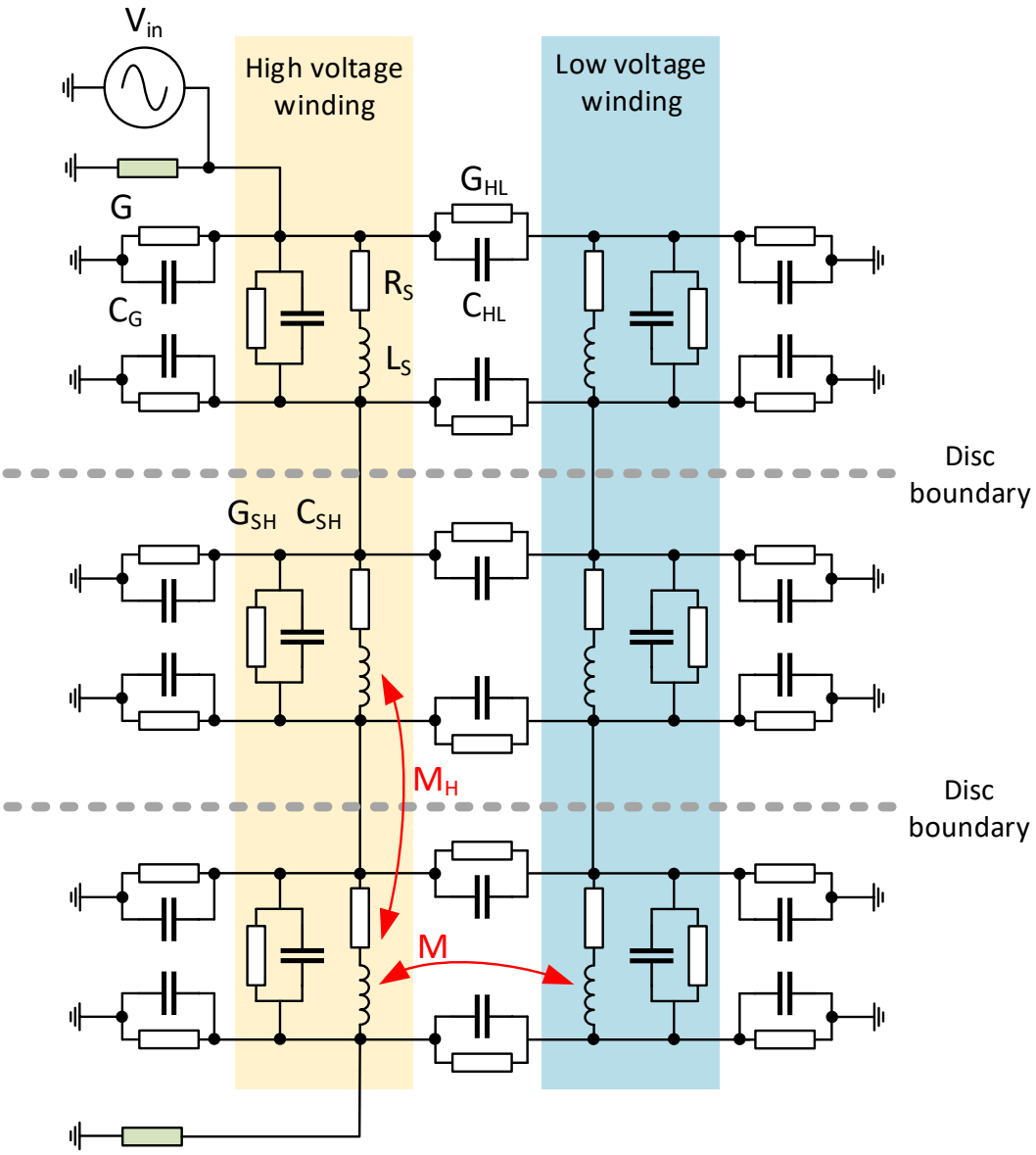


Fig. 9 Equivalent schematic model of power transformer [10]

2 State of the Art

2.1 Electrical methods

The following text provides brief information about mostly used electrical diagnostic methods. Basic connection, advantages, and disadvantages are mentioned together with the data analysis.

2.1.1 Partial discharge measurement

Partial discharge as a result of insulation defects in the high voltage machinery has been described in detail in [11]. This paper was published early in the 1940s. More complex information of the application of this method in the field of the transformer measurement has been described in [12].

The method is done typically at the disconnected device under test (hereinafter as DUT), except for online monitors. The DUT is excited with nominal testing voltage in the range of several thousands of volts (typical levels 6 kV, 12 kV). The frequency of the nominal voltage is the same as the mains frequency at the particular location.

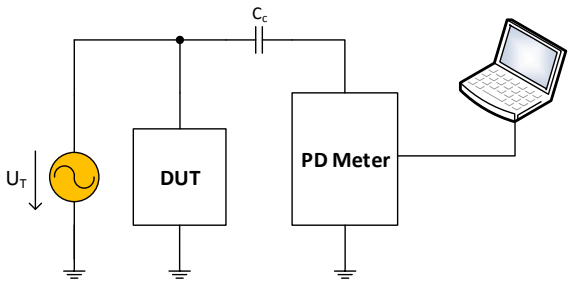


Fig. 10 Basic connection of PD measurement

PD Meter is connected via a coupling capacitance to the DUT like in Fig. 10. Then the signal is filtered and pre-processed via internal circuits inside the instrument. Proper data is typically digitalized via the analog-to-digital converter or measured via an operational amplifier network. The most important measured value is an apparent charge Q which has to be under some criteria to fulfill the insulation parameters. More detailed information on this procedure could be found in the Czech standard [13] or its European equivalent.

2.1.2 Capacitance and dissipation factor measurement

The second parameter which can be studied to obtain more information about the insulation state is capacitance and dissipation factor. Insulation between two windings or between winding and neutral terminal is examined. Standard laboratory equipment like the RLC meter can not be used for this purpose. All inspections should be done at the nominal operation voltage, which could be again in the range of thousand volts

(typical levels 6 kV, 12 kV), which is a limitation for classic instruments. Some of the widely used methods for a low voltage measurement are mentioned in [14]. On the other hand, the I-V from [14] method could be modified to achieve the high-voltage operation required for the DUT examination.

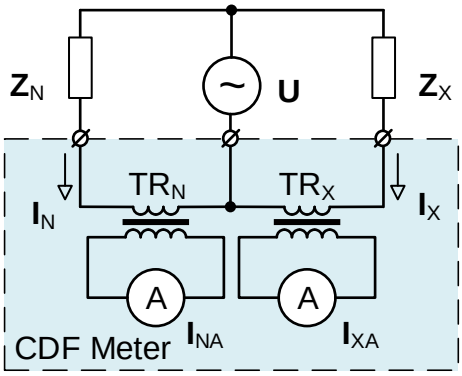


Fig. 11 Modified I-V method for HV measurement [15]

One of the possible connections is described in [15]. Comparison method is shown in Fig. 11. The unknown impedance Z_x is compared to the known impedance Z_n, which is typically inside the instrument. Both impedances are excited with nominal testing voltage, and conversion to the low voltage signal for the data processes is done by current transformers. The particular and momentary values are not as much testifying as to their long-term trends, especially for lifetime prediction. Data comparison and representation have the same importance as the actual measurement.

2.1.3 Dielectric spectroscopy

Extension of the dissipation factor measurement in a frequency domain is the main idea under the dielectric spectroscopy method. The measuring circuit could be based similarly as in Fig. 11. The excitation voltage source is capable of a frequency sweep. In other words, determination of the $tg\delta$ from a few millihertz up to units of kilohertz will form a unique fingerprint, which could be used for diagnostic purposes.

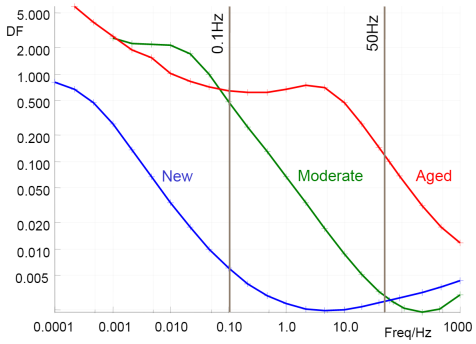


Fig. 12 Changes in dielectric spectroscopy results [16]

The [16] shows the comparison between DSP measurements at various aging levels of the high voltage machinery. Fig. 12 illustrates the change in the dielectric spectroscopy during the aging of the high voltage transformer.

2.2 Frequency response analysis

FRA method will be discussed more in the following text. Motivation for FRA measurements is very similar to the methods mentioned above. Many dielectric and mechanical failures in the large power transformers are preceded by mechanical changes in the winding structure. These changes, or displacements in the winding structure, may be the result of transportation damage occurring between the manufacturer and the service location, short circuit forces imposed on the windings resulting from a low impedance fault occurring close to the transformer, or natural effects of aging on the insulating structures used to support the windings. Detection of these displacements in advance of a dielectric failure can reduce unplanned maintenance costs and provide the possibility to improve system reliability by preventing outages. Additionally, when damage is discovered, repairs may be targeted to a specific phase winding.

2.2.1 Theory

The main idea behind the FRA process is to measure the transfer function of the inspected subsystem in some frequency span. IEEE Standard Dictionary defines the transfer function as "a complex frequency response function that defines the dynamic characteristics of a constant parameter linear system. For an ideal system, the transfer function is the ratio of the Fourier transform of the output to that of a given input." Inputs and outputs of the particular transfer function could be freely chosen to obtain various data.

Diagnostic result for the high voltage machinery diagnostic FRA is typically a relation between AC impedance of the DUT as a function of the excitation voltage (current) frequency. The typical frequency range according to [17] is:

$$10\,Hz < f < 5\,MHz \tag{6}$$

It has been verified that even minor displacements in the geometric structure of the large power transformer windings or changes in the dielectric parameters of the insulation system will lead to the relevant changes in the FRA fingerprint. This fact supports results from simulations in [17] and [18].

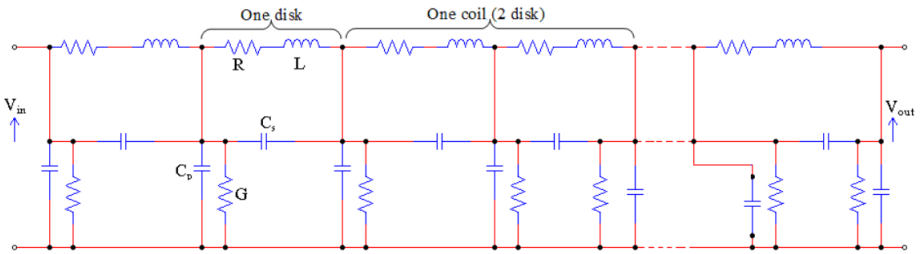


Fig. 13 Transformer circuit equivalent circuit [18]

To understand even better the relationship between transfer function estimation and physical transformer changes, the [18] provides a simplified equivalent schematic of the transformer in Fig. 13 with an explanation of what value is changed by what defect. A useful overview of these changes is documented in [19]. Some examples are in the Tab. 1.

Physical parameter	Type of fault
Inductance	Disk deformation, local breakdown, winding short circuits
Shunt capacitance	Disc movements, buckling due to large mechanical forces, moisture ingress, loss of clamping pressure
Series capacitance	Ageing of insulation
Resistance	Shorted or broken disk, partial discharge

Tab. 1 Transformer electrical parameter and fault type relationship.

2.2.2 FRA methods

There have been two basic methods used in the past to measure the low voltage frequency response on the power transformers. Each method has its advantages and disadvantages.

Swept Frequency Method

The first method, known as the swept frequency method, makes use of the simple truth that the sinusoidal AC impedance (or admittance) of a transformer winding varies with frequency. The basic connection is shown in Fig. 14.

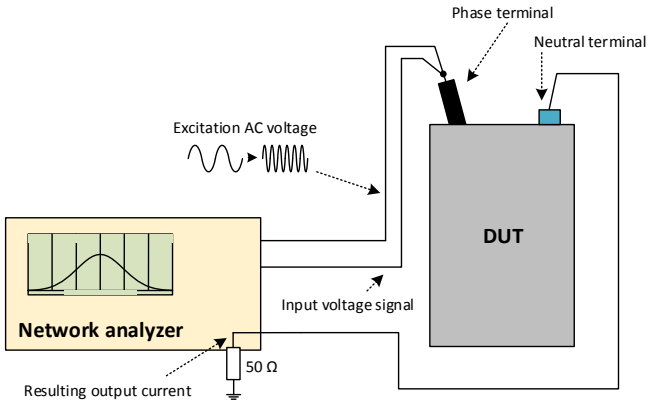


Fig. 14 Typical test connection for a low voltage swept frequency FRA measurement

The FRA analyzer could be substituted as a network analyzer for simplicity. DUT is excited with AC voltage with amplitude in the range of tens of volts, acc. to [17]. There is another voltage probe to measure the real voltage present on the phase terminal. This connection eliminates any mistakes caused by testing voltage cable wiring. The current flown from the neutral terminal of the DUT is the output measured value. The input impedance of the network analyzer could be used to convert the resulting current from the neutral terminal to the voltage as shown in Fig. 14. Despite the simple data analysis, there are several disadvantages of this method. At very low frequencies (in the range of some hundreds of Hz to low kHz), these instruments tend to lack sufficient power to appreciably excite the large power transformer due to the heavy inductive load presented by the steel core. This problem is described more deeply in [17]. The fixed sensing impedance of 50 Ω is insufficient to properly convert small current signals,

especially at high excitation frequencies. Generally, the advantages and disadvantages could be summed up:

- Advantages
  - Simple hardware connection
  - Possible to use basic instruments like network analyser
  - Easy data analysis processes
- Disadvantages
  - Excitation power sufficient for whole frequency range
  - Sensing impedance selection
  - Cable length and connection
  - Repeatability problem

Measuring principle

FRA instrument, which uses the classical SFRA, must measure two voltage signals which one corresponds to the voltage on the input phase terminal and the second one on the sensing impedance, which corresponds to the current-flown through DUT. The simplified electrical schematic is shown in Fig. 15.

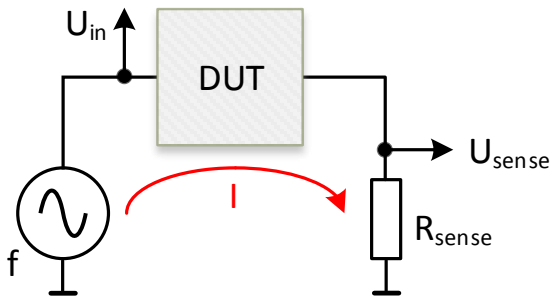


Fig. 15 Measurement principle of DUT impedance

Impedance is then given by:

$$Z = \frac{U_{DUT}}{I} = R_{sense}\frac{U_{in} - U_{sense}}{U_{sense}} \tag{7}$$

Traditional Impulse Method

In contrast with the previous method, the impulse method tries to compensate for several imperfections of the swept mode. Basic principle is described in [17] and especially in [19]. Measurement is done in the frequency domain with a single impulse transition response analysis.

Test connection for the impulse measurement is shown in Fig. 16. The network analyzer is altered by the impulse generator with a high-speed digitalization unit. The main idea behind this measurement is to produce a single low voltage impulse to one terminal of the DUT and measure a particular response to this impulse on the neutral terminal. Similarly, the current on the neutral terminal should be properly converted to the voltage. There is a possibility to use another value of a sensing impedance in

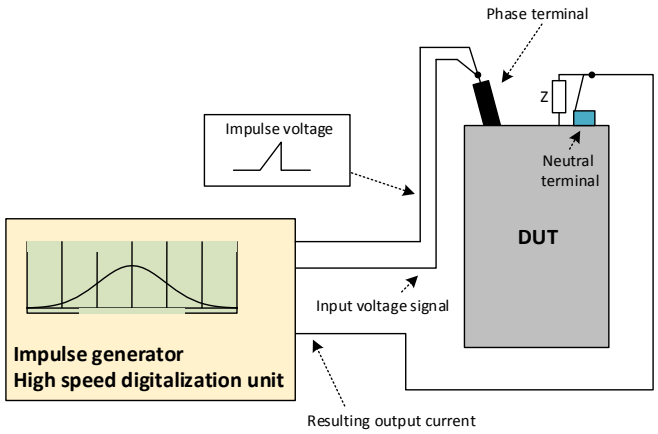


Fig. 16 Test connection and setup for a low voltage impluse FRA measurement

contrast with the internal one in the network analyzer. Once the time-domain record of the voltage (input) and current (output) are recorded, the transfer function is calculated as the Fast Fourier Transform (FFT) of the output divided by the FFT of the input.

Unfortunately, this method also has its limitations. There are several practical problems that cause difficulties with repeatable results together with an accuracy aspect. Present noise in the signal has a negative effect on the final FFT result. The easiest elimination is to apply to the average of more than one result. This is one of the recommendations in [17]. A good level of repeatability is limited by another two factors. Test impulse should be the same for every single measurement of the averaged set. The second is the quality and performance of the digitalization unit. The constraints of this method are summed up as follows:

- Advantages
  - Overcome mentioned problems of swept method
  - Theoretically shorter time to proceed method
- Disadvantages
  - Impulse generation issues
  - Noise background should be eliminated
  - More complex digital signal processing
  - Repeatability problem

2.2.3 Data interpretation

The correct data interpretation and visualization is a key process for all methods of diagnostics. The important fact is that the ratio between impedance (or admittance) of the DUT versus frequency consists of several peaks, local minimums, and/or resonances forms a unique signature. This signature changes as the DUT characteristics change. There is no special rule for the signature appearing for a particular DUT. Analysis of FRA test results always involves the comparison of two or more signatures of the FRA response. It was mentioned before that one way is to compare only the FRA results of one device at various times. Comparing two same units at one time is the second approach. The results are expected to be the same because it is very unlikely that both DUTs will suffer from the same damage at the same time. There is also a possibility to measure FRA immediately after manufacturing of the DUT, then at the location

of operation, and after that, periodically. This comparison may reveal the particular moment of the damage. There are commonly used several interpretation methods. The [17] describes the traditional method and proprietary method developed by the National Electrical Energy Testing Research and Applications Center (NEETRAC).

Traditional method

The common problem around diagnostics is the fact that there are almost no specific rules on how to determine if some DUT is going to fail or not. A high degree of specialization and expertise is required for proper judgment. This is the main idea behind all traditional methods. Anyway, the process could be somehow generalized. Example of some measured signature data is in Fig. 17 from [20].

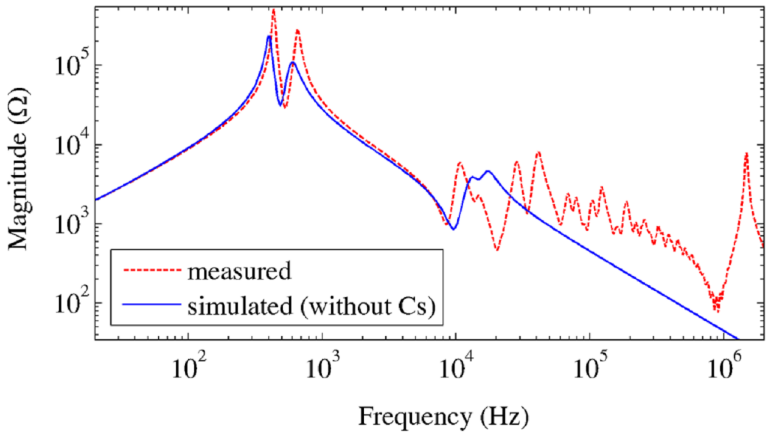


Fig. 17 Test connection and setup for low voltage impulse FRA measurement [20]

There are some points of interest, which must be correctly localized by a skilled operator. When comparing two transfer functions, the general approach has been to look at the location (frequency) of the resonant peaks in the transfer function magnitude plot. Shifts in a frequency of a particular resonant peak or the appearance or disappearance of peaks in the transfer function at a particular frequency represent cause for concern. Anyway, this data interpretation is extremely subjective and must be done by staff with a large experience. To sum up, this method has some degree of reliability, but it depends on individual thinking and hundreds of FRA signature analyses. Nevertheless, some failures could be localized easily by this traditional method because the operator could apply some of the precedences while inspecting the FRA signature. For example, the [21] shows FRA comparison between single (normal) grounding of the core and double grounding. This is often a problem where overheating could be the result of such a defect. Fig. 18 from [21] shows the frequency shift of the resonant peak.

Weighted Normalized Difference

Weighted Normalized Difference (hereinafter as WND) could be added to those methods, which does not rely on the individual skills of some operator. This method has been introduced by the National Electrical Energy Testing Research and Applications Center (NEETRAC) in [17]. As it was mentioned many times before, the FRA measurement could indicate some defect. But this can not be done from a single fingerprint. Comparing is the key process. WND method tries to define a single numeric value that

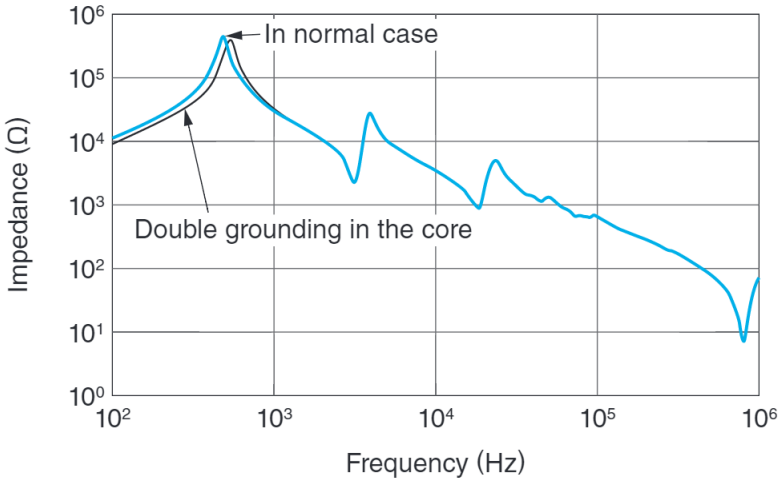


Fig. 18 Issues in grounding of the core [21]

tells about two FRA signatures difference. Shapes of two (or more) FRA measurements are inputs to the WND calculations. The key processes behind this algorithm are (acc. to [17]):

- the arithmetic difference between transfer function magnitudes is computed at each frequency.
- each sample is normalized
- each sample is weighted according to an error function at a particular frequency
- WND = a constant times the average of the weighted values

After WND value calculation is done, there are some intervals, which describe changes in the DUT. For instance, if the value is below 25, there is no or very slight change. In another way, if the value is more than 100, there are major changes in DUT. Nevertheless, this method is somehow proprietary and could be used as-is or a little modified to compare FRA signatures. Unfortunately, this interpretation does not give any specific cause of the failure, just the progress or change level.

Objective Winding Asymmetry

WND method could also apply in a different way. Objective Winding Asymmetry (hereinafter as OWA) does not take into account a single DUT with several (periodical) FRA signatures, neither the FRA of a particular unit nor the FRA of the sister unit. The main idea of this method is to use WND for the same transformer at the same time. OWA must be done, for instance, on a three-phase transformer where the high voltage windings and low voltage windings are suspected. This method is also patented by NEETRAC. It is possible to run diagnostic also when no historical data is available. The method uses strict geometry, which is typical for three phases DUTs, and this fact is used to draw conclusions when comparing transfer functions across phases. In the OWA, the WND numbers are calculated in some way, as it was mentioned before. The difference is then in fact that, instead of comparing results taken on different dates or from sister units, each high voltage winding is compared to the other two high voltage windings on the same transformer, and similarly, each low voltage winding is compared to the other two low voltage windings. The OWA is given in percentages, and it is defined by the average of the highest two WND numbers divided by the lowest WND number for the three separate winding phase comparisons. Then subtract one from

the result and convert it to percent. Afterward, there are some percentage intervals to judge the result. This calculation is again proprietary, and it is published in [17].

Mathematical solution based on DL 911/2004

Most of the current instruments and their PC application use the traditional judgment method together with mathematical solutions based on the Chinese standard DL 911/2004. This standard is not an open-source document. One can speculate that this algorithm is somehow similar to the WND calculation.

2.2.4 State of art in FRA instruments

There are several well-known companies, which are designing and manufacturing instruments for high-voltage diagnostic disciplines like FRA. To be more specific, there is a list of the most important players in this field:

- Omicron (www.omicron.at)
- Doble Enginnering (www.doble.com)
- HAEFELY HIPOTRONICS (www.haefely-hipotronics.com)
- Tettex (bought by HAEFELY HIPOTRONICS)
- Megger (www.megger.com)

FRA analyzers, together with their technical parameters and data representation possibilities, will be described in the following text.

Omicron FRAnylzer

Omicron offers a single FRA system called FRAnalyzer, which contains everything needed for diagnostic purposes. The image of the whole system is in Fig. 21

Fig. 19 Omicron's FRA system FRAnalyzer

This instrument provides only the classical SFRA method (sweep frequency response analysis), which is described in 2.2.2. The frequency range of the instrument is:

$$10\,Hz < f < 20\,MHz$$

Data visualization

Data is transferred to the computer via a USB interface, and it is processed by Omicron's PC application. According to the [22] the user can use the traditional method (expertise) to judge the results of FRA (described in 2.2.3). There is also implemented support for mathematical auto judgment based on the Chinese standard DL 911/2004

Parameter	Value
Frequency range	10 Hz. . . 20 MHz
Measuring point spacing	logarithmic, linear or both
Calibration interval	3 years
FRA method	sweep frequency
Output impedance	50 Ω
Output Amplitude	2,83 Vpp, resp. 1 Vrms at 50 Ω load
Number of measuring points	max 3201
Inputs	Reference and measurement
Impedance	50 Ω or 1 $M\Omega$
Dynamic range	> 120 dB
Guaranteed accuracy	± 0.3 dB to -50 dB
	± 1.2 dB from -50 to -80 db
Host connection	USB 1.1
Size	26 x 5 x 26,5 cm
Supply DC	10V .. 24V
Supply AC	100V .. 240 V / 50 .. 60 Hz

Tab. 2 Omicron's FRAnalyzer parameters

Doble M5x00

Doble offers two systems called M5300 and M5400. While both of them can suit FRA analysis, the M5300 is better equipped. M5300 can be used without a PC or laptop, while the M5400, similarly to the Omicron, the PC is required to run the analysis. Both types are shown in Fig. 20. M5x00 uses the sweep frequency method similarly to the Omicron. They have a slightly different frequency range up to 25 MHz. The main advantage is larger excitation voltage comparing the Omicron. This fact could help to excite the winding in the whole frequency range.

Data visualization

Data interpretation is available on the built-in screen in case of M5300 or via PC software in case M5400. The judgment is done in the traditional way (expertise).

The M5400 comes with intuitive, Windows-based SFRA software that runs on a user-supplied PC. The software allows you to compare and analyze SFRA measurements. It also comes with pre-configured templates as a guide to specifying tests for the field.

Parameter	Value
Frequency range	10 Hz. . . 25 MHz
Measuring point spacing	logarithmic
Calibration interval	3 years
FRA method	sweep frequency
Output impedance	50 Ω
Output Amplitude	20 Vpp at 50 Ω load
Number of measuring points	max 1800
Inputs	Reference and measurement
Sampling frequency	100 MSPs
Impedance	50 Ω
Dynamic range	> 90 dB
Repeatability	± 1 dB to -80 dB
Host connection	USB / Ethernet
Size	25,4 x 40,6 x 39,4 cm (M5300)
Supply AC	AC 100V . . . 240 V / 50 or 60 Hz

Tab. 3 Doble's FRA instrument M5300/M5400

(a) M5300 FRA **(b)** M5400 FRA

Fig. 20 Doble's FRA instruments

Haefely Hipotronics FRA5310 (Tettex)

The FRA5310 uses the classical approach with the SFRA mechanism again while combining some of the advantages from the previous two systems. The instrument has its own built-in display and has a higher amplitude at the excitation output, which will again better work with various DUTs. Input impedance is selectable like Omicron.

Fig. 21 HAEFELY HIPOTRONICS FRA5310 analyser

Data visualization and judgment are done in two ways, the same as Omicron. FRA5310 relies on the Chinese standard DLT 911/2004.

Parameter	Value
Frequency range	10 Hz... 10 MHz
Measuring point spacing	logarithmic
FRA method	sweep frequency
Output impedance	50
Output Amplitude	12 Vpeak at 50 Ω load
Number of measuring points	max 2000
Inputs	Reference and measurement
Sampling frequency	100 MSPs
Impedance	50 Ω or 1 $M\Omega$
Dynamic range	> 100 dB
Repeatibility	±0.5 dB down to -90 dB
Host connection	USB / RS232
Size	41 x 31 x 17 cm
Supply AC	AC 90V ... 265 V / 50 or 60 Hz

Tab. 4 FRA instrument FRA5310

3 Objectives

The main aim of this work is to design and develop complete fully-functional instrumentation which will extend the state-of-art devices and could offer better performance parameters and also increase the robustness of the manufactured device. In addition, the future instrument should make the operation with this diagnostic method more convenient comparing the others.

This main goal of the thesis, which is in the form of device development, has to be separated into the smaller stages or work phases to proceed towards the successful instrumentation design. Each sub-goal will be defined in a more detailed way. These necessary stages are:

- **Research of the FRA method and state-of-art instruments**

  In order to achieve the main goal, this sub-stage is one of the very important beginning goals. The output of this stage should define the starting line of the following development. All key information about the proposed FRA method, together with the parameters of the common instruments, should be analyzed and listed. The advantages and disadvantages of all devices should be identified.

- **Analyse the requirements for the hardware - HW concept**

  The concept and block overview of the hardware should be clearly defined before any design and research part of the particular device. This sub-stage should answer the question of the key parameters of the future device. This list of requirements should be the main output of this part. Special emphasis must be placed on the cross-method compatibility in the field of HV diagnostics. In other words, the output of this part should be usable in various diagnostic methods.

- **Setting up the team work**

  As the hardware design is predicted as a quite complex system with the hardware part, software (firmware), control computer software, and other smaller tasks, the setting up of the teamwork is a very important section. This doctoral thesis is covered by a larger university funding project of high-voltage diagnostic system diagnostics.

- **Electrical design of the system**

  This stage should provide the design transfer from the concept and block diagram into the real component parts selection and to the full schematic design of the selected hardware units. The following stage after the completion of the schematic material is in the form of the high-speed and modern PCB design. Not only PCB routing should be done, but also the complete mechanical and interconnection idea should be defined clearly to ensure issue-less manufacture process

- **Complete manufacture process of prototypes**

  At least one fully functional and assembled prototype must be the output of this process. Without any ready hardware, there is no possibility to proceed with the following defined sub-goals.

- **Digital signal processing design**

  Research in the field of the VHDL and/or C code algorithms involved in the vector-voltmeter applications should be the major part of this partial objective. The specific implementation of signal processing and data handling should be the important output.

- **Software work connected with the visualization**

  Communication with the host system and visualization platform must be implemented correctly to ensure a complete and fully-functional diagnostic system. This work part should select the suitable communication standard as well as describe and the implemented software support inside the instrumentation.

- **Uncertainty and accuracy analysis**

  Proposed and designed signal processing blocks should be analyzed in terms of the accuracy aspect. This work part should pay attention to the theoretical estimation of the final accuracy of the inside DSP blocks. Moreover, these results should be discussed and compared with the laboratory tests.

- **Verification of the system in laboratory / real-environment**

  One of the most important partial aims is the verification of the system in the laboratory environment as well as with the real device-under-test (DUT). First of all, the specific test types should be selected, and after that, the tests by themselves could take place. The output of this stage must be evaluated in detail.

Team work setup

Research team

High-voltage diagnostic methods are suspect of several-year research and development work of a university group. Our research team consists of the following members:

- doc. Ing. Josef Vedral, CSc.
- Ing. Radek Sedlacek, PhD.
- Ing. Ondrej Teren
- Ing. Jan Tomlain

This group is involved in the following high-voltage diagnostic research projects:

- TA02010311 - Intelligent measuring diagnostic system for determining the operating state of high voltage electric machines, both rotating and non-rotating
- SGS15/213/OHK3/3T/13 Nondestructive diagnostic methods of HV power transformers

- TH02020288 - The compact diagnostic system for operating high voltage condition monitoring of electrical machines using DC and low-frequency test voltage

Doc. Vedral is the supervisor of all projects and partial works on the projects. Dr. Sedlacek directly collaborates on hardware and software development in terms of conceptual design and shares engineering knowledge. Mr. Teren and I work in a team on all scientific and engineering tasks among these projects. As the tasks and developed tools become more and more complex, the complete results are the results of the collaborative research. This doctoral thesis describes in detail the theory, methods, and own work of my contribution to the work. The shared work of Mr. Teren, which is implemented and used in the whole system, is described very briefly, and the details can be found in the colleague's doctoral thesis. Vice versa, my designed parts are described only shortly in Mr. Teren's work. With this, I would like to thank all research groups for their excellent collaboration on all mentioned projects.

To sum up, the work and collaboration team set up on the system is divided as follows:

- **Tasks of my doctoral thesis research**

  Hardware design of the FPGA digital board which could be used as cross-platform for various high-voltage diagnostics (FRA, DSP, PD, and others)

  Hardware design of the powering system for portable diagnostic instrumentation

  Excitation board design and the construction finishing (enclosure, interconnection idea)

  VHDL and C code for signal processing (LIA and FRA method) with laboratory verification.

  Frequency-response analysis FRA testing on real DUT with evaluation

- **Tasks of Mr. Teren thesis research connected with this diploma thesis**

  Hardware design of the ADC/DAC daughterboard, which could also be used as cross-platform for various high-voltage diagnostics (FRA, DSP, PD, and others)

  Signal processing (LIA) with laboratory verification

  Control software for high-voltage diagnostic methods.

4 Analysed HW requirements on instrumentation

Specification for the whole new instrumentation was analyzed based on the previous chapters and the current state of the art of FRA instruments on the market (described more in deep in 2.2.4). All of the classical instruments rely on the SFRA approach. There are no instruments on the market with the impulse method implemented. All experiments with impulse method were done only under laboratory conditions acc. to [23]. This fact supports the reason while this work and further design will use SFRA analysis as the basic operational method. This decision affects the whole HW design of the instrumentation.

4.1 Frequency working range

For the swept frequency range, the main parameter is the working frequency range. Designed HW should be capable of measurement in the following extended frequency range:

$$1\ Hz < f < 25\ MHz \tag{8}$$

This range covered all instruments on the market and extended their operating conditions from both limits. As was discussed earlier, there is no valid standard for FRA measurements. However, most of the captured FRA fingerprints of a variety of devices-under-test are in the range from tenths of Hz to several MHz.

4.2 Excitation voltage

The very important parameter is also the excitation signal characteristics. There are various implementations from low-voltage up to 20 Vpp in the case of Doble's instrument. The excitation voltage source and its output power should be sufficient for sourcing various loads at various frequencies. Results from [20], and [21] show that the typical impedance of DUT is in the range from 10^6 Ω down to 10^1 Ω. The advantage of the classical SFRA connection shown in Fig. 14 is that the excitation voltage is measured at the input terminal of the DUT and evaluated based on this value. In other words, the level of the output voltage may vary with frequency to avoid overloading the output buffers. Based on the instruments, the voltage range of the output should be at least:

$$U_{out\,\max} = 30\ Vpp \approx 10.6\ Vrms \tag{9}$$

The worst power estimation is applicable in the higher operating frequencies, where the load becomes higher. Nevertheless, the maximum output power is in units of several Watts.

4.3 Input voltage range and sensing impedance selection

One of the issues is the proper selection of the sensing impedance, which is directly connected with the input voltage range of the sensing analog to the digital channel. This signal is closely related to the impedance range of the particular DUT. To analyze this problem more in deep the best way is to pay attention to the minimum and the maximum impedance level. Imagine that sensing impedance $R_{sense} = 50\ \Omega$ and excitation voltage $U_{out} = 10.6$ Vrms. Based on Eq. 7 we get:

$$U_{sense} = R_{sense}\frac{U_{in}}{Z + R_{sense}} \tag{10}$$

$$\begin{aligned} U_{sense} &= 530\,\mu V \quad I \approx 10\,\mu A \qquad Z = 10^6\,\Omega \\ U_{sense} &= 8,83\,V \quad I \approx 176\,mA \qquad Z = 10^1\,\Omega \end{aligned} \tag{11}$$

From Eq. 11 the input signal has a relatively large range from several hundred microvolts up to units of volts. This fact supports the usage of switchable sensing impedance based on the currently measured impedance and voltage levels at the inputs.

The second possibility is **usage of two types of ADC converters** in one time. ADC converter with higher resolution for the small frequency span and the fast ADC converter for the higher frequencies where the signal is sufficient for high-speed SAR converters.

The input voltage range of the excitation voltage (U_{in}) is based directly on the selected outputted signal defined in 4.2, and the voltage amplitude should be insufficient level for the proper sensing.

4.4 Data conversion sampling frequency

Requirement on this parameter is connected with selected frequency working range in 4.1. The core of the instrument will work fully digital the analog-to-digital (ADC) and digital-to-analog (DAC) front-end data conversion must take place. The maximum working frequency was selected as high as 25 MHz. Based on the sampling theorem, the minimum sampling frequency should be more than 50 MSPs. All instruments on the market are working with $F_s = 100$ MHz while their maximum operating frequency is 20 MHz. A higher sampling rate will bring more samples per period, and especially in the higher frequency span, the estimation of the input to output ratio could become more precise. In other words, the instruments should be capable of processing the data conversion at a rate of:

$$f_s \geq 150\ MSPs \tag{12}$$

4.5 Communication and visualization

For communication with the host system (e.g., laptop), Ethernet is one of the possible connections. It has a number of advantages like standard galvanic isolation, good throughput, and high modularity. The idea behind the networking in the field of high-voltage diagnostic is a convenient connection with several diagnostic test types of equipment (partial discharge monitors, etc.) with one operational host computer. In addition, devices should implement classical peer-to-peer connections like USB.

4.6 Power supply and enclosure

The system should be able to run from batteries and from the AC power network as well to obtain maximum versatility. Input voltage range should be adapted for a direct connection in a vehicle power network (nominal values are 12 VDC or 24 VDC). This connection supports the on-the-field maintenance test where is no other power supply available. On the other hand, in-house static measurements could run directly from the local AC power network.

Mechanical finish and enclosure selection must be in industrial grade to ensure operation in various conditions.

5 FPGA board design and development

Hardware for the whole diagnostic instrument consists of three main parts. The core part of the digital signal analysis is an FPGA board. Data conversion and acquisition are made on an analog daughterboard. A high voltage interface will be implemented on the third high-voltage excitation part. The designed system will use the frequency swept method, which is described in chapter 2.2.2. According to this method, designed HW should fulfill the possibility to work in the frequency spectrum from tens of hertz up to tens of megahertz.

This section will describe the complete HW design of the FPGA part in a detailed way. All functional blocks will be presented from their conceptual way through schematic design up to the PCB layout if it is necessary. The discussed HW platform could be divided into the following sub-blocks:

- power circuitry
- external peripheral RS485 interface
- FPGA core
- DDR3 memories
- LCD display and visualization
- Ethernet interface
- USB interface
- daughterboard connection

The block diagram of the unit is shown in Fig. 22.

5.1 FPGA core

The core parts of digital subsystems are placed in the field-programmable gate array (FPGA) board. To obtain an easy implementation of real-time parallel tasks and large scalability, the FPGA architecture was chosen. The Altera Arria V GX device in the FBGA672 case provides a reasonable ratio between functionality and price. The very short summary of the main parameters could be found in Tab. 5. For a better understanding of the FPGA technology and the main advantages of such a technology, a short introduction to this technology is given below.

Unlike the possibilities of some CPUs, such as single-chip microprocessors, it is possible with the FPGAs to achieve large, complex systems that are hidden in one case. This approach is especially preferred because of the simple exchange of software blocks that are implemented within the FPGA circuit, and the main advantage is the possibility of changing the HW functionality of the circuit as a whole system by means of the SW modifications. It is necessary to realize that the FPGA circuit is, unlike the microprocessor, which contains pre-built HW support components such as counters/-timers, communication peripherals such as SPI / I2C or UART, and a large number of others, do not contain with no simplification of any functionality. The HW blocks of the microprocessors are, of course, composed of the more elementary parts of the digital electronics such as sequential and combinational circuits that once again consist of

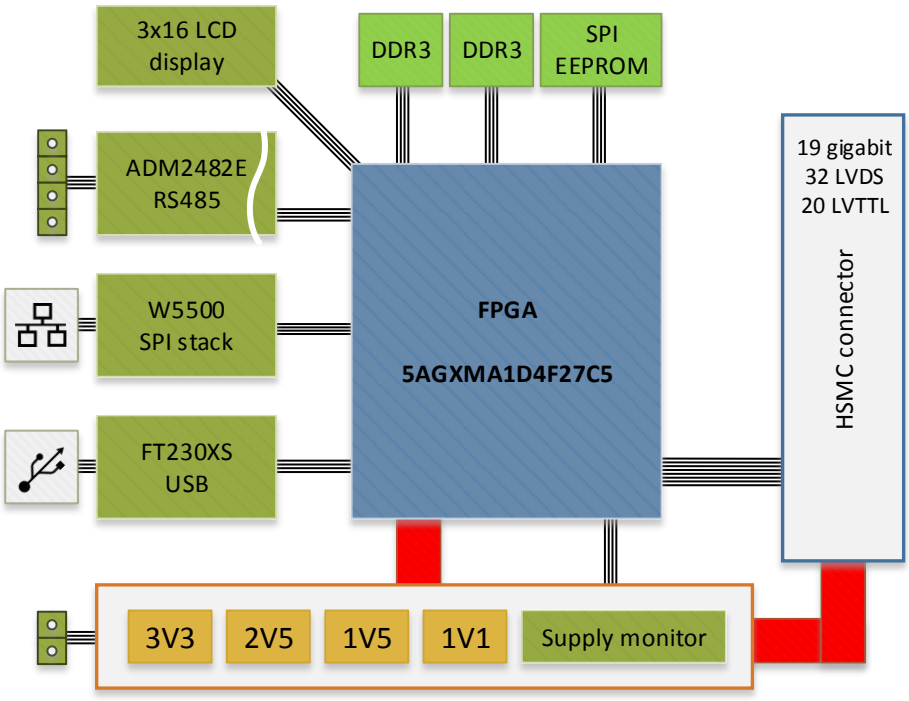


Fig. 22 FPGA board block diagram

Parameter	Value
Core Voltage	1.1 V
ALM units	28300
Total I/O	336
Gigabit TX lanes	9
Gigabit RX lanes	9
Hard memory controller	2
Embedded memory	1 MB
DSP multipliers	240
PLL units	10

Tab. 5 5AGXMA1D4F27 parameters

individual logic gates and overall functionality provided so through the proper interconnection of these basic blocks. Therefore, the Field-Programmable-Gate-Array (FPGA) does not contain pre-packaged hard-mounted peripherals composed of interconnected gates. However, FPGAs provide to the user the possibility of inserting almost any arbitrarily connected and connected logical elements, which in their increasing complexity and extensiveness can handle complex peripheral blocks such as communication peripherals, timers, memory controllers, and many others. The only limit here is the size of the field gate itself, that is, the capacity of the logical blocks that can be coupled

and used to create individual parts. When creating software or actually connecting logical elements, they are used different graphical block plotting approaches, similar to drawing circuit sketches involvement with specialized programming languages such as Verilog or VHDL. The advantage of programming using Verilog or VHDL is that this plug-in and functionality is easily portable to other FPGAs from different manufacturers and different types. Writing and programming in these languages can be compared to the higher programming languages used by microprocessors and so on. Vice versa, the graphic interface is more visual, but it does not apply to more complicated and complex engagements that are difficult to draw using basic logic elements (counters, logic functions, multiplexers, etc.). The graphical editor should therefore be used to link individual blocks that are already written in a higher language. This approach will provide a clear link and visually display block interconnection.

The FPGA circuit needs basically the following subblocks for proper operation and for easy system implementation:

- power according to the specific datasheets, described in. 5.6
- clock sourcing, at least one, described in. 5.7
- configuration memory, if it is not included inside
- debugging interface, in most cases the JTAG

The configuration memory and the debugging interfaces are shown in Fig. 23. The part **U3O** is the subblock of the FPGA chip, while the component **U2** is the QSPI Flash memory for the image of the loaded system. Its size is 128 Mbit, so the total available size of this memory is sufficient for his particular FPGA according to. [24]. JTAG configuration connector is **J1**. The pinout of this connector is the same as a

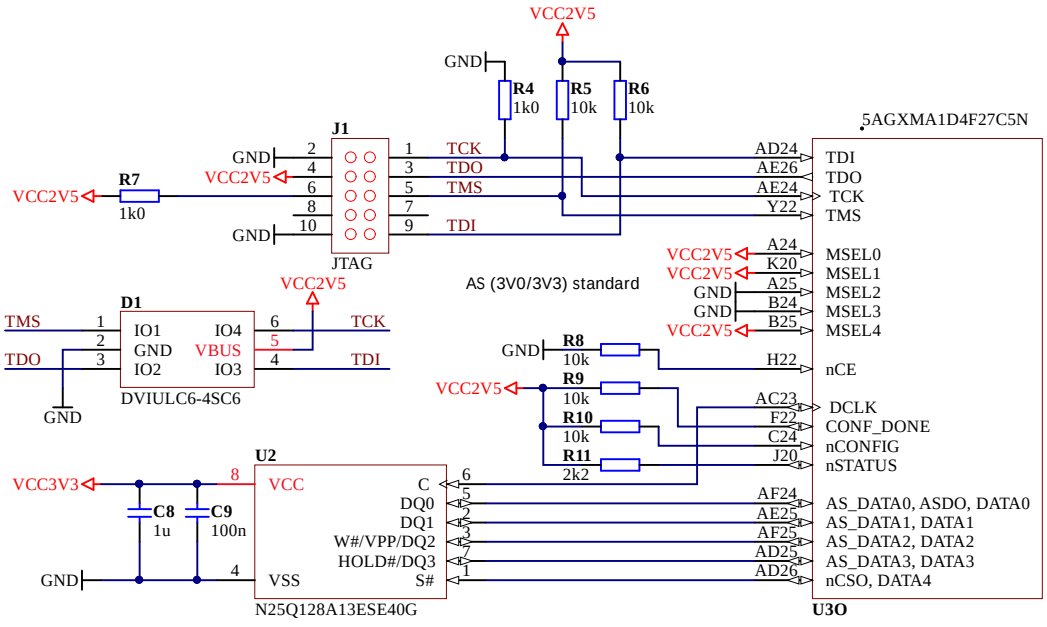


Fig. 23 Configuration memory and debug interface of Arria V

classical USB official Altera tool for loading the system image. The ESD protector **D1** is implemented due to the hazardous situations while plugging in/out the USB loading tool. The used variant of a configuration is Active Serial with external configuration memory. Other modes could be chosen with MSELx pins, and more modes could be

found in [24].

Fig. 24 Used 6-layer PCB stack

Layout of the FPGA block is the one of the most important on the board. For instance, the FBGA package determines the minimum number of layers, which has to be used. The final selected PCB layer stack is shown in Fig. 24. The used package has 26 times 26 balls minus 4 balls in the corner. The fanout of such a package will need

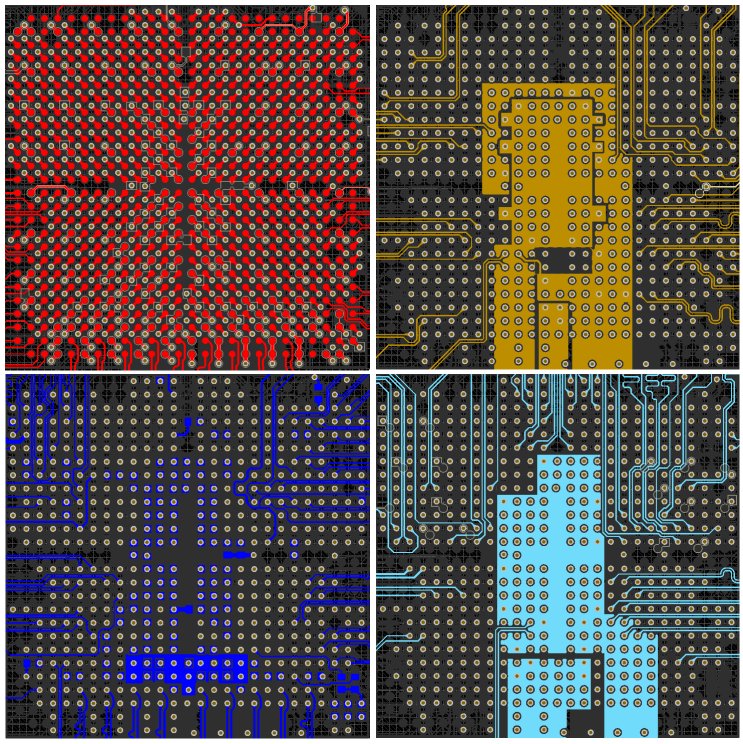


Fig. 25 Fanout of the FBGA672

at least four signal layers according to the [25]. For keeping the manufacturing prices

at low levels, blind vias technology was not used. Because of the complexity of the power structure, the internal layers were also used for power distribution. This layer contains four distinct polygons for this purpose. Finally, the 6-layer PCB was picked as a platform for the device. One can notice that each signal layer is next to some solid plane (ground or power). Critical signals should be routed in these layers to the current loops, which are formed underneath that particular connections. The colors used in the figure are the same as in the design software Altium Designer.

5.2 Ethernet connection

This type of interface was chosen because of several reasons. The first point of view, which supports this interface is the widespread implementation in all kinds of industrial and measurement systems. TCP/IP possibilities for such networking are almost unlimited. The second advantage is the possibility of easy physical layer selection. Optical or wireless (WLAN) Ethernet connection could become useful in the field of high-voltage diagnostics systems to achieve an isolation state from the machinery. In addition, a user is not limited by any proprietary host converters. The majority of PC systems already support classical Local-area-network (LAN) connection.

There are several options for how to implement Ethernet connectivity inside the FPGA-designed hardware concept. Basically, it can be divided into several possible solutions:

- external PHY, MAC control inside FPGA, TCP/IP stack in firmware
- external PHY + MAC, TCP/IP hard-wired in VHDL
- external PHY + MAC with hard-wired TCP/IP, socket control in firmware

To sum up all variants, the first solution relies on the already made medium access control block (MAC), which is designed in the FPGA core. In this case, the possible variant is the usage of Altera's Triple-Speed-Ethernet MAC (TSE) documented in [26]. To top of this, the control program inside VHDL or inside soft-core processor must implement the complete TCP/IP socketing overhead. Altera's solutions provides NicheStack [27] stack together with obligatory real-time-operating system (RTOS). Due to the licensing fees for MAC TSE and RTOS system, this variant was not selected. The second possible approach is to include MAC and PHY in the form of the external chip like 78Q8430 from Maxim company [28]. This way eliminates the MAC block, but all TCP/IP stack networking still needs to be implemented by software. These two mentioned methods have benefits in the maximum usage of the FPGA power. On the other hand, this FRA instrumentation platform does need to serve large bulks of data blocks neither the high speed is necessary.

FRA instrument implements the last mentioned option. Selected Ethernet TCP/IP controller is Wiznet W5500 [29] Complete schematic of this subblock is in the Fig. 26. The controller is connected to the FPGA general-purpose pins (GPIO) via the SPI interface, which could work with a maximum clock speed up to 80 MHz. The selected chip implements the physical layer of the internet together with a medium access control block and hard-wired TCP/IP socket networking with the possibility to serve up to 8 parallel UDP or TCP sockets. FRA instrument is designed for wired metallic connection of RJ45 connection via **J2** connector with inbuilt magnetics. For proper operation, the analog power supply for sensitive circuits is available in the form of **A3V3ETH**. The connection inside the FPGA core is made according to Fig. 27. The control lines of the SPI and addition control lines are connected directly as single-ended LVTTL pins to the FPGA chip. Inside the FPGA core, the connection continues to the border of the

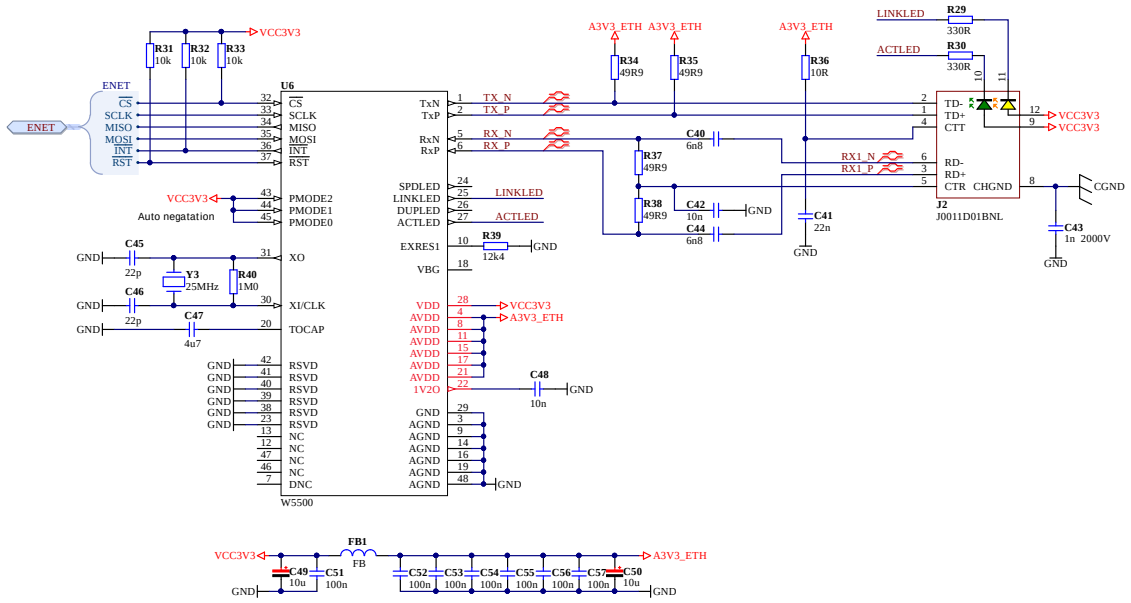


Fig. 26 Ethernet interface W5500

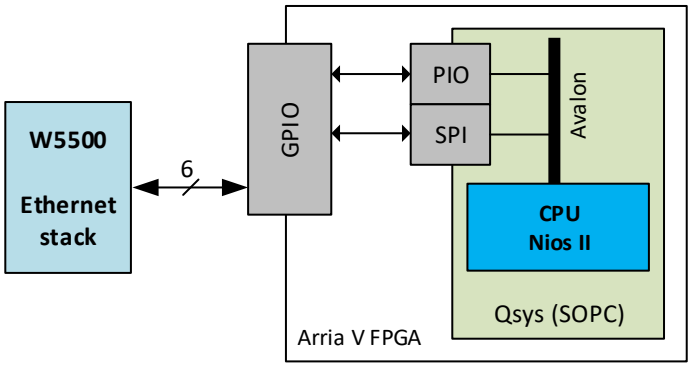


Fig. 27 FPGA Ethernet interconnection

system-on-the-chip Qsys subsystem via PIO (Pin input/output) and SPI peripheral. These peripherals are connected to the interconnection bus Altera's Avalon to the CPU Nios II core.

5.3 USB connection

The USB connection was added to the hardware concept mainly due to debugging purposes in the first place. In addition to the development stage of the device, this interface could become useful in the case of simple user PC interconnection with the device. For instance, the maintenance laboratory does not offer and support the LAN environment, so the user could easily use this interface. To simplify the USB connection in terms of hardware and software implementation and to achieve straightforward support of selected communication protocol Modbus (described in detail in. 10.4).

FTDI FT230XS **U15** acts like a transparent serial converter. On the host side, the

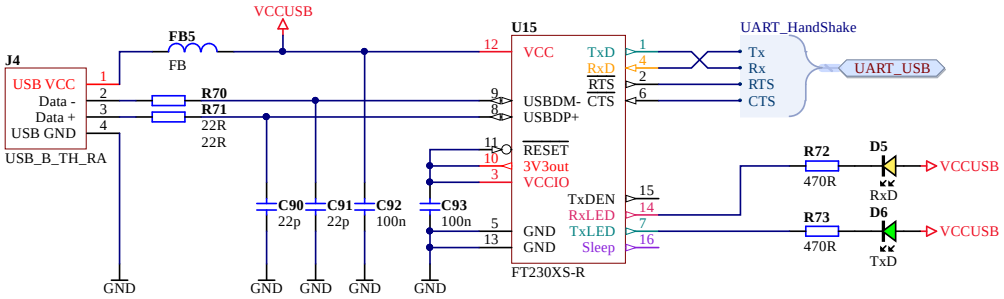


Fig. 28 USB connection FT230XS

USB device behaves like a classic serial COM port. On the slave side, the interconnection between FPGA is implemented as a full-duplex handshake serial UART connection. Physical connection is designed with classic USB 2.0 B device connector type. Differential USB pair is filtered and directly connected to the FT230XS. Inside the FPGA core, the connection is made according to Fig. 29. UART lines are fed into the Arria chip via LVTTL IO pins. It is connected inside the Qsys part via UART peripheral module, which is mapped onto the Nios CPU core to the peripheral memory space.

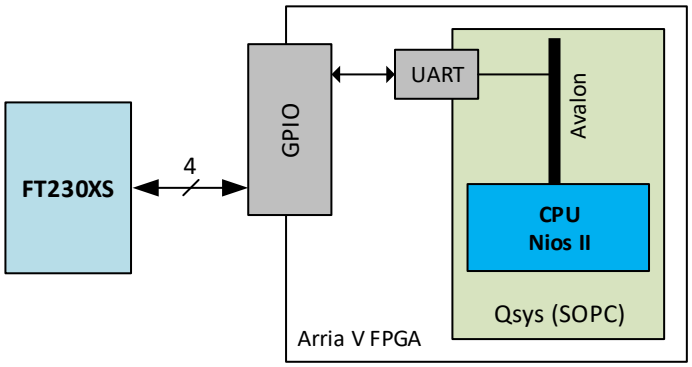


Fig. 29 USB serial connection

5.4 External peripheral RS485 port

For future purposes and the possibility for external components connection, the universal galvanically isolated RS485 interface has been designed. From the previous experience, during the partial-discharge meter design, sometimes the measuring set of instruments needs to be expanded by some special equipment, e.g., high-voltage multiplexer, switchboard circuit, PD meter calibrator, or visualization displays. These devices are typically designed in the other time period as the main units, and the future connection to the stable systems is difficult. For this future FRA, instruments implement expansion full-duplex differential RS485 port for interfacing other devices. The full schematic of this subpart is in Fig. 30.

The ADM2582E **U16** is used as a level converter with inbuilt galvanic isolation 2500 Vrms documented in [30]. It behaves like a full-duplex driver/receiver with selectable driver/receiver enable. This connection offers a direct device-to-device connection with

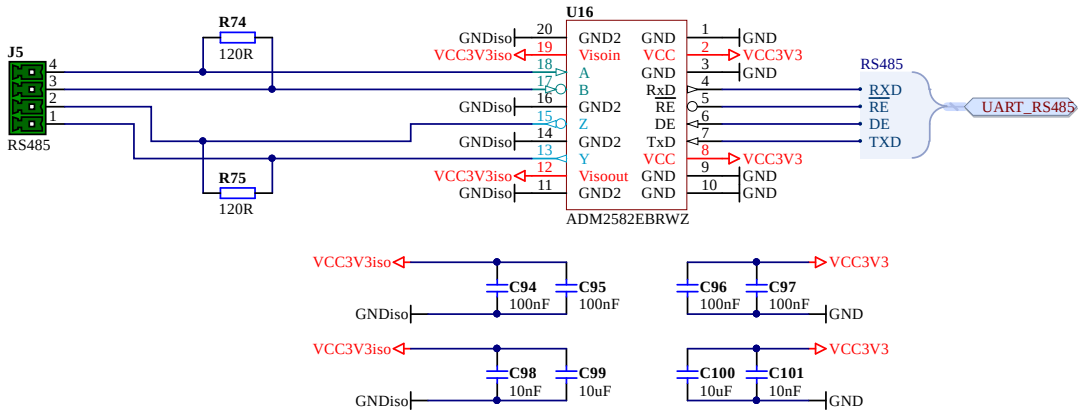


Fig. 30 RS485 external peripheral connection

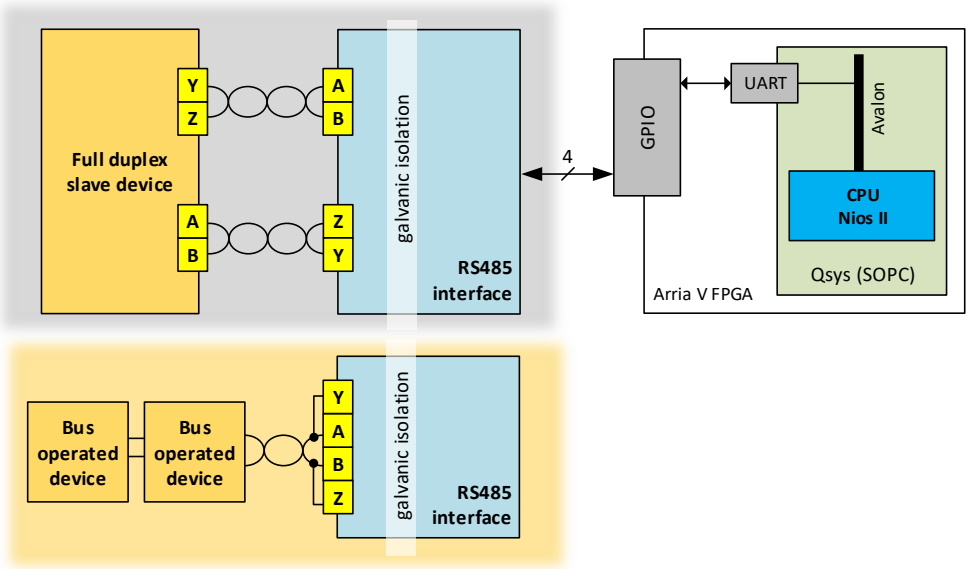


Fig. 31 RS485 external peripheral connection

the usage of the full-duplex capability as well as the half-duplex bus connection. Types of the connections are described in Fig. 31. On top of this, the Modbus protocol could be routed from the LAN connection to the external RS485 bus. The interconnection to the firmware control is done by general-purpose pins via the FPGA system inside the Qsys SoC. Complete control is designed with a UART controller, which is accessible directly in the peripheral memory space of the Nios II CPU core.

5.5 Visualization block

For signalization and debugging purposes, the hardware platform includes the character display and signalization LED diodes on the front panel of the device. The schematic

design of this part is in Fig. 32. Selected display **DI1** ([31]) is 3 rows with 16 characters each and it is only for the debugging purposes. Its position is inside the enclosure, and it is not accessible from the user's point of view anyhow. However the control LED diodes **D7,D12,D13** are designed with light-pipe **O1** for front panel position of the device. All control ports from connection ports **LCD** and **LED** are routed to the LVTTL general purpose IO pins to the FPGA core.

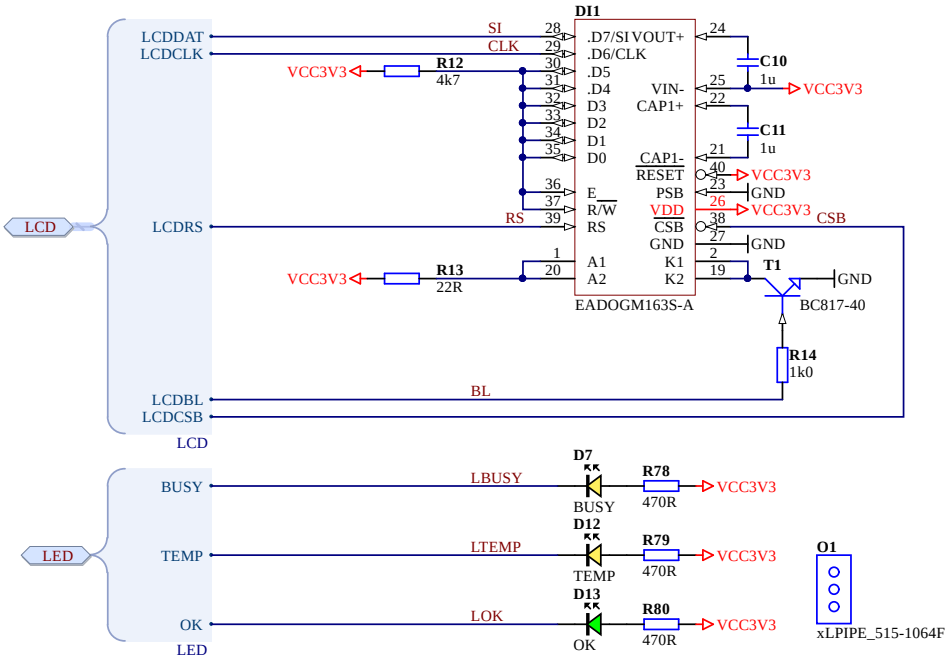


Fig. 32 Visualization block

5.6 Powering structure

The supply power section of the digitalization FPGA board is one of the most important parts of the device. FPGA designs often require special design for proper powering of all chip entities and chip sub-block. Selected FPGA chip Arria V requires a number of supply voltage rails for digital and analog purposes. A list of needed voltages with approximate current requirements is listed in the following Tab. 6. The Tab. 7 consists of measured mean currents of the selected power supply rails in active fully running mode of the FRA equipment board.

To achieve the correct operation of the FPGA core, the Altera's Arria V needs to be power sequenced in the defined order. It means that some power rails must be powered on prior to some other rails to maintain proper power-up without reset failure of any block inside the FPGA block. The power-up sequencing is described in detail here [32]. This procedure involves three separate groups of power with several voltages, detailed shown in Fig. 35. To ensure such a staging, the voltage rails were separated into several distinct regulators and converters.

The main supply voltage denoted as **VCCIN** enters the main board from the interconnection from the accupack board 7. This schematic input is shown in detail in Fig. 34. Input voltage is monitored with simple SAR Analog-to-digital converter **U12**. This converter is connected to the FPGA and CPU core via the SPI interface. Polarity

Voltage	Schematic symbol	Type	Usage
1.1 V	VCC1V1	digital	FPGA core main power
1.1 V	VCC1V1GX	analog	FPGA gigabit transciever's power
1.1 V	VCC1V1P	digital	FPGA periphery circuitry
1.1 V	VCC1V1F	analog	FPGA gigabit transciever's power
1.5 V	VCC1V5	digital	FPGA I/O banks supply + DDR3
1.5 V	VCC1V5F	digital	FPGA PLL digital power
2.5 V	VCC2V5	digital	FPGA I/O bank supply and pre-drivers
2.5 V	VCC2V5F	analog	FPGA PLL analog power
3.3 V	VCC3V3	digital	All other board peripherals
5.0 V	VCC5V	digital	Auxilary supply for termination DDR3
0.75 V	VTT_0.75	digital	Termination potential for DDR3
7.4 - 8.4 V	VCCIN	battery	Input power from the battery pack

Tab. 6 Summary of used power rails in the FPGA board

Voltage	Schematic symbol	Measured current in active mode [mA]
1.1 V	VCC1V1	133.5
1.1 V	VCC1V1GX	less than 1.0
1.1 V	VCC1V1P	26.3
1.1 V	VCC1V1F	less than 1.0
1.5 V	VCC1V5	14.0
1.5 V	VCC1V5F	2.7
2.5 V	VCC2V5	132.2
2.5 V	VCC2V5F	126.2
3.3 V	VCC3V3	78.1
5.0 V	VCC5V	less than 1.0
0.75 V	VTT_0.75	less than 1.0
7.4 - 8.4 V	VCCIN	to daughter board around 310.0

Tab. 7 Summary of current consumption of power rails

protection is provided by **D9,D10**. Overvoltage transients are protected by voltage suppressor **D11**. Accupack board interconnection is done by connectors **J4,J7**. **CHRG** and **ACIN** signals are from the charger monitor. Signal **KILL** is the control signal of the push-button controller. Its usage is ideal for software switch-off purposes. Signals are protected against ESD with **D8**. Battery supply voltage then continues directly to the daughterboard interconnection block, which is described 5.9. The main supply produces a 1.1 V supply for digital and analog parts in the FPGA core and for the gigabit transceiver blocks inside FPGA. When these supplies are ready, the supply chain

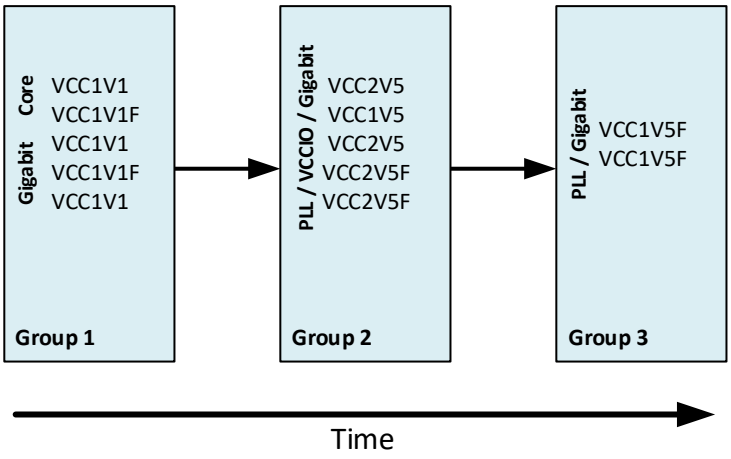


Fig. 33 FPGA power sequencing Arria V

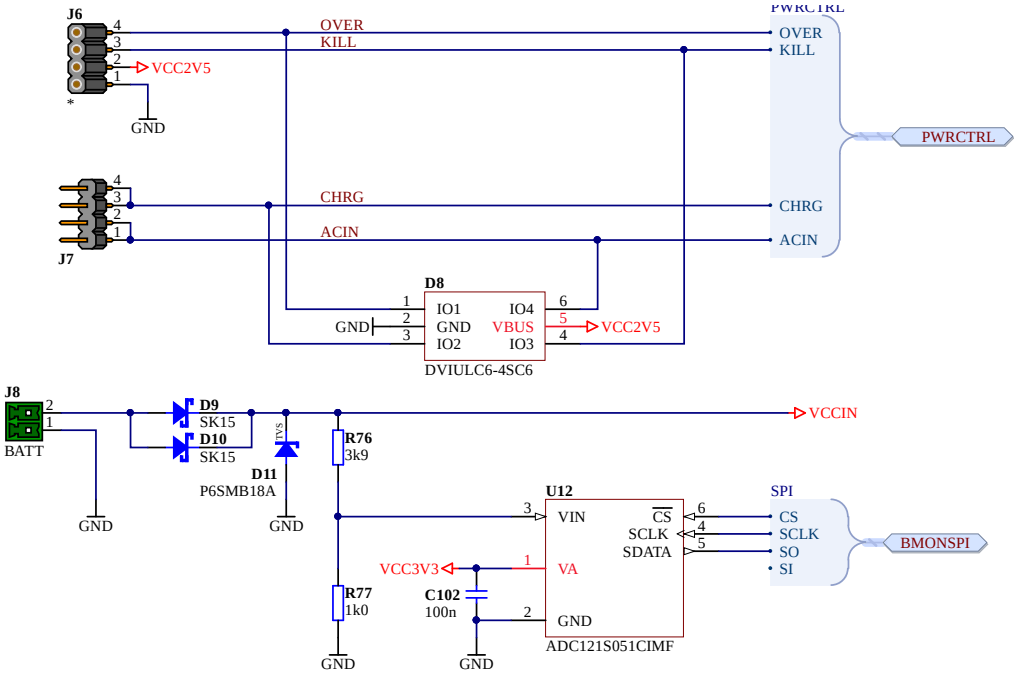


Fig. 34 Battery input schematic

continues with 2.5 V for IO banks and 1.5 V for DDR3 memories. General-purpose 3.3 V supply is created at this stage as well. 1.5 V for PLL and gigabit transceivers are at the last stage of the supply chain. In parallel with this chain, the potential for a DDR3 termination circuit is created in the form of **VTT 0.75**. All supplies are designed with 0 Ω resistors or with the usage of ferrite bead filters for easy testing after assembly. This way helps to measure precise currents of all circuitry if it is needed.

5.7 Clock distribution

The clock distribution network of the digitalization board was designed to offer maximum versatility for future application changes or other application implementation.

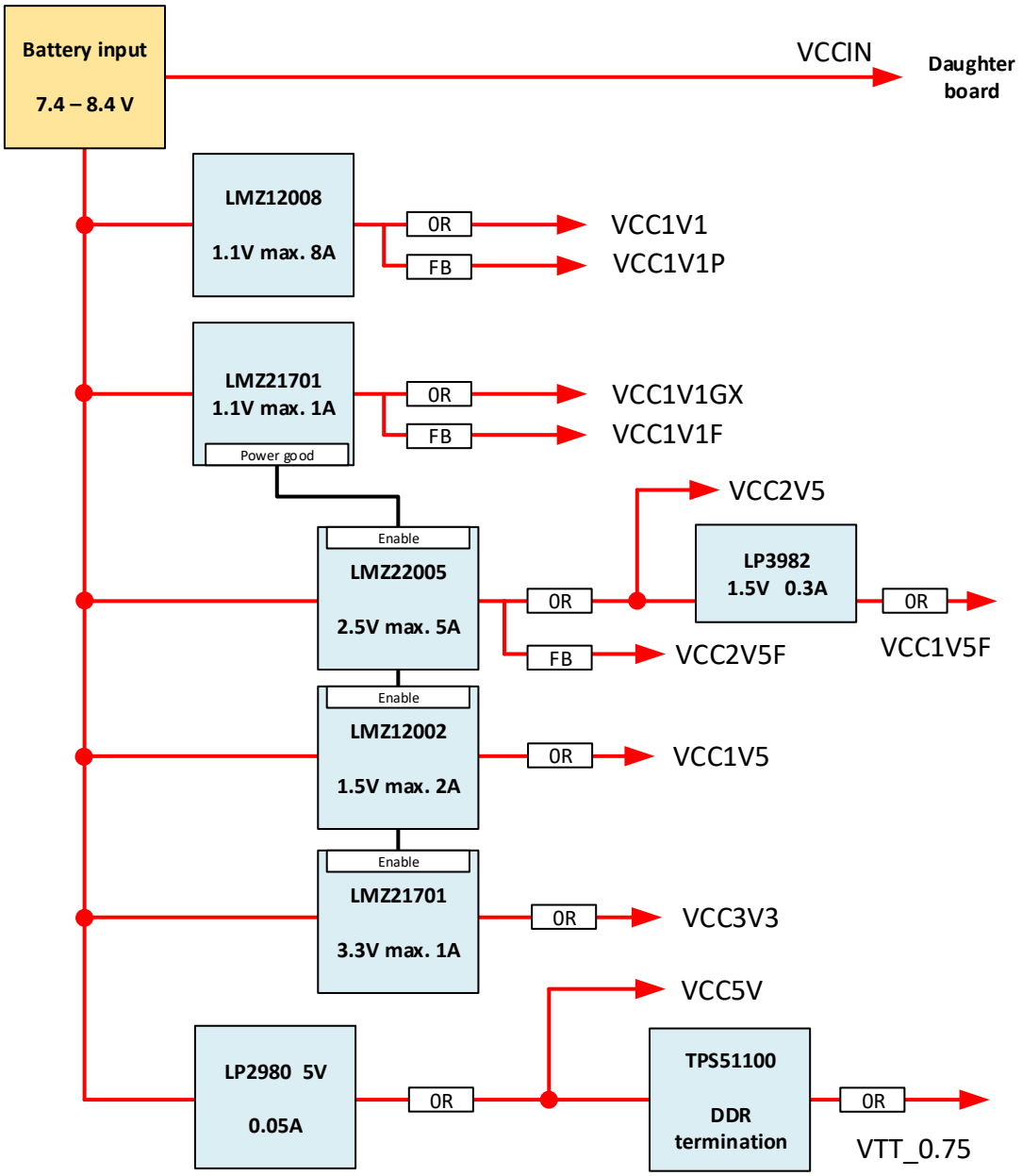


Fig. 35 Desing of the complete power chain of the FPGA board

FPGA device needs at least one clock source available after start-up for proper operation of the core. Anyway, some FPGA subblocks like gigabit transceivers or external parts need separate clock sources in specific frequencies. The schematic part of the clocking system is shown in Fig. 36.

The main clock source for the FPGA is 100 MHz fully differential LVDS oscillator **Y1**. Differential signaling of the clock helps to maintain clock integrity in a harsh environment affected by, for instance by noise, etc. Typical output signal definition for LVDS is shown in Fig. 38. The common-mode voltage is 1.2 V while the total differential swing is typically 350 mV according to the standards [33]. The difference between signals V+ and V- are evaluated as logical states. The auxiliary clock source is

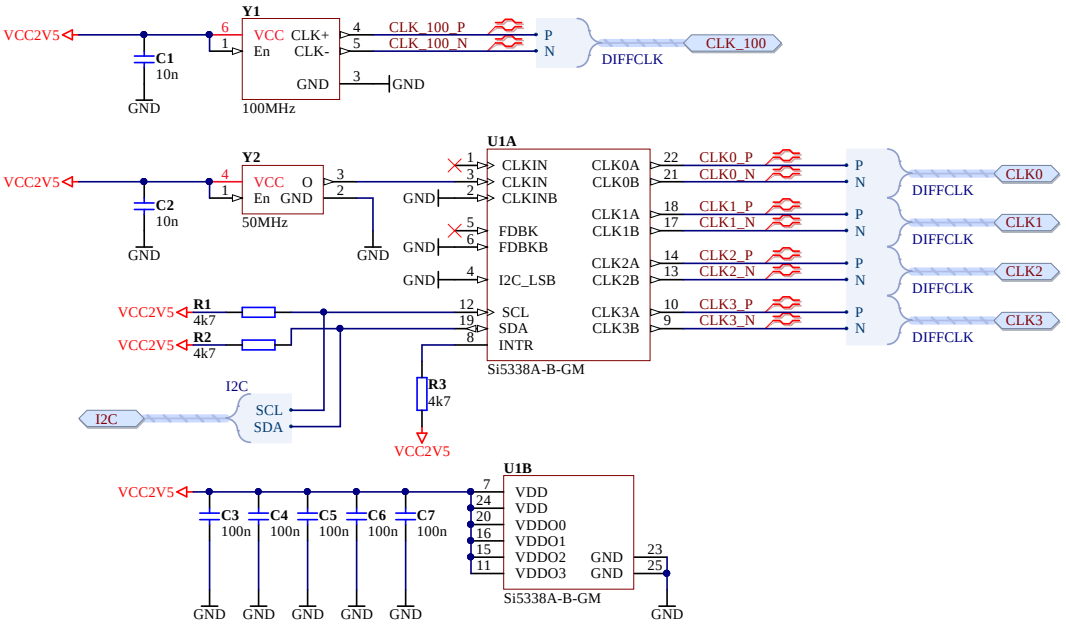


Fig. 36 Clocking circuit of the FPGA board

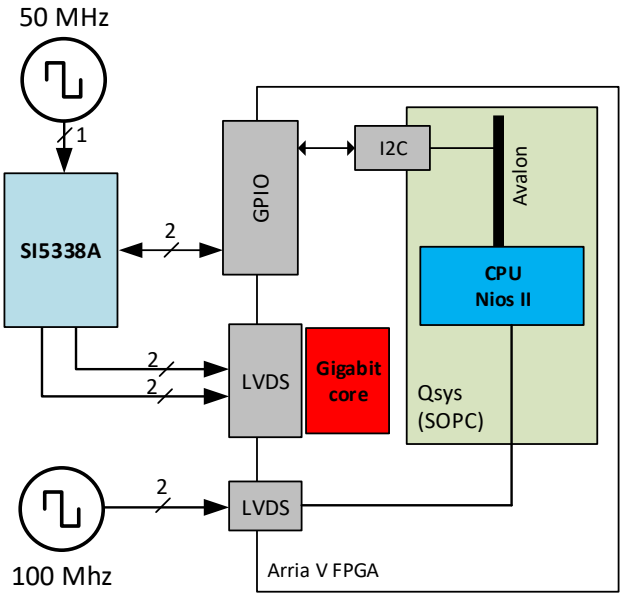


Fig. 37 Interconnection of clock system and the FPGA core

generated by the special clock generator SI5338A **U1**. The connection of the universal clock generator and its parameters could be found in [34]. This device is clocked by the external crystal **Y2** with frequency 50 MHz. Clocks denoted as **CLK0**, and **CLK1** are used as a differential excitation clock for the gigabit transceiver blocks inside the FPGA. Altera's Arria V device can not use an internal PLL circuit for self-excitation of the transceivers. Thus an external clock must be provided for these purposes. Configuration

of SI5338A circuit is done via the I2C interface from the FPGA core and from the CPU runtime code. The block diagram of this connection is shown in Fig. 37.

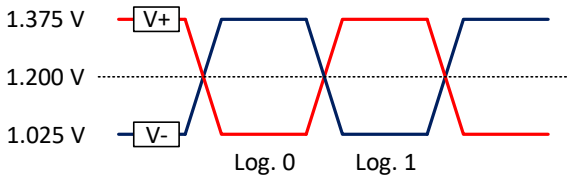


Fig. 38 LVDS voltage levels

5.8 DDR3 memories

The selected FPGA chip offers 1 MB of the internal memory space. This space is used as the code and data space of the NIOS soft-core processor. For additional memory requirements, two external DDR3 chips with a total capacity of 2x 64 MB. Each chip is connected to the distinct hard memory controller (HMC) of the FPGA. HMC is a hard-wired peripheral part that could be used for interconnection with several types of memory organization types or external peripherals with memory interface. Fig. 39

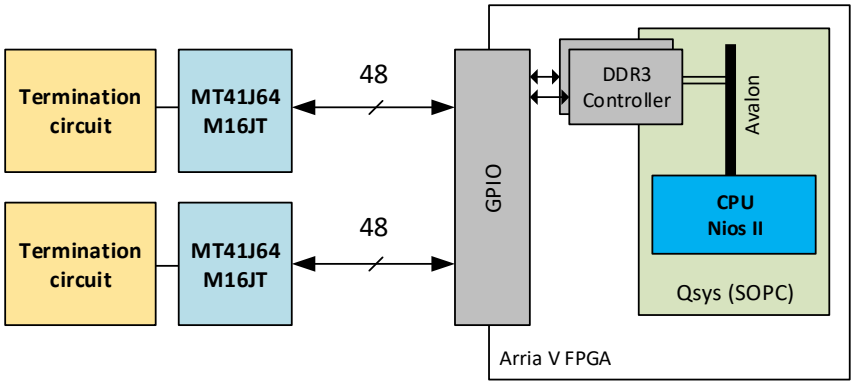


Fig. 39 Connection of the memory chips to the FPGA core

shows the basic connection of the external memory chips. Each memory is connected via GPIO pins inside the FPGA part. Signals then lead to the Qsys subsystem via DDR3 memory controllers, which are mapped into the CPU Nios memory space as data memory. The basic configuration of the DDR3 connection is as follows:

- Row count: 13
- Column count: 10
- Bank address: 3
- Memory device speed grade: 666.667 MHz
- Memory clock frequency: 300 MHz

5.9 Daughterboard interface on FPGA board

The connection between the data converters and the FPGA digitalization unit is made by a special high-speed interconnect 160 pin connector type High-Speed Mezzanine Card (HSMC). The manufacturer of this connector is SAMTEC, and its precise ordering type number is QSH-090-01-X-D-A-RT1 ([35]). This connection is implemented on the right corner of the PCB, and its basic block connection diagram is shown in Fig. 40. The connection is in the form of the 19 LVTTL general-purpose pins and several LVDS fully-differential lines for interfacing the data converters with the serialized data bus. This part consists of 18 receive lines and 14 transmit lines. The maximum throughput of these LVDS lanes is up to 400 MHz according to the [33]. These LVDS pairs could be used for any data communication purposes and also for the clock excitation of the slave peripherals on the daughterboard as well as these pins could be configured for single-ended GPIO pins in special cases. The rest of the connector is occupied by the gigabit lanes from the Arria V GX core. This interface could produce a nominal speed of 1.25 Gbps. Its voltage standard is PCML, and it is compatible with the majority of the Ethernet gigabit PHY controllers with Serial-gigabit-media-independent-interface (SGMII) interface like Small-form-pluggable (SFP) cage modules. The slave board supply is also available on the connector. Two voltage rails are offered for the daughterboard according to the 5.6. First is a direct connection of the **VCCIN** from the battery, and the second rail is generated **VCC2V5** from the supply chain.

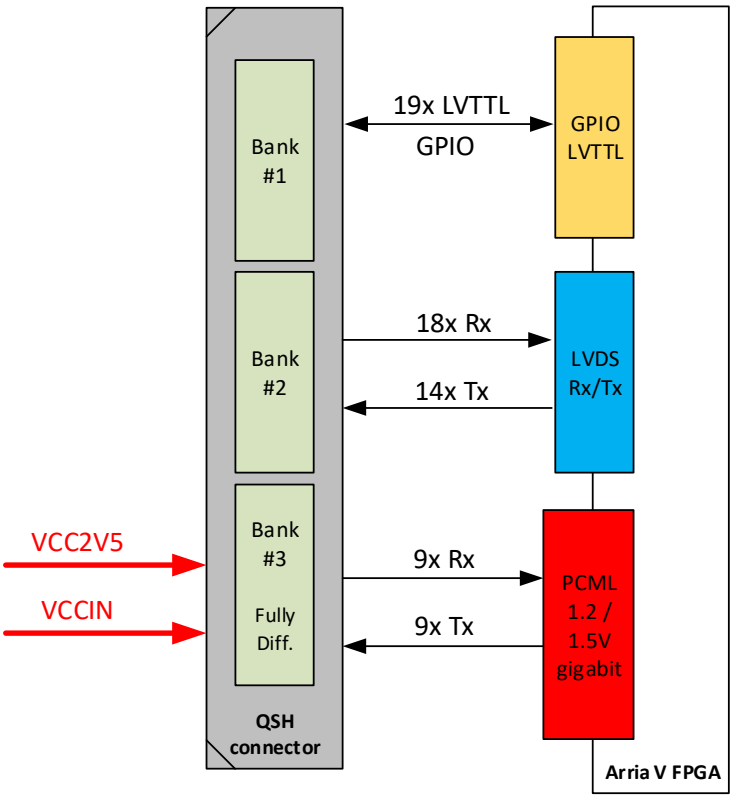


Fig. 40 Daughter board HSMC connector

One of the important PCB layout issues is the length-tuning of the sensitive signals.

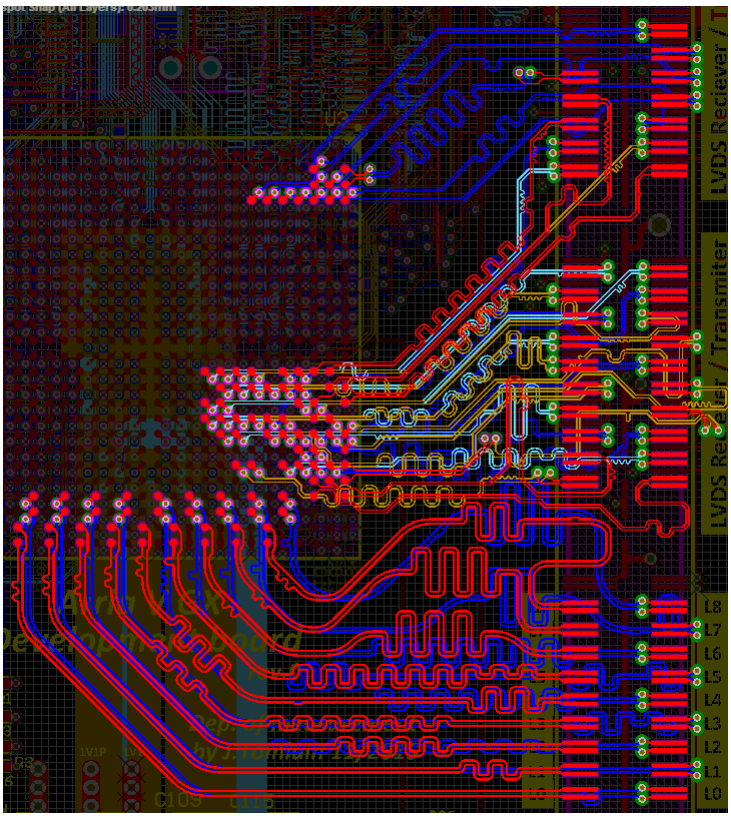


Fig. 41 Length tuning of the daughter board connection

There are basically two types of the length-tuning:

- length-tuning of the positive and negative signal inside one differential pair
- length-tuning of more differential pairs of some particular signal group

The design of the FRA FPGA board includes both techniques for proper high-speed signal routing. Length-tuning tools were used inside the Altium Designer software with the precise rules definition for such groups. The rules were set according to the maximum speed used on specific lines:

- LVDS group tolerance was set to 0.5 mm
- Gigabit group tolerance was set to 0.127 mm

These values are basically selected as higher demanding criteria from [36]. As the USB 2.0 interface uses 480 Mbit/s signaling and used LVDS pairs in the FRA meter will work with maximum speed below 400 Mbit/s (quad-data-rate signaling of 100 Mbit/s data), and the USB 2.0 has a maximum difference of lines 50 mils (1.27 mm), the designed criteria of 0.5 mm are well selected. In the case of gigabit connection, the criteria were inspired by the HDMI/USB 3.0 interface. The skew of the lines for these interfaces is maximum of 5 mils (0.127 mm) according to the same description [36]. These interfaces have a higher speed than 1.25 Gbps, so used criteria of the same 0.127 mm is more than enough in this case. The final layout of the routed groups is shown in Fig. 41.

The final connection of all interfaces to the FPGA device uses all gigabit resources of the selected FPGA chip on the special transceiver IO bank (2x 9 pairs). The LVDS and LVTTL signals occupy free signals on the following banks:

- **BANK 5A** - 16x GPIO 2.5 LVTTL
- **BANK 6A** - 3x GPIO 2.5 LVTTL
- **BANK 7A** - 4x RX pair, 7x TX pair

- **BANK 8A** - 6x RX pair, 5x TX pair
- **BANK 8D** - 8x RX pair, 2x TX pair

5.10 Component layout

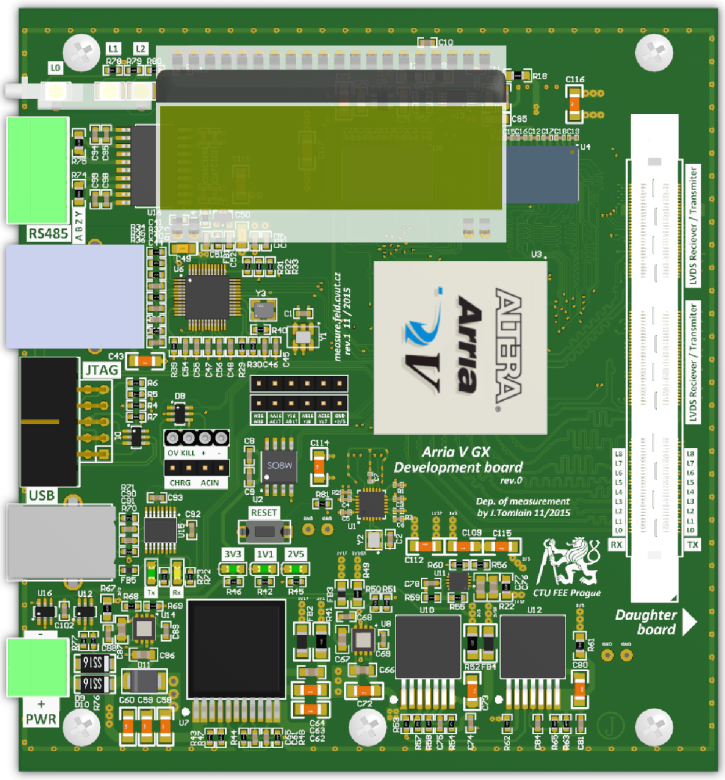


Fig. 42 Final design of the FPGA board

6 Excitation board design

The basic proposal of the excitation board was discussed in 4.2. This chapter will describe the design of the excitation board a little more in detail. This unit covers two physically distinct parts:

- 2x Output / Excitation
- 1x Input / Sensing

The basic block diagram is shown in Fig. 43. To get the main paramaters of the excitation board, the summarization of the input/output parameters are as follows:

- 2 input channels with amplitude range 30 Vpp
- 1 excitation output with amplitude range 30 Vpp
- output power up to 1 A

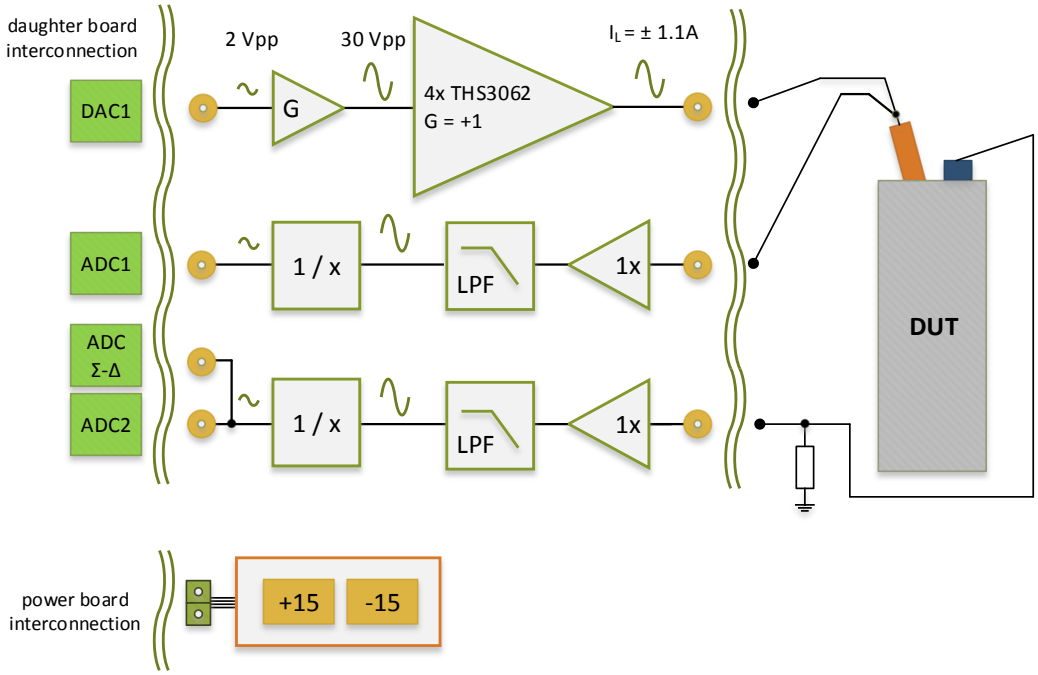


Fig. 43 Proposed design of excitation FRA board

6.1 Excitation

The criteria for this board were analyzed from the state-of-art instruments mentioned in 2.2.4 and from the HW requirements stated in the 4. There are few calculations made to support of proposed parameters of the excitation board. In addition to this also the standby mode must be implemented. This is mainly due to the power saving of the high-speed amplifiers when the measurement is not running. As the daughterboard supports the connection of the high-speed ADC as well as the connection to the low-speed sigma-delta ADC, the excitation board should be able to interconnect both of them. First of all, the most important subpart is the output amplification. Based on this, the analog signal preparation should be designed. To remind the limiting and specific parameters are:

- single-tone signal (one frequency sinusoidal signal)
- frequency range higher than 100 MHz but lower than 200 MHz
- output power and amplitude swing as mentioned before (max. 1 A and 30 Vpp)

Based on these parameters the Texas Instrument THS3062D high voltage (documented in [37]), high output current component was chosen. This amplifier are available in dual version in the SOIC8 package. In Tab. 8 is the brief summarization of its key its key paramaters for our design. To use the best parameters of this amplifier, the

Parameter	Value	Unit
Unity gain bandwidth	300	MHz
Output current / channel	± 145	mA
Power supply range	± 15	V
Common-mode input range	± 13.1	V
Voltage output swing	± 12.5 - ± 13.5	V

Tab. 8 Key THS3062 parameters

gain $G = +1$ was selected. With this setting, the slew rate of the amplifier is the highest. One of the requirements is the output voltage swing of 30 Vpp. Unfortunately, this parameter was adjusted to the lower value of approximately 25 Vpp, due to the powering circuitry and typical amplifier market availability. Most of the amplifiers are $\pm 15\ V$ supplied, and also, the accupack board is generating this voltage output. To satisfy the output power, the eight amplifiers should be used together. The next aspect is driving the capacitive load, which is always present in the DUT in the high-voltage diagnostics. This technique is described in [37] in the section *driving a capacitive load*.

To prepare the input signal for the THS3062 amplifiers the pre-amplification must take place. The output signal from the DAC and the maximum acceptance value for the end-stage are shown in Eq. 13.

$$\begin{aligned} VO_{DAC} &= 2\,Vpp \\ VI_{THS} &= 26.6\,Vpp \end{aligned} \tag{13}$$

From this, the gain of the stage should be +12.5 x (the output swing limited to 25 Vpp to keep from the documented limits). This stage should fulfil the same AC parameters as the output stage. The block diagram of the output is shown in Fig. 44. The first

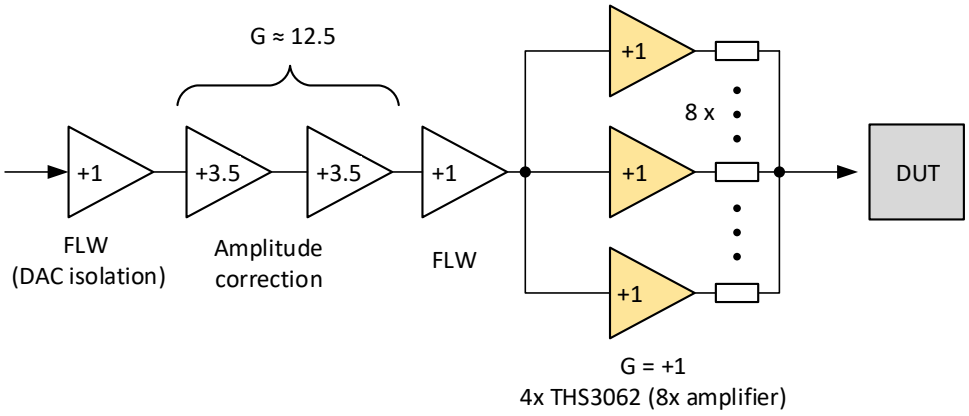


Fig. 44 Excitation board output

block is the follower to isolate the DAC output circuitry, and then the amplification is divided between two amplifiers for easier implementation and satisfaction of the AC parameters. Afterward, an additional follower has connected in-between the amplitude correction and the power output stage. This complete section is implemented with dual amplifier LM6172 from Texas Instruments ([38]). Its basic parameters are in Tab. 9. The output voltage swing is the same as the input voltage swing of the THS3062,

Parameter	Value	Unit
Unity gain bandwidth	100	MHz
Power supply range	± 15	V
Voltage output swing	± 12.5	V

Tab. 9 Key LM6172 parameters

which is required. The frequency span is not as high as it could be implemented, but this version of the amplifier was implemented in the prototype units just to prove the concept. Its working frequency range on used gains is lower than 100 MHz, so the output signal amplitude drops. This possible issue could be neglected by two facts. As we know from the previous theoretical parts, the larger the frequency is, the lower the DUT impedance is. According to the Eq. 10 from 4, it is obvious that measured sensed voltage is larger when the impedance is lower. Impedance is lower in the higher frequency range. This is the first fact, which helps the amplitude loss in the excitation. The second behavior is that the FRA instrument actually measures both voltages (input to the DUT and also the sensed voltage. In other words, any amplitude imperfection in the excitation output voltage is measured and passed to the calculations.

6.2 Sensing

This part is responsible for the input signal processing. As the input signal amplitude could be as high as the excitation voltage the input range must again satisfy the rating about from 25 Vpp to 30 Vpp. The same operational amplifier was used (LM6172). The block diagram of this stage is in Fig. 45. The input signals are protected with transient voltage suppressors with a nominal value of $\pm 18\ V$. To prevent problems with sensing and to keep the input impedance at high levels, the follower block is

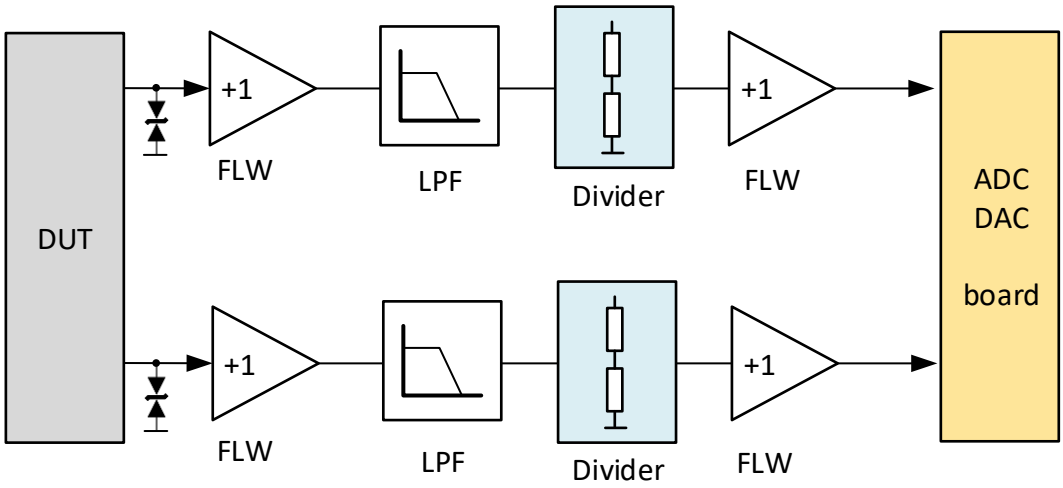


Fig. 45 Excitation board input

connected in the first place. After this operational amplifier block, the low-pass filter block is integrated. To accommodate the input voltage range of the ADC, the resistor divider is implemented prior to the last follower block. The chosen ratio is in :

$$DivRatio = \frac{1\,k\Omega}{1\,k\Omega + 15\,k\Omega} = 0.0625 \tag{14}$$

The final follower is designed to maintain good excitation parameters (in terms of output impedance) to the input amplifiers of the daughter board. In the Fig. 46 is the complete 3D model of the designed HW board. On the left bottom corner is the connection to the accupack board. (see Fig. 52). The right edge is occupied by the input BNC connectors and output BNC excitation port. There are three SMB jack-type connectors on the upper part of the right corner. These connectors fit directly to the analog daughterboard, where are mating-type SMB plug connectors. The connection concept is shown in Fig. 47. The large area above the THS3062 array is prepared for a possible mounting of the heatsink on the top of these amplifiers.

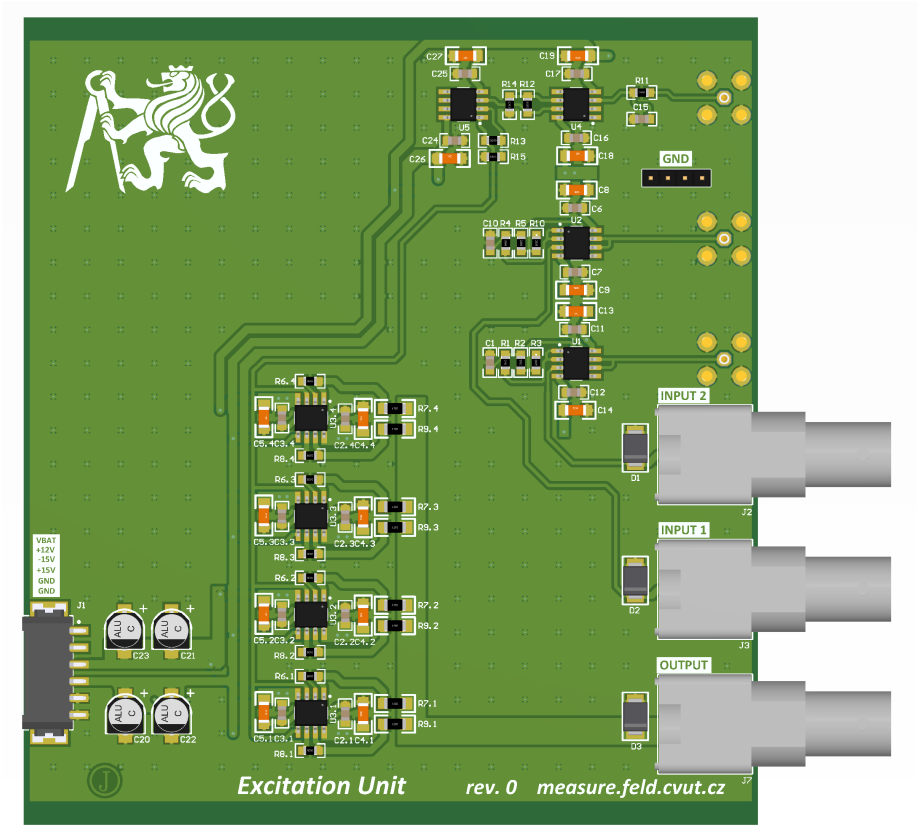


Fig. 46 Final design of the excitation board

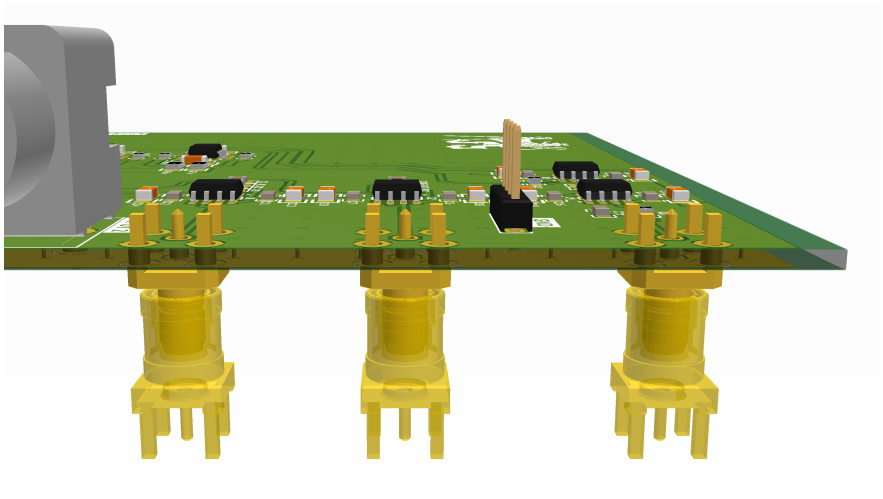


Fig. 47 Direct cable-less interconnection between daughter board and excitation board

7 Accumulator pack design

A brief introduction to the design of the powering stage was done. 4.6 and 5.6. From the main requirements on the device, the portable was chosen mainly due to the convenient usage in the off-laboratory environment. In addition to this, no other instrument mentioned in 2.2.4 does not offer direct portable usage in one enclosure without any special external power source like a battery pack, etc.

7.1 Battery selection criteria

Battery type selection for the design of the accupack is one of the most important steps which has to be done prior to the implementation of the particular battery type. Summary of the main features of the device in terms of the operation procedure is as follows:

- 6 to 8 hours of operation with an approximately real measurement time of 20 %
- no permanent runtime
- typical operation temperature above 0 °C
- compact dimensions
- maximum voltage swing needed in device +15 V / -15 V

The first point of this requirement determines the needed capacity of the accumulator bank. Based on the measurement of the device, the standby power consumption of the FPGA board with the daughterboard and the power consumption based with all data-converter switched on are as follows. This measurement was done with the Keysight 34465A instrument on the shunt resistor of value 0.1 Ω. The results are in Eq. 15. This measurement covered the current from the **VCCIN** port to the FPGA board and then to the daughter board according to the. 5.6.

$$\begin{aligned} I_{FPGA\_STDBY} &= 260\,mA \\ I_{FPGA\_RUN} &= 400\,mA \end{aligned} \tag{15}$$

Based on the defined criteria the averaged consumption of the digital core parts could be calculated as follows:

$$0.8 \cdot I_{FPGA\_STDBY} + 0.2 \cdot I_{FPGA\_RUN} = 288\,mA \tag{16}$$

The no-load current consumption of the DC/DC converter used for the digital part (THL 25-2412WI) is an additional 85 mA which must the added to the calculated consumption in Eq. 16. As the battery voltage is one of the variables, current values should be converted to the power of better calculation. All DC/DC converters nowadays offer at least 85 % efficiency, so the calculation with the power in Watts should not be an issue. The measurement of the currents made was processed with a voltage of 12 V. The power could be stated as follows:

$$P_1 = U \cdot I = 12\,(0.288 + 0.085) = 4.48\,W \tag{17}$$

In other words, for an 8 hours operation of the digital part only, the battery (12 V nominal) of the approximate capacity of 3.0 Ah should be enough. However, the excitation board consumption will be critical, and this power must be calculated as well. Device-under-test is not defined, so the calculation must include the maximum possible values. According to the brief description in 5.6 the used DC/DC converter for analog excitation has a maximum rating of 40 Watts. This power is used for 20 % of the time, so the effective load is in the form of 8 W. This assumption will result in:

$$P_T = P_1 + 0.2 \cdot 40 = 12.48\,W \tag{18}$$

This solution points to the battery (12 V nominal) with a minimum capacity of approximately 8.5 Ah. Fortunately, much less power is needed in the real world. The real impedance graphs of already tested DUT stated, for instance in 13.1 shows that average impedance in the test is around 1000 Ohms or even more. If the excitation voltage is 30 Vpp (ca 10 Vrms), the real power needed is one hundred times less on average. To be more critical, this assumption will be applied only ten times less, so the final power needed in average by the excitation unit is 0.8 W (comparing the 8 W). The final consumption then could be recalculated in the following manner:

$$P_T = P_1 + \frac{0.2 \cdot 40}{10} = 5.28\,W \tag{19}$$

Considering the maximum time limit of the operation, 8 hours, the final capacity should be 42.24 Wh.

The situation is also positive about the service time and the typical using style of the portable equipment. Typically the testing time is one working day, and then the equipment could be recharged for the next measuring cycle. This is an advantage for some chemistries of the batteries. On the other hand, there are, typically, lead-acid batteries, which are suitable for float charging. Float charging is a mechanism with the charger permanently connected, while the battery power is just covering blackouts. Standard Ni-Cd and Ni-MH cells were omitted due to the significant problems with memory effect in these chemistries and also standardized low-voltage per cell. Combining a large number of such cells must be protected against the wrong balanced of the cells. Lead-acid and Li-Ion technologies were picked as final candidates prior to design. The main parameters are summarized below in Tab. 10 according to [39].

Parameter	**Lead-Acid**	**Li-Ion**
Energy density	35-40 Wh/kg	150-180 Wh/kg
Temperature range	-30 °C to +40 °C	-20 °C to +50 °C
Charing cycles	1500-5000	1000-5000
Charger complexity	Easy	Complex
Price	200 USD / kWh	800 USD / kWh

Tab. 10 Lead-Acid, Li-Ion chemistry comparison

As this FRA instrument should be relatively easy to carry the energy density points to the Li-Ion technology. This parameter is 4 to 5 times better compared to the Lead-Acid technology. Older technology is then more suitable for negative temperature installation. The charging cycles are almost the same, this fact will probably be manufacturer-depended, and also, it will change over the application range. The main

disadvantages of the Li-Ion technology are the price of comparable quality products and the charging process complexity. While the Lead-Acid technology withstands more rough operations, the Li-Ion technology is more sensitive to external treatment. For the FRA measurement system, the Li-Ion technology was selected. The charging issue was solved directly inside the instrument with the built-in charger to overcome the user maintenance attention.

The classical Li-Ion cell has a nominal voltage of 3.7 V with a maximum voltage of 4.2 V. There are several types of battery cases of this chemistry. The most common and most spread packaging type is the 18650 cell type (shown in Fig.48), which could be found in portable computers, battery-operated tools, industrial applications, and electric vehicles (EV). This packaging offers the highest energy density, and several professional manufacturers (Panasonic, Samsung, etc.) offers various capacities and types of this cell type. The common capacity range is from 1500 mAh up to 3600 mAh. Due to the used DC/DC converters, the input voltage range should be from 9 V up to

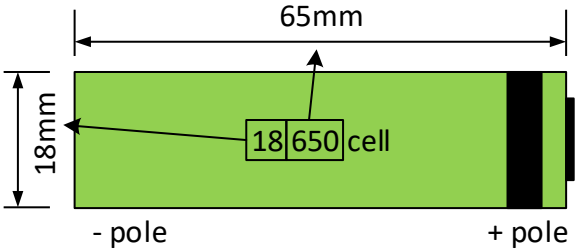


Fig. 48 Dimension of the 18650 cell **(scale 1:1)**

18 V. Panasonic NCR18650B offers 3400 mAh [40] in price less than 10 EUR a cell in single quantities. Several independent tests proved that the capacity in various loads is about 3200 mAh and more (test sources are, in most cases, web pages of hardware projects). Based on the capacity and voltage, the nominal watthours value is 12.6 Wh per one cell. The requirements are 42.24 Wh. Therefore, four cells will cover the complete consumption of the device with about 15 % reserve. The final organization of the cell could not be chosen freely due to the DC/DC convertor's topology. The minimum voltage is 9 V, so the 4s (four serial) connection was implemented with a nominal voltage of 14.8 V and maximum voltage 16.8 V. Assuming the non-fatal end voltage of the cell at a higher value, for instance, 3.3 V (0.5 V higher than the specification in [40]), the resulting minimum voltage of about 13.0 V is fully acceptable.

7.2 Li-Ion charging process theory

Compared to the other types of chemistries, the Li-Ion technology needs a special charging process which typically consists of the following three stages acc. to [41], and [42].

- **Precondition phase**
  In this phase, the charger circuitry monitors the cell voltage and does not enable the maximum setpoint current to flow inside the battery. The limit of this monitoring current is typically about 10 % of the maximum current. As the voltage on

the cell rising the preconditioning phase will end. If the voltage does not rise in the timer period, most of the charger controllers will end up with failure detected.

- **Constant current phase CC**
  During this phase, more than 80 % of the battery capacity is charged. During this phase, the charger continually pushes the maximum (according to the setting) current inside the battery cells. In the background, the temperature and the total charge time are monitored. If any of those are exceeded, the limits charger should end up with an error. The main monitoring value is the cell voltage. Once the voltage is raised, the maximum cell voltage (in Li-Ion chemistry typically 4.2 V), this phase ends and continues to the last phase.
- **Constant voltage phase CV**
  The last phase will cover the full charge capacity of the cell. The difference between the previous stage is in the constant voltage mode instead of current. The regulator sets the maximum voltage and starts to monitor the consumed current. Typically the threshold is set to 10 % of the maximum current. When the current drops below this limit, the charging process is finished.

Graphically the charging stages are shown in Fig. 49 from the MCP73843 single-cell linear charger chip.

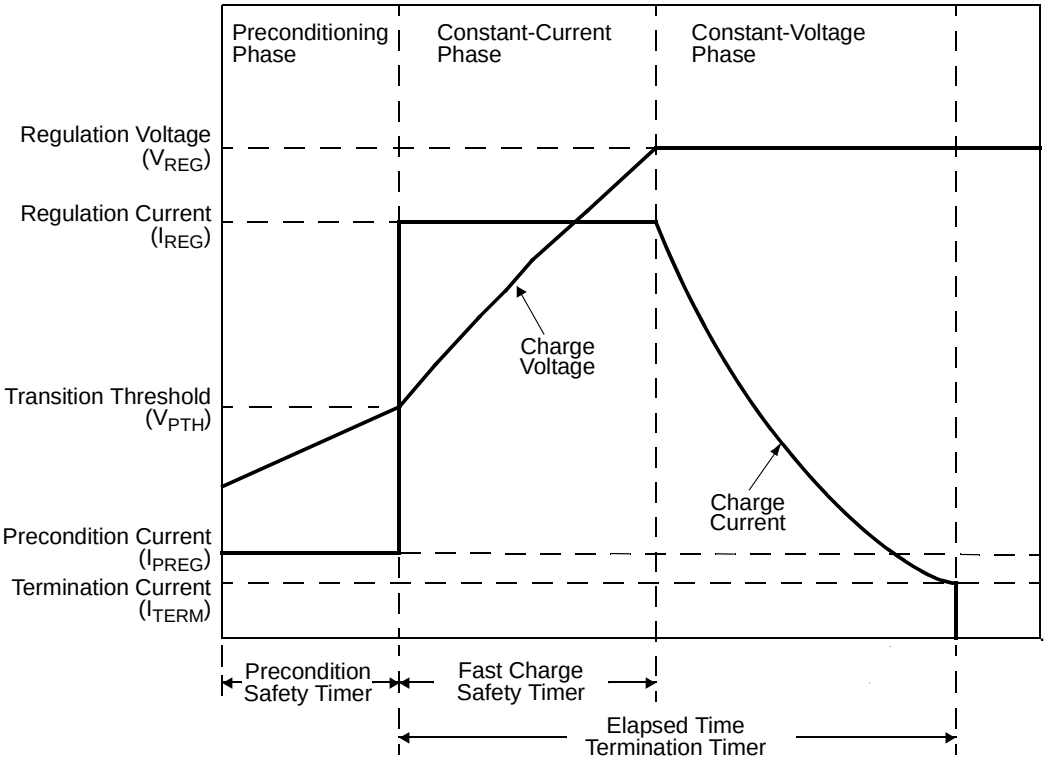


Fig. 49 Li-Ion charging stages

Basically there are two types of ready-made charging controllers. These two groups differs on the regulator topology used.

- **linear charger** - uses linear regulator
- **switched charger** - uses some DC/DC topology, step-up/step-down/combined

The first group are cheap and could become very useful in single-cell application with smaller cell capacities and when the input voltage is close to the target maximum

cell voltage. The main problem is the heat dissipation of such a charger chip. FRA instrument case uses four cells in series and a capacity of 3.4 Ah. Typically the charging current should be selected in the range from 0.5 C to 1.0 C. The **C** is the nominal capacity of the particular battery. The linear charger dissipation is then calculated as in Eq. 20. The values were selected in the most acceptable way: minimum value of maximum current limit, drop-out of 1.2 V at the input voltage, and the discharged voltage of the cell at the value 3.25 V per cell. This results in 8.5 W of the dissipated power. This value is quite high, and its cooling with compact heatsinks is almost unable.

$$P_{diss} = (V_{IN} - V_{disch}) \cdot I_{max} = (18 - 13) \cdot (0.5 \cdot 3.4) = 8.5\,W \tag{20}$$

In contrast, these linear regulators are ideal for classical USB-based charging. Imagine a 2000 mAh battery and linear charger from a 5.0 V USB port. Its critical dissipation is only as in Eq. 21. This value could be handled by common PCB heatsinks.

$$P_{diss} = (V_{IN} - V_{disch}) \cdot I_{max} = (5 - 3.25) \cdot (0.5 \cdot 2.0) = 1.75\,W \tag{21}$$

FRA instruments accupack must be designed with the switched charger circuit. In addition to the controllable heat dissipation, the operator is not limited to the precise type of the input charging voltage. Finally, the LTM8062A from Analog Devices (formerly Linear Technologies) was selected as the ideal part for such an accumulator bank. Summary of critical parameters is following [41]. The used package shown in Fig. 50 encapsulates all components, so only a few external resistor-based settings were implemented. The current limit was set to the maximum of this part (2 A), so the

Fig. 50 LTM8062A LGA77 package

Parameter	**Value**
Input voltage:	max. 32 V
Maximum battery voltage:	18.8 V
Charge limit	2 A
Efficiency at 18.8 V / 1.5 A	92 %
Package	LGA77

Tab. 11 LTM8062A basic parameters

maximum power which goes into batteries could be during the starting phase of the constant-current mode. In this case, this voltage is 3.0 V, so the output power is a maximum of 6 W. The efficiency is around 90 %, so the total heat dissipated power should be less than 1 W.

7.3 Design of the accupack board

The 3D model of the final design is shown in Fig. 52. The block diagram is shown in Fig. 51. The main supply is, as mentioned, four serially connected 18650 cells. Their charging process is controlled via LTM8062A from the external power supply adaptor (nominally 24 V). The device then implements a push-button controller LTC2950. This device is constantly connected to the battery cells and monitors the state of the external push-button. When the button is pressed for a specific period of time, the device is switched on via the P MOSFET switch **T1**. The switching-off process is similar. The

battery is connected to two DC/DC converters. The first one is the TRACO THL25 series which produces stable 12 V for FPGA and the daughterboard. This supply is always accessible when the accupack is in the ON state. The second DC/DC Traco TEN40 converter supplies the analog excitation board with $\pm 15\ V$. This DC/DC is entering shutdown mode based on the standby mode. This is done by the **T2** transistor on the accupack board. The one important thing is the voltage monitoring of the battery pack. To achieve the under-voltage protection and automatic switch-down, the simple SAR analog-to-digital converter was designed on the accumulator pack board.

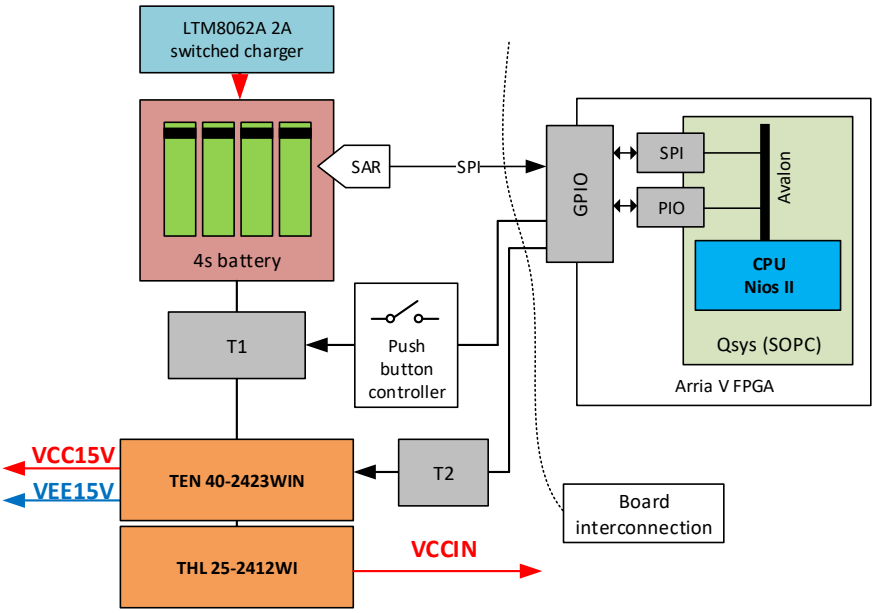


Fig. 51 Block diagram of designed Accupack

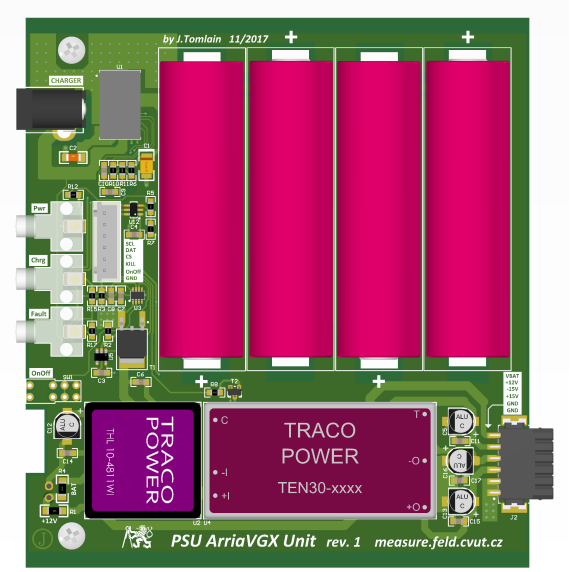


Fig. 52 Final design of the accumulator pack board

8 Instrument enclosure

Extruded aluminum case form was picked as a universal solution for the whole measuring system. The mechanical layout in horizontal guides for particular boards will help in robustness and mechanical durability. The proposed design is in Fig.53. At the

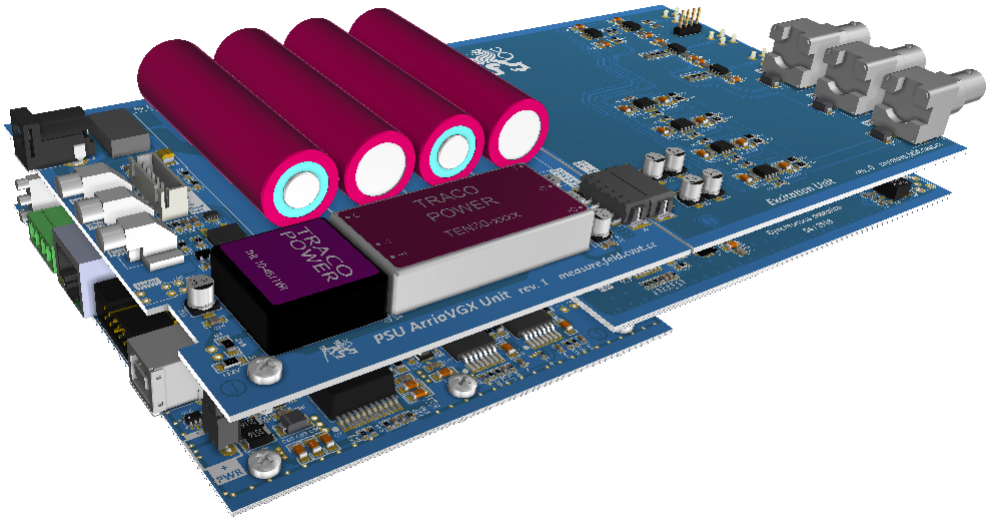


Fig. 53 Developed design of the instrumentation

Fig. 54 Picture of the front side of the instrument

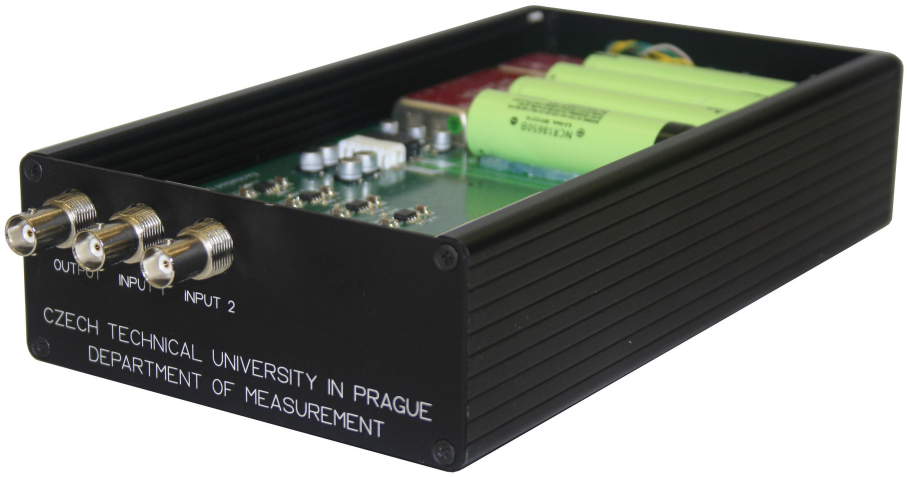


Fig. 55 Picture of the backside of the instrument

bottom, the FPGA board together with the analog daughterboard are fitted. Above the digital board, the power board proposed in 5.6 will be installed, and next to this board, the excitation board above the daughter board will be located. Finally, above the analog daughter board, the excitation part will be mounted. The final used enclosure is the aluminum extruded profile enclosure from Hammond, Canada. The precise type is the 1455Q2201BK. The mechanical fixing of all boards is done with the metal endplates, which are milled and labeled with the laser. The final device without top cover is shown in Fig. 54 and Fig. 55.

9 ADC / DAC daughter board

This hardware module was designed in the team by Mr. O. Teren, and the complete detailed description can be found in his Ph.D. thesis. For required background, this work will cover just a very brief description of the board.

The analog conversion front-end board connects via an HSMC connector. The high-speed ADC part consists of ADS42LB69 from Texas Instruments, which provides 16-bit conversion at a maximum rate of 250 MSPs. According to [43] the connection with the FPGA is made via LVDS DDR (double date rate) or QDR (quad data rate) interleaving mode. Both possibilities could be used due to the versatile PCB design. The second low-speed precise converter is ADS1263, which has Σ-Δ architecture with a maximum data rate of 38.4 kSPs and 32 bit output word. The high-speed ADC is located in the

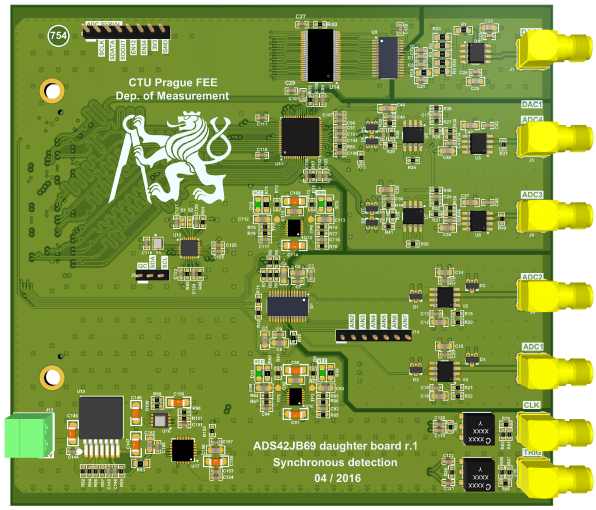


Fig. 56 3D model of the daughter board

top part of the board, while the low-speed converter is next to it below. Analog inputs are prepared for a signal in the range up to 2 Vpp. Signal conditioning is prepared for both DC coupling via an operational amplifier and a fully differential output amplifier.

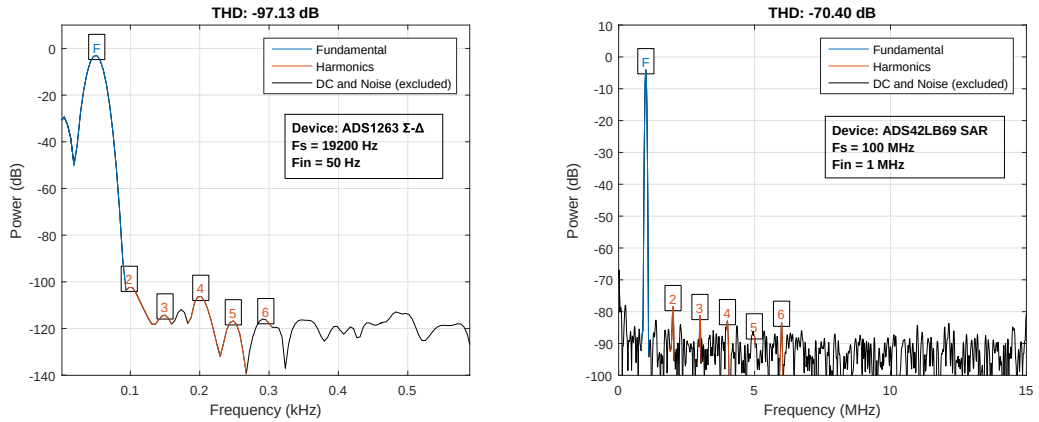
Signal generation block builds on the DAC904EG high-speed dual-channel digital to analog converter with a maximum rate of 165 MSPs. Data input is done with CMOS parallel bus with voltage translation from FPGA's 2.5 V logic to the 3.3 V, which is the operational supply of the DAC circuit. The output voltage is generated by the output amplifier, and the output voltage dynamics are again 2 Vpp. The clocking of all parts is also implemented with the Si5338A generator. Powering of all subparts is done by its own powering structure. It consists of DC/DC converters and low-noise linear regulators.

9.1 System preliminary tests

To basic test the characteristics and features of the module, during the prototyping phase, a few simple tests were made.

9.1.1 High speed and Σ-Δ AD conversion test

Hardware acts like a local-are-network (LAN) node and reacts to the TCP communication port, which is available for data exchange and control commands. Data throughput via TCP connection is about 10 Mbit/s. High-speed data conversion is done inside VHDL, and the user is able to acquire 16-bit wide samples from dual-channel input in $f_s = 100$ MSPs. A sampling of the 1 MHz sine wave signal with $f_s = 100$ MHz has been done as one of the preliminary tests. THD values of the obtained data are shown in Fig. 57b. The low-speed AD conversion is done with a specially developed VHDL SPI driver. This input has been tested by 50 Hz sine wave signal with $f_s = 19.2$ kHz, and the result is in Fig. 57a.



(a) Σ-Δ ADS1263 **(b)** High-speed ADS42LB69

Fig. 57 THD estimations results of both converter types

9.1.2 Noise and harmonic distortion analysis

The next hardware verification test was aimed at the complete noise and harmonic distortion analysis. As the SFRA (swept FRA) is working with a single excitation frequency at one time, the analog to digital conversion as well as the signal generation way should be tested to verify that all hardware components in the daughterboard and the excitation board are suitable for such a task.

First of all, the noise analysis of the high-speed digitalization channels was done using converter ADS42LB69 according to. [43] should have an effective number of bits (ENOB) equal to 11.76 bits with the reference voltage 2 Vpp and sampling frequency 170 MSPs. But this value describes only the single ADC chip without any amplification circuit and signal conditioning. In other words, the real ENOB should be ideally measured with the complete board setup. Following three different connections were used to measure characteristics. The connection is shown in Fig. 58. The list of tests are as follows:

- **I.** shorted input to measure effective resolution and/or ENOB
- **II.** excitation with low-distortion generator DS360 to measure THD

- **III.** self-excitation with on-board analog output

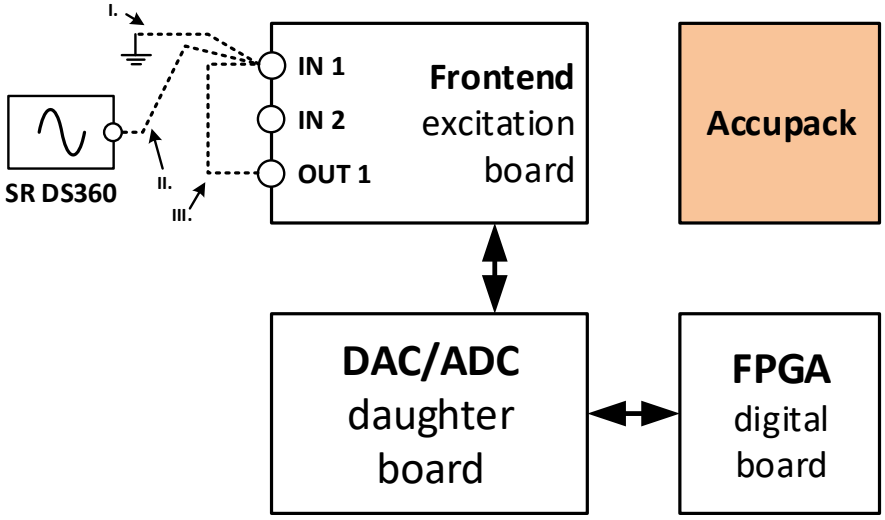


Fig. 58 Connection for noise and THD tests

The sampling frequency was set to the normal working frequency 100 MHz as the usual operation of the device. The data was directly sampled with the FPGA board and sent as raw LSB data to the computer via Ethernet port. The data portion was set to the 4096 samples window.

Noise tests

For the noise evaluation, the captured data plot is shown in Fig. 58. Calculation of the effective resolution and the ENOB was done as follows according to. [44].

$$ER(bits) = \log_2 \frac{fullscale\ range}{rms\,noise} \tag{22}$$

$$ENOB(bits) = \log_2 \frac{fullscale\ range}{rms\,noise \cdot \sqrt{12}} \tag{23}$$

$$NFR(bits) = \log_2 \frac{fullscale\ range}{pp\ noise} \tag{24}$$

The *fullscale range* is always considered as 65536 (16-bit converter), while the *rmsnoise* is root mean square value of the captured data and *pp noise* is the peak-to-peak noise from the captured data. Results are calculated by the above mentioned equations:

- ER (effective resolution) = 12.09 bit
- ENOB (effective number of bits) = 10.29 bit
- NFR (noise-free resolution) = 9.50 bit

The ENOB of the specification of the converter is reduced by 1 bit, which is mainly due to the amplification circuits together with the signal and PCB routes path.

THD external excitation

The second experiment uses Stanford research systems low distortion function generator DS360. Its maximum working frequency is 200 kHz, with the worst THD value specified as -68 dB. For the calculation of the THD, the Matlab R2015b was used. This

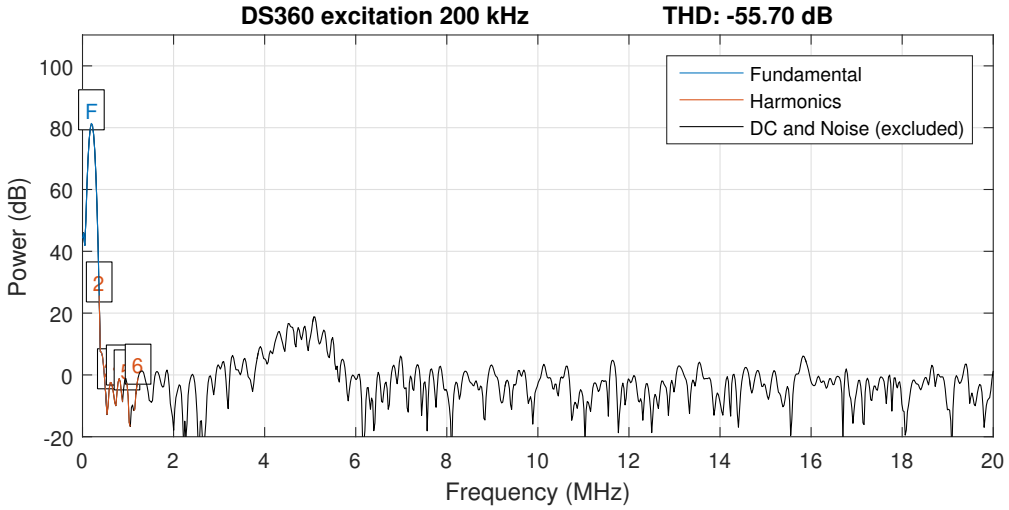


Fig. 59 THD DS360 excitation 200 kHz

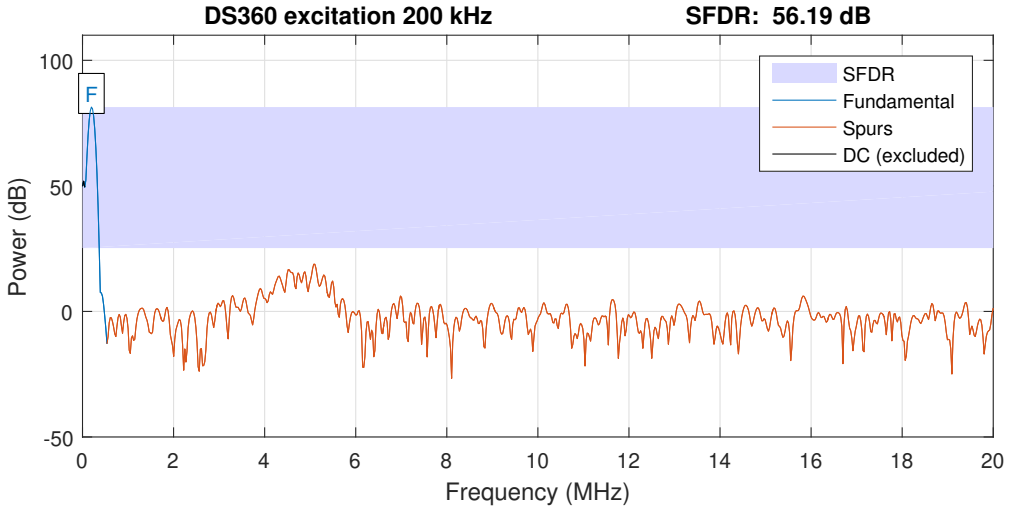


Fig. 60 SFDR DS360 excitation 200 kHz

software offers direct THD, SFDR (spurious free dynamic range) and other parameters calculations. The THD and SFDR equations for calculation are as follows (according to [45]):

$$THD(db) = 20 \cdot \log\left(\frac{\sqrt{V_2^2 + V_3^2 + ... + V_x^2}}{V_1}\right) \tag{25}$$

$$SFDR(dB) = fundamental(dB) - largestspur(dB) \tag{26}$$

where the V_1 is the power of the fundamental and V_2 up to V_x are higher harmonics. The largest spur is the frequency with the largest magnitude after the fundamental one, as shown in Fig. 60.

THD self-excitation

Not only is the analog-to-digital way is an important part of the whole device but also parameters of the signal generation part should be tested. As the signal generator is done as DDS (direct-digital-synthesis), the final frequency spectrum could be distorted. As the results are numerically below the results of the ADC itself, it can be assumed

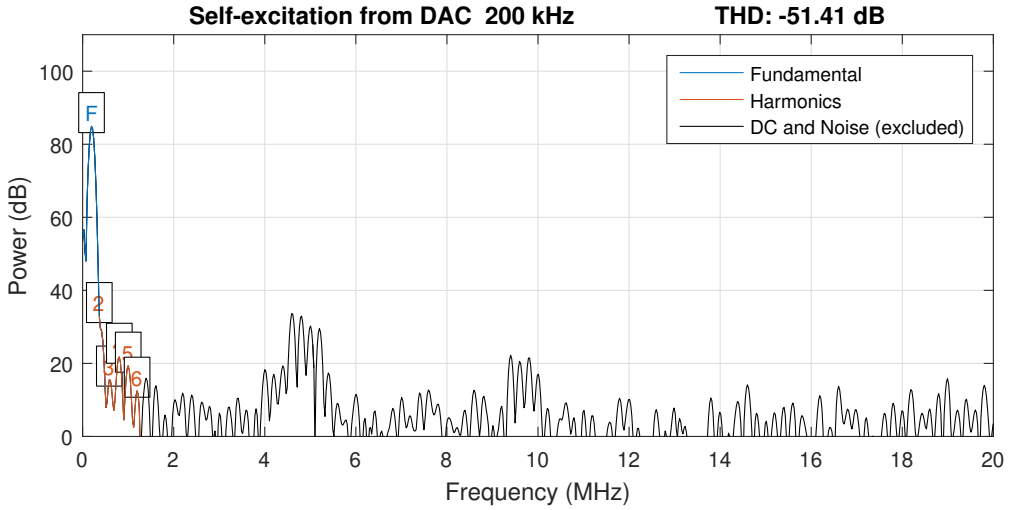


Fig. 61 THD Self excitation 200 kHz

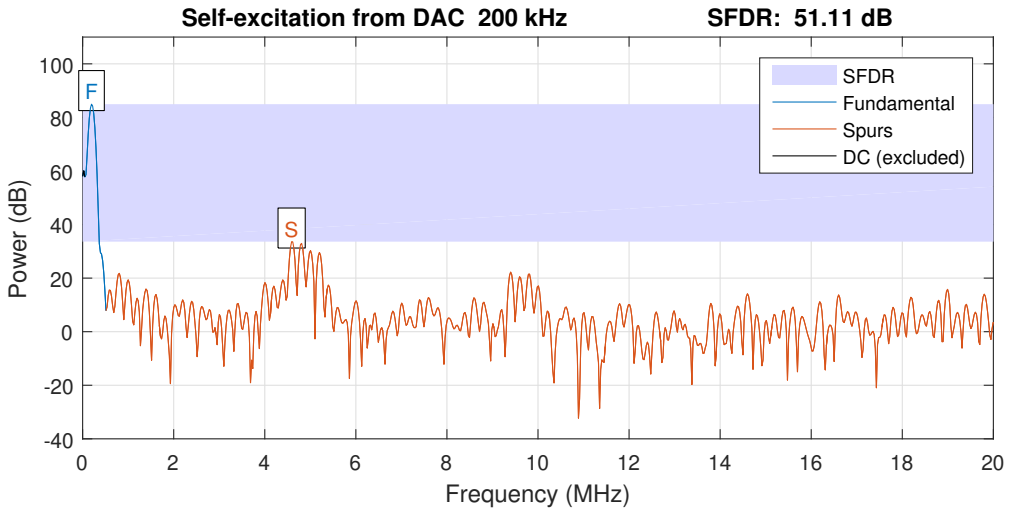


Fig. 62 SFDR Self-excitation 200 kHz

that the final THD of the output DAC generated sine waves are around -51 dB. A spurious spectrum in the range of 5 MHz is probably produced by the power supplies and/or digital core parts.

9.1.3 FRA measurement

Frequency response measurement was analyzed and tested in a simple connection, where the DUT was substituted by a simple RC low-pass filter. Connection is shown in Fig. 63. The cut-off frequency of the circuit was approximately 900 Hz. The used capacitor was 100 nF and 1800 Ω resistor. Starting frequency was 100 Hz, and 2 MHz

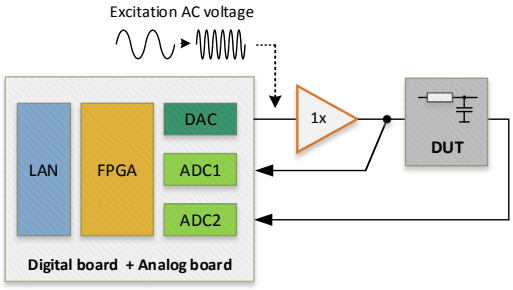


Fig. 63 Frequency response test circuit

was the last used value. Data has been transferred via LAN to the host. Complete VHDL logic behind this test is shown in Fig. 64. NIOS processor controls the output frequency by a parallel output port, which is connected to the direct digital synthesis (DDS) block. Output code is then used for a sine wave generation via the ROM lookup table. Input signals from ADC are deserialized, and the mean value is estimated from

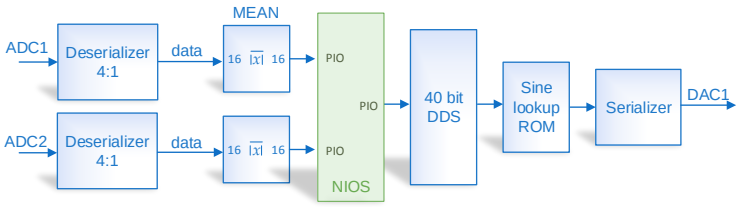


Fig. 64 Implemented core for FRA tests

the input data stream. NIOS processor then calculates a ratio between ADC1 and ADC2 input for magnitude determination. FRA of the experimental DUT is shown in Fig. 65. The measured characteristics are very close to the ideal magnitude plot of such RC filter (measured with oscilloscope and generator). The difference in the higher frequency range could be caused by non-ideal connections or inaccurate analog to digital chain calibration.

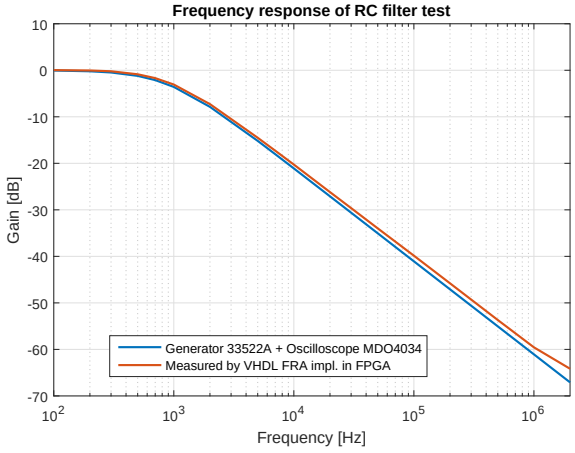


Fig. 65 Frequency response of RC filter test

10 Software package

This chapter will detailly describe the software development, which has been done on the FRA instrument during its design and testing phase. Software of the whole instrument consists of several types of subsystems, which are programmed in a special language or designed in a graphical development environment. Basically, the FRA instrument and its operation rely on the following software parts:

- logic FPGA blocks created and programmed in the VHDL language
- schematic interconnections between FPGA blocks
- design of the SoC (System-on-the-chip) for FPGA
- firmware for the soft-core microprocessor inside the SoC (Nios II Fast)
- host computer software for visualization and control

In detail, this chapter will cover the first four disciplines. The host computer software will be described very shortly. Before the detailed FPGA and SoC systems description, the short introduction to the theory of these systems is given below.

10.1 SoC (system-on-the-chip), soft-core

SoC technology (System on chip) is also called soft-core. In both cases, these names define purely software products and blocks that can be implemented directly on special chips by the applications from the FPGA manufacturers. This enables the usage of the preprocessed elements (pre-programmed in Verilog or VHDL) and using these blocks literally builds more sophisticated systems, ideally for your application needs. When considering the SoC system, it is an ideal candidate to implement a proprietary microprocessor system directly using HW elements on the FPGA circuit. This solution is one of the most commonly used because the sequential or combinational logic itself is not always sufficient for the overall functionality of the device. Sure, it is the majority of control applications, which can be built directly from the logical elements, but if it is necessary to use already designed sophisticated algorithms for the implementation like, for example, communication layers of industrial protocols, a microprocessor with strictly sequential principles enters the game. In addition, most of the software packages are written in languages like C / C ++. The use of SoC in the form of a microprocessor system appears to be an ideal intermediate, which provides, on the one hand, excellent conditions for the implementation of time demanding, parallel tasks that can be implemented directly in VHDL on the FPGA circuit. On the other hand, where the time is less critical but more complicated (algorithmically), it is advisable to write in the classical programming language for the processor core. However, physically a single circuit is still used, and the overall peripheral solution is still consistent. Softcore is the name used for the processor platforms that are used within the SoC for FPGA programming. It is actually the software product that carries a full description of the processor unit core type. Including major building blocks such as data or instruction

buses, interrupt system, ALU unit, etc. So the SoC system programmer can choose which soft-core processor to use in his application with respect to the performance of the selected kernel, function, or other specific features. Typically, it is possible to find their own from the individual manufacturers of FPGA circuits. These are basically recommended, soft-core processors. However, on the market, it is also possible to buy the processor cores from third parties that are universally applicable (like ARM Cortex or x8051 core). For better abstraction of the whole subsystem, the situation is shown in Fig.

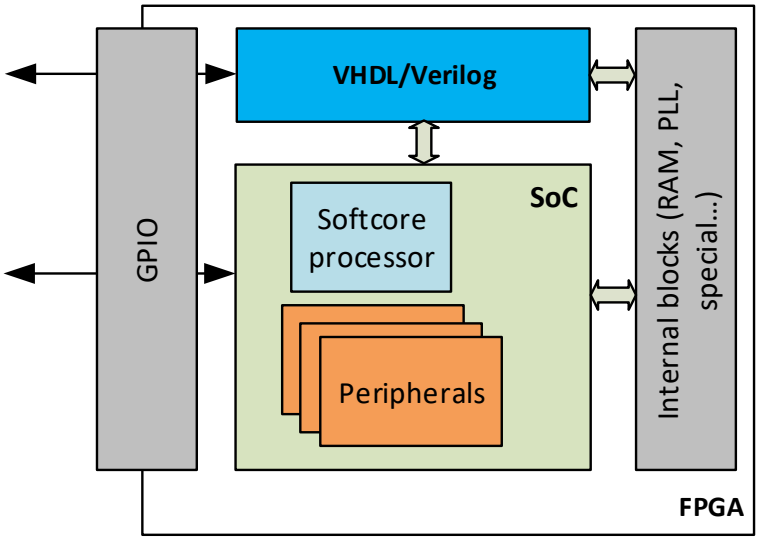


Fig. 66 Systen-on-the-chip SoC architecture overview

10.2 VHDL / schematic core of the FRA instrument

First of all, the schematic block diagram of the designed FPGA software will be discussed. All VHDL blocks will be discussed in detail for a better understanding of the software work which has been done for the FRA measurement system. The main interconnection inside FPGA consists of the following most important blocks:

- 2x de-serialization units for analog-to-digital convertor data
- 2x VHDL based lock-in-amplifier (LIA) cores
- 2x output filter block for the VHDL LIA outputs
- direct digital synthesis core (DDS) for excitation signal generation
- SoC block

The following text will describe step by step mentioned block in detail.

10.2.1 De-serialization block

Used ADC circuit ADS42LB69 uses data LVDS data interface of the sampled data. The hardware parameters of the LVDS signal is described in 5.7. To sum up the parameters of the signal, it is neccesary to summarize the parameters of the converters

data stream.

$$DataWidth = 16\,bit \qquad F_{S\,\max} = 250\,MSPs \tag{27}$$

The device supports to possible connection DDR (double-data-rate) and QDR (quad-data-rate). The basic difference in this connections are in the total bitrate speed on the single LVDS pair. For better understanding the comparison of both data streams are shown in the Fig. 67 and Fig. 68 ([43]). It can be easily calculated that the final

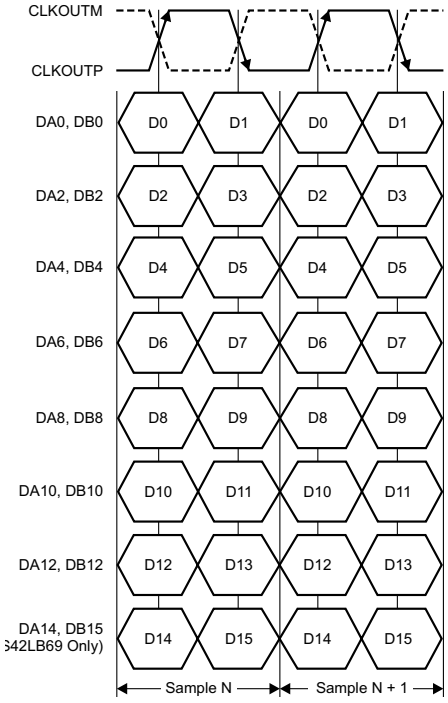


Fig. 67 DDR mode

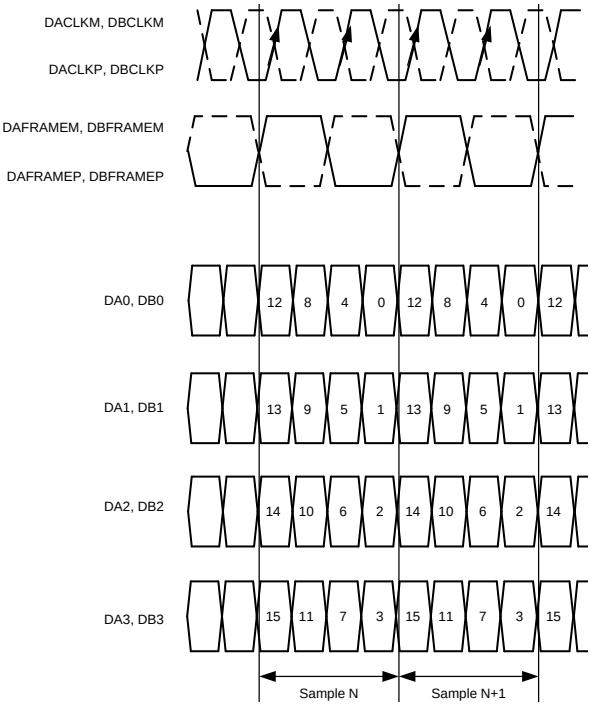


Fig. 68 QDR mode

bitrate on the single data LVDS pair is:

$$BR_{DDR} = 2 \cdot F_S \qquad BR_{QDR} = 4 \cdot F_S \tag{28}$$

FRA instrument in this software version is working maximum sampling frequency of 100 MSPs, so the final required speeds are as follows:

$$BR_{DDR} = 200\,Mbit/s \qquad BR_{QDR} = 400\,Mbit/s \tag{29}$$

As the final layout of the device includes the interconnection between two PCB boards and the total distance of tracks from the ADC to the FPGA is about 11 cm with the HSMC connection, the final FPGA software is implemented the DDR variant. This solution is even more suitable for future speed upgrades as it is always half of the QDR mode. According to the 5.9, the minimal number of LVDS RX pairs needed is 8 lanes for each data bus plus one clock lane. The total amount of 17 data lanes (34 physical connections). The daughterboard connection supports a maximum of 18 data RX lanes, so the DDR mode is fully compatible.

A De-serialization circuit for the DDR mode could be implemented without special FPGA block support. The data is always aligned with the signal **CLKOUT**, which is actually produced by the analog-to-digital converter itself. On the rising edge of

the signal, the even bits of the data word are clocked out, and on the trailing edge of the clock signal, the odd bits are valid on the bus. This procedure relies on the perfect length matching of all data and clock lines. This is described in the 5.9 as well. The designed VHDL blocks are shown in Fig. 69. Data bus A and data bus B

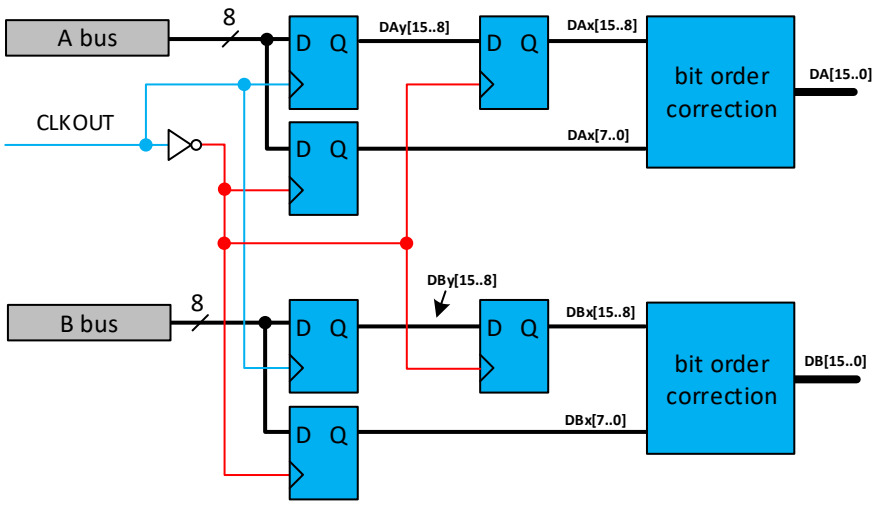


Fig. 69 De-serialization block

represent the eight LVDS data lines which are mapped as the bus type signal. Each data group is connected to the two bus D-type flip-flops (in blue color). The first flip-flop latches with the rising edge of the **CLKOUT**, while the second one works with the inverted **CLKOUT** signal, so the data bus is latched at the second (trailing) edge of the clock signal. This procedure produces the even **Dy [15..8]** and odd bits **Dx[7..0]** of the data signals. The issue could be that these signals are not latched at the precise same. This could be the problem for the further connected blocks. To maintain strict synchronization, another flip-flop block is used for the first triggered data. It will produce clock aligned data of **Dx[15..8]** and **Dx[7..0]**. As the layout of the design does not correspond with the precise bit order and also some bits are inverted due to the positive and negative LVDS line cross, the bit order correction block must be included. This block will correct mixed-up order and also invert those pairs which are inverted by the mentioned layout.

The designed de-serialization circuit was tested with the special analog-to-digital converter capabilities. With the SPI configuration circuit, the ADC chip could produce fixed data patterns in order to test the HW interface together with the de-serialization chain. The real signal measurement data stream is hard for error detection. The ADC supports following patterns ([43]):

- toggle between 0xAAAA and 0x5555
- custom single or toggle pattern
- digitally generated ramp
- 8 point sine wave generation
- constant zero or ones pattern

10.2.2 Lock-in-amplifier FPGA block

Prior to the FPGA implementation of the Lock-in-amplifier (LIA) block, the basic background of this method must be included. As the FRA method implement the amplitude measurement of the impedance in the wide frequency range, the precise input signal processing must be included. As the excitation frequency and the excitation signal is known at any time, the vector voltmeter implementation is one of the possible approaches which will satisfy this measurement. In other words, a basic vector voltmeter implementation was designed to prove the suitability of the designed platform for the method described in chapter 5. A principle of the used algorithm is shown in Fig. 70, and it is also well-known as a lock-in amplifier (LIA). The LIA is one of the commonly used techniques used to evaluate the amplitude and phase of the harmonic signals. The algorithm consists of two multipliers, two low pass filters, and a phase shifter. U_S is an input sinus wave signal, and U_R is a reference sinus wave signal.

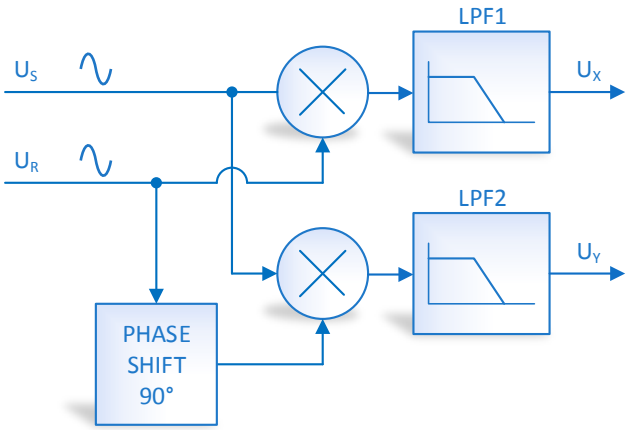


Fig. 70 The principle of the lock-in amplifier

Then the output signals U_X and U_Y can be expressed as

$$\begin{aligned} U_X =& \frac{1}{2} U_S U_R \cos\left[(\omega_S - \omega_R)\, t + \theta_S - \theta_R\right] - \\ &+ \frac{1}{2} U_S U_R \cos\left[(\omega_S + \omega_R)\, t + \theta_S + \theta_R\right], \end{aligned} \tag{30}$$

$$\begin{aligned} U_Y =& \frac{1}{2} U_S U_R \sin\left[(\omega_S + \omega_R)\, t + \theta_S + \theta_R\right] + \\ &+ \frac{1}{2} U_S U_R \sin\left[(\omega_S - \omega_R)\, t + \theta_S - \theta_R\right], \end{aligned} \tag{31}$$

that indicates that the output signal U_X is proportional to a real part of the input signal and the output signal U_Y is proportional to an imaginary part of the input signal.

The implemented core inside the FPGA is shown in Fig. 71. The signal from the correct data bus (in Fig. 69) goes to the adding block called **add16** which performs fully signed mathematical addition. This block is useful for the offset correction of the signal from the ADC converter, which is useful for auto-calibration purposes. The signal **OFF A** (**OFF B**) comes from the CPU NIOS and could be set by the firmware. After the

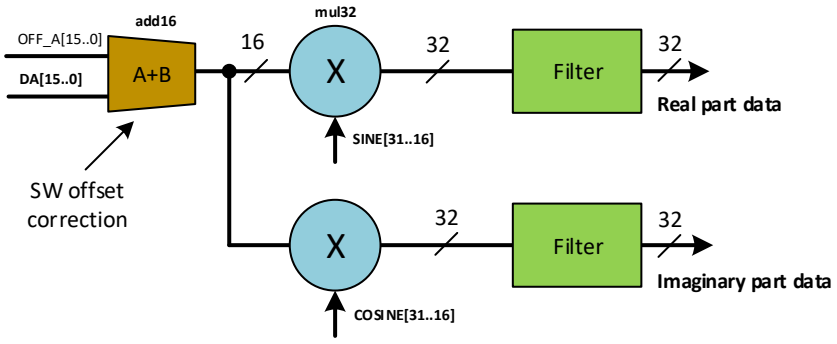


Fig. 71 Lock-in-amplifier FPGA implementation

offset correction, the signal continues to the multiplication stage, which is formed by two signed multiplication blocks **mul32**. This block performs real-time multiplication of two-bit vectors, each 16-bit width. The result is 32 bits wide. After the multiplication, the filter block is chained.

The signals **SINE** and **COSINE** are created inside the FPGA core based on the excitation data stream to the data-to-analog converter (DAC) . There are two memories of the sine-wave samples stored in the FPGA for this purpose. Each memory contains 1024 points of 32-bit wide digitally generated and preloaded sine-wave.

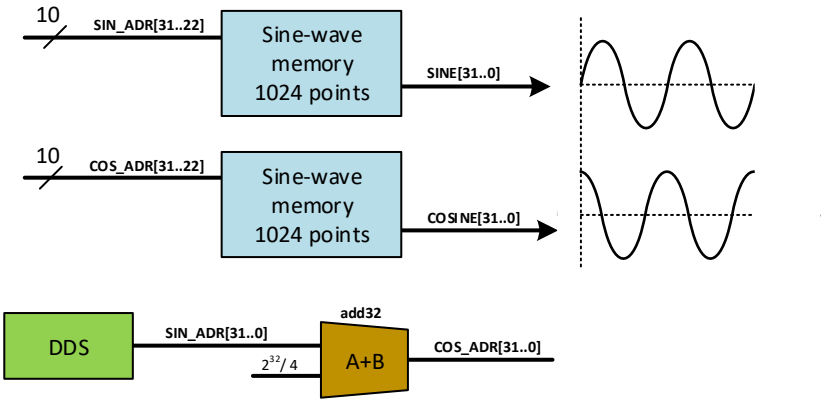


Fig. 72 Multiplication signals generation from DDS

The address generation is done by the DDS (direct-digital-synthesis) block in connection with the mentioned memories. The phase shift between the sine and cosine data output is ensured with the address shift block. This block consist of the **add32** block which moves the cosine memory address by $2^{32}/4$. As the DDS address is 32-bit wide, this addition will create a strict 90 degrees phase shift.

Tests of the vector voltmeter block

In order to test the functionality of the digital core of the LIA and to prove the parameters and features which is essential for the LIA cores, the testing platform was set. For all the performance and noise tests, the fast ADS42LB69 analog-to-digital converters were substituted by the ADS1263 sigma-delta converter, which is also available on the daughterboard, described in 9. The testing signal selection, together with the results, could be found in [46]. Briefly, the summary is following:

A few experiments were made to verify the designed platform. The first experiment was focused on a long-term stability of used ADC, the second experiment was focused on a sensitivity of a phase shift measurement, and the third experiment was focused on an accuracy of the phase shift measurement. The block diagram of the first and the second experiment is shown in Fig. 73 In Fig. 74 it is plotted data measured by the

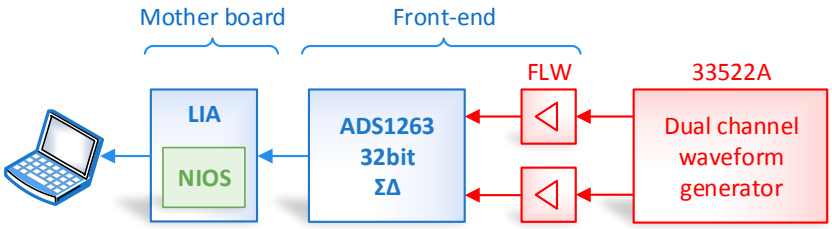


Fig. 73 The block diagram of the stability and phase sensitivity experiment

LIA algorithm (described in chapter 5) with a stable sinus waveform with a frequency of 50 Hz led into the input of the front-end board. During the two hours test, no drift was observed. The root mean square error was evaluated as $1.5\,\mu VRMS$.

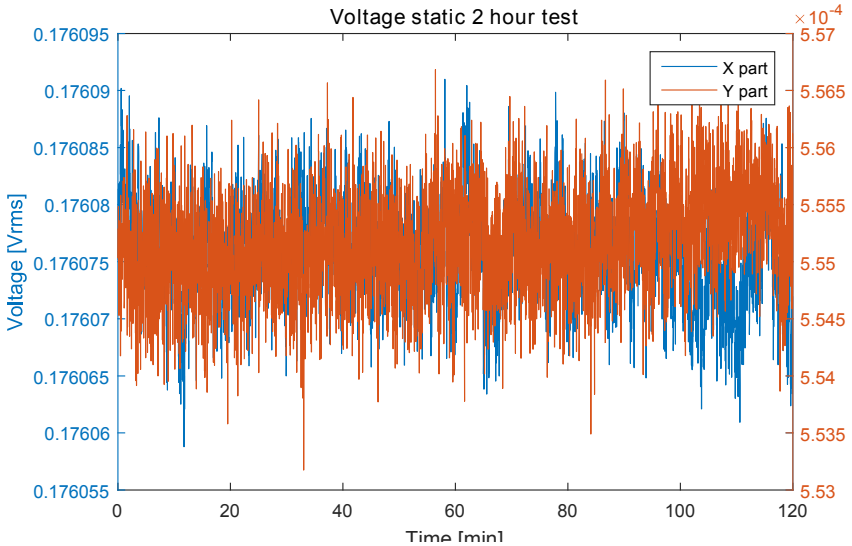


Fig. 74 The results of the long-term stability test

The second experiment was designed to prove the phase-shift sensitivity close to 0.001° that leads to the tangent delta of $1.75 \cdot 10^{-5}$. The tested signal was generated using an arbitrary waveform generator Agilent 33522A. A minimal phase shift that can be generated using this generator in the arbitrary mode at the frequency of 50 Hz is 0.00108°. The sensitivity of the phase shift change of 0.00108° is visible from the

measured data shown in Fig. 75. It is evident that the designed measuring system is able to detect at least the phase shift changes of 0.00108°.

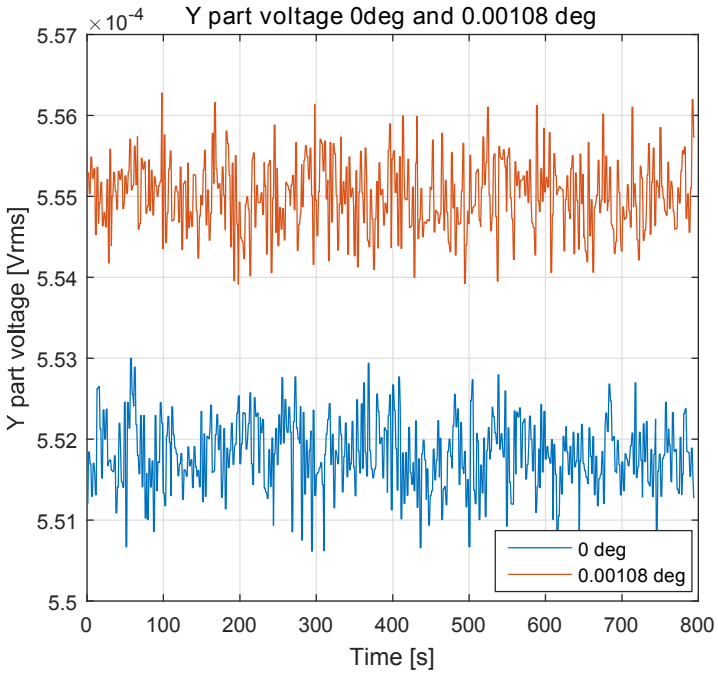


Fig. 75 The results of the phase sensitivity experiment

The third experiment was aimed to prove the accuracy of the measurement of the phase shift. A block diagram of the experiment is shown in Fig. 76. The front-end was excited by a sine waveform with a frequency of 50 Hz, and the internal phase shifter was set for different angles. Measured results are stated in Tab. 12, where UIN is an RMS value of input voltage, Φ is a phase shift set into the internal PLL phase shifter, θ is phase computed from output values of the implemented LIA algorithm, and ε is an absolute error with respect to the set internal phase shift.

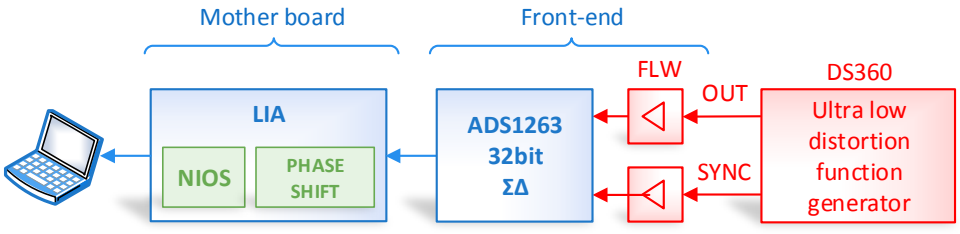


Fig. 76 The measurement of phase shift accuracy

$U_{IN}[V]$	$\varphi[rad]$	$\theta[rad]$	$\epsilon[rad]$
0.17966	0π	$-2.55 \cdot 10^{-5}$	$2.55 \cdot 10^{-5}$
0.17966	$^1/_8\pi$	0.39267	$2.91 \cdot 10^{-5}$
0.17966	$^1/_4\pi$	0.78537	$2.82 \cdot 10^{-5}$
0.17966	$^3/_8\pi$	1.17807	$2.72 \cdot 10^{-5}$
0.17966	$^1/_2\pi$	1.57077	$2.63 \cdot 10^{-5}$
0.35934	0π	$1.6 \cdot 10^{-5}$	$1.60 \cdot 10^{-5}$
0.35934	$^1/_8\pi$	0.39272	$2.09 \cdot 10^{-5}$
0.35934	$^1/_4\pi$	0.78540	$1.84 \cdot 10^{-5}$
0.35934	$^3/_8\pi$	1.17811	$1.28 \cdot 10^{-5}$
0.35934	$^1/_2\pi$	1.57078	$1.63 \cdot 10^{-5}$

Tab. 12 The results of the angle measurement accuracy

10.2.3 Excitation and frequency generation

As the excitation frequency is swept in some particular range, the intelligent frequency generation block was implemented to cooperate between the control application in the processor and the output hardware in the form of the DAC block. The implementation relies on the Direct-digital-synthesis (DDS) algorithm. First of all, the DDS algorithm should be described.

This algorithm is the basic method which is commonly used in the arbitrary function generators. It is quite trivial method for generating an analogue signal of various frequencies with help of the reference oscillator and the DAC converter. The basic principal is shown in Fig. 77. The key part is f_{REF} signal which is the reference

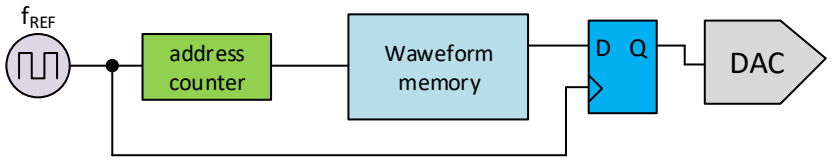


Fig. 77 Basic DDS architecture

clock signal and must be stable. The address counter and the output register latch are clocked with this reference clock signal. The waveform memory contains samples of a single period of the wanted signal (in this case, sine-wave). The output of the register continues to the DAC circuit. In every clock cycle, the following procedure is done:

- the counter value increments
- address process of the particular sample in the memory
- sample is send to DAC

The change in the frequency could be done only with the change of the waweform memory length or with the change of the f_{REF}. These changes are quite inconvenient in the real world application. Because of that the **phase accumulator** is added. The phase accumulator is increased by the preset value (here called **increase**) by each clock

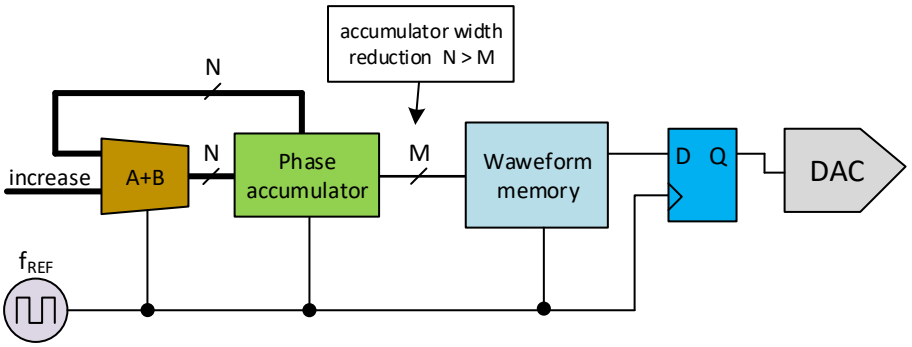


Fig. 78 Advanced DDS architecture

cycle. The accumulator, in general, is a N-bit wide number. Simply said the output frequency is follows (Eq. 32) when the increase equals 1.

$$f_{out} = \frac{f_{REF}}{2^N} \tag{32}$$

The change in the actual frequency could be made by changing the **increase** value. With the N-bit wide accumulator the frequency resolution is stated as in Eq. 33.

$$\Delta f_{OUT} = \frac{f_{REF}}{2^N} \tag{33}$$

So, in other words, the final frequency resolution is directly connected with the width of the phase accumulator. But when a better frequency resolution is demanded, the phase accumulator must increase. This is basically not a problem to increase the width of the accumulator. For instance, with the $f_{REF} = 100$ MHz, the resolution is as good as 23 mHz. The issue is in the waveform memory implementation. If the whole N-bit wide address is used, the memory requirements are too large to be designed. To overcome this problem, the accumulator width reduction takes place as shown in Fig. 78. This approach keeps the frequency resolution at superior values and also keeps the memory demands on the level which could be implemented. The actual frequency could be represented as (Eq. 34). The ΔACC is the actual value of the **increase** bus shown in Fig. 78.

$$\Delta f_{OUT} = \frac{f_{REF}}{2^N} \Delta ACC \tag{34}$$

The additional advantage is the very precise phase-shift trimming possibility. The finest step of the phase correction is in Eq. 35. This setting could be useful in combination with the LIA core described in 10.2.2. Setting the specific phase shift helps with rotating the real/imaginary output part of the LIA core.

$$\Delta\varphi = \frac{2\pi}{2^N} \tag{35}$$

The VHDL implementation is quite simple, as shown in the following shortlisting. The architecture covers the global logic vector signal **ACC**, which is a representation of the phase accumulator. Its bit width is a variable and could be set during the compilation process. At each clock rising edge, the ACC vector is increased by the input vector **f**. The output port **OUTPUT** is wired to the phase accumulator.

```
architecture a_dds of dds is

signal ACC : std_logic_vector((n-1) downto 0);
begin

OUTPUT <= ACC;

process(CLK)
begin
if rising_edge(CLK) then
ACC <= std_logic_vector(unsigned(ACC) + unsigned(f));
end if;
end process;
end;
```

10.3 SoC system and the soft-core processor NIOS

The last software block which is implemented inside the FPGA is the whole SoC subsystem. The theory behind this architecture could be found in 10.1. The list of all peripherals connected inside the SoC system could be found at the Fig. 79 (exported from Quartus software). The first subblock takes care of the input clock signal. This

Use	Name	Description	Clock
☑	clk_100	Clock Source	*exported*
☑	pll	Altera PLL	clk_100
☑	cpu	Nios II Processor	pll_outclk0
☑	sysid_qsys_0	System ID Peripheral	pll_outclk0
☑	ram	On-Chip Memory (RAM or ROM)	pll_outclk0
☑	jtag_uart	JTAG UART	pll_outclk0
☑	uart_usb	UART (RS-232 Serial Port)	pll_outclk0
☑	lcd_pio	PIO (Parallel I/O)	pll_outclk0
☑	spi_enet	SPI (3 Wire Serial)	pll_outclk0
☑	enet_pio_out	PIO (Parallel I/O)	pll_outclk0
☑	enet_pio_irq	PIO (Parallel I/O)	pll_outclk0
☑	mem_if_ddr3_emif_0	DDR3 SDRAM Controller with UniPHY	*multiple*
☑	spi_adc	SPI (3 Wire Serial)	pll_outclk0
☑	spi_sigma	SPI (3 Wire Serial)	pll_outclk0
☑	adc_outputs	PIO (Parallel I/O)	pll_outclk0
☑	adc_inputs	PIO (Parallel I/O)	pll_outclk0
☑	adc_sigma_ch1	PIO (Parallel I/O)	pll_outclk0
☑	i2c	I2C Master	pll_outclk0
☑	adc_sine_mult	PIO (Parallel I/O)	pll_outclk0
☑	adc_cosine_mult	PIO (Parallel I/O)	pll_outclk0
☑	adc_a_phase	PIO (Parallel I/O)	pll_outclk0
☑	adc_a_average	PIO (Parallel I/O)	pll_outclk0
☑	x_dds_out	PIO (Parallel I/O)	pll_outclk0
☑	x_adc_in1	PIO (Parallel I/O)	pll_outclk0
☑	x_adc_in2	PIO (Parallel I/O)	pll_outclk0
☑	x_adc_ctrl_out	PIO (Parallel I/O)	pll_outclk0
☑	x_adc_offset_in1	PIO (Parallel I/O)	pll_outclk0
☑	x_adc_offset_in2	PIO (Parallel I/O)	pll_outclk0
☑	xx_adc_in1_amplitude	PIO (Parallel I/O)	pll_outclk0
☑	xx_adc_in1_sampcount_0	PIO (Parallel I/O)	pll_outclk0
☑	xx_adc_in2_amplitude	PIO (Parallel I/O)	pll_outclk0
☑	xx_adc_in2_sampcount	PIO (Parallel I/O)	pll_outclk0
☑	spi_adc_0	SPI (3 Wire Serial)	pll_outclk0
☑	power_port	PIO (Parallel I/O)	pll_outclk0
☑	ch1_x_lia	PIO (Parallel I/O)	pll_outclk0
☑	ch1_y_lia	PIO (Parallel I/O)	pll_outclk0
☑	ch1_lia_sampcount	PIO (Parallel I/O)	pll_outclk0

Fig. 79 Qsys subsystem peripheral list

block is very important for the correct further implementation of the connected peripherals. The definition of the input clock is set to 100 MHz. The next block which

is connected to the input clock block is the **PLL** (Altere PLL core). This unit could increase or decrease the final frequency of the system by SW control from the processor. In the actual implementation, the PLL clock output is set to 100 MHz, and physically it produces a copy of the input clock signal. The most important block is the NIOS II processor core. A short introduction to this architecture could be found in 10.3.1. The next connected block is called **sysid**, which is useful for the determination of multi-SoC systems inside one FPGA or if one SoC contains more processor blocks. The sysid number could be set to any value and linked to a particular processor core. The JTAG interface and the debugging IDE will then recognize the correct core. For debugging purposes, the **jtag-uart** block is included. The program inside the NIOS processor puts the standard text output via this interface to the console of the IDE program. The very important block is the RAM block. This block is the implementation of the on-chip ram blocks. The parameters of the RAM is following:

- data width: 32 bit
- total size: 131 072 bytes (128 kB)

The ram is connected to the CPU processor to its **data master bus** and to the **instruction master bus**. This means that the Nios processor has the same memory for the code and also for the data space. There are several communication interface blocks designed for communication with the host or to control the peripheral blocks. Namely, the blocks are in the Tab. 13: The SPI for Ethernet is directly connected to the exter-

Interface type	**Symbolic name**
SPI	spi adc
SPI	spi sigma
SPI	spi enet
SPI	spi adc bat
UART	uart usb
I2C	i2c

Tab. 13 Overview of used serial interfaces

nal peripheral, which is described in . The SPI interface parameters for Ethernet are: $f_{clk} = 50$ MHz, the idle state of the clock signal is low, and the data is latched on the leading edge of the clock series. The **spi adc** is controlling the high-speed ADS42LB69 converter. The speed of this interface is not as important as Ethernet because the initialization is done only once at the start-up. The clock speed is $f_{clk} = 1$ MHz, and the clock polarity and data bit sampling are the same as the Ethernet SPI. The last SPI bus is implemented for the ADS1263 sigma-delta converter. The clock speed is the same as the previous SPI interface, while the only difference is in the data bit sampling. There is the trailing edge implemented. In the case of the ADS1263, the special block is implemented inside the VHDL. Because of the LIA tests mentioned in 10.2.2, the SPI interface of the sigma-delta must be available inside the VHDL for the LIA and also for the converter setup during the initialization phase. The connection is made as shown in Fig. 80. The control signal from the NIOS core in the form of single GPIO signals is connected to the multiplexer as a selection input and also to the VHDL core as the enable input. The initial procedure inside the NIOS processor initializes the converter, and after successful start-up, the multiplexer is switched to the VHDL core, and the enable signal runs the VHDL core. The CS signal is simply connected via, AND gate, and

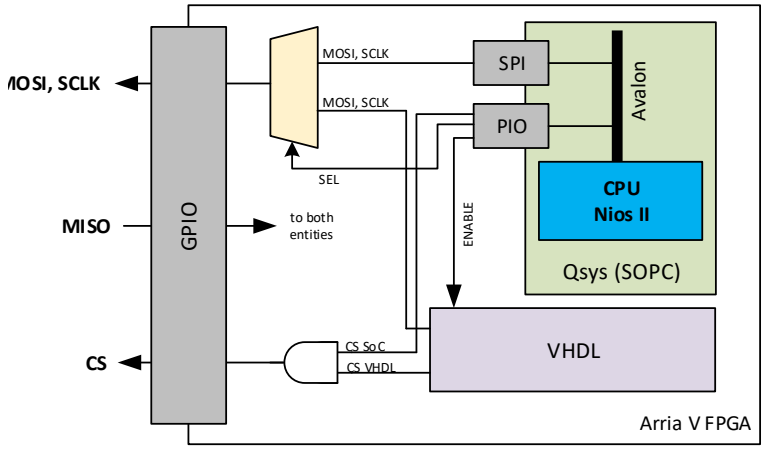


Fig. 80 The implemented connection between SPI blocks in VHDL/SoC

the MISO signal is connected to the VHDL and the processor in parallel. The last SPI interface called **spi adc bat** is connected to the accumulator board ADC monitoring circuit as described in detail in 7 and 5.6. The UART interface for the serial communication is implemented as a classical fully-handshake serial interface **uart usb**. The UART core is set to a fixed baudrate of 115200 bps with native support of handshake lines RTS/CTS. The second UART core for the RS485 core is not enabled inside the FPGA SoC in the latest firmware version. The last peripheral communication interface is the I2C master block which cooperates with the clock generator chips (described in. 5.7). This unit is responsible for the clock setup for the analog-to-digital high-speed converter. A large part of the SoC core consists of various PIO peripherals. The PIO is

Symbolic name	Direction	Used width	Usage
adc_outputs	output	4	ADS1263 control signals
adc_inputs	input	2	ADS1263 control signals
adc_sigma_ch1	input	32	ADS1263 sample data
adc_sine_mult	input	32	debugging input for multiplicated data
adc_cosine_mult	input	32	debugging input for multiplicated data
x_dds_out	output	32	phase accumulator setting
power_port	input/output	4	control of the accumulator board
adc (various)	inputs	32	monitoring of LIA stages process

Tab. 14 Overview of used PIO peripherals

typically a generic general purpose input/output port which is very similar to the pin ports in classic processors. The short summary of used PIO gates is in the Tab. 14. As the design was developed, many VHDL stages had to be monitored with the processor core, and the data from them was pushed to the PC via USB or Ethernet port. Because of that, several connections were made for LIA stage monitoring. The basic idea behind the communication between the SoC processor system and the VHDL parts is the interconnection between **std_logic_vector** elements (basic "wire" bus connection) and

the GPIO port of the processor. The results of the VHDL calculations are represented typically N-bit signed or unsigned numbers. Inside the processor core, the classical approach is to read such a wire bus to the standard C code variable type (like unsigned int, signed int, etc.).

10.3.1 NIOS processor cores

In brief, the main features of the NIOS II soft-core processor will be briefly according to [47]. It is a 32-bit processor core that and it is offered in 3 variants:

- Economy
- Standard
- Fast

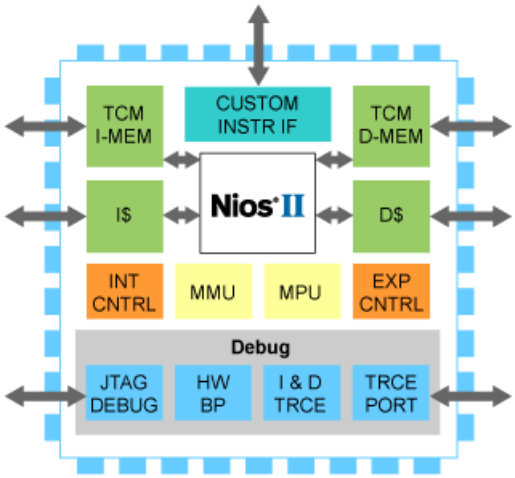


Fig. 81 Nios II processor block diagram

In the case of the FRA instrument, the fastest Fast core used in use is used (according to [47]). In the case of Arria GX, the final maximum speed could be 203 MIPS (millions of instructions per second), with the ratio MIPS / MHz, which is about 1.13. It is possible to get 100 MHz clocking processor power of approximately 115 MIPS. Next, the core preferences will be discussed. There are two memory interfaces for both data and processor code, both of which provide cache functions to speed up work with the individual memory spaces. The processor can use internal HW multiplier blocks, which provide higher computing power at the mathematical operations. The core part provides the usage of an internal interrupt controller or an external interrupt controller, which may be used with an externally implemented SoC special block. Signal processing features are implemented as a barrel shifter etc. The address space can be up to 2 GB without the use of external extensions for address bus enlargement. As the memory peripherals are not inside the kernel, they must be implemented as the external blocks within the SoC. The kernel generally supports several debugging options applications using a connected JTAG interface, with the support of breakpoints, data launchers, and other advanced tuning technologies. The advantage is the possibility of using its own instructions. In this case, there is an implementation of an HW block, which performs the requested function, and it is represented on its own within the processor application instruction. A similar style can be implemented using VHDL languages, HW calculation accelerators, and other complicated operations. The block view of the core is in Fig. 81.

10.3.2 C firmware code for NIOS

The last software block is the firmware for the NIOS II processor. The code is written in the ANSI C programming language. The control firmware is designed as a single thread control application. Very simplified main diagram of the start-up sequence is shown in Fig. 82. The power-up part initializes all SoC peripherals by its own

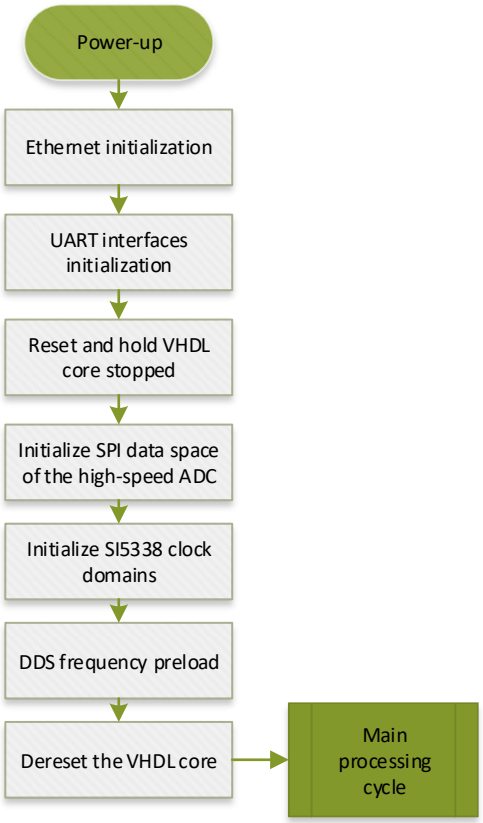


Fig. 82 Start-up procedure of NIOS C code

start-up routines, which are built-in after the SoC creation. In other words, it is not necessary to initialize all peripherals with the basic settings. For instance, if the UART peripheral is enabled inside the SoC with the particular baud rate, these settings are applied automatically. The first initialization is the setup of the Ethernet W5500 chip (HW described in 10.3). The TCP/IP settings, together with the MAC address, are done inside this routine. In addition, the socket settings are applied. After this, the network block becomes ready for interconnection in the LAN. The device could be pinged, and the socket connection is available. Very similar is the UART interface initialization. This initialization consists of the interrupt setting and buffer queues setup. To ensure that the VHDL blocks are stopped, and no data are transferred to or from the ADC/DAC parts (described in 10) the reset of all relevant VHDL blocks are held active during the rest of the initialization process. The next routine is responsible for the correct setting of the ADC configuration space. These settings consist of the correct data bus configuration and the LVDS interface. Following procedure is the I2C configuration of the SI5338 (HW described 5.7). This setup is important for the proper

data throughput of the ADC unit as well as the DAC part. The DDS algorithm is preset to the initial frequency just to maintain the reset state properly. After this power-up sequence, the initialization routine enables the VHDL blocks to continue running and to overtake the control of the sampling and digital signal processing algorithms. The firmware enters the main processing cycle. Very simplified, this part is shown in Fig. 83. The main program cycle consists of four main subroutines the ethernet handler, UART

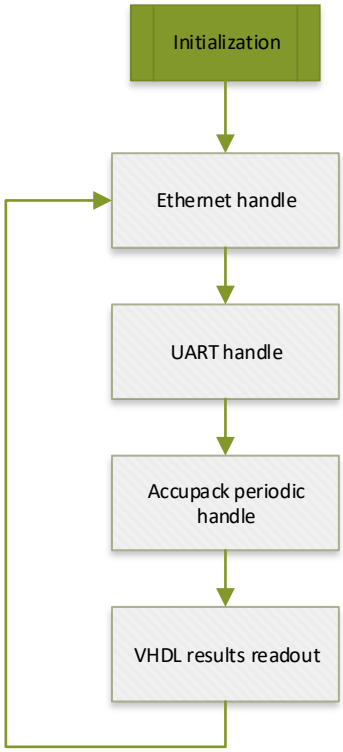


Fig. 83 Main program cycle

handler, accupack service part, and the most important, the readout of the VHDL signal processed values. Detail description of these blocks will be included in the following text.

The Ethernet handle is responsible for a complete periodic management of the networking socket. As the W5500 is hard-wired multiple TCP stack chip the control must include the socket state management together with the data exchange procedures. The detailed diagram of this part is shown in Fig. 84. This algorithm is implemented as many times as a number of sockets are desired to be used. TCP server mode is initialized in all sockets, so the connection is created from the remote client-side (typically the operator computer). When the socket connection is established, the C code firmware will synchronize all internal socket states of the code together with connection timeout renewal. The W5500 controller is then able to data exchange. The main communication protocol is Modbus, as described in detail in 10.4. This protocol is strictly Master-Slave, so the first communication must come from the connected client. When the controller signalizes the incoming data, the firmware starts to read out the packet data. This data byte array is then fed into the Modbus parser functions. This parser will completely fill the data elements (when it was a write command) or prepare output data structure

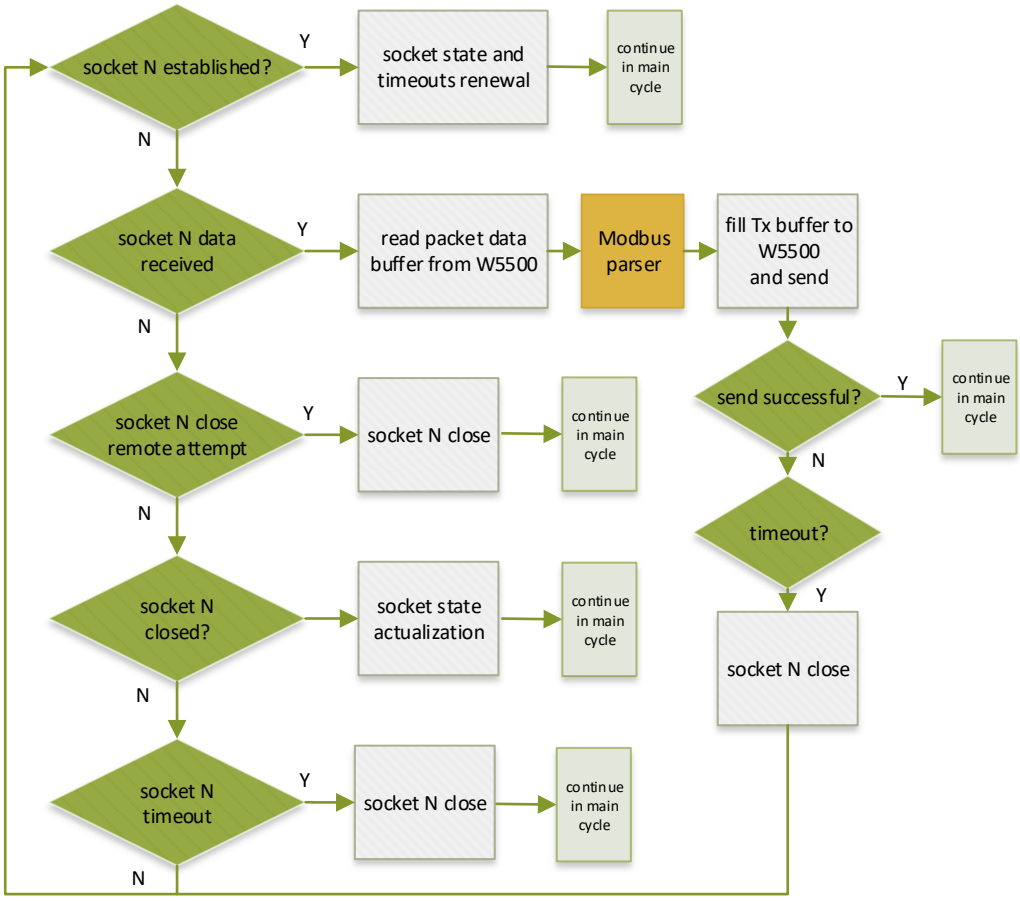


Fig. 84 Ethernet handle block

elements (when it was a read command). The reply is then passed to the function, which will fill in the transit buffer of the W5500 and command the chip to send. The sending process is then monitored to get the flag of the successful sending result. When the sending process takes too much time, the connection is closed to prevent algorithm collapse. In addition, the close procedures must be implemented as well. There are two possible scenarios. The first is the situation when the remote client is closing the socket. This situation is noticed by the W5500, and the firmware will complete the close socket procedure. The second point is when the instrument needs to close the socket due to some failure or due to timeout occurrence. The timeout is implemented for security reasons when the socket starts starving due to the physical link removal. When this happens, the socket resource is still in use, while the client-side is unable to create a new connection as the resource is occupied by previous dead binding. The inactivity on the socket connection will close down the socket for future reuse.

The second periodic task is the UART handler. The functional model of this part is very similar to the Ethernet part, while there is no concept of the connection. In other words, the connection management is omitted. When the data packet is received, it is again passed to the Modbus parser, and the reply is then sent back via UART procedures.

Accupack periodic handle consists of the continuous monitoring process of the battery

accupack voltage. This is done by the external ADC SAR implemented inside the accupack board. More detail on the hardware concept could be found in 7 especially in Fig. 51. The momentary values of the battery state are continually passed to the Modbus data structure. In addition, this routine is also responsible for switching on and off the excitation board circuitry. When the battery voltage drops below the critical under-voltage limit, the firmware shutdowns the whole device via the push-button controller chip on the accupack board (more in deep described in 7.3).

The most important periodic part is the actual measurement reading and data processing part. While most of the signal processing tasks are done inside VHDL blocks, the actual data representation must be included in the processing FW due to the propagation of the values to the host system. The actual process includes periodically following procedures:

- DDS algorithm frequency trim from Modbus actual setting
- Readout of the filtered values of the channel 1
- Readout of the filtered values of the channel 2

As the host software controls the actual excitation frequency, the Modbus setpoint is passed via the PIO peripheral to the VHDL core implementation of the DDS algorithm. In fact it is the **increase** port shown in Fig. 78 in 10.2.3. The second part is the readout of the measured values. There is a quad-port 32-bit PIO gate for reading the real and imaginary parts of both channels simultaneously. After reading, the scale factor is applied to get human-readable values in μV. These values are then sent to the Modbus data structure for computer reading. The block diagram of this readout process is shown in Fig. 85.

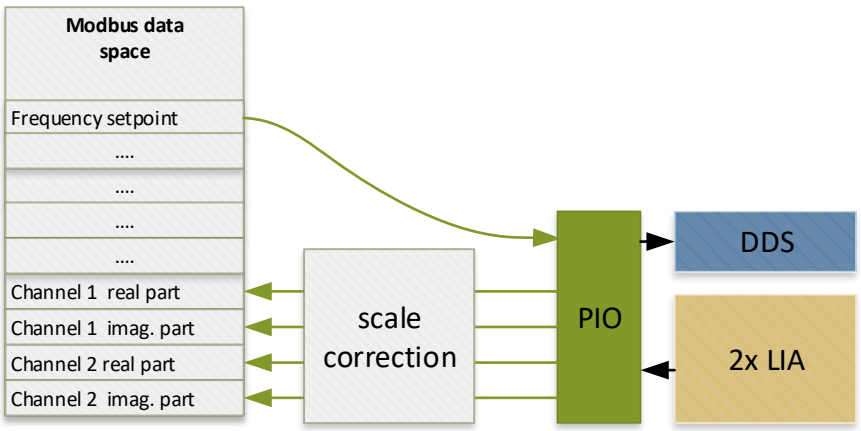


Fig. 85 Measurement readout and frequency configuration

10.3.3 Control PC application

The computer control software is programmed and crated in the Qt programming environment. The software covers communication with the FRA instrument as well as with the FDS (frequency domain spectroscopy) instrument. For computer software

and its implementation is responsible person Mr. O. Teren. As with the daughter-board in my Ph.D. thesis is only a very brief description of complete detailed software implementation is described in Mr. Teren's thesis.

The main control window is shown in Fig. 86. The central part of the control software is the plot of the measured value, while the top ribbon is for the main settings. Setting

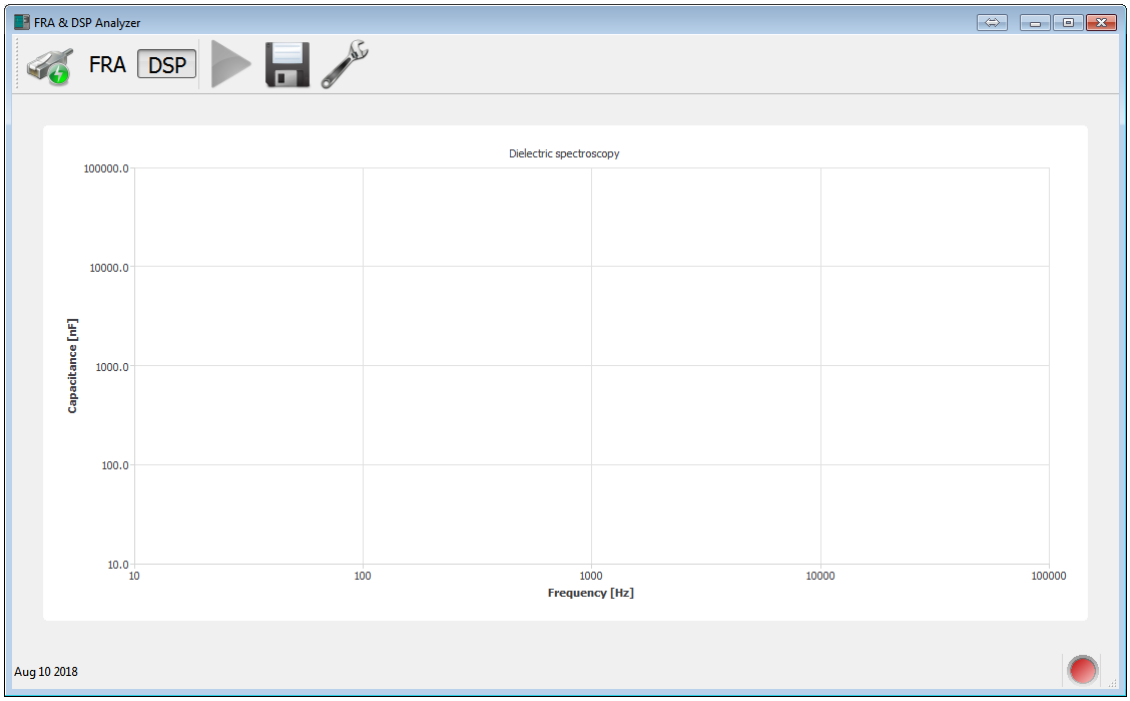
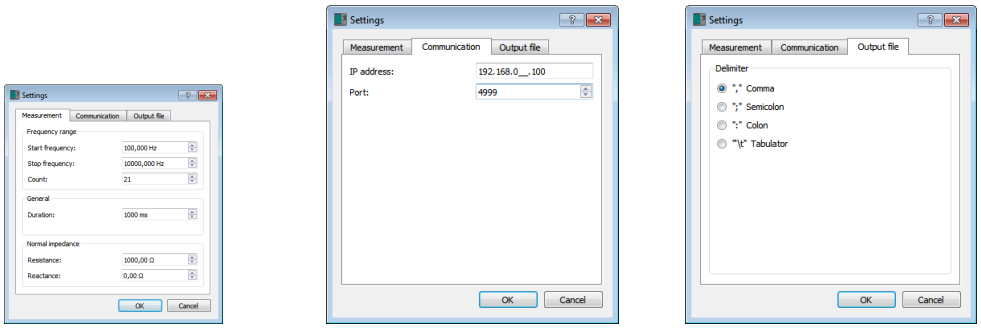


Fig. 86 Ethernet handle block

panes are shown in Fig. 87. The communication parameters, frequency measurement range, and output data representation are the very basic settings of the control software. The software is prepared to control both instruments with two types of communication protocol. Modbus TCP for the FRA and TnT bus for the FDS instrument. The data output could be in a format that is easily readable with the Matlab and Excel software as well.



(a) Measurement settings **(b)** Communication settings **(c)** Output file settings

Fig. 87 Screenshot of the application settings dialog

10.4 Communication protocol

Interconnection between the designed instrumentation and the laboratory equipment was analyzed in various aspects. Possibility of the future modularization of all designed hardware units was one of the most important objectives. In other words, the communication protocol which will be used should be chosen ideally in a standardized, well-documented, and consistent form.

At the first point, the final topology of the communication elements should be discussed. To simplify the Fig. 88 describes the typical application, where the instrumentation is directly connected via the classical wired local area network connection to the user equipment (notebook or, for instance, the measuring vehicle network structure). The LAN connection offers large modularity. The LAN interface selection was discussed more in deep in 10.3.

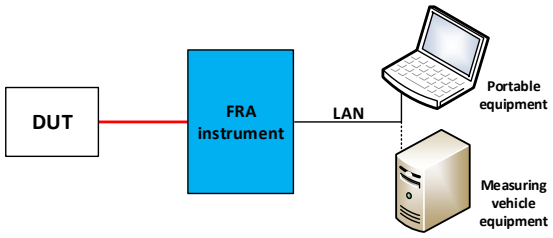


Fig. 88 User interface connection

This topology is classical P2P (Peer-to-peer) communication which enables standard Master-Slave oriented communication. There are several possibilities for how to implement sufficient protocol for this instrumentation. There are two basic approaches, how to design, implement and program any communication protocol:

- proprietary implementation ("user" standard)
- standardized protocol

The proprietary implementation involves the complete design of the protocol structure, commands, and data space. As the output of this work is a versatile instrument, which could be used as a standalone device or as a part of the functional structure, the proprietary design was not selected. The proprietary approach could be more interesting for large well-known companies, which are designing complete measuring sets for diagnostic laboratories and in-field measuring sets. The key advantage for such a company is "locked" design. Other manufactures are not compatible, so the end customer will be forced to use some type of equipment in the larger time period.

On the other hand, the standardized protocol offers more open possibilities to install various instruments in the various communication systems together. If the standardized protocol is implemented, the programmer could test the robustness with other third-party tools to achieve a more reliable program and HW implementation. The documentation for such protocol could be shortened and simplified for the end-user and/or for the programmer of the virtual instrumentation computer program as well.

10.4.1 Protocol selection

There is a number of standardized protocols used in industrial and measurement practice. The selection issue could be focused only on those protocols which are capable of Ethernet physical layer due to the HW design of the FRA instrument. The other

selection criteria were the open-source state of such a protocol. To sum up, there are a few standardized protocols that are able of Ethernet implementation:

- **Profinet**, closed standard, maintained by Profibus & Profinet International,
- **Modbus TCP**, open standard, developed by Schneider Electric in 1979
- **IEC 104/101**, documented standard, developed by IEC Technical Committee 57
- **SCPI**, semi-standardized, documented, maintaned by IVI Foundation

Among mentioned protocols, the worst implementation overhead was the Profinet, as this is the closed standard maintained by its own organization. The complete documentation should be purchased prior to implementation. The second most complex protocol is the IEC 104 (newer version of IEC 101) protocol. The complexity, which could be studied more in deep in [48] is very versatile, but on the other hand, the implementation for the FRA instrument does not really need such a specialized protocol. IEC protocol is one of the most modern protocols, especially for industrial automation and energetic applications. SCPI command set for local area communication devices could be compared to the classical text input/text output terminal protocol. The Modbus family protocols are used in a wide choice of applications with various end-usage purposes. One of the most important aspects of the final selection between the SCPI command processor and the Modbus is the communication stack. There are basically two types of communication protocols:

- command oriented protocol **without** separated variable address space

  This protocol relies on the strict command set implementation. The classical approach is the insertion of the text commands manual to the terminal program to get the output values. Users should remember the human-readable form of the commands like, for instance, *VERSION?*, *VOLTAGE?* etc. The main disadvantage of such a protocol in the future expansion of the device features. While most of the ready-made commands will not cover new functionality, the new text commands must be added. Programmed command parser must be changed on both sides of the communication. The documentation should be trimmed as well.

- communication command layer **with** separated from variable address space

  This type of protocol offers larger future scalability. Because of the separated variable (measurements, inputs, setpoints, etc.) address space, the complete protocol handler stack will stay unchanged on both sides. Only the record of the variable addresses and their meaning will be changed. In addition, backward compatibility is easily implemented.

SCPI command set is a more command-oriented protocol without strict variable data structure, while the Modbus protocol implements the second type of communication protocol very strictly. Due to the mentioned future instrumentation updates and possible features expansion, the Modbus family protocol was chosen as a more suitable protocol. In the following text, the Modbus protocol will be discussed more in deep.

10.4.2 Modbus TCP

The Modbus protocol was designed for a classical serial-line communication on the physical layers like RS485/RS422 or RS232 as the Ethernet became part of the industrial standards, the classical Modbus TCP version was created as a derivative of the serial version. Complete documentation of the Modbus could be found in [49]. Typically the end-device implements one Modbus connector on the TCP port number 502. In

addition, networking allows to implementation of more Modbus instances (runtime variables, maintenance space, service space, etc.) on several TCP ports in one physical device. The following text will describe the most important parts of the Modbus stack, which was implemented into NIOS C code runtime. The basic communication schema consists of timeout blocking request-respond schema shown in Fig. 89.

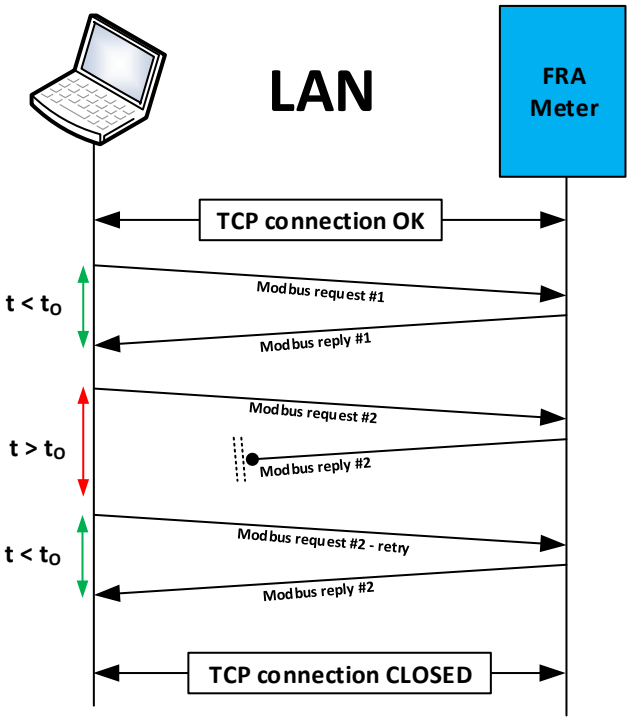


Fig. 89 Request - respond communication flow Modbus

Object types

As it was mentioned in the earlier parts of the protocol selection, the architecture involved the variable data space and the communication service for them. Modbus natively implements the following object data types in Tab. 15.

Type	Bit width	Read/write access
coil	1	full access
input discrete	1	read only
holding register	16	full access
input register	16	read only

Tab. 15 Modbus object types

One of the disadvantages is the lack of the implementation of other data types like double or float numbers. The signedness of the types is also not strictly defined by standard directly. However, the larger data types are typically formed as a connection

of the neighbors inside the data space. For instance, the float 32-bit number is a merger of two input/holding registers. The symbolic names of the object types are from the industrial meanings (coil = relay etc.). The output values address space is distinct from input values. In addition, the set values (coils or holing registers) are able to read back.

Frame format

The format of the communication frame differs between the serial version of the protocol and the TCP version. The fields like CRC (cyclic-redundancy-check) are omitted in the Ethernet version due to the implementation of the other used network layers. The basic format of the TCP frame is described in Tab. 16.

Meaning	Number of bytes	Usage
Transaction identifier	2	numbering of the request/responds
Protocol identifier	2	Modbus TCP always 0
Length field	2	bytes in the frame
Unit identifier	1	slave adress (logical)
Function code	1	function code
Data payload	n	data payload (request/response

Tab. 16 Modbus TCP frame

The transaction identifier is a mandatory field with optional usage. This number is given by the host (master), and the slave device must include the very same number in the reply. The protocol identifier is a fixed number in the case of Modbus TCP implementation. The length field indicates the remaining number of bytes after this field. The unit identifier could be used to address more subsystems inside one physical block. For instance, calibration address space could have another unit identifier.

Function codes

FRA instrument implements the following function codes from the Modbus standard.

- **FC 1** - read multiple coils
- **FC 2** - read multiple discrete inputs
- **FC 3** - read multiple holding registers
- **FC 4** - read multiple input registers
- **FC 5** - write single coil
- **FC 6** - write single holding register
- **FC 15** - write multiple coils
- **FC 16** - write multiple holding registers

In addition, the error codes like illegal data address and illegal function are fully implemented (error code 1, 2). The precise datagrams for all function codes could be found in the [49].

Data space definition

All control elements and also setpoints are defined according to the following data space definition in the Tab. 17.

Meaning	Address	Usage
Input registers		
Battery	0-1	Voltage of the battery [V]
Channel 1 real part	2-3	Real part voltage [uV] channel 1
Channel 1 imaginary part	4-5	Imaginary part voltage [uV] channel 1
Channel 2 real part	6-7	Real part voltage [uV] channel 2
Channel 2 imaginary part	8-9	Imaginary part voltage [uV] channel 2
Holding registers		
Output frequency	0-1	setpoint of the output frequency [Hz]
Coils		
Power ADC/DAC	0	when 0, reducing power consumption
Input discretes		
Low battery	0	when 1 battery level is low

Tab. 17 Modbus data space of FRA instrument

11 Uncertainties analysis

11.1 Theory

All measurements done by any human developed and manufactured instrumentation can not be taken in general as absolute precise. In other words, each instrumentation includes some imperfections or errors related to the readings of the output values. For a better understanding and defining of those issues, the uncertainty tool was presented. The measurement uncertainties are well described in [50] For a better understanding of the background of the measurement uncertainties, a few of the basic terms will be reminded. In the real world, there are many possible sources of uncertainties from the incomplete definition of the measurand up to the, for instance, finite resolutions of the used instrument. Mentioned problems above could be then covered in the standard measurement uncertainty u as it is described in [50] or [51].

Moreover, the [51] introduced the **Type A** evaluation of uncertainty which is based on the statistical results, where a higher number of observations are taken into account. The **Type B** is then connected with the other issues, which are not related to the number of the observations. Finally, the **Type C** uncertainty is called the combined value of the two mentioned before. In the more complex measurements, where the final value Y depends on the several input parameters (arguments) X_1 up to, let's say, X_n the mathematical model of the measurement Eq. 36 is useful to introduce (based on [50]).

$$Y = f(X_1, X_2, ..., X_n) \tag{36}$$

The estimate y of the measured quantity Y is then given by the Eq. 37.

$$y = f(y_1, y_2, ..., y_n) \tag{37}$$

where x_1 up to x_n are the estimates of the X_1 ... X_n.

11.1.1 Uncertainties of direct measurements

This section will briefly describe the approach for calculating the procedure how to evaluate the uncertainty of the direct measurement. The mentioned approach is used for direct measurements of the observed value. For instance, measuring the voltage with the voltmeter. Combined standard uncertainty is then equal to Eq. 38.

$$u_{C_Y} = \sqrt{u_{A_Y}^2 + u_{B_Y}^2} \tag{38}$$

The Type A covers the statistical part and equals to the standard deviation

$$u_{A_Y} = \sqrt{\frac{1}{n(n-1)} \sum_{i=1}^{n} (y_i - \overline{y})^2} \tag{39}$$

The standard Type B is then not related to the number of observations. Type B covers the other factors which affect every single measurement. In the mentioned example,

it could be the manufacturer's specification or the calibration report of the voltmeter. If there are more sources of the Type B uncertainties like the systematic error of the meter and, for instance, the temperature coefficient of the reading, then the overall Type B uncertainty is as follows:

$$u_B(Y) = \sqrt{u_{B_1}^2(Y) + ... + u_{B_n}^2(Y)} \tag{40}$$

Special emphasis should also be placed on the probability distribution. The behavior of the analyses error over specified intervals must be taken into the calculation as well. More information regarding this distribution could be found in [50].

11.1.2 Uncertainties of indirect measurements

A more complex challenge is the uncertainty analysis of the indirect measurements. For a further explanation, the mathematical model from the Eq. 36 will be as taken as the model of the indirect measurement. As well as the estimate y from Eq. 37 will be the estimate of the indirect measurement. Each of the input arguments could be obtained by the number of observations, so particular estimates have their $u_A(x_i)$ value. In addition each of those input arguments x_1 up to x_n could have specific $u_B(x_i)$ uncertainty. To combine those values correctly the **law of propagation of uncertainty** ([51], [50]) should be used.

If the input estimates x_1 up to x_n are uncorrelated, then, according to this law, the uncertainty values should be

$$u_A^2(y) = \sum_{k=1}^{m} A_{xk}^2 u_A^2(x_k) \tag{41}$$

$$u_B^2(y) = \sum_{k=1}^{m} A_{xk}^2 u_B^2(x_k) \tag{42}$$

where A_{xk} are sensitivity coefficients and they are calculated as a partial derivation of the f consequently by the particular input quantities, as shown in Eq. 43.

$$A_{xk} = \left.\frac{\partial f(X_1, ..., X_m)}{\partial X_k}\right|_{X_1=x_1,...,X_m=x_m} \tag{43}$$

Combining both types are then the same as in Eq. 38. On top of this, the expanded standard uncertainty could be calculated as follows ([50]):

$$U = k u_{C_y} \tag{44}$$

where k is the coverage factor, in values from 2 to 3 (typically).

11.1.3 Uncertainty sources in the proposed instrumentation

First of all, it is necessary to distinguish between possible sources of errors and connected uncertainties in the whole instrumentation. As the proposed solution builds all the performance parameters mainly on the digital signal processing inside the FPGA core, special emphasis will be placed on the uncertainty calculations connected with the lock-in-amplifier core. As it was briefly discussed in the 11.1.2, it is helpful to prepare basic mathematical background of the output values (readings) of the proposed FRA instrumentation.

Based on the fundamental principle (more in detail in 2.2.2), the impedance value Z is calculated as:

$$Z = \frac{U_{DUT}}{I} = R_{sense}\frac{U_{in} - U_{sense}}{U_{sense}} \tag{45}$$

In more detail, it is not sufficient to analyze and work with this simple equation because all of the measured voltages are vectors. FRA instrumentation produces measurement (estimation) of all complex components of each particular voltage. In other words, inputs to this equation are real and imaginary parts of voltage U_{in} and same U_{sense}. The corrected equation is then as follows:

$$\mathbf{Z} = R_{sense}\frac{\mathbf{U}_{in} - \mathbf{U}_{sense}}{\mathbf{U}_{sense}} \tag{46}$$

The impedance R_{sense} **will be omitted** from uncertainty calculations. The following text and analysis will use these components as **absolute precise resistance standard** without frequency-related changes in its value. Moreover, the interesting and output reading of the FRA device is the absolute value (magnitude) of the **Z**. So revising the Eq. 46 in terms of this, the output reading at specified frequency f is as follows:

$$Z(f) = R_{sense}\frac{|\mathbf{U}_{in}(f)| - |\mathbf{U}_{sense}(f)|}{|\mathbf{U}_{sense}(f)|} \tag{47}$$

And even more detailed as follows:

$$Z(f) = R_{sense}\frac{\sqrt{\mathrm{Re}(\mathbf{U}_{in}(f))^2 + \mathrm{Im}(\mathbf{U}_{in}(f))^2} - \sqrt{\mathrm{Re}(\mathbf{U}_{sense}(f))^2 + \mathrm{Im}(\mathbf{U}_{sense}(f))^2}}{\sqrt{\mathrm{Re}(\mathbf{U}_{sense}(f))^2 + \mathrm{Im}(\mathbf{U}_{sense}(f))^2}} \tag{48}$$

The purpose behind preparing the Eq. 48 in such form is to highlight the true inputs to the final calculation. As it was stated previously the instrumentation itself covers dual lock-in-amplifer and producing the complex parts of two voltages namely:

- $\mathrm{Im}(\mathbf{U}_{in})$ + $\mathrm{Re}(\mathbf{U}_{in})$
- $\mathrm{Im}(\mathbf{U}_{sense})$ + $\mathrm{Re}(\mathbf{U}_{sense})$

The simplified diagram is in the Fig. 90 The filter block behaves as the mean value

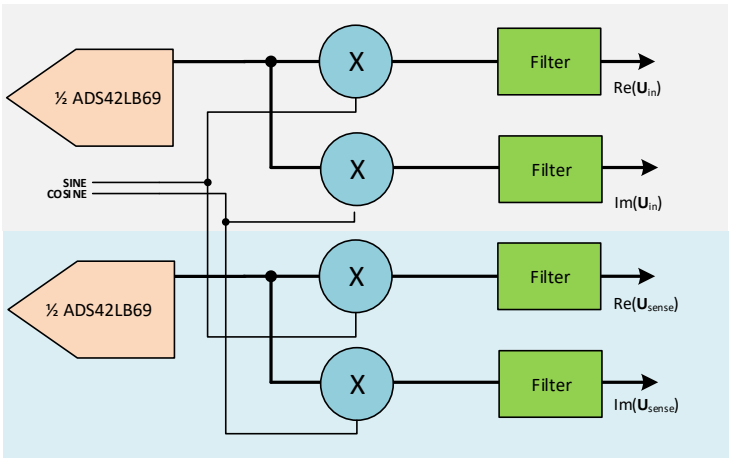


Fig. 90 Dual lock-in-amplifier simplified schematics

calculator and its depth is related to the particular signal frequency. In general for

the output value of the real and imaginary part of some voltage U applies Eq. 49 and Eq. 50.

$$\mathrm{Re}(U) = \frac{1}{n}\sum_{i=1}^{n} U_{ADC}[i]\,\mathrm{sin}_{LUT}[i] \tag{49}$$

$$\mathrm{Im}(U) = \frac{1}{n}\sum_{i=1}^{n} U_{ADC}[i]\,\mathrm{cos}_{LUT}[i] \tag{50}$$

where index n goes up to the number of samples per particular period. In other words, at large signal frequencies, the sampling rate of the analog to digital converter provides fewer samples per period T than at lower frequencies. To avoid this drawback, the algorithm takes more periods for calculating the mean value at higher signal frequencies. Sine and cosine waves are saved as non-volatile waveforms inside the FPGA in the look-up-table (LUT), the notation is sin_{LUT} and cos_{LUT}. The cosine part is actually generated directly from the sine wave memory by the memory offset, which corresponds to the 90°. For further processes of the uncertainties, it is necessary to calculate the uncertainty for all outputted values of real and imaginary parts based on the Eq. 49 and Eq. 50. Both equations are equal in terms of the final uncertainty because the whole multiplication process by the saved sine and cosine wave uses the very same samples (numbers) over the complete period T. In the most simplified and basic approach, the uncertainty connected with the ADC is $\frac{1}{2}LSB$. For better estimation, the results of the THD and ADC performance test (9.1) on the proposed HW were used. Following ADC uncertainty equation will be used (Eq. 51).

$$u_B(U_{ADC}) = \frac{1}{2}\frac{30}{2^{10.29}\sqrt{3}} \approx 13.8\,mV \tag{51}$$

The uncertainty connected with Eq. 49 (or Eq. 50) must be calculated as the partial derivation of the particular equation sequentially across the measurement points. For better illustration, assume that the sum consists of just three elements 1, 2, 3.

$$\mathrm{Re}(U)_3 = \frac{1}{3}U_{ADC}[1]\,\mathrm{sin}_{LUT}[1] + \frac{1}{3}U_{ADC}[2]\,\mathrm{sin}_{LUT}[2] + \frac{1}{3}U_{ADC}[3]\,\mathrm{sin}_{LUT}[3] \tag{52}$$

Results for sensitivity coefficients (by applying the law from Eq. 43) are following (k from 1 to 3).

$$A_{U_{ADC}}[k] = \frac{1}{3}\,\mathrm{sin}_{LUT}[k] \tag{53}$$

Proceeding to the calculation of the u_B results into

$$u_B^2(\mathrm{Re}(U)_3) = \left(\frac{1}{3}\,\mathrm{sin}_{LUT}[1]\right)^2 u_B(U_{ADC})^2 + ... + \left(\frac{1}{3}\,\mathrm{sin}_{LUT}[3]\right)^2 u_B(U_{ADC})^2 \tag{54}$$

Or in general as follows.

$$u_{_B}(\mathrm{Re}(U)) = \sqrt{\sum_{i=1}^{n}\frac{1}{n^2}\mathrm{sin}_{LUT}[i]^2 u_B(U_{ADC})^2} \tag{55}$$

This little example points to the fact that the uncertainty of the real and imaginary components are not just simple numbers, but they depend on the actual number of evaluated points as well as the look-up-table values of the multiplication waves. Using the same principle, it is necessary to calculate the uncertainty for the complete measurement result (Eq. 48). To keep the following equations more simplified (in terms of reading), the following abbreviations will be used.

- $\mathrm{Im}(\mathbf{U}_{in})$ ... I_1 $\quad \mathrm{Im}(\mathbf{U}_{sense})$ ... I_2
- $\mathrm{Re}(\mathbf{U}_{in})$ ... R_1 $\quad \mathrm{Re}(\mathbf{U}_{sense})$ ... R_2

Sensitivity coefficients are then:

$$A_{R_1} = \frac{R_1}{\sqrt{I_1^2 + R_1^2}\sqrt{I_2^2 + R_2^2}} \tag{56}$$

$$A_{I_1} = \frac{I_1}{\sqrt{I_1^2 + R_1^2}\sqrt{I_2^2 + R_2^2}} \tag{57}$$

$$A_{R_2} = \frac{R_2\sqrt{I_1^2 + R_1^2}}{(I_2^2 + R_2^2)^{\frac{3}{2}}} \tag{58}$$

$$A_{I_2} = \frac{I_2\sqrt{I_1^2 + R_1^2}}{(I_2^2 + R_2^2)^{\frac{3}{2}}} \tag{59}$$

All mentioned equations should be calculated automatically based on the particular signal excitations at various levels of the input voltage on both lock-in-cores to gain the final estimation of the accuracy of the proposed system. For this purpose, a Matlab script was created to run and simulate the signals and proceed with the calculation of the uncertainties for various measured magnitudes of connected impedance as well as different frequency span. The plotted results are shown in Fig. 91.

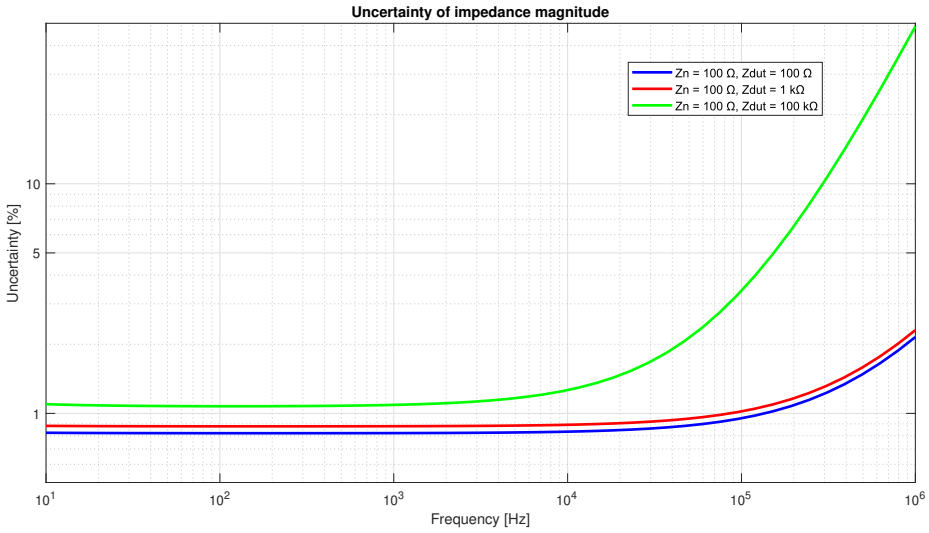


Fig. 91 Results of the estimated uncertainties

These results support the fact that when the signal becomes small in amplitude and the frequency is growing, the final values are less accurate, while when both lock-in-amplifier inputs are excited with proper signal, the uncertainty estimation stays below approximately 0.8 %. The real verification example in the 12 shows that the evaluated errors against the MFIA instrument are even smaller.

12 Verification in laboratory environment

Prior to the real environment tests, the laboratory verification took place. Based on the past simulations a simple testing prototype was built. This physical DUT was used also for the different measurement purposes of the Ph.D. work of Mr. O. Teren. This

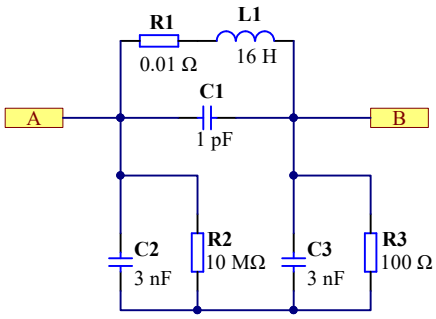


Fig. 92 Testing circuit schematic

physical DUT represents part of the equivalent schematic of the transformer disc, and its FRA response was compared to the reference measurement. The schematic of the laboratory DUT is shown in Fig. 92. The inductance L1 was physically substituted by the winding of the AC 400 W transformer. The complete details about this verification can be found in the [52]. This test was not only verification in terms of functionality, but moreover, also the accuracy issues were analyzed. For this purpose, the test consists of a reference measurement of the FRA fingerprint with the professional impedance analyzer MFIA from Zurich Instruments. In the suspected range of the frequency span between units of Hz up to units of MHz and range from several Ω up to 100 $k\Omega$, the accuracy of the measured impedance magnitude is always better than 0.1 %. In most of the suspected regions, even better than 0.05 %. More information could be found in [53]. Connection of the reference measurement was made according to Fig. 93. Reference

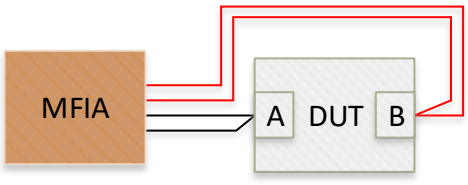


Fig. 93 DUT connection during laboratory test

output plot of the FRA fingerprint measured with the MFIA is shown in the Fig. 94. After that, the test measurement with the designed FRA instrument took place. As the connection schematic for the FRA measurement needs the sensing impedance (see

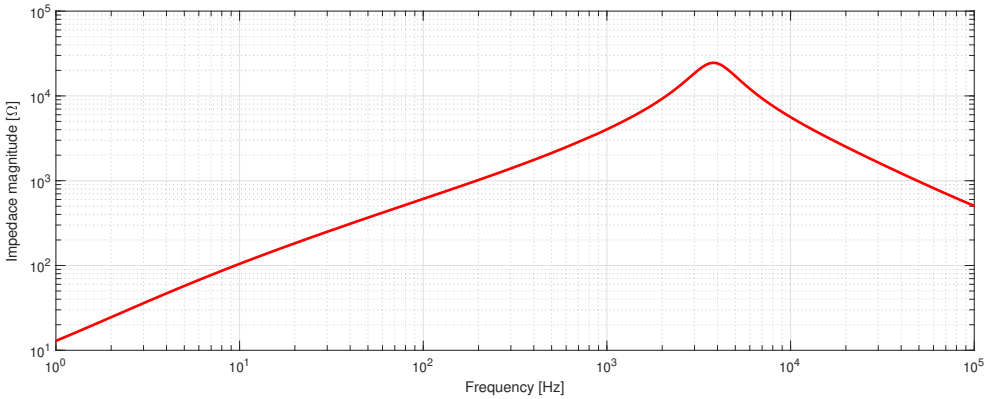


Fig. 94 Result of the measurement with MFIA Instrument

Fig. 15), the resistive etalon of nominal value 1 $k\Omega$ was chosen. The exact value of this sensing impedance was verified by the same MFIA instrument. The most important was the character of the sensing impedance over the whole suspected frequency span. It was verified that the used etalon behaves as a resistance of 999.3 Ω from 1 Hz up to 1 MHz. The setting of the proposed FRA instrument is to measure 301 points from 1 Hz up to 100 kHz. To better analyze the deviance from the reference measurement very simple metric was chosen. In each frequency point, the error value was calculated based on the Eq.60.

$$error = \frac{X - X_{MFIA}}{X_{MFIA}} \quad [\%] \tag{60}$$

The X_{MFIA} is the value measured at the specific frequency point by the MFIA reference instrument, while the X is the measured value with proposed instrumentation. The output of this analysis is the error plot in the suspected range, and it is shown in Fig. 95

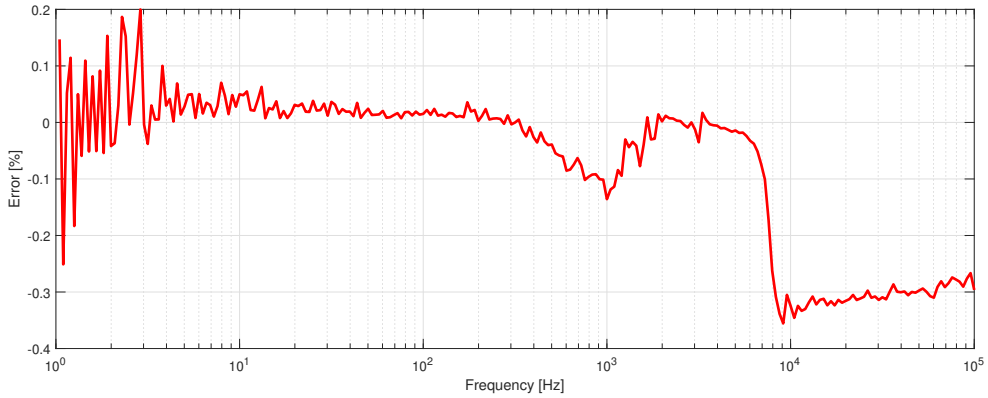


Fig. 95 Evaluated error between the reference instrument and proposed FRA instrument

The results of this test show that overall accuracy performance is promising, while the maximum difference from the reference measurements is always less than ±0.4 %.

13 Testing in real environment

Finally, the real complete verification and testing of the complete working instrumentation took place in the fall of 2017 in the company OMZ Hranice, s.r.o., which is situated in the Moravia region of the Czech republic in the Hranice na Morave city. At this place was tested also the system for the FDS measurement which is covered by the Mr O. Teren's Ph.D. thesis. This partner was selected mainly due to their rich experience in the field of high-voltage transformer maintenance. Another reason is that partner company Orgrez, a.s, which is a stable partner of our research group, has established working cooperation with the OMZ Hranice. In addition, Orgrez, a.s., is our direct partner in research projects funded by the Technology Agency of the Czech Republic (TAČR).

Fig. 96 Testing place in OMZ Hranice, s.r.o.

The complete test was done at two distinct transformer units. The units will be

hereinafter called as **transfomer A** (object A) and **transformer B** (object B). The diagnostic hall, together with our instrumentation, is shown in photography in Fig. 96. Both objects were three-phase transformers with the following winding connection inside. The connections are done in **Yzn1** style as shown in Fig. 97. So both sides are Y connected, while the second part has a neutral pole connection. The two objects were

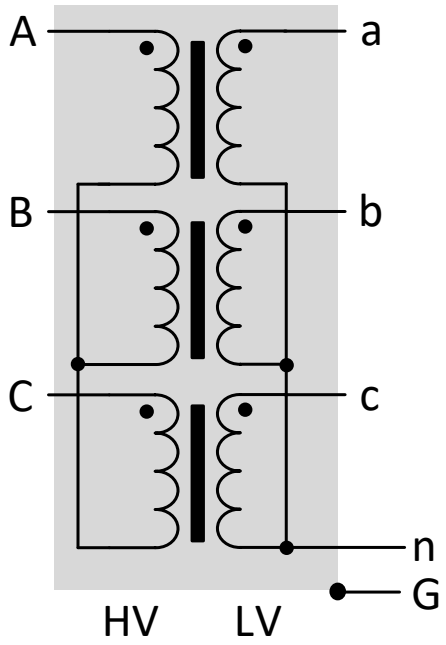


Fig. 97 Winding connection inside DUT transformers

following transformers from company BEZ Transformers, a.s. Slovakia was manufactured in the years 1985 and 1995. Both transformers were oil-cooled 100 kVA with the following specific parameters shown in Tab. 18: From the table it is obvious that both

Parameter	Transformer B	Transformer A	Unit
Primary apparent power	100	100	kVA
Secondary apparent power	100	100	kVA
Primary voltage rating	22000	22000	V
Secondary voltage rating	400 / 231	420 / 242	V
Primary current	2,62	2,62	A
Secondary current	144,4	137,5	A
Weight incl. oil	780	850	kg
Manufacture year	1985	1995	

Tab. 18 Transformer parameters

transformers are from the same manufacturer and they are the very same types with 10 year age gap.

13.1 Instrument connection

The real instrument connection to the transformer unit includes sensing impedance in addition to the FRA instrument and DUT. The connection of the measuring method must fulfil the theoretical connection of the SFRA mentioned in 2.2.2. The particular installation in OMZ is shown in Fig. 98. The instrument on the primary side was

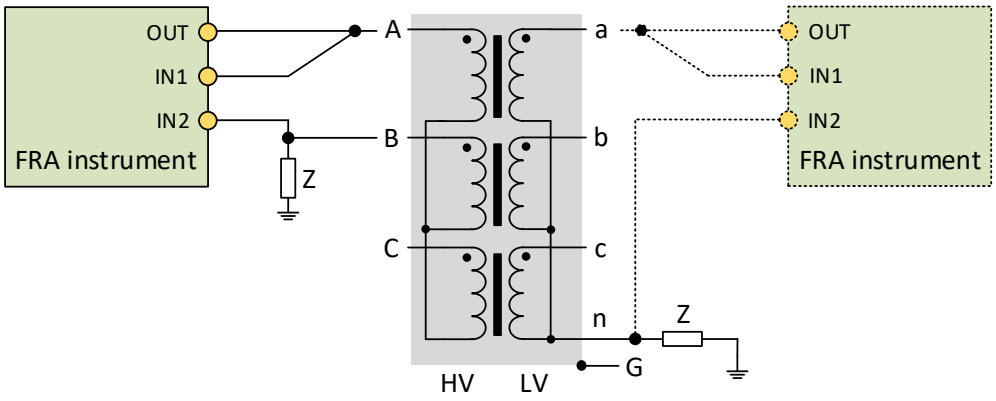


Fig. 98 Transformer connection to the instrumentation

connected to the winding A through B and the second end of the winding B, and the current which flowed out was sensed with sensing impedance Z in the form of 1000 Ω resistor. The primary side diagnostics consists of the following connections:

- A - B (sensing impedance from the end of B)
- A - C (sensing impedance from the end of C)
- B - C (sensing impedance from the end of C)

The high voltage side has no neutral terminal, so the winding can not be tested separately without opening the transformer.

Low voltage side windings have the common point terminal (neutral) directly on the case of the transformer, so the FRA connection could be individual for each winding of the three-phase transformer. The particular connection is shown in dashed lines in Fig. 98. The secondary side diagnostics consists of the following connections:

- A - n (sensing impedance from neutral terminal)
- A - n (sensing impedance from neutral terminal)
- B - n (sensing impedance from neutral terminal)

Both sides (primary and secondary) were tested in the following frequency span. This working range was selected according to the previous results in the field of the FRA testing mentioned in .

$$0.1\,Hz \quad - \quad 100\,kHz \tag{61}$$

The frequencies large than 100 kHz typically do not add any further information about defects of the DUT. The lower limit could be set to a larger value (typically 10 Hz), but the real measurement at OMZ was done in parallel with the frequency domain spectroscopy testing, so the results could be somehow compared in the future.

13.2 FRA fingerprints

The Fig. 99, 100, 101 shows the FRA fingerprint for the Object A transformer (m.y. 1995) in red colour and Object B transformer (m.y. 1985) in blue colour of all secondary windings.

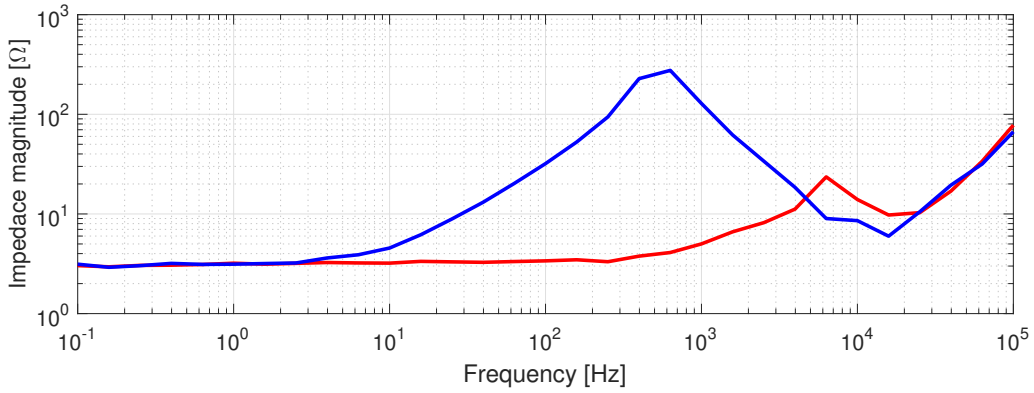


Fig. 99 Secondary winding A FRA Fingerprint

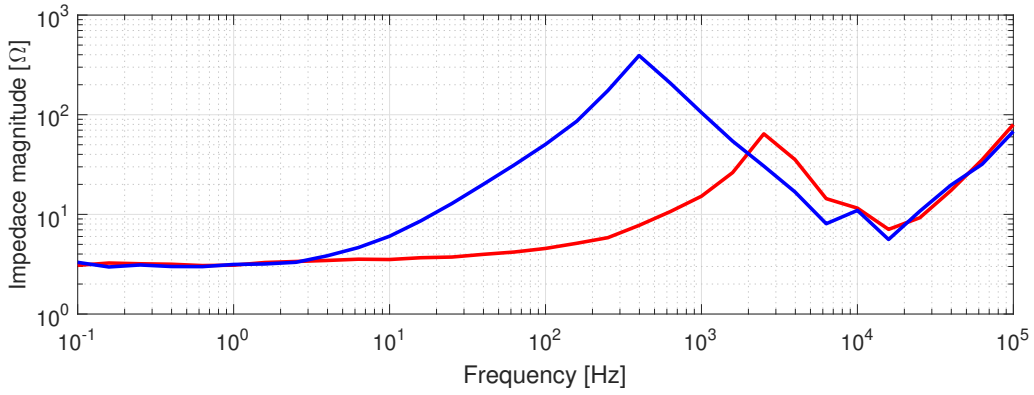


Fig. 100 Secondary winding B FRA Fingerprint

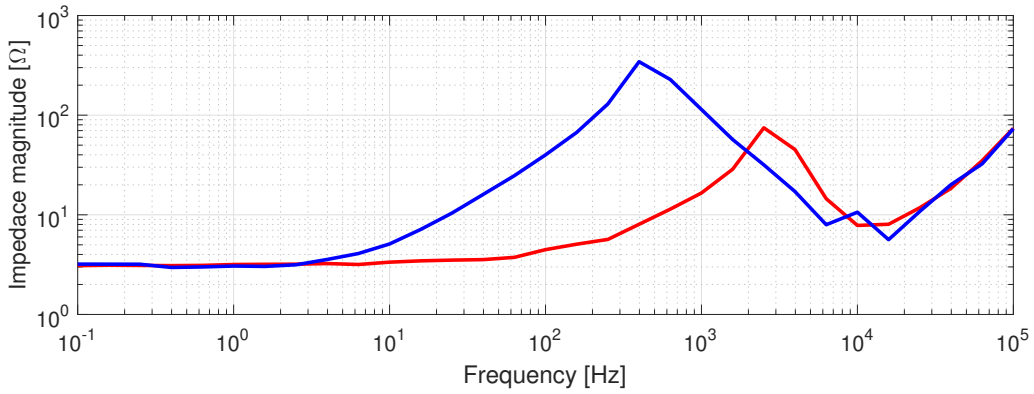


Fig. 101 Secondary winding C FRA Fingerprint

The Fig. 102, 103, 104 shows the FRA fingerprint for the Object A transformer (m.y. 1995) in red colour and Object B transformer (m.y. 1985) in blue colour of all primary windings configurations.

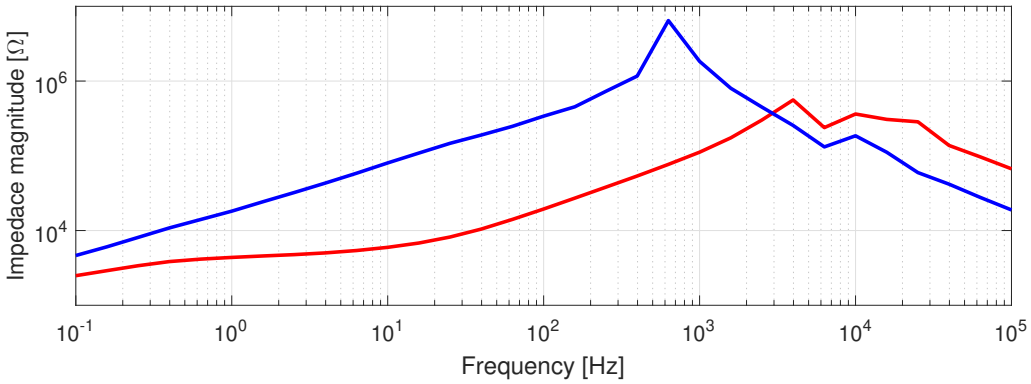


Fig. 102 Primary winding A-B FRA Fingerprint

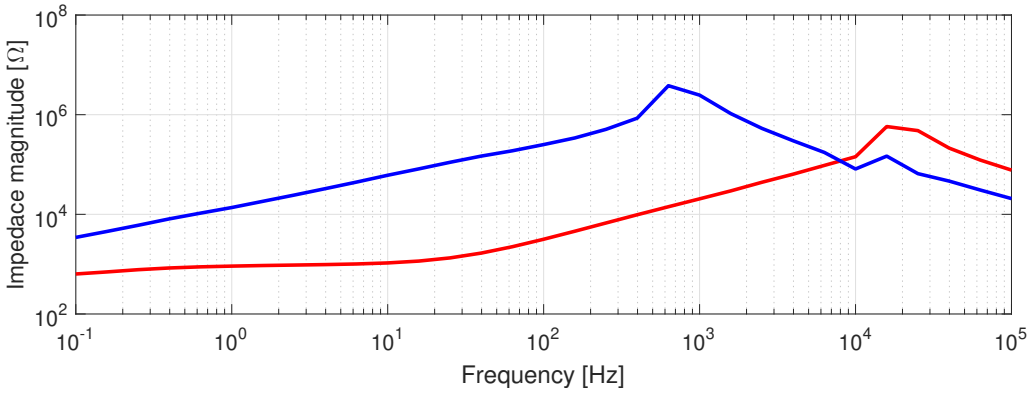


Fig. 103 Primary winding A-C FRA Fingerprint

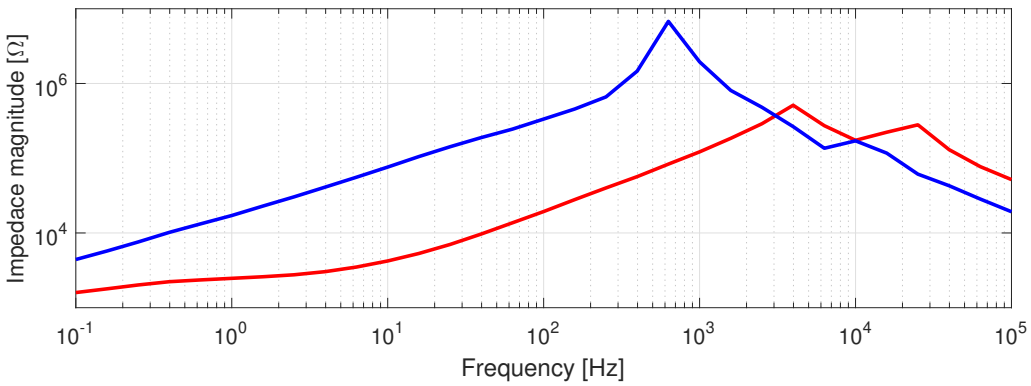


Fig. 104 Primary winding B-C FRA Fingerprint

From all FRA fingerprints above is clear that the main impedance peak has a major frequency shift, and also the magnitude of this peak is lowered. The red plots are plots of the 1995 transformer which has a failure. According to the known FRA fingerprint

changes, the most probable failure is double grounding presence together with shortened or broken disk inside the transformer. Lowered impedance is the most probable result of this mentioned. The resonance peak is shifted as well, which could also be the result of changes in the inductance and capacitance parameters. As this peak is in a higher frequency range, the capacitance and/or inductance should drop. In any case, the results of the FRA fingerprints must always be discussed and consulted against the sister or very same unit (as in our case) or with the older FRA fingerprint of the very same unit. Unfortunately, there was no chance to run that measurement with the state-of-art device at that time because it was unavailable to borrow or rent at that particular time. Despite this, the measured FRA fingerprints pointed out that the proposed instrument is capable of real tests.

14 Conclusion

The main goal in developing a specific instrumentation platform for frequency response analysis of high-voltage power devices (e.g., transformers) was completely fulfilled. This doctoral thesis covers research, scientific, and engineering work that has been done to build a specific device, test and verify signal processing algorithms, and the real-environment operation of this diagnostic tool. One of the main scientific contributions is to show the possible digital signal processing way for the manufacturers of high-voltage diagnostic equipment how to improve the versatility and quality of state-of-art devices. As the main objective is the design of the instrumentation, the specification of the device could be found in Tab. 19. The main goal consists of early mentioned several partial objectives of this thesis. The summed up results are as follows.

Research of the FRA method and state-of-art instruments

Overview of widely used electrical methods together with the reminder of the construction theory of the disk power transformers is stated in the 1.1. The physical construction of transformers is closely connected with the principles of used electrical methods. This research includes the description and brief application usage of techniques like partial discharge measurement, capacitance and dissipation factor measurement, dielectric spectroscopy, and finally a detailed look at the frequency response analysis in 13.1. In addition, the complete list of used state-of-art instruments with the full specification is included in 2.2.4.

Analyse the requirements for the hardware - HW concept

The unique hardware development as the primary goal relies on the precise conceptual design. That's why this stage was marked as a separate subgoal. The chapter 4 offers a solid list of the key parameters together with the specification for the newly developed instrumentation platform. Running the diagnostics and control of the diagnostic instruments were also analyzed, and the design of mechanical finish and remote operation was also considered. The device was designed as a battery operated with the latest modern communication interfaces and control.

Setting up the team work

The fully-functional instrument clearly proves the correct fulfillment of the teamwork setup stage. As the instrumentation platform relies on several integrated hardware and software blocks, the task division between research group members has been done. The details about the collaboration are stated in 3.

Electrical design of the system

Transferring the block hardware concept together with the stated hardware requirements into the complete schematic and circuit design has been done in the most modern electronic software tools (Altium Designer 18). Selection of the newest designing methods enables effective printed circuit board design and multi-board platform development

with the support of a 3D mechanical overview for the final instrument enclosure design and mobile operation. Each of the integrated system parts and its research and following schematic design could be found in chapter 5 for the FPGA control board, excitation unit in section 6 and last larger block of the powering structure then in the section 7. Tightly connected with the schematic design is the design work of the printed circuit boards. The specialized routing algorithms and methods were used, especially during the high-speed design of the FPGA board. Very fast LVDS and DDR3 memory connections were implemented together with the length-tuning work on the critical parts of the board. PCB result of the work at the digital FPGA board in the form of the 6-layer high-speed design with BGA 762 package satisfies modern standards of nowadays similar boards. Two more units were designed beside the most crucial FPGA board design (excitation and power circuitry parts). Details could be found in chapters 5, 6, 7. Finally, to remind, the very first revisions of all PCB units are now mounted inside the fully-functional prototypes. This fact supports the fulfillment of this stage with very successful outcomes.

Complete manufacture process of prototypes

Apart from the design phases, the physical completion of the fully-functional prototypes has been done. The research of the signal processing and the real-environment testing could not proceed without the physically finished instrument. This stage covered assembly of the printed circuit boards with all components, verifying the wide range of the peripheral parts, and mechanical parts preparation.

Digital signal processing design

As the hardware phases were ended successfully, the actual signal processing algorithms and the digital frequency response analysis were implemented inside all three levels of the firmware section. First of all, the digital samples are processed with the VHDL parallel blocks of the LIA principle (more in detail in 10. Before the particular sample handling, the high-speed stream of serialized data (up to 400 Mbps) was parsed and de-serialized inside custom VHDL blocks designed especially for the used ADC circuitry. The second level is the complete custom design of the SoC design, which enables the convenient transfer of the computed data from the logic parallel domain into the third level in the form of the sequential microprocessor core of the NIOS 32-bit microcontroller.

Software work connected with the visualization

As the instrumentation was able to measure and calculate essential data for the fingerprint visualization, the critical software task was also the robust and reliable data transfer to the visualization platform (typically portable computer). Chapter 10.4 describes the implementation and selection of the communication protocol. The Modbus/TCP variant was selected and own-programmed inside the FPGA core. This protocol is world standard, so it opens the future possibilities to interconnect our designed system with other devices or the simple addition of our future instruments.

Uncertainty and accuracy analysis

The chapter 11 covers this goal entirely. There is a brief summary of the fundamental uncertainty theory. Moreover also the law of uncertainty propagation was mentioned.

The proposed digital signal processing core was discussed in terms of the particular mathematical operations. Finally, the different excitation conditions were analyzed together with the usage of the specific frequency span. In connection with the last objective of the verification on the laboratory environment, these results bring the final accuracy estimation and validation.

Verification of the system in laboratory / real-environment

The very important stage of the laboratory testing of the complete system has been done before the real-environment testing. The main emphasis was put on laboratory verification of the complete analog-to-digital way of the signal, from the very beginning through the precise sampling and evaluation of the high-speed de-serialization and LIA signal processing. Perfect results were reached, and the instrumentation offers excellent phase sensitivity together with perfect stability and noise performance. The instrument is able to determine the phase change of 0.001°. More details can be found in. 10.2.2. As the instrumentation excites the DUT by itself, the quality of the output stage was verified as well. In addition, a comparison with the MFIA professional impedance analyzer was processed. The results of this laboratory verification (on simulated DUT) could be found in 12. Finally, the instrumentation platform was used to run tests in the real environment in the Hranice na Morave at company OMZ Hranice at several working and defective transformers. Results could be found in. 13.

To sum up the device parameters the Tab. 19 is included.

Parameter	**Value**
Frequency range	0.1 Hz ... 100 MHz (max. 250 MHz)
Measuring point spacing	linear and logarithmic
FRA method	sweep frequency
Output amplitude	30 Vpp (Z_L larger than 10 Ω)
Input amplitude	30 Vpp
Inputs	reference and measurement
Number of measuring points	unlimited
Sensing impedance	any external (typically 50 Ω or 1 $M\Omega$)
Host connection	Ethernet 10/100 Mbit/s or USB 2.0
Battery lifetime	8 h
Charger input	12 - 24 VDC

Tab. 19 Instrument parameters

14.1 Future research

The designed instrumentation platform is now in the stage that the operator could control the complete FRA measurement and inspect each of the FRA fingerprints "by eye", in other words, a high level of operator experience is needed. All of these systems typically rely on this. Some state-of-art instruments offer some kind of gallery of defects, but those are only older fingerprints received on specific devices. According to this, the future research part should involve some automatic heuristics to determine the defects. However, these algorithms need a large set of fingerprints with an accurate defect list to analyze and add to the software packages.

Another discipline and very actual topic is the online monitoring of high-voltage devices. This part could involve the FRA measurement and a partial discharge measurement system, which could be based on the same instrumentation platform as the proposed FRA platform.

15 List of publications and scientific outputs

During research on my PhD thesis, the progressive results are publicated in several scientific papers in journals and conference proceedings as well. In addition four functional samples were published. The following was generated from the Czech Technical University database V3S at November 2021.

15.1 Related with thesis

Following two impact factor publications have the same author's contribution of 40 % for Mr. Tomlain and 40 % for Mr. Tereň, rest 20 % are always for the supervisor-specialist and/or supervisor of the Doctoral Thesis.

15.1.1 Publications in jorunals with impact factor

- **TOMLAIN, J., TEREŇ, O., SEDLÁČEK, R., and VEDRAL, J.** A Hardware Platform for Frequency Domain Spectroscopy and Frequency Response Analysis. Acta Polytechnica Hungarrica. 2017, 14(8), pp. 47-63. ISSN 1785-8860.

- **TEREŇ, O., TOMLAIN, J., and SEDLÁČEK,** R. DIRECT COMPARISON OF ANALOG AND DIGITAL FGPA-BASED APPROACHES OF SYNCHRONOUS DETECTION. Metrology and Measurement Systems. 2018, 25(1), pp. 57-69. ISSN 0860-8229.

15.1.2 Publications in ISI

- **TOMLAIN, J.; TEREŇ, O.** Hardware Platform for FRA and FDS Instrumentation In: Proceedings of Student Conference on Sensors, Systems and Measurement 2021. Praha: CESKE VYSOKE UCENI TECHNICKE V PRAZE, 2021. p. 39-40. ISBN 978-80-01-06822-9.
  - **Received Diploma - 3rd. place in Ph.D. Student Prize from the Program Committee.**

- **TOMLAIN, J.; TEREŇ, O.; SEDLÁČEK, R.; VEDRAL, J.** Experimental Verification of the Fully-Digital High Voltage FPGA-Based Diagnostic Equipment In: Proceedings of the International Conference on New Trends in Signal Processing 2020. Liptovský Mikuláš: Akadémia ozbrojených síl, 2020. p. 116-120. ISSN 1339-1445. ISBN 978-1-7281-6154-9.
  - **Received Diploma Ph.D. Student Prize from the Program Committee of NTSP 2020.**

- **TEREŇ, O., TOMLAIN, J., and SEDLÁČEK R.,** The design of an analog to digital front-end for frequency domain spectroscopy analyzer. In: BEC 2016 15th Biennial Baltic Electronics Conference (BEC). 15th Biennial Baltic Electronics Conference (BEC). Tallinn, 03.10.2016 - 05.10.2016. USA: IEEE Computer Society. 2016, pp. 155-158. ISSN 1736-3705. ISBN 978-1-5090-1393-7.
- **TEREŇ, O., TOMLAIN, J., and SEDLÁČEK R.,** The design of an analog to digital front-end for frequency domain spectroscopy analyzer. In: BEC 2016 15th Biennial Baltic Electronics Conference (BEC). 15th Biennial Baltic Electronics Conference (BEC). Tallinn, 03.10.2016 - 05.10.2016. USA: IEEE Computer Society. 2016, pp. 155-158. ISSN 1736-3705. ISBN 978-1-5090-1393-7.

- **TEREŇ, O. and TOMLAIN, J.** An analog to digital front-end for frequency domain spectroscopy analyze [online]. In: HUSNÍK, L., ed. Proceedings of the 20th International Scientific Student Conferenece POSTER 2016. 20th International Student Conference on Electrical Engineering. Praha, 24.05.2016. Praha: Czech Technical University in Prague. 2016, ISBN 978-80-01-05950-0.
  - **Received Diploma for the Ph.D. work from the Program Committee of POSTER 2016.**

- **TOMLAIN, J. and TEREŇ, O.** FPGA-based System for Non-invasive Frequency Response Analysis Testing [online]. In: HUSNÍK, L., ed. Proceedings of the 20th International Scientific Student Conferenece POSTER 2016. 20th International Student Conference on Electrical Engineering. Praha, 24.05.2016. Praha: Czech Technical University in Prague. 2016, ISBN 978-80-01-05950-0.
  - **Received Diploma for the Ph.D. work from the Program Committee of POSTER 2016.**

- **TOMLAIN, J., SEDLÁČEK, R., and VEDRAL, J.** PARTIAL DISCHARGE DIAGNOSTIC SYSTEM FOR NON-DESTRUCTIVE TESTING OF HIGH - VOLTAGE MACHINES. In: HOLUB, J., ed. XXI IMEKO WORLD CONGRESS - Full Papers. XXI IMEKO WORLD CONGRESS. Prague, 30.08.2015 - 04.09.2015. Prague: Czech Technical University in Prague, Faculty of Electrical Engineering. 2015, ISBN 978-80-01-05793-3. Available from: http://www.imeko2015.org
  - **Received award for the 3.rd place in the competition "best Ph.D. paper" from the The International Measurement Confederation (IMEKO).**

- **SEDLÁČEK, R., VEDRAL, J., and TOMLAIN, J.** A Wideband Partial Discharge Meter using FPGA. In: 9th IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives. 9th International Symposium on Diagnostics for Electrical Machines, Power Electronics Drives. Valencia, 27.08.2013 - 30.08.2013. Piscataway: IEEE. 2013, pp. 519-524. IEEE CFP13SDE-USB. ISBN 978-1479-9002-5-1.

15.1.3 Scientific outputs / Functional samples

- **VEDRAL, J., et al.** Programové vybavení diagnostického systému. [Software] 2018.

- **VEDRAL, J., et al.** Funkční vzorek diagnostického systému. [Functional Sample] 2018.
- **TEREŇ, O., TOMLAIN, J., and SEDLÁČEK, R.** Měrič dielektrické spektroskopie pro vysokonapěťové stroje. [Functional Sample]. 2017
- **TOMLAIN, J., TEREŇ, O., and SEDLÁČEK, R.** Měrič frekvecnčí odezvy pro vysokonapěťové stroje. [Functional Sample]. 2017
- **TOMLAIN, J., SEDLÁČEK, R., and VEDRAL, J.** Řídicí modul FRA analyzátoru. [Functional Sample]. 2015
- **TOMLAIN, J., TEREŇ, O., and SEDLÁČEK, R.** Širokopásmový dvoukanálový synchronní detektor. [Functional Sample]. 2015

15.2 Non-related with Thesis

15.2.1 Publications in ISI

- **TOMLAIN, J., O. TEREŇ, and J. TOMLAIN.** Communication Technologies and Data Exchange Possibilities for Smart Energy Solutions. In: Proceedings of the International Conference on New Trends in Signal Processing. 2018 New Trends in Signal Processing (NTSP), Demänovská dolina, 2018-10-10/2018-10-12. Liptovský Mikuláš: Akadémia ozbrojených síl, 2018. p. 210-215. ISSN 1339-1445. ISBN 978-80-8040-546-5.
- **TOMLAIN, J., TEREŇ, O., and TOMLAIN, J.** Interoperability between Islands and Smart Concentrator Unit [online]. International Research Journal of Electronics and Computer Engineering. 2017, 3(2), pp. 28-30. ISSN 2412-4370.
- **TOMLAIN, J., TEREŇ, O., and TOMLAIN, J.** Smart grid communication technologies for renewable power sources [online]. In: BAN, M., DUIĆ, N., and SCHNEIDER, D.R., eds. 12th Conference on Sustainable Development of Energy, Water and Environment Systems. 12th Conference on Sustainable Development of Energy, Water and Environment Systems. Dubrovnik, 04.10.2017 - 08.10.2017. Zagreb: SRCE University of Zagreb. 2017, pp. 480. ISSN 1847-7178.

15.2.2 Scientific outputs / Functional samples

- **VEDRAL, J., et al.** Diagnostický systém [Prototype] 2019.
- **SEDLÁČEK, R., et al.** Functional sample of TOF camera based on application OPT8320 senzor [Functional Sample] 2019
- **JÍROVSKÝ, V., et al.** Poloprovoz: Carsharing Uniqway [Pilot Plant] 2019.
- **TOMLAIN, J., et al.** SSD Logger [Functional Sample] 2018.
- **SEDLÁČEK, R., et al.** Konstrukční návrh sério-paralelní odporové zařízení (SPRD) pro kalibraci referenčních indukčních děličů napětí. Praha: OI Praha. 2016, HS8301641C000.

- **BOHÁČEK, J., et al.** Proudové ekvalizéry pro koaxiální měřicí systémy. Praha: Úřad pro technickou normalizaci, metrologii a státní zkušebnictví. 2016, VI-II/16/16.

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