DOI: https://doi.org/10.14311/ISPS.2021.020

Measuring Transient *I*/*V* Turn-On Behavior of a Power MOSFET without a Current Sensor

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Abstract

Double pulse test (DPT) is usually used to characterize and verify turn-on/turn-off operation of power switches. Yet, new high frequency switching devices based on SiC and GaN technologies require much more elaborate DPT circuitry and sensing nodes compared to the established Si devices. Especially, suitable current sensors are challenging to realize and always limit the bandwidth.
We propose a Transmission Line Pulsing (TLP)-based technique, which we call sensor gap TLP (sgTLP) and which is capable to monitor the transient currents and voltages during the turn-on sequence of a power MOSFET, without the need of a current sensor. The proposed sgTLP approach is compared to established TLP methods in two applications: the passive switching of a fast transient voltage suppression diode and the active switching of a Si power MOSFET. The novel sgTLP shows the same or better characteristics than both of the standard methods, but needs only one measurement, where standard TLP would need two separate methods. Especially, sgTLP detected rise times of 54 ps of a current and 52 ps of a voltage signal using a pulse duration of 100 ns. The measured characteristics of the MOSFET turnon reveals several inductive and capacitive coupling mechanisms that are not analyzable by the established TLP methods but become visible applying sgTLP.

Keywords: Device characterization, Time-Domain Analysis, Power MOSFET, Transmission Line, Pulsing, sensor gap TLP (sgTLP)

I. INTRODUCTION

Electronic switches based on gallium-nitride (GaN) and silicon-carbide (SiC) materials are capable of turn-on times in the single digit nanosecond domain; some manufacturers even advertise devices with sub nanosecond rise times.[1] The circuit design and simulation with such fast devices relies on adequate large signal models [1]. Here, model validation or parameter extraction becomes increasingly challenging, as the simultaneous detection of the voltage (few volts and several hundreds of volts) and current (tenths and several tenths of amperes) waveforms at the terminals during the nanosecond switching process is hardly feasible. Therefore, state of the art characterization includes different kinds of measurement setups for different sets of parameters. Ranging from pulsed techniques [2] to frequency-based methods [3-5] every technique needs different setups and operational requirements.
The gold standard method that comes closest to the conditions the switches are exposed to in the field is the double pulse test (DPT). Here, the terminal quantities are monitored during the dynamic turn-on/ turn-off cycle. Yet, the DPT cycle is not only dependent on the device under test (DUT), but also on the DPT circuitry the DUT is embedded into and the type and position of the sensing nodes. Especially the current sensors have the most intricate realization requirements for characterization of SiC and GaN devices: high bandwidth, very low loading effect and high current ratings.
To reduce the number of different setups and to overcome the DPT restrictions we introduce first steps towards a characterizing technique that does not rely on a current sensor limiting the performance w.r.t. the above-mentioned aspects.
The presented transmission line pulsing (TLP) [6]-based setup can characterize the turning on sequence of a power MOSFET, while maintaining the exact synchronization of the acquired voltage and current waveforms at both transistor ports simultaneously.
Section II describes the novel approach and contextualize it into several established TLP techniques. Key aspects are validated using a fast transient voltage suppression (TVS) diode.
The turn-on transients of a silicon (Si) power MOSFET extracted with the proposed approach are described in Section III. A comparison with a similar technique utilizing a dedicated current sensor shows good correlation. Lastly, Section IV summarizes the results.

[1] i.e., IMW120R350M1H Infineon Technologies

DOI: https://doi.org/10.14311/ISPS.2021.020

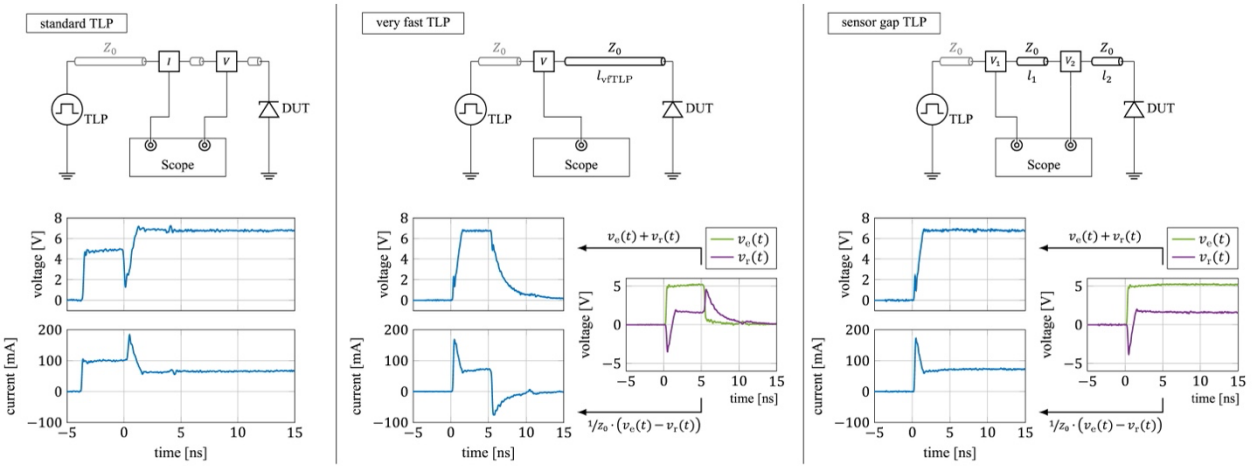

Figure 1: Three different TLP setups with the same TVS diode as DUT[2]: standard TLP, very fast TLP and sensor gap TLP. Each of the three sub-images illustrates the setup and the resulting current and voltage waveforms. Additionally, for very fast TLP and sensor gap TLP the acquired and synchronized excitation $v_e(t)$, the DUT response $v_r(t)$ and the mathematical operations to compute the current and the voltage are depicted.

II. TRANSMISSION LINE PULSING

Many different forms of the TLP method evolved out of the initial method introduced by Maloney and Khurana in 1965 [7], which was the first description of a TLP method to characterize semiconductor devices in the fast ESD regime. This evolution was driven by requirements of signal resolution and new application fields [8]. Even so, all of them have a common feature: the pulse generator (or pulser) and waveguide (cable) with a constant impedance Z_0 connecting the pulser to the DUT.

The pulser produces a very replicable short, constant voltage pulse $v_e(t)$ with a fast-rising edge, which then travels along the cable to the DUT. There, in response to this excitation, the DUT generates a transient voltage waveform $v_r(t)$, which in turn travels into the opposite direction along the cable. According to the transmission line theory the superposition of the excitation and the response at the terminals yields the current and waveforms at the DUT.

The process of sensing the signals present in the system distinguishes the different TLP methods. For the analysis in this paper, the following three are important: standard TLP, very fast TLP and sensor gap TLP.

To illustrate the relevance and limitations of each method to the topic of transistor characterization, the applicable measurements setups and the prevalent signal waveforms are depicted in figure 1. A fast TVS diode as DUT[2] shows pivotal effects: turn-on time in single nanosecond range with subsequent clamping of the voltage.

Standard TLP

The method in figure 1a is referred to as "standard" TLP or TLP (with any epithet) and is very similar to its primal origin. Here, current and voltage sensors are located near the DUT.

To understand the structure of the resulting standard TLP waveforms the following details must be considered:

(1.) The sensors are placed as close as possible to the terminals of the DUT. Even so, there are unavoidable cable pieces between the sensors themselves and between the last sensor and the DUT. Deliberately, these must be as short as possible. Additionally, as the excitation $v_e(t)$ and the DUT response $v_r(t)$ are travelling in opposite directions, small misalignments result at the measuring points of the sensors.

(2.) Both sensors generate a voltage signal proportional to the current or voltage present at their location. However, they utilize different measurement principles (current: transformer principle, voltage: resistive pickoff). This implies different transient responses, especially at the beginning of the sensor waveforms.

Moving from left (-5 ns) to right (15 ns) in figure 1a, the standard TLP voltage and current waveforms can be explained as follows:

The first part (-5 to 0 ns) of the signals is just the incoming excitation $v_e(t)$ from the pulse generator, which is a constant voltage pulse with a fast-rising edge. Both voltage and current signals are not aligned (see explanation given in (1.) above) and there is no proper way to align them, as the $v_e(t)$ and $v_r(t)$ are travelling in opposite directions. In addition, the transient responses of the sensors are clearly different at the onset of the plateaus, which is due to remark (2.).

From 0 ns onward the actual signal from the TVS DUT establishes. The voltage sensor registers a sudden drop followed by a rising edge with a small overshoot until the voltage settles to the clamping value of around 7 volts with an additional small voltage ringing in the plateau at

[2] TVS Diode: „ESD5V3S1U-02LRH" Infineon Technologies

DOI: https://doi.org/10.14311/ISPS.2021.020

about 4 ns (which will turn out to be an artefact). The current waveform shows a peak around 0 ns (during the voltage rise) with a drop to approx. 65 mA afterwards and a similar ringing at about 4 ns.
The TVS DUT turns on during the first nanosecond (0 to 1 ns). At that time, the voltage and current are determined by the charging process intrinsic capacitance of the diode until it switches to the conduction mode, where current and voltage are set by its DC characteristic.
The sensor signals do not represent this reactive turn-on behavior properly, as the misalignments (1.) and unequal sensor specific influences (2.) do disturb the first 10 ns in this measurement setup. Therefore, in standard TLP the data is usually extracted only after some nanoseconds, i.e. in the non-reactive part at the end of the pulse. Thus, the waveforms deduced by the standard TLP resemble the quasi-static DUT characteristics without second order effects like i.e., self-heating.

Very Fast TLP

If more information about the reactive DUT behavior at the beginning of the excitation is needed, the temporal resolution can be increased using very fast TLP (vfTLP). The core idea driving this method is that as soon as the exact waveforms of the excitation $v_\mathrm{e}(t)$ and the DUT response $v_\mathrm{r}(t)$ are known, both current and voltage transients can be calculated by superimposing the signals. Therefore, the main goal is to extract the excitation signal $v_\mathrm{e}(t)$ and response $v_\mathrm{r}(t)$ of the DUT separately.
To do so, vfTLP uses only one voltage sensor and a long cable between the sensor and the DUT. The cable length l_vfTLP is chosen long enough to ensure that $v_\mathrm{e}(t)$ and $v_\mathrm{r}(t)$ do not overlap at the location of the sensor. Since the current information is redundant in this setup and current sensors usually tend to have lower bandwidth ratings, the current sensor is omitted.
The figure 1b shows the vfTLP setup with the resulting voltage and current waveforms at the DUT for the same TVS diode[2] as before. Also shown are the synchronized waveforms of the excitation $v_\mathrm{e}(t)$ and the DUT response $v_\mathrm{r}(t)$, from which the voltage and the current are calculated.
Using vfTLP, the turn-on process of the TVS diode is determinable in more detail: a capacitive signal at the beginning is followed by the clamping behavior. The current rise time is determined as 145 ps, corresponding to the TLP pulse onset. Additionally, the resolution is sufficient to unveil a small inductive voltage peak during the rising current edge due to the conductors to the DUT. Moreover, the small voltage overshoot and the ringing in the plateaus (see at 2 ns and 4 ns in standard TLP waveforms) is not present.
The principal limitations of vfTLP are the cable length (l_vfTLP) between the sensor and the DUT needed to separate $v_\mathrm{e}(t)$ and $v_\mathrm{r}(t)$, which depends on the pulse duration. With common cable delays of about 4 ns/m, several meters of cable are needed for pulses longer than about 10 ns. Since long cables distort high bandwidth signals, state of the art vfTLP methods produces useful results only with pulse durations in the range of a single digit nanosecond regime.

Sensor Gap TLP

The sensor gap TLP method (sgTLP) was developed to overcome the pulse duration restriction of vfTLP, while keeping its high temporal resolution. As depicted in figure 1c, sgTLP uses two voltage sensors, separated by a well-known cable with a length of less than a meter. The cable connecting the DUT can be even shorter, so that the total cable length corresponds to delays of about 5 ns, but the method allows considerably longer pulse widths (e.g. 100 ns and more).
A sophisticated algorithm [10] combines both voltage signals to separate the excitation $v_\mathrm{e}(t)$ from the DUT response $v_\mathrm{r}(t)$, even if they overlap at the locations of the sensors. Thus, with the sgTLP method, useful pulse durations are independent of the cable lengths. The basic algorithm is described in the appendix.
The graphs below the sgTLP setup in figure 1c show the extracted pulses of the excitation $v_\mathrm{e}(t)$ and the DUT answer $v_\mathrm{r}(t)$, as well as the resulting current and voltage transients.
The voltage and currents are almost identical to the vfTLP waveforms during the duration of the vfTLP pulse, showing the quality of the sgTLP algorithm. The current rise time amounts to 153 ps, corresponding to the vfTLP value within less than one sampling period (12.5 ps) and again representing the pulse onset. Moreover, like in vfTLP, the ringing observed in standard TLP data is not present and the inductive voltage peak is visible in sgTLP, too.
But while the vfTLP pulse ends after 5 ns, much longer pulses can be used in the novel sgTLP method. Figure 1c shows only the first 15 ns of a 100 ns pulse for clarity, longer transients are discussed below.
As the sgTLP method does not rely on a bandwidth limiting current probe and employs shorter cables, the overall bandwidth of the setup can be higher in comparison to both standard TLP and vfTLP.

In conclusion, this study shows that sgTLP is superior to both standard TLP and vfTLP, as it combines the advantages of either world: very fast transients and long pulses. The sgTLP waveforms show the TVS' fast turn-on characteristics, also present in vfTLP, together with the quasi-static characteristics prevalent in the standard TLP data. The current rise times measured in this TVS experiment by vfTLP and sgTLP match within one sampling point and represent the excitation pulse rise time of 150 ps. In the standard TLP data, the rising edges are not accessible due to the described artefacts.
Nonetheless, the extraction algorithm for sgTLP with its required calibration increases the level of complexity.

III. USING TLP TO TURN-ON A POWER MOSFET

In a double pulse test (DPT) the initial condition of the DUT drain voltage is set in a predefined manner prior to

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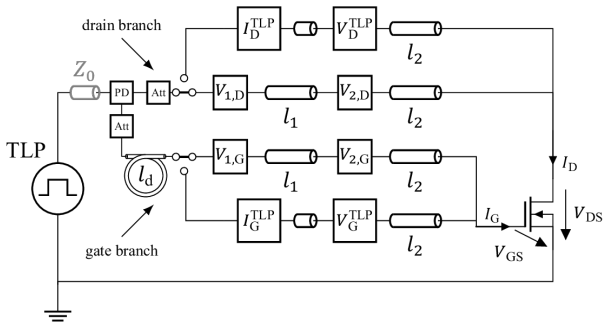

Figure 2: Measurement setup for the turn-on experiment with standard TLP and sgTLP methods.

starting of the turn-on sequence. How the device behaves during a fast ramp up for that condition is not accessible by measurement but can be very valuable for the characterization [9]. The TLP methods can be used to monitor both sequences: the settling of the drain voltage and the subsequent turning on of the device.
The following section describes the measurement setup for the turn-on of a Si power MOSFET[3] with standard TLP and sgTLP methods. This experiment inter alia directly compares the current waveforms acquired with a dedicated current sensor (standard TLP) and by the indirect current measurement (sgTLP).

Measurement Setup

As the desired turn-on sequences have durations of few nanoseconds, the following prerequisites are important:

A. Each transistor port needs a separate excitation with different amplitudes.
B. The excitation of the gate branch must be delayed with respect to the drain excitation, so there is enough time to set the drain voltage before the gate excitation initiates the turn-on process.

Figure 2 depicts the setup for the turn-on experiment with standard TLP and sgTLP setup separated by switches, so both experiments can be performed in succession. A TLP pulser system produces a single excitation with a high amplitude. This pulse is then split into two branches by a set of a power divider (PD) and attenuators (Att) to meet the first experiment prerequisite (see A.); the maximum voltages that can be acquired in the drain and gate branch are 200 V and 30 V, respectively. The attenuators have a second purpose besides setting of the amplitudes: without them there would be disruptive crosstalk between the drain and the gate branch.
In each branch there are two sensors; two voltage sensors for the sgTLP setup and a close-by current and voltage sensor combination for the standard TLP method.

[3] Si Power MOSFET: „IRFSL4127PbF" Infineon Technologies

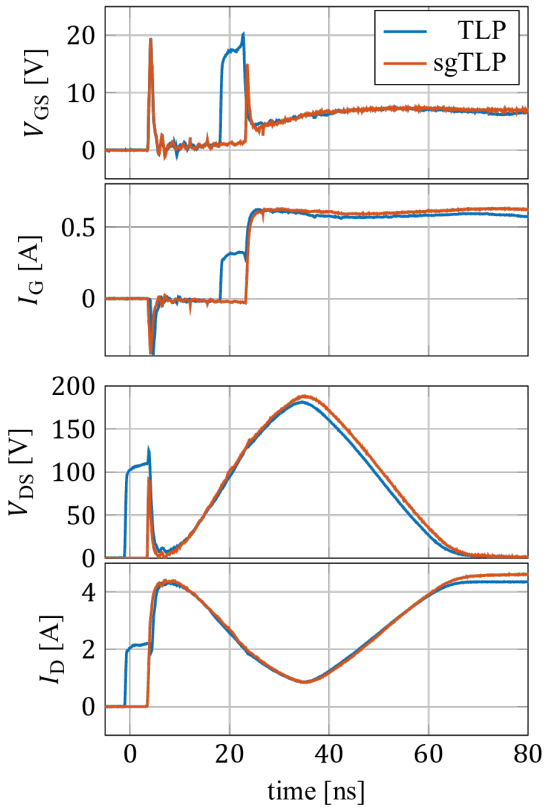

Figure 3: Transient current and voltage waveforms at the gate port (top) and the drain port (bottom) of a power MOSFET[3] during the turn-on experiment.

The second experiment prerequisite (see B.) is ensured by the additional delay line l_d in the gate branch that introduces a time difference of about 20 ns between the drain and gate excitations. Each port of the MOSFET is connected with RF needles (pitch of 0.5 mm and 40 GHz bandwidth) guaranteeing proper pulse polarities and grounding. The DUT packaged in a D^2Pak is soldered onto a PCB with about 1.5 cm copper lines.

Experimental Results

Figure 3 illustrates the average (50 pulses) transient evolution of the terminal voltages and currents during the turn-on experiments for the standard TLP and sgTLP setups. For standard TLP, the incoming pulses again occur as artefacts in the drain and gate signals at about 0 ns and 20 ns, respectively. Those artefacts mask features that are clearly visible in the sgTLP data.
The pulse enters the drain path of the DUT at $t \approx 4$ ns, starting the charging of the output capacitance until $t \approx 38$ ns. Around that time, the delayed gate pulse (starting at $t \approx 23$ ns) has charged the gate to the threshold voltage and the transistors turns on during about 22 ns.
Taking a closer look, additional more or less subtle features are evident. Starting at $t = 0$ ns the sgTLP waveforms clearly show a voltage peak in V_{GS} and V_{DS} around

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$t \approx 3$ ns. The cause of this peak is the rising current edge at the drain terminals up to 4 A in around 0.2 ns. Due to the inductance of the PCB lines and bonding wires in the drain path, the current rise is limited and an inductive voltage peak manifests in V_{DS}.
At the same time, the gate electrode exhibits a positive voltage and a negative current peak. As there is no incoming signal at the gate terminals, this gate waveform can be interpreted as magnetic coupling from the drain-source current loop to the gate-source loop.
From here onwards, the V_{DS} and I_{D} curves show the described capacitive charging behavior of the output capacitance towards about 200 V. Simultaneously, the gate electrode exhibits an increase in voltage due to the capacitive voltage divider between the miller capacitance and the gate source capacitance. Having a positive voltage at the gate terminal and no external excitation at the gate source port, a negative current flows into the Z_0 impedance cable.
At around 23 ns the gate excitation arrives at the gate port. An inductive voltage peak is evident that can be used to analyze the gate path inductance. As this voltage peak at the gate port subsides, the excitation of 30 V together with the $Z_0 = 50\ \Omega$ impedance of the cable acts as a constant 0.6 A current source for the gate. This current is charging the input capacitance until $t \approx 38$ ns, where the threshold voltage of around 5 V is reached and the turn-on sequence starts. Due to the relatively small gate current the V_{GS} remains at the miller plateau for another 20 ns while V_{DS} decreases and I_{D} rises to the values given by the transfer characteristics of the transistor.

Comparison of TLP and sgTLP Waveforms

As the V_{GS} curves in Figure 3 (top) show, the gate delay is slightly longer in the sgTLP setup. This leads to a delayed turn-on instant and, thus, to a higher maximum drain-source voltage. The difference in the gate branch delays is caused by laboratory restrictions for the cables and adaptors and is below one nanosecond.
Additionally, starting with the turn-on of the transistor, both gate and source currents become slightly higher in sgTLP than in standard TLP. A similar difference can be observed for the TVS diode described above (not shown), where the currents from sgTLP match those from vfTLP, but the standard TLP currents are slightly lower. Those discrepancies are still under investigation but seem to stem from the differences of the setups' components.
In summary, the waveforms produced by both methods match very well during the entire turn-on sequence. The inductive crosstalk to the gate loop is observable in both TLP signals, but the primary effects during the excitations' rising edges are masked in the standard TLP data, as the unavoidable distances in the setup generate artefacts just at exact this time.
For standard TLP, further attention must be paid when aligning currents and voltages in a signal path, because incoming and reflected pulses have different timings in the voltage and current sensor, respectively.

In contrast, sgTLP avoids those disadvantages by design, as the mentioned artefacts are not present in the sgTLP waveforms. Temporal resolution is increased and reveals additional information i.e., inductive and capacitive signals and crosstalk. Also, the synchronization of voltage and current in each path is more accurate, due to the manner the sgTLP waveforms are generated.
Utilizing the mentioned crosstalk, the very first peak of I_{G} and V_{GS} reveals the rise time characteristics of the respective sensor itself, undisturbed by the reflections in standard TLP. The rise times of the negative current peak are 75 ps for standard TLP and 54 ps for sgTLP, the rise time of the voltage peak is 52 ps for both methods.
The data clearly show the reduced bandwidth of the current probe in standard TLP. In sgTLP, however, the current detection rise time matches the value of the voltage measurement (in both setups) and reaches the scope limit of 50 ps, impressively showing the potential of the new method.

IV. SUMMARY

We proposed a novel Transmission Line Pulsing (TLP) based method, the so-called "sensor gap TLP" (sgTLP) that is able to monitor voltage and current transients, e.g. during the turn-on sequence of a power MOSFET, for sufficiently long times and with very high temporal resolution of 54 ps or less, for both voltage and current detection.
Instead of using a dedicated current sensor, two spatially separated voltage sensors are utilized to extract voltage and current transients at the terminals of the DUT.
Using a fast TVS diode as DUT, the proposed approach could be directly compared to established TLP methods and its very good performance could be shown for fast transients as well as for long pulses.
These findings could be further confirmed by analyzing the turn-on sequence of a Si power MOSEFT with sgTLP and a current-sensor-utilizing standard TLP setup. Applying two unequal and shifted excitations to the drain and gate terminals, the transient evolution of voltages and currents during the establishing biasing process and the subsequent turning on of the transistor could be recorded. Both approaches (with and without current probe) showed the expected general turn-on behavior. However, only sgTLP showed additional details that were masked in the current-sensor-based approach.
Thus, the noval "sensor gap TLP" (sgTLP) combines both the ability to apply "long" pulses of 100 ns or more and a very high temporal resolution of 54 ps or less. This is a promising approach, especially for the analysis of present-day fast power semiconductor devices or modules.

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APPENDIX: BASIC ALGORITHM FOR SGTLP

Figure A.1 (top) shows the measurement setup for sensor gap TLP (sgTLP) and the corresponding voltage waveforms of sensors V_1 and V_2. To illustrate the core idea of the separation algorithm clearer, the load is an inductance followed by a resistor with value of the systems characteristic impedance Z_0.
The sensor signals represent overlapping pulser excitation $v_e(t)$ and DUT answer $v_r(t)$, but the cables ensure different time shifts. The time shifts are determined as follows:

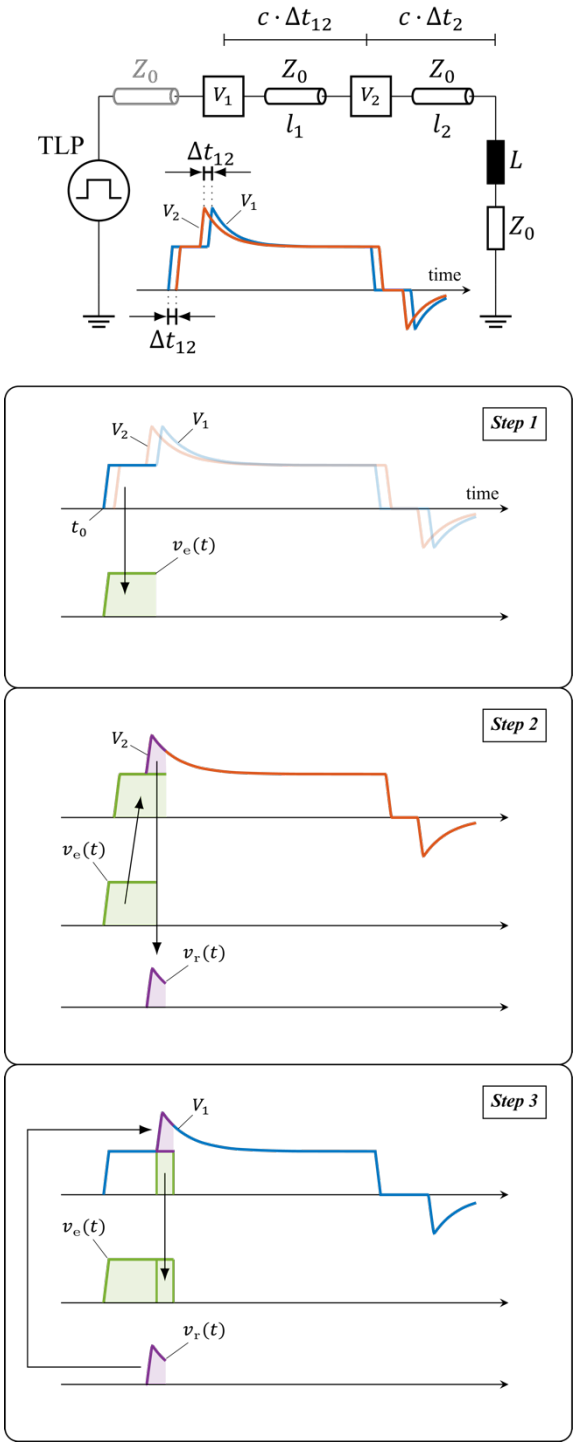

Figure A.1: Basic principle of sgTLP algorithm to separate $v_e(t)$ and $v_r(t)$.
Top: sgTLP setup with suitable DUT ($L + Z_0$) and the corresponding voltage waveforms of each voltage sensor V_1 and V_2.
Bottom: the first three steps of the sgTLP algorithm.

DOI: https://doi.org/10.14311/ISPS.2021.020

- The time delay between excitation $v_e(t)$ and DUT answer $v_r(t)$ of the sensors is
    - the double of time delay of cable 2 (l_2) for sensor V_2 and is denoted as $2 \cdot \Delta t_2$,
    - the double of combined time delay of cable 1 (l_1) and cable 2 (l_2) for sensor V_1 and is denoted as $2(\Delta t_{12} + \Delta t_2)$.
- The time shift between the sensor signals amounts to the single delay time of cable 1 (l_1) denoted as Δt_{12}.

This means that sensor V_1 "sees" $2 \cdot \Delta t_{12}$ more of the prevalent excitation $v_e(t)$ compared to sensor V_2 before the waveform is overlapped by the DUT answer $v_r(t)$. To understand how that additional information is useful to separate the overlapping signals, consider first three steps of the iterative algorithm [10], which are depicted in figure A.1.

Step 1: t_0 to $t_0 + 2(\Delta t_{12} + \Delta t_2)$ of sensor V_1's waveform is identified as the beginning of the excitation $v_e(t)$.

Step 2: This known beginning of $v_e(t)$ is first shifted by Δt_{12} to the right and then overlapped with the waveform of sensor V_2. Subtraction of both signals reveals the beginning of the DUT answer $v_r(t)$.

Step 3: The new part of $v_r(t)$ is shifted Δt_{12} to the right and overlapped with the waveform of the sensor V_1. Subsequent subtraction unveils an excitation waveform that is $2 \cdot \Delta t_{12}$ times longer than the waveform from step 1.

Steps 2 and 3 are then repeated until $v_e(t)$ and $v_r(t)$ are separated entirely. Having both separated waveforms, the current and voltage results from the usual vfTLP calculation (see figure 1).