DOI: https://doi.org/10.14311/ISPS.2021.019

Development of an HBM-ESD tester for power semiconductor devices

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Abstract

Recently, the human body model - electrostatic discharge (HBM-ESD) test capability for power diodes was introduced among the requirements in the field of automotive include for a superior reliability. During the HBM-ESD test, the DUT works in avalanche conditions and it is still not well understood the failure modality occurring in power diodes. The available commercial HBM-ESD testers only give information about the maximum voltage rate, without any specific measurement of electrical waveforms. In this work we present a HBM - ESD tester for the characterization of power semiconductor devices up to 6 kV. In the proposed tester both the voltage and current DUT waveforms are measured, for a further gain of the failure analysis in power diodes.

Keywords: Human-Body-Model Electrostatic Discharge (HBM-ESD), Avalanche Breakdown, Power Diode

INTRODUCTION

The power semiconductor devices market is demanding for power semiconductor devices with a superior reliability in out of safe operating area (SOA), with a specific emphasis on the avalanche capability. Usually, the avalanche capability of a power diode is measured through the unclamped inductive switch (UIS) test [1], that is the maximum energy that the DUT can stand in avalanche conditions (A sketch of the UIS test schematic is reported in Fig. 1a). However, the last requirements in the field of automotive concern about the reliability in terms of HBM-ESD [2] (A sketch of the UIS test schematic is reported in Fig. 1b). This model approximates the electrostatic discharge that may occur when a person handles a device. Typically, the HBMESD event is not considered detrimental for power diodes. However, recent studies highlight as power diodes may fail under electrostatic discharge [2], unexpectedly. The HBM-ESD capability concerns the reliability in handling procedures for mounting discrete power diodes is automotive applications, such as DC-DC converters or inverters. As for UIS, the HBM-ESD test forces the DUT to operate in avalanche conditions. Since the HBM-ESD test energy is at least one order of magnitude lower than the one of the UIS test, different current density dynamics are expected to occur during the test. Numerical results in highlight as the higher di/dt occurring during the HBM-ESD test leads to the occurrence of failures different from that of UIS. As reported in [2], unexpected effects as current filamentation may occur during the ESD test, leading to premature failure. Typically, the current filamentation leads to a strong variation of the Cathode voltage. Therefore, the measurement of the current and voltage

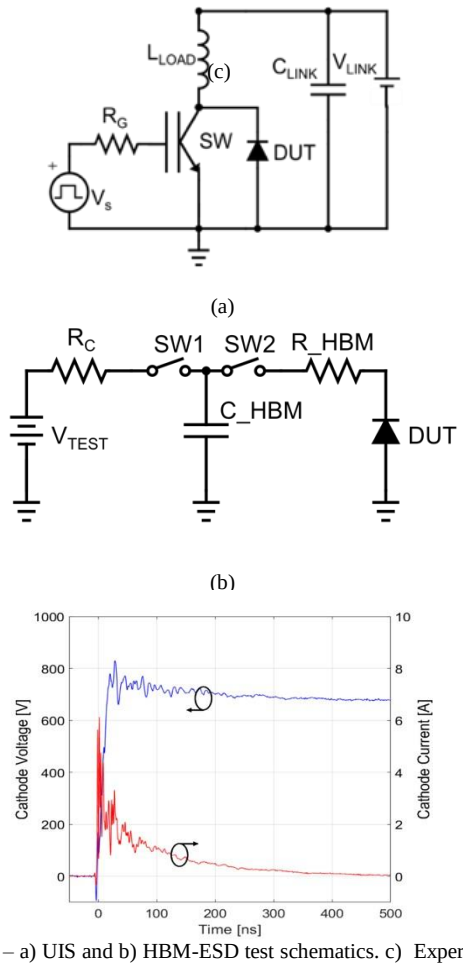

Figure 1 – a) UIS and b) HBM-ESD test schematics. c) Experimental device [4] HBM-ESD test waveforms.

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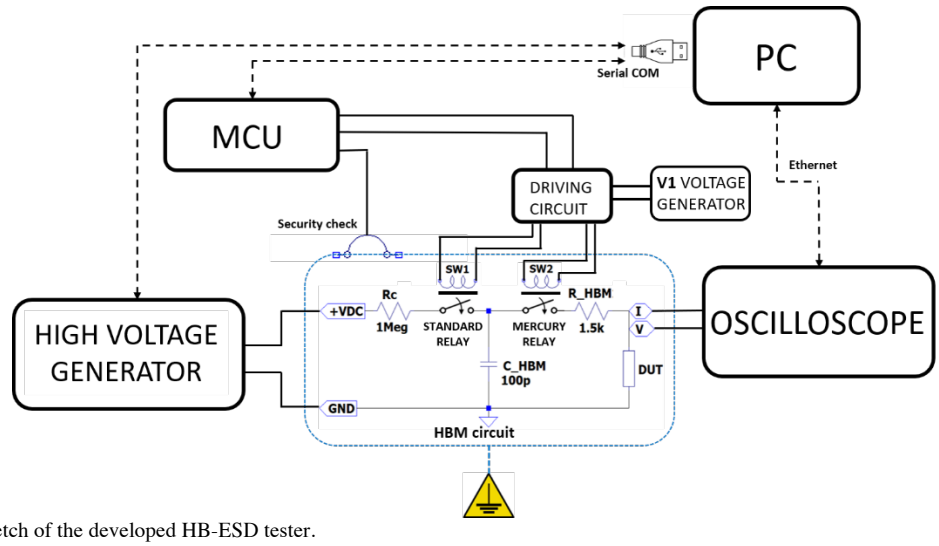

Figure 2 – A sketch of the developed HB-ESD tester.

waveforms at the DUT terminals during the ESD test gives further elements for the investigation of failure, supported by TCAD simulations. The main disadvantage of the commercial ESD tester is the impossibility to measure the current and voltage waveforms occurring at the terminals of the DUT during the test. Results in [2] show as the cathode voltage waveform during the HB-ESD test gives important information about the current distribution over the time. In this work we present an HBM-ESD tester capable to measure the electrical waveforms, with a consequent gain in the comprehension of the failure events. Therefore, in a first section the experimental setup in presented. In a second section some experimental data are reported and commented.

THE DEVELOPED HBM-ESD TESTER

The reference standard for the HBM - ESD tester is reported in [3] and in Fig. 1b the circuit of principle is reported. C_HBM=100 pF, R_HBM = 1.5 kΩ and R_C = 1 MegΩ. Basically, the C_HBM capacitance in a first step is charged at the V_{TEST} voltage through SW1 that is a short circuit. In this phase SW2 is an open. When the voltage drop at the C_HBM terminals achieves the target value, SW1 becomes open and after a suitable delay time SW2 turns to the short-circuit condition. At this point, since the DUT voltage is zero, a current equal to V_{TEST}/R_HBM flows into the DUT and forces it into the avalanche condition. Therefore, once the DUT voltage achieves the breakdown voltage (BV) the voltage clamps and the current exponentially drops with a time constant equal to $\tau = R\_HBM \cdot (C\_HBM + C_{DUT})$, where C_{DUT} is the DUT capacitance. This time constant is the main difference between the UIS and the HBM-ESD tests. For the former test the current falls down with a slope equal to $di/dt = -(BV - V_{LINK})/L_{LOAD}$ and typically it is at least one order of magnitude higher than that of a HBM-ESD test. As an example, the HBM-ESD waveforms of device [4] are reported in Fig. 1c. However, the implementation of the setup involves the design of the different parts that compose the test, as sketched in Fig. 2. The most critical component of the tester is SW2, a

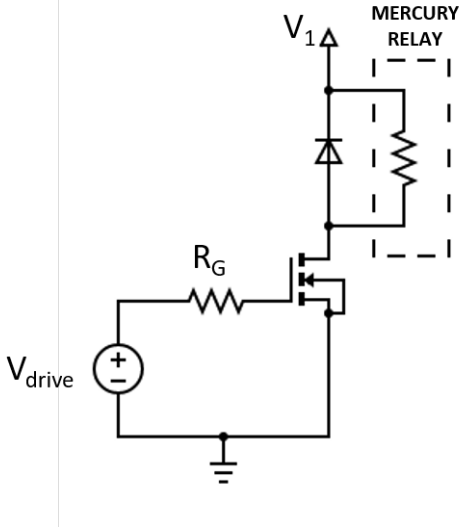

Figure 3 – The Relays driving circuit schematic.

relay that uses mercury as a switching technology. This is mandatory to achieve the requirements of the [3] standard. The SW2 switch must become instantaneously a short circuit to replicate the exact testing conditions. Moreover, a V_{TEST} up to 7kV is applicable to the terminals of both SW1 and SW2. This is not compatible with most of the semiconductor or vacuum tubes switches. A standard relay is not usable, since it exhibits contact bounces that interrupt the C_HBM discharge and this is not suitable for an HBM-ESD tester. In Fig. 3 the driving circuit of both the switches SW1 and SW2 is reported. Basically, the relay coil is the load of a power MOSFET in common emitter configuration. V_{drive} in Fig. 3 comes from the driver IC MCP1404, supplied at 15 V by the voltage generator V1, that has as the input a digital output of the STM32F401RE Nucleo-64 board. The same board checks that the circuit box is closed, to assure a safety measurement. If it is open, the MCU does allow to run the test. Finally, through a Matlab© graphical user interface the PC in connected to the high voltage generator, the oscilloscope and the STM32F401RE Nucleo-64 board. A multi-purpose sock is used to

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quickly connect up to three terminals power devices (TO220 like), as well as two general purpose terminals. The current flowing through the DUT is measured by a current transformer.
Finally, the high voltage supply is given by the SRS PS375 generator [5], that has a maximum voltage capability of 20kV. The limitation to 7 kV is related to the maximum measurable voltage of the voltage probe of the oscilloscope.

RESULTS AND COMMENTS

Different families of devices were tested to validate the setup and to evaluate their HB-ESD capability. Recalling results in Fig. 1c, the voltage and current waveform is reported for the commercial device [4] for V_{TEST} = 3.2 kV. When the SW2 gets close, the current suddenly achieves its peak and after 20 ns the cathode voltage achieves the breakdown voltage (BV) of the device, that is in the order of 700V. Some cathode voltage oscillations are visible, but their variation lays in the range of 50 V. These oscillations are mainly related to the parasitic elements of the circuit. Therefore, the setup board design was carried out with very low parasitic capacitance and inductance. However, the DUT itself may be the origin of the oscillations and their evolution may give information about the current distribution into DUT, as reported in [2]. In Fig. 4 the electrical waveforms are reported for the device [6] with V_{TEST} = 3 kV. As for the previous device, after 20 ns the cathode voltage achieves a BV voltage in the range of 1000 V, even if the voltage rate of the device is 650 V. Moreover, when the cathode current becomes negligible, the cathode voltage rises up to 1200V. At the same time the cathode current exponentially goes down. Differently from data reported in Fig. 1c, the voltage oscillations have a lower and irregular frequency. This a complex behavior and it is a typical experimental evidence that highlights the presence of a strong current filamentation in the device [2], [7]. The current filamentation is due to the presence of a negative differential resistance (NDR) in the reverse I-V curve of the DUT and it becomes more relevant when the conduction carriers concentration becomes comparable to the doping concentration of the Drift layer [8]. The more the oscillations are large, the more the current density is higher into the filaments, with the consequent voltage variation. In these conditions the high instability of the impact ionization phenomenon becomes dominant and the current crowding becomes the stable condition. When the current filamentation occurs, the cathode voltage drops down to a voltage that is typically up to 200 V lower than the BV at low current levels. However, as soon as the total current flowing in the device achieves a value where the I-V blocking curve has a positive differential resistance, the current spreads and becomes constant over the area of the device. When this occurs, the cathode voltage goes back to the BV voltage for low current densities, that is typically higher. This kind of dynamic occurs if the current filamentation does not leads to a premature destruction of the device.

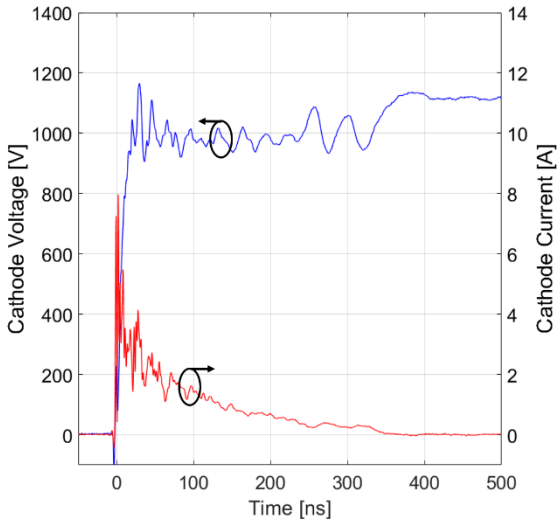

Figure 4 – Experimental device [6] HBM-ESD test waveforms.

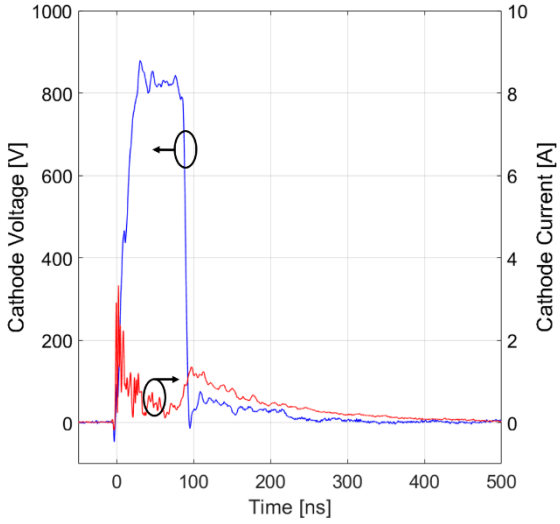

Figure 5 – Experimental device [9] HBM-ESD test waveforms.

As an example, in Fig. 5 the electrical waveforms are reported for device [9] that fails for V_{TEST}=1.5kV. Standard HB-ESD testers only give the maximum test voltage, while the developed tester allows an accurate characterization of the device even when it fails.

CONCLUSION

In this work, the development and validation of a custom HBM-ESD tester has been presented, for a test voltage up to 7 kV. The main advantage of the developed setup in the possibility to measure the electrical waveforms during the test, giving a further insight into the investigation of the failures. Some measurements are presented to show the capability of the setup.

REFERENCES

[1] Riccio, M., et al. "Impact of gate drive voltage on avalanche robustness of trench IGBTs." Microelectronics Reliability 54.9-10 (2014): 1828-1832.
[2] *Maresca, Luca, et al. "Novel Cathode Design to Improve the ESD Capability of 600 V Fast Recovery Epitaxial Diodes." Energies 11.4 (2018): 832.*
[3] https://www.jedec.org/document_search?search_api_views_fulltext=JS-001-2017.

DOI: https://doi.org/10.14311/ISPS.2021.019

[4] Commercial device RFUH20.
[5] https://www.thinksrs.com/downloads/pdfs/manuals/PS365m.pdf.
[6] Commercial device BYR29X.
[7] Irace, Andrea, et al. "200 V Fast Recovery Epitaxial diode with superior ESD capability." Microelectronic Reliability 64 (2016): 440-446.
[8] Riccio, M., et al. "Cell pitch influence on the current distribution during avalanche operation of Trench IGBTs: design issues to increase UIS ruggedness." 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD). IEEE, 2014.
[9] Commercial device E20ED1.

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