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Power device solutions for highly efficient power supplies

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Abstract

Switched mode power supplies (SMPS) for target applications covering a wide range from telecom rectifiers through servers to solar inverters or electric vehicle chargers share the need for high efficiencies in order to minimize the overall energy consumption and the total cost of ownership. With the appearance of wide bandgap semiconductors designers cannot only choose between different devices but also may benefit from using advanced topologies. This work compares important properties of a CoolSiC™ Silicon-Carbide MOSFET, a CoolGaN™ E-mode GaN power transistor, a TRENCHSTOP 5™ IGBT accompanied by a SiC Schottky diode and a CoolMOS™ Superjunction (SJ) device, and discusses an approach to avoid the limitations of SJ devices with respect to hard commutation of the body diode and evaluates the achievable efficiency in the AC-DC conversion stage of a power supply.

Keywords: power semiconductor, super-junction, wide bandgap, MOSFET, IGBT, SMPS

INTRODUCTION

The investigated four device technologies with a voltage rating of 600 V to 650 V differ substantially in their device structure in order to benefit most from the respective semiconductor material. Examples of the fundamental device structures are shown in Fig. 1 in order to explain the basic device properties [1-4]. The SJ- and the SiC-MOSFET are both vertical structures. However, the purpose of the incorporated p-regions in the vertical structure is different. While the SJ p-columns provide charge compensation to optimize the trade-off between low on-resistance and high breakdown voltage, the buried p-region of the SiC-MOSFET limits the electric field at the gate oxide to maintain the required oxide lifetime. Both devices have the drain on the backside. The IGBT is also a vertical but bipolar device with a backside pn-junction that provides the carriers for conductivity modulation in the drift region. The SiC device requires a roughly ten times smaller drift region length compared to the IGBT or SJ MOSFET, enabling both a strongly reduced area-specific on-resistance $R_{DS(on)}$ and small reverse recovery charge Q_{RR}. In contrast, the GaN device consists of a lateral structure placed on a (not shown) Silicon substrate. The Silicon backside is electrically isolated but typically tied to the source potential. The GaN device is based on the heterojunction High Electron Mobility Transistor (HEMT) structure and does not contain physical pn-junctions between source and drain. Instead, the channel builds through a highly conductive two-dimensional electron gas (2DEG) at the AlGaN/GaN interface. A recessed, non-isolated p-GaN gate is provided for local interruption of the 2DEG to achieve a normally-off (E-mode) device. This GaN transistor can be operated as a power switch or also as a diode in the reverse direction with practically zero reverse recovery charge Q_{RR}.

APPLICATION REQUIREMENTS

Fig. 2 shows the main building blocks of a power supply designed for a universal input voltage range of 85 – 265 VAC. The compared devices are intended for use in the AC-DC conversion power factor correction

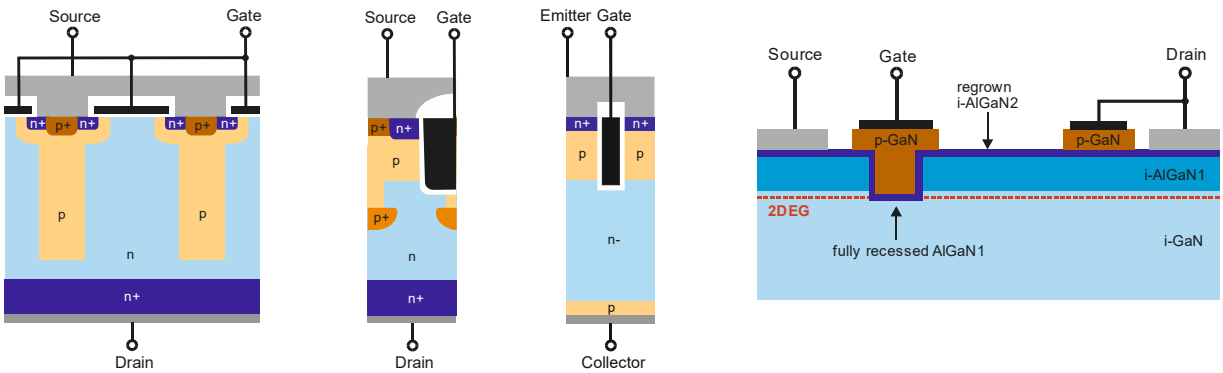

Fig. 1: Exemplary device structures: SJ-MOSFET [1], SiC-MOSFET [2], IGBT [3], E-mode GaN Power Transistor [4]

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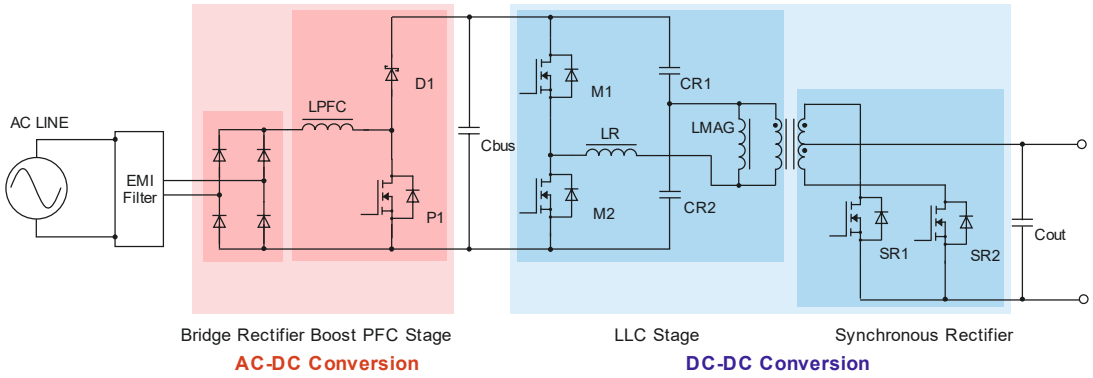

Fig. 2: Main building blocks of a power supply

(PFC) stage. The different device properties require the use of different topologies.

The PFC stage as shown in Fig. 2 employs a common Boost PFC topology as typically used with SJ devices. The typical operating frequency is limited to 70 kHz to keep the fundamental and second harmonics below 150 kHz due to EMI reasons. A higher operating frequency also clearly increases the switching losses. The typical control mode is the Continuous Conduction Mode (CCM) as here the ripple current losses and switching losses are well balanced. The PFC stage may also be operated in Discontinuous Conduction Mode (DCM) or Critical Conduction Mode (CrCM) at the cost of a much higher ripple current while at the same time enabling quasi Zero Voltage Switching (ZVS) for reduced switching losses. However, the input bridge rectifier is the dominant source of losses and is responsible for an efficiency loss of between 1 %…2 %. The switching losses of the transistor P1 strongly depend on the energy stored in the output capacitance; consequently it is good to use devices with low E_{OSS} values here. To achieve a higher efficiency, the use of a Dual Boost PFC stage is possible [5,6]. As shown in Fig. 3, the higher efficiency is paid for with a higher effort on the system side. To gain an even higher efficiency, one could replace the input diodes D3 and D4 by SJ MOSFETs working as synchronous rectifiers. This further minimizes the conduction losses, but the overall system effort and control complexity becomes even higher. Another topology offering comparable efficiency is the H4 PFC [5].

A better-suited topology is the Totem Pole PFC as depicted in Fig. 4 [7]. This bridgeless topology eliminates the need for traditional bridge rectifiers which contribute substantially to the overall losses in the PFC stage. While being a rather simple topology, the Totem Pole PFC is intrinsically capable of providing a bi-directional power flow and provides the highest practically achievable efficiency. However, this topology imposes serious challenges for the power semiconductors. The switching frequency of the power semiconductors WBG1 and WBG2 is relatively high with values of up to 100 kHz, with one transistor working as a boost switch and the other as a synchronous rectifier. The Totem Pole usually operates in Continuous Conduction Mode (CCM), however other control modes including DCM or CrCM may also be employed [8]. In any case, this topology requires devices with low values of reverse recovery charge Q_{RR} to enable the repetitive hard commutation operation of a conducting body diode. The output capacitance dependency on the drain voltage must avoid sharp drops, in addition a low output charge Q_{OSS} is needed to facilitate short dead times and to enable higher switching frequencies. This low output charge together with a small value of E_{OSS} helps to achieve high efficiencies. Wide bandgap devices provide all these properties and are a perfect match for this topology.

IMPACT OF DEVICE TECHNOLOGY ON THE DEVICE PARAMETERS

Thermal Considerations

Being wide-bandgap semiconductor devices, the chip area for SiC and GaN devices of a given on-resistance is several times smaller than for a silicon device. A smaller area leads to an increase in the thermal resistance from junction to case R_{thJC}. SiC is advantageous in terms of its much higher thermal

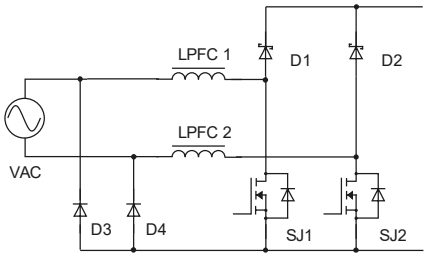

Fig. 3: Dual Boost PFC stage

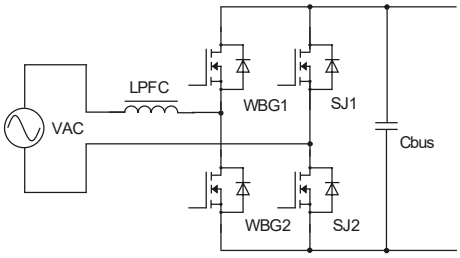

Fig. 4: Totem Pole PFC stage

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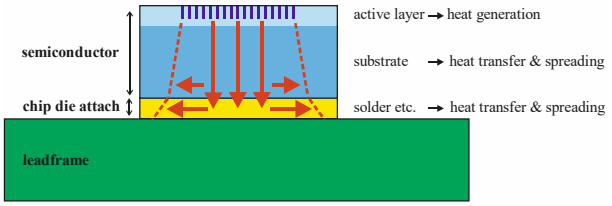

Fig. 5: Simplified illustration of heat flow (red arrows) and heat spreading (dashed lines) in the power device

conductivity of 360 W/m K compared to 150 W/m K for the other two devices. This better thermal conductivity largely compensates the increased R_{thJC} value due to the reduced chip area. The GaN device is limited here by the thermal conductivity of the Silicon substrate. As it is a lateral device, the chip area is larger compared to a SiC MOSFET. Still, this cannot fully compensate for the increased thermal resistance, and a good thermal design becomes crucial. A higher thermal conductivity is also beneficial for the lateral heat spreading within the chip itself as illustrated in Fig. 5 for two reasons: Firstly, the heat is only generated in the active area of the chip and not in the surrounding inactive parts (like the edge termination). Secondly, the heat is not generated over the full thickness of the semiconductor die. Instead, almost all of the power dissipation occurs within the active region of the device. Its thickness depends on the properties of the semiconductor material. Wide bandgap semiconductors require much less thickness here than Silicon. Also the die attach from the chip to the lead frame plays a significant role. The use of a traditional soft solder process introduces a solder layer with a thickness of up to 120 µm. This increases the thermal resistance from junction to case and limits the thermal performance especially for smaller chips. Diffusion solder processes [9] enable much thinner layers for the die attach and, in addition, the use of thinner semiconductor substrates. All these factors can reduce the thermal resistance R_{thJC}.

Temperature dependence of on-resistance

The temperature dependence of the on-resistance, shown in Fig. 6, indicates major differences between the investigated device technologies. The SiC-MOSFET shows the smallest increase with junction temperature T_J. From an application point of view, this small increase with temperature offers a benefit. It means that if all devices come with an identical $R_{DS(on)}$ at the datasheet condition of 25 °C, the on-state resistance for the typical operation junction temperature of 100 °C of the silicon SJ device is 45 % higher and for the GaN device it is 25 % higher than for the SiC MOSFET.
Considering the thermal behavior discussed before and the junction temperature dependence of the on-resistance, the SiC device and the IGBT show the best overall performance. To give an example, a CoolMOS CFD7 57 mΩ device operated at a temperature of 100 °C could ideally be replaced by a 62 mΩ CoolGaN device or by a 84 mΩ CoolSiC part. An appropriate selection of the device on-resistance at the targeted operation temperature is key to enabling cost savings and achieving substantially lower dynamic losses.

Transfer Characteristics

Another aspect that needs to be considered is the proper choice of the gate drive voltage. While the CoolSiC devices can generally be used with the same standard gate drivers as CoolMOS parts, this is not recommended due to differences in the transfer characteristics.
Fig. 7 compares the transfer characteristics for all technologies at temperatures of 25 °C and 150 °C. The CoolMOS device reaches its full current capability with gate voltages of V_{GS} = 10 V while the IGBT is still far from saturation The characteristics of the CoolSiC device shows a lower transconductance and the use of higher gate voltages gives a benefit as the on-resistance reduces. So it is recommended that a gate drive voltage of V_{GS} = 18 V is used for CoolSiC devices.
The further comparison of the different transfer characteristics depicted in Fig. 7 indicates that the impact of junction temperature is lowest for the IGBT and the CoolSiC part. In contrast, the CoolGaN devices reach the required current capability at much lower gate voltages due to the low typical achievable threshold voltage of 1.2 V. To gain immunity against unwanted parasitic turn-on, a negative gate voltage of down to V_{GS} = -5 V should be considered for use of these parts in hard-switching totem-pole configurations.

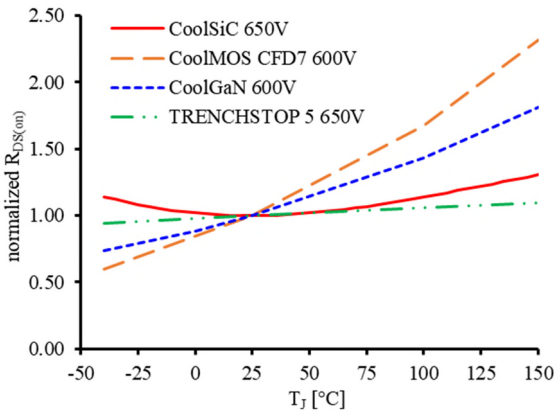

Fig. 6. Normalized temperature dependence of $R_{DS(on)}$ for the different device technologies

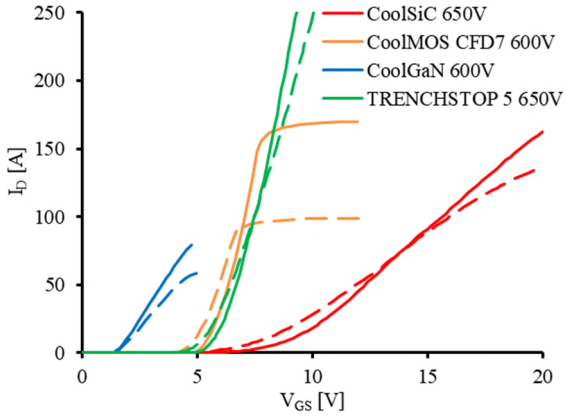

Fig. 7: Transfer characteristic comparison at two temperatures (solid lines – 25 °C, dashed lines – 150 °C)

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Device breakdown

Due to the differences in the properties of the semiconductor materials and the device structures, also the drain-source breakdown behavior differs.
In the case of the two MOSFETs and the IGBT, the breakdown mechanism is due to impact ionization at a pn-junction once the electric field in the device structure exceeds the critical electric field strength. The breakdown voltage is temperature dependent and governed by the impact ionization rates that reduce at elevated temperatures, therefore the breakdown voltage increases with temperature. Fig. 8 compares the temperature dependent breakdown voltages of the silicon and silicon-carbide devices, indicating a stronger dependence for the silicon part. From an application point of view, the higher breakdown voltage at low temperatures for the CoolSiC and IGBT devices is beneficial for usage in outdoor applications or if devices need to start up at lower temperatures.
In the case of the GaN device, the breakdown mechanism is different due to the device structure [10]. The breakdown is not limited by the critical electric field of the semiconductor but by the dielectric strength of the surface materials in the lateral GaN HEMT structure. The breakdown mechanism is a dielectric breakdown similar to the one found in ceramic capacitors. This behavior requires a destructive failure limit that must be at least 50 % larger than the maximum rated peak voltage of the device in order to safely avoid device degradation. This different breakdown behavior as well as the much higher breakdown voltage are clearly visible in the breakdown characteristics as depicted in Fig. 9. In contrast to the MOSFET and IGBT devices, the CoolGaN device shows an exponential current increase.

Forward voltage of body diode

There are significant differences in the body diode conduction between the device technologies. The CoolMOS and CoolSiC devices both incorporate an intrinsic pn-diode structure as is usual for a power MOSFET. Nevertheless, the forward voltage of the SiC

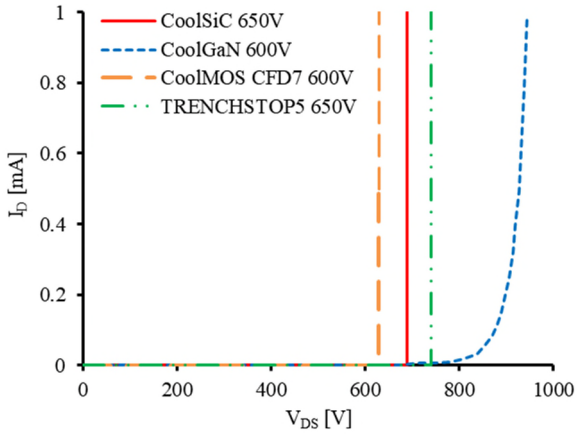

Fig. 9: Breakdown characteristics for the different device technologies at room temperature

device is around four times higher than that of the silicon MOSFET due to the wide bandgap of the silicon-carbide material. The forward voltage V_F shows a negative temperature coefficient for both materials. Due to the larger conduction losses of the CoolSiC body diode it is not efficient to use the intrinsic diode to conduct current over long periods of time. The impact on the light-load efficiency in an LLC converter can be as big as 0.5 %. As such it is recommended to limit body diode conduction to dead-time operation and employ synchronous rectification to limit the body diode conduction losses. Synchronous rectification has the additional benefit that the positive temperature coefficient of $R_{DS(on)}$ supports current sharing.
The IGBT does not contain an intrinsic body diode and requires a separate freewheeling diode. The IGBT is accompanied by the latest SiC Schottky diode technology [11] that comes with the lowest forward voltage V_F currently available in this voltage class.
In the case of the CoolGaN device, the structure does not incorporate an intrinsic diode structure. However, with the gate driven to the on-state, the GaN HEMT will conduct current equally well in either direction. If the gate is turned-off at $V_{GS} = 0$ V and the drain potential exceeds the gate threshold voltage, the HEMT structure turns-on and begins conducting in the reverse direction with a voltage drop of about 2 V. Applying a negative

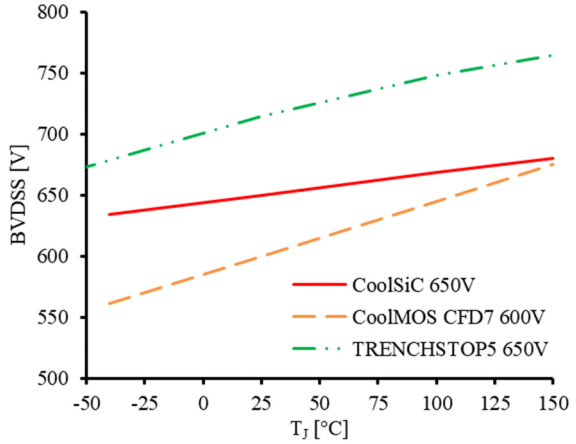

Fig. 8: Comparison of temperature dependence of breakdown voltage for CoolMOS, CoolSiC and IGBT devices

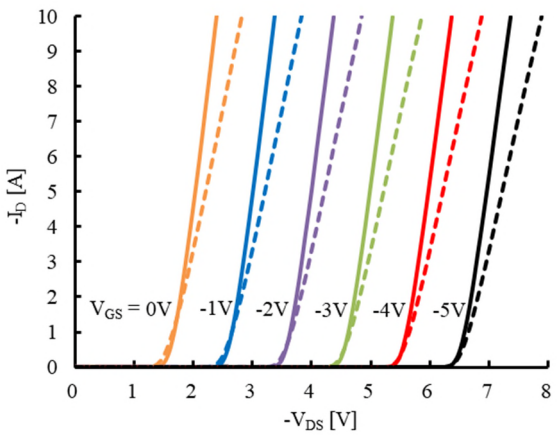

Fig. 10: CoolGaN 3rd quadrant characteristics at two temperatures (solid lines – 25°C, dashed lines – 125°C)

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gate-source voltage will shift the onset of reverse conduction appropriately and the "diode-like" voltage drop increases as depicted in Fig. 10. Consequently one should also limit this "diode-like" conduction mode to a brief period during the dead time between switching intervals as in the case of SiC devices.

Gate drive considerations

The gate drive requirements are practically identical for SJ- and SiC-MOSFETs and IGBT, however the SiC device benefits a lot from a higher $V_{GS} = 18$ V. The GaN device is a gate injection transistor (GIT) and the required gate-driving scheme differs significantly. Different to all other devices, the CoolGaN device has a non-isolated gate with a pn-diode between gate and source. The forward voltage V_F of 3.0 … 3.5 V is defined by the GaN band structure. It is evident that the V_F must always be higher than the threshold voltage of the transistor, which is ensured by the comparably low achievable threshold voltage of GaN devices. However, it is this gate diode that requires a different driving scheme compared to devices with insulated gates.
As for any MOSFET, the switching speed depends on the gate current available in the Miller plateau phase. In the case of a GaN device with a non-isolated gate, a permanent current I_{SS} will flow into the gate diode during the on-state, see Fig. 11. As this current causes additional losses, it should be kept as small as possible. However, gaining low switching losses requires large peak currents I_{ON} and I_{OFF} in the transition phases. To achieve this, the classic gate resistor is substituted by a RC network that provides two parallel branches as depicted in Fig. 12. Here, a small resistor R_{on} is coupled to the gate via the capacitor C_C while a large resistor R_{ss} provides the direct current path for the stationary on-state. The capacitor C_C provides the required charge to drive the transient current I_{on} defined by the value of the resistor R_{on}, assuming properly dimensioned values of the parts [12]. If the device is turned off, the gate-drive voltage level shifts to negative values again due to the capacitor C_C. This guarantees a fast turn-off transient and the avoidance of a potential re-turn-on.

Capacitances and Charges

Fig. 13 - Fig. 16 compare the output capacitance, the output charge, the energy stored in the output capacitance, and the gate charge of the different

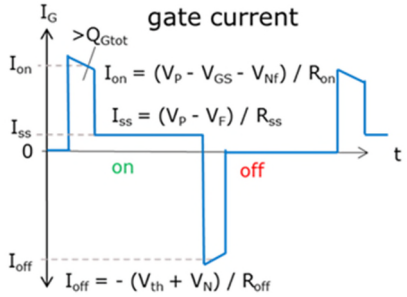

Fig. 11: Driving scheme of the GaN Power Transistor

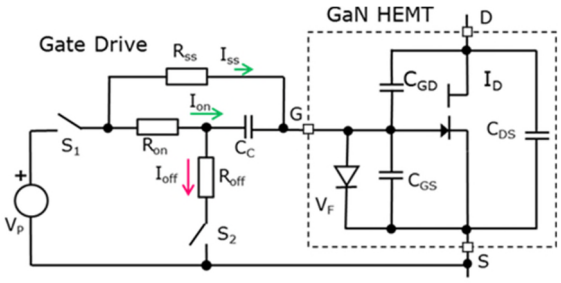

Fig. 12: Equivalent circuit to properly drive the gate of the GaN Device

technologies using devices with a comparable on-resistance of 50 - 55 mΩ at nominal current and room temperature (e.g. for normal datasheet conditions). With respect to the output capacitances as shown in Fig. 13, the CoolMOS technology offers a smaller output capacitance than the other devices at $V_{DS} > 24$ V. Therefore, the CoolMOS is capable of offering lower switching losses in a standard boost PFC application. However, the CoolMOS shows a more sensitive behavior to PCB and design related parasitic elements as well as larger V_{DS} overshoots during turn-off. At drain voltages larger than 24 V, the output capacitances of the SJ-MOSFET and the GaN device are almost identical. However, the lower output capacitances of the GaN and SiC MOSFET and the IGBT below $V_{DS} = 24$ V represent a clear benefit as it allows an overall faster transition of the drain voltage. GaN offers the lowest C_{OSS} values below $V_{DS} = 24$ V which translates into a lower output charge Q_{OSS} and a lower E_{OSS} of the GaN transistor as indicated in Figs. 14 & 15.
In terms of output charges, both wide bandgap devices offer a clear benefit over the SJ MOSFET. The lower Q_{OSS} value allows either the discharge of the output capacitance with a lower re-circulating current or the minimization of the dead time. Short dead time settings are important in conjunction with wide bandgap devices in order to minimize body diode conduction losses related to a forward voltage drop which is four times higher than the CoolMOS device. As shown in Fig. 15, CoolSiC has a higher E_{OSS} than CoolMOS and CoolGaN technology. The E_{OSS} represents the minimum energy that translates into switching losses in standard hard switching topologies. However, the large output charge together with the dramatically larger reverse recovery charge of SJ devices usually prevents these devices from being used in hard-switching bridge topologies such as in a Totem Pole.
Fig. 16 compares the gate charge characteristics at a drain current of ~9 A as typically used in the targeted application. Lower overall gate charge values result in lower driving losses at higher switching frequencies and enable higher efficiencies in light-load operation. Here the SiC-MOSFET shows a clearly smaller value than the CoolMOS and IGBT devices, nevertheless the difference gets smaller if the SiC device is driven with the recommended on-state gate voltage of $V_{GS} = 18$ V.
In comparison, the gate charge of the CoolGaN device is substantially smaller, acting as an enabler for high-frequency applications. However the losses due to the

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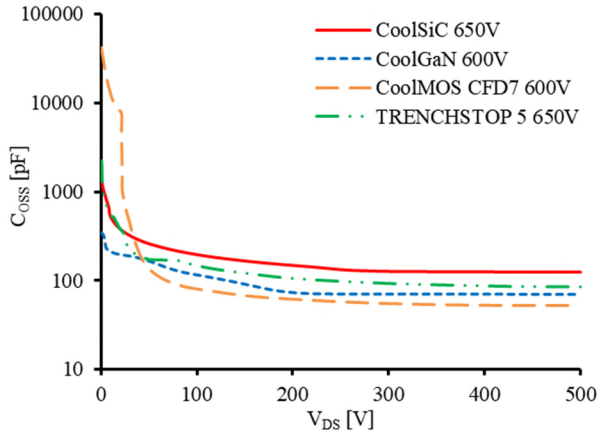

Fig. 13: Comparison of the output capacitances

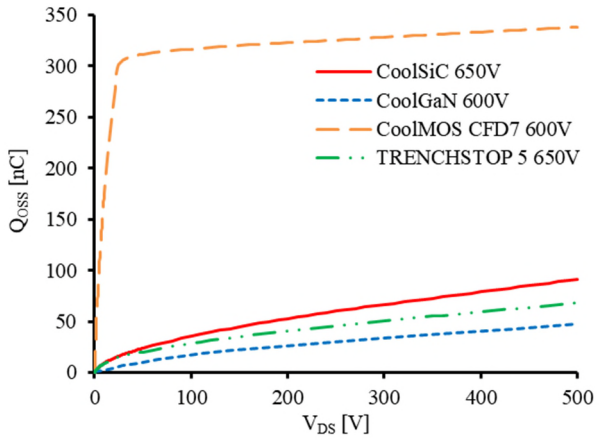

Fig. 14: Comparison of the output charges

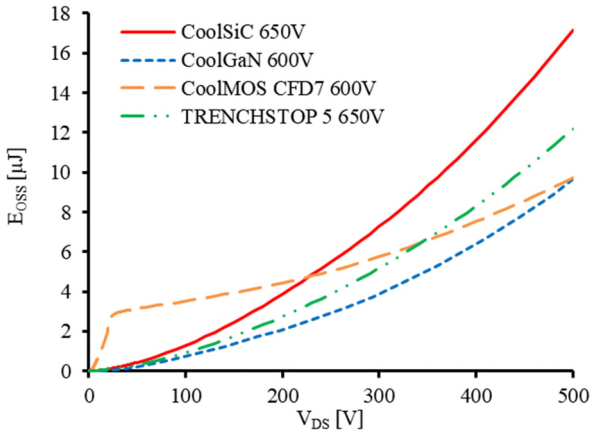

Fig. 15: Comparison of the energies stored in output capacitance

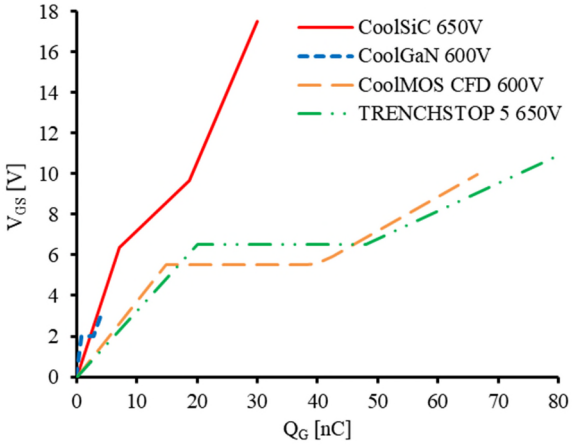

Fig. 16: Comparison of the gate charges

stored energy in the output capacitance E_{OSS} remain at comparable levels to other device technologies. A high-frequency operation will be most efficient in soft-switching or resonant topologies.

Reverse Recovery Charge

The reverse-recovery charge Q_{RR} is a very important factor for highly efficient hard-switching topologies like the CCM Totem Pole PFC discussed in this work. This charge builds-up during conduction of the intrinsic body diode of Si and SiC MOSFET devices and needs to be removed during hard commutation of the body diode. The amount of charge generated depends on internal device properties like doping profiles, thickness of the drift layer or carrier lifetimes as well as on external conditions controlled by the application such as current density, temperature or the conducting time of the body diode. The part of this charge that does not recombine during the body diode commutation must be removed by the reverse-recovery current and represents the reverse-recovery charge.

In the case of the CoolMOS CFD7 technology, the amount of stored charge was significantly reduced by a factor of 10 over the standard CoolMOS technology. Still, the stored charge Q_{RR} remains too large to allow the direct use of the device in the CCM Totem Pole PFC. This is very different for the SiC MOSFET. Being a wide bandgap device, the drift region thickness required for the targeted blocking voltage is much smaller. Also the active area is clearly reduced compared to even the best Superjunction MOSFET. Due to the dramatically reduced volume of the drift region, the amount of stored charge in the device becomes significantly smaller, which is further supported by the short carrier lifetimes in SiC. A low stored-charge also supports an improved robustness in hard commutation, as the risk of a snap-off at high reverse-recovery currents is much lower.

Fig. 17 compares the reverse-recovery waveforms of all three technologies, clearly indicating the much higher stored charge within the CoolMOS device, although a 50 % lower forward current was running through the device. The CoolGaN part does not actually generate any reverse-recovery charge because the device does not contain an intrinsic bipolar diode. As discussed before, the structure conducts in the third quadrant due to an open channel. Consequently, the “reverse-recovery” current here is purely capacitive and driven solely by the output charge of the device. This is also valid for the IGBT accompanied by the SiC Schottky diode. Being a unipolar device, the SiC Schottky device

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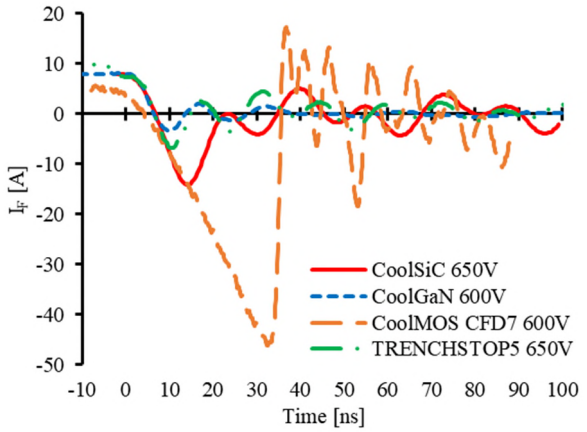

Fig. 17: Comparison of reverse-recovery current waveforms

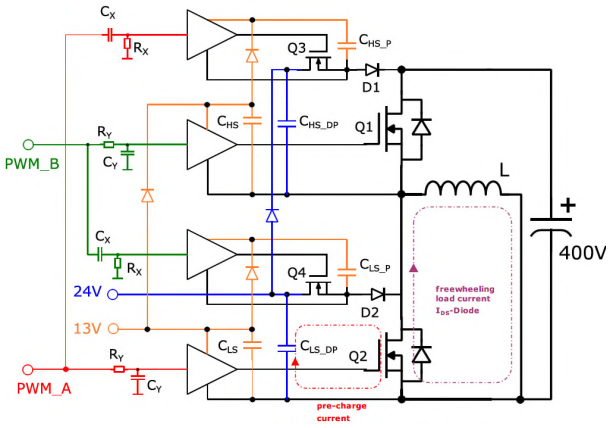

Fig. 18: Schematic of the pre-charging circuitry for the use of CoolMOS devices in a half-bridge configuration [15]

does not build-up a bipolar charge and commutation losses are again related only to the output charge, explaining the lower Q_{RR} of the SiC MOSFET.

PRE-CHARGING OF THE SJ DEVICE

It is not possible to use SJ MOSFETs in a half-bridge configuration in CCM operation due to the high output charge Q_{OSS} and the significant reverse recovery losses of the intrinsic body diode. There are several proposals that try to tackle this issue [13,14], but these solutions suffer from the use of extra switches and magnetics which limit the performance and power density.
However, the output capacitance and output charge characteristics of the SJ device as shown in Fig. 13 and Fig. 14 indicate that the major part of the linked losses are generated within a relatively small voltage range. If the output capacitance could be pre-charged to this respective voltage level, for example to 24 V, the commutation losses due to the output charge Q_{OSS} and reverse recovery charge Q_{RR} would dramatically reduce.

[15] describes such a solution that avoids the utilization of additional inductors and instead provides the previously discussed current into the switching node from a low-voltage source. This approach pre-charges the output capacitance of the SJ device operating in diode mode to a certain level. This enables the use of the SJ MOSFET in the Totem Pole PFC with normal CCM operation.
Fig. 18 depicts this implementation within a common half-bridge solution that reflects the situation in the Totem Pole PFC operating in CCM mode with hard commutation of the body diode. This pre-charge solution requires one high-voltage Schottky diode (D1, D2) and a low-voltage (LV) MOSFET (Q3, Q4) per device in the half-bridge and two separate supply voltages to drive the LV-MOSFET and provide the pre-charge voltage. This solution implements a level-shifting technique using bootstrap capacitors with traditional drivers for both the driver power supply (highlighted in orange) and the depletion voltage (highlighted in blue). The additional filter networks at the driver inputs, provided by C_X-R_X and C_Y-R_Y, allow the proper timing of the PWM signals to both the half-

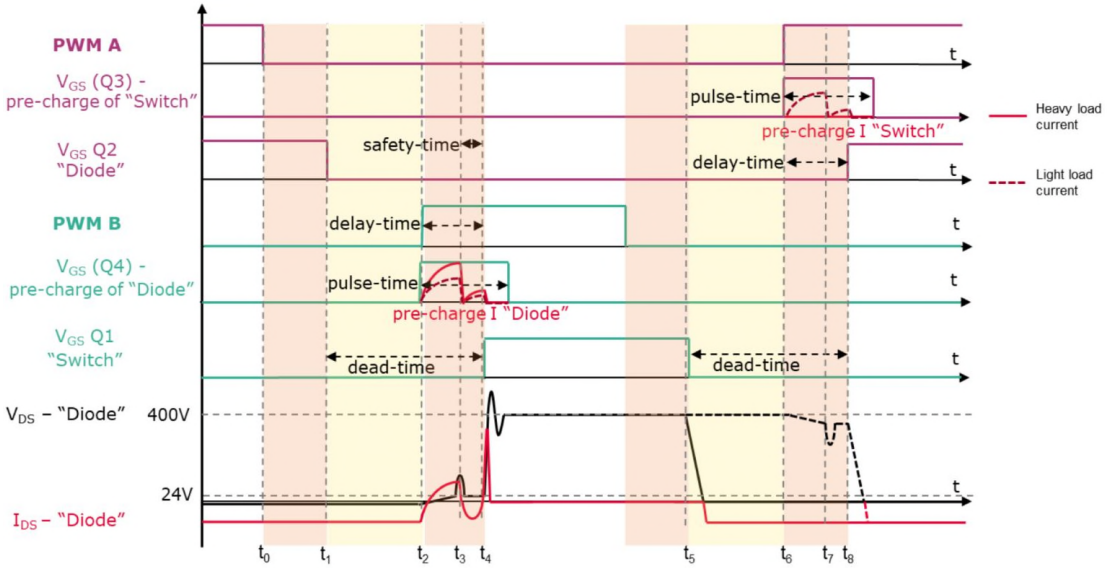

Fig. 19: Commutation waveforms of the pre-charge solution [15]

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bridge devices and the added LV switches. This avoids the need for extra PWM control signals from the controller.

Fig. 19 shows the commutation waveforms of the pre-charge solution to indicate the intended effects of this approach. As can be seen, the C_X-R_X network at the input of the gate driver of Q4 generates a pulse that turns-on the pre-charging MOSFET Q4 at t_2. This results in a pre-charging current (I "Diode") circulating through Q2, Q4, D2 and C_{LS_DP}. At the end of the pre-charging period at t_3, the body diode of Q2 is deactivated and the drain-source-voltage of Q2 is pre-charged to 24 V. This sets the stage for a smooth diode-to-switch transition, avoiding the otherwise high losses due to Q_{OSS} and Q_{RR} as Q2 is already depleted to 24 V.

As depicted in Fig. 19, the pre-charge current has a second peak between t_3 and t_4 that originates in the resonance of the output capacitance with the stray inductances of the pre-charging loop. A detailed description of the hard-commutation transition and the design of the pre-charge circuit is found in [15].

EFFICIENCY COMPARISON

The performance of the different devices is evaluated in the PFC stage of 3.3 kW power supplies. For the purpose of this comparison, the SJ devices are used with a Dual Boost PFC stage whilst all other devices are used in a Totem Pole topology:

- CoolSiC Trench MOSFET with $R_{DS(on),typ}$ = 48 mΩ in a Totem Pole PFC
- CoolGaN E-mode HEMT with $R_{DS(on),typ}$ = 33 mΩ in a Totem Pole PFC
- CoolMOS CFD7 with $R_{DS(on),typ}$ = 37 mΩ pre-charged in a Totem-Pole PFC
- TRENCHSTOP 5 IGBT and SiC Schottky Diode with equivalent $R_{DS(on),typ}$ = 54 mΩ in a Totem Pole PFC
- CoolMOS P7 (2x) with $R_{DS(on),typ}$ = 26 mΩ in a Dual Boost PFC
- CoolMOS CFD7A with $R_{DS(on),typ}$ = 41 mΩ in a Classic Boost PFC

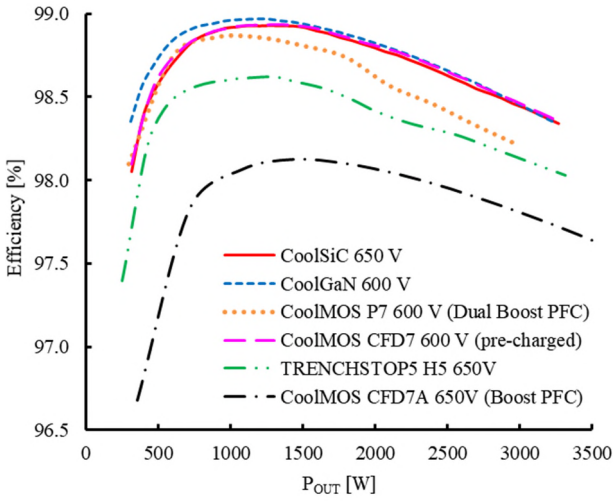

Fig. 20: Comparison of the absolute efficiency achievable in the respective 3.3 kW PFC stage (CoolSiC, CoolGaN, IGBT and pre-charged CoolMOS measured in Totem Pole topology, CoolMOS measured in Classic and Dual Boost topology, V_{IN} = 230 VAC, V_{OUT} = 400 VDC, f_{sw} = 45 – 65 kHz (Dual Boost PFC), f_{sw} = 65 kHz (Totem Pole & Classic Boost PFC))

The need to use different topologies for the different devices in combination with the need for varying gate drive schemes for MOSFET, IGBT and GaN devices makes a true performance comparison challenging. Consequently, the measurements were performed using different evaluation boards which introduces further uncertainties related to the different parasitic elements introduced by the different layouts.

However, the comparison shown in Fig. 20 reveals a clear trend of the capabilities of the different technologies. Both wide bandgap devices clearly enable higher efficiencies of around 99 % which is similar to the CoolMOS SJ device with pre-charging circuitry. The CoolGaN enables the highest peak efficiency but requires a significantly more complex driving scheme and hence more effort in the system design compared to the CoolSiC devices. The CoolMOS SJ device used in a Dual Boost configuration is capable of delivering a peak efficiency of 98.8 % but loses efficiency at high loads. The IGBT solution is capable of yielding a peak efficiency of almost 98.6 %, making this solution attractive for price-driven applications. In direct comparison with the efficiency delivered by a Classic Boost PFC representing the standard solution employed in most of today's power supplies, all alternatives offer a much better performance.

CONCLUSION

SJ devices in a standard boost PFC will remain the first choice for the PFC stage of a SMPS with an overall efficiency below 97 %. The devices are easy to drive, offer the most granular portfolio and offer a proven quality and reliability. Due to the higher output capacitance shape at V_{DS} > 20 V, wide bandgap devices do not offer clear advantages in this topology.

SiC MOSFET, GaN HEMT and pre-charged SJ MOSFET offer comparable solutions for SMPS with standard form factor and an efficiency range of 97 % to 98 %. This better efficiency is linked to the move to a Totem Pole topology and the elimination of the bridge rectifiers. The use of SJ devices in a Dual Boost PFC falls behind those solutions in terms of efficiency.

Although C_{OSS}, Q_{OSS} and E_{OSS} are all higher than for a GaN transistor, the SiC device clearly benefits from a much lower increase of on-resistance with temperature. The SiC MOSFET is easy to drive although it is recommended to use a gate drive voltage of 18 V to benefit from the further lowered $R_{DS(on)}$. SiC MOSFET are especially beneficial for high power applications. However, the application of a pre-charge circuitry with SJ devices could currently offer a more cost efficient solution for power levels beyond 3 kW.

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The combination of a fast IGBT and a SiC Schottky diode enables the use of IGBTs in the Totem Pole topology. This approach offers the best solution for cost-driven applications whilst still delivering peak efficiencies clearly beyond 98 %.
Solutions using GaN devices are currently capable of delivering the highest efficiencies, exceeding 98 % in standard form factor. They are the first choice for high frequency applications where the form factor is the key requirement. However, GaN solutions use a dedicated gate drive concept that requires additional effort for its implementation.

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REFERENCES

[1] Deboy, G. et al: A new generation of high voltage MOSFETS breaks the limit line of silicon, Proc. IEDM 1998

[2] Siemieniec, R. et al: 650 V SiC Trench MOSFET for high-efficiency power supplies, Proc. EPE 2019

[3] Kimmer, T. et al: Trenchstop™5 A new application specific IGBT series, Proc. PCIM 2012

[4] Amano, H. et al: The 2018 GaN power electronics roadmap, J. Phys. D: Appl. Phys., Vol. 51, No. 16

[5] Jang, Y. et al: A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization, IEEE Transactions on Power Electronics, 2009, Vol. 24, No. 1, pp. 85-93

[6] Huber, L., Jang, Y., and Jovanivić, M.M.: Performance Evaluation of Bridgeless PFC Boost Rectifiers, IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp.1381-1390, 2008

[7] Zhou, B.: CCM Totem-Pole Bridgeless PFC with Ultra-Fast IGBT, Master Thesis, Virginia Polytechnic Institute and State University, Blacksburg, USA, 2014

[8] Mohan, N., Undeland, T.M. and Robbins, W.P.: Power Electronics – Converters, Applications, and Design – 2nd Edition, John Wiley & Sons, USA, 1995

[9] Pürschel, M., and Röschlau, K.: Diffusion soldering for automotive power MOSFETs offers the first 100% lead free die attach, Proc. EPE, Birmingham, UK, 2011

[10] Persson, E.: CoolGaN™ application note. Infineon Technologies AG, Application Note AN_201702_PL52_010. Available at: https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs-AN-v01_00-EN.pdf?fileId=5546d46262b31d2e016368e4cab10701

[11] Draghici, M., Rupp, R., Elpelt, R., Gerlach, R. and Schörner, R.: A new SiC diode with significantly reduced threshold voltage, Proc. ISPSD, Sapporo, Japan, 2017

[12] Zojer, B.: Driving CoolGaN™ 600 V high electron mobility transistors. Infineon Technologies AG, Application Note AN_201702_PL52_012. Available at: https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs_Driving_CoolGaN_high_electron_mobility_transistors_with_EiceDRIVER_1EDI_Compact-ApplicationNotes-v02_00-EN.pdf?fileId=5546d46262b31d2e016368e4d7a90708

[13] Bellar, M.D., Wu, T.S., Tchamdjou, A., Mahdavi, J. and Ehsani, M.: A review of soft-switched DC-AC converters, IEEE Transactions on Industry Applications, 34, 4, 1998

[14] Irving, B.T., Jang, Y. and Jovanovic, M.M.: Implementation and performance evaluation of 100 kHz, soft-switched bidirectional PFC/inverter with silicon MOSFETs, Proc. APEC, San Antonio, USA, 2018

[15] Mora, R.A.G. et al: Lossless Hard-Commutated Operation of SJ MOSFETs and Application to CCM Totem-Pole Bridgeless PFC, Proc. PCIM 2021