THESIS SUPERVISOR'S REPORT

I. IDENTIFICATION DATA

Thesis title:	**FlexPRET real-time processor in heterogenous systems**
Author's name:	**Prasoon Dwivedi**
Type of thesis :	bachelor
Faculty/Institute:	Faculty of Electrical Engineering (FEE)
Department:	Department of Cybernetics
Thesis reviewer:	Ing. Martin Košťál, MSc.
Reviewer's department:	(37230) CIIRC - Industrial Informatics

II. EVALUATION OF INDIVIDUAL CRITERIA

Assignment — **challenging**

How demanding was the assigned project?

In the context of the student's branch of study, the assignment requires the student to learn a lot of theory and practical skills outside of the scope of the curriculum.

Fulfilment of assignment — **fulfilled with major objections**

How well does the thesis fulfil the assigned task? Have the primary goals been achieved? Which assigned tasks have been incompletely covered, and which parts of the thesis are overextended? Justify your answer.

The thesis shows well how to work with hardware described in Chisel HDL. Than, it describes well how the FlexPRET has been ported onto an FPGA, utilization of FPGA resources is shown in the appendix. The selection of TacleBENCH benchmark suite is presented well.

The thesis does not show benchmark results of the FlexPRET, only presents benchmark results of another real-time processor Patmos. A direct comparison of the two processors is missing.

Activity and independence when creating final thesis — **C - good.**

Assess whether the student had a positive approach, whether the time limits were met, whether the conception was regularly consulted and whether the student was well prepared for the consultations. Assess the student's ability to work independently.

The student exhibited a great degree of independence. Commitment to regular progress was lacking and is surfacing in deficiencies of the thesis.

Technical level — **E - sufficient.**

Is the thesis technically sound? How well did the student employ expertise in his/her field of study? Does the student explain clearly what he/she has done?

The thesis contains numerous author's personal opinions and comments, which might be suitable for fiction, but are not suitable for a technical text. Explanations are often vague or inherently incorrect, especially HDL description in chapter 2.1.3, ISA description in chapter 3.1, instruction types of Risc-V in 3.3. Description of Chisel language could be more detailed, the thesis does not explain clear advantages over what can already be achieved with Verilog using macros.

Formal level and language level, scope of thesis — **C - good.**

Are formalisms and notations used properly? Is the thesis organized in a logical way? Is the thesis sufficiently extensive? Is the thesis well-presented? Is the language clear and understandable? Is the English satisfactory?

The thesis is well organised, the page count is appropriate. The language level is exceptional and easy to read, but too informal sometimes. Chapter 6 Conclusion does not clearly conclude the thesis, and it is unclear what was achieved in the project.

CTU CZECH TECHNICAL UNIVERSITY IN PRAGUE

THESIS SUPERVISOR'S REPORT

Selection of sources, citation correctness **C - good.**
Does the thesis make adequate reference to earlier work on the topic? Was the selection of sources adequate? Is the student's original work clearly distinguished from earlier work in the field? Do the bibliographic citations meet the standards?
References are lacking in the theoretical part, i.e.: Based on what the author claims, that CLBs, IO and flash memory is typically less than 20% of FPGA silicon, in chapter 2.1.2? The selected references are good.

Additional commentary and evaluation (optional)
Comment on the overall quality of the thesis, its novelty and its impact on the field, its strengths and weaknesses, the utility of the solution that is presented, the theoretical/formal level, the student's skillfulness, etc.
The project tested the student's ability to learn a new HDL (Hardware Describtion Language) Chisel and ability to resolve various problems in porting. The selected benchmarks of TacleBENCH are a good choice for real-time benchmarking, as it standardises a wide range of tests and is open-source. Many papers present a carefully selected comparison with proprietary or custom benchmarks, which makes objective comparison harder or even impossible. The selected real-time processor Patmos for comparison with FlexPRET is good. A comparison with a commercially available real-time ARM cortex R series could have been even better.

III. OVERALL EVALUATION, QUESTIONS FOR THE PRESENTATION AND DEFENSE OF THE THESIS, SUGGESTED GRADE

Some objectives have not been accomplished. The quality of the technical writing and references is good. In my final grade, I emphasize the incomplete objectives of the project.

I have the following questions:

Can you explain what is Worst-Case-Execution-Time (WCET) and Execution-Time Jitter and how FlexPRET improves those metrics over a traditional processor?

What is the best- and worst-case interrupt latency of FlexPRET?

The grade that I award for the thesis is E - sufficient.

Date: 26.8.2021 Signature: