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Improvements in the Electrical Performances of MOSFETs in Integrated Circuits by Physical Mask Design

Doctoral Thesis

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Statement of Original Authorship

The work contained in this thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is made.

in Prague, ...

Dalibor Barri

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Abstract

At present, the criteria for ecology and vital environment protection are rigorous and must be respected. However, despite the established rules, our initiative can prevent potential life disasters, as it is in this doctoral thesis. Living in a healthy environment is essential for all of us, and therefore this thesis focuses on research into improvements in the electrical properties of integrated field-controlled transistors (MOSFET), which will ultimately reduce both environmental pressure and financial costs in the production of integrated circuits (IC). Reducing manufacturing costs and pressure on the environment is achieved by using smaller silicon wafer surfaces while retaining the original chip functionality. This is achieved by using the advanced diamond layout shape (DLS) gate pattern of MOS transistors (DLS MOSFETs) on the IC chip design that is subject of this thesis.

In this thesis, there are presented three innovative crucial knowledge of the DLS MOSFETs, such us novel analytical descriptions of the effective aspect ratio of DLS MOSFET, the way how to improve electrical performances of the MOSFETs, and the new precise model of the effective threshold voltage changes in the DLS MOSFETs. All these points are essential for the high-quality level design of integrated circuits with DLS MOSFETs and are defined for the first time in this thesis.

The new innovative approach of the effective aspect ratio calculation is based on the Schwarz-Christoffel (SC) transformation. It has been observed and proved by numerical calculations, 3D TCAD simulations, and measurements that the newly presented approach achieves much better results than already one existing method based on the longitudinal (parallel) corner effect (LCE) and parallel association of MOSFET with different channel length effect (PAMDLE). The measures have also demonstrated both the mentioned improvements and the effective threshold voltage changes in the DLS MOSFETs, respectively, where 1 124 samples in 160 nm BCD technology have been fabricated for this purpose.

Abstrakt

V současnosti jsou kritéria na ekologii a ochranu životního prostředí velmi přísná a je nezbytné je dodržovat. Avšak, i navzdory zavedeným pravidlům, vlastní iniciativou můžeme předcházet možným životním katastrofám, jako je tomu v této doktorské práci. Žít v zdravém životním prostředí je důležité pro každého z nás, a proto se tato práce zaměřuje na výzkum v oblasti vylepšení elektrických vlastností integrovaných polem řízených tranzistorů (MOSFET), která v konečném důsledku sníží, jak tlak na životní prostředí, tak i finanční náklady při výrobě integrovaných obvodů (IO). Snížení výrobních nákladů a tlaku na životní prostředí je dosaženo použitím menších ploch křemíkových desek při zachování původní funkčnosti čipu. Toho je dosaženo použitím pokročilých kosočtvercových topologií MOS tranzistorů (DLS MOSFETů) na integrovaném čipu, která jsou předmětem této práce.

V této práci jsou představeny tři zásadní inovativní znalosti týkajících se DLS MOS transistorů, kterými jsou: nové analytické popsání efektivního poměru stran DLS MOSFETů, navržené řešení jak zlepšit elektrické vlastností u MOSFETů a nový přesný model efektivních změn prahového napětí v DLS MOSFETech. Všechny výše zmíněné body jsou zásadní pro vysoce kvalitní návrh integrovaných obvodů s DLS MOSFETy a jsou prvně publikovány v této práci.

Nový inovativní přístup výpočtu efektivního poměru stran je založen na Schwarz-Christoffelově (SC) transformaci. V této práci je jak číselnými výpočty či 3D TCAD simulacemi, tak i měřením pozorováno a prokázáno, že nově prezentovaný přístup dosahuje lepších výsledků, než-li tomu je u jiného přístupu založeným na podélných paralelních rohových jevech (LCE) a paralelních asociaci MOSFETů s různou délkou kanálu (PAMDLE). Měření na reálných vzorcích také prokázala, jak zmíněné vylepšení, tak i změny efektivního napětí v DLS MOSFETech. Za tímto účelem bylo vyrobeno 1 124 vzorků v 160nm BCD technologickém procesu.

Keywords

diamond layout shape MOSFET (DLS MOSFET), electrical performance of MOSFETs in integrated circuit, MOSFET effective aspect ratio $(W/L)_{\mathrm{eff}}$, effective threshold voltage $(V_{\mathrm{th,eff}})$, rectangular layout shape MOSFET (RLS MOSFET), Schwarz–Christoffel transformation (SC transformation)

Klíčová slova

diamantový tvar rozložení MOS transistoru (DLS MOSFET), elektrický výkon MOSFETů v integrovaném obvodu, efektivní poměr stran $(W/L)_{\mathrm{eff}}$ u MOSFETů, efektivní prahové napětí $(V_{\mathrm{th,eff}})$, obdélníkový tvar rozložení MOSFET (RLS MOSFET), Schwarz–Christoffelova transformace (SC transformace)

"Creativity is intelligence having fun."
- Albert Einstein

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List of Abbreviations

Parameter	Unit		Description
2D	(-)	. . . . .	Two Dimensional
3D	(-)	. . . . .	Three Dimensional
A	(m^2)	. . . . .	Active channel area of MOSFET
B	(-)	. . . . .	Bulk terminal of MOSFET
CGAA	(-)	. . . . .	Cylindrical Gate-All-Around
C_{GD}	(F)	. . . . .	Gate-drain parasitic capacitance
C_{GS}	(F)	. . . . .	Gate-source parasitic capacitance
CMOS	(-)	. . . . .	Complementary MOS
C_{ox}	(F)	. . . . .	gate oxide capacitance
D	(-)	. . . . .	Drain terminal of MOSFET
DC-DC	(-)	. . . . .	Direct Current to Direct Current
DIBL	(-)	. . . . .	Drain-Induced Barrier Lowering
DLS	(-)	. . . . .	Diamond Layout Shape
DMOS	(-)	. . . . .	Drain extended MOS
DUT	(-)	. . . . .	Device Under Test
ELT	(-)	. . . . .	Enclosed-Layout Transistor
FEM	(-)	. . . . .	Finite Element Method
FOM	(-)	. . . . .	Figure-of-merit
G	(-)	. . . . .	Gate terminal of MOSFET
GAA	(-)	. . . . .	Gate-All-Around
GIDL	(-)	. . . . .	Gate-Induced Drain Leakage
GPS	(-)	. . . . .	Global Positioning System
HV	(-)	. . . . .	High Voltage
IC	(-)	. . . . .	Integrated Circuit
I_D	(A)	. . . . .	Drain current of MOSFET
ITRS	(-)	. . . . .	International Technology Roadmap for Semiconductors
k_B	($J\,K^{-1}$)	. . . . .	Boltzmann constant ($k_B = 1.38 \cdot 10^{-23}\,J\,K^{-1}$)
L	(m)	. . . . .	Length of MOSFET
LDDMOS	(-)	. . . . .	Low Doped Drain MOS
LOCOS	(-)	. . . . .	Local Oxidation of Silicon
LP	(-)	. . . . .	Low Power
LPEs	(-)	. . . . .	LCE+PAMDLE
MOS	(-)	. . . . .	Metal Oxide Semiconductor

MOSFET	(-)	. . . . .	MOS Field Effect Transistor
n_i	(ions m^{-3})	. . . . .	intrinsic doping concentration of silicon ($n_i = 1.45 \cdot 10^{10}$ cm^{-3})
N_{ch}	(ions m^{-3})	. . . . .	is a channel doping
N_A	(ions m^{-3})	. . . . .	acceptor impurity density in silicon
N_D	(ions m^{-3})	. . . . .	donor impurity density in silicon
NC	(-)	. . . . .	Negative Capacitance
PZT	(-)	. . . . .	Piezoelectric polycrystalline
O-CGT	(-)	. . . . .	overlapping circular-gate transistor
q	(C)	. . . . .	magnitude of the electron charge ($q = 1.602 \cdot 10^{-19}$ C)
R&D	(-)	. . . . .	Research and Development
RESURF	(-)	. . . . .	Reduced Surface Field
RF	(-)	. . . . .	Radio Frequency
RGT	(-)	. . . . .	Rectangular Gate Transistor
RHDB	(-)	. . . . .	Radiation Hardening by Design
RLS	(-)	. . . . .	Rectangular Layout Shape
S	(-)	. . . . .	Source terminal of MOSFET
SC	(-)	. . . . .	Schwarz-Christoffel
SCT	(-)	. . . . .	Schwarz-Christoffel Transformation
SG	(-)	. . . . .	Surrounding Gate
Si	(-)	. . . . .	Silicon
SoC	(-)	. . . . .	System-on-Chip
STI	(-)	. . . . .	Shallow Trench Isolation
T	(K,°C)	. . . . .	Temperature
TCAD	(-)	. . . . .	Technology Computer-Aided Design
t_{ox}	(m)	. . . . .	gate oxide thickness
TID	(-)	. . . . .	Total Ionizing Dose
VLSI	(-)	. . . . .	Very Large Scale Integration
V_{bi}	(V)	. . . . .	Built-in voltage of MOSFET
V_{BD}	(V)	. . . . .	Breakdown voltage of MOSFET
V_{BS}	(V)	. . . . .	Bulk-Source voltage of MOSFET
V_{GS}	(V)	. . . . .	Gate-Source voltage of MOSFET
V_D	(V)	. . . . .	Drain voltage of MOSFET
V_{DS}	(V)	. . . . .	Drain-Source voltage of MOSFET
V_{Dsat}	(V)	. . . . .	Drain saturation voltage of MOSFET
V_{DD}	(V)	. . . . .	Supply voltage
V_{FB}	(V)	. . . . .	Flatband voltage of MOSFET
V_{th}	(V)	. . . . .	Threshold voltage of MOSFET
$V_{th,eff}$	(V)	. . . . .	Effective threshold voltage of MOSFET

W	(m)	. . . . .	Width of MOSFET
(W/L)	(-)	. . . . .	Aspect ratio of MOSFET
$(W/L)_{\mathrm{eff}}$	(-)	. . . . .	Effective aspect ratio of MOSFET
x_{j}	(m)	. . . . .	Junction depth of MOSFET
α	(°)	. . . . .	Angle in diamond layout structure
γ	($V^{1/2}$)	. . . . .	body effect of MOSFET
ε_0	($F\ m^{-1}$)	. . . . .	vacuum permittivity, $\varepsilon_0 = 8.854 \cdot 10^{-12}\ F\ m^{-1}$
$\varepsilon_{\mathrm{ox}}$	($F\ m^{-1}$)	. . . . .	permittivity of oxide
$\varepsilon_{\mathrm{Si}}$	($F\ m^{-1}$)	. . . . .	permittivity of silicon
ε_{r}	(-)	. . . . .	relative permittivity of a material
ϕ_{p}	(V)	. . . . .	channel/bulk potential

Chapter 1

Introduction

1.1 Motivation

Nowadays, the criteria for ecology and vital environment protection are rigorous and must be respected. The 2030 Agenda for Sustainable Development [1] provided a clear direction that the world must aim to tread a more economically, socially, and environmentally sustainable path. Except for the other, the plan is focused on improving the life quality for everyone and protecting our environment [1]. Currently, there is also think about the area of resource extraction in outer space [2] because, in extremes cases, mining on Earth also has not a positive impact on vital environment and ecology.

The idea of a technology roadmap for semiconductors can be traced back to a paper [3] by Gordon Moore in 1965, in which he stated that the number of components that could be incorporated per integrated circuit would increase exponentially over time. This would result in a reduction of the relative manufacturing cost per function, enabling the production of more complex circuits on a single semiconductor substrate. Since 1970, the number of components per chip has doubled every two years. This historical trend has become known as “Moore’s Law”.

However, despite the established rules, our initiative can prevent potential life disasters, as it is in this work. Therefore, this work focuses on research into improvements in the electrical performances of integrated Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [4, 5], which will ultimately reduce both environmental pressure and financial costs in the production of integrated circuits. Reducing manufacturing costs and pressure on the environment is achieved by using smaller silicon wafer surfaces while retaining the original chip functionality. It can be achieved by using the advanced diamond layout shape of MOS transistors (DLS MOSFETs) in the integrated circuits [6 -8] such it is presented in this thesis.

Moreover, there is currenlty significant demand for analog high-frequency integrated circuits (ICs) with a chip area on a die as small as feasible [9]. This specific requirement can be realized by using DLS MOSFET as well. Typical applications of these ICs are for example DC-DC (Direct Current to Direct Current) converters for example in Bluetooth communication [10], touch-screen controllers in smart mobile phones [11], or power switches controllers in electronic fuses [12], where the key components should have the parasitic capacitance as small as possible. These parts include any analog circuit that switch-on/switch-off an analog control device. For example, it could be a power MOS (Metal Oxide Semiconductor) as a discharge device. In the switch-on/switch-off operation, there should be charged/discharged parasitic capacitance of the discharge devices. It has two impacts on applications. The first one is decreasing the maximal frequency of application systems for the specified current consumption. The operation cycle consumes additional electrical energy (e.g., from a battery of mobile phones) in each switching period. The next impact on applications is decreasing the lifetime of the mobile devices due to limited power energy in the battery, that is discharged by the switching frequency [13]. Into the category of mobile devices, we can sort devices such as (smart) mobile phone, (smart) watches, tablets, mobile GPS (Global Positioning System) devices, and so on.

Since the active area of the MOS Field Effect Transistor (MOSFET) has a direct influence on parasitic capacitance [14], the most effective way to improve these undesirable effects is to use different layout topologies that decrease the area of the MOSFET and keep or have better electrical performances. Moreover, the smaller active area of silicon dies allows to create smaller products, such as the smallest wireless sensor node for accurate cellular temperature measurement, which has just (360x400x150 μm) [15], or it opens market for the new applications such as electronic medical pills [16]. Considering the previous requirements, in this thesis is reported possibility how to satisfy the requirements.

Therefore, this thesis focuses on an exciting topic, which is how to improve the electrical performances of MOSFETs in integrated circuits by physical mask design. **For this goal: the precise innovative analytical description of the effective aspect ratio of DLS MOSFETs is described for the first time, the improvements in the electrical performances of the DLS MOSFETs have been calculated, simulated, and measured in 180 nm BCD technology process, and the precise model of the effective threshold voltage has been numerically approximated, simulated, and compared with the measured data.**

1.2 Thesis Outline

This thesis is divided into five chapters, the first of which is this short introductory chapter, which describes the motivations, aims of this thesis, author's scientific contributions and state of the art. Next, chapter 2 discusses the problems in the scaling of integrated circuits and reviews different MOSFET gate layout shape architectures. Following this, chapter 3 describes the design and methodology adopted by this research to achieve the aims and objectives stated in section 1.3 of Chapter 1. Chapter 4 reports all the innovative results achieved in this doctoral thesis, such as innovative analytical description of the effective aspect ratio of DLS MOSFET, improvements in the electrical performances of the DLS MOSFET by physical mask design, and the new precise model of the effective threshold voltage changes in the DLS MOSFETs. Finally, chapter 5 discusses the conclusions arising from the finding of this thesis and proposes future work.

1.3 Aims of This Thesis

The aim of this thesis is to investigate and describe the way, how to improve electrical performances of MOSFETs’ in integrated circuits. The main goals of this thesis are the following:

- Investigate how to improve electrical performances of MOSFETs’ in integrated circuits by physical mask design without complex structural modification.
- Develop and innovatively describe the lateral DLS MOSFET structure with better performance in comparison with the standard rectangular layout shape MOS transistor.
- Investigate and develop an innovative approach that analytically describes the effective aspect ratio of DLS MOSFETs.
- Define a new expression, which continuously describes the DLS MOSFETs in the whole range of DLS MOSFETs angles.
- Research the improvements in the electrical performances (the drain-source current) of the DLS MOS transistors by the analytical model, 3D-TCAD simulations and measurement on real silicon samples.
- Research and develop a new model of the interesting phenomenon related to the effective threshold voltage changes in the diamond layout shape MOS transistors.

All the above-mentioned goals are innovative, new, and never have been published before. These goals represent a possible new trend in semiconductor integrated circuits that improve MOS transistors' electrical performances, define a new methodology, and an innovative DLS MOSFET expression. The objectives further investigate and develop a new model of an interesting phenomenon related to effective threshold voltage changes in DLS MOS transistors.

1.4 Author's Scientific Contributions

The aims of this thesis are specified in the previous section of this Chapter 1, and the author's scientific contribution are highlighted in this part. The author's scientific contributions that have been achieved in this thesis are:

- **Analytical description of the effective aspect ratio of DLS MOSFETs**

  The new innovative analytical expression and methodology of calculating the effective aspect ratio of the MOSFET with the diamond layout shape gate pattern is described this thesis in section 4.1 for the first time. There has been used an innovative approach based on the conformal map function. As the conformal map function, the Schwarz-Christoffel transformation has been used. Both the new methodology and the new innovative analytical model, respectively, are described in section 4.1.2, verified with the 3-D TCAD simulations in section 4.1.3, and compared with the different methodology in section 4.1.4. The important results are described in section 4.1.5. All the mentioned results have been published in the impacted journal [6] **IEEE Transactions on Electron Devices, 2019, (Quartile 1).**

- **Improvements in the electrical performances of the DLS MOS transistors**

  The improvements in the electrical performances of the DLS MOSFETs are described in section 4.2 of this thesis for the first time. In sub-section 4.2.2, there is illustrated the theoretical drain-source current enhancement, and in the sub-section 4.2.3 is described the 3-D TCAD simulations of the drain-source current enhancement. Also, it has been measured on the real silicon samples fabricated in the BCD

160 nm technology process (section 4.2.4). All the theoretical, simulated, and measured data has been compared and summarized in section 4.2.5. The measurement results have been presented at an international conference [17] **IEEE Proceedings of the 25th International Conference on Applied Electronics, 2020**, and the complete data results have been published in the impacted journal [7] **IEEE Transactions on Electron Devices, 2020, (Quartile 1).**

- **Precise model of the effective threshold voltage changes in the DLS MOSFETs**

  The interesting phenomenon related to the effective threshold voltage changes in the diamond layout shape MOS transistors has been observed. This phenomenon has been analytically approximated by the new expression for the first time (section 4.3.3) and verified with the measured data in 4.3.4. All the important data are compared in section 4.3.5 and published in [8] **IEEE Transactions on Electron Devices, 2020, (under review, Quartile 1).**

1.5 State of the Art

Since 1971, the number of functional components (transistors, capacitors, etc.) per chip has exponentially increased (doubled practically every two years), and this historical trend was widely accepted by the chip fabrication community (International Technology Roadmap for Semiconductors – ITRS), as a Moor Law. The ability of the semiconductor industry to follow with the Moor's Law has been the engine of the strong cycle: transistor scaling delivers a better performance-to-price ratio, and it drives exponential growth in the semiconductor market. This, in turn, allows for further investment in semiconductor technologies that support further scaling. For example, software growth makes Moor's law possible. Why? Because people buy new hardware because the software requires it [18]. To remember, in 1971 Intel, that time not a well-known small company, released its first-ever microprocessor, the 4004. The chip, sized 12 mm^2, contained 2 300 transistors spaced by 10 µm gaps. To compare, the latest Intel IC product, the 10-core Intel® Core™ i7 64-bit Extreme Edition processor, being only about x10 larger than the 4004, provides incredible computing power, having several billion transistors at a spacing of 10–14 nm [19]. In the case of uses smaller technology nodes, there should be kept in mind the problems in technology scaling. Section 2.1 "Problems in Scaling" provides more details on this interesting and important topic.

The semiconductor IC's surface areas have been increasing, although there are opportunities to use the latest scaled-down technologies nodes with smaller and smaller surface areas of used IC functional components. This is because current and future ICs are becoming more complicated than they have been in recent years [20]. So, the higher complexity of the ICs thus leads to an increase in their total surface area. Of course, the increased surface area of ICs also increases the costs of the final products. Therefore, many research and development (R&D) centers are looking for ways, how to save the costs of the final products. The general solution of it is to reduce the surface area of the MOSFET, but the same or better electrical

performance should be maintained. As has been mentioned before, it can be achieved by using the proposed diamond layout shape MOS transistor which is the topic of this work.

Recent growth in the smart-power applications, wireless communication functionalities, mobile communication and other electronic systems in different CMOS technologies handling different functionalities like voltage regulation, signal conditioning, data conversion, and digital processing is one of the driving factors for advanced system-on-chip (SoC) solution [21–23] on the same silicon substrate. Accordingly, various subsystems, such as power management and RF (radio frequency) power amplifier, need to be fabricated using standard silicon process. However, exists other technologies using either GaN high-electron mobility transistors or SiC-based power MOSFETs due to their higher operation temperature, carrier mobility and breakdown voltage (V_{BD}) compared with silicon-based devices [24]. The integration of these GaN or SiC devices on the silicon substrate is not trivial [25]. Furthermore, difficulty in scaling of these compound semiconductor devices is also reported in [26]. Hence, for CMOS-based advanced SoCs, a Si-based design is still of interest and is discussed in this work. The following part summarizes the pros and cons of the current methods, how to get better MOSFETs performances for low voltage applications fabricated in CMOS technologies on silicon-based design.

In [27] is presented a solution, uses a negative capacitance (NC) as a universal digital and analog performance booster for complementary MOS transistors. A ferroelectric capacitor interconnecting with the gate stack of an MOS transistor creates a series connection and increases the total capacitance of the gate. In this approach, the gate stack is not a passive part of the transistor anymore and contributes to signal amplification. Specifically, the series structure brings an abrupt increase in the differential charge in the internal node by changing the gate voltage, thus providing a step-up voltage transformer [28, 29]. The ferroelectric performs two separate NC regions, demonstrating a zig-zag polarization

characteristic. This mainly happens due to the fact that the piezoelectric polycrystalline (PZT) is showing two main polarization domains and a multi-domain ferroelectric capacitor in steady states cannot hold more than one negative capacitance domain at a time [30, 31]. As a result, the manifested polarization characteristic of the multi-domain ferroelectric is different from the S-shaped curve which is expected for a single-domain ferroelectric. Thus, the drawback of this NC-FET is in the hysteretic behavior due to the NC effect. This is trade-off between the hysteretic behavior and the performance-boosting.

In [32, 33] are presented methods that improve DC and RF behavior of drift MOS transistors. The drift MOS transistor is a high-voltage device of which the fabrication process is compatible with the standard CMOS processing steps. In many publications, the authors use different names for the same structures. For that reason, this work will be synchronized according to the naming convention as follows:

- The LDDMOS (Lightly Doped Drain/Source MOS) is a MOSFET that has a lightly doped (N^-/P^-) drain (LDD) below a spacer oxide region between the drain (N^+/P^+) terminal and the gate [34]. That region is shorter in comparison to drain-extended MOSFET.
- The drift MOS is a MOSFET that has LOCOS, FOX or STI between drain and gate terminal [35, 36].
- The drain-extended MOSFET [37] is a MOSFET that has an extended long region between the drain (N^+/P^+) terminal and the gate. That region is low doped and like a region in LDDMOS, but there is necessary to have special one extended mask.
- The LDMOS is a lateral double diffused MOSFET, also known as the DMOS. This kind of MOSFET has a lightly-doped region below the source terminal known as a P_{body} for NLDMOS or N_{body} for PLDMOS [38].

The upper drift MOS transistors have been detailed analyzed with other high-voltage MOS structures such as drain-extended MOS devices in [39]. Drift MOS transistors can sustain high terminal breakdown voltages due to the reduced surface field (RESURF) action, which makes it suitable for high-power applications [40], high-voltage line drivers or level shifters [41]. However, in that paper is written: to have better performances of drift MOS transistors, it is necessary to reduce the electron density under the drain N^{+} concentration doping. It has been realized by increasing the diffusion length of the drain terminal. Thus, the total area of the improved drift MOS is bigger than the standard drift MOS transistor, and this is the drawback of this improvement. Moreover, the drift MOSFET area is greater in comparison to standard MOSFET, which is fabricated with the same primary mask set for not high-voltage applications.

Nowadays, there is also a trend to improve the electrical performances of silicon-based MOSFET transistors through various vertical trench topologies, such as the conventional trench MOSFET, double trench MOSFET or for example superjunction trench MOSFET [42]. The source and drain terminals of the vertical trench MOSFETs are located on the opposite sides of the chip wafer. For this reason, the vertical trench MOSFET can be realized as discrete components, and this is not within the scope of this work. These trench MOSFETs are useful for high-voltage applications where hundreds and thousands of volts are needed as a discrete component [43].

Another category leading to improved performances of MOSFETs uses superjunction (SJ) topology [44]. SJ MOSFETs can be realized in such vertical structure as well as lateral structures. The vertical SJ structure has consisted of multiple P^{-} and N^{-} columns (pillars) to allow a higher drift region (N^{-} columns for SJ N-LDMOSFET) doping concentration than conventional power MOSFETs. The highly doped N^{-} column directly reduces the specific on-resistance. As a charge compensation concept, the excess charge in the N^{-} column is counterbalanced by the adjacent charges in P^{-} column, and thus high breakdown voltage is maintained

due to high vertical electric field distribution [45]. The SJ structure breaks the traditional silicon limits for breakdown voltage and specific on-resistance in power MOSFETs. In [46] is reported study between vertical Si SJ MOSFETs and vertical GaN SJ MOSFETs, where breakdown voltage is $V_{\mathrm{BV,Si}} = 0.6 \sim 1.2\ \mathrm{kV}$ and $V_{\mathrm{BV,GaN}} = 2.7\ \mathrm{kV}$, respectively and specific on-resistance $R_{\mathrm{on,sp}} = 2 \sim 10\ \mathrm{m\Omega\ cm^2}$ and $R_{\mathrm{on,sp}} = 0.78\ \mathrm{m\Omega\ cm^2}$, respectively. The vertical SJ topologies cannot be used for very large scale integration (VLSI) onto a single chip due to its vertical topology. This topology is very useful for a realization of discrete components.

Such an example of superjunction topology is a lateral conventional superjunction LDMOS (CSJ LDMOS) and a lateral superjunction trench LDMOS (SJT LDMOS) [47]. In this case, the CSJ LDMOS has break-down voltage 169 V, and the other one has improved break-down voltage up to 218 V. SJT LDMOS has also improved specific on-resistance ($R_{\mathrm{on,sp}}$) by decreasing it up 20 % ($R_{\mathrm{on}} = 9.28\ \mathrm{m\Omega\ cm^2}$). The disadvantage of these LDMOSes is their manufacturing process since two independent wafers are needed for their final implementation. These wafers are later folded to form one SJT LDMOS. It is a very expansive and critical step for mass production, and moreover it is not suitable for low-voltage applications as it has been recommended for the V_{GS} higher than 5 V [47]. The similar results have been reached in [48], where double trench-gate drift MOSFET has been studied. Its break-down voltage and specific on-resistance have been $V_{\mathrm{BD}} = 182\ \mathrm{V}$ and $R_{\mathrm{on,sp}} = 0.96\ \mathrm{m\Omega\ cm^2}$, respectively. Of course, it depends on the doping concentration of a MOSFET. For this kind of MOSFET, the disadvantage is a much bigger structure in comparison to standard LDDMOSFET for not high-voltage applications.

The other categories are FinFETs and gate-all-around (GAA) MOSFETs structures. Let remind, over a span of decades, the scaling of CMOS technology has been a primary focus of the semiconductor industry in order to reduce the cost per function, increase speed, and reduce power [49]. The CMOS scaling was initially accomplished by shrinking device physical feature sizes [50], in particular, gate-

length, and enabled by process innovations, such as scaled gate dielectrics, improved junction profiles, and new contact materials [51]. After many scaling steps, the scaling was not possible anymore, and therefore, the new FinFETs and GAA MOSFETs structures have been developed. The typical applications for them are in developing digital functional circuits such as different SRAM cell topologies [52], burst clock generator [53], but also, untypically, it could be used, such as bandgap references [54, 55]. The uses drawback of FinFETs and GAA MOSFETs (nanowires) for analog circuits is mainly in a dramatically higher source/drain resistance, and higher C_{GS} and C_{GD} parasitic capacitance. C_{GS} and C_{GD} are higher due to gate coupling to the trench diffusion contacts and to the epitaxial source/drain fill between fins. As a fin width of FinFETs (W_{fin}) is a small fraction of the fin pitch, junction capacitance to the wells is reduced, but the vertical well resistance is much higher. Finally, self-heating is worse given the higher area density of device currents [56]. In addition, the process variability accuracy of too small parts, such as FinFET's and nanowire's parts, is very low [57, 58]. Therefore, the FinFETs are desired for ultra-low voltage designs such as digital topologies (SRAM, clock generators, etc.) and not for analog circuits with the partially higher power requirements. Currently, innovation studies focus on the elimination of Gate-Induced Drain Leakage (GIDL) and off-state gate-leakage [59]. The off-state gate-leakage is dominant for sub-micron technologies, and it is also a limiting factor in achieving ultra-low current consumption [60] of digital blocks. In the case of FinFETs, there is a possibility to have the width of the gate W_{fin} only in a few nanometers $W_{\mathrm{fin}} = 6$ nm [60], and the same, of course, is valid as well as for nanowires (GAA).

So far, in this work, the improvements in the electrical performances of planar MOSFETs have been realized by complex structural modifications. These modifications have increased the active area of the MOSFETs (such as, for example, in the case of drift MOSFETs, drain-extended MOSFETs, etc.) or significantly changed its current-voltage (I-V) characteristic (NC-FETs). These modifications increase MOSFETs breakdown voltages or change the character of MOSFETs

output characteristics. It means, they do not increase the electrical performances of planar MOSFETs in terms of boosting current-voltage characteristics, and thus do not help in improvements in the electrical performances in both low power and low voltage applications, respectively. In other non-planar technology processes, such as the “3D” transistor, the modifications are suitable for ultra-low voltage applications. Into this category are sorted for example FinFETs, GAA MOSFETs, etc. However, these modifications cannot be realized in planar technologies. Therefore, here the question arises on how to improve the electrical performances of planar MOSFETs. Such as a promising way, how to improve the electrical performances of low voltage MOS transistors, is to change/modify its gate shape. As highlighted in section 2.2 ”Review of Different MOSFET Gate Shape Architectures”, the gate modification is a very actual topic and it is often discussed in terms of the improvements of electrical performances of the MOS transistors. Not all possible modifications have been detailed described and therefore, it needs to be explored in more details such it is in this thesis.

Chapter 2

Technical Background

This technical background chapter demonstrates a thorough knowledge of the interesting field and provides arguments to support the study focus. The aim of this chapter is to delineate various theoretical positions and from these to develop a conceptual framework for the generation of hypotheses and setting up the research question.

The topic of this dissertation is to improve the electrical performances of planar MOSFETs in integrated circuits by physical mask design. The main goal of the improvements is to strengthen the output characteristics of MOSFETs or, in other words, to maintain the electrical performances of MOSFETs, but to use smaller active areas of MOSFETs for it. The following text proposes two different ways how to achieve this.

The first way how to save MOSFETs' areas and keep the same MOSFETs' performances is to down-scale the process. It allows us to maintain the original MOSFETs' performances and use the smaller MOSFET's active area for it. In the down-scaling process, there is a trade-off between the boosting, cost, and problems during the downscaling. Therefore, the following sections discuss the scaling

problems of MOSFETs such as technology field scaling theory, gate oxide variation, gate leakage, SCE, DIBL, GIDL, high-k, low-k, and other undesirable effects such as TID, and hump effect.

The second way how to save the areas and keep the same MOSFETs' performances is to modify the physical masks. Based on that, the other part of the next section presents various layout topologies of the MOSFETs such as circular gate shape with overlapping, cylindrical gate layout shapes, diamond layout shapes based on the "Longitudinal Corner Effect", enclosed layout shapes (square enclosed layout topologies, rectangular enclosed layout topologies, annular enclosed layout topologies, circular enclosed layout topologies), ellipsoidal gate shapes, octagonal gate shapes, trapezoidal gate shapes, waffle gate shapes, wave gate shape, Z gate shapes, which lead to better electrical performances of transistors.

This chapter reviews two different methods of MOSFETs' improvements in electrical performances in terms of mentioned requests to the silicon area. The first method is related to the technology process step, and the second one is related to the geometry modification of the MOSFETs' gate shape. Therefore, this chapter is organized as follows. The first section 2.1 ("Problems in Scaling") describes the problems that become with the IC technologies process downscaling for MOSFET devices and also describes a few specific parasitic effects of MOSFETs. The second section 2.2 ("Review of Different MOSFET Gate Shape Architectures") reviews many different MOSFET gates shape topologies resulting in improvements in electrical performances of MOS transistors.

2.1 Problems in Scaling

CMOS technology scaling has been a primary key for continuous progress in the silicon-based semiconductor industry. Scaling is followed by Moore's Law that provides a simple rule for transistor design to increase circuit density (Fig. 2.1) and speed for a few decades for digital design parts such as microprocessors units, SRAM, DRAM [61]. The improved circuit performances and density enable more complicated functionalities that require more integrated transistors on one single chip. However, as device scaling continues for the 21st century, it turns out that the historical growth doubled circuit density and increased performance followed by Moore's Law cannot be maintained only by the conventional scaling theory. Increasing leakage current does not allow further reduction of threshold voltage, which in turn prevents further supply voltage scaling for the speed improvement. Higher electric fields generated inside of the transistor worsen device reliability and increase leakage currents. Moreover, the required high channel doping causes significant challenges such as mobility degradation and random dopants induced threshold voltage fluctuations [62].

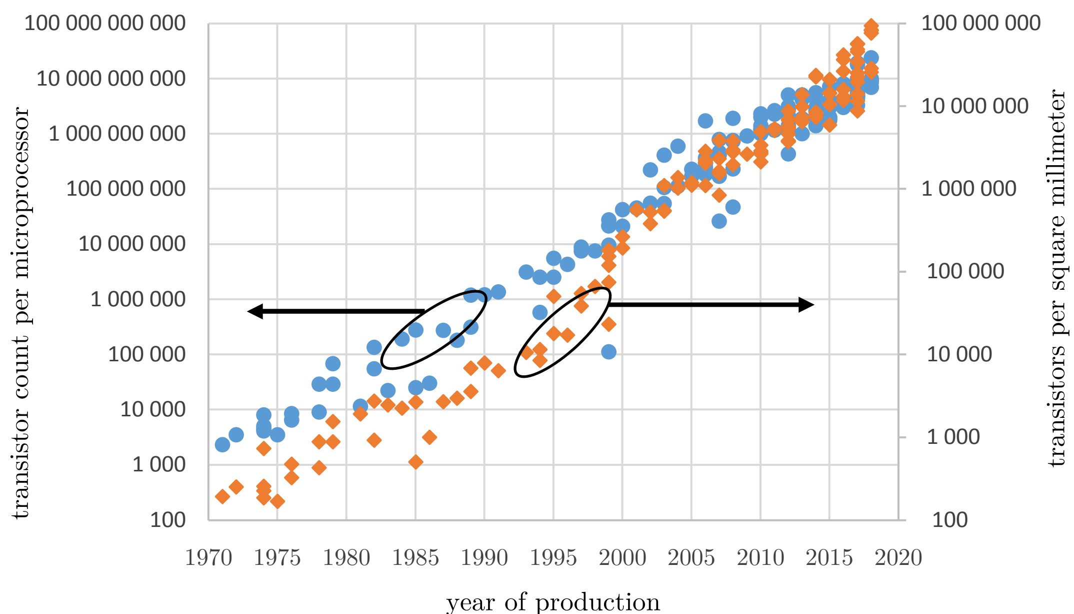


Fig. 2.1: Transistor count per different microprocessors of many vendors (blue circle symbol), transistor per square millimeter of different microprocessors of many vendors (orange diamond symbol), data from [61]

There is a question, why we do not use another material instead of silicon that can partially overcome the upper issues. There is the answer: One of the most important reasons for why the silicon is the most popular material is that billions of dollars and incredible amounts of time have been invested over the past several decades perfecting the process of making very reliable, ever smaller transistors with millions and sometimes billions of working transistors per chip. So even if another material could be better than silicon, a huge amount of time (many years) and money (billions of dollars) would still be needed to refine the designs and manufacturing processes [63]. Tab. 2.1 presents a comparison of the electronic properties of Si with GaAs, GaN, SiC [64], Ge, InAs [65], and diamond [66]. As we can see, the optimal material for the HV applications is 6H-SiC, or diamond which have a breakdown field equal to 3.2 MV cm^{-1} or 10 MV cm^{-1}, respectively. Moreover, the diamond has the highest thermal conductivity that is important for HV applications. Otherwise, for the low voltage applications, the germanium (Ge) material is the most optimal, since it has a very low bandgap equal to 0.66 eV. Although Ge has a very low bandgap, the drawback of the germanium is its very low thermal conductivity, which is three times less in comparison to silicon.

Another reason why silicon became dominant is that it is very easy to create a high quality thin insulator on the surface of a silicon chip, because you can just put silicon in a hot furnace with oxygen and it will form a thin film of silicon dioxide which performs as an excellent insulator which gave it a huge advantage when MOSFETs were first created. Modern chips are formed entirely with insulated gate MOSFET devices, this insulator is used to reduce power consumption and increase performance [63].

Some applications today such as very high-speed high-power transistors for wireless applications including communication and radar use other more specialized semiconductors including Gallium Nitride (GaN) because electrons move very quickly in GaN and the electron bonds are very tight in GaN so it can be operated up to higher voltages [67]. In contrast, the hole mobility is lower than electron

Tab. 2.1: Comparison of electronic properties of Si with GaAs, GaN, SiC [64], Ge, InAs [65], and diamond [66].

Property	**Si**	**Ge**	**GaAs**	**InAs**	**GaN**	**3C-SiC**	**4H-SiC**	**6H-SiC**	**dia-mond**
Bandgap (eV)	1.1	0.66	1.142	0.35	3.39	2.2	3.26	3	5.45
Breakdown field @ $T = 300$ K ($MV\,cm^{-1}$)	0.6	0.1	0.6	0.002	3.3	1.5	3	3.2	10
Electron mobility @ $T = 300$ K ($cm^2\,V^{-1}\,s^{-1}$)	1 100	3 900	6 000	40 000	1 000	750	800	370	2 200
Hole mobility @ $T = 300$ K ($cm^2\,V^{-1}\,s^{-1}$)	420	1 900	320	500	200	40	115	90	850
Saturated electron drift velocity ($cm\,s^{-1}$)	$1x10^{7}$	$6x10^{6}$	$1x10^{7}$	$3.5x10^{7}$	$2.5x10^{7}$	$2x10^{7}$	$2x10^{7}$	$2x10^{7}$	2.7
Intrinsic concentration, n_i (cm^{-3})	$1.5x10^{10}$	$2x10^{13}$	$1.9x10^{-10}$	$1x10^{15}$	$2.1x10^{6}$	6.9	$8.2x10^{-9}$	$2.3x10^{-6}$	$\sim10^{-27}$
Thermal conductivity @ $T = 300$ K, ($W\,cm^{-1}\,K^{-1}$)	1.5	0.58	0.55	0.27	1.3	5	4.9	4.9	22

mobility, and therefore it is not suitable for CMOS applications. Ultra-high-speed transistors operating at up to 1 000 GHz are built with Indium Gallium Arsenide semiconductors because electrons move even faster in this material so it is very difficult for silicon transistors to match the speed, these transistors may be used someday for ultra-high-speed wireless communication links with far more bandwidth than is possible today [68].

The excellent graphical overview of high-speed and high-power transistors uses different materials is shown in the following Fig. 2.2. There is shown, the best material for high-speed and high-power applications is GaN on SiC substrate. The GaAs and SiGe materials are useful for high-speed in low-power applications. As a compromise can be used GaN on Silicon substrate. For middle-high-speed and high-power applications can be used Silicon LDMOS transistors.

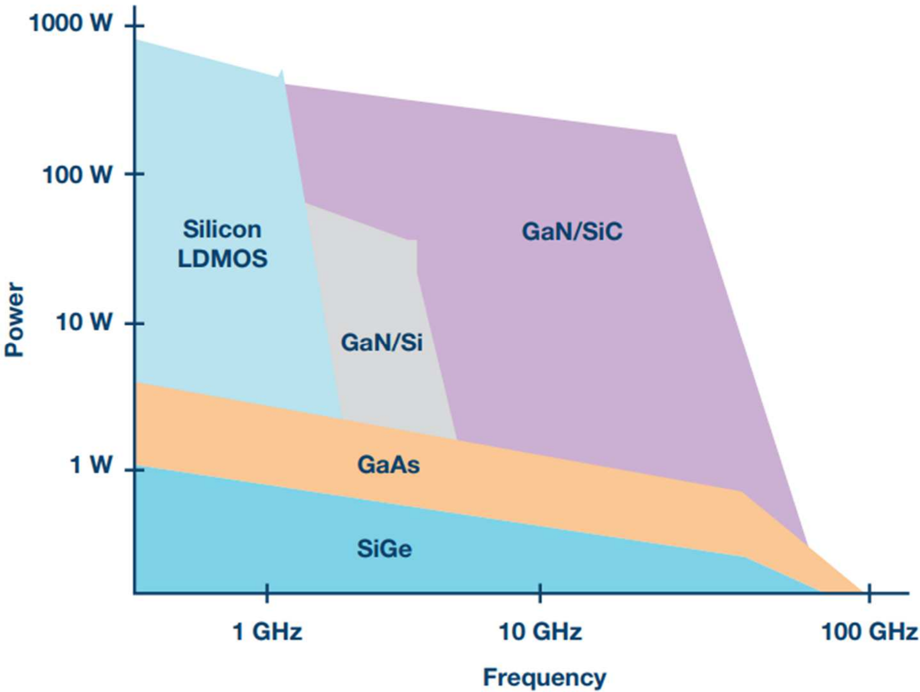


Fig. 2.2: A process technology comparison of microwave frequency range power electronics [69].

2.1.1 **Constant Field Scaling Theory**

To increase the performances of MOSFETs, we could reduce the size of the transistors. In order to maintain the electric field in MOSFET devices constant, the supply voltage should decrease linearly with the linearly MOSFETs' size downscaling. On the other side, the doping concentration should increase linearly with the linearly size downscaling. Just in this way, the downscaling keeps the

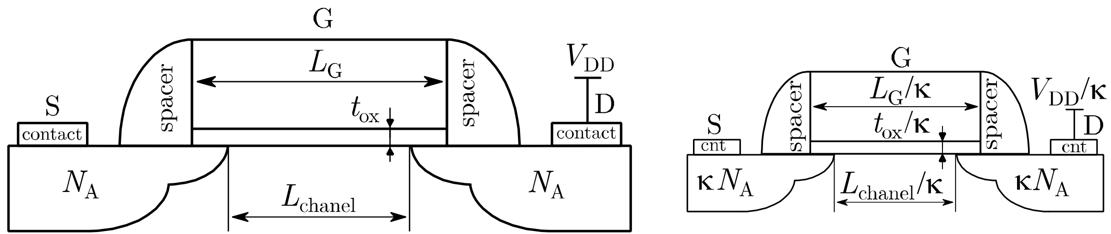


Fig. 2.3: Illustration of MOSFET miniaturization. The sketch on the right hand is the scaled device according to the constant field rule.

electric field in the device constant [70]. This a pioneer "constant field scaling" theory (Fig. 2.3) defines relations between three design parameters (supply voltage, doping concentration, and physical dimensions) of a particular generation of the transistor by the same scaling factor κ.

The scaled-down device will have a reduced supply voltage (V_{DD}/κ), vertical (t_{ox}/κ and x_j/κ) and horizontal (L/κ) dimensions, and an increased doping concentration (κN_A), as depicted in Fig. 2.3. Despite the change in those parameters, the intensity of the electric field remains virtually unchanged. It happens due to the fact, both the dimension and the supply voltage were scaled by the same ratio ($V_{DD}/L = V'_{DD}/L'$). The following Tab. 2.2 summarizes the changes in device dimensions and circuit parameters as a result of both the constant field and the generalized scaling rules.

Tab. 2.2: Summary of the constant field scaling and the generalized scaling rules.

Scaled Parameters	Constant field Scaling
t_{ox}, L, W, xj, W_d	$1 / \kappa$
N_A, N_D (ions m^{-3})	κ
Power supply: (V_{DD})	$1 / \kappa$
Electric field in device: (E)	1
Capacitance: (C)	$1 / \kappa$
Inversion charge density: (Q)	1
Circuit delay time: $\tau \approx CV/I$	$1 / \kappa$
Power dissipation: (P)	$1 / \kappa^2$
Power density: (~ PA)	1
Chip Area: (A)	$1 / \kappa^2$
Current, Drift: (I)	$1 / \kappa$

2.1.2 **Gate Oxide Variation**

The gate oxide is an insulator layer between the gate and substrate of MOSFET. The gate oxide thickness (t_{ox}) influences many crucial electrical parameters of MOS transistors such as a gate oxide capacitance (C_{ox}) (2.1), a threshold voltage (V_{th}) (2.2), a saturation voltage (V_{Dsat}) (2.3), and so also a drain current (I_D) (2.4). The drain current depends on the gate oxide thickness in all its operation regions: subthreshold, linear (triode) (for small V_{DS} (2.5), and for large V_{DS} (2.6)), saturation (2.8), and pinch-off.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_0 \varepsilon_r A}{t_{ox}} \tag{2.1}$$

where ε_{ox} is a (absolute) oxide permittivity, ε_0 is a vacuum permittivity ($8.854 \cdot 10^{-12}$ F m^{-1}), ε_r is a relative permittivity of the oxide (relative dielectric constant), A is a surface area of the gate oxide. In the case of silicon dioxide, ε_r is equal to 3.9.

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + 2|\Phi_{\mathrm{B}}| + \sqrt{\frac{2\varepsilon_{\mathrm{Si}} q N_{\mathrm{A}} (2|\Phi_{\mathrm{B}}|)}{C_{\mathrm{ox}}}} \tag{2.2}$$

where V_{FB} is a flat band voltage, Φ_B is a bulk potential, q is a magnitude of the electron charge ($q = 1.602 \cdot 10^{-23}$ J K^{-1}), and N_A is a net ionized acceptor density.

$$V_{\mathrm{Dsat}} = V_{\mathrm{G}} - V_{\mathrm{th}} \tag{2.3}$$

where V_G is a gate voltage of MOSFET.

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} \left[\left(V_{\mathrm{G}} - V_{\mathrm{FB}} - 2|\Phi_{\mathrm{B}}| - \frac{V_{\mathrm{DS}}}{2} \right) V_{\mathrm{DS}} - \frac{2\sqrt{2\varepsilon_{\mathrm{Si}} q N_{\mathrm{A}}}}{3C_{\mathrm{ox}}} \left\{ (2|\Phi_{\mathrm{B}}| + V_{\mathrm{DS}})^{\frac{3}{2}} - (2|\Phi_{\mathrm{B}}|)^{\frac{3}{2}} \right\} \right] \tag{2.4}$$

where W and L are the width and length of MOSFET, respectively. ε_{Si} is a relative permittivity of the silicon substrate, μ_n is an electron mobility.

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{G}} - V_{\mathrm{th}}) V_{\mathrm{DS}} \tag{2.5}$$

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{G}} - V_{\mathrm{th}}) V_{\mathrm{DS}} - \frac{\gamma}{2} V_{\mathrm{DS}}^2 \right] \tag{2.6}$$

$$\gamma = 1 + \frac{\sqrt{\frac{\varepsilon_{\mathrm{Si}} q N_{\mathrm{A}}}{4|\Phi_{\mathrm{B}}|}}}{C_{\mathrm{ox}}} = 1 + \frac{C_{\mathrm{Si}}}{C_{\mathrm{ox}}} = 1 + \frac{3t_{\mathrm{ox}}}{d_{\mathrm{max}}} \tag{2.7}$$

where γ is related to the body effect and is called the body-effect coefficient, d_{max} is a saturated width of the depletion region, which reaches its maximum at the effective inversion mode of MOS transistors.

$$I_{\mathrm{Dsat}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{G}} - V_{\mathrm{th}})^2 \frac{1}{\gamma} \quad (2.8)$$

In order to achieve the required current drive at an ultra-low power supply voltage in MOSFETs, aggressively modified gate dielectric with an equivalent thickness of oxide (EOT) down to 0.39 nm is required by the standard latest edition of International Technology Roadmap for Semiconductors (ITRS) [71]. In such ultrathin oxides, channel carriers can be inserted into the tunnel of a polysilicon gate through a dielectric gate material. This process electron or hole transmission by the dielectric barrier increases the leakage current of the gate exponentially with decreasing t_{ox} [72 -74]. In [75] it is expressed by the following approximate equation (2.9), where k_1 and k_2 are constant.

$$I_{\mathrm{GB}} \approx k_1 \, e^{\frac{t_{ox}}{k_2}} \quad (2.9)$$

As shown in Fig. 2.4, in addition to the tunneling current from the gate-to-channel I_{GB}, the edge currents from the gate overlap with the source and drain extension, respectively, contribute to the total gate leakage current. The process of tunneling is well shown in Fig. 2.5 for NMOS transistor.

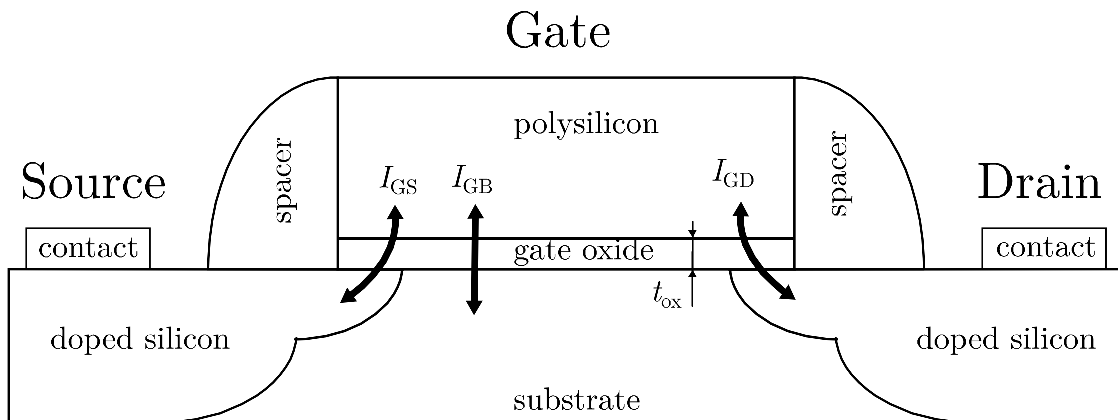


Fig. 2.4: The overall gate tunneling current is the sum all the components tunneling current namely the gate-to-source, gate-to-drain and gate-to-substrate currents.

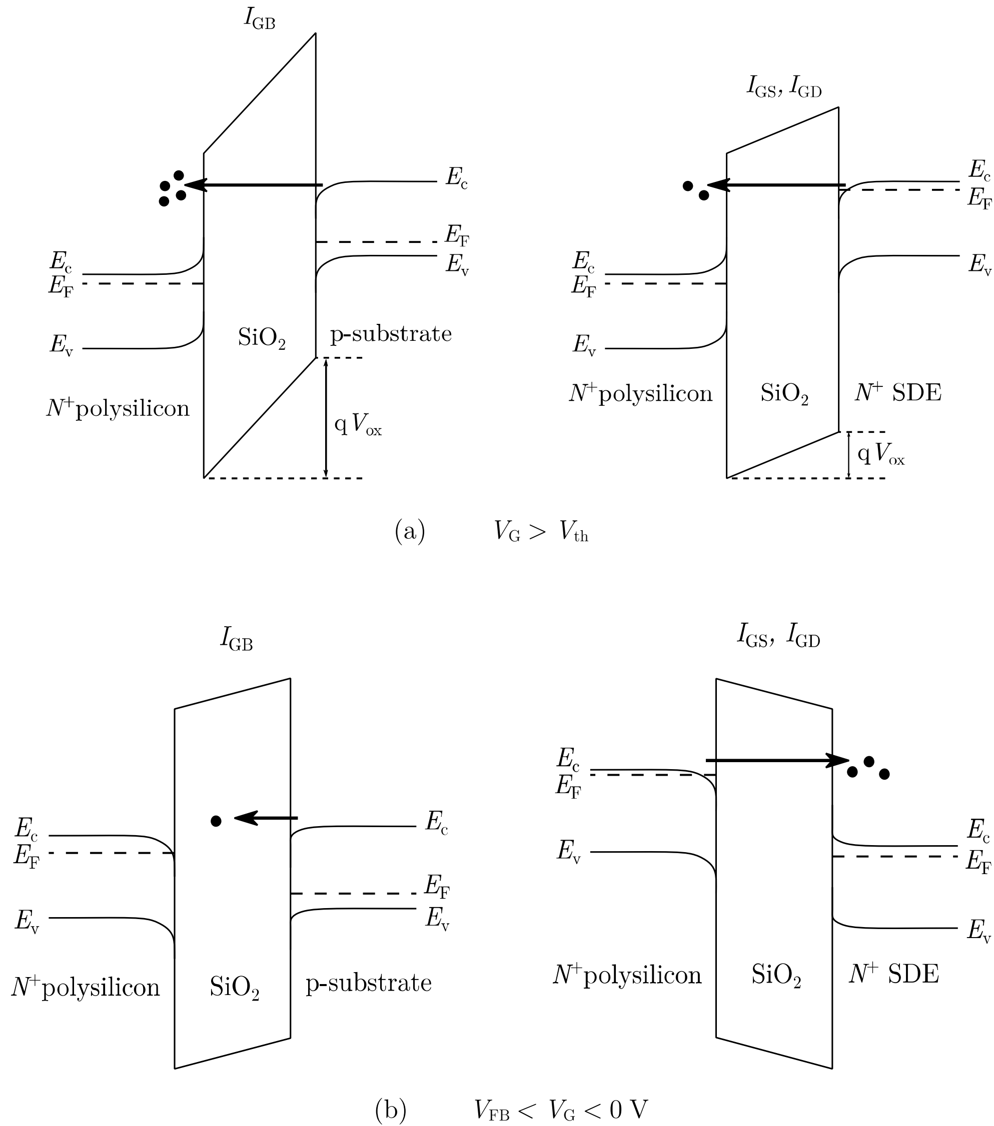


Fig. 2.5: Gate bias dependent band diagrams and electron tunnelling in the channel (I_{GB}) and the gate edge (I_{GS} and I_{GD}); (a) $V_G > V_{th}$ (inversion mode), (b) $V_{FB} < V_G < 0$ V (depletion mode).

Moreover, the non-uniformity of the gate oxide thickness creates higher gate current leakage, and different breakdown voltage, as it is shown in Fig. 2.6. These problems occur mainly for downscaling of the transistors when the t_{ox} is lower than 2 nm [76]. For the interesting: in the case, where the t_{ox} is equal to 0.4 nm, there are just 3 atomic layers of SiO_2. The theoretical SiO_2 monolayer thickness (one atomic layer) is equal to 1.36 Å [77, 78].

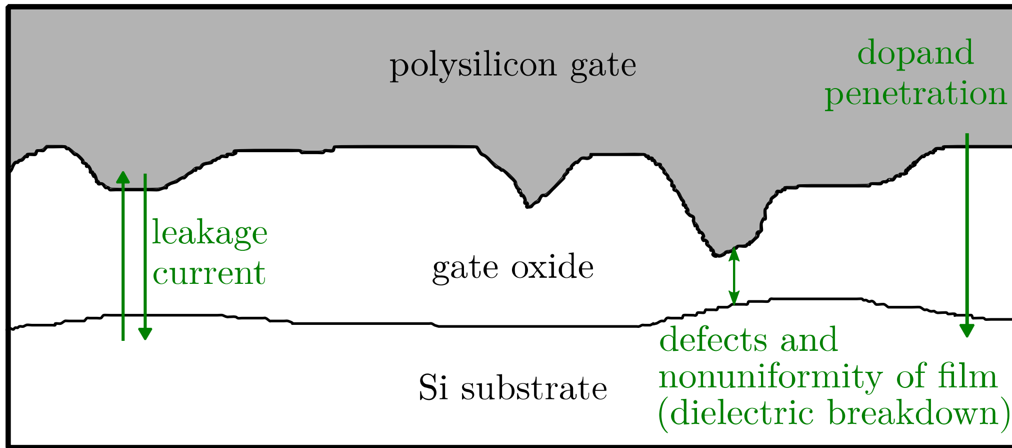


Fig. 2.6: Problems in scaling of the gate oxide thickness leads to higher leakage gate current, and different breakdown voltage.

2.1.3 **Short Channel Effect (SCE)**

Since the physical scaling-down mechanism enhances the MOSFETs performance, it does not exclude the short channel effect (SCE) that becomes prominent. As the channel length shrinks, the gate controllability above the channel depletion region reduces due to increased charge sharing from source/drain terminal Fig. 2.7. The SCE leads to several reliability issues, including the dependence of device characteristics such as threshold voltage on channel length. An example of threshold voltage vs. gate length for Si and InGaAs is depicted in Fig. 2.8 [79]. This

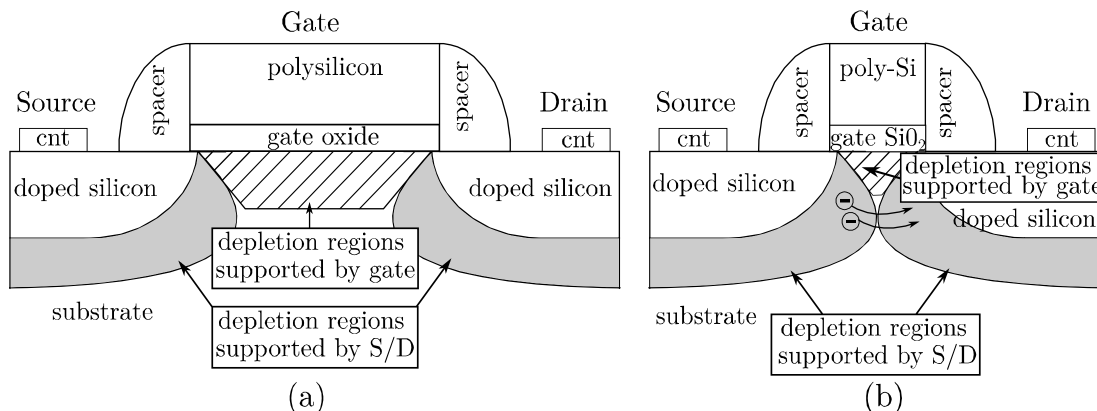


Fig. 2.7: Charge sharing in a long channel (a) and short channel (b) of MOSFET. In the case of the short channel, there is shown sub-surface punch-trough. It means, the depleted regions around the drain and source terminals, causing current to flow irrespective of gate voltage (i.e. even if the gate voltage is zero).

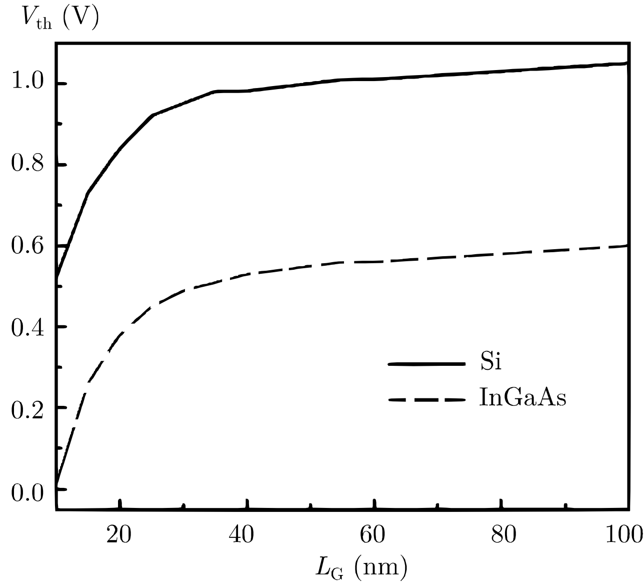


Fig. 2.8: An example of threshold voltage vs. gate length for Si and InGaAs MOSFETs, inspired by [79].

leads to the scatter of device characteristics because of the scatter of gate length produced during the fabrication process. The predominating reliability problems associated with SCE are a lack of pinch-off and a shift in threshold voltage (threshold voltage roll-off TVRO) [79] with decreasing channel length as well as drain-induced barrier lowering (DIBL) and hot-carrier effect (HCE) [80, 81] at increasing drain voltage. In addition, SCE degrades the controllability of the gate voltage to drain current, resulting in degradation of the subthreshold slope and the increase in drain off-current [82]. This degradation is described as charge sharing by the gate and drain electric fields in the channel depletion layer in [83], which was reported as the first SCE model.

To reduce this effect, different techniques have been implemented in silicon MOS technologies. Using a multi-gate stack approach [84], high-K dielectric [85], thicker gate oxide [86], halo pockets [87], using shallow source/drain junction, and higher substrate doping are known to be effective ways of preventing SCE. With short-channel devices, the reliability margins have also been cut down significantly. Particularly, the high electric field near the drain becomes more crucial and poses a limit on device operation, notably by a large gate current, substrate current, and a substantial threshold voltage shift [88].

The SCE can be chiefly attributed to the DIBL effect which causes a reduction in the threshold voltage as the channel length decreases. The DIBL effect discussion is in the following section.

2.1.4 **Drain-Induced Barrier Lowering (DIBL)**

The DIBL effect has not a negligible impact on a depletion region of the MOSFETs channel. With the increasing drain voltage, the drain depletion region around the drain diffusion expands (Fig. 2.9) and the part of channel surface becomes already depleted. Since the channel must be depleted of charge before inversion takes place, any help on the depletion process will reduce threshold

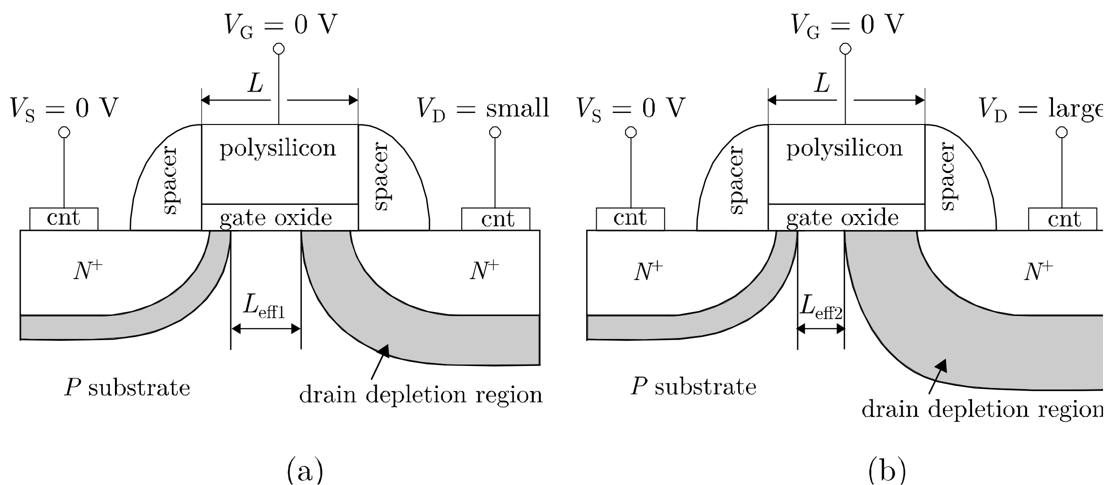


Fig. 2.9: An example of modification depletion region in NMOSFET depending on different drain voltage: small drain voltage (a), and large drain voltage (b).

voltage. In the weak inversion regime, there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance. As is depicted in Fig. 2.10, inspired by [89], the DIBL effect [90] occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field by a high drain voltage. This increases the number of carriers injected into the channel from the source leading to

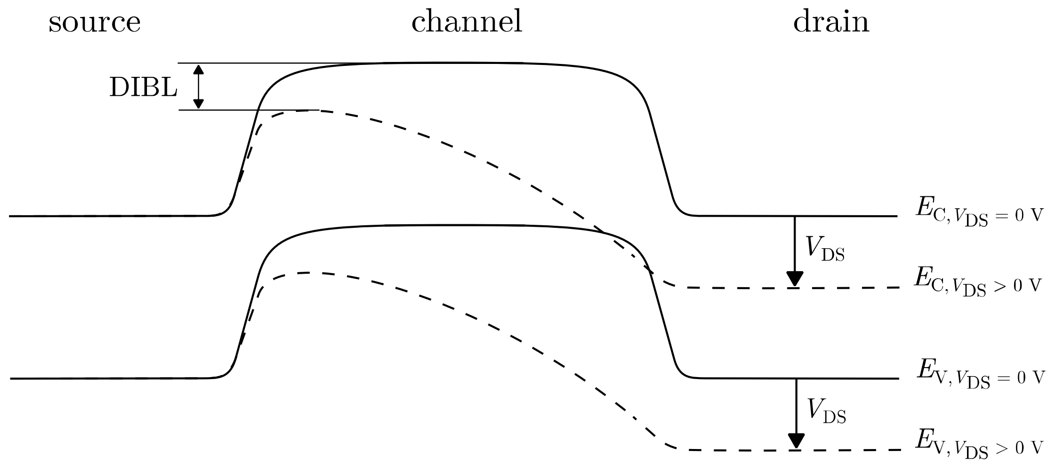


Fig. 2.10: Comparison of schematic energy band diagrams near to surface of the NMOSFET with the drain voltage equal to zero volts (solid line) and with the drain voltage higher than zero volts.

an increased drain off-current. Thus, the drain current is controlled not only by the gate voltage but also by the drain voltage.

As the result of this parasitic effect is a threshold voltage reduction depending on the drain voltage Fig. 2.11 [91] and higher drain off-current Fig. 2.12 [92].

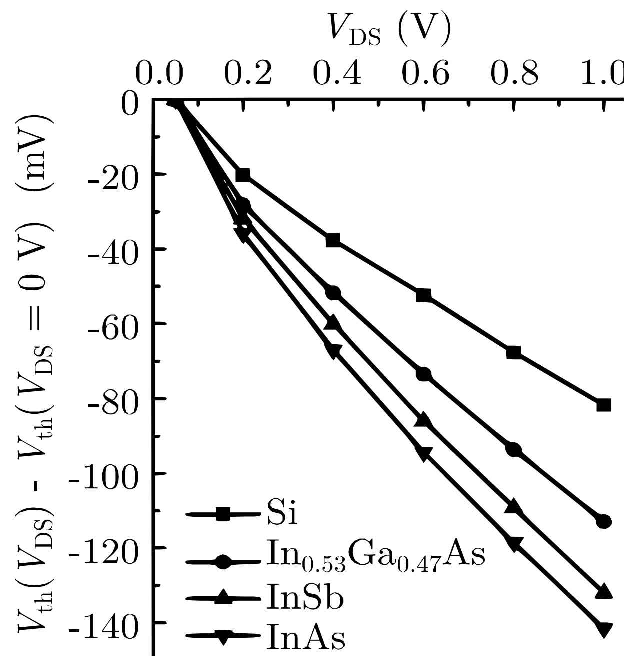


Fig. 2.11: An example of DIBL comparison for various III-V-on-insulators NMOSFET, for the same technological parameters such as W, L, and t_{ox}, insipred by [91].

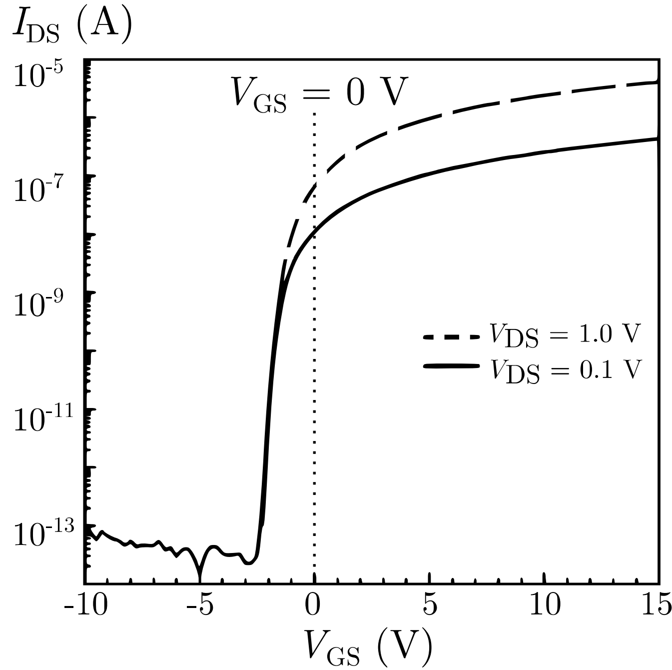


Fig. 2.12: An example impact of DIBL effect on drain off-current for different drain voltages, insipred by [92].

Choosing a suitable source/drain extension provides an effective way to suppress the DIBL effect [93]. Also, it allows balancing the performances drain off-current and drain on-current, if it is necessary. The drawback of this method is the higher series resistance between the source and drain terminal in on-state of MOSFET. As another technique for reducing this effect is to use a specific MOSFET structure called a "junction-less" MOS transistor, where the SiO_2 BOX is replaced by high-K BOX [94].

2.1.5 **SCE + DIBL**

As the dimensions of the device enter the sub-micron dimensions, the two-dimensional effects (SCE and DIBL) become more important and significant. The successive field approximation is invalid and the field changes significantly even if the constant field scaling scenario is used. It is well illustrated in Fig. 2.13 where an energy conductivity band changes dependently on the presence of SCE, DIBL, and both SCE+DIBL.

The typical electrical behavior of device under the influence of short channel effect (SCE) and drain induced barrier lowering (DIBL) are highly dependent on at least five major design parameters as it is shown in equations (2.10) and (2.11) [95].

$$SCE = \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\left(1 + \left(\frac{x_{\mathrm{j}}}{L_{\mathrm{eff}}}\right)^2\right)\frac{t_{\mathrm{ox}}t_{\mathrm{dep}}}{L_{\mathrm{eff}}^2}V_{\mathrm{bi}} \tag{2.10}$$

$$DIBL = \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\left(1 + \left(\frac{x_{\mathrm{j}}}{L_{\mathrm{eff}}}\right)^2\right)\frac{t_{\mathrm{ox}}t_{\mathrm{dep}}}{L_{\mathrm{eff}}^2}V_{\mathrm{DS}} \tag{2.11}$$

where $\varepsilon_{\mathrm{ox}}$ is a (absolute) oxide permittivity, $\varepsilon_{\mathrm{Si}}$ is a relative permittivity of the silicon, x_{j} is a junction depth, t_{ox} is a oxide thickness, t_{dep} is a depletion region (a gate field penetration depth into channel region), V_{bi} is a built-in potential of a MOSFET, V_{DS} is a drain-source voltage of a MOSFET, and L_{eff} is an effective length defined by the following expression:

$$L_{\mathrm{eff}} = L_{\mathrm{G}} - \Delta L \tag{2.12}$$

where L_{G} is the physical gate length and ΔL is the sub-diffusion length.

The *SCE* and *DIBL* parameters enable to calculate the saturation threshold voltage [96] on nominal devices as:

$$V_{\mathrm{th_nom}} = V_{\mathrm{th_long}} - SCE - DIBL \tag{2.13}$$

$$V_{\mathrm{th_long}} = V_{\mathrm{FB}} - 2\Phi_p - \frac{qN_{\mathrm{ch}}t_{\mathrm{dep}}}{C_{\mathrm{ox}}} \tag{2.14}$$

where V_{FB} is a flat-band voltage, Φ_{p} is a channel/bulk potential, N_{ch} is a channel doping, C_{ox} is an oxide capacitance.

This is a point that should be respected during the scaling down approach and can be understanding as a difficulty [97].

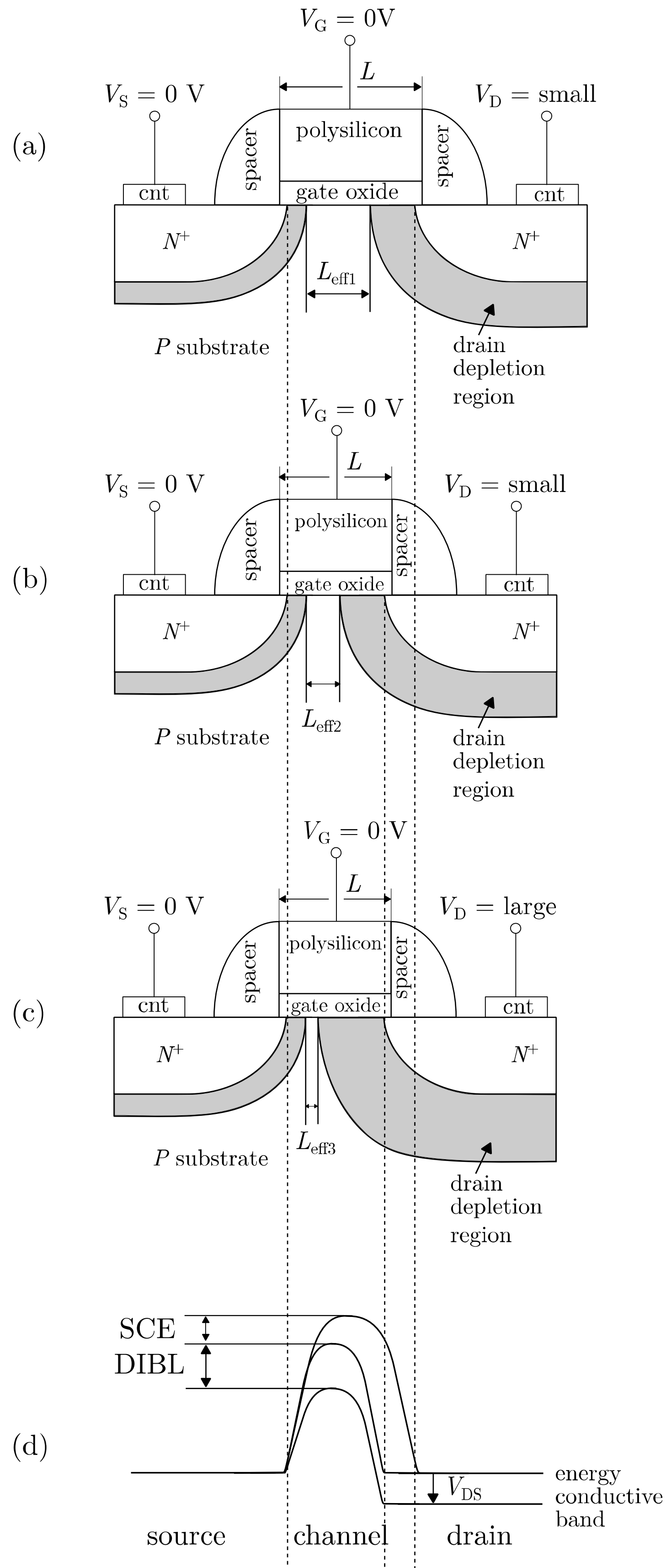


Fig. 2.13: An example of energy conductive bands for different drain voltages and different MOSFET's lengths. Standard MOSFET (a), MOSFET with a short channel (b), MOSFET with a short channel and DIBL effect (c), and energy conductive bands (d).

2.1.6 **Gate-Induced Source and Drain Leakage (GISL and GIDL)**

Other sources of off-state leakage current in down-scaled processes are the gate-induced drain leakage (GIDL) and gate-induced source leakage (GISL), respectively. It is important to understand its causes and be able to predict its severity. This off-state leakage is a particular problem for some low-power and long-retention applications, such as DRAMs [98].

Fig. 2.14a illustrates a cross-section of an NMOSFET and its energy-band diagram at the point of interest (Fig. 2.14b) for the gate-drain overlap region when a low gate voltage and a high drain voltage are applied. If the band bending at the oxide interface is greater than or equal to the energy band gap E_g of the drain material, band-to-band tunneling (BTBT) is performed. The electrons in the N-type valence band of the drain will tunnel through the thinned band gap into the conductive band and will be collected at the drain contact to be a part of the drain current, while the reaming holes will be collected at the substrate contact and will contribute to the substrate leakage [99].

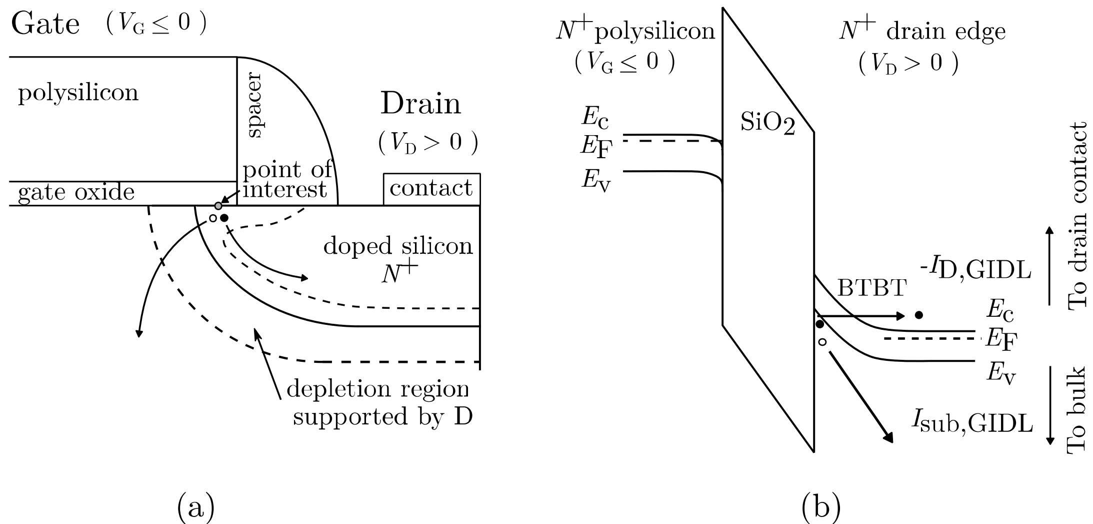


Fig. 2.14: Cross-section of the NMOSFET (a), and illustration its energy-band diagram (b) in the point of interest shown in (a).

When the gate is at zero or negative voltage, and the drain area at the supply voltage level, there can be a dramatic increase of effects like avalanche multiplication and band-to-band tunneling. The result of this phenomenon is

increasing drain leakage current depending on drain voltage as it is depicted in Fig. 2.15 [100]. With the higher supply voltage and thinner oxide, the GIDL increases.

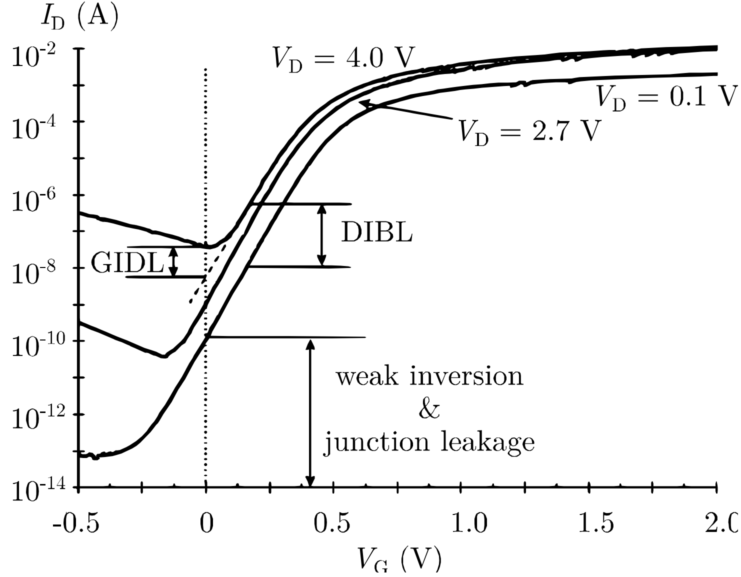


Fig. 2.15: Contributions of DIBL and GIDL to the transistor's off-state leakage current. The position of the dip caused by GIDL will vary around $V_{GS} = 0$ V depending on V_D, the channel material, doping, and trap density, inspired by [100].

GIDL is more serious in partially depleted SOI MOSFET devices as it gets amplified by the lateral parasitic BJT [101], in contrast with fully depleted SOI MOSFET, where the phenomenon is suppressed. In case of SOI NMOSFET, the holes moving out from the drain accumulate in the body activating parasitic bipolar junction transistor (pBJT), and a current of βI_{GIDL} flows to the drain terminal. The GIDL current (I_{GIDL}) is independent of channel length, whereas the current gain β of the lateral pBJT increases as the base width (channel length) decreases. This implies that in SOI MOSFET devices, the GIDL current gets amplified with channel length scaling, because of the increase in the gain of pBJT [102].

There exist methodologies to suppressed the GIDL effect, such as a longer N^- spacer [103], a larger substrate back-biasing [104], or using dual work-function metal gate [105].

2.1.7 High-K Dielectrics

Continuous down-scaling of complementary MOSFETs with the silicon dioxide (SiO_2) layer used as a gate dielectric leads to increasing its leakage current by tunneling effect. As MOSFETs have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 2.0 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability.

Replacing the silicon dioxide gate dielectric with a high-K material (Tab. 2.3) allows increased gate capacitance without the associated leakage effects. The term high-K dielectric refers to a material with a high dielectric constant, as compared to SiO_2. The implementation of high-K gate dielectrics such as hafnium oxide and hafnium silicate are one of several strategies developed to allow further

Tab. 2.3: Static dielectric constant K and experimental bandgap for gate dielectrics.

Material	$\varepsilon_r = K$ (-)	E_g (eV)
Si	-	1.1
SiO_2	3.9	9
Si_3N_4	7	5.3
Al_2O_3	9	8.8
Ta_2O_5	22	4.4
TiO_2	80	3.5
$SrTiO_3$	2 000	3.2
ZrO_2	25	5.8
HfO_2	25	5.8
$HfSiO_4$	11	6.5
La_2O_3	30	6
Y_2O_3	15	6

miniaturization of microelectronic components, colloquially referred to as extending Moore's Law.

In [106, 107], the tunneling current density (J) decreases exponentially with increasing distance by the following equation.

$$J = J_0\, e^{(-2kt_{\mathrm{ox,eq}})} \tag{2.15}$$

$$k = \sqrt{(2m^* \Phi_{\mathrm{p}})}\left(\frac{K}{\varepsilon_{\mathrm{r,SiO_2}}}\right) \tag{2.16}$$

where k is defined a theoretical figure of merit parameter [108] for direct tunneling, based on the barrier height Φ_{p}, tunneling mass m^*, dielectric constant K, and dielectric constant of SiO_2 $\varepsilon_{\mathrm{r,SiO2}}$. A parameter $t_{\mathrm{ox,eq}}$ is effective oxide thickness (EOT).

A MOSFET is a capacitance-operated device, where the source–drain current of the transistor depends on the gate capacitance

$$C_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}}}{t_{\mathrm{ox}}} = \frac{\varepsilon_0 K}{t_{\mathrm{ox}}} \tag{2.17}$$

where $\varepsilon_{\mathrm{ox}}$ is a (absolute) oxide permittivity, ε_0 is a vacuum permittivity ($8.854 \cdot 10^{-12}$ F/m), ε_{r} respectively K is the relative permittivity, and t_{ox} is the oxide

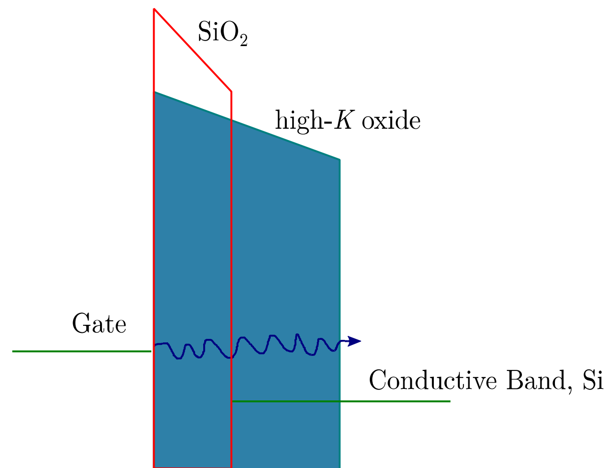


Fig. 2.16: Schematic of direct tunnelling through a SiO_2 layer (red polygon) and the more difficult tunnelling through a thicker layer of high-K oxide (blue polygon).

thickness. Hence, the solution to the tunneling problem is to replace SiO_2 with a physically thicker layer of new material of higher dielectric constant K (Fig. 2.16). This will keep the same capacitance but decrease the tunneling current.

For the electrical design of a device the precise material does not matter, so it is convenient to define an ”electrical thickness” of the new gate oxide in terms of its equivalent silicon dioxide thickness or equivalent oxide thickness (EOT) as

$$t_{\mathrm{ox,eq}} = \mathrm{EOT} = \frac{\varepsilon_{\mathrm{r,SiO_2}}}{\varepsilon_{\mathrm{r,high-K}}} t_{\mathrm{high-K}} = \frac{3.9}{K} t_{\mathrm{high-K}} \tag{2.18}$$

where 3.9 is the static dielectric constant of SiO_2. The objective is to develop high-K oxides which allow scaling to continue to ever lower values of EOT [109].

2.1.8 **Total Ionizing Dose (TID) Effect**

Nowadays, the aggressive downscaling of CMOS technologies introduces ultra-thin dielectrics [110]. But in the case of ultra-thin dielectrics, there is higher gate current leakage, which should be suppressed. For this reason, we should use the high-K dielectric materials, such as hafnium oxide (HfO_2) as the gate oxide. In this case, the gate oxide is thicker and decreases the gate leakage current, but in the counterpart with it, it is less resistant to Total Ionizing Dose (TID) effect. The TID effect is the other effect that should be respected for high precision devices such as the upcoming high luminosity large hadron collider (HL-LHC) at CERN. This HL-LHC requires highly enhanced tracking systems with more radiation-resistant front-end electronics to overcome 1 Grad of TID for ten years of operation [111].

There are, basically, two parts of MOS transistors, where the TID effect modifies electrical functionality. Both are due to the ionizing effects of radiation interacting within dielectric regions present in the device.

The first cause of the damage that occurs in CMOS devices after ionizing radiation is the generation of the electron-hole pairs in the oxide (or another

dielectric) as a material that is the most sensitive to ionizing radiation in CMOS devices. After the generation of the electron-hole pairs, some of the pairs are immediately recombined. Since the electron mobility in the oxide is considerably bigger that the hole mobility, the electrons will be soon swept out of the oxide or the dielectrics, while the holes will move slowly through the oxide to the interface SiO_2-Si, causing long-term effects of the ionizing radiation [112]. Fig. 2.17 shows the processes after the ionizing radiation.

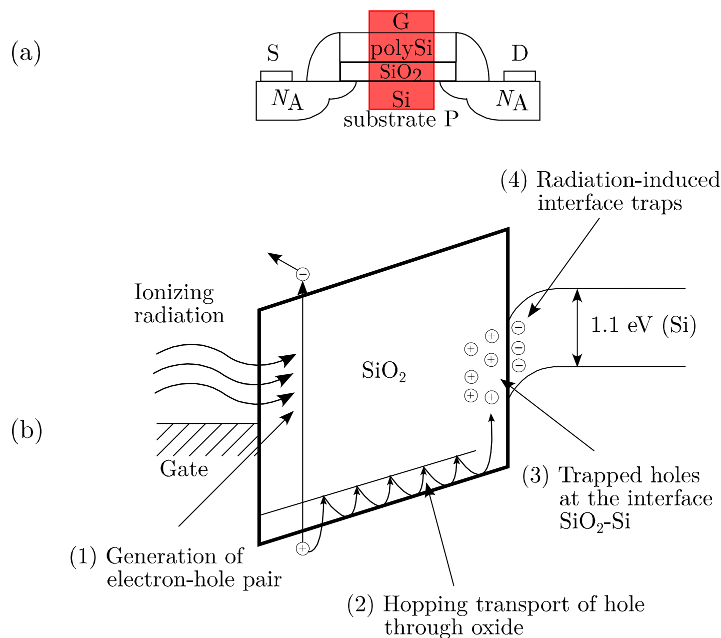


Fig. 2.17: MOS structure with the highlighted red part (a) where the ionizing radiation induce charge trapping and interface state generation (b).

The second case is the interaction of active regions of MOSFET being surrounded by field oxide such as LOCOS or modern thick Shallow Trench Isolation (STI) oxides [113] depicted in Fig. 2.18. This interaction can lead to trapped positive charge and also increase the defect density at SiO_2-Si boundaries.

Comparison of upper possibilities, CMOS transistors are less susceptible to charge trapping in the gate oxide as it is normally very thin (<10 nm). More of a problem is the STI which is significantly thicker (~300 nm) and the charge trapping is proportionately more severe, leading to parasitic leakage currents. The effect of

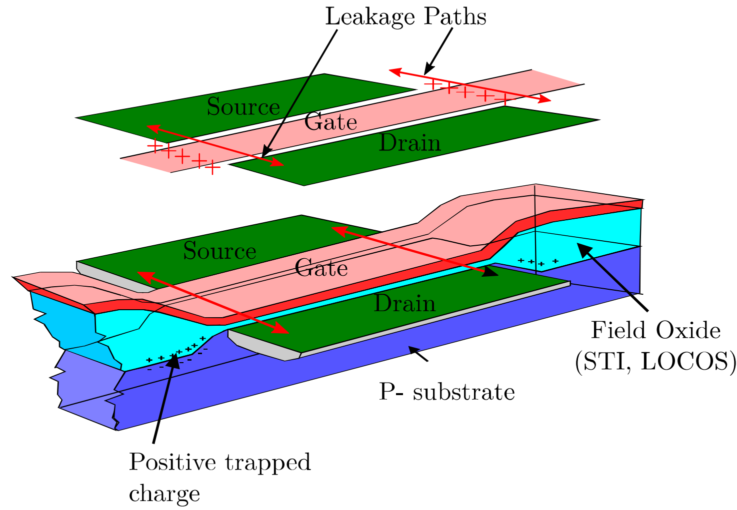


Fig. 2.18: Drain leakage current of N-channel MOSFET with respect to total ionizing dose.

increased defect density (interface states) at oxide boundaries is an issue for both types of region and will lead to increased noise. Moreover, the tarped charge changes the threshold voltage V_{th} of CMOS devices. Formula of the threshold voltage shift is given by the following expression:

$$\Delta V_{th} = -\frac{q t_{ox}^2 N_{ox}}{\varepsilon_{ox}} \tag{2.19}$$

where q is the electron charge, t_{ox} is the oxide thickness, N_{ox} is the quantity of trapped charge and ε_{ox} is the oxide permittivity. The threshold voltage shift ΔV_{th} is negative, which means that in the case of the NMOS transistor the off current increases, while in the case of the PMOS transistor the total value of threshold voltage V_{th} increases, as shown in Fig. 2.19.

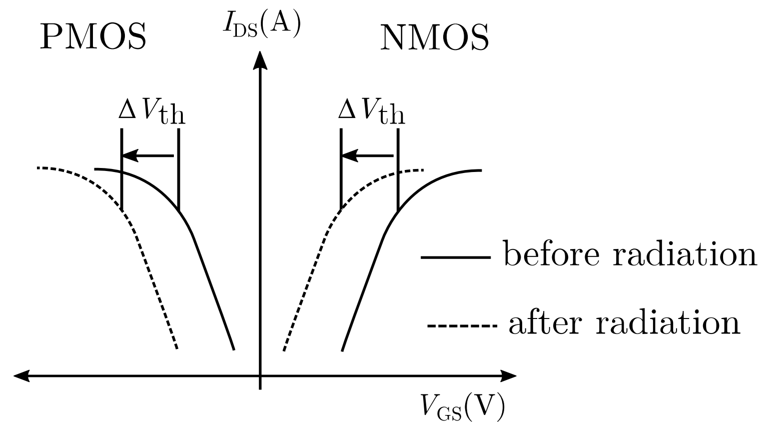


Fig. 2.19: Illustration of the threshold voltage shift ΔV_{th} due to the oxide trapped, inspired by [112].

2.1.9 **Hump Effect**

In the present, there is a trend to use new design integrated circuits in low power mode in the sub-threshold regime of MOS transistors. The sub-threshold regime has become a standard for low power applications due to the very low current level with low supply voltage [114]. Moreover, the mainstream of the semiconductor industry is to increase the density of ICs on a chip. It is possible due to the evolution of submicron technologies, where the transition between active area and isolation becomes more abrupt to increase device integration density and performance. This is possible using shallow trench isolation (STI) process instead of a local oxidation of silicon (LOCOS) process. The STI process allows downscale lateral CMOS technology family and thus to reach a higher device density on

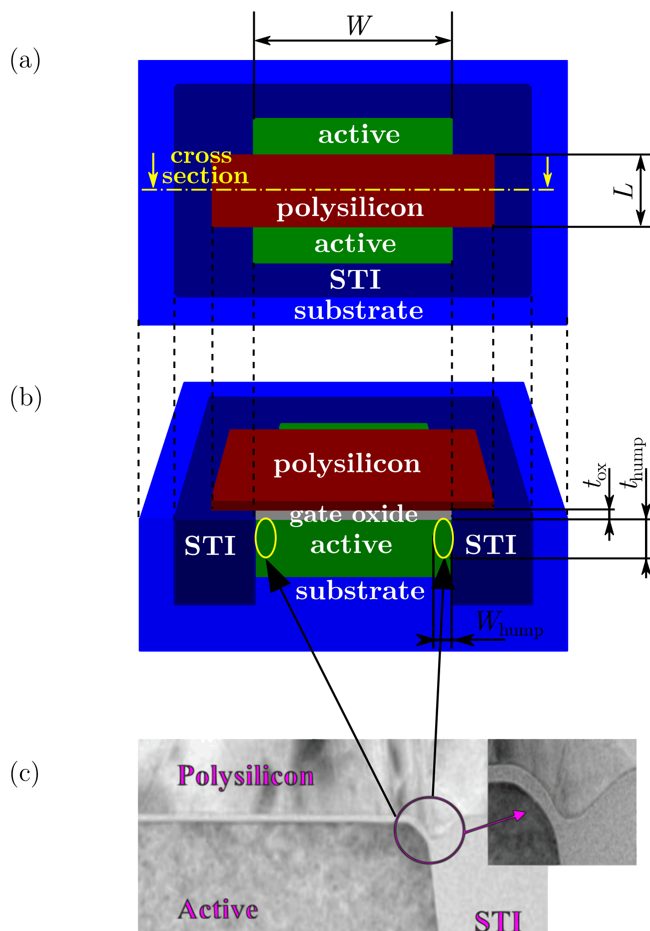


Fig. 2.20: Top view of the MOS transistor (a), its cross-section view (b) with highlighted parts of MOS transistor where the hump effect is located. The (c) part is TEM micrograph photo [115] of the fabricated MOS transistor.

a chip [116]. In the case of a combination low-power STI technology process and high-power devices, the hump effect has been observed.

Although the STI process offers to us a lot of improvements the abrupt separation of an active area of MOS transistors from STI oxide field (Fig. 2.20) fundamentally alters electrical characteristics of the MOS transistors [117]. As one of the most important parameter of the MOS transistor, which is modified, is drain current I_D of MOS transistors in the sub-threshold regime (Fig. 2.21b, [117]).

The hump effect is understood as a drawback in downscaling of IC MOSFETs technology processes and should be respected during the front-end design. For that reason, the equivalent circuit of MOSFETs should be modeled as it is depicted in Fig. 2.21a.

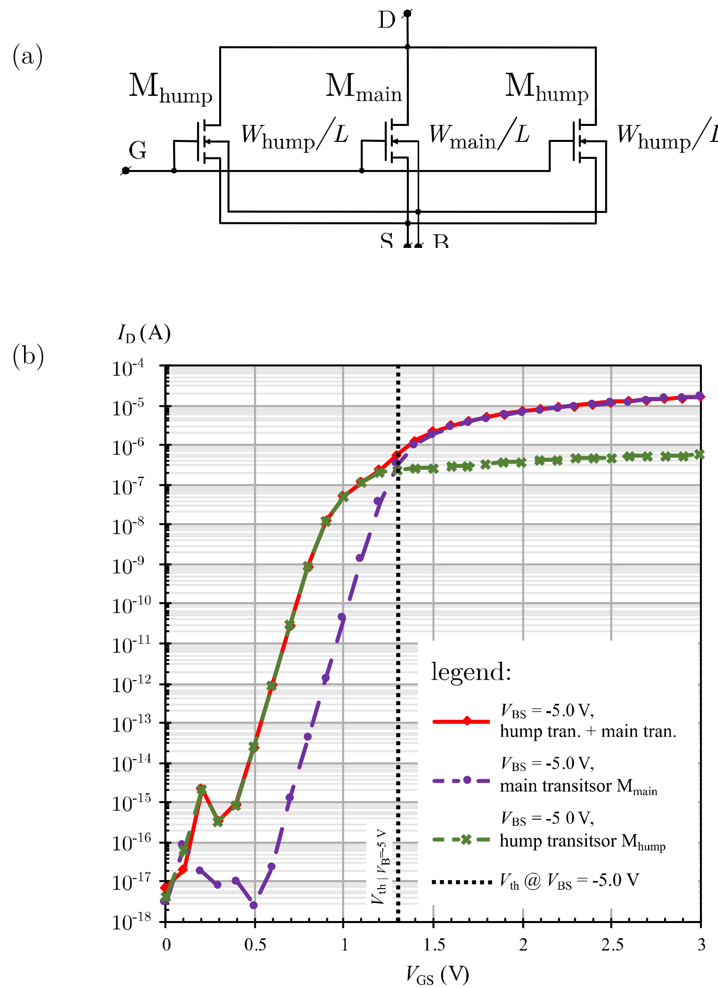


Fig. 2.21: Equivalent circuit of a hump effect (a) and hump effect on I_D - V_{GS} characteristics of MOS transistors with body effect $V_B = -5.0$ V.

2.2 Review of Different MOSFET Gate Shape Architectures

The MOSFET gate shapes play a crucial role in advanced MOSFET's enhancement techniques. The modification of the gate shape is still the actual topic, and it needs to be deeply investigated in order to develop better analytical models of them. In this part, there are reviewed many different types of gate shapes with their advantages and disadvantages. The topologies in this section are categorized into three parts. The first part is enclosed layout shape topologies, the second part is the not enclosed layout shape topologies, and the last is the 3D layout shape topologies.

After this section, there is a chapter that describes a diamond structure, which is the goal of this dissertation thesis. In this chapter, there is a diamond layout shape analytically analyzed, simulated, evaluated, and validated by measurements.

2.2.1 **Enclosed Layout Shape Topologies**

As the name suggests, in the enclosed-layout transistors (ELTs), one of the diffusions, either the source or the drain, is completely surrounded by the polysilicon gate. The following text presents different enclosed-layout transistors topologies such as square enclosed layout shape topology, rectangular enclosed layout shape topology, octagonal enclosed layout shape topology, annular enclosed layout shape topology, and circular enclosed layout topologies and its effective aspect ratio width to length.

(a) Square enclosed layout topology

Square enclosed layout topology is depicted in Fig. 2.22 [118]. As the electric field under the corners is not uniform (Fig. 2.23a), the aspect ratio (W/L) has to be calculated such as the sum of four individuals parts (transistors) depicted in Fig. 2.23b (T1, T2, T3, and T4). These parts have been realized by decomposition of the main transistor into four segments. After that splitting, each transistor has to be solved separately, as it is described in Fig. 2.24 [119]. To solve each transistor, the conformal mapping has been used to calculate the electrical field along with the metallic layers and to define the borderline between the edge and corner transistors [119].

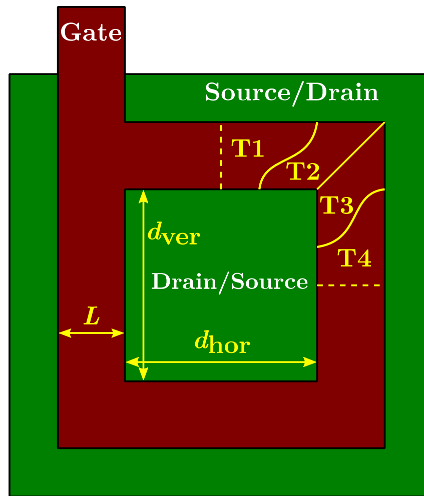


Fig. 2.22: Square gate-enclosed transistor

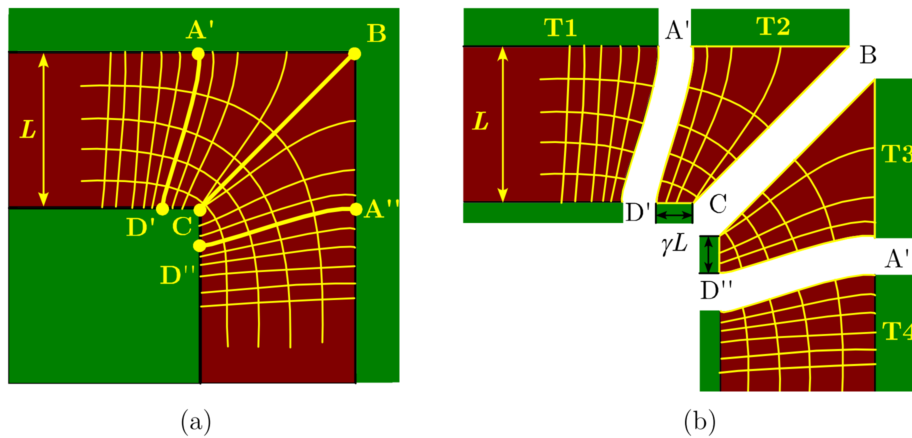


Fig. 2.23: Non-uniform geometry of the electrostatic field in square MOSFETs (a), decomposition of the square MOSFET into two edge transistors (T1 and T4) and two corner transistors (T2 and T3).

As a result of this analysis are effective aspect ratio expressions for T1 (2.20), T2 (2.21), and for the final square layout (2.24).

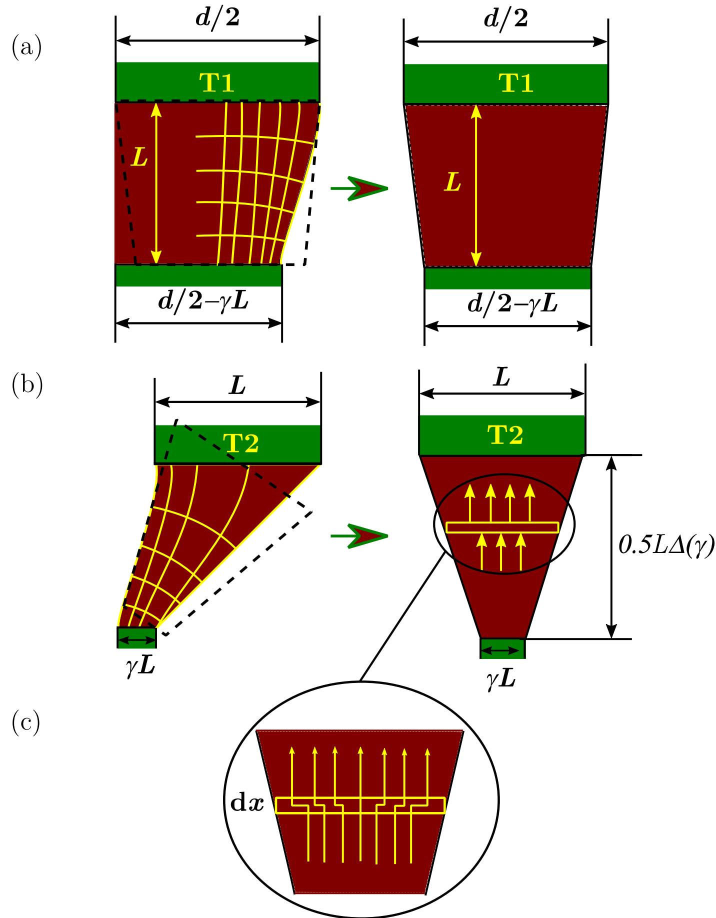


Fig. 2.24: Approximation of the edge transistor T1 with an equivalent trapezium (a), approximation of the corner transistor T2 with an equivalent trapezium (b), enlargement showing the method adopted to preserve current continuity during the integration for drain current (c).

$$\left(\frac{W}{L}\right)^{\text{square enclosed}}_{\text{T1,eff}} = \frac{\gamma}{\ln\left(\frac{d}{d-2\gamma L}\right)} \tag{2.20}$$

where d is a drain/source size (i.e. the diffusion side length enclosed by gate terminal d_{hor}, and d_{ver} in Fig. 2.22). The γ parameter has been found to be almost technology independent, 0.05 being the best fit to the experimental data [120]. For very large

L values, $\gamma L \approx d/2$, and only the contribution of the corner transistor is important. The L is a length of enclosed MOSFET as is depicted in Fig. 2.22.

$$\left(\frac{W}{L}\right)_{\mathrm{T2,eff}}^{\mathrm{square\ enclosed}} = \frac{1}{\Delta(\gamma)} \frac{1-\gamma}{\ln\left(\frac{1}{\gamma}\right)} \tag{2.21}$$

$$\Delta(\gamma) = \frac{1}{2}\sqrt{\gamma^2 + 2\gamma + 5} \tag{2.22}$$

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{square\ enclosed}} = 4 \cdot 2\left(\left(\frac{W}{L}\right)_{\mathrm{T1,eff}}^{\mathrm{square\ enclosed}} + \left(\frac{W}{L}\right)_{\mathrm{T2,eff}}^{\mathrm{square\ enclosed}}\right) \tag{2.23}$$

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{square\ enclosed}} = 8\left(\frac{\gamma}{\ln\left(\frac{d}{d-2\gamma L}\right)} + \frac{1-\gamma}{\frac{1}{2}\sqrt{\gamma^2 + 2\gamma + 5}\,\ln\left(\frac{1}{\gamma}\right)}\right) \tag{2.24}$$

(b) Rectangular enclosed layout topology

The rectangular enclosed layout topology is depicted in Fig. 2.25. Instead of the square shape (Fig. 2.22), the rectangular enclosed layout topology has two different gate lengths L_1 and L_2. The calculated expressions (2.24) for the aspect ratio can also be used for rectangular transistors designed by stretching the square shape. In this case, has been added the contribution of the linear regions generated by the stretching. When assuming a rectangular layout with channel lengths L_1 and $L_2 = mL_1$ (Fig. 2.25), we obtain the aspect ratio for the rectangular shape (2.25).

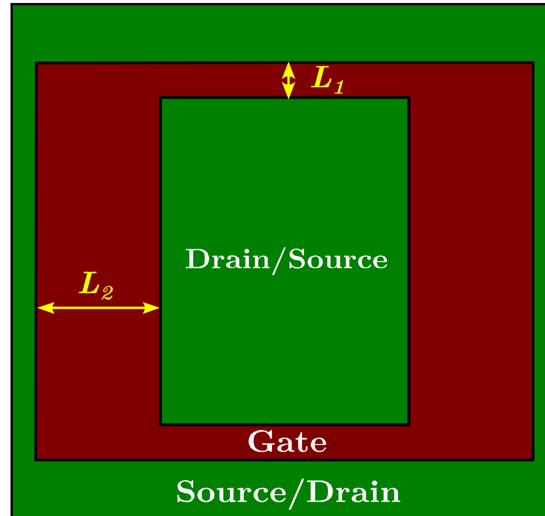


Fig. 2.25: Rectangular enclosed layout topology with two different length L_1 and L_2.

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{rect enclosed}} = 4\left(\frac{\gamma}{\ln\left(\frac{d}{d-2\gamma L_1}\right)} + \frac{\gamma}{\ln\left(\frac{d}{d-2m\gamma L_1}\right)}\right) + 4\cdot 2\left(\frac{1-\gamma}{\frac{1}{2}\sqrt{\gamma^2+2\gamma+5}\,\ln\left(\frac{1}{\gamma}\right)}\right) \tag{2.25}$$

(c) Octagonal enclosed layout topology

The octagon gate shape MOS transistor (Fig. 2.26) is promising in terms of driving capability for the short channels MOSFET, but its capability is significantly reduced with the large channels MOS transistors [121]. The aspect ratio of the octagonal gate shape MOS transistor is given by the following expression (2.26):

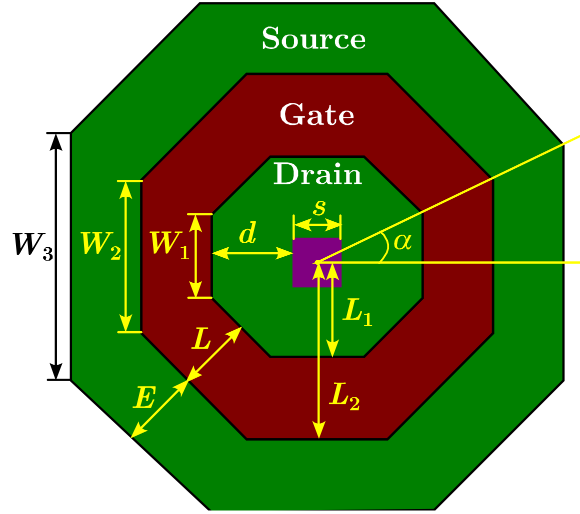


Fig. 2.26: Basic top layout view of the octagon MOS transistor.

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{octagon}} = 2n\frac{\tan(\alpha)}{\ln\left(\frac{W_2}{W_1}\right)} \tag{2.26}$$

Moreover, besides, it also be shown that the total layout area (2.27) is bigger than the total area of RLS MOSFET (2.30)(2.29). The following expression gives the total area of octagonal MOSFET:

$$A_{\text{octagon}} = n(d + L + E)^2 \tan(\alpha) \tag{2.27}$$

$$L = L_2 - L_1 \tag{2.28}$$

where an L is the channel length, L_1 and L_2 are lengths from the center of the structure to the inner edge of the gate and the outer edge of the gate, respectively. An E the extension of the source diffusion over the gate and an $x_{\text{d,drain}}$ is the drain

distance between the center of the inner diffusion and the gate taking the drain as the inner diffusion and the source as the outer diffusion, thus,

$$x_{\mathrm{d,drain|min}} = \frac{s}{2} + d \tag{2.29}$$

being an s the minimum contact size and a d the minimum distance between the drain contact and the edge of the gate. The total layout area of a conventional transistor, on the other hand, is:

$$A_{\mathrm{rect}} = W(4x_{\mathrm{d,drain}} + L) \tag{2.30}$$

The increase in the total layout area has a strong dependence on the L. In the case of the large L, the increase in the total layout area overcomes the benefit of a reduced drain area that is limiting the driving capability of the device. However, if we consider a short-channel device, the driving capability of the device is having even better performance than that of conventional layouts.

As another example of the application of the octagon layout gate shape MOS transistor, is, for example, a using it such as a stress sensor for eight direction stress detection Fig. 2.27 [122, 123].

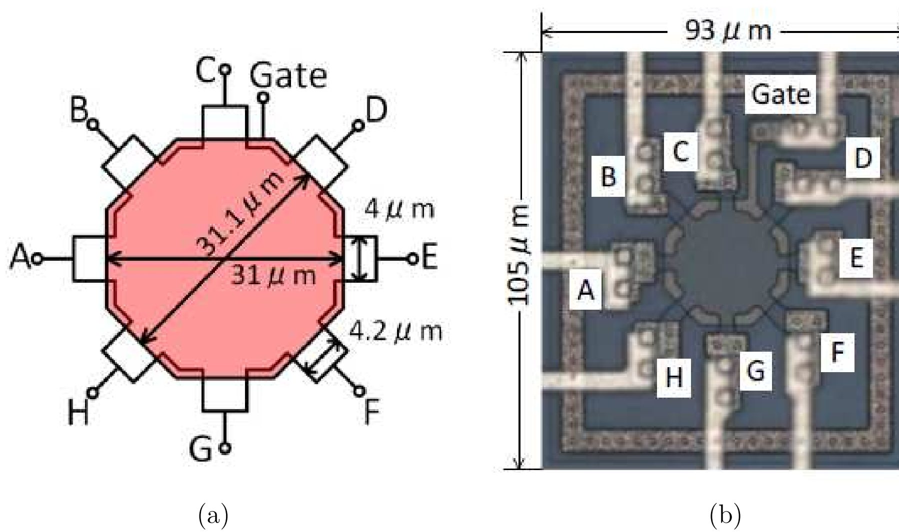


Fig. 2.27: Octagon MOSFET device layout (a), microphotograph (b) [123].

(d) Annular enclosed layout topology

The annular enclosed layout topology (Fig. 2.28), is a composition of three parts, labeled as T1, T2, and T3. The first part corresponds to the linear edges of the transistors, the second to the corners without the 45° cut, which is considered separately from the third party. The parts T1 and T2 have been described in the previous section. The third contribution is added from the linear transistor corner with channel width c and length $L\sqrt{2}$ (2.31). Each of these parts contributes to calculating the total aspect ratio width to length (2.32) - (2.34).

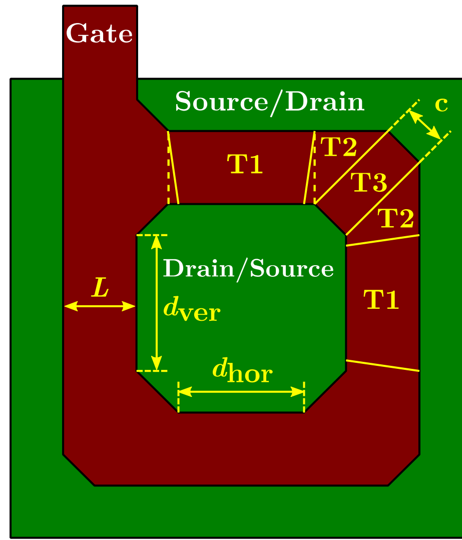


Fig. 2.28: Annular enclosed layout topology with the decomposition of the broken corner square MOSFET into edge (T1), corner (T2), and linear corner.

$$\left(\frac{W}{L}\right)_{\mathrm{T3,eff}}^{\text{annular enclosed}} = \frac{c}{L\sqrt{2}} \tag{2.31}$$

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\text{annular enclosed}} = \left(\frac{W}{L}\right)_{\mathrm{eff}}^{\text{square enclosed}} + 4\left(\frac{W}{L}\right)_{\mathrm{T3,eff}}^{\text{annular enclosed}} \tag{2.32}$$

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\text{annular,Giraldo}} = 8\left(\frac{\gamma}{\ln\left(\frac{d}{d-2\gamma L}\right)} + \frac{1-\gamma}{\frac{1}{2}\sqrt{\gamma^2+2\gamma+5}\,\ln\left(\frac{1}{\gamma}\right)} + \frac{1}{2}\frac{c}{L\sqrt{2}}\right) \tag{2.33}$$

In [120] the expression formula for annular gate-enclosed MOSFET is a little bit different (2.34)

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{annular,Anelli}} = 4\frac{2\gamma}{\ln\left(\frac{d}{d-2\gamma L}\right)} + 2K\frac{1-\gamma}{\frac{1}{2}\sqrt{\gamma^2+2\gamma+5}\ln\left(\frac{1}{\gamma}\right)} + 3\frac{c}{L\sqrt{2}} \tag{2.34}$$

where a K is a geometry dependent, being 7/2 for short-channel transistors ($L \leq 0.5\ \mu m$) and 4 for longer devices. The other parameters have been already described in the previous subsection "Square enclosed layout topology".

(e) Circular enclosed layout topology

The model for a circular enclosed layout MOSFET (Fig. 2.29) can be easily developed starting from the basic long channel equations in cylindrical coordinates. In this device, the electric field is circularly symmetric.

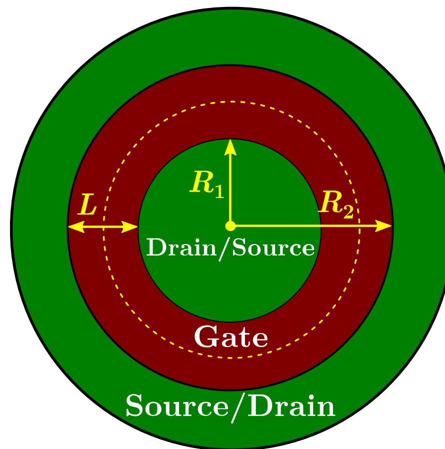


Fig. 2.29: Gate-enclosed circular transistor shape.

The aspect ratio for the circular enclosed layout topology is defined as

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{circular}} = \frac{2\pi}{\ln\left(\frac{R_2}{R_1}\right)} \tag{2.35}$$

where R_1 and R_2 are radii between the source and drain as it is depicted in Fig. 2.29.

The aspect ratio of the circular enclosed layout topology can also be defined by using results related to the middle-channel approximation (dashed line in Fig. 2.29) [119], where $L = R_2 - R_1$ and $W_{1/2} = \pi(R_1 + R_2)$:

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{circular,mid}} = \frac{W_{1/2}}{\text{L}} \frac{1}{\left(\frac{1}{2}+\frac{R_1}{L}\right)\ln\left(1+\frac{L}{R_1}\right)} \tag{2.36}$$

If the inner radius (R_1) is greater than the gate length, i.e., $L \ll R_1$, the middle-channel approximation is satisfactory. Instead, for the long channel devices, the middle-channel calculation overestimates the effective aspect ratio [119].

(f) Circular enclosed layout topology with overlapping

The layout style named overlapping circular-gate transistor (O-CGT) is a layout style strategy of conventional CGT (Fig. 2.30), where the gate terminals of MOSFET are overlapped (Fig. 2.31). This strategy allows the overlapping of circular gates from neighboring cells.

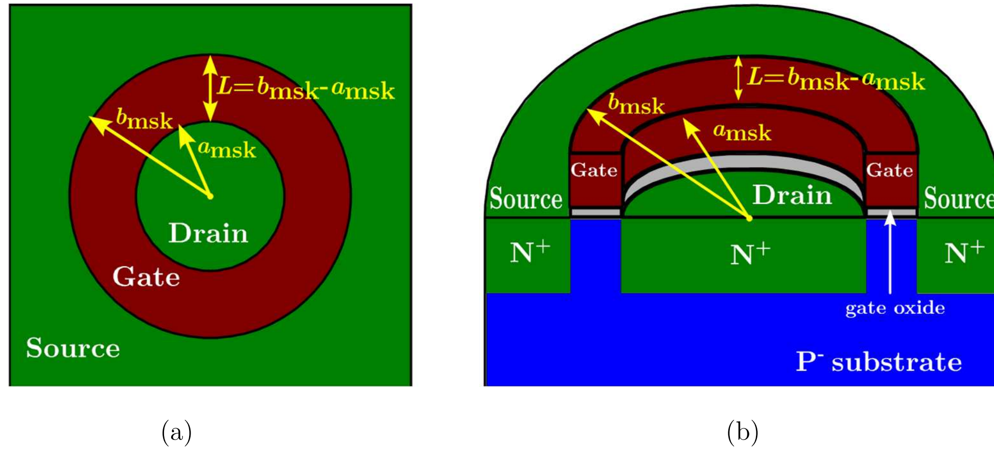


Fig. 2.30: Basic top-view layout of conventional CGT (a) and its cross section (b).

Using a conventional notation, the CGT effective aspect ratio [124] is equal to the following expression:

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{CGT}} = \frac{2\pi}{\ln\left(\frac{b_{\text{msk}}}{a_{\text{msk}}}\right)} \tag{2.37}$$

where a_{msk} and b_{msk} are internal and external radius of the gate annulus, respectively, and the subscript msk stands for a mask of drawn layers. The channel length of this MOS transistor shape L_{CGT} is defined as

$$L_{\mathrm{CGT}} = b_{\mathrm{msk}} - a_{\mathrm{msk}}. \tag{2.38}$$

The effective aspect ratio of O-CGT [125] depicted in (Fig. 2.31) is defined by the following expression:

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{O\text{-}CGT}} = \frac{360° - 4\alpha}{360°}\frac{2\pi}{\ln\left(\frac{b_{\mathrm{msk}}}{a_{\mathrm{msk}}}\right)} \tag{2.39}$$

where α is an internal angle that defined the MOSFET gate overlaps.

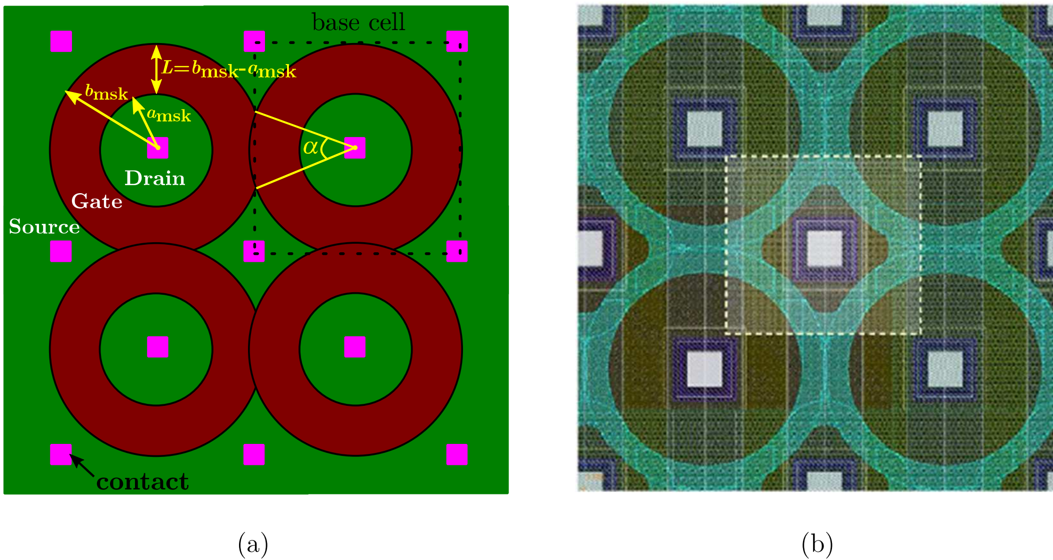


Fig. 2.31: O-CGT layout top view (a) and its alternative physical design (b).

The aspect ratio of O-CGT is lower in comparison to the CGT effective aspect ratios and expresses the drain-source current driving loss. Despite this constraint, O-CGTs structures compete with traditional doughnut CGT structures and fingerstyle rectangular transistors, as discussed next. To facilitate this comparison, a figure-of-merit (FOM) has been defined by the following expression

$$\text{FOM} = \frac{\left(\frac{W}{L}\right)}{A} \quad (2.40)$$

where A is the transistor layout area. The expression (2.40) introduces and reflects the driving capability of the device by its active area.

The conclusion of this structure in the study [125] is, that for $a_{\mathrm{msk}} < 1.25\ \mu\mathrm{m}$ the FOM is larger for O-CGT in comparison to Rectangular Layout Shape (RLS) MOS transistor. As the next conclusion is that for $a_{\mathrm{msk}} < 1.42\ \mu\mathrm{m}$ the area of the O-CGT is smaller in comparison with RLS MOS transistor and CGT.

The drawback of this method is in increasing a gate capacitance C_{GC} up to 5 %. The next drawback is associated with distributed RC elements of the gate terminal. This drawback can be mitigated by placing a channel of metal routing between clusters to improve the gate and substrate [125]. As the next drawback for low voltage application is an unbalanced area for drain and source terminals that affects higher specific resistance-on the area. In some cases, there can happen, just one drain or source contact can be used.

(g) Application

In general, the transistors with gate-enclosed layout topology can be used in radiation environments to prevent the onset of any leakage current through a radiation-induced lateral path under the bird's beak or at the shallow trench isolation corner Fig. 2.33 [118] of the MOS transistor. This special layout approach helps to maintain leakage current of MOS transistors at a low level even after irradiation, in contrast to a linear layout MOS transistor, where leakage current could increase by orders of magnitude [126]. It improves the reliability of electronics in the proximity of the ionizing radiation in particular high energy physics, nuclear power, or space applications. That hardening technique is named as Radiation Hardening by Design (RHBD).

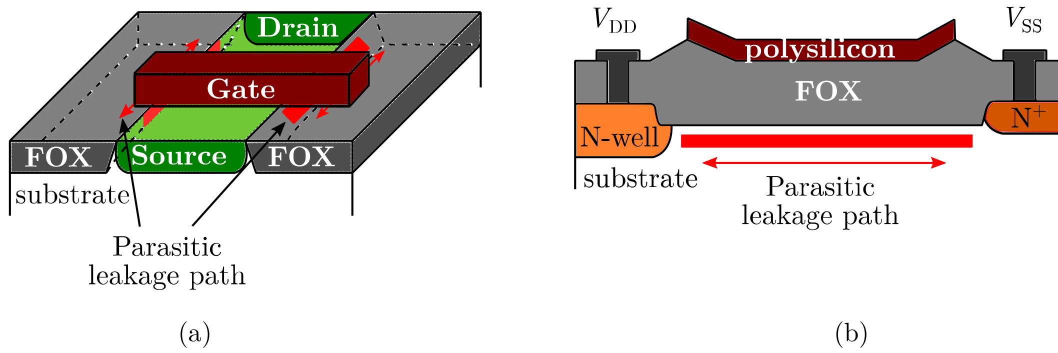


Fig. 2.33: Representative cross section of leakage current path between source and drain of the same device (intra-device) (a), and between adjacent n-well regions of different devices (inter-device) (b).

A comparison example between standard MOSFET and gate-enclosed MOSFET is depicted in Fig. 2.32 [118]. The general area penalty related to enclose the gate, when compared to standard MOS device, incurs in approximately 15 % in case of a single transistor, 150 % for an inverter cell with an area discrepancy tending to increase in case of more complex cells [118].

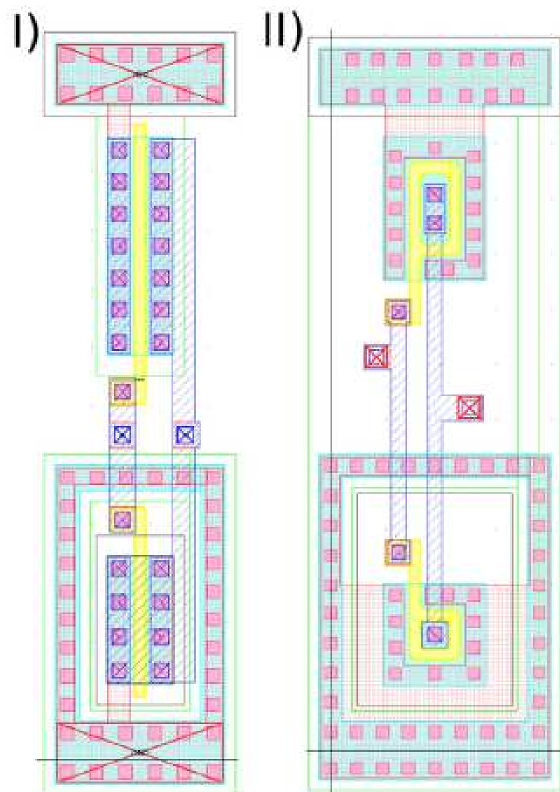


Fig. 2.32: Physical design example of standard MOSFET (I) and gate-enclosed MOSFET device (II) [118].

2.2.2 **Not Enclosed Layout Shape Topologies**

(a) Diamond Gate Layout Shape Based on the "Longitudinal Corner Effect"

Description of the Diamond Layout Shape (DLS) has been recently published in [127, 128]. In these publications, the DLS MOS transistor description is based on two effects. The first effect is the "corner effect" along the channel longitudinal (parallel) direction named "Longitudinal Corner Effect" (LCE) (Fig. 2.34a) [127]. In considering LCE the gate hexagonal geometry can be composed of two trapezoidal geometries. The second effect is a Parallel Association of MOSFET with Different Channel Lengths Effect (PAMDLE) (Fig. 2.34b) [128] with the

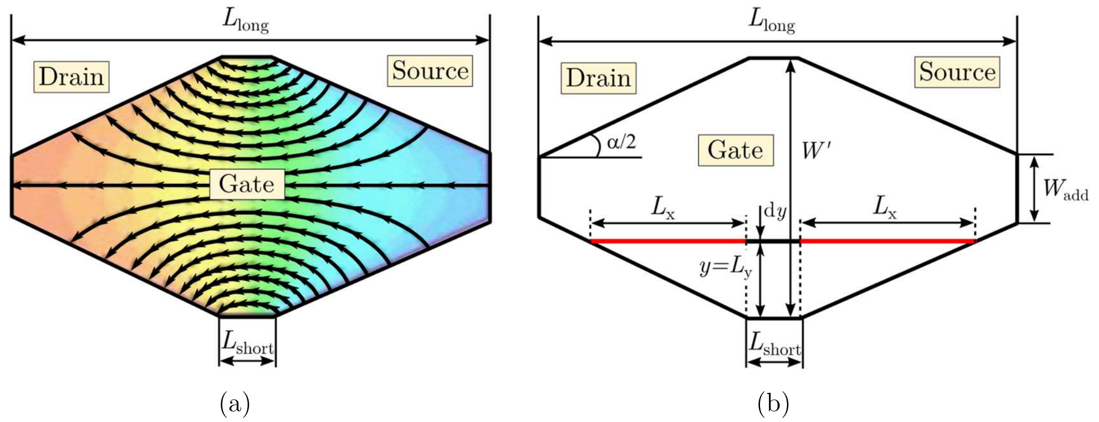


Fig. 2.34: The 3D numerical simulation of longitudinal electrical field (LEF) along the channel of the diamond layout shape MOSFET (a), diamond channel electrically treated as a parallel association of an infinite number of MOSFETs (PAMDLE) with the infinitesimal width (dy) and different channel length (L_i).

infinitesimal narrow width (dy) and different channel length (L_i). In the case, where W_{add} is equal to zero, the different channel length L_i is defined by the following expression:

$$L_i = L_{short} + 2\,L_x = L_{short} + 2\frac{y}{\tan\left(\frac{\alpha}{2}\right)} \tag{2.41}$$

where i is an incremental parameter and its maximal value depends on the step dy and the geometric width of MOSFET (W').

The PAMDLE reduces the effective channel length L_{eff} of diamond MOSFET in comparison of the rectangular MOSFET counterpart. The first-order approximation of effective channel length is given as an average channel length of the trapezoidal regions as is indicated in equation (2.42)

$$L_{\text{eff}} = \frac{L_{\text{short}} + L_{\text{long}}}{2} \tag{2.42}$$

where a L_{short} is a length of the transistor gate on the up/downsides (see Fig. 2.34a), a L_{long} is a length of the transistor gate in the middle of the transistor structure.

Taking in the account (2.42), the first-order aspect ratio approximation of DLS MOSFET is described based on the LCE [127] (2.43) for angle α in the range from 0° to 90° and (2.44) for angle α in the range from 90° to 180°, respectively. That effective aspect ratio is calling as $(W/L)_{eff,LCE}$.

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LCE}} = 2\left(\frac{W'}{L_{\text{short}} + L_{\text{long}}}\right)\sqrt{2(1+\cos\alpha)} \tag{2.43}$$

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LCE}} = 2\left(\frac{W'}{L_{\text{short}} + L_{\text{long}}}\right)\sqrt{2+\cos\alpha} \tag{2.44}$$

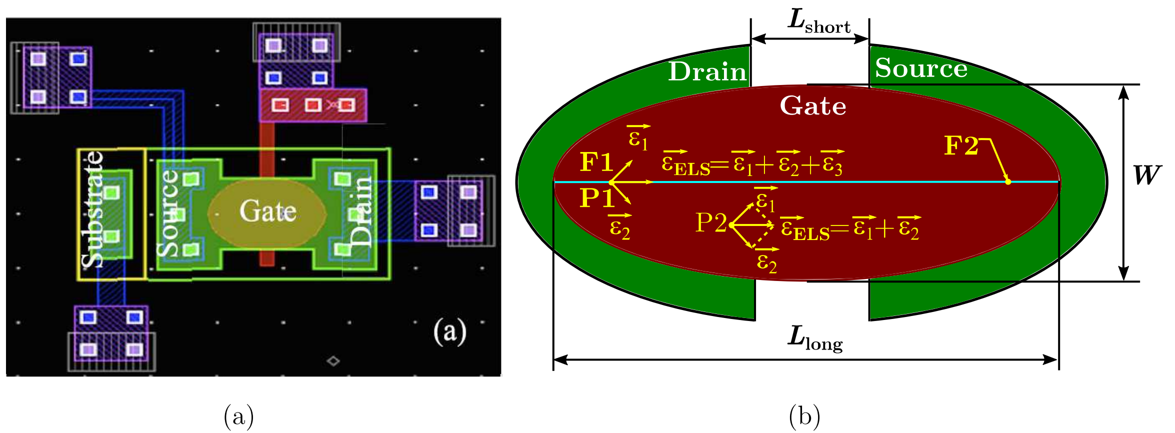
where a W' is a geometric width of the DLS (see Fig. 2.34).

As has been written, all mentioned publications offer only the first-order approximation of DLS, which is not sufficient for high-end applications. The more precise model is under investigation of this dissertation thesis in section 4.1.

(b) Ellipsoidal Gate Shape

The Ellipsoidal gate Layout Shape (ELS) (Fig. 2.35) is the next alternative way to implement and to improve the MOSFET performances. The goal of this structure is to increase the drain-source saturation current and to reduce the delay time constant [129]. Furthermore, an ellipsoidal gate shape MOSFET computed from Chi-square distribution tables is the optimal shape, as compared to the rectangular and circular gate shapes because the gate volume is smaller than the other geometries [130]. Unfortunately, in the literatures above, it has not been compared with the other layout shapes such as cylindrical enclosed gate layout shapes, diamond gate layout shape, waffle gate shapes, wave gate shapes etc. The ellipsoidal gate layout shape is promising for the device with an aspect ratio of less than one because the short-channel effect is suppressed [131].

The ellipsoidal gate geometry contains the Longitudinal Corner Effect (LCE) and Parallel Connection of MOSFET with Different Channel Lengths Effect (PAMDLE) Fig. 2.35b [129]. The Fig. 2.35b illustrates the simplified superior view of the ellipsoidal gate layout shape MOSFET (ELS MOSFET), where this transistor, at the point P1, has three longitudinal electric fields (LEFs) components ($\boldsymbol{\varepsilon}_1$, $\boldsymbol{\varepsilon}_2$, and $\boldsymbol{\varepsilon}_3$) in the central straight line. That central line is defined by the focuses F1 and F2 of the ellipse along the channel length. Out of this central line, such as



(a) (b)

Fig. 2.35: The ellipsoidal layout (a) and its superior view (b) with the indications of the LEF vector components in its structure, where L_{short} and L_{long} are the smallest and the highest dimensions of the channel length and W is the channel width, respectively.

for example the point P2, it has only two LEF components (ε_1, and ε_2), due to the drain bias (V_{DS}). The resultant LEF (ε_{ELS}) which is given by $\varepsilon_1 + \varepsilon_2 + \varepsilon_3$ or $\varepsilon_1 + \varepsilon_2$, depends on if point P is considered along the channel region or not. In the case of the ELS MOSFET, the resultant LEF is higher than the one observed in the conventional rectangular layout shape, regarding the same gate area and bias conditions.

Based on the PAMDLE approach, the aspect ratio $(W/L)_{eff,ellipsoidal}$ is given by the following equation (2.45) reported in [129] such as:

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{ellipsoidal}} = \frac{W}{L_{\text{eff}}} = \frac{\mathrm{W}}{\dfrac{L_{\text{long}}}{\arcsin\left(\sqrt{1-\dfrac{L_{\text{short}}^2}{L_{\text{long}}^2}}\right)}} \tag{2.45}$$

where L_{short} and L_{long} are the smallest and the highest dimensions of the channel length and W is the channel width, respectively.

In order to compare the electrical performance of the ELS MOSFET and an equivalent conventional rectangular MOSFET (RLS MOSFET) counterpart with both presenting the same A_{gate}, it is necessary that ELS MOSFET has L_{long} equal to $4L/\pi$ [129]. The following Tab. 2.4 [131] summarizes the improvements of ellipsoidal shape in compare to RLS MOSFET shape.

Tab. 2.4: The ELS MOSFET and RLS MOSFET dimensions, A_{gate}, L_{eff}, and the L_{eff} reduction in relation to the RLS MOSFET in counterpart in percentage due to the PAMDLE effect calculated by equation (2.46).

Rectangular shape			Ellipsoidal shape				$(L_{eff}-L)/L$
W	$L = \frac{L_{long}\pi}{4}$	A_{gate}	W	L_{short}	L_{long}	L_{eff}	x100
(μm)	(μm)	(μm²)	(μm)	(μm)	(μm)	(μm)	(%)
5.950	9.975	59.35	5.950	1.050	12.70	8.530	-14.4
5.950	7.000	41.65	5.950	1.050	8.913	6.140	-12.3
5.950	4.025	23.95	5.950	1.050	5.125	3.760	-6.7

The drawback of this method is that ELS MOSFET is electrically represented as a parallel connection of infinite standard MOSFETs with the same channel width of infinitesimal dimension and different channel lengths ($L_{short} \leq L_i \leq L_{long}$), according to Fig. 2.36. However, the current flow has not straightway but the rounding way to keep the perpendicular angle between equipotential lines and current flow lines (similar in Fig. 2.34). Therefore, the presented estimation is only for the first order approximation.

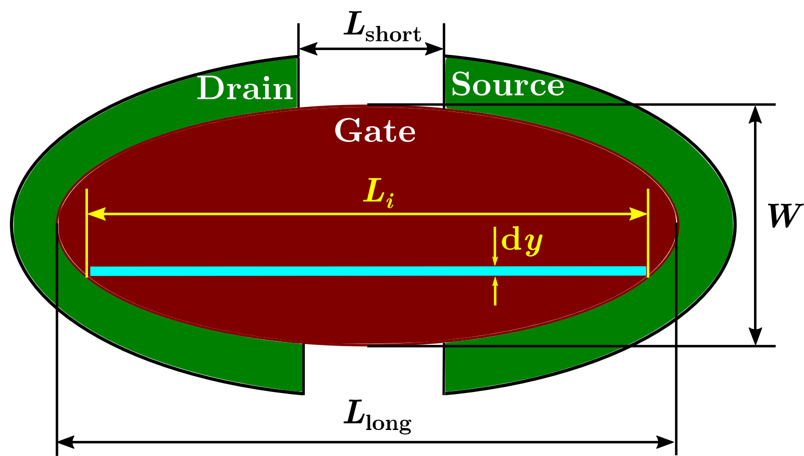


Fig. 2.36: Picture of an ELS MOSFET composed by infinite MOSFETs with aspect ratio of dy/L_i, used to calculate the $L_{eff,ELS}$.

Even, the Computer Aided Design (CAD) layout tools (lC StationlPixys of Mentor Graphics and Virtuoso layout editor of Cadence) are capable of implementing the MOSFETs with any geometric shape (square, rectangle, circle, ellipse, etc.), regarding the planar MOSFETs technology, the ellipsoidal MOSFET does not present corners and it tends to present a small influence of the CMOS ICs manufacturing process variations in the geometric parameters (aspect ratio and area). It is understood as another disadvantage of this structure.

(c) Waffle Gate Shape

The waffle structure provides an effective trade-off between device area and on-resistance in comparison with conventional multi-finger layouts. Waffle structures have diagonal (Fig. 2.37a) [132] or orthogonal (Fig. 2.37b) [133] source and drain metal orientation, respectively. Generally, in the case of the same MOSFET aspect ratio width to length, the diagonal structures have better performance than orthogonal structures in terms of saving area [134]. The waffle layout is beneficial to many mixed-signal circuits for a compact design of wide MOSFET [132].

In [132], and [135], respectively, the waffle structures with diagonal source/drain metal orientation exhibit up to a 25 % reduction in overall on-resistance dependently on the used area. With increasing the MOSFET area, the saving of the area is increasing, too.

The analytical effective aspect ratio $(W/L)_{\text{eff,waffle_1}}$ and area $A_{\text{waffle_1}}$ expressions for diagonal waffle MOSFET structures have been described in [136] by the following expression (2.47), and (2.48):

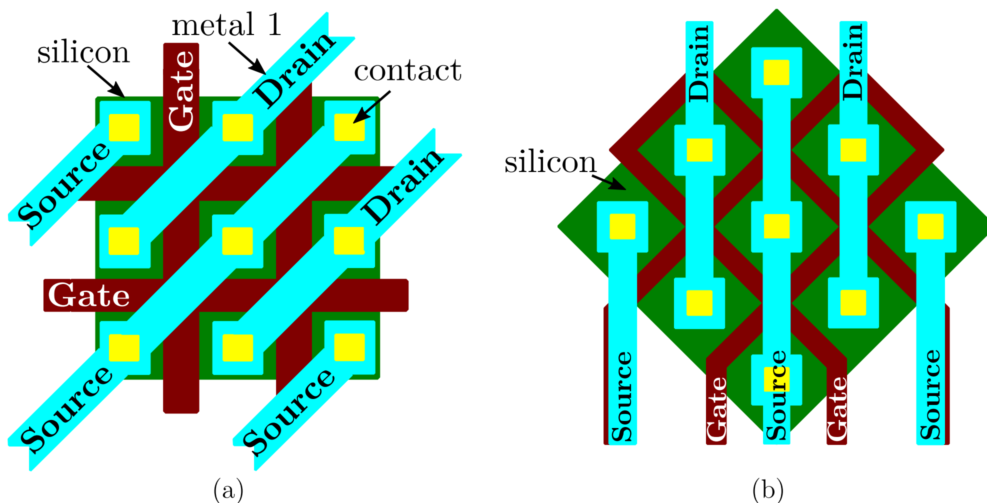


Fig. 2.37: Waffle MOSFET structures with the interconnection for the source and drain terminals oriented diagonal (a) or orthogonal (b).

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{waffle_1}} = 2\frac{2(d_2 + 2d_3) + 0.55d_1}{d_1} \tag{2.47}$$

$$A_{\text{waffle_1}} = \frac{d_1(d_1 + d_2 + 2d_4)^2}{2(d_2 + 2d_3) + 0.55d_1} \tag{2.48}$$

where a d_1 is a poly width, a d_2 is a contact opening, a d_3 is a contact to poly spacing. In [134], it has been described more deeply by the following expressions (2.49), and (2.51), respectively.

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{waffle_2}} = \frac{d_5(N_{\text{xWd}} + N_{\text{yWd}} + 2N_{\text{xWd}}N_{\text{yWd}})}{d_1} + N_{\text{xWd}}N_{\text{yWd}}WL_{\text{B}} \tag{2.49}$$

$$WL_{\text{B}} = \frac{5.44 - 1.146\left(\frac{L'}{W'}\right) + 0.56\left(\frac{L'}{W'}\right)^2 - 7\cdot 10^{-4}\left(\frac{L'}{W'}\right)^3}{9.719 - 2.071\left(\frac{L'}{W'}\right) + \left(\frac{L'}{W'}\right)^2} \tag{2.50}$$

where an N_{xWd} is a number of gate fingers in X-axis direction and an N_{yWd} is a number of gate fingers in Y-axis direction. W' and L' are shown in Fig. 2.38.

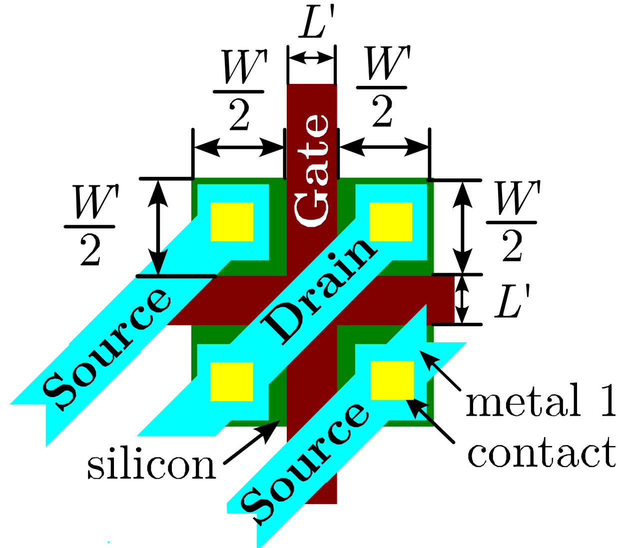


Fig. 2.38: The 2D cross diagonal waffle structure.

$$A_{\text{waffle_2}} = (d_5 + (d_1 + d_5)N_{\text{xWd}})(d_5 + (d_1 + d_5)N_{\text{yWd}}) \tag{2.51}$$

where $d_5 = d_2 + 2d_3$.

In [137], the waffle structure has been also used to improve the matching of current mirror topology (Fig. 2.39). There, it has been shown that the two waffles structures can offer significantly better matching performance than the two-segment common centroid structure in the presence of linear parameter gradients. It is also observed that the matching performance of the waffle mirror structure for a fixed active area improves when the drain contacts are moved farther from the source contact. In this simulation, the distance X was kept at $(3/16)\,W$, R was $(3/8)\,W$ and the drain diffusions were square with a side length of $(1/8)\,W$.

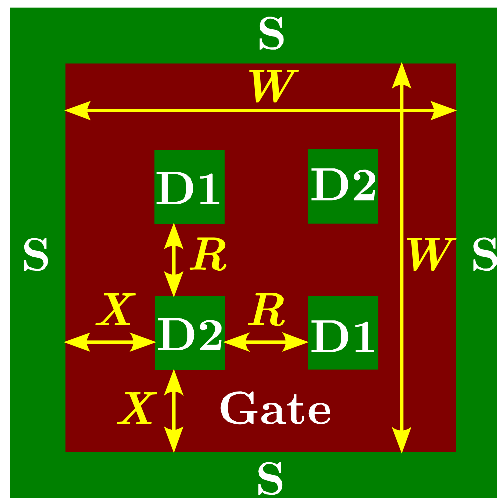


Fig. 2.39: The current mirror topology laid as waffle structure.

The drawback of this method is in the limitation of the uses. For the matching topology, such as depicted in Fig. 2.39, it compensates just the first order of the variance of the technology process. The second and higher-orders are not compensated, which are very important for the final quality of the layout [138]. The next drawback is associated with the dimension of the source/drain diffusion and contacts. The waffle topology overcomes the conventional layout topology for the case, where the dimension of the contacts is much higher than the dimension of the source/drain area [134].

(d) Wave Shape

The wave MOSFET shape comes from the circular annular gate MOSFET (section 2.2.1(e)). It is realized by cutting it in the middle of the circular structure and shifting of the cut semicircles and connecting themselves. In this way, the “wave” or “S” shape is composed (Fig. 2.40a,b) [139]. The wave layout style can be implemented by using any planar IC CMOS manufacturing processes which are used to implement the circular annular gate MOSFET.

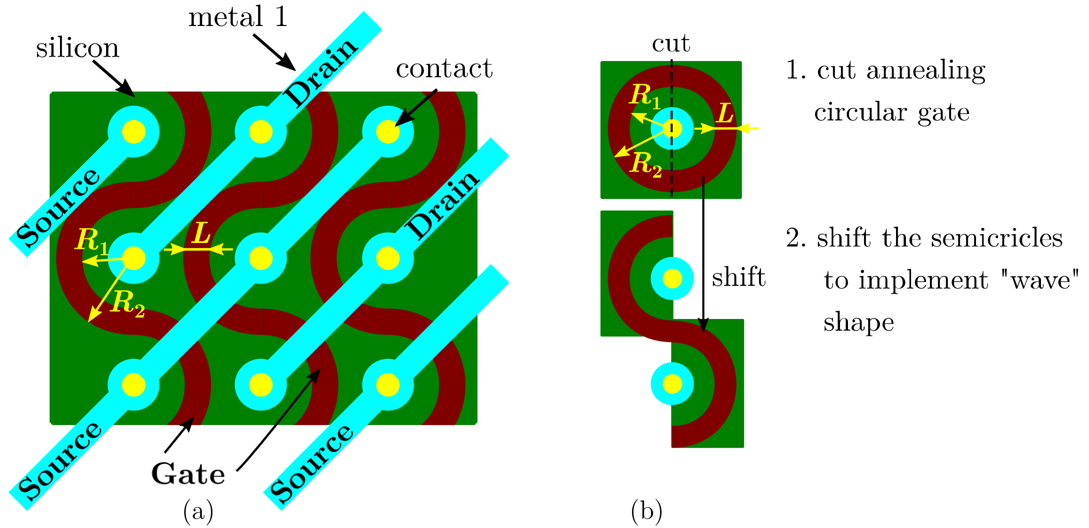


Fig. 2.40: Layout view of the wave MOSFET structure (a) and its composition/realization (b).

The wave MOSFET owns the following important effects: the high Longitudinal Electrical Field (LEF) that is responsible for increasing the drain current in the device channel up to 25 % [140], and special behavior of the Bird’s Beak Regions (BBR) in terms of radiation effect. The wave MOSFET varied about 13.2 % less after the Total Ionizing Dose (TID) (1.5 Mrad) in comparison to its equivalent rectangular transistor [140].

The aspect ratio for the wave shape is given by following equation (2.52) [141]

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{wave}} = \frac{2\pi}{\ln\left(\frac{R_2}{R_1}\right)} = \frac{2\pi}{\ln\left(1+\frac{L}{R_1}\right)} \tag{2.52}$$

where an L is a gate length, an R_1 and R_2 are the radiuses that define the beginning and the ending of the channel region of the transistor structure.

(e) Z Gate Shape

The main advantage of the Z layout gate shape (Fig. 2.41) is better tolerance in terms of total ionizing dose in comparison to rectangular gate shape [142]. Although a precise W/L model of the Z layout gate is not available at present, the drain current level of the Z gate layout, when compared with the drain current of a single gate layout with the same W, L is nearly the same [142]. Moreover, it has the advantages of a small footprint, no limitation in W/L design, possible to realize the "long" transistor, and a smaller gate capacitance compared with the enclosed gate layout.

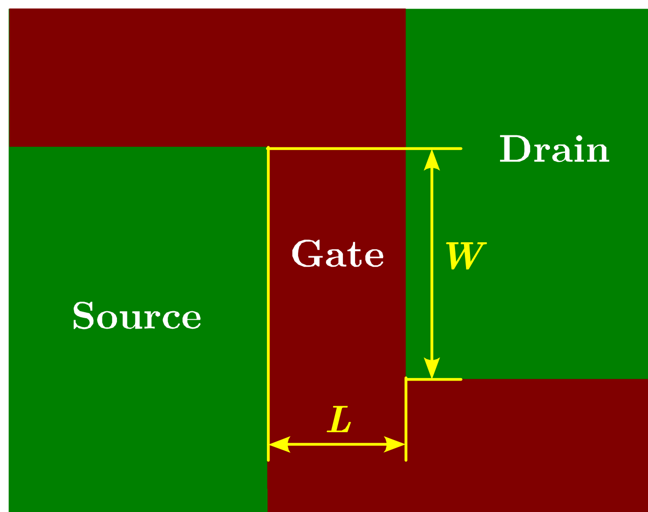


Fig. 2.41: An example of the Z layout gate shape MOSFET.

The threshold voltage of the non-radiation-hardened single gate layout shape (Fig. 2.42a) at pre-radiation and post-radiation (5 Mrad) is 363 mV and 138 mV, respectively, and the total shift is 225 mV. In the case of a gate enclosed layout shape (Fig. 2.42b), it is 374 mV and a close to 374 mV with a total shift of less than 1 mV. For the Z shape (Fig. 2.42c), it is 354 mV and 329 mV with a total shift of 25 mV [142]. The parameters that were used by authors of [142] for the device's simulation are shown in Tab. 2.5. Regarding the V_{th} shift value in descending order, the order of three layout types is the conventional rectangular gate layout shape, the Z gate layout shape, and the enclosed gate layout shape.

Based on the above comparison, the enclosed gate layout achieved the best radiation-hardness performance, and the Z gate layout was more effective in mitigating the TID effect on the transistor than the single gate layout.

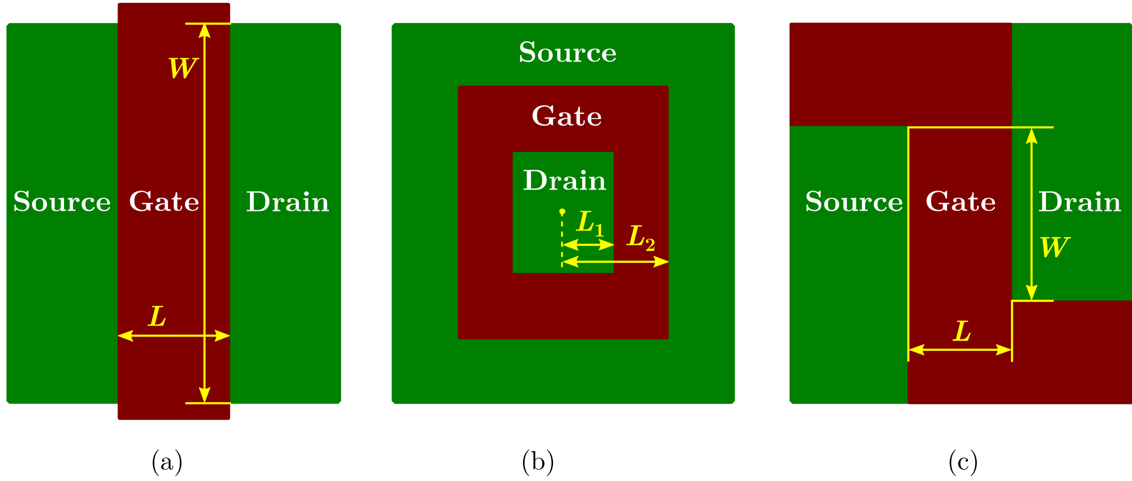


Fig. 2.42: The conventional rectangular gate layout shape (a), the enclosed gate layout shape (b), the Z gate layout shape (c).

Tab. 2.5: The parameters that were used for the device's simulation

Parameter	Value
Length of channel	0.12 µm
Width of channel	0.21 µm
Thickness of n-type poly gate	100 nm
Thickness of gate oxide	2 nm
Doping of source/drain region	$1.0 \cdot 10^{19}$ cm^{-3}
Depth of source/drain region	100 nm
Doping of p-type substrate	$4.0 \cdot 10^{17}$ cm^{-3}

The drawback of this structure is at the missing model and expense of fabrication feasibility due to the asymmetric active area design, as shown in Fig. 2.41.

2.2.3 **"3D" layout shape topologies**

(a) Cylindrical Gate Shape

The cylindrical gate shape, also known as cylindrical gate-all-around (CGAA), nanowire (NW) or surrounding-gate (SG) MOSFETs is shown in Fig. 2.43a. That structure has ultimate gate structures and it is a potential

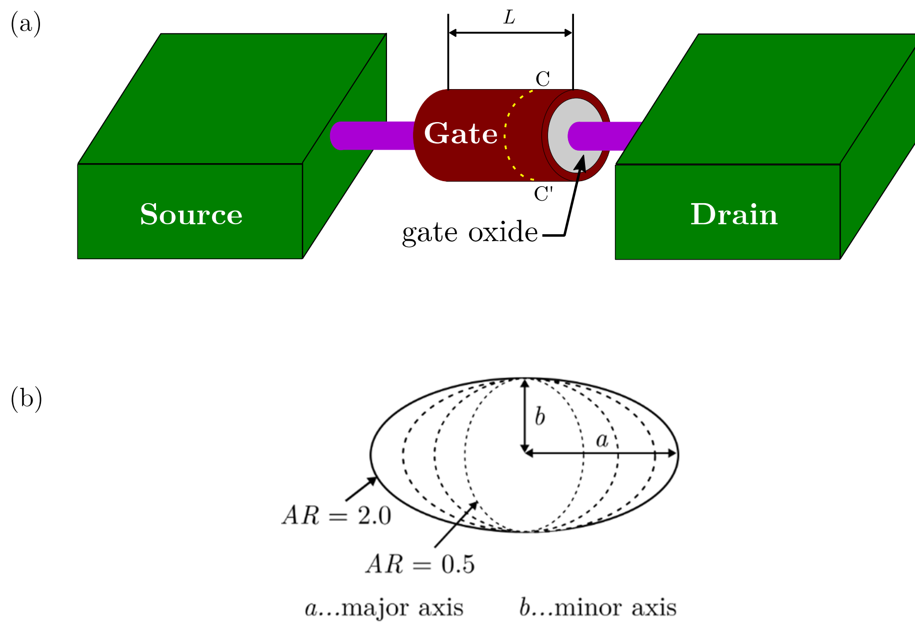


Fig. 2.43: Layout representatoin of cylindric gate shape (a) and its cross-section (b) along c-c' cutting line.

candidate for use in next-generation high-performance nano-devices. Also, into this category, we can sort FinFETs, tri-gate topologies, and other 3D structure toplogies. However, because of the limitations of the fabrication process, a theoretically ideal round shape of the surrounding gate may not always guarantee. These limitations may lead to the formation of an ellipse-shaped surrounding gate with major (a) and minor (b) axes of different widths Fig. 2.43b. Therefore, the aspect ratio $AR_{\mathrm{CGAA\text{-}NW}}$ can vary depending on a and b parameters (2.53). It introduces variability in the effective diameter, which in turn affects the

$$AR_{\mathrm{CGAA\text{-}NW}} = a/b \tag{2.53}$$

performance parameters such for example threshold voltage, DIBL, subthreshold slope, and drain current [143].

The effective aspect ratio width to length of the CGAA-NW MOSFET is defined by [144]

$$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{CGAA-NW}} = \frac{\pi\, d_{\mathrm{eff}}}{L} \tag{2.54}$$

where L is a channel length of the CGAA-NW structure, and a d_{eff} is an effective diameter of the elliptical silicon body given by (2.55) [145]

$$\frac{4\varepsilon_{\mathrm{ox}}}{2\varepsilon_{\mathrm{Si}} d_{\mathrm{eff}} t_{\mathrm{ox}} + \varepsilon_{\mathrm{ox}} d_{\mathrm{eff}}^{2}} = \\ = \frac{2\varepsilon_{\mathrm{ox}}}{2\varepsilon_{\mathrm{Si}} a t_{\mathrm{ox}} + \varepsilon_{\mathrm{ox}} a^{2}} + \frac{2\varepsilon_{\mathrm{ox}}}{2\varepsilon_{\mathrm{Si}} b t_{\mathrm{ox}} + \varepsilon_{\mathrm{ox}} b^{2}} \tag{2.55}$$

where t_{ox}, $\varepsilon_{\mathrm{ox}}$, and $\varepsilon_{\mathrm{Si}}$ are the gate oxide thickness, oxide relative permittivity, and silicon relative permittivity, respectively.

In the case of small d_{eff} (less than 10 nm), the V_{th} is very sensitive to the d_{eff} precision, and its shift is significant [146]. That drawback should be respected in the uses of the devices with an extremely small silicon body radius. As the next drawback is significant V_{th} dependence on geometric aspect ratio $AR_{\mathrm{CGAA-NW}}$ [147] that is not 100 % guaranteed by technology processes.

Currently, the lower drain current transport capability makes the CGAA–NW MOSFET more suitable for digital circuits than for analog circuits. To increase the drain current transport capability, it is possible by nanowires stacking Fig. 2.44 [144].

The drawback of this method in the improvements of electrical performances of planar MOSFETs is the necessity to change the technological process to produce the GAA structures.

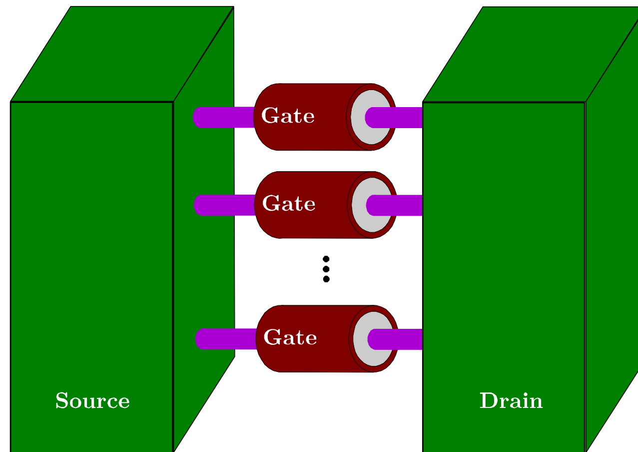


Fig. 2.44: llustration of CGAA-NW MOSFET with the stacked channels (nanowires) to increase drain current capability.

(b) Trapezoidal Gate Shape

It has been found that the trapezoidal gate shape (Fig. 2.45) has better control of the current driving capability of FinFETs than it is for the conventional FinFET [148]. Generally, the FinFET has superior gate control, but in the current driving ability, it suffers from degradation, and the trapezoidal gate shape can improve it. The degradation becomes due to the limited channel width and the parasitic source/drain resistance.

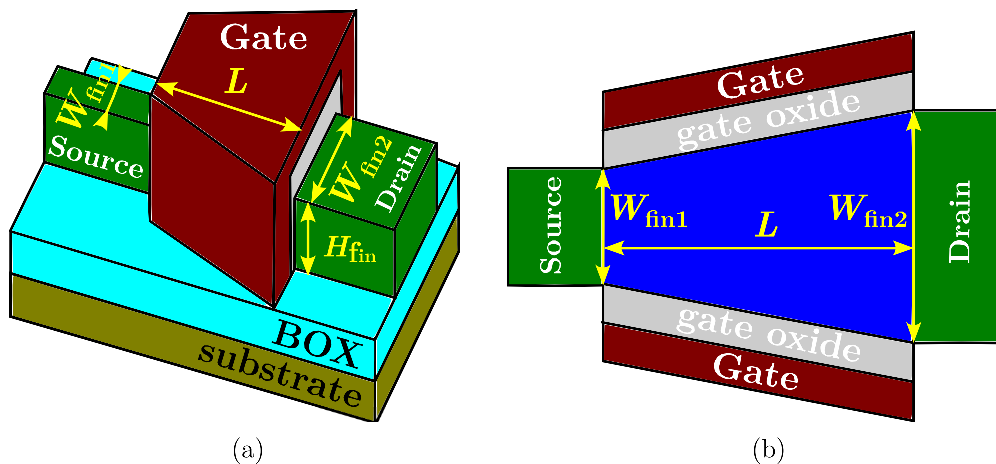


Fig. 2.45: 3D trapezoidal FinFET view (a), 2D cross-section of trapezoidal FinFET (b).

The trapezoidal gate shape can form the sharp carrier concentration gradient along the direction of carrier transport and thus introduce the extra diffusion current component. That structure improves the current driving capability in comparison with the conventional FinFET [148].

The maximum increase of on-state current I_{on} (2.56) compared to the conventional FinFET is 33 % when $\lambda = 1/4$ (Fig. 2.46).

$$I_{on}(\lambda) = \frac{I_{on,\lambda} - I_{on,\lambda=0}}{I_{on,\lambda=0}} \tag{2.56}$$

where $I_{on,\lambda}$ and $I_{on,\lambda=0}$ are on-state currents for the specific parameter λ and conventional FinFET (λ=0). The λ represents the degree of change in fin width and it is defined as the following expression (2.57) [148].

$$\lambda = \frac{W_{fin2} - W_{fin1}}{2L} \tag{2.57}$$

where W_{fin1} and W_{fin2} are the fin widths of trapezoidal gate shape FinFET, and L is a channel length of the FinFET.

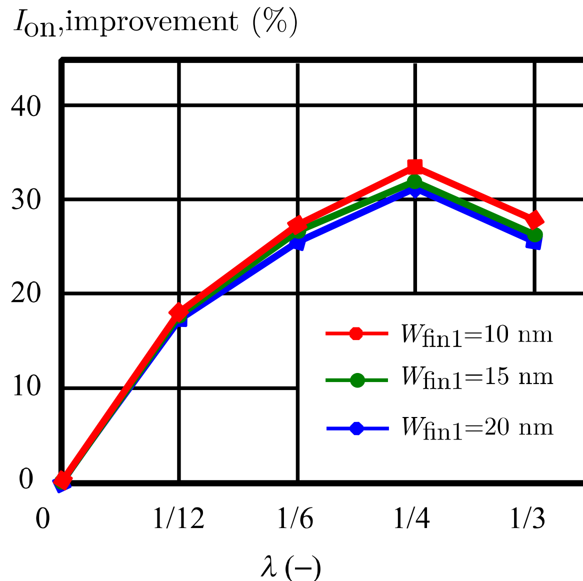


Fig. 2.46: Improvement of I_{on} as a function of the λ with different W_{fin1}.

The fabrication process of this trapezoidal FinFET is a very challenging manufacture since the graded fin width is difficult to be achieved by the double-patterning spacer method [149]. Therefore, this is only the feasibility method to form the graded fin width [148].

Chapter 3

Research Design of the Diamond Layout Shape MOSFET

This chapter describes the design and methodology adopted by this research to achieve the aims and objectives stated in section 1.3 of Chapter 1. Section 3.1 discusses the methodology and the research design used in this thesis. The methodology has been split into the stages by which the methodology has been implemented. These stages are symbolic-numerical computation, numerical computation, 3D device simulation, and experimental measurements. Section 3.2 lists all the instruments used in the study and justifies their use. These instruments are sorted into three categories (software, silicon wafer, and laboratory equipment). The last section 3.3 deals with how the data was analyzed and their analysis setups. These setups (numerical computation setup, simulation setup, and measurement setup) have been defined based on needs to achieve the aims and objectives of this thesis.

3.1 Methodology and Research Design

3.1.1 Methodology

The methodologies used in this work to research the lateral DLS MOSFET structures with better performances compared to the standard rectangular MOSFET structure have been divided into the following different categories:

(a) Symbolic-numerical computation

The growing demand for speed, accuracy, and reliability in scientific and engineering computing has been met by the merging of symbolic and numeric computation [150]. For this reason, an innovative symbolic-numerical expression for the calculation of DLS MOSFETs has been defined for the first time.

In this work, the symbolic-numerical calculation is based on a conformal transformation. Such as the conformal transformation, the Schwarz-Christoffel transformation has been used. More details about this exciting, innovative approach are provided in section 4.1.2 of Chapter 4: Results, Analyses and Discussions.

(b) Numerical computations

In order to verify the innovative symbolic-numeric expression, three different numeric calculations have been proceeded.

- ***Schwarz-Christoffel transformation method:***

  The first one is the Schwarz-Christoffel plugin into MATLAB software. This plugin verifies the correctness of the symbolic-numerical expression mentioned in the previous section. More details about this method is provided in the section 4.1.3.

- ***2D finit element method:***

  As the second approach has been used a 2D finite element method (FEM). This method proves the correctness of the symbolic-numerical expression as well. The FEM analysis have been run in the Agros2D tool.

- ***3D TCAD simulation method:***

  The last one method, which proves the innovative expression is based on the 3D TCAD simulation describes in the following sub-section. In the case of the upper numeric methods, there is a drawback in limitation in precision. The precision in these cases is defined by the number of digits used in the mentioned methods.

(c) 3D device simulations tool

As the optimal simulation tool for verification of the innovative expression the 3D TCAD Silvaco simulation tool has been chosen. It enables to simulate electrical, optical, chemical, crystalline wafer orientation, and thermal behavior of semiconductor devices. Moreover, it provides a physic-based platform to analyze DC, AC, and time domain responses for silicon. For the analyzing of the DLS MOSFET structures the electrical simulations with DC analysis have been run. More details about this 3D TCAD approach are provided in section 4.2.3 of Chapter 4: Results, Analyses, and Discussions.

(d) Experimental measurements

The last methodology used to verify the expression is measurement on the fabricated samples in BCD technology process. More details about this measurement are provided in section 4.2.4 of Chapter 4.

3.1.2 **Research Design**

The research of the lateral DLS MOSFET structures has two main objectives. The first one is to model and define conditions, where the researched DLS MOSFET structures have better electrical performances in comparison to rectangular layout shape (RLS) MOSFET structures. For this part 3D TCAD Silvaco simulation tool, MATLAB software, Agros2D software, Schwarz-Christoffel transformation, Python programming language, and Wolfram Mathematica have been used. To preserve the same input conditions for correct analyzing of them, the both layout styles (DLS, RLS respectively) have the same process settings, as well as they keep the same gate area A, and an effective aspect ratio width to length $(W/L)_{\mathrm{eff}}$. In this work, the gate area of MOSFETs has been to 10 μm^2 and the effective the aspect $(W/L)_{\mathrm{eff}}$ varied from 0.5 to 2.0 with a step equal to 0.5. As the second objective is to verify the theoretical background by measurement on real silicon samples. For this kind of objective, the Cadence environment tool, Mentor Graphis software, and measurement equipment have been used. For this purpose, there have been fabricated 1 124 samples, which were proportionally divided into RLS MOSFETs and DLS MOSFETs with the angles equal to 120°, 100°, and 80°. More details about the theoretical and experimental results are summarized in sections 4.1.6 and (c) of Chapter 4: Results, Analyses, and Discussions.

3.2 Instruments

3.2.1 **Software**

(a) Symbolical and numerical calculations

The software for symbolical and numerical calculations used in this work are listed here below in alphabetical order.

- **Agros2D**

  Is an open-source code for numerical solutions of 2D coupled problems in technical disciplines. Its principal part is a user interface serving for complete preprocessing and postprocessing of the tasks (it contains sophisticated tools for building geometrical models and input of data, generators of meshes, tables of weak forms for the partial differential equations and tools for evaluating results and drawing graphs and maps) [151]. The processor is based on the library Hermes [152] containing the most advanced numerical algorithms [153 - 155] for monolithic and fully adaptive solution of systems of generally nonlinear and nonstationary partial differential equations (PDEs) based on hp-FEM (adaptive finite element method of higher order of accuracy). In the case of this thesis, it has been used as a verification tool which is able to numerically calculate physical fields such as electrostatic and electric currents.

- **MATLAB**

  MATLAB (an abbreviation of "MATrix LABoratory") is a multi-paradigm numerical computing environment and proprietary programming language developed by MathWorks. MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages. While other programming languages mostly work with numbers one at a time, MATLAB is designed to operate primarily on whole matrices and arrays. MATLAB combines a desktop environment tuned for iterative analysis and design processes with a programming language that expresses matrix and array mathematics directly [156]. In the case of this work, it has been used due to the Schwarz-Christoffel Toolbox [157], which is important for verifying the innovative symbolic expression.

- **Python program language**

  Is an open-source interpreted, high-level, general-purpose programming language created by Guido van Rossum and first released in 1991. Python's design philosophy emphasizes code readability with its notable use of significant whitespace. Its language constructs and object-oriented approach aim to help programmers write clear, logical code for small and large-scale projects [158]. In this thesis, the Python program language has been used for many reasons such as: 2D and 3D plotting of the mathematical analyses and measured data, to run parallel TCAD simulations, to control Agros2D tool, post-processing of simulated and measured data. In this work, hundreds of thousands and millions of simulations and measurement data have been generated during DLS MOSFET research and another program, such as Excel

from MS Office 365, has been able to process only tens of thousands of this data.

- **Wolfram Mathematica**

  Usually termed Mathematica is a modern technical computing system spanning most areas of technical computing — including neural networks, machine learning, image processing, geometry, data science, visualizations, and others. The system is used in many technical, scientific, engineering, mathematical, and computing fields. It was conceived by Stephen Wolfram and is developed by Wolfram Research of Champaign, Illinois. The first release has been on June 23, 1988. The Wolfram Language is the programming language used in Mathematica. In this thesis, it has been used for symbolic calculation of elliptic integrals in Schwarz-Christoffel transformation.

(b) Semiconductor Process and Device Simulation

- **TCAD from Silvaco**

  Silvaco Inc. develops and markets Electronic Design Automation (EDA) and Technology Computer Aided Design (TCAD) software and Semiconductor design IP (SIP). The company is headquartered in Santa Clara, California, and has a global presence with offices located in North America, Europe, and throughout Asia. Since its founding in 1984, Silvaco has grown to become a large privately held EDA company. The TCAD software from Silvaco Inc. [159], starting at the atomic and molecular level, simulates semiconductor device behavior without the need to run expensive and time-consuming experiments in manufacturing. The DLS MOSFET in this thesis has been simulated by the ATLAS device simulation software [160]. ATLAS is a modular and extensible framework for one, two- and three-dimensional

semiconductor device simulation. In this work, the DLS MOSFET has been simulated in three-dimensional setting. Before any semiconductor device structure is finalized for commercial production, it is important to understand device characteristics and performance. Technology Silvaco TCAD software provides an effective solution for simulating semiconductor device structure under steady-state and transient condition. Analysis of electrothermal parameters like electric field, leakage current, localized heating, and lattice temperature can aid in isolating structural vulnerability and understanding possible causes of device failure. For the above-mentioned characteristics of the software, the TCAD Silvaco has been chosen as the optimal device simulator.

(c) Transistor level simulation

- **Eldo platform from Mentor Graphics**

As the transistor level simulator, the Eldo platform from Mentor Graphics, has been used, because it is the industry proven, most advanced circuit verification platform for analog-centric circuits offering differentiated solution for reliability verification and comprehensive circuit analysis & diagnostics for analog, RF and mixed-signal circuits. It has been used for the simulation and verification of the measured data of the RLS MOSFET devices.

(d) Physical mask design

- **Virtuoso Layout Suite from Cadence**

The Virtuoso platform is the industry's most silicon-proven, comprehensive, custom IC design platform, trusted in taping out thousands of designs each year [161]. It supports custom analog, digital, and mixed-signal designs at the device, cell, block, and chip

levels. The enhanced Virtuoso Layout Suite offers accelerated performance and productivity from advanced full custom polygon editing (L) through more flexible schematic-driven and constraint-driven assisted full custom layout (XL), to full custom layout automation (GXL). Seamlessly integrated with the Virtuoso Schematic Editor and the Virtuoso Analog Design Environment, the Virtuoso Layout Suite enables the creation of differentiated custom silicon that is both fast and silicon accurate. In the case of this thesis, the (XL) version has been used. It allows to have connectivity between the corresponding schematic and layout view.

- **Calibre platform Mentor Graphics**

  The Calibre platform, delivers outstanding performance, accuracy and reliability for the world's most successful chipmakers and IC designers. It allows to check correctness of the layout in terms of requested connectivity and process fabrication rules [162]. These checks are called DRC (Design Rule Check) and LVS (Layout Versus Schematic). Both rules are essential for the successfully closed design and layout. For the upper mentioned reason, the Calibre platform has been used in this work.

(e) Post-processing and support programming

- **Office 365**

  Office 365 is a line of subscription services offered by Microsoft as part of the Microsoft Office product line. The brand encompasses plans that allow use of the Microsoft Office software suite over the life of the subscription, such MS Word, Skype, MS Excel and others. All Office 365 plans include automatic updates to their respective software at no

additional charge, as opposed to conventional licenses for these programs—where new versions require purchase of a new license [163]. In this work, the MS Excel and MS Word products have been used. The MS Excel is a spreadsheet with the features such as calculation, graphing tools, pivot tables, and a macro programming language called Visual Basic for Applications. It has been a very widely applied spreadsheet for these platforms, especially since version 5 in 1993. In the case of this thesis, it has been used for plotting simulated and measured data. For the post-processing of the simulated and measured data, it is better to use Python, which can cooperate with a huge volume of data.

- **SKILL program language**

  SKILL is a Lisp dialect used as a scripting language and PCell (parameterized cells) description language used in many EDA software suites by Cadence Design Systems. SKILL was known as IL. SKILL was a library of IL functions. The name was originally an initialism for Silicon Compiler Interface Language (SCIL), pronounced "SKIL", which then morphed into "SKILL", a plain English word that was easier for everyone to remember. In this work, it has been used to design the DLS MOSFET with the correct DRC result.

3.2.2 **Silicon Wafer**

Besides others, the measurement set-up depends also on the kind of the packaging of the device under test (DUT). In the case of this thesis, the measurements have been performed directly on the 200 mm silicon wafer Fig. 3.1a-e. The direct measurements and automized measurements of the devices

on the wafer in comparison with the measurement of the packed devices and manual measurements have, for example, the following benefits:

- It allows us to measure devices or chips on the specific locations of the wafer or it allows us to note locations where the measurements have been performed. Due to the process variability over each location on the wafer [164], the measurements on the different locations over the whole wafer is important. Based on that, we get more realistic results than it is in the opposite case, where the measurements are performed just on the small part of the wafer. Each wafer is divided into small parts (segments) called reticle fields (Fig. 3.1a). For the final qualification production step, it is also essential to measure the devices on more than one wafer.
- Reduction of the parasitic capacitance of the chip terminals areas connected to the measurement equipment. It is ensured by the possibility to use a smaller interface area between the measurement equipment and DUT. These special areas are named as probes points Fig. 3.1d. These probes points are much smaller in comparison with a chip pad. The reason, why the chip pads are bigger comes from the possibility to permanently bind them to the leads of chips by bond wires and to ensure high reliability of the connections [165].
- Reduction final cost, due to chip measuring before the packaging process step.
- Finally, the automatized measurement speed-up the production and verification line of the products, where each second of the measurement plays a key role. As one of the main tasks of the chip qualification engineers, who supervise the chip qualification to the massive production, is it to optimize the measurement set-up in terms of requested time for the measurement of the one device/chip.

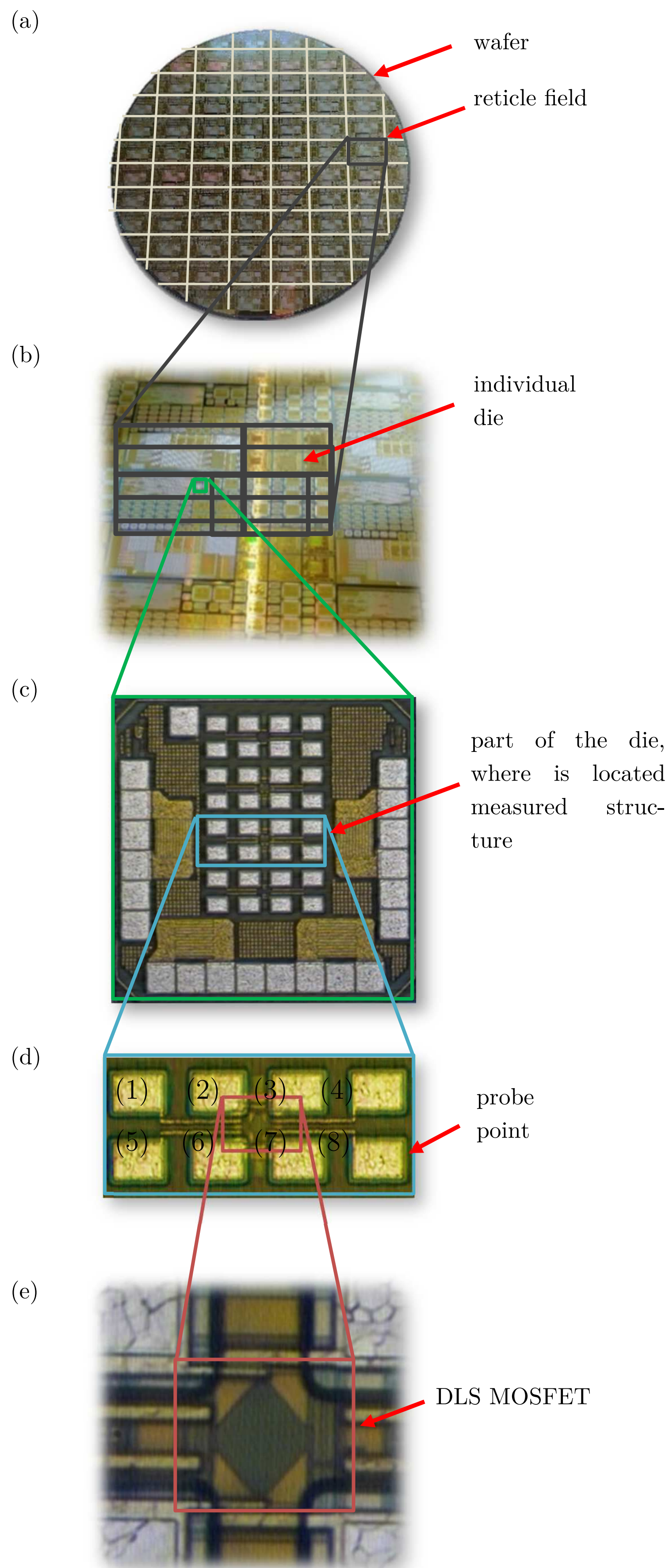


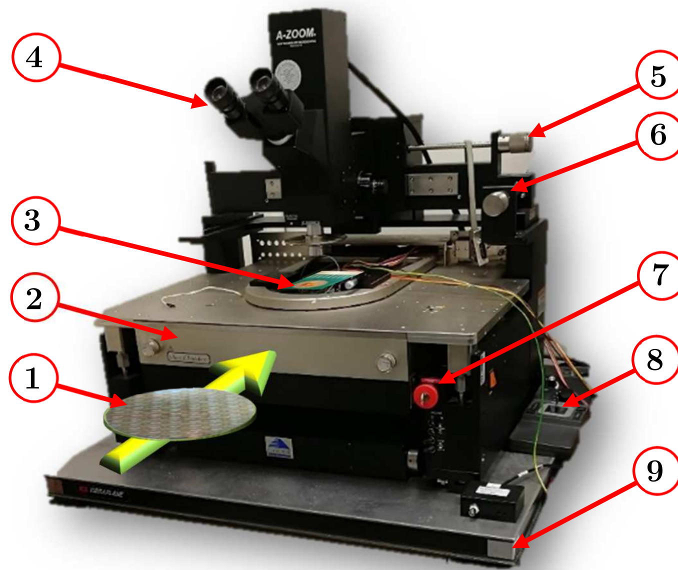
Fig. 3.1: Photos of the measured sample directly on the wafer.

3.2.3 **Laboratory Equipment**

To measure DLS MOSFETs on silicon wafer, the following laboratory equipment have been used.

(a) Advanced wafer probing machine (Cascade Microtech 1200)

The advanced wafer probing machine Cascade Microtech 1200 (depicted and described in Fig. 3.2) allows both, manual and automatized measurements of the silicon samples directly on the wafer, respectively. The manual method is more suitable for the measurement of a few samples. In the case of this thesis, there is possible to measure up to 1 124 samples. For this number of samples, the manual approach is unacceptable, and therefore in the presented thesis, the advanced wafer probing machine has been used such as the optimal measurement method.



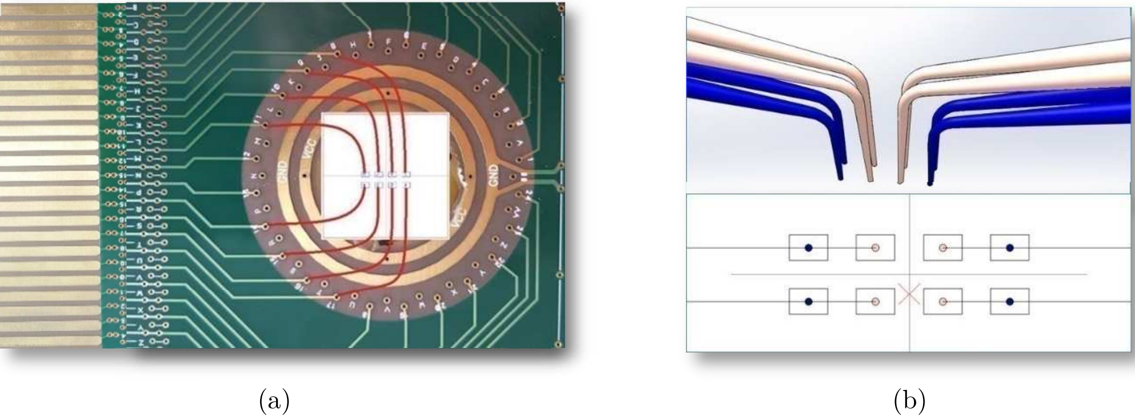
1. wafer with DLS MOSFETs
2. microchamber enclosure
3. advanced probe card
4. optical check, microscope
5. horizontal wafer shift
6. vertical wafer shift
7. emergency off button
8. electrical shift wafer controlled by a joystick
9. kinetic system Vibraplane table

Fig. 3.2: Advanced wafer probing machine.

Cascade Microtech offers a complete line of high-performance solutions for on-wafer probing, circuit boards and modules, vertical probe cards, MEMS, electro-optic devices, and more. Probe stations are available with accessories such as thermal control systems, special cables, calibration software, and industry-leading probes [166]. In the case of this thesis, there has been used also the thermal control system for thermal measurement. For the measurement, the horizontal probe card has been developed, which is described in the following section.

(b) Probe Card

The probe card for the measurement of the DLS MOSFETs (Fig. 3.3a) is a special connection interface that ensures precise connecting of the DUT and measurement equipment via the probe needles (Fig. 3.3b). It is also used for electrical testing of integrated circuits on a wafer during the wafer test process in manufacturing. The wafer test process is highly important and highly dependent on the reliability of probe cards. In the test process, the needles of the probe card contact the DUT chip electrodes to conduct electrical testing for the go/no-go test.



(a) (b)

Fig. 3.3: Probe card (a) and route planning of probe wires (b).

(c) Precision semiconductor parameter analyzer (Agilent 4156C)

The precision semiconductor parameter analyzer (Agilent 4156C) is a highly accurate laboratory benchtop solution for advanced device characterization. It is an electronic instrument for measuring and analyzing the characteristics of semiconductor devices. This one instrument allows us to perform both measurement and analysis of measurement results. Also, it allows us to store measurement data on a storage disk or store the data via LAN to a personal computer. Moreover, this instrument can be controlled by an external controller via GPIB by using remote control commands. This instrument also plots the measured data directly to its screen.

Fig. 3.4: Precision semiconductor parameter analyzer Agilent 4156C [161].

In the case of this thesis, the precision semiconductor parameter analyzer has been used for advanced device characterization. The measured and set I-V characterization data of the DLS MOSFETs have been read and set with high accuracy (Tab. 3.1 and Tab. 3.2) [167].

Tab. 3.1: Voltage Range, Resolution, and Accuracy (HRSMU = High Resolution Source Monitor Unit).

Voltage Range	Set Res.	Set Accuracy	Meas. Res.	Meas. Accuracy	Max. Current
± 2 V	100 μV	±(0.02 %+400 μV)	2 μV	±(0.01 %+200 μV)	100 mA
± 20 V	1 mV	±(0.02 %+3 mV)	20 μV	±(0.01 %+1 mV)	100 mA

Tab. 3.2: Current Range, Resolution, and Accuracy (HRSMU).

Current Range	Set Res.	Set Accuracy	Meas. Res.	Meas. Accuracy	Max. Volt
±100 nA	10 pA	±(0.12 %+40pA+ 100 fA×Vout)	100 fA	±(0.1 %+20pA+ 100 fA×Vout)	100 V
±1 μA	100 pA	±(0.12%+400pA+ 1pA×Vout)	1 pA	±(0.1 %+200pA+ 1 pA×Vout)	100 V
±10 μA	1 nA	±(0.07 %+4nA+ 10 pA×Vout)	10 pA	±(0.05 %+2nA+ 10 pA×Vout)	100 V
±100 μA	10 nA	±(0.07 %+40nA+ 100 pA×Vout)	100 pA	±(0.05 %+20nA+ 100 pA×Vout)	100 V
±1 mA	100 nA	±(0.06 %+400nA+ 1 nA×Vout)	1 nA	±(0.04 %+200nA+ 1 nA×Vout)	100 V

3.3 Analysis Setup

This section discusses how the numerical, simulation and measured data were processed and analyzed.

3.3.1 **Numerical Computation Setup**

The numerical calculations of DLS MOSFETs have been performed in MATLAB software in cooperation with the Schwarz-Christoffel plugin, which calls SC Toolbox. For the numerical calculations, in the MATLAB environment has been used 16 digits of precision. For higher precision, vpa function in Symbolic Math Toolbox™ is available. The vpa provides variable precision which can be increased without limit. By default, vpa uses 32 significant decimal digits of precision.

3.3.2 **Simulation Setup**

In this thesis, the 3D TCAD simulation tool from Silvaco company [159] has been used as the reference simulation tool. The advantages and features of the TCAD simulation tool form the Silvaco company have already been described in section 3.1.1(c). That simulation tool has been used to realize DLS structures, considering the same effective aspect ratio $(W/L)_{\mathrm{eff}}$ and same gate area A for any angle α. Angle α is an angle between metallurgical junctions of the drain/silicon-film regions, respectively source/silicon-film regions (Fig. 3.5a).

The DLS structures improve the electrical performances of MOSFETs in analog circuits. From the layout point of view, the DLS structures also have good matching parameters [168], which maintain the best performances of the analog circuits using DLS MOSFET devices. In general known, the device random mismatch is related to MOSFET gate area value [169, 170], and therefore the MOSFET gate area values are not set to the minimal value even for the latest planar technology nodes [171-173]. In the case of this work, it has been motivated by design in 28 nm, respectively 32 nm technology process where the MOSFETs of key analog circuits have the gate area over 20 μm^2.

In this thesis, the gate area of MOSFETs has been set to 10 μm². The $(W/L)_{\mathrm{eff}}$ values have been varied from 0.5 to 2.0 with a step equal to 0.5. Partially considered [174] a gate polysilicon thickness t_{Gate} has been set to 0.2 μm, a gate oxide thickness t_{ox} has been set to 8.5 nm, drain/source thicknesses $t_{\mathrm{N+}}$ have been set to 0.4 μm, and a silicon thickness t_{Si} has been set to 1.0 μm. Pwell and N^+ drain/source doping concentrations have been set to $1 \cdot 10^{16}$ cm^{-3} and $1 \cdot 10^{20}$ cm^{-3}, respectively (see Fig. 3.5). In Fig. 3.5, Drain, Source and Gate are terminals' names of MOSFET, L_{short} is a length of the transistor gate on the up/down sides, L_{long} is a length of the transistor gate in the middle of the transistor structure, and W' is a geometrical width of the DLS.

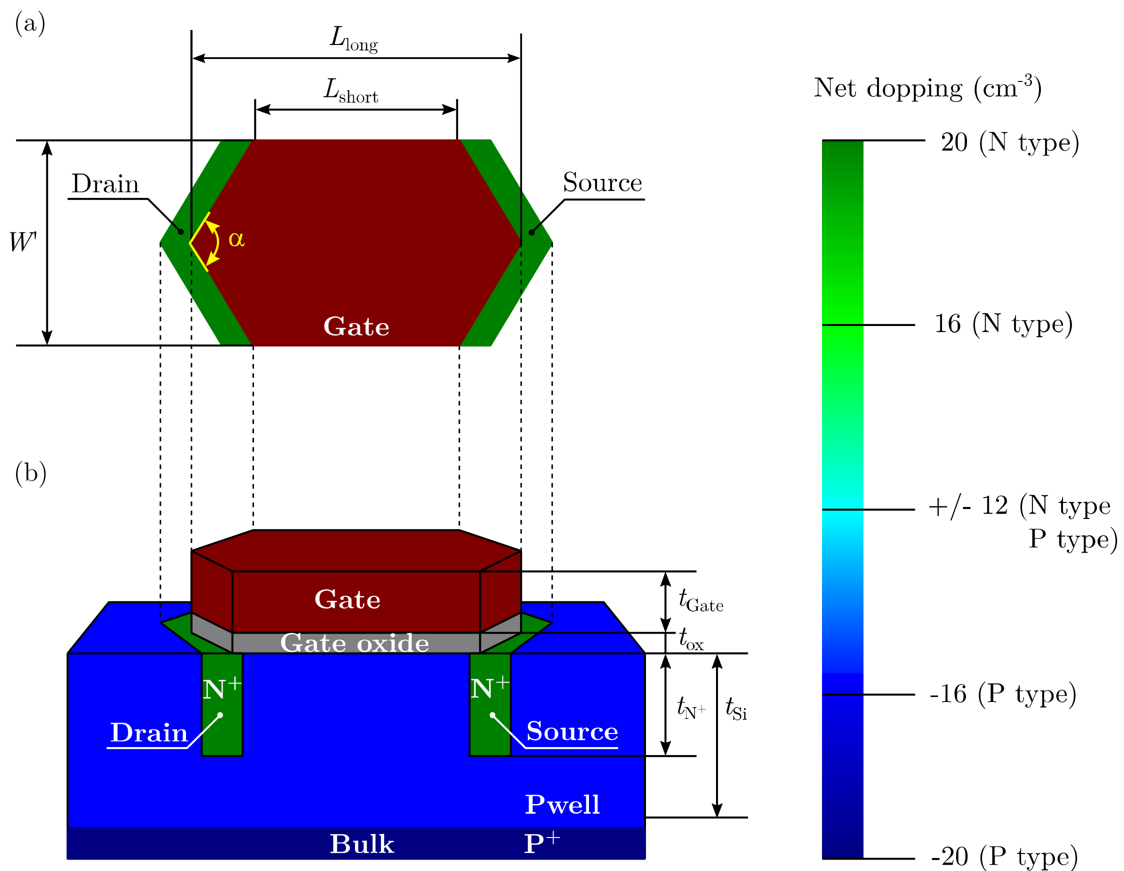


Fig. 3.5: Diamond Layout Style (DLS) of the general N channel MOSFET structure (a) 2D top-view of the structure, (b) 3D side-view of the structure.

The 3D numerical simulations were run with a lateral electric field-dependent model, a concentration-dependent mobility model, Selberherr impact ionization model and Shockley-Read-Hall model for a behavior of a generation-recombination process.

3.3.3 **Measurement Setup**

The measurement setup in this work uses the latest advanced measurement methodology. This methodology is graphically depicted in Fig. 3.6, and here below are listed the used parts of the presented methodology:

- samples with the adjustment for four-points measurement,
- fully automatized measurement system,
- air compressor for temperature forcing system,
- temperature forcing system,
- one or more probe cards,
- precision semiconductor parameter analyzer, and
- personal computer (PC) for data control and processing.

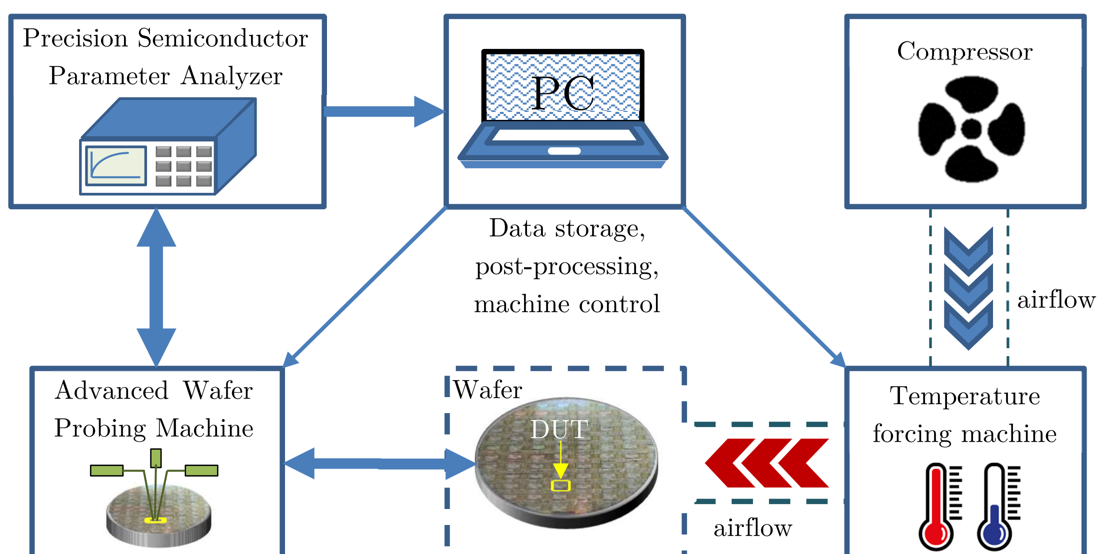


Fig. 3.6: Measurement setup – flow chart.

Each item of the measurement flow chart is described in more details in the following text:

- Samples with the adjustment for four-points measurement:

  The sample of this four-points measurement technique is depicted in Fig. 3.7. This technique ensures to measure the voltage delivered to the load independent of the voltage drop in the supply wires. In Fig. 3.7 there are the probe points connected to N-channel MOSFET as the follows order:

(1) Gate MOSFET terminal

(2) Drain force MOSFET terminal that power supplies the DUT

(3) Drain sense MOSFET terminal, also known as Kelvin sensing, is immediately adjacent to the target terminal and sense the exact drain voltage of the drain terminal without the drop voltage that is present in the case of the force drain terminal

(4) Nwell MOSFET terminal, in the case of this article, there is used triple well isolation [175]

(5) Substate of the chip

(6) Source force MOSFET terminal

(7) Source sense MOSFET terminal

(8) Bulk terminal of MOSFET

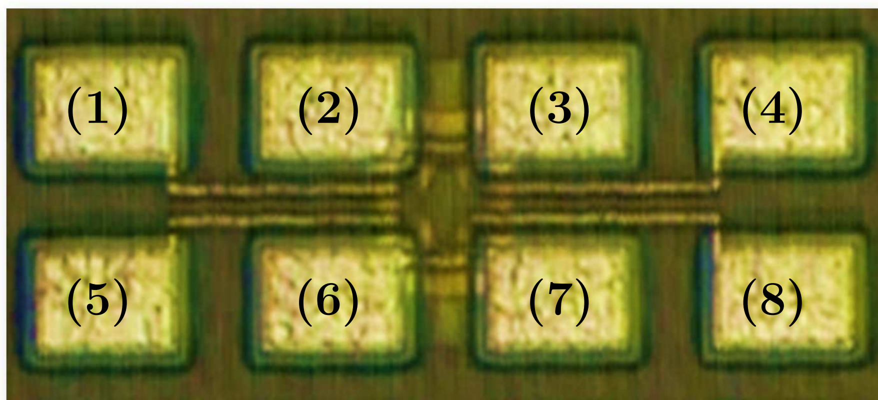


Fig. 3.7: Sample ready for for-point measurement.

- Air compressor:

  Air compressor together with the temperature forcing system is able to set different temperature conditions of the DUT. Components usually fall into one of the three temperature grades: commercial (0 to 70 °C), industrial (–40 to 85 °C), and military (–55 to 125 °C) [176]. In case of this thesis, it has been measured for the commercial grade. To be sure the measured results are correct in the specific range, the temperature ranges have been extended. The final temperature range has been set to (-25 to 75 °C).

- The advanced wafer probing machine, the precision semiconductor parameter analyzer, and the probe card have been describe in the previous section 3.2.3 Laboratory Equipment.

As the next part of the measurement flow chart, is also a minimum number measurement needed to obtain relevant results. For the minimum number measured samples, it is recommended to follow the central limit theorem. The central limit theorem states that if we have a population with mean μ and standard deviation σ and take sufficiently large random samples from the population with replacement, then the distribution of the sample means will be approximately normally distributed. This will hold true regardless of whether the source population is normal or skewed, provided the sample size is sufficiently large (usually $n > 30$) [177]. Sampling ''with replacement'' means that when a unit selected at random from the population, it is returned to the population (replaced), and then a second element is selected at random. In case of this thesis, the number of samples and measurement have been every time over 30.

Chapter 4

Results, Analyses, and Discussions

THIS chapter 4 details all the innovative results achieved in this doctoral thesis, such as innovative analytical descriptions of the effective aspect ratio of DLS MOSFET, improvements in the electrical performances of the DLS MOSFET by physical mask design, and the new precise model of the effective threshold voltage changes in the DLS MOSFETs. These results are discussed and presented in detail in the following three sub-section (4.1, 4.2, and 4.3). Furthermore, in this section are written theoretical analyses which are compared with the simulations and measurement results. In this thesis, the latest modern advanced measurement flow of integrated circuits directly on a wafer has been used to obtain high quality level of the measured data. This latest modern advanced measurement flow has been described in the previous Chapter 3: Research Design of the DLS MOSFET.

At the begging of the each sub-section (4.1, 4.2, and 4.3), there is noted, where the results have already been published. Also, an author's contribution is written for each published article.

4.1 Analytical Descriptions of the Effective Aspect Ratio of DLS MOSFETs

All parts of this chapter have been published by the author with major contribution in the following reference:

D. Barri, P. Vacula, V. Kotě, J. Jakovenko and J. Voves, "Improvements in the Electrical Performance of IC MOSFET Components Using Diamond Layout Style Versus Traditional Rectangular Layout Style Calculated by Conformal Mapping." ***IEEE Transactions on Electron Devices***, vol. 66, no. 9, pp. 3718-3725, September 2019. doi: 10.1109/TED.2019.2931090. **(Quartile 1)**
Co-authorship: 70 %

4.1.1 Introduction

The DLS MOSFET is a special layout shape of MOSFETs due to its an irregular shape of the polysilicon gate. It is not a typical structure, such as a conventional rectangular layout shape, and due to its irregular shape, it has an inhomogeneous electric field in the active channel area of the MOSFET devices. To have possibility to use the DLS MOSFETs in integrated circuits, that inhomogeneous of the electric field should be precisely solved.

In this thesis, an innovative analytical expression of the DLS MOSFET is presented. This presented analytical expression is based on a conformal mapping and it is compared to an already one existing approach based on the "Longitudinal Corner Effect" (LCE). The LCE approach describes the DLS MOSFET only with the first-order approximation, and it is understood as a limitation in high-end integrated circuits, where the high level of precision is required. Therefore, there is a need to express the DLS MOSFET more precisely, such it is in this thesis. In the end of this section, the both methodologies are compared.

This section is organized as follows. Section 4.1.2 introduces the innovative analytical expression of DLS MOS transistor based on the Schwarz-Christoffel (SC) mapping theorem. In this section, there is presented the SC transformation and

using the SC transformation to get the novel analytical solution for calculation of the DLS MOS transistor. Section 4.1.3 describes steps how to use SC Toolbox in the MATLAB software to get SC numerical data. Section 4.1.4 introduces the first order approximation for the calculation of DLS MOSFETs based on the LCE and PAMDLE effects. Section 4.1.5 discusses and compares the novel presented analytical expression with the LCE+PAMDLE (LPEs) expression. The last section 4.1.6 summarizes achieved results and highlights the precision of the innovative model for calculation of the effective aspect ratio of the DLS MOSFETs based on the SC transformation.

4.1.2 **The Innovative Analytical Description of the DLS MOSFET Based on the Schwarz-Christoffel Transformation**

The presented innovative analytical expression of the DLS MOSFET is based on the conformal transformation. In mathematics, a conformal map is a function that preserves angles locally [178]. From an electric point of view, it is essential transformation for the correct transformation of electrical objects because it keeps the same local angles between equipotential lines and current flowlines inside of objects before and after geometric transformation. It is well shown in Fig. 4.1, where equipotential lines (pink colored lines) are everywhere perpendicular to current flowlines (green colored lines) for the object before transformation (Fig. 4.1a) as

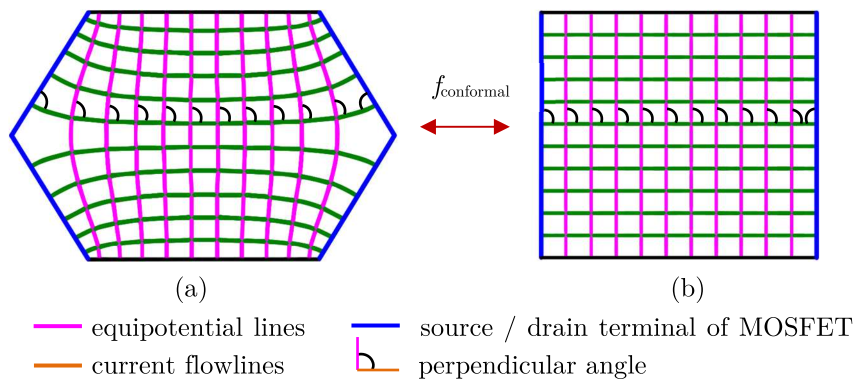


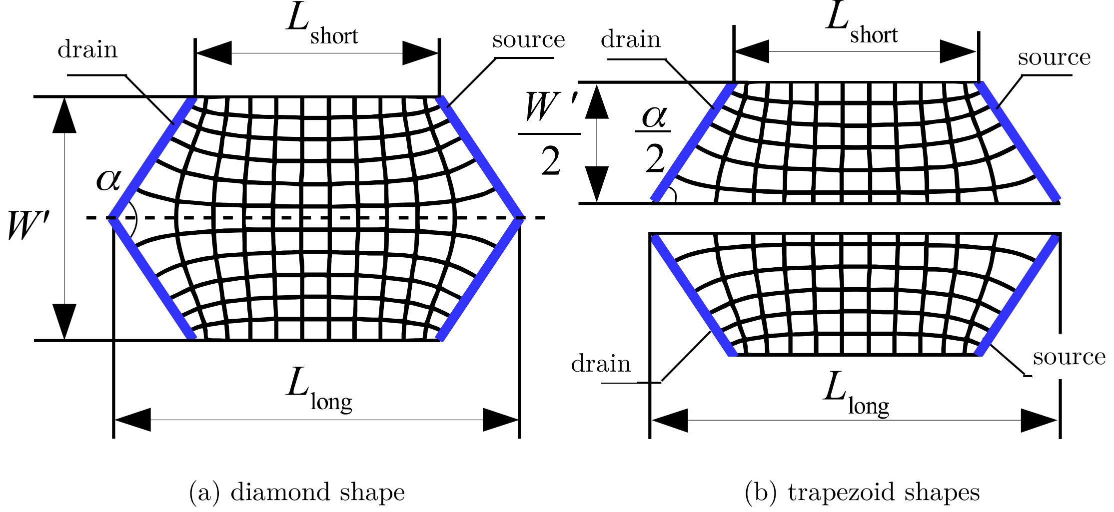
Fig. 4.1: An example of conformal mapping.

well as for the object after transformation (Fig. 4.1b). This is the reason why this transformation has been decided as the correct one.

The conformal transformation allows the analytical transformation of an arbitrary polygon onto an equivalent rectangular shape, where the internal electrostatic conditions are solved and maintained [179, 180]. Such an arbitrary polygon can be triangular shapes [181], pentagon shapes [182], quadrilateral shapes (such as the trapezoidal shape used to describe DLS in this work) and others polygonal shapes [183].

In this thesis, the Schwarz–Christoffel (SC) transformation has been used such as a conformal function. Elwin Bruno Christoffel (1829-1900) and Hermann Amandus Schwarz (1843-1921) independently discovered the Schwarz–Christoffel mapping in 1867 and 1869 respectively, which provides a conformal mapping as it is for example depicted in Fig. 4.1 by conformal function $f_{\text{conformal}}$. Moreover, that conformal function returns an analytic result and therefore it has a high level of precision in electrical performances of MOSFET [183]. Besides the Schwarz–Christoffel mapping, there also exist other numerical methods for conformal mappings describes in [184].

Generally, as it is shown in Fig. 4.2, the DLS is a symmetrical structure where L_{short} is a length of the transistor gate on the up/down sides, L_{long} is a length of the transistor gate in the middle of the transistor structure, W is a geometrical width of the DLS, and α is an angle between metallurgical junctions. The Source and Drain terminals of the MOS transistor are highlighted by blue bold lines on the sides of the diamond/trapezoid structures. As the symmetrical line of this structure is a dashed line shown in Fig. 4.2a that allows split diamond layout style into two trapezoidal shapes. Because of the symmetry, only one part of the DLS structure is sufficient to solve [185], as it is in this paper. Since the symmetry boundary has the Neumann boundary condition with current density equal to zero, the final



(a) diamond shape (b) trapezoid shapes

Fig. 4.2: A DLS structure (a) split into two trapezoidal layout shapes (b).

aspect ratio of the equivalent rectangle has the same length and doubled width. In the case, where the reflection boundary is the Dirichlet boundary condition, the final equivalent rectangle will have the length doubled, and the width will be the same [185].

The non-rectangular gate shape has a significant impact on the final MOS effective aspect ratio $(W/L)_{\text{eff}}$ and thus on the performance of the DLS MOS transistor. The effective aspect ratio $(W/L)_{\text{eff}}$ plays a key role for drain-source current calculation (I_{DS}) of the DLS MOS transistor. In the case of an N-channel DLS MOSFET, the I_{DS} is defined for a linear region by (4.1) and in a saturation region by (4.2) [186].

$$I_{\text{DS}} = \mu_{\text{N}} C_{\text{ox}} \left(\frac{W}{L}\right)_{\text{eff}} \left(V_{\text{GS}} - V_{\text{th}} - \frac{V_{\text{DS}}}{2}\right) V_{\text{DS}} \tag{4.1}$$

$$I_{\text{DS}} = \frac{1}{2} \mu_{\text{N}} C_{\text{ox}} \left(\frac{W}{L}\right)_{\text{eff}} (V_{\text{GS}} - V_{\text{th}})^2 (1 + \lambda V_{\text{DS}}) \tag{4.2}$$

where μ_{N} is an electron mobility, C_{ox} is an oxide capacitance, W is an effective width of MOS transistors, L is an effective length of MOS transistors, V_{GS} is a gate-source voltage of MOS transistors, V_{DS} is a drain-source voltage of MOS transistors, V_{th} is a threshold voltage of MOS transistors and λ is a channel length modulation factor.

Considering the previous symmetry theory, the equivalent effective aspect ratio of the trapezoidal structure should be multiplied by a factor of two to obtain the correct equivalent effective aspect ratio for the symmetric DLS structures. Moreover, this approach makes at least 2 times faster simulation and therefore, in this thesis, the DLS analytic solution is based on SC mapping of trapezoidal shape to a rectangular shape instead of the direct SC mapping of diamond to a rectangular shape.

The Schwarz-Christoffel mapping theorem is defined as a transformation that maps the upper-half plane z (Fig. 4.3(b)) to an arbitrary polygon in w-plane (Fig. 4.3(a),(c)) [185]. In connection with the previous and for the case if this thesis, the SC function maps the upper-half of the z-plane onto the trapezoid in the w_1-plane by the mapping $w_1=\phi_1(z)$,

$$w_1 = \phi_1(z) = \int_0^z (1-x^2)^{\alpha_n - 0.5}(1-k^2x^2)^{-\alpha_n - 0.5}dx \tag{4.3}$$

and also, the SC function maps upper-half of the z-plane onto the rectangle in the w_2-plane by the mapping $w_2=\phi_2(z)$

$$w_2 = \phi_2(z) = \int_0^z (1-x^2)^{-0.5}(1-k^2x^2)^{-0.5}dx \tag{4.4}$$

where ϕ_1, and ϕ_2 are SC mapping functions, α_n is a normalized angle by the expression $\alpha_n = (90° - \alpha/2)/360°$ and it is indicated in degrees. Parameter k provides a relationship between the parameters that describe the trapezoidal shape and those that describe the rectangular shape.

Then mapping of the trapezoid to the rectangle is given by $w_2 = \phi_1(\phi_2^{-1}(w_1))$. After routine manipulations [187] we have got the equivalent relationship between width and length of a trapezoid. It is signed as an effective aspect ratio $(W/L)_{\text{eff,SCT,ana,trapezoid}}$ expressed by the following expression (4.5):

$$\left(\frac{W}{L}\right)_{\text{eff,trapezoid}}^{\text{SCT,ana}} = f\left(\alpha, \frac{W'}{L_{\text{short}}}\right) \tag{4.5}$$

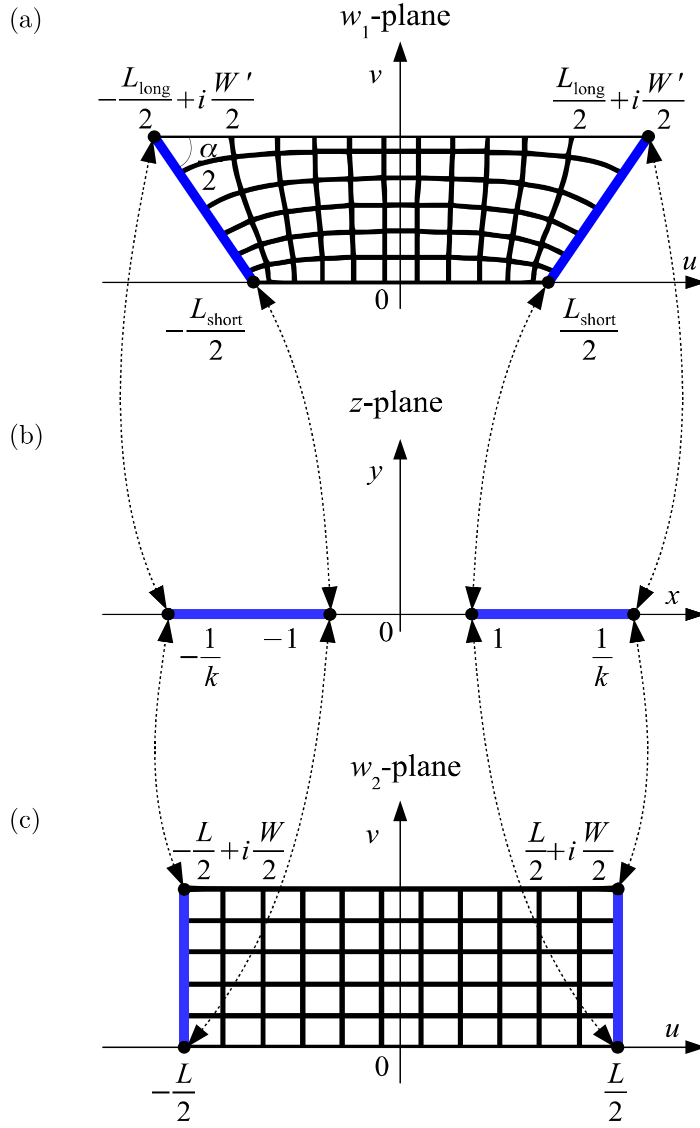


Fig. 4.3: Schwarz-Christoffel mapping of a trapezoid (a) onto a rectangle (c) by mapping through upper-half of the z-plane (b).

An analytical approximation of the relationship indicated in (4.5) is shown in the following expression (4.6)

$$\left(\frac{W}{L}\right)_{\text{eff,trapezoid}}^{\text{SCT,ana}} = \\ = \frac{1}{\frac{2L_{\text{short}}}{W'} - 7.10^{-5}\left(90-\frac{\alpha}{2}\right)^{2} + 1.57.10^{-2}\left(90-\frac{\alpha}{2}\right) - 2.10^{-3}} \tag{4.6}$$

where α is in degrees and is accurate to within one percent provided $2L_{short}/W' > 1.4$. A L_{short} is a shorter parallel side of the trapezoid, and a W' is a geometrical width of the trapezoid

Considering non-parallel lines of trapezoid as a source and a drain of MOS transistors, the final analytical effective aspect ratio $(W/L)_{eff}$ expression of the diamond layout shape MOSFET is defined as twice (4.6) by the following expression (4.7):

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,ana}} = \\ = \frac{2}{\frac{2L_{\text{short}}}{W'} - 7.10^{-5}\left(90 - \frac{\alpha}{2}\right)^2 + 1.57.10^{-2}\left(90 - \frac{\alpha}{2}\right) - 2.10^{-3}} \tag{4.7}$$

To verify the novel analytical expression of the DLS MOSFET (4.7), the MATLAB SC Toolbox has been used. Further details about this method are briefly described in the following section.

4.1.3 The Verification Methodology of the Innovative Expression using MATLAB SC Toolbox

The Schwarz-Christoffel SC Toolbox is a plugin for MATLAB software that was created by Tobin A. Driscoll. It uses a following conformal function $f(z)$ (4.8) for a conformal map from the complex half-plane (the canonical domain, z-plane in Fig. 4.4) to the interior of a polygon (the physical domain, w-plane in Fig. 4.4):

$$w_k = f(z) = A + C \int_{z_0}^{z} \prod_{k=1}^{n-1} (\zeta - z_k)^{\beta_k \pi - 1} d\zeta \tag{4.8}$$

where the vertices of the polygon are denoted as $w_1, w_2, \ldots, w_n$ and $\beta_1\pi, \beta_2\pi, \ldots, \beta_n\pi$ are the interior angles at these vertices. The A and C are unknown

complex constants that need to be determined. Different choices of the constants A and C rotate, scale and/or translate the target polygon [188]. Index n is the number of vertices. It is convenient to suppose that $f(\infty) = w_n$. Coordinates $z = x + jy$ and $w = u + jv$ denote complex numbers in the z-plane and w-plane, respectively.

The MATLAB SC toolbox provides a numerical calculation method with both graphical user interface and command line functions to perform mapping numerically. SC toolbox provides a lot of SC map constructors and one of them is calling rectmap. The rectmap directly maps a polygon to a rectangle.

For the calculation of DLS MOS transistor, the numerical MATLAB calculation of the SC transformation has been used as well. An important outcome of this process is the modulus. It returns the effective aspect ratio $(W/L)_{\text{eff}}$ that will be compared to the other approaches in this thesis.

In the case of this thesis, the conformal mapping theorem for mapping diamond layout shapes to rectangular layout shapes (Fig. 4.2) where the both objects have the same effective aspect ratio and after routine numeric operations also the same surface area has been used. It is a very important point in terms of comparison of MOSFET performances with different layout shapes.

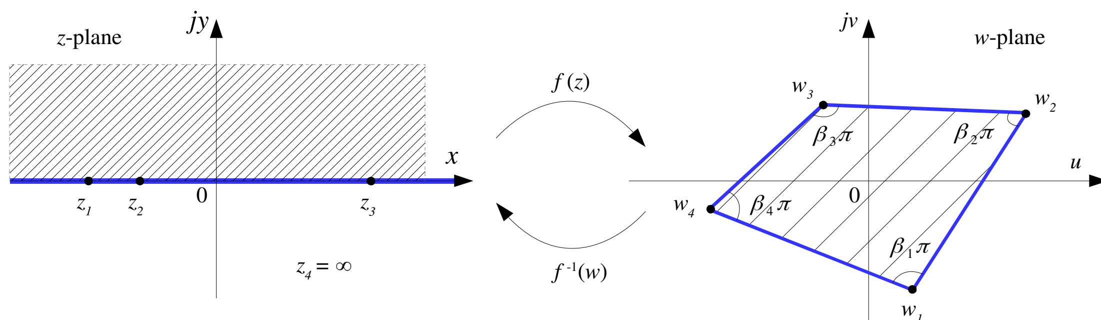


Fig. 4.4: SC mapping theorem from half z-plane onto a polygon in w-plane

4.1.4 **The Analytical Description of the DLS MOSFET Based on the LCE and PAMDLE**

In previous sections, two ways to calculate the effective aspect ratio $(W/L)_{\mathrm{eff}}$ have been described. The first one is based on the analytic expression of DLS by using Schwarz-Christoffel mapping and that effective aspect ratio is calling as $(W/L)_{\mathrm{eff,SCT,ana}}$. The second approach is a numerical calculation of DLS by applying using the SC Toolbox in MATLAB software and then that effective aspect ratio is calling as $(W/L)_{\mathrm{eff,SCT,num}}$. The next approach that describes DLS is presented in the following parts of this section. This method is based on the longitudinal corner effect and it will be in the next section compared with the formerly described Schwarz-Christoffel mapping methods.

Description of the Diamond Layout Shape based on the LCE (Longitudinal Corner Effect) and PAMDLE (Parallel Association of MOSFET with Different Channel Lengths Effect) has been recently published in [127] and [128]. In these publications, the DLS MOS transistor description is based on two effects. The first effect is "corner effect" along the channel longitudinal (parallel) direction named "Longitudinal Corner Effect" (LCE) [127]. In considering LCE the gate hexagonal geometry can be composed by two trapezoidal geometries. The second effect is PAMDLE effect [128] that reduces the effective channel length L_{eff} of Diamond MOSFET in comparison of the rectangular MOSFET counterpart, in the first order approximation, by the average channel length of the trapezoidal regions, as it is indicated in equation (4.9)

$$L_{\mathrm{eff}} = \frac{L_{\mathrm{short}} + L_{\mathrm{long}}}{2} \tag{4.9}$$

where L_{short} is a length of the transistor gate on the up/down sides (see Fig. 4.2), L_{long} is a length of the transistor gate in the middle of the transistor structure.

So, taking into account (4.9) the aspect ratio of the DLS described based on the LCE and PAMDLE is (4.10) for angle α in range from 0° to 90° and (4.11) for angle α in range from 90° to 180°, respectively. That effectives aspect ratio is calling as $(W/L)_{\text{eff,LPEs}}$

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LPEs}} = 2\left(\frac{W'}{L_{\text{short}} + L_{\text{long}}}\right)\sqrt{2(1+\cos\alpha)}; \quad \alpha = 0^{\circ} - 90^{\circ} \tag{4.10}$$

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LPEs}} = 2\left(\frac{W'}{L_{\text{short}} + L_{\text{long}}}\right)\sqrt{2+\cos\alpha}\,; \quad \alpha = 90^{\circ} - 180^{\circ} \tag{4.11}$$

where W' is a geometrical width of the DLS MOSFET (see Fig. 4.2).

4.1.5 **Results, Discussion and Comparison**

The effective aspect ratios $(W/L)_{\text{eff,LPEs}}$ and $(W/L)_{\text{eff,SCT,ana}}$, respectively have been compared to the aspect ratio calculated by MATLAB SC toolbox $(W/L)_{\text{eff,SCT,num}}$, by the following expressions (4.12) and (4.13), respectively.

$$\epsilon\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LPEs}} = \left(\frac{\left(\frac{W}{L}\right)_{\text{eff}}^{\text{LPEs}} - \left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,num}}}{\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,num}}}\right).100 \tag{4.12}$$

$$\epsilon\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,ana}} = \left(\frac{\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,ana}} - \left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,num}}}{\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,num}}}\right).100 \tag{4.13}$$

The sample data for the case where the effective aspect ratio $(W/L)_{\text{eff,SCT,num}}$ is equal to 1.0 is shown in the Tab. 4.1. The complete results of this analysis are depicted on Fig. 4.5 in condition where the gate area A of DLS is fixed to 10 µm², an angle α is set from 180° (conventional rectangular shape) down to 30°, and the effective aspect ratio $(W/L)_{\text{eff,SCT,num}}$ is set from 0.5 to 2.0.

By analyzing Fig. 4.5, we can see that an error of the effective aspect ratio $\epsilon(W/L)_{\text{eff,LPEs}}$ is increasing if the angle α of the DLS is decreasing. It is valid until a specific α-point is reached. After that, it changes a trend and the error of the effective aspect ratio $\epsilon(W/L)_{\text{eff,LPEs}}$ is decreasing. The position of the specific α-point depends on geometry setting of DLS MOS transistor, i.e. effective aspect ratio. If the effective aspect ratio $(W/L)_{\text{eff,SCT,num}}$ is decreasing then the position of the specific α-point is increasing. The maximal error values of the aspect ratio

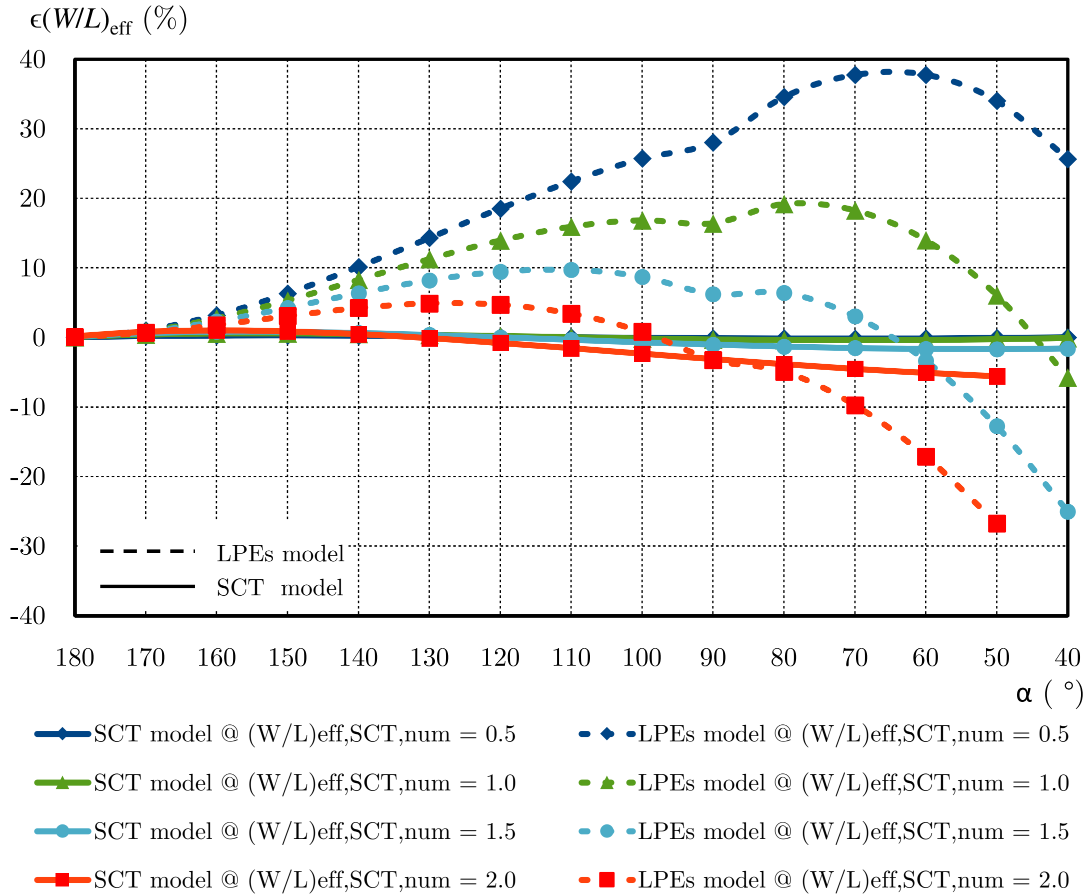


Fig. 4.5: Calculated error of effective aspect ratio $(W/L)_{\text{eff}}$ depending on angle α between SCT model (solid line) and LPEs (LCE+PAMDLE) model (dashed line) respectively and numerically simulated aspect ratio (MATLAB simulation).

calculated by LCE+PAMDLE are in the range from -27 % to +38 %. In counterpart with the new SC analytical description of DLS MOS transistor, the maximal error values are in the range from 0 % to -5.5 %. The new SC approach is much more precise than LCE+PAMDLE approach and moreover, the maximal error of the effective aspect ratio values $\epsilon(W/L)_{\mathrm{eff,SCT,ana}}$ are linearly increasing if the angle α is decreasing. It is an important knowledge because we can easily predict where the maximal deviation error happens and also its maximal value.

Tab. 4.1: Analysis of effective aspect ratio $(W/L)_{\mathrm{eff}}$ for both LPEs and SCT cases of the DLS with various angles α

α (°)	$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{SCT,num}}$ (-)	A (μm²)	W (μm)	L_{short} (μm)	L_{long} (μm)	$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{LPEs}}$ (-)	$\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{SCT,ana}}$ (-)	$\epsilon\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{LPEs}}$ (%)	$\epsilon\left(\frac{W}{L}\right)_{\mathrm{eff}}^{\mathrm{SCT,ana}}$ (%)
180	1.0	10	3.162	3.162	3.162	2.0009	2.0020	0.05	0.10
170	1.0	10	3.159	3.027	3.304	2.0187	2.0086	0.94	0.43
160	1.0	10	3.149	2.898	3.453	2.0555	2.0116	2.77	0.58
150	1.0	10	3.132	2.773	3.612	2.1067	2.0119	5.33	0.60
140	1.0	10	3.109	2.651	3.783	2.1659	2.0104	8.30	0.52
130	1.0	10	3.077	2.532	3.967	2.2260	2.0076	11.30	0.38
120	1.0	10	3.038	2.415	4.169	2.2794	2.0043	13.97	0.21
110	1.0	10	2.990	2.298	4.392	2.3189	2.0008	15.94	0.04
100	1.0	10	2.931	2.182	4.641	2.3374	1.9975	16.87	-0.12
90	1.0	10	2.862	2.064	4.925	2.3284	1.9948	16.42	-0.26
80	1.0	10	2.778	1.944	5.255	2.3843	1.9929	19.21	-0.35
70	1.0	10	2.679	1.819	5.646	2.3657	1.9923	18.29	-0.39
60	1.0	10	2.560	1.689	6.123	2.2800	1.9928	14.00	-0.36
50	1.0	10	2.416	1.549	6.730	2.1217	1.9950	6.09	-0.25
40	1.0	10	2.238	1.395	7.543	1.8852	1.9989	-5.74	-0.06
30	1.0	10	2.011	1.220	8.725	1.5639	2.0045	-21.81	0.22

4.1.6 **Summary**

This section presents and compares the new innovative methodology for calculation effective aspect ratio of a diamond layout shape MOS transistor based on the Schwarz-Christoffel transformation with the already existing approach based on the Longitudinal Corner Effect. The result of this part is an analytical expression describing the effective aspect ratio of the DLS MOS transistor. It was observed and proved, by numerical calculation in MATLAB software, that the new presented approach of effective aspect ratio calculation reaches much better results. The maximal deviation values of the effective aspect ratio calculated by LCE+PAMDLE are in the range from -27 % to +38 %. In counterpart with the new SC analytical description of DLS MOSFET the maximal deviation values are in the range from 0 % to -5.5 %, and moreover the maximal effective aspect ratio deviation values are linearly increasing if the angle α of DLS MOS is decreasing. It is an important knowledge because we can easily predict where the maximal deviation happens and the maximal value of it. It was calculated for aspect ratio lower than 2.0. Such the next benefit of the new model is continuous character over all angles. In the LCE+PAMDLE approach, and in the case where angle α is equal to 90°, there is a non-continuous point (Fig. 4.5). It happened due to needing two different expressions to describe the effective aspect ratio for DLS MOSFETs. In the new presented approach, there is just one expression, which fully describes the effective aspect ratio of the DLS MOSFETs for all angles.

4.2 Improvements in the Electrical Performances of the DLS MOSFET by Physical Mask Design

All parts of this chapter have been published by the author with major contribution in the following references:

D. Barri, P. Vacula, V. Kotě, J. Jakovenko and J. Voves, "Improvements in the Electrical Performance of IC MOSFET Components Using Diamond Layout Style Versus Traditional Rectangular Layout Style Calculated by Conformal Mapping." ***IEEE Transactions on Electron Devices***, vol. 66, no. 9, pp. 3718-3725, September 2019. doi: 10.1109/TED.2019.2931090. **(Quartile 1)**
Co-authorship: 70 %

D. Barri, P. Vacula, T. Grešl, P. Švancara, V. Kotě, J. Jakovenko and J. Voves, "MOSFETs' Electrical Performance in the 160-nm BCD Technology Process with the Diamond Layout Shape." ***IEEE Transactions on Electron Devices***, vol. 67, no. 8, pp. 3270-3777, August 2020. doi: 10.1109/TED.2020.3000744. **(Quartile 1)**
Co-authorship: 61 %

D. Barri, and J. Jakovenko, "Comparison of Measured Data Given by Automatized Measurement Methodology with the Analytical Expression of DLS MOSFET." *in IEEE Proceedings of the 25th International Conference on Applied Electronics (AE) 2020*, Pilsen, Czech Republic, 8 September 2020. pp. 3-8. ISBN 978-80-261-0891-7. doi: 10.23919/AE.2019.8866997.
Co-authorship: 90 %

4.2.1 Introduction

In the previous section, the latest analytical calculation method of the effective aspect ratio $(W/L)_{\text{eff}}$ of DLS MOSFET has been described. The effective aspect ratio $(W/L)_{\text{eff}}$ has a significant role for drain-source I_{DS} current calculation of MOSFET in a linear region (4.1), and in a saturation region (4.2), respectively.

Generally, among the crucial electrical parameters of MOS transistors also belongs a drain-source current I_{DS}. Therefore, in this thesis, the impact of DLS MOS transistors on the I_{DS} performance has also been analyzed.

The latest analytical expression of the effective aspect ratio of the DLS MOS transistors (4.7) is used in the following part 4.2.2 to calculate the theoretical drain-source current enhancement. In subsection 4.2.5 of this part, the given theoretical drain-source current enhancement is compared with the 3D TCAD simulations results and measurement results.

4.2.2 Theoretical Drain Current Enhancement Given by Schwarz-Christoffel Transformation of the DLS

The theoretical drain-source current enhancement $\delta I_{\mathrm{DS,SCT}}$ of the DLS MOSFETs is calculated as the ratio of DLS MOSFET drain current with an arbitrary set angle to the drain current of the conventional rectangular layout shape of the MOS transistor with the following expression

$$\delta I_{\mathrm{DS,SCT}} = \left(\frac{I_{\mathrm{DS,SCT,DLS}} - I_{\mathrm{DS,SCT,RLS}}}{I_{\mathrm{DS,SCT,RLS}}} \right) \cdot 100 \tag{4.14}$$

where $I_{\mathrm{DS,SCT,DLS}}$ is a calculated drain-source current of the DLS MOS transistor, and $I_{\mathrm{DS,SCT,RLS}}$ is a calculated drain-source current of the RLS MOS transistor.

The flowchart depicted in Fig. 4.6 clearly describes the methodology to calculate the theoretical drain-source current enhancement. In the first step, there is necessary to create a list of compared structures. In our case, the list has at least two items. One of them is RLS MOSFET, which is taken as a reference MOS transistor, and the second is a DLS MOSFET with the arbitrarily required set angle. After then, the list of studied structures is created, the next step is a decision if all items in the list have already proceeded the following step. The action list of the following step is:

- Create a studied structure (for example RLS or DLS MOS transistor).
- Calculate the effective aspect ratio of the created structure by the new analytical expression (4.7) based on the Schwarz-Christoffel transformation, and save as $(W/L)_{\mathrm{eff}}$.

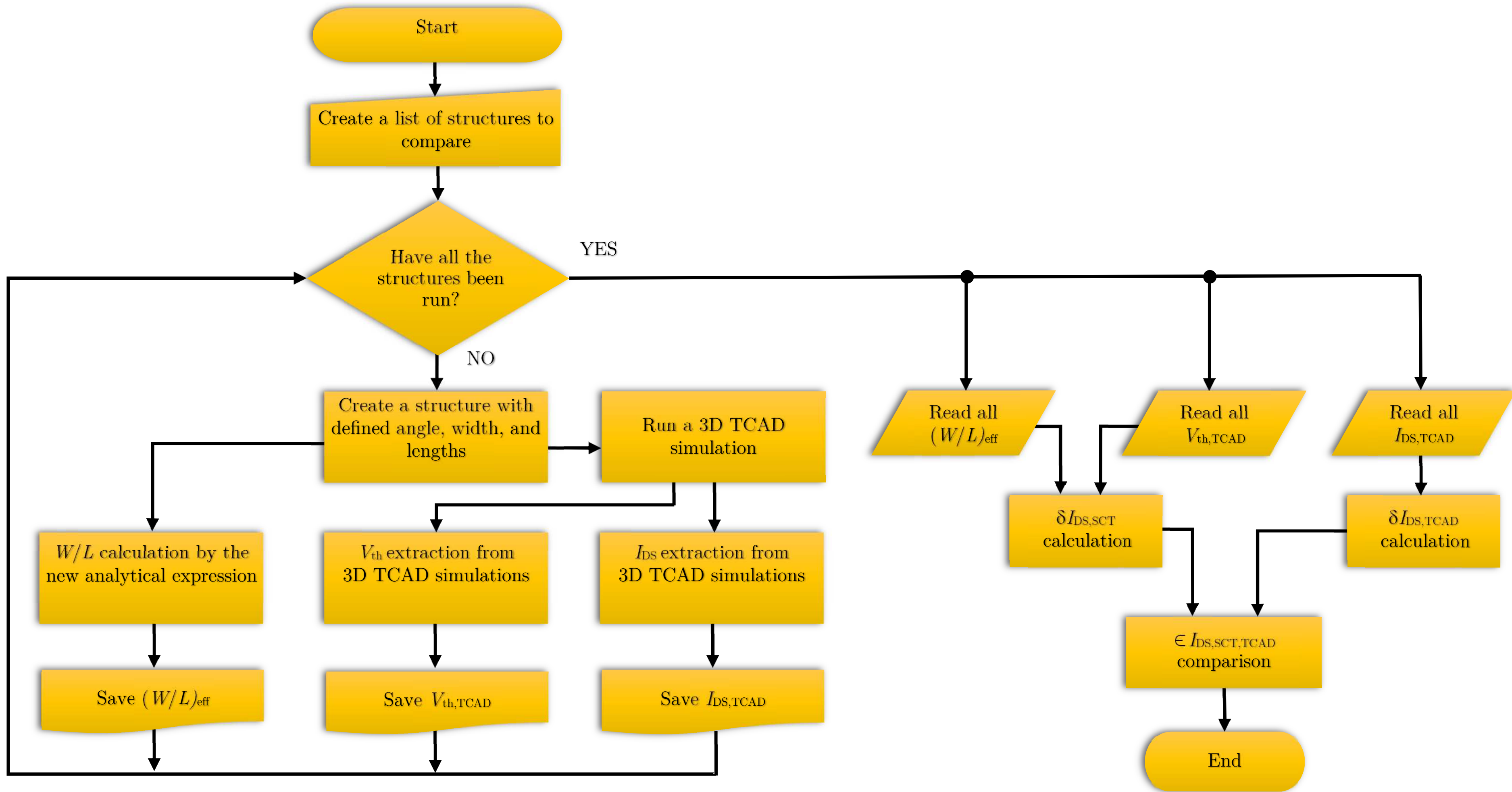


Fig. 4.6: The flowchart calculation of the theoretical drain current gain given by Schwarz-Christoffel transformation.

- Run 3D TCAD simulation in Silvaco DeckBuild tool.
- The output of the 3D TCAD simulation are two values. The first one is a threshold voltage and the second is a drain-source current of the studied structure. The given values are saved such as $V_{th,TCAD}$, and $I_{DS,TCAD}$, respectively.

When all the studied structures have finished the upper steps, the next step reads the stored values such as calculated effective aspect ratio $(W/L)_{eff}$, and its extracted the threshold voltages $V_{th,TCAD}$ and drain-source currents $I_{DS,TCAD}$ from 3D TCAD simulations. After the data reading, it follows:

- The drain-source current enumeration is calculated for each studied structure (i.e. 1x RLS, and 1x or more DLS MOS transistor). For the drain-source current calculation has been used the expression for saturation region (4.2).
- After the routine manipulation, the drain-source current enhancement enumeration is calculated, with the expression (4.14) for the calculated data $\delta I_{DS,SCT}$.

The results of the this part are described in the section 4.2.5 "Results, Discussion and Comparison" together with the simulated TCAD results and measured results on silicon samples.

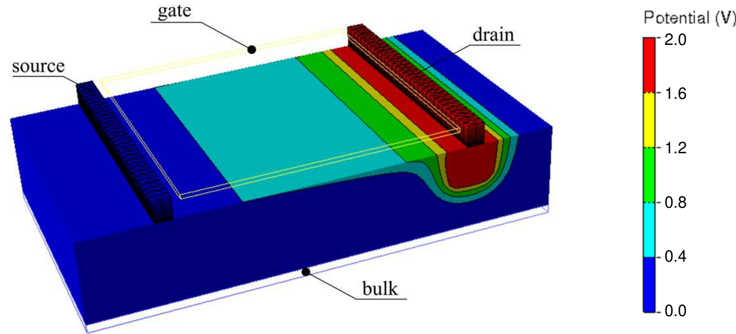
4.2.3 **3D TCAD Simulations of the Drain-Source Current Enhancement**

In order to analyze an impact of an angle α of the DLS MOS transistor on the drain-source current saturation I_{DS}, the 3D TCAD Silvaco simulation tool was used. Detailed description of the simulated structures is described in section 3.3.2 "Simulation Setup" of this thesis.

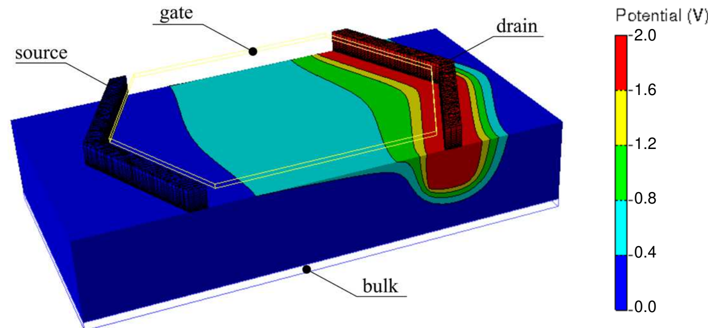
The 3D TCAD simulations graphically confirm the correctness of the theoretical section 4.1.2 of this thesis. As we can see, the theoretical characteristics

of electrostatic potential and current density (Fig. 4.1a-b) meet with the characteristics given by the 3D TCAD simulations. The results of these 3D TCAD simulations are depicted in Fig. 4.7a-b and Fig. 4.8a-b respectively for RLS MOS transistor and DLS MOS transistor. This similarity demonstrates the correctness of the proposed theoretical approach and can be reliable used for further research.

In the above-mentioned examples, the both RLS and DLS MOS transistors have the same effective aspect ratio $(W/L)_{\text{eff,SCT,num}}$ equal to 1.0, and DLS MOS transistor has α angle equal to 130° for this example. The gate-source voltage V_{GS} for these transistors has been set to 2.0 V and drain-source voltage V_{DS} has been set to 2.0 V. As we can see the electrostatic potential of the RLS MOS transistor Fig. 4.7a has the maximal voltage value on the drain electrode ($V_{\text{D}} = 2.0$ V), the minimum voltage value is on the source electrode ($V_{\text{S}} = 0$ V), and the voltage



(a) potential of the rectangular layout shape

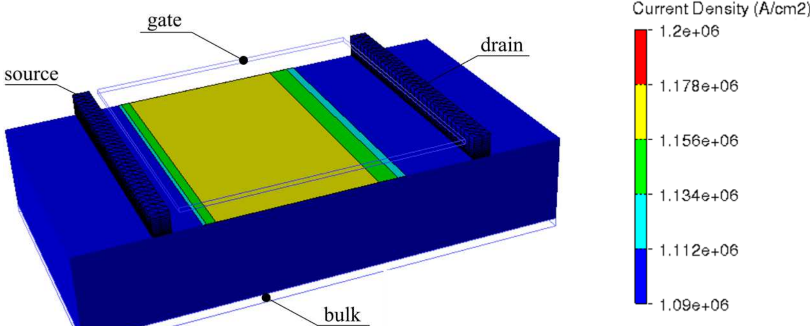


(b) potential of the diamond layout shape

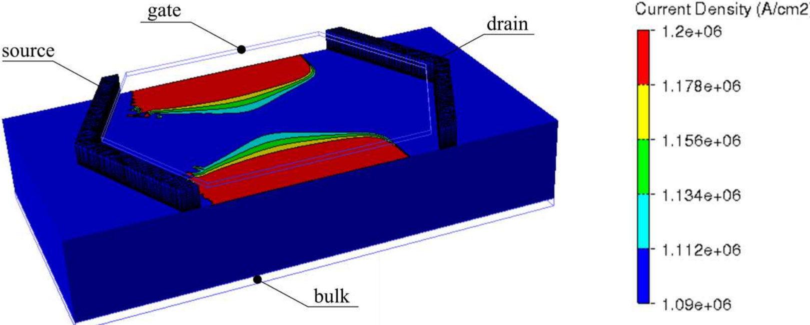
Fig. 4.7: Potential examples of the RLS, DLS respectively of MOS transistor for $(W/L)_{\text{eff}}$ equal to 1.0

gradient has orderly characteristics from the drain electrode to th e source electrode. The potential gradient sequentially changes throughout the physical width of the RLS MOS transistor at the same time. In the counterpart, for the DLS MOS transistor, the potential gradient does not change sequentially throughout the physical width of the DLS MOS transistor at the same time. The potential of the DLS MOS transistor changes in the specific equipotential lines as it has been presented in theoretical section 4.1.2 "The Innovative Analytical Description of the DLS MOSFET Based on the Schwarz-Christoffel Transformation" of this paper. In section 4.1.2, the electrostatic potential is described by vertical equipotential lines.

Since the equipotential lines are always perpendicular to electric field lines thus the current flow is perpendicular to the equipotential lines. The current flow along the channel length of the RLS/DLS MOS transistor is represented on Fig. 4.8a-b by current density. The Fig. 4.8a presents the current flow of the RLS



(a) current density of the rectangular layout shape



(b) current density of the diamond layout shape

Fig. 4.8: Current density examples of the RLS, DLS respectively of MOS transistor for $(W/L)_{\mathrm{eff}}$ equal to 1.0

MOS transistor. In this case, the current density is homogenously spread along the channel width of the MOS transistor. Instead in the DLS MOS transistor case (Fig. 4.8b), the current density reaches a maximum when the gate channel length is the shortest (the shortest distance between the source and the drain electrode). It is highlighted with red-colored region in Fig. 4.8b. Also, Fig. 4.8b shows how the current density decreases from the edge of the gate channel length of the DLS MOS transistor to the center of the DLS MOS structure, where the distance between the source to the drain electrode is maximum. In conformity with the theory already presented in theoretical section 4.1.2 “The Innovative Analytical Description of the DLS MOSFET Based on the Schwarz-Christoffel Transformation” of this paper. In section 4.1.2, the current density has been described by density of horizontal current lines from drain to source in the Fig. 4.1a. The higher density of the current flowlines crossing a certain part means the higher current density in this part because an equal amount of current flows between each neighboring pair of current flowlines [189]. In the 2D (two dimensional) case, the certain part is replaced by a line [190].

The simulated drain-source current enhancement $\delta I_{\mathrm{DS,TCAD}}$ related to the RLS MOS transistor, is given by the following expression (4.15)

$$\delta I_{\mathrm{DS,TCAD}} = \left(\frac{I_{\mathrm{DS,TCAD,DLS}} - I_{\mathrm{DS,TCAD,RLS}}}{I_{\mathrm{DS,TCAD,RLS}}}\right) \cdot 100 \tag{4.15}$$

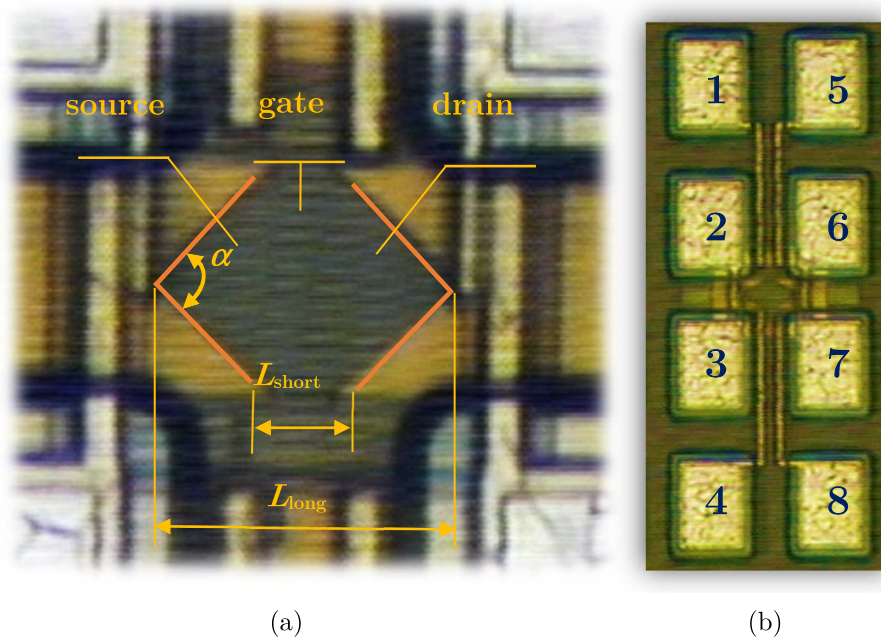
where $I_{\mathrm{DS,TCAD,DLS}}$ is a simulated drain-source current of the DLS MOS transistor, and $I_{\mathrm{DS,TCAD,RLS}}$ is a simulated drain-source current of the RLS MOS transistor.

The results of the this part are described in the section 4.2.5 “Results, Discussion and Comparison” together with the calculated results and measured results on silicon samples.

4.2.4 Experimental Measurement of the Drain-Source Current Enhancement In 160 nm BCD Technology Process

An example of the measured sample and its pad out for the four points measurement method is depicted in Fig. 4.9(a), and Fig. 4.9(b), respectively. In this example, the DLS NMOS transistor has an angle α equal to 100°. All measured samples are isolated with the triple well strategy [175]. Thanks to the triple well isolation, all devices are perfectly isolated from the substrate, and each of them has an independent bulk connection for each device. In our case, it is realized by Nwell isolation, which is connected to pad 1 in Fig. 4.9(b). The pad 2 is a drain terminal of the N-channel MOSFET device for the sensing of the electrical properties; pad 3 is used for the drain forcing by an external environment. The pad 4 controls the gate terminal, and the pad 5 is a bulk of the N-channel MOSFET device. The pad 6 and 7 are used for the sensing and forcing, respectively of the source terminal of the transistor. The last pad 8 is connected to the substrate of the samples.

Tab. 4.2 presents the physical dimensions of the devices that were implemented with the 160 nm BCD STMicroelectronics technology [174]. In this technology, 1 124 samples were fabricated, which were proportionally divided.



(a) (b)

Fig. 4.9: Photography of the DLS NMOS transistor with the angle $\alpha = 100°$ (a) and its pad out connections for four points measurements (b)

The first category is RLS MOS transistors ($\alpha = 180°$) as the reference devices and the other category are three types of DLS MOS transistors with the angles α equal to 120°, 100°, and 80°. All the fabricated devices have a similar area equal to 500 μm^2, and effective aspect ratio $(W/L)_{eff}$ equal to 2.004 (RLS MOS transistor, $\alpha = 180°$), 1.892 ($\alpha = 120°$), 1.834 ($\alpha = 100°$), and 1.758 ($\alpha = 80°$). The big effective active area of the MOSFETs ensures true measurement of MOS parameters, that are not affected by the short channel effect. The last column of the table represents the measured drain-source current enhancement $\delta I_{DS,Meas}$ (4.16) related to the RLS MOS transistor, given by the following expression:

$$\delta I_{\mathrm{DS,Meas}} = \left(\frac{I_{\mathrm{DS,Meas,DLS}} - I_{\mathrm{DS,Meas,RLS}}}{I_{\mathrm{DS,Meas,RLS}}}\right) \cdot 100 \tag{4.16}$$

where $I_{DS,Meas,DLS}$ is a measured drain-source current of the DLS MOS transistor, and $I_{DS,Meas,RLS}$ is a measured drain-source current of the RLS MOS transistor. The data in Tab. 4.2 have been given from the output characteristic of MOS transistors depicted in Fig. 4.10, where all data have been normalized to the same effective aspect ratio equal to 2.

Tab. 4.2: Dimensions of the measured and fabricated MOS transistors in BCD 160 nm technology

α (°)	W (μm)	L_{short} (μm)	L_{long} (μm)	$\left(\frac{W}{L}\right)_{eff}$ (-)	A (μm^2)	$\delta I_{DS,Meas}$ (%)
180	31.62	15.81	15.81	2.004	500	0.00
120	28.24	9.28	25.24	1.892	487	3.48
100	26.34	7.68	29.28	1.834	487	6.80
80	23.94	6.42	34.22	1.758	486	10.99

By analyzing Tab. 4.2, we can observe that DSL MOSFETs devices with a decreasing angle α have higher drain-source enhancement related to conventional rectangular MOS transistors. For example, for the DLS MOSFETs with the angle α equal to 80°, it is up to 10.99 %.

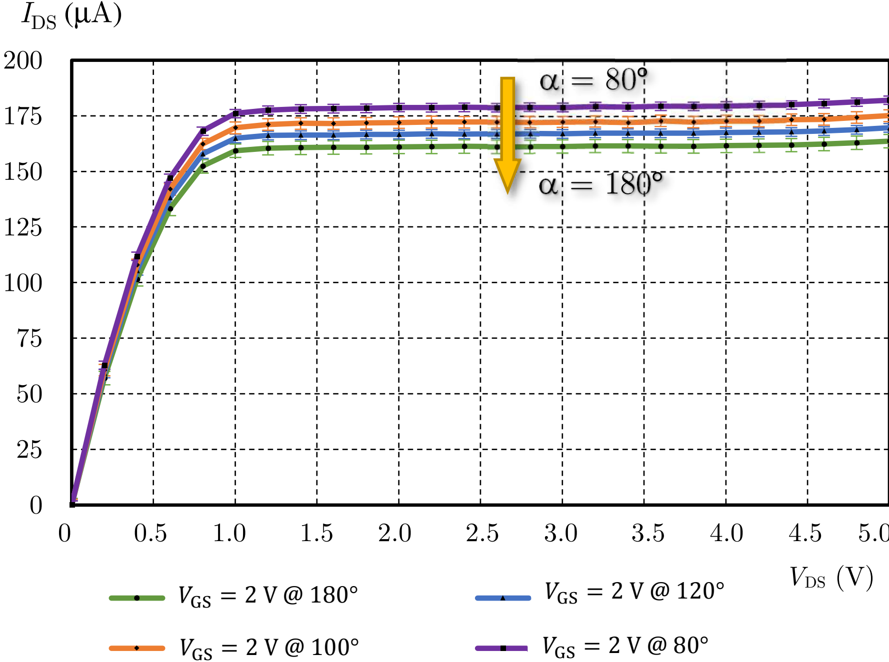


Fig. 4.10: Measurement results of performance improvement of the drain-source current in the saturation region of the DLS MOS transistor given from measured data

The following section compares all theoretical, simulated, and measured data in order to highlight the conformity between the innovative expression and the simulated and measured data.

4.2.5 **Results, Discussion and Comparison**

This section summarized the drain-source current enhancement results given by the theoretical calculation, 3D TCAD simulation and measurement. The following

(a) Comparison of the theoretical calculations with the 3D TCAD simulations

An example of the calculated and simulated drain-source current enhancement data ($\delta I_{DS,SCT}$ and $\delta I_{DS,TCAD}$,) for the case where the effective aspect ratio $(W/L)_{eff}$ is equal to 2.0 for various angles α (from 180° to 80°) and with the same active MOS transistor area equal to 10 μm^2 is presented in Tab. 4.3. The MOSFETs have been simulated in the saturation region, where $V_{DS} = 2.0$ V,

Tab. 4.3: Sample data of the enhancement saturation drain-source current δI_{DS} for both TCAD simulations and analytic calculations of the DLS MOS transistor for the various angles α, the same aspect ratio equal to 2.0 and the same active area.

α (°)	$\left(\frac{W}{L}\right)_{eff}$ (-)	A (μm²)	W (μm)	L_{short} (μm)	L_{long} (μm)	$\delta I_{DS,SCT}$ (%)	$\delta I_{DS,TCAD}$ (%)	$\epsilon I_{DS,SCT,TCAD}$ (%)
180	2.0	10	4.4721	2.2361	2.2361	0.00	0.00	0.00
170	2.0	10	4.4621	2.0459	2.4363	0.16	0.13	0.03
160	2.0	10	4.4321	1.8655	2.6470	0.44	0.37	0.07
150	2.0	10	4.3823	1.6948	2.8690	0.99	0.64	0.35
140	2.0	10	4.3132	1.5335	3.1034	1.50	1.76	-0.26
130	2.0	10	4.2251	1.3817	3.3519	2.40	2.21	0.20
120	2.0	10	4.1184	1.2393	3.6170	3.36	3.57	-0.20
110	2.0	10	3.9935	1.1059	3.9022	4.74	4.80	-0.05
100	2.0	10	3.8506	0.9815	4.2125	6.41	6.46	-0.05
90	2.0	10	3.6895	0.8656	4.5551	8.48	8.68	-0.19
80	2.0	10	3.5097	0.7579	4.9406	11.50	11.35	0.15

$V_{GS} = 2.0$ V, and V_{th} has been approximately 1.48 V – it has varied depending on the angle α of DLS MOS transistor.

The drain-source current enhancement is depicted in Fig. 4.11 for cases where the gate area of DLS MOSFET is set to A = 10 µm^2, an angle α is in a range from 180° to 80°, and effective aspect ratio $(W/L)_{\text{eff}}$ varies from 0.5 to 2.0.

By analyzing drain-source current enhancement curves as a function of an angle α (Fig. 4.11), it has been observed that the drain-source current enhancement significantly increases when the angle α decreases. The increase of the drain-source current is caused by the decreasing of the threshold voltage. The similar phenomenon has been presented in [125] for the circular gate layout shape. In the case of this thesis, when the effective aspect ratio $(W/L)_{\text{eff}}$ increases, the enhancement also increases. The maximal current enhancement of the simulated DLS MOS transistor is approximately 11.35 % for effective aspect ratio $(W/L)_{\text{eff}}$ equal to 2.0 and angle α equal to 80°.

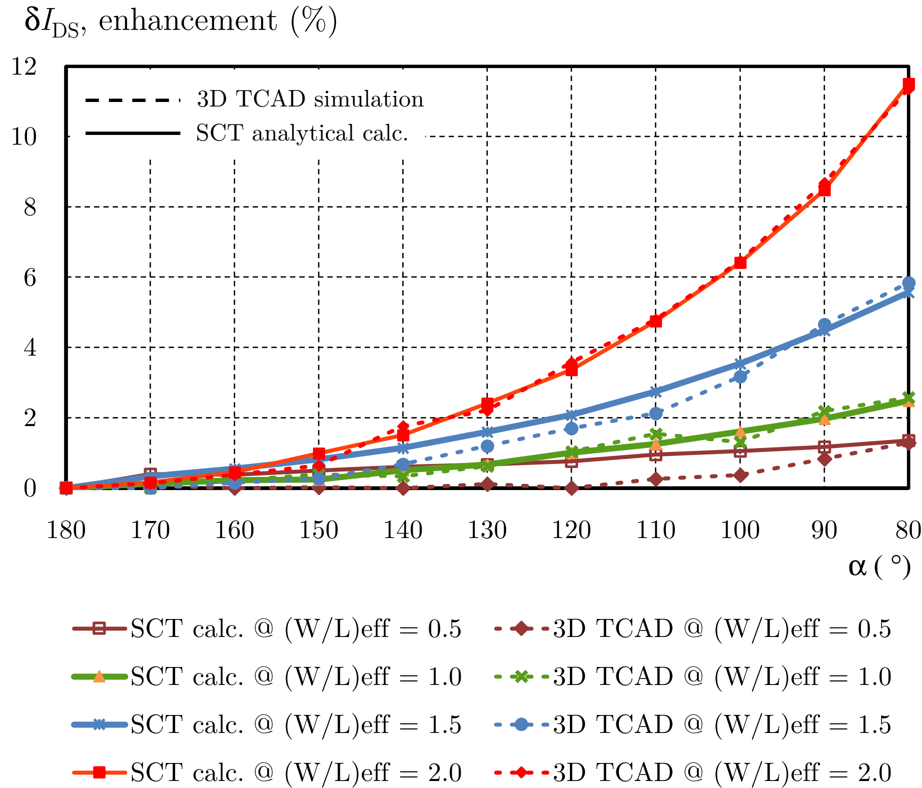


Fig. 4.11: A drain-source current enhancement in the saturation region of the DLS MOS transistors described by SCT model and TCAD simulations

The drain-source current enhancement depicted in Fig. 4.11 also shows a trend of it. Based on this trend, it can be supposed further increasing drain-source current enhancement with continuously decreasing the angle α, down to close to 0°. To be able to improve drain-source current for the given effective aspect ratio $(W/L)_{\text{eff}}$ with the given gate area A of the DLS MOS transistor, it is necessary to set the angle α of the DLS MOSFET based on the curves depicted in Fig. 4.11.

The last step is an error calculation of the given drain-source currents enhancements with the following expression (4.17)

$$\epsilon I_{\text{DS,SCT,TCAD}} = \delta I_{\text{DS,SCT}} - \delta I_{\text{DS,TCAD}} \tag{4.17}$$

By analyzing the error deviation $\epsilon I_{\text{DS,SCT,TCAD}}$ depicted in Fig. 4.12 it can be said that the proposed approach of the analytic calculation of the DLS MOS transistor fits very well with the simulated data. The maximal value of the error $\epsilon I_{\text{DS,SCT,TCAD}}$ is decreasing with the increasing angle α and it is less than 3 %. For the case shown in Tab. 4.3, it is less than 0.35 %.

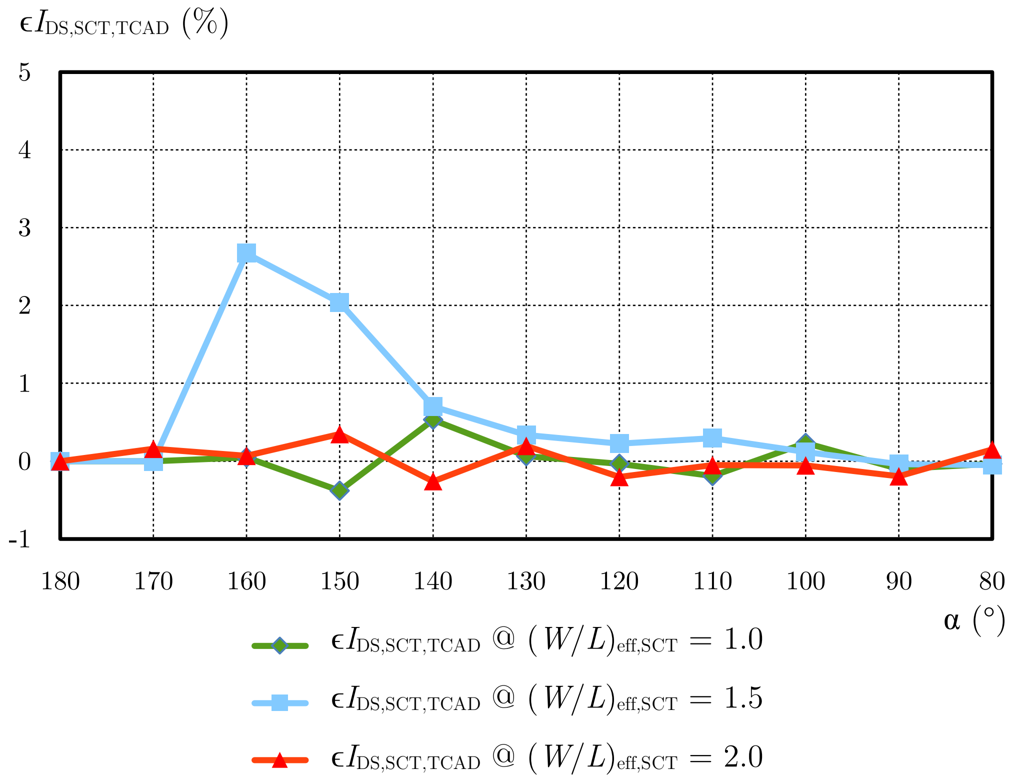


Fig. 4.12: Calculated error of the drain-source current between simulated and calculated results

(b) Comparison of the theoretical calculations, 3D TCAD simulations and the measured data

Finally, Fig. 4.13 proves the drain-source current enhancement concerning the RLS MOS transistor as a function of angle α, for the BCD 160 nm STMicroelectronics technology process (red crosses), TCAD simulations (yellow line), and the innovative theoretical calculation based on the Schwarz-Christoffel transformation (blue line). From Fig. 4.13, we can also see that the TCAD simulation, SCT model, and measurement fit very well together. So, it is a recommended approach for calculation MOS transistors with the diamond layout shapes, as well as for the other layout shapes, such as a waffle gate shape [191]. Moreover, from Fig. 4.13, we can see that the maximal drain-source current enhancement for the case where the aspect ratio of MOS transistor is set to 2, and angle α is equal to 80° is 11.50 %, 11.35 % and 10.99 % for SCT calculation, 3D TCAD simulations, and measurement, respectively.

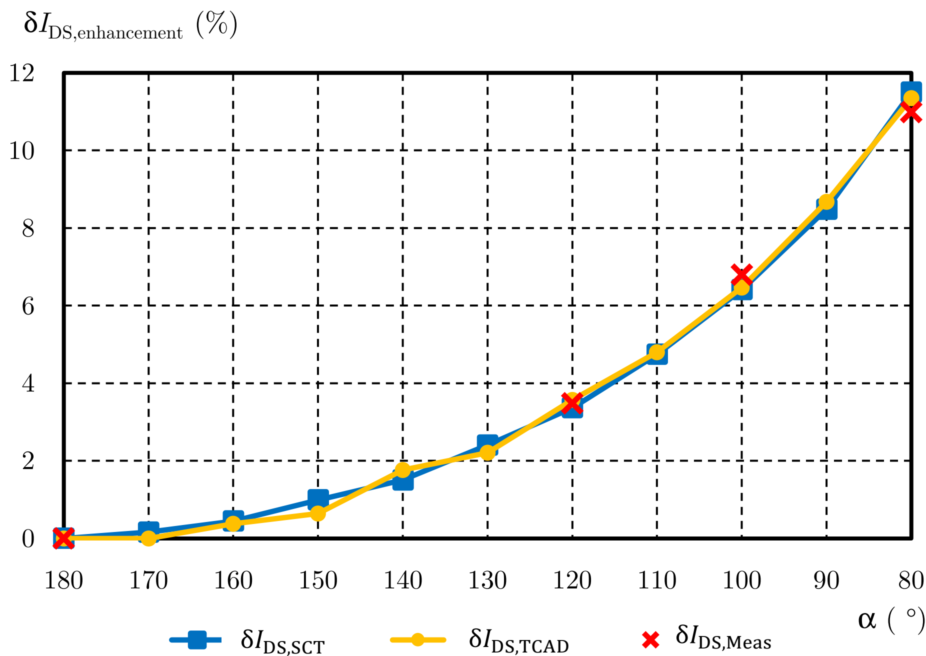


Fig. 4.13: A comparison of drain-source current enhancement given by theoretical calculation based on Schwarz-Christoffel transformation (blue line), TCAD simulations (yellow line), and measurement on samples in BCD 160 nm technology (red crosses)

(c) Comparison of the theoretical calculations and the measured data for different temperatures conditions

The measurements have been performed at temperatures equal to T = -25°C, 25°C, and 75°C.

The Fig. 4.14 proves the conformity of drain-source current enhancement in relation to the RLS MOS transistor as a function of angle α, for different temperatures of the chip die in the BCD 160 nm STMicroelectronics technology process, and the innovative theoretical calculation based on the Schwarz-Christoffel transformation. So, it is a recommended approach for calculation of the MOS transistors with the diamond layout shapes. Moreover, from Fig. 4.14, we can see that the maximal drain-source current enhancement for the case where the aspect ratio of MOS transistor is set to 2, and angle α is equal to 80° is 11.50 %, and 10.99 % for SCT calculation, and measurement at room temperature, respectively.

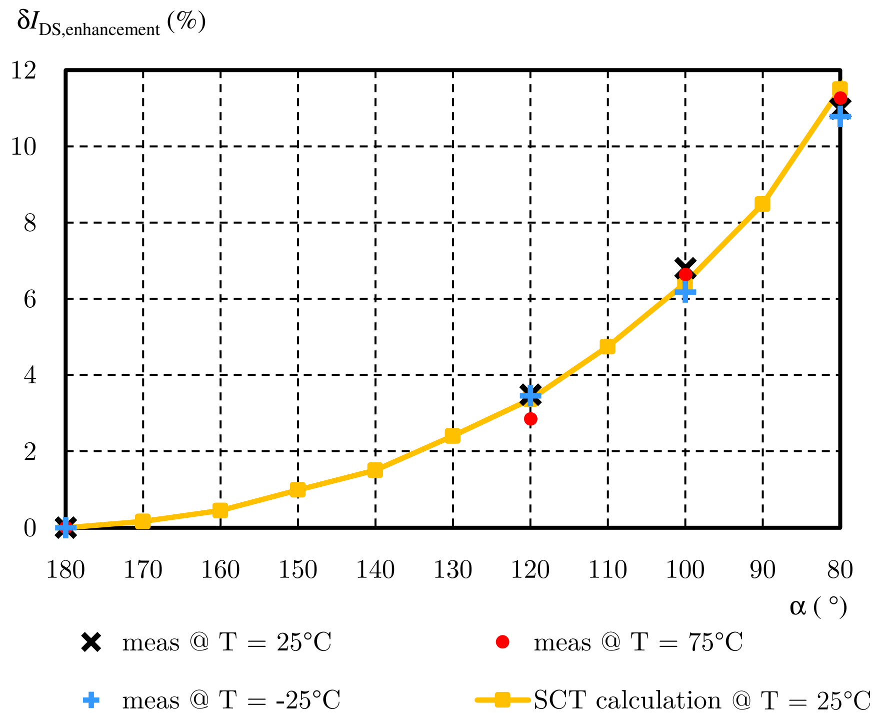


Fig. 4.14: A comparison of drain-source current enhancement given by theoretical calculation based on Schwarz-Christoffel transformation (yellow line), and measurement on samples in BCD 160 nm technology (black crosses T = 25°C, blue crosses T = -25°C and red dots T = 75°C).

4.2.6 **Summary**

This section emphasizes the quality of the innovative analytical expression for calculation of the aspect ratio of DLS MOS transistors based on the Schwarz-Christoffel transformation, which is used in real practical applications such as the computation of the improvements in the electrical performance of MOSFETs.

The first part of this section summarizes the theoretical calculations of the improvements in the electrical performances of the MOSFETs with the 3D TCAD simulations. The calculated and simulated results of the drain-source current fit very well together. In this way, the analytical expression proves its quality, and the error between analytical expression and simulation is lower than 3 %. It is a crucial point of this thesis because, thanks to that, we can estimate the DLS MOSFETs behavior. It allows us to precisely describe improvements in the electrical performances of the DLS MOS transistors in comparison to the conventional rectangular layout shape MOS transistors. Namely, it is a drain-source current enhancement, and based on that knowledge, we can easily predict where the maximum deviation happens and what the maximum value is. In the studied cases, the maximal drain-source current enhancement of the DLS MOSFETs given by numerical calculations and TCAD simulations is 11.50 %, respectively 11.35 % for effective aspect ratio $(W/L)_{\mathrm{eff}}$ equal to 2.0 and angle α set to 80°. All simulation results respect the same effective aspect ratio for all angles α and maintain the same gate area for all angles α, as well. Furthermore, there has been observed that the drain-source current enhancement significantly increases when the angle α decreases.

The second part compares all data given by the theoretical calculations, 3D TCAD simulations, and measurement on real silicon samples. Measurements have also proved the mentioned enhancement, where 1 124 samples in 160 nm BCD technology have been fabricated. The measurements were performed on the samples with the angles α equal to 180°, 120°, 100°, and 80°. As the conclusion of the measurement is that the drain-source current enhancement perfectly fits with the

numerical calculations and 3D TCAD simulations. The maximal measurement drain-source current enhancement result is excellent, and it is close to 11.00 % for the effective aspect ratio $(W/L)_{\mathrm{eff}}$ equal to 2.0 and angle α equal to 80°.

The last part graphically summarizes DLS MOSFETs for different temperature conditions. There has been confirmed the drain-source current enhancement is also valid for other temperature conditions, where the measurements have been performed at temperatures equal to T = -25°C, 25°C, and 75°C.

4.3 Precise Model of the Effective Threshold Voltage Changes in the DLS MOSFETs

All parts of this chapter have been published by the author with major contribution in the following reference:

D. Barri, P. Vacula, T. Grešl, V. Kotě, J. Jakovenko and J. Voves, "Precise Model of the Effective Threshold Voltage Changes in the DLS MOSFETs for Different Gate Angles Compared with the Measured Data." ***IEEE Transactions on Electron Devices***, under review. **(Quartile 1)**
Co-authorship: 70 %

4.3.1 Introduction

In the previous sections of this thesis, the latest analytical calculation method to express the effective aspect ratio of DLS MOSFETs, and improvements in the electrical performance of the DLS MOSFETs devices have been presented. In this section, there is presented an innovative and precise model, which describes the effective threshold voltage changes in the DLS MOSFETs for different gate angles. The innovative model is based on the 3D TCAD simulations data and compared with the measured data.

This section is arranged as follows: the first part 4.3.2, presents the general calculation of the threshold voltage of MOSFETs. The next 4.3.3 section introduces 3D TCAD simulated data and the innovative expression describing the effective threshold voltage changes. Part 4.3.4 presents measured data of the effective threshold voltage obtained from the real samples fabricated in the 180-nm BCD technology process. The following section 4.3.5, compares the measured and simulated data. Finally, section 4.3.6 summarizes achieved results and highlights the quality level of the presented innovative model.

4.3.2 **Threshold Voltage: Theoretical Background**

The threshold voltage (V_{th}) of the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), is a crucial electrical parameter, which defines the MOSFET turn on voltage and influence the transfer between the linear and saturation region [192]. Therefore, the threshold voltage plays a key role in the semiconductor industry, and any unpredictable behavior or its high sensitivity causes problems during front-end analog design. Such as, in the case of the high-precise voltage references [193, 194]. These unpredictable behaviors and V_{th} high sensitivities are present, for example, in the case of a TID effect (section 2.1.8), hump effect [195] (section 2.1.9), etc., but also in the case of the DLS MOSFET, which is the subject of this thesis. The unpredictable behavior of DLS MOSFET has not been described yet, and therefore and moreover this thesis also focuses on it.

Generally, the V_{th} is the value of the MOSFET gate-source voltage V_{GS} that will cause the interface potential to be equal in magnitude and opposite in sign to the substrate potential Φ_p [196]. Physically, for the N-channel MOSFET, it means that there would now be a concentration of mobile electrons at the surface equal in magnitude to a concentration of mobile holes in the P-substrate.

In common, the threshold voltage equals to the sum of the flatband voltage V_{FB}, twice the bulk potential Φ_p and the voltage across the oxide [197], such it is described in [198] by the following expression:

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + \gamma\sqrt{2(-\phi_{\mathrm{p}})} - 2\phi_{\mathrm{p}} \tag{4.18}$$

where the V_{FB} is the flatband voltage, the Φ_p is a workfunction of a substrate, and the γ is a body effect defined such as the following expression (4.19):

$$\gamma = \sqrt{2q\varepsilon_{\mathrm{Si}}N_{\mathrm{sub}}}/C_{\mathrm{ox}} \tag{4.19}$$

where q is the magnitude of the electron charge ($q = 1.602 \cdot 10^{-19}$ C), $\varepsilon_{\mathrm{Si}}$ is the permittivity of silicon, N_{sub} is the substrate impurity density in silicon. In case of the N-channel MOSFET $N_{\mathrm{sub}} = N_{\mathrm{A}}$, where N_{A} is the net ionized acceptor density. C_{ox} is a gate oxide capacitance of MOSFET.

After a routine operation, we will get the following expression (4.20) and its simplification (4.21) with basic technology parameters:

$$V_{\mathrm{th}} = \frac{T \log\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right) k_{\mathrm{B}}}{q} - \frac{T \log\left(\frac{N_{\mathrm{D}}}{n_{\mathrm{i}}}\right) k_{\mathrm{B}}}{q} + \frac{2\sqrt{\frac{T \log\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right) k_{\mathrm{B}}}{q}}\, t_{\mathrm{ox}} \sqrt{q N_{\mathrm{A}} \varepsilon_{\mathrm{Si}}}}{\varepsilon_{\mathrm{ox}}} \tag{4.20}$$

$$V_{\mathrm{th}} = \frac{T \log\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{D}}}\right) k_{\mathrm{B}}}{q} + \frac{2 t_{\mathrm{ox}} \sqrt{T \log\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right) k_{\mathrm{B}} N_{\mathrm{A}} \varepsilon_{\mathrm{Si}}}}{\varepsilon_{\mathrm{ox}}} \tag{4.21}$$

where the T is the temperature, k_{B} is the Boltzmann constant ($k_{\mathrm{B}} = 1.38 \cdot 10^{23}$ J K^{-1}). N_{D} is the donor impurity density in silicon, and n_{i} is the intrinsic doping concentration of silicon ($n_{\mathrm{i}} = 1.45 \cdot 10^{10}$ cm^{-3} at $T = 300$ K). $\varepsilon_{\mathrm{ox}}$ is the permittivity of oxide.

As it can be seen, the final expression (4.21) does not consider the geometry settings of the MOSFETs. In the case of DLS MOSFETs, it could be a problem in terms of circuits accuracy. For this reason, in this thesis is presented an innovative expression of the changes in the effective threshold voltage based on simulation data, which are compared with measured data with excellent results.

In this work, the sub-threshold drain current method [199] has been used to extract the effective threshold voltage. This method is a function of gate-source voltage below the threshold voltage and plotted as $\log(I_{\mathrm{DS}})$ versus V_{GS} [200]. All measurements have been adjusted for the four-points measurement approach [17]. The measurements have been performed in the linear region with drain voltage set to 0.05 V and with the gate voltage step size of 10 mV.

4.3.3 **3D TCAD Simulations of the Threshold Voltage**

In this research, the gate areas of MOSFETs have been set to A = 10 μm^2 with effective aspect ratios $(W/L)_{eff}$ varied from 0.5 to 2.0 with a step equal to 0.5. The DLS MOSFET's effective aspect ratio is described in section 4.1 of this thesis by the following expression:

$$\left(\frac{W}{L}\right)_{\text{eff}}^{\text{SCT,ana}} = \\ = \frac{2}{\frac{2L_{\text{short}}}{W'} - 7.10^{-5}\left(90 - \frac{\alpha}{2}\right)^2 + 1.57.10^{-2}\left(90 - \frac{\alpha}{2}\right) - 2.10^{-3}} \tag{4.22}$$

where an angle α is in degrees, a L_{short} is a shorter parallel side of the trapezoid, and a W' is a geometrical width of the trapezoid.

The simulation technological parameters of the DLS MOSFET have partially considered [174] as follows, a gate polysilicon thickness t_{gate} is equal to 0.2 μm, a gate oxide thickness t_{ox} is equal to 8.5 nm, drain/source thicknesses t_{N+} is equal to 0.4 μm, and a silicon thickness t_{Si} has been set to 1.0 μm. A Pwell and N^+ drain/source doping concentrations have been set to $1 \cdot 10^{16}$ cm^{-3} and $1 \cdot 10^{20}$ cm^{-3}, respectively.

The Atlas, 3D TCAD device simulation tool from Silvaco company, has been used to realize and simulate the DLS MOSFETs considering the same effective aspect ratio $(W/L)_{eff}$ with the same gate area A for any angle α. The 3-D numerical simulations were run with a lateral electric field-dependent model, a concentration-dependent mobility model, Selberherr impact ionization model, and Shockley-Read-Hall model for generation-recombination processes. In the TCAD simulations, the mesh grid has a direct effect on the accuracy and time of simulations. To find the proper grid is essential, and it has been considered in the case of these 3D TCAD simulations. The correct setting of the grid mesh has also been proved by measurements.

The 3D TCAD simulations data are shown in the following Tab. 4.4. and illustrated in Fig. 4.15.

The Tab. 4.4 presents simulated changes in the effective threshold voltage ($\delta V_{th,eff,TCAD}$) calculated by the following expression:

$$\delta V_{th,eff,TCAD} = \left(\frac{V_{th,eff,TCAD,DLS} - V_{th,TCAD,RLS}}{V_{th,TCAD,RLS}}\right) \cdot 100 \qquad (4.23)$$

where $V_{th,TCAD,RLS}$ is a threshold voltage of conventional rectangular layout shape MOSFET, and the $V_{th,eff,TCAD,DLS}$ is an effective threshold voltage of DLS MOSFETs.

Tab. 4.4: The simulated effective threshold voltage changes ($\delta V_{th,eff,TCAD}$) of DLS MOSFETs for different effective aspect ratios $(W/L)_{eff}$.

α (°)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff} = 2.0$ (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff} = 1.5$ (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff} = 1.0$ (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff} = 0.5$ (%)
180	0.00	0.00	0.00	0.00
160	-0.11	-0.07	0.01	-0.03
140	-0.30	-0.17	-0.04	-0.07
120	-0.63	-0.33	-0.13	-0.10
100	-1.16	-0.59	-0.23	-0.15
80	-1.92	-0.92	-0.39	-0.19

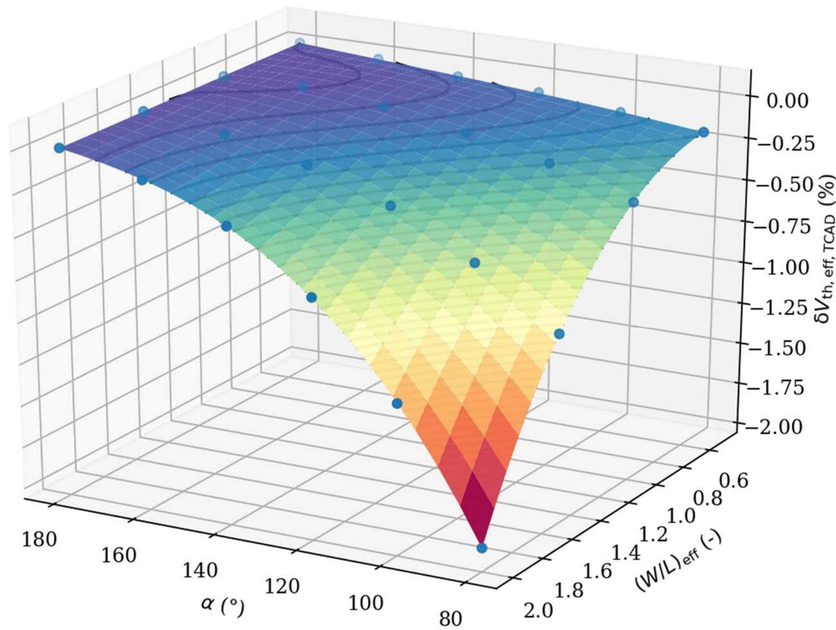


Fig. 4.15: Comparison of the effective threshold voltage decreasing for DLS MOSFETs with the different effective aspect ratio $(W/L)_{eff}$.

The Fig. 4.15 illustrates the comparison of the changes in the effective threshold voltage for RLS and DLS MOSFET devices. It has been studied at different effective aspect ratios $(W/L)_{\mathrm{eff}}$ equal to 2.0, 1.5, 1.0, and 0.5. As it can be seen, the simulated effective threshold voltage $(V_{\mathrm{th,eff,TCAD}})$ decreases if the angle α of the DLS MOSFETs decreases, too. And moreover, if the effective aspect ratio $(W/L)_{\mathrm{eff}}$ increases, the $V_{\mathrm{th,eff,TCAD}}$ decreases more significantly. It is an interesting point that can be useful, for example, for the effective threshold voltage trimming of MOSFET devices in integrated circuits (ICs).

$$\begin{aligned}
\delta V_{\mathrm{th,eff,approx}} = {} & -1.349 + \alpha\, 7.57\cdot 10^{-2} + \left(\frac{W}{L}\right)_{\mathrm{eff}} 5.244 - \alpha \left(\frac{W}{L}\right)_{\mathrm{eff}} 0.387 \\
& -\alpha^2 1.62\cdot 10^{-3} + \alpha^2 \left(\frac{W}{L}\right)_{\mathrm{eff}} 9.2\cdot 10^{-3} - \alpha^2 \left(\frac{W}{L}\right)^2_{\mathrm{eff}} 1.39\cdot 10^{-2} - \left(\frac{W}{L}\right)^2_{\mathrm{eff}} 7.09 \\
& + \alpha \left(\frac{W}{L}\right)^2_{\mathrm{eff}} 0.554 + \left(\alpha^3 1.052 - \alpha^3 \left(\frac{W}{L}\right)_{\mathrm{eff}} 6.152 + \alpha^3 \left(\frac{W}{L}\right)^2_{\mathrm{eff}} 9.573\right)\cdot 10^{-5} \\
& - \alpha^3 \left(\frac{W}{L}\right)^3_{\mathrm{eff}} 3.614\cdot 10^{-5} - \left(\frac{W}{L}\right)^3_{\mathrm{eff}} 5.232 + \alpha \left(\frac{W}{L}\right)^3_{\mathrm{eff}} 6.702\cdot 10^{-3} \\
& + \alpha^2 \left(\frac{W}{L}\right)^3_{\mathrm{eff}} 3.832\cdot 10^{-3}
\end{aligned} \tag{4.24}$$

In the case of trimming effective threshold voltage, there is important to know how much the $V_{\mathrm{th,eff}}$ will be changed. Therefore, there has been simulated $V_{\mathrm{th,eff}}$ variation $\delta V_{\mathrm{th,eff,TCAD}}$ (Fig. 4.15), which has been approximated by the third order polynomial fitting function (4.24). It describes the decreases of the effective threshold voltage as a function of angle α and effective aspect ratio $(W/L)_{\mathrm{eff}}$. This trend is valid independently on MOSFET physical characteristics such as a gate material, a gate oxide thickness, and so on, because it defines just a variation of the effective threshold voltage of DLS relative to RLS. In case of needs, an absolute value of the DLS MOSFET effective threshold voltage can be derived from (4.23), where $V_{\mathrm{th,TCAD,RLS}}$ is close to V_{th} $(V_{\mathrm{th,TCAD,RLS}} \cong V_{\mathrm{th}})$ defined by the analytical

expression It could be also important in analog design with DLS MOSFETs [201]. The final expression fits the simulated data with excellent results, where root mean square error (RMSE) parameter is equal to 0.00307, and R-squared parameter is equal to 0.99995. The innovative expression (4.24) is illustrated in Fig. 4.15 as the 3D surface plot and its contour plot is illustrated in Fig. 4.16.

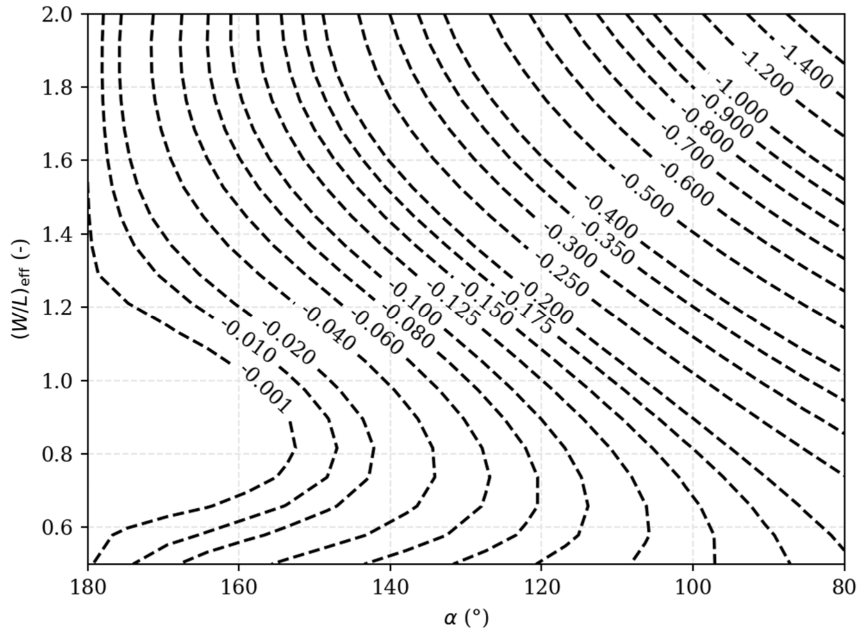


Fig. 4.16: Contour plot of effective threshold voltage variation ($\delta V_{\text{th,eff,approx}}$) as a function of angle α and effective aspect ratio $(W/L)_{\text{eff}}$.

4.3.4 **Experimental Measurement of the Threshold Voltage**

The measured test structures for this thesis are N-channel DLS MOSFET devices with 1.8 V operating voltages fabricated in a 160-nm BCD technology process with a triple well isolation.

For this study, 1 124 samples were fabricated, which were proportionally divided into four different structures shown in Tab. 4.5. The first structures are reference conventional rectangular layout shape (RLS) MOS transistors ($\alpha = 180°$) and the other structures are DLS MOS transistors with the angles α equal to 120°, 100°, and 80°. All the fabricated devices have a similar area equal to 500 µm^2, and effective aspect ratio $(W/L)_{\text{eff}}$ equal to 2.004 ($\alpha = 180°$; RLS MOSFET), 1.892 ($\alpha = 120°$), 1.834 ($\alpha = 100°$), and 1.758 ($\alpha = 80°$).

Tab. 4.5: The measured effective threshold voltage changes ($\delta V_{th,eff,meas}$) of DLS MOSFETs for different effective aspect ratios $(W/L)_{eff}$.

α	W	L_{short}	L_{long}	A	$\delta V_{th,eff,meas}$ @ $(W/L)_{eff} = 2.0$
(°)	(μm)	(μm)	(μm)	(μm²)	(%)
180	31.62	15.81	15.81	500	0.00
120	28.24	9.28	25.24	487	-0.63
100	26.34	7.68	29.28	487	-1.16
80	23.94	6.42	34.22	486	-1.94

The Tab. 4.5 presents measured threshold voltage changes ($\delta V_{th,eff,meas}$) calculated by the following expression:

$$\delta V_{th,eff,meas} = \left(\frac{V_{th,eff,meas,DLS} - V_{th,meas,RLS}}{V_{th,meas,RLS}} \right) \cdot 100 \tag{4.25}$$

where $V_{th,meas,RLS}$ is a measured threshold voltage of conventional RLS MOSFET, and $V_{th,eff,meas,DLS}$ is a measured effective threshold voltage of DLS MOSFETs. Both $V_{th,meas,RLS}$, and $V_{th,eff,meas,DLS}$ have been measured by sub-threshold drain current extraction method [199]. This method is a common practice reference method for a long time, and it has been sequentially applied on RLS MOSFETs ($\alpha = 180°$), and DLS MOSFETs with angle α equal to 120°, 100°, and 80°.

All the measured data of the experimental devices and their details are depicted in plots, Fig. 4.17 and Fig. 4.18, respectively. Fig. 4.17 and Fig. 4.18 illustrate the measured data (solid lines), the sub-threshold drain current extraction data (dashed lines), and the constant drain-source current level $I_{DS,RLS}$ (dot line). The extracted threshold voltage of the RLS MOSFET ($V_{th,RLS}$) defines $I_{DS,RLS}$. Both, the extracted values are in accordance with the technological process data, and thus they confirm the correctness of the method used. To maintain the same $I_{DS,RLS}$ level also for DLS MOSFETs, the lower gate-source voltage level, i.e. $V_{th,eff,DLS,}$ is required. If the angle α of DLS MOSFETs decreases, the effective threshold voltage decreases,

too. This means that in order to achieve the same drain-source current level for both RLS and DLS MOSFETs, the required effective threshold voltage is lower for DLS MOSFETs than for RLS MOSFETs.

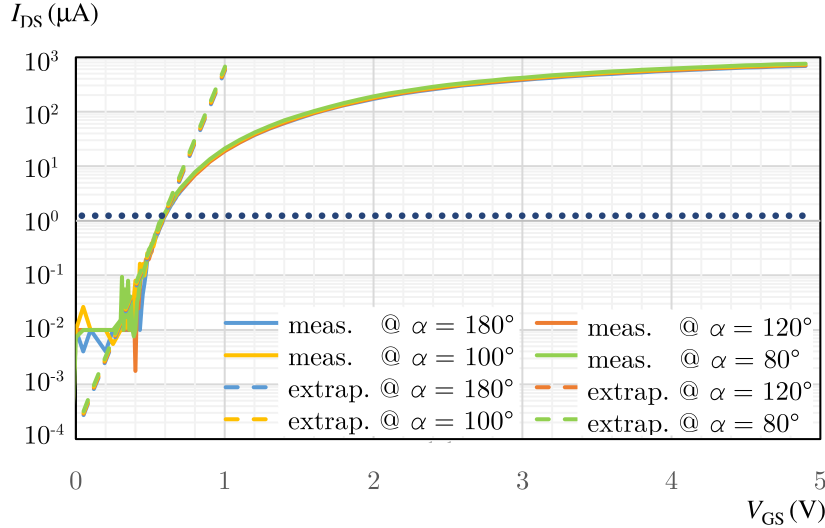


Fig. 4.17: Transfer characteristics of DLS MOSFETs with angle $\alpha = 180°$ (blue), 120° (brown), 100° (orange), and 80° (green).

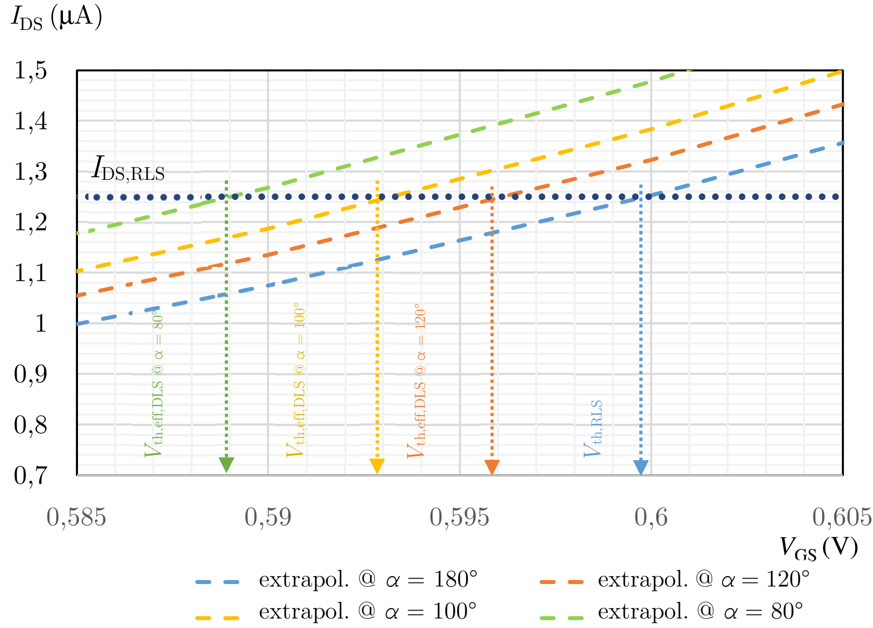


Fig. 4.18: Transfer characteristics of DLS MOSFETs with angle $\alpha = 180°$ (blue), 120° (brown), 100° (orange), and 100° (green) – in details.

The measured data and post-processed results are independently depicted in Fig. 4.19 – Fig. 4.26. There are shown transfer characteristics and details of the transfer characteristics for the RLS MOSFET and DLS MOSFETs, as well.

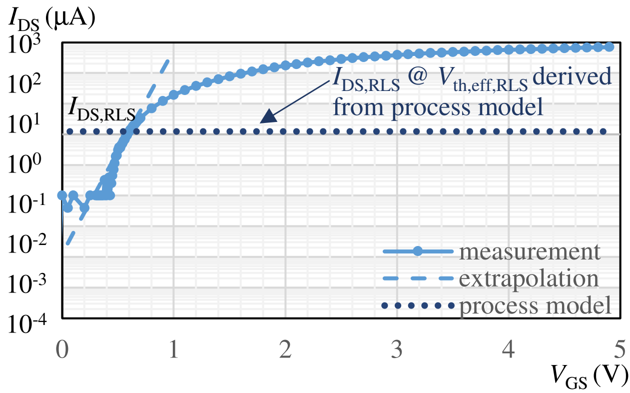


Fig. 4.19: Transfer characteristic of DLS MOSFET with angle $\alpha = 180°$.

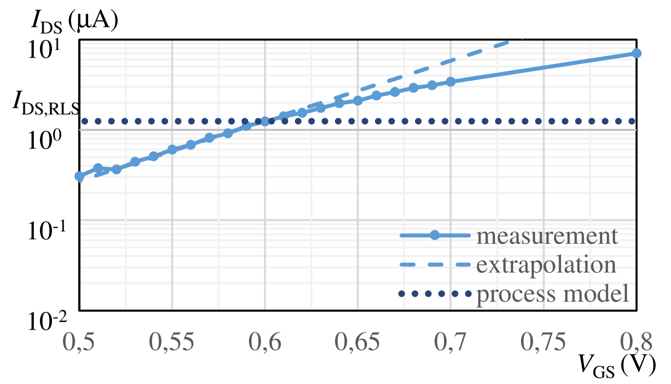


Fig. 4.20: Transfer characteristic of DLS MOSFET with angle $\alpha = 180°$ (detail).

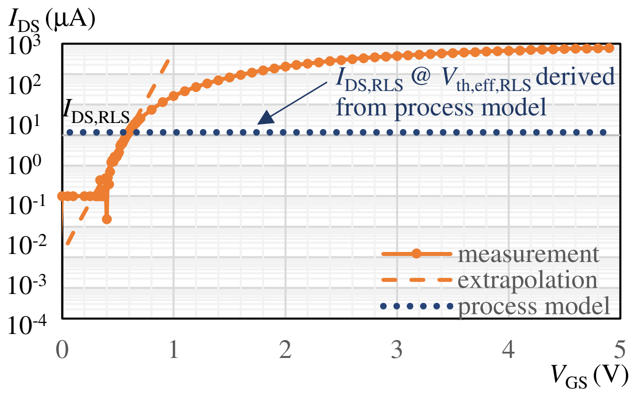


Fig. 4.21: Transfer characteristic of DLS MOSFET with angle $\alpha = 120°$.

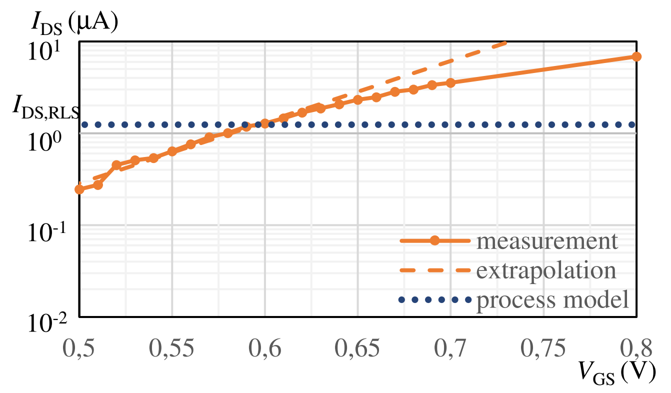


Fig. 4.22: Transfer characteristic of DLS MOSFET with angle $\alpha = 120°$ (detail).

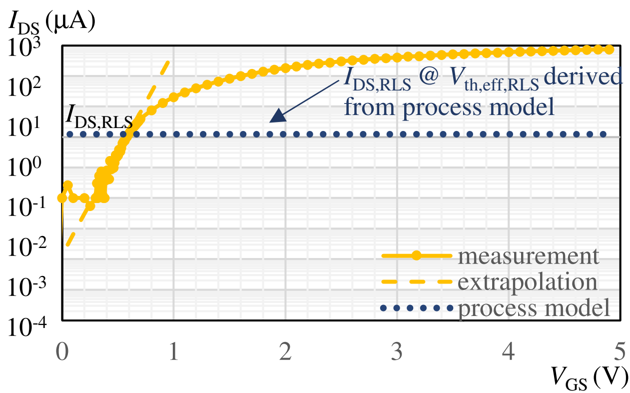


Fig. 4.23: Transfer characteristic of DLS MOSFET with angle $\alpha = 100°$.

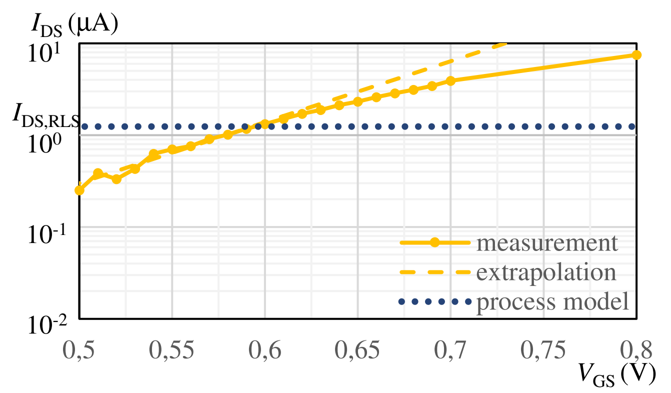


Fig. 4.24: Transfer characteristic of DLS MOSFET with angle $\alpha = 100°$ (detail).

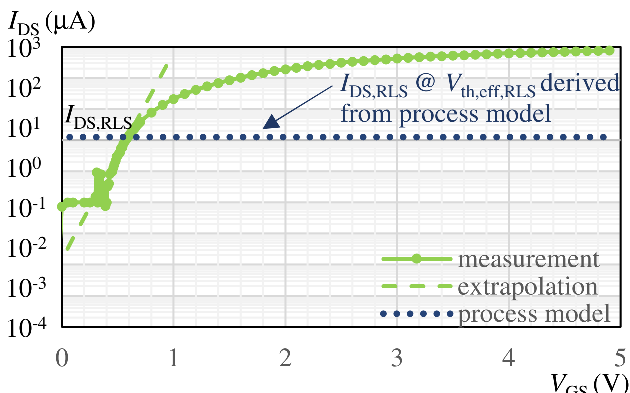


Fig. 4.25: Transfer characteristic of DLS MOSFET with angle $\alpha = 80°$.

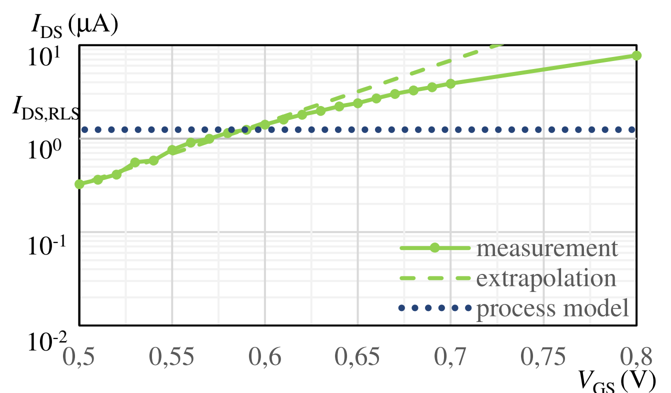


Fig. 4.26: Transfer characteristic of DLS MOSFET with angle $\alpha = 80°$ (detail).

4.3.5 **Results, Discussion and Comparison**

The following Tab. 4.6 summarizes $\delta V_{\text{th,eff,TCAD}}$, $\delta V_{\text{th,eff,approx}}$, and $\delta V_{\text{th,eff,meas}}$ data with the excellent conformity depicted in Fig. 4.27. All the results fit very well together, and therefore, in the case of the IC analog design with DLS MOSFETs, it is recommended to use the innovative expression (4.24). Only in this way we can ensure the high accuracy level of the calculated drain-source current.

Tab. 4.6: Summary of the effective threshold voltage changes of DLS MOSFETs for effective aspect ratio $(W/L)_{\text{eff}}$ equal to 2.0 and different angles α.

α (°)	$\delta V_{\text{th,eff,TCAD}}$ @ $(W/L)_{\text{eff}} = 2.0$ (%)	$\delta V_{\text{th,eff,approx}}$ @ $(W/L)_{\text{eff}} = 2.0$ (%)	$\delta V_{\text{th,eff,meas}}$ @ $(W/L)_{\text{eff}} = 2.0$ (%)
180	0.000	0.000	0.000
160	-0.11	-0.11	-
140	-0.30	-0.30	-
120	-0.62	-0.63	-0.63
100	-1.16	-1.16	-1.16
80	-1.91	-1.95	-1.94

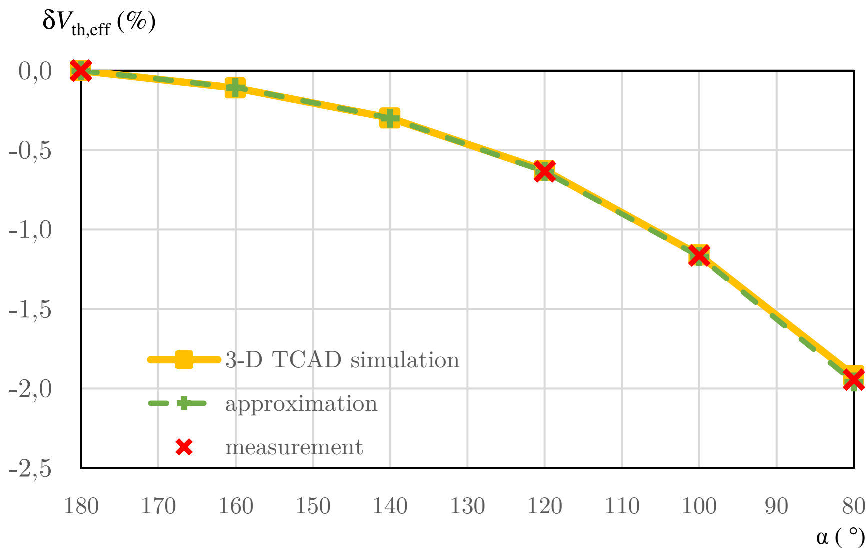


Fig. 4.27: A Comparison of changes threshold voltage given by TCAD simulation, analytical approximation, and measurement.

In the case of the drain-source current calculation, it also should be respected different hole and electron mobility ($\mu_{0,\text{P}}$, $\mu_{0,\text{N}}$) in MOSFETs affected by the different MOSFET channel orientation [202, 203]. In [204], the drain-source current can be

varied up to 42 % dependently on the channel and silicon orientation. In the case of this article, there has been used CMOS standard (100) silicon wafers [205] and N-channel DLS MOSFETs have a top and bottom edge of the channel aligned with <110> direction. Crystalline orientations in channel area varied dependently on the geometry settings of DLS MOSFET due to curved current trajectory. For the drain-source current calculation of N-channel DLS MOSFET devices, the following fitting function (4.26) should be used. In this way, we can respect different channel orientations and electron mobility.

$$\mu_{0,\mathrm{N,eff}} = (-9.8235 \cdot 10^{-4}\, \alpha^2 + 1.9913 \cdot 10^{-1}\, \alpha - 3.0154)\, \mu_{0,\mathrm{N}} \tag{4.26}$$

where $\mu_{0,\mathrm{N,eff}}$ is effective electron mobility as a function of angle α of DLS MOSFET devices and electron mobility for N-channel RLS MOSFET devices $\mu_{0,\mathrm{N}}$.

The presented effective threshold voltage phenomenon could be explained such as consequence of the multi-threshold transistor consists of infinitive numbers of curved narrows MOSFETs with different channel lengths [206, 207].

The threshold voltage variation, which has been confirmed by the measurement, is relatively small. But due to a quadratic dependence of the drain-source current on V_{th} in the above-threshold region and exponential dependence of the drain-source current on V_{th} in the sub-threshold region, each V_{th} modification should be considered. Moreover, in the case where the V_{GS} is close to V_{th}, the consequence of the V_{th} variation is even more significant. This is the case, when the circuits operate in an ultra-low voltage domain, such as operating voltage below 1.0 V, and low temperatures [208]. In the case when the angle α is set to 80° and respecting [208], the V_{th} variation may be up to 18 mV, which is a relatively a lot. The presented possibility to change V_{th} can help to complete the design comfortably.

In the case of the high electric field, the effect of the hot-carrier injections is significant and should be respected. The HCE can occur when relatively "high-voltage" conditions are present or when a short MOSFET channel length is used.

In both upper cases, we should avoid using the sharpest shape angles as much as possible.

However, the advantage and purpose of the diamond layout shape are not to suppress hot-carrier injections but to increase the performance of the MOSFET, where HCE or SCE is not expected. For example, it is in the case when we use current mirrors structures in low-voltage and low-power applications. Such as an example of this application can be, for example, ultra-low-power RFID circuits. In this case, we can use the diamond layout shape successfully.

In the case, where we use the diamond layout shape with the angle equal to 80° (it is not the sharpest shape), we can save up to 11 % of the total area, or we can boost the MOSFET performances by 11 %. There is already an existing design, where the diamond layout shape approach has been successfully used [201].

Another shape in comparison to diamond layout shape is for example waffle topology. There is also a potential risk of HCE, but as we can see in [134] it can be used in a real application and it saves over 10 % of the related area.

Finally, the design based on the diamond layout shape makes sense for low voltage and ultra-low voltage applications where we can recommend using the diamond layout shape with the angle up to 80°. The diamond layout shape with angles higher than 80° have been validated by measurement. There we can define the question of how to define the limit of the angle to avoid HCE. This question is a good idea for the next evaluation and future work.

4.3.6 **Summary**

This interesting section presents the changes in the effective threshold voltage of the DLS MOSFET devices dependently on its shapes. For this reason, the DLS MOSFET structures have been simulated in 3-D Silvaco TCAD simulator as well as they have been verified by measurement on samples. Moreover, the described phenomenon has been for the first time numerically approximated by the expression with a very high accuracy level equal to 99.995 % for the measurement, simulation and numerical setup described in section 3.3.

There has been observed, if the angle α of the DLS MOSFETs decreases, the effective threshold voltage $V_{\mathrm{th,eff,DLS}}$ decreases too. In additional, if the effective aspect ratio $(W/L)_{\mathrm{eff}}$ of DLS MOSFETs increases, the effective threshold voltage decreases more significantly.

The advantage of the diamond layout shape in compared with the conventional rectangular layout shape is in the possibility to reduce V_{th} selectively for the interesting MOSFET and without any technology process modification. This is very important point, because without any extra expenses we are able to trim or reduce the threshold voltage for the requested MOS transistor selectively and not for the whole IC as it is in case of V_{th} change with a process modification. In the case of thickness modification, it is not possible to do selectively, but globally for the same kind of the MOSFET components. This kind of MOSFET process component can be for example LV-MOSFET, HV-MOSFET and so on.

In both measurement and simulation cases, the effective threshold voltage for the DLS MOSFET with the effective aspect ratio $(W/L)_{\mathrm{eff}}$ equal to 2.0, and angle α set to 80° has been decreased close to by -2 %. The threshold voltage variation, which has been confirmed by the measurement, is relatively small but due to quadratic dependence of the drain-source current on V_{th}, the effect is not negligible.

This section apprises us about the interesting phenomena in IC DLS MOSFETs that can be used for both effective threshold voltage trimming as well as for the analog ICs design using DLS MOSFETs.

Chapter 5

Conclusions and Scope for Future Work

5.1 Conclusions

This thesis focuses on the crucial question of how to improve the electrical performances of MOSFETs in integrated circuits by physical mask design. For this reason, the technical analyses of many different mask designs have been studied in detail. As a result of these analyses has been observed, the diamond layout shape MOS transistors have not been precisely modeled so far. For this reason, the investigations of this thesis are related to DLS MOSFETs and these investigations have been split into the three following parts, where:

- For the first time, the innovative analytical description of the effective aspect ratio of DLS MOSFETs has been described
- For the first time, the improvements in the electrical performances of the DLS MOSFETs have been calculated, simulated, and measured in 180 nm BCD technology process

- For the first time, the precise model of the effective threshold voltage has been numerically approximated, simulated, and compared with the measured data.

The first part of this thesis “Analytical Description of the Effective Aspect Ratio of DLS MOSFETs” have proposed an innovative approach how to calculate the effective aspect ratio of the DLS MOSFETs and has been published in **IEEE Transaction on Electron Devices** [6]. The result of this approach is an innovative expression, which has been compared with the already one existing method. The already one existing method is based on the LCE+PAMDLE approach and it is just the first order approximation of the aspect ratio of the DLS MOSFETs. The new investigated model has an innovative analytical description based on a conformal mapping theory. As a conformal mapping, there has been chosen a Schwarz-Christoffel (SC) transformation. The maximal deviation values of the aspect ratio calculated by LCE+PAMDLE are in the range from -27 % to +38 %. In counterpart with the new SC analytical expression of the DLS MOSFETs the maximal deviation values are in the range from 0 % to -5.5 %.

The second part of this thesis describes improvements in the electrical performances (the drain-source current) of the MOS transistors and has been published in **IEEE Transaction on Electron Devices** [7] and **IEEE conference** [17]. It is based on the geometrical modification of MOSFET's channel from rectangular layout shape (RLS) into a diamond layout shape (DLS). In this way, the drain-source current enhancement is increased up to 11 % for the DLS MOS transistors with an effective aspect ratio $(W/L)_{\mathrm{eff}}$ equal to 2.0, and angle α set to 80°. Moreover, there is present the comparison of 3D TCAD simulations data, analytical model data based on Schwarz-Christoffel transformation, and measurement data given by measurement of the MOS transistors fabricated in the BCD 160 nm technology process. For this purpose, there have been fabricated 1 124 samples, which were proportionally divided into RLS MOSFETs and DLS MOSFETs with the angles equal to 120°, 100°, and 80°. For all studied aspect

ratios, the presented model has an excellent analytic description in comparison with the 3D TCAD simulation results with an error lower than 3 %. So, it proves the quality of the analytical model based on the SC transformation approach, and it is the recommended approach to use also for modeling other MOSFET gate layout shapes.

The third part presents an interesting phenomenon related to the effective threshold voltage changes in the diamond layout shape MOS transistors and is under review in **IEEE Transaction on Electron Devices**. Besides it, its analytical expression is presented here for the first time. The analytical approximative expression has been defined based on the results of the 3D TCAD simulations for the different effective aspect ratio and different angle α of DLS MOSFET. The effective aspect ratio has been set to 2.0, 1.5, 1.0, 0.5 with the angle α varied from 180° to 80° with the step 20°. Furthermore, for purpose to verify the 3D TCAD simulation results and measurement results, 1 124 samples were fabricated, which were proportionally divided into rectangle layout shape (RLS) MOSFETs and DLS MOSFETs with the angles α equal to 120°, 100°, and 80°. All the samples have been fabricated in the 160 nm BCD technology process. The mentioned phenomenon described by the proposed expression fits the measured data with a very high level of accuracy equal to 99.995 %. Thus, the presented analytical expression proves its quality. Thanks to the high level of the expression quality, the given expression is recommended to use for the analog designs with high-level precision requests and DLS MOSFET components.

All the achieved innovative results are essential for the case, where the DLS MOSFETs devices are used in the front-end design of the integrated circuits.

To have the above-mentioned DLS MOSFETs' advantages, it is essential to respect conditions in which the DLS MOSFETs can work. The first one is to avoid using the DLS MOSFET with small geometric sizes, because it may cause a high peak field and current concentration at the local angle region of the DLS MOSFET topology. The second condition is using the DLS MOSFET in low-voltage and low-

power applications which is a trend of nowadays ICs. In this way, we can reduce the total die area up to 36.9 % compared to the same circuit using the conventional MOSFETs [201]. These conditions are typically requested in real applications [134]. Moreover, in this case, another non-conventional MOSFET shape topology with sharp angles has been successfully used as well [134].

Furthermore, this approach is very useful in terms of V_{th} modification for the selectively requested components. In general, the V_{th} can be changed by process modification (4.21), as an example modification of the gate insulator's thickness. Nevertheless, in this case, this approach modifies the effective V_{th} of one type of component and not selectively, such as the presented approach enables it.

In summary, all the defined goals have been successfully solved with positive feedback for the further development of integrated circuits in the semiconductor industry. This thesis describes more precisely the approach on how to calculate the effective aspect ratio of the diamond layout shape MOS transistors. In this case, the newly described method has a maximal deviation value of the calculated effective aspect ratio in the range from 0 % to -5.5 % instead of -27 % to +38 % of the recently described method based on the LCE+PAMDLE effects. Furthermore, the MOS transistor with the diamond layout shape has better electrical performance compared to the conventional rectangular MOS transistor. In this case, the drain-source current enhancement increases up to 11 % for the DLS MOS transistors with an effective aspect ratio $(W/L)_{eff}$ equal to 2.0, and angle α set to 80°. Moreover, the ability to adjust the effective threshold voltage of the DLS MOS transistors by the different geometry settings of the transistor has been observed. For example, in the case when the angle α is set to 80°, it has been close to -2.0 %. Although the threshold voltage variation is relatively small, due to a quadratic dependence of the drain-source current on V_{th} in the above-threshold region and exponential dependence of the drain-source current on V_{th} in the sub-threshold region, each V_{th} modification should be considered. Moreover, in the case where the V_{GS} is close to V_{th}, the consequence of the V_{th} variation is even more significant.

This is the case, when the circuits operate in an ultra-low voltage domain, such as operating voltage below 1.0 V, and low temperatures [208]. In the case when the angle α is set to 80° and respecting [208], the V_{th} variation may be up to 18 mV, which is relatively a lot. The presented possibility to change V_{th} can help to complete the design comfortably.

All the presented goals have been confirmed by the measurement and for this purpose 1 124 samples were fabricated which were proportionally divided into RLS MOSFETs and DLS MOSFETs with the angles equal to 120°, 100°, and 80°.

5.2 Future Work

This thesis achieved great results, in the description of the innovative analytical expression of the effective aspect ratio of the DLS MOSFETs; in the description of the improvements in the electrical performances of DLS MOSFETs; and also in description of the interesting phenomenon related to the effective threshold voltage changes in the diamond layout shape MOS transistors. Further, this work can be extended to circuit levels design since this thesis is limited to the device level. Integrated circuits, such as operation amplifiers, current bias, voltage references, can be explored with the DLS MOSFETs. Such as the other topic, this thesis can be extended to study the effect of the crystalline orientation on the improvement in the electrical performances of DLS MOSFETs. In this thesis, the crystalline mesh (100) with the DLS MOSFET device orientation <110> has been used. In could be interesting to investigate in detail more different crystalline directions and more device orientations on the die as well.

5.3 Final Words

The future of the electronics will depend on its efficiency, cost, and reliability. Thanks to the investigated DLS MOSFET approach, the efficiency can increase, and or the cost can decrease. It can make the electronics more available for each of us, and in this way, we also can protect a vital environment.

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Appendix A:
List of Author’s Publications

A.1. Publications Related to the Topic of This Work

A.1.1. Publications in Impacted Journals

D. Barri, P. Vacula, T. Grešl, P. Švancara, V. Kotě, J. Jakovenko and J. Voves, “MOSFETs’ Electrical Performance in the 160-nm BCD Technology Process with the Diamond Layout Shape.” ***IEEE Transactions on Electron Devices***, vol. 67, no. 8, pp. 3270-3777, August 2020, doi: 10.1109/TED.2020.3000744.
Co-authorship: 61 %, **(Quartile 1)**

D. Barri, P. Vacula, V. Kotě, J. Jakovenko and J. Voves, “Improvements in the Electrical Performance of IC MOSFET Components Using Diamond Layout Style Versus Traditional Rectangular Layout Style Calculated by Conformal Mapping.” ***IEEE Transactions on Electron Devices***, vol. 66, no. 9, pp. 3718-3725, September 2019, doi: 10.1109/TED.2019.2931090.
Co-authorship: 70 %, **(Quartile 1)**

D. Barri, P. Vacula, T. Grešl, V. Kotě, J. Jakovenko and J. Voves, “Precise Model of the Effective Threshold Voltage Changes in the DLS MOSFETs for Different Gate Angles Compared with the Measured Data.” ***IEEE Transactions on Electron Devices***, under review.
Co-authorship: 70 %, **(Quartile 1)**

P. Vacula, V. Kotě, **D. Barri**, M. Vacula, M. Husák, and J. Jakovenko, “Comparison of MOSFET Gate Waffle Patterns Based on Specific On-Resistance.“, ***Radioengineering***, vol. 28, no. 3, pp. 598-609, September 2019. doi: 0.13164/re.2019.0598
Co-authorship: 20 %, **(Quartile 3)**

A.1.2. Publications Excerpted by WoS

D. Barri, and J. Jakovenko, “Comparison of Measured Data Given by Automatized Measurement Methodology with the Analytical Expression of DLS MOSFET.” *in **IEEE Proceedings** of the 25th International Conference on Applied Electronics (AE) 2020*, Pilsen, Czech Republic, 8 September 2020, pp. 3-8, ISBN 978-80-261-0891-7, doi: 10.23919/AE.2019.8866997.
Co-authorship: 90 %

D. Barri, and J. Jakovenko, “Design and Optimization of an Active OTA-C Filter Based on STOHE Algorithm.” *in **IEEE Proceedings** of the 24th International Conference on Applied Electronics (AE) 2019*, Pilsen, Czech Republic, 10-11 September 2019, pp. 3-8, ISBN 978-80-261-0813-9, doi: 10.23919/AE.2019.8866997.
Co-authorship: 95 %

A.1.3. Other Publications

D. Barri, “Modeling of a Hump Effect Using a Three-Dimensional TCAD Device Simulator.” in *Proceedings of the International Student Scientific Conference Poster – 23/2019. 23rd International Student Conference on Electrical Engineering POSTER 2019*, ČVUT FEL, Technická 2, Praha 6, 2019-05-23, Praha: ČVUT FEL, Středisko vědecko-technických informací, 2019, pp. 61-64, 1. sv. ISBN 978-80-01-06581-5.
Co-authorship: 100 %

D. Barri, F. Gaetano, P. Vacula, V. Kote, J. Behounek, and J. Jakovenko, “Precise Layout Area Estimation of Analog/Mixed-Signal Circuits”, *in Proceedings of the Cadence User Conference 2019*, CDNLive EMEA – Munich, Gerrmany – May 6-8, May 2019.
Co-authorship: 80 %

D. Barri, “A Design of an Active OTA-C Filter Based on DESA Algorithm” in *Proceedings of the International Student Scientific Conference Poster – 22/2018, 22nd International Student Conference on Electrical Engineering POSTER 2018*, ČVUT FEL, Technická 2, Praha 6, 2019-05-23, Praha: ČVUT FEL, Středisko vědecko-technických informací, 2018, pp. 1-5, 1. sv. ISBN 978-80-01-06428-3.
Co-authorship: 100 %

P. Vacula, V. Kote, **D. Barri**, "Trench MOS Having Source with Waffle Patterns" in *Proceedings of the International Student Scientific Conference Poster – 22/2018, 22nd International Student Conference on Electrical Engineering POSTER 2018*, ČVUT FEL, Technická 2, Praha 6, 2019-05-23, Praha: ČVUT FEL, Středisko vědecko-technických informací, 2018, pp. 1-5, 1. sv. ISBN 978-80-01-06428-3.
Co-authorship: 20 %

D. Barri, and J. Jakovenko, "An Algorithm for Assessment IC Matched Structure with Respecting nth order Gradient Parameter Effects" in *IMAPS flash conference 2017,* Brno, 2017-11-09/2017-11-10, Brno: Brno University of Technology, FEEC, Department of Electrical Power Engineering, 2017, pp. 12-93, ISBN 978-80-214-5535-1.
Co-authorship: 75 %

A.2. Publications Not Related to the Topic of This Work

A.2.1. Publications in Impacted Journals

V. Kotě, P. Vacula, V. Molata, O. Veselý, O. Tláskal, **D. Barri**, J. Jakovenko, and M. Husák, “A true random number generator with time multiplexed sources of randomness,” *Radioengineering*, 2018, vol. 27, no. 3, pp 796-805, ISSN 1210-2512, doi: 10.13164/re.2018.0796
Co-authorship: 3 %, **(Quartile 3)**

Appendix B: Recognitions and Review

Review of regular article “The Autonomy of the Gains of the Diamond Layout Style for Analog MOSFETs at High-Temperatures Range and Different CMOS ICs Technology Nodes”, ***IEEE Transactions of Electron Devices***, 2020.

The best Ph.D. Oral Presentation Award, for the work “Modeling of a Hump Effect Using a Three-Dimensional TCAD Device Simulator.”, *Poster 2019 23rd International Student Conference on Electrical Engineering*, Poster 2019, Prague, Czech Republic, 2019.

Certificate of Participation for the contribution “Precise Layout Area Estimation of Analog/Mixed-Signal Circuits.” in CDNLive Cadence User Conference EMEA 2019, as speaker, Munich, Germany, May 6–9, 2019.

Review of diploma thesis “Area Allocation for Yield Optimization in Integrated Circuits”, National Taiwan University of Science and Technology, Department of Electronic and Computer Engineering and Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics, author Bc. Martin Košťál, Prague, 2019.

Certificate of Attendance in the internship of intensive course by Athens Network (Advanced Technology Higher Education Network) “MP/TUD01: Introduction into Finite Elements and Algorithm” at *Delft University of Technology organized in Paris*, Paris, France, November 17 – 23, 2018.