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F3

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Switching power supply for high output currents

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Declaration

I hereby declare that I have worked on this diploma thesis independently, and all the sources of information I have used have been listed in the bibliography.

In Prague, 1. May 2020

Abstract

This diploma thesis deals with the topic of switch-mode power supplies (SMPS) for high current outputs suitable for welding technology. The goal of this thesis is the design, construction, and measurements of the SMPS of previously selected topology with the use of SiC MOSFETs and the maximum power output of up to 4 kW, which will be used for electrode welding. The work describes the workflow of the design, including the construction and measurements itself. The theoretical presumptions have been verified on the constructed prototype. The outputs of this thesis provide the necessary means for replicating the designed converter.

Keywords: Electrode, Welding, SMPS, high current, SiC, MOSFET

Abstrakt

Tato diplomová práce se zabývá problematikou spínaných zdrojů (SMPS) pro vysoké výstupní proudy vhodné pro sváření techniku. Cílem této práce je navrhnout, postavit a změřit SMPS předem zvolené topologie s použitím SiC MOSFET a maximálním výstupním výkonem až 4 kW, který má sloužit pro elektrodové sváření. Práce popisuje průběh návrhu včetně stavby a měření. Teoretické předpoklady byly ověřeny na postaveném prototypu. Výstupy této práce poskytují potřebné dokumenty pro kopii navrženého měniče.

Klíčová slova: Elektrodové, sváření, SMPS, vysoký proud, SiC, MOSFET

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Chapter 1

Introduction

The goal of this thesis is to design, construct, and measure a functioning prototype of the inverter welding machine for electrode welding. We use the SiC MOSFETs as the primary side main switching elements to test their superior temperature and frequency properties when compared to Si MOSFETs or Si IGBTs. The electrode welding is the most common type of manual welding which works on the principle of a melting electrode, also known as shielded metal arc welding (SMAW) or manual metal arc welding (MMA or MMAW). The welding is carried out at the atmospheric pressure conditions without the presence of inert gases. This type of welding method is commonly used for small home repairs of light professional use. In recent years, the decreasing cost of semiconductor components has contributed to use of power electronics based solutions in welding. The use of high frequency transformers and switches makes these solutions very compact and relatively low cost. Chapter 2 contains the theoretical part of the thesis, including

Input voltage V_{IN}	185 - 265 V_{AC}
Maximum (no load) output voltage V_{OUT}	85 V
Maximum output current I_{OUT}	150 A
Maximum output power P_{outMAX}	4000 W
Switching frequency f_{SW}	100 kHz
Maximum output current ripple I_{ripple}	0.15 I_{OUT}

Table 1.1: Inverter parameters

the topologies suitable for use in welding, a brief comparison of the Si and SiC switching components and types of transistors. In the 3rd chapter, we are dealing with the design and construction of the SMPS itself and in the 4th chapter we present the results including the measurements.

Chapter 2

Theoretical part

2.1 The electrode welding principle

The welding machine works on the principle of an electric arc. The electric arc is a breakdown of a gas dielectric, which occurs after exceeding the dielectric strength (exceeding the maximum electric field strength) when the gas present becomes conductive. The breakdown voltage V_{BR} between the electrodes is a function of pressure, and the type of gas surrounding the electrodes. The current flow through a normally dielectric medium like, e.g., the air, produces plasma. The light emission in the visible spectrum, high current density, and very high temperature is characteristic for the electric arc in the gases at atmospheric pressure. The electric resistance R alongside the arc creates heat, which ionizes more molecules of gas where the temperature determines the degree of ionization of these molecules. The temperature is relatively homogenous throughout the atoms, molecules, and electrons.
The energy supplied to the electrons is distributed to the heavier particles through elastic collisions thanks to the electron's high mobility and concentration. The relation between the current and voltage of the arc is non-linear. (Credit:[3]) In welding machines for manual non-automatic welding, we most commonly use the constant current (CC) power sources. The reason behind this is the fact that the output voltage changes dramatically as a result of the change of length of the welding arc, and the constant current sources are able to supply relatively constant current even while the voltage fluctuates. Figure 2.2 displays the basic functional scheme of a welding machine. The cathode of the machine connects to the piece of metal being welded, and the anode is the welding electrode. The actual electrode rod is covered in

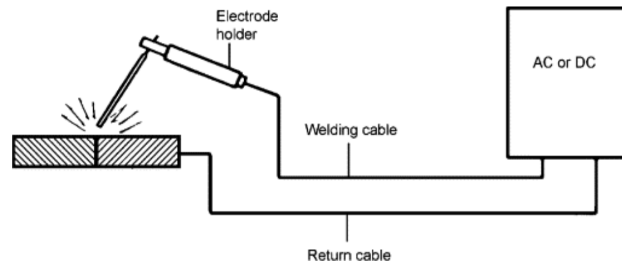


Figure 2.1: Welding principle diagram [26]

a thin layer of flux. When melted, the flux evaporates, e.g., in the form of carbon dioxide (CO_2) and isolates the weld from oxygen, hence improves the quality of the weld. The result of the molten metal coming into contact with air is the formation of oxides and nitrides, which results in lower strength of the weld. This principle is displayed in figure no. 2.2.

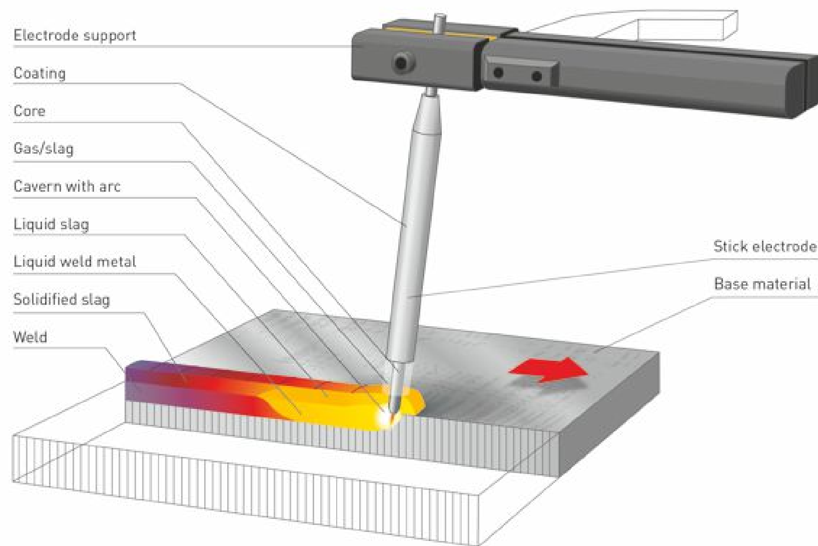


Figure 2.2: MMA welding process[25]

2.2 Most commonly used topologies

The input power comes from the AC network (185 V_{AC} - 265 V_{AC}). Therefore we are speaking of AC/DC conversion. Since that is the case, the power supply's essential function is to ensure the galvanic insulation of the welding ground from the mains. The reason behind this is that the welding ground is connected directly to the metal piece being welded, therefore posing a safety hazard.
In this chapter, we focus on a few of the most commonly used fully isolated SMPS topologies. There are some specific topologies, including resonant topologies operating at soft-switching mode and hard-switching mode operating topologies. The hard-switching topologies are the most commonly used due to their robustness and easy control scheme design based on the widespread pulse-width modulation (PWM) controllers. We focus solely on those and briefly talk about their features and principles.

- Half-bridge converter (HB)
- Full-bridge converter (FB)
- Forward converter (FC)

All of the above are very similar buck derived topologies. Therefore, we consider them one type. The topologies supply the energy to the load through a high-frequency transformer. The output stage is fully isolated, and there is a possibility of multiple isolated outputs.

2.2.1 Half bridge converter

The half-bridge is one of the topologies possibly used for the welding SMPS. This topology is very widely spread across the industry. Its basic functional schematic and waveforms are displayed in the figures 2.3 and 2.4. The switches Q_1 and Q_2 create a pulsed voltage across the primary of the transformer. The transformer steps down the voltage on the secondary through its ratio. This principle is the same for all topologies we are going to discuss. The capacitors C_3 and C_4 create a voltage divider, and for the steady-state operation, they are charged to the same voltage level, which is half of the V_{IN}. At the Q_1 turn-ON, the primary is connected between the V_{IN} and C_4, which means the voltage V_{C4} is present. Q_1 turns off before half of the

T_S, and the Q_2 won't turn on until the second half of the T_S. The deadtime between the activity of both switches shown in 2.4 is necessary to prevent the switches from cross-conducting. In this time, the body diode of Q_2 provides a way for the energy stored in the leakage inductance of the transformer to discharge. The capacitor C_B in series with the primary serves a blocking purpose of the DC magnetic flux in the core of the transformer.

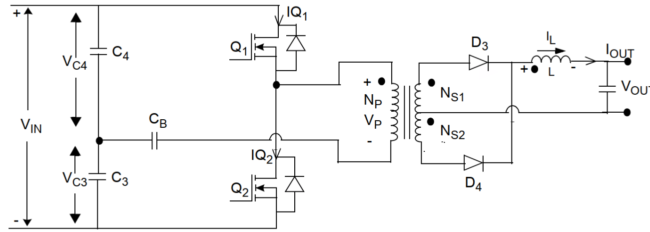


Figure 2.3: Half-bridge schematic [10]

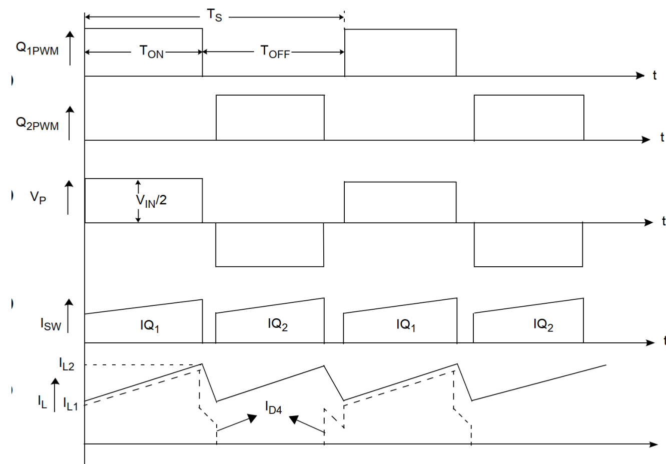


Figure 2.4: Half-bridge waveform [10]

In conclusion, this topology is usually used for output currents up to 250 A. The transformer use is very efficient resulting in the possibility of the use of a smaller transformer. Since the switching frequency is double on the output filter, it's possible to use a smaller sized inductor as well. There are two large capacitors needed across the switches, which increase the system's cost. The Miller induced turn-on of the MOSFETS also needs to be addressed. Still, probably the main drawback is the fact that the amplitude voltage of the transformer's windings is half of the input amplitude, reducing the output power capacity level and increasing the current stress on the switches significantly.

2.2.2 Full bridge converter

This topology and its general characteristics are very similar to the previous half-bridge converter topology, i.e., relatively small size transformer and output filter inductors. However, this converter eliminates the main drawback

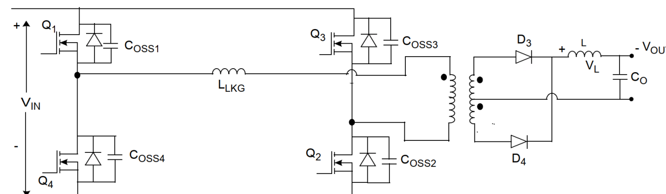


Figure 2.5: Full-bridge schematic [10]

of the half-bridge converter. The total input voltage is applied across the primary winding of the transformer, which means this topology can deliver double the power output compared to the half-bridge converters for the same current rated semiconductor switches. It is the reason why this converter topology is used for the highest power outputs with currents above 250 A. The apparent downside is the need for more semiconductor power switches as well as drivers and heatsinks, which translates to a bigger system, more complicated design, and higher cost. For more see [19].

2.2.3 Forward converter

We recognize the three following most common versions of the forward converter:

- Single switch forward (SSF)
- Double switch forward (DSF)
- Interleaved double switch forward (IDSF)

Single switch forward

The single switch forward topology is mostly used in low power applications (up to 500 W) and lower input DC voltage range. This version of

forward is popular in the United States thanks to their mains voltage being 120 V. As the input voltage V_{IN} is applied across the primary winding of the transformer at T_{on}, the current increases linearly from its initial value. The total current that flows through the winding is the magnetizing current I_M plus the inductor current I_L. When the switch turns off, there's no path for the current to dissipate the stored energy in the magnetic core. The most common way to dissipate this energy in single switch forward is through the use of reset winding N_R shown in figure 2.6.

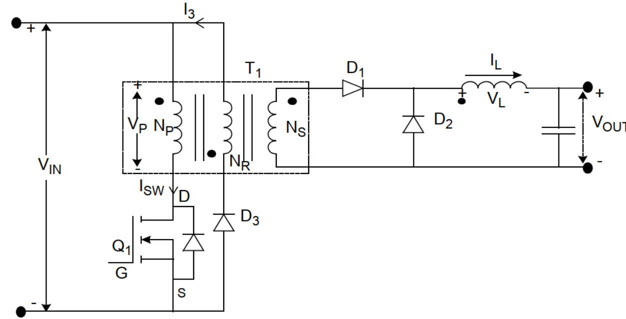


Figure 2.6: Single switch forward converter schematic [10]

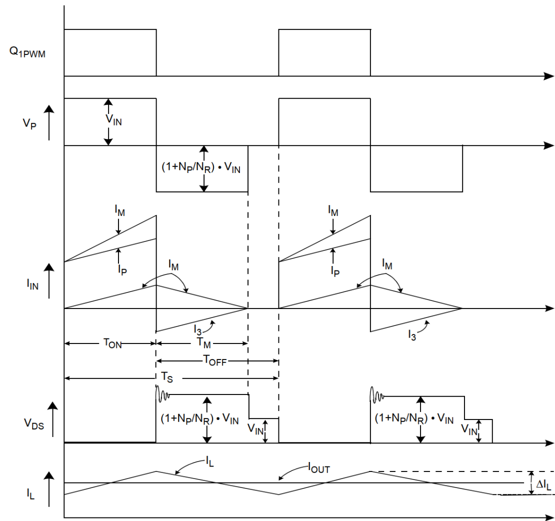


Figure 2.7: Single switch forward converter waveform [10]

Without the freewheeling diode D_3 the dot end of N_R would go very far negative and since the winding N_R and N_P usually consist of the same amount of turns, the non-dot end of N_P would go sufficiently positive to exceed the avalanche voltage of the transistor and destroy it. However, the diode D_3 is going to clamp the negative voltage spike of N_R. The voltage at the T_{off} is equal to $2V_{in}$ plus the leakage inductance spike as it is shown in figure 2.7.

For this reason, the use of single switch forward topology is discouraged for the input voltage of 230 V even though today's semiconductor switches can withstand high voltage levels.

Double switch forward

This topology works on the same principle as the single switch forward, just with some minor adjustments, which we will talk about below. In the figure 2.8 we can see the basic double switch circuit. The DSF is more

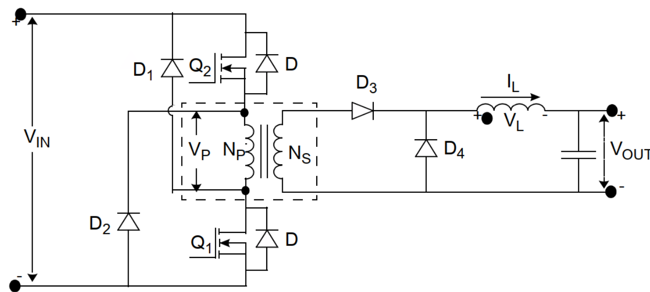


Figure 2.8: Double switch forward schematic [10]

suitable for our device since it contains two power switches. In this case, there's no reset winding used. As we can see in the figure 2.8, there are two freewheeling diodes making way for the energy stored in the transformer to be returned to the input V_{DC}(instead of being dissipated in a snubber circuit) as well as clamping the voltage spikes. The voltage across the switches will never be larger than the value of the input voltage V_{DC}. The main

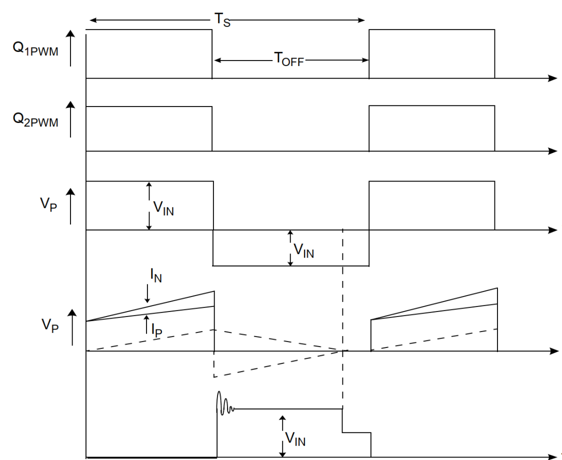


Figure 2.9: Double switch forward waveform [10]

difference between the DSF and HB topology is the fact that the transformer's

primary is in series with both switches, and they switch on and off in phase. The transformer's core needs to reset to the initial magnetic flux density $\vec{B}$ value in every cycle to prevent the step saturation of the core, over current and its destruction. The following must apply:

$$0 < D \leq 0.5 \tag{2.1}$$

It is customary to introduce a safety margin from obvious reasons. Then the expression will be following:

$$0 < D \leq 0.45 \tag{2.2}$$

In our case this will be taken care of by the PWM controller itself. From the figure 2.9, we can see that the transformer works in discontinuous conduction mode (DCM). Since we are constructing a constant current source, it's obvious the output inductor has to work in CCM. We are assuming the efficiency of the converter to be $\eta = 0.85$. This is a very common value that will be used for the design, even though the maximum efficiency ambitions are higher. The following expressions for primary current, output power, and input voltage apply:

$$P_{OUT} = 0.85 P_{IN} \tag{2.3}$$

$$P_{IN} = 1.176 P_{OUT} \tag{2.4}$$

If the output current period is $0.9T/2$. Then:

$$I_{Avg} = 0.45 I_p \tag{2.5}$$

$$P_{IN} = 1.176 P_{OUT} = V_{DC}(0.45 I_p) \tag{2.6}$$

$$I_p = \frac{2.61 P_{OUT}}{V_{DC}} \tag{2.7}$$

This topology is probably the most frequently used for portable welding machines up to 200 A or up to 300 A in the interleaved version discussed in the section below. The topology is very robust, with a simple control scheme. There is no need for dead-time like it is in the HB and FB topologies. Therefore, there are no issues due to cross-conduction incidents. The main drawback of the topology is the fact that its duty cycle is always less than 50% resulting in a relatively large transformer.

Interleaved double switch forward converter

Interleaved topology is a cascade of DSF converters. The switches of the single DSFs switch in the opposite phase creating more pulses in one period (one for every DSF). The presence of more pulses should theoretically

decrease the current ripple on the output. Every converter supplies the proportional part of the power, therefore, we can reach much higher output power. From the equation 2.7 we get:

$$I_p = \frac{1.176P_{OUT}}{NV_{DC}}$$

Where N is the number of power stages and therefore, the I_p through each power switch is proportionally decreased. This fact should theoretically affect the intensity of electromagnetic interference (EMI) generated by the converter since the intensity of EMI is proportional to the peak current I_p, not the number of pulses. The result would be a converter with higher

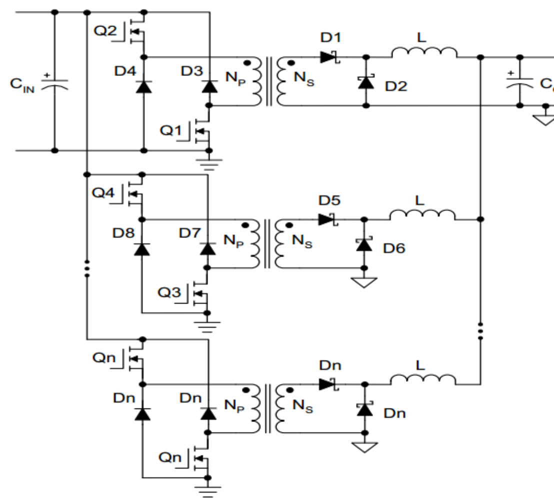


Figure 2.10: Interleaved DSF schematic [19]

output power capability and lower EMI compared to the DSF. The disadvantage is the complexity of the design and the high price. (Credits [19] and [13]).

In the end, the DSF topology has been chosen for its robustness, efficiency, and also the fact that the author has never encountered it before and has no previous experience with it was a contributing factor.

2.3 Semiconductor switches

In this section, we will focus on the main semiconductor switches commonly used in power applications and their essential parameters. The most commonly used semiconductor material for the manufacture of transistors is silicon (Si). In recent years other compounds like silicon-carbide (SiC) or galium-nitride (GaN) are starting to be more and more frequently used thanks

to their superior parameters and the advances in the semiconductor manufacturing technology. We mainly focus on MOSFET and IGBT technologies since these are the two most frequently used types of switches we can encounter in power electronics. Our power supply will be using switches made of SiC compound semiconductor.
The work on wide bandgap semiconductors such as SiC has been known for many years. Since the end of the 19th century, the synthetic form of SiC has been used widely through the cutting and grinding industry, mainly for its hardness. Their use in the electronic industry followed not long after. These compounds, such as SiC, GaAs, or GaN, are very exciting since they promise a substantial performance improvement over their Si-based competitors. The reason for this excitement is based on their ability to operate at higher power densities, higher voltages, higher frequencies, and higher temperatures.
As we characterize some material as being wide-bandgap, it refers to the energy required for an electron to jump from the top of the valence band to the bottom of the conduction band within the material. Semiconductors which require energies larger than 1-2 eV are considered wide-bandgap. The figure 2.11 below compares the material properties of Si, 4H-SiC and GaN semiconductors. These material properties have a direct influence on

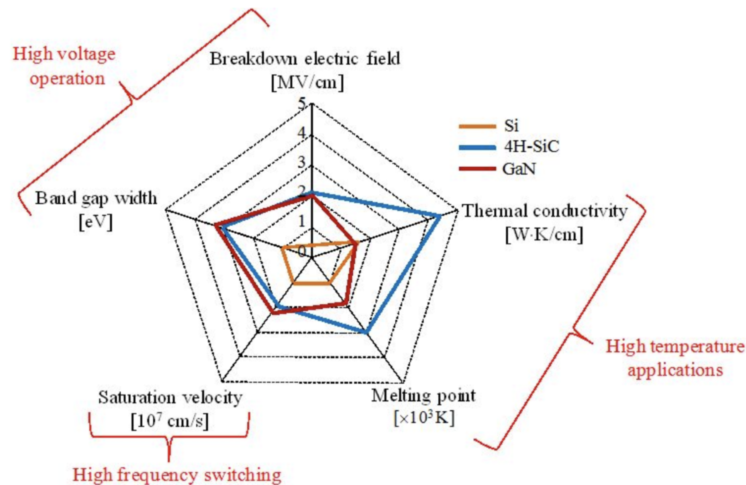


Figure 2.11: Semiconductor properties comparison [6]

the performance characteristics of the device. We can see that both SiC and GaN are superior to Si when it comes to RF and switching power devices. High breakdown voltage, together with wide bandgap, allows the SiC to work on higher voltages with lower leakage currents. Higher electron saturation velocity and electron mobility allow higher frequency operation, and the higher thermal conductivity makes the device superior when it comes to heat transfer efficiency. More can be found in [18].

2.3.1 IGBT

IGBT (Insulated gate bipolar transistor) is a technology used since the mid-1980s. It combines bipolar and unipolar technologies. Thanks to easy driving and low conduction losses, the IGBTs found their application in power electronics and have been dominating it for the past decades. As we can see in the figure 2.12, the IGBT consists of an N-channel MOSFET directly driving a wide base of a PNP BJT. The MOSFET provides a very high input

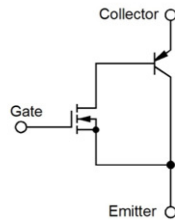


Figure 2.12: IGBT circuit

impedance and low input capacity since the gate surface is rather small, and the MOSFET drives the BJT with a small voltage drop in the saturation region. This way, IGBT combines the best features off both technologies. These advantages come at a cost. The main disadvantage of IGBT is its low switching speed capability coming as a result of higher losses caused by the tail current. At turn-off, it is possible to stop the flow of the ma-

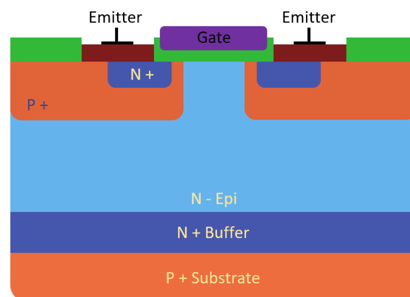


Figure 2.13: IGBT structure

jority carriers through the structure by lowering the gate-emitter voltage V_{GE} below the threshold voltage value V_T. The minority carriers, however, stay in the drift region and contribute to internal recombination current (beforehand mentioned tail current). Tail current flows until all the minority carriers are drained or recombined. Because the tail current is a collector current at a high voltage V_{CE}, it is a significant contributor to switching losses. The recombination speed can be affected by the insertion of a heavily doped layer (2.13), which will decrease the width of the space charge region (SCR). This layer quickly absorbs the left-over minority charge carriers.

The type of IGBT with this layer is called punch-through (PT), and the devices without this layer are called non-punch-throught (NPT). PT IGBTs have a significantly wider frequency bandwidth. For a parallel use, it is safer to use NPT type for its positive temperature coefficient (the current throughput of the switch decreases with an increase in temperature. This prevents current and temperature imbalance in the switches. PT IGBTs can be used in parallel, but it is not an ideal solution. More can be found in [19].

2.3.2 MOSFET

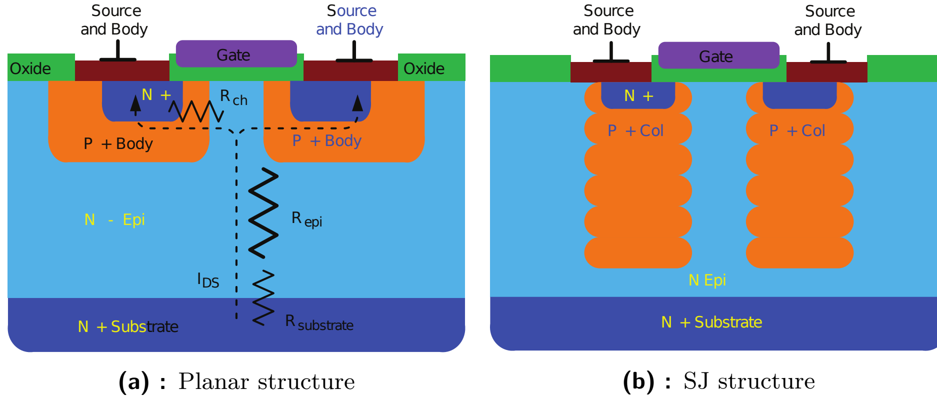
MOSFET technology went hand in hand with IGBT and has been the core of the industry standard for decades. Prior to the availability of super-junction MOSFETs, the dominant structure for high-voltage applications has been planar. The planar structure typically has relatively high on-state resistance $R_{DS(on)}$. The only way to decrease $R_{DS(on)}$ and with it related conduction losses is to increase the die size and increase the cell density. High cell density and die size results in larger input capacitances and input charge, increasing the switching losses and cost. Overall, the $R_{DS(on)}$ can be expressed as the following sum:

$$R_{DS(on)} = R_{ch} + R_{epi} + R_{sub} \tag{2.8}$$

Where:
R_{ch} is the induced channel resistance
R_{epi} is the epitaxial layer resistance
R_{sub} is the resistance of the substrate

For switches with low breakdown voltage, each component of the eq. 2.8 represents almost the same percentage of the final $R_{DS(on)}$. With the need for a higher voltage rating of the device, we must increase the thickness of the epitaxial layer, and the doping has to be lighter. If we double the breakdown voltage (V_{BR}), the area required to maintain the $R_{DS(on)}$ increases more then five-fold. For a 600 V rated MOSFET, more than 95% of the $R_{DS(on)}$ comes from the epitaxial layer. It is evident that for a significant $R_{DS(on)}$ reduction, it is necessary to find a way of heavy doping of the drift region and drastically reducing the resistance of the epitaxial layer.
Super-junction (SJ) structure MOSFETs has since its invention become the industrial standard. Figure 2.14b shows the structure of SJ MOSFET based on the idea of charge balancing. The drift region has multiple vertical highly doped P columns canceling the charge in the surrounding N region under reverse bias. As a result, the SJ MOSFET has a much thinner epitaxial layer, and it can be heavily doped for the same blocking voltage since the

structure offers much higher resistance to reverse voltage. As the N region becomes more heavily doped, the $R_{DS(on)}$ decreases. The doping of the N region (N_D+) also balances out the doping of the P region (N_A-). As a result of this relation between $R_{DS(on)}$ and the blocking voltage becomes linear. In comparison with the planar structure, the SJ structure disposes with much lower $R_{DS(on)}$ [8].

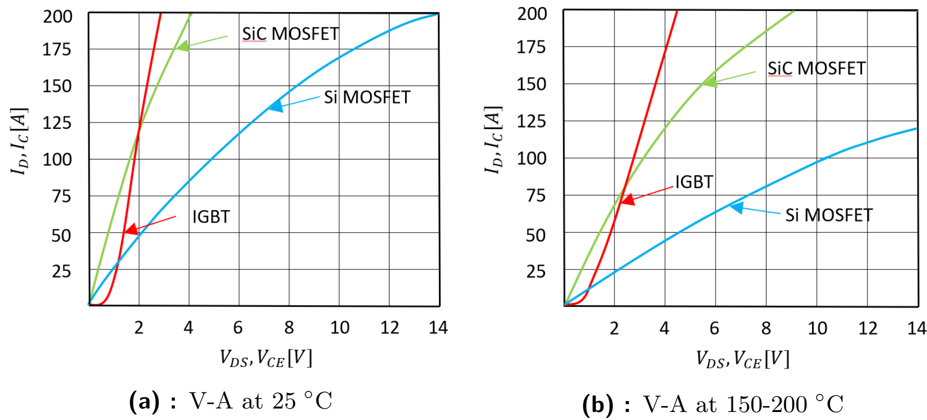


(a) : Planar structure **(b) :** SJ structure

Figure 2.14: Planar and superjunction structure of MOSFET [8]

The author took some time to make a comparison of three different components with similar power capability. The comparison is used only for the demonstration of the differences, not the actual choice of a component. The compared devices are following:

- ST's SCTW90N65G2V - 650 V, 90 A, 0.018 Ω, SiC power MOSFET
- IR's IPW65R048CFDA - 600 V, 63 A, 0.048 Ω, Si power MOSFET
- ST's STGW75M65DF2 - 650 V, 75 A, IGBT



(a) : V-A at 25 °C **(b) :** V-A at 150-200 °C

Figure 2.15: V-A characteristics comparison

From the characteristics, it is evident that SiC MOSFET yields superior $R_{DS(on)}$ at 25 °C and at high temperatures, the difference even increases. As mentioned before, thanks to SiC's higher thermal conductivity, the devices can work at temperatures reaching as high as 200 °C. Another area where SiC dominates is the low switching energy needed. It is advised to use $V_{GS} = 20$ V in SiC applications for achieving the lowest $R_{DS(on)}$ possible.

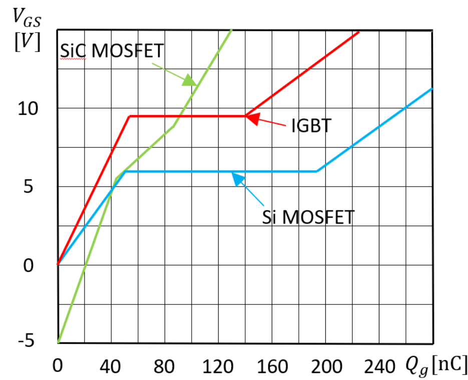


Figure 2.16: Gate charge

Thanks to the low gate charge needed, the high V_{GS} doesn't affect the driving power. We can see in figure 2.16 we can see that the Miller plateau is not as horizontal as we are used to with Si components. The SJ technology combined with the SiC compound semiconductor gives us a very fine tool for our application.

Chapter 3

Practical part

This chapter contains the practical design description of the hardware. The block schematic of the designed converter is shown in the picture 3.1. The energy flow happens from left to right, and the thick black arrow represents the high power path. Green paths represent digital signals, red paths analog signals, and blue arrows auxiliary power supply. The primary and

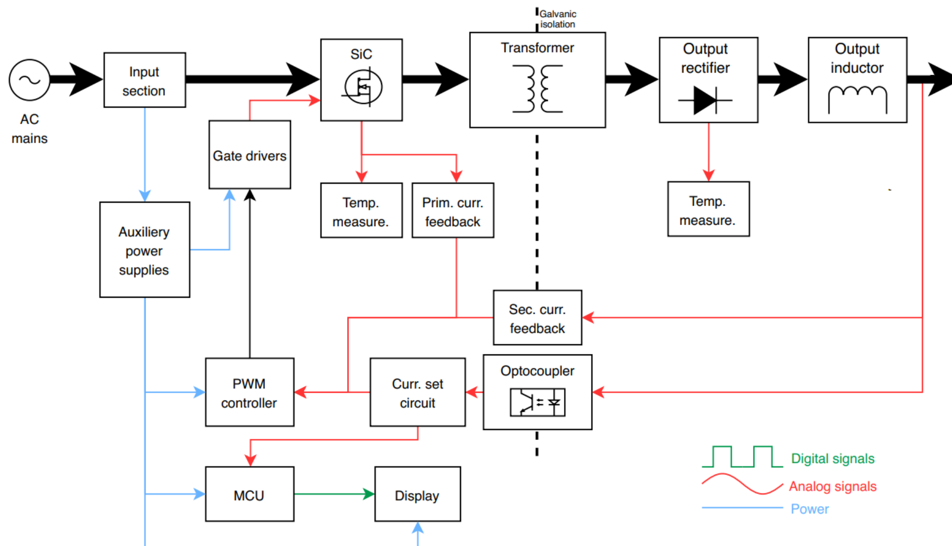


Figure 3.1: Converter block schematic

secondary sides are galvanically isolated. The transformer isolates the power path, and for the feedback signal isolation, we use an optocoupler. When it comes to the arrangement of the power components on the PCB, there are two main choices dependent on the package in use. If we go with the SMD version

(H^2PAK packages), the best solution would be to place the components on a ceramic plate attached to a heatsink, both located underneath the main PCB. This decreases the size of the PCB and the overall size of the device dramatically. The drawback of this solution is undoubtedly the thermal stress of the PCB at a lower air circulation underneath it. The author decided to evaluate the final overall parameters of the device using the solution based on TO-247 packages. Since there are no constraints when it comes to the size of the device, this solution seemed like the better choice (for the first version).

3.1 Input section

The converter input stage shown in figure 3.2 consists of an input header, start-up switch, the fuse, EMI filter consisting of capacitors and common-mode choke, inrush protective NTC, bridge rectifier, and bank of input capacitors. We use AC mains (185 V_{AC} - 265 V_{AC} range) on the input. Therefore, all the components have to possess sufficient current and voltage ratings. The standard-sized (e.g. 5x20 mm) 20 A rated fuse seems like the obvious option. A single inrush current limiting NTC with a value of $R = 1\ \Omega$ has been used.

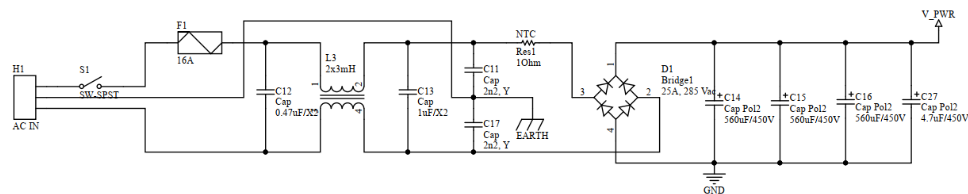


Figure 3.2: Input section circuit

Selecting at least a 10 Ω NTC would be preferred, but there are no NTCs with sufficient current and power rating available. A 1 Ω NTC is a solution used for welding devices with lower input capacitance(around 800 μF). We take into consideration the reactance of our common-mode choke and the input capacitors themselves in the calculation of the total amount of inrush current. Since this device is meant for evaluation purposes only, the author has decided to put this solution to the test. As expected, we can see in figure 3.3 that the inrush protection is not sufficient. The inrush current peak in figure reaches up to 150 A. This depends on where on the AC curve we turn on the device. A standard 16 A circuit breakers allow a peak current of around 165 A for up to 20 ms and a capacitive load of up to 3 mF. Not just that, there is a high probability that the device will trip the breaker, but also this amount of inrush current is not good for components in the input section from the long term perspective and will most likely decrease their life span noticeably. Therefore, this problem has been addressed by using a fixed value

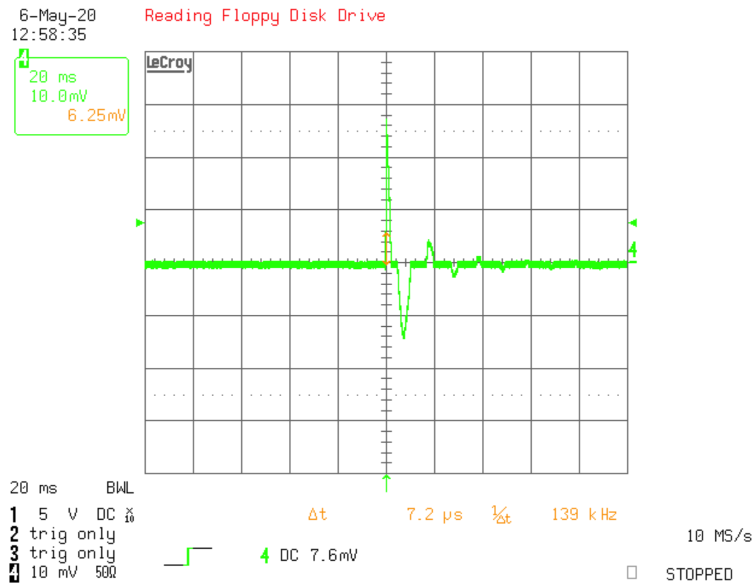


Figure 3.3: Inrush current with 1 Ω NTC [50 A/div]

resistor with a parallel relay instead of the NTC itself. The resistor damps the inrush peaks, and right after the relay bypasses it. The result displayed in figure 3.4. We can see that the current has been sufficiently damped and

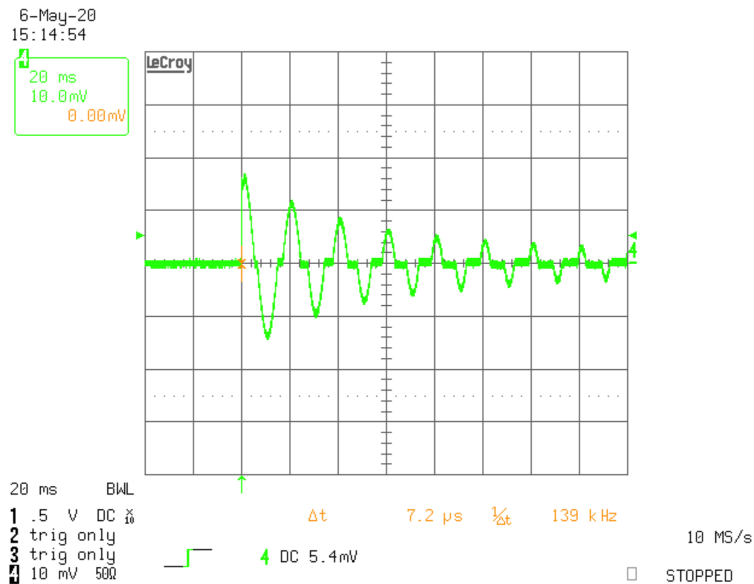


Figure 3.4: Inrush current with resistor and bypass relay [10 A/div]

the device will not trip any breakers.
The input capacitors are rated to 450 V since the 260 V_{AC} equals to amplitude of approx. 375 V_{DC}. Their capacitance has been calculated in a way that prevents the input voltage from dropping under 170 V_{DC} at converters full output power. This voltage lower limit seems reasonable. If we were to

choose a higher amplitude, larger or more capacitors would have to be used. That would unnecessarily increase the price and take more space on the PCB.

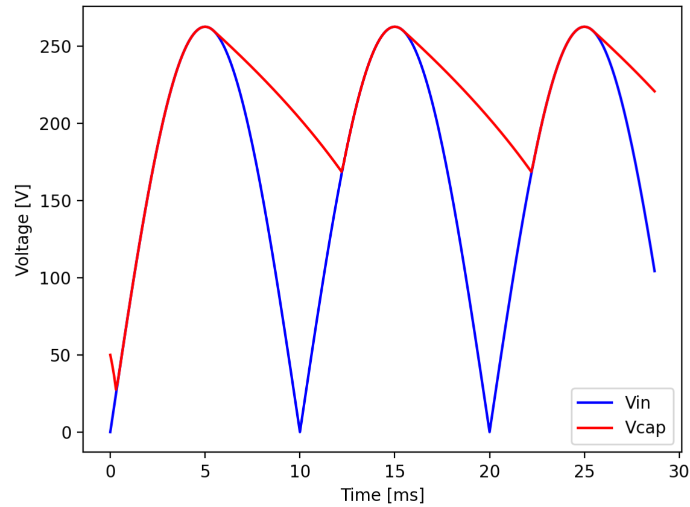


Figure 3.5: Rectified input voltage V_{IN} at maximum P_{OUT}

3.1.1 EMI filter

The problem with switching power supplies, in particular, is that the switching element creates very high dV/dt and dI/dt. The edges are extremely sharp, resulting in a very high harmonic content. This could cause an enormous amount of problems, and that's why various regulations are put in place to stop us from having such amounts of harmonics and force us to filter them out. There are two main types of noise we need to filter:

- Differential-mode noise (DM)
- Common-mode noise (CM)

In figure 3.6, we see the complete EMI filter circuit for both DM and CM noise. The DM current enters the SMPS through the phase (L) branch and exits through the neutral (N) branch and can be very easily filtered using the capacitor C_{X2} and both L_{DM} inductors from the figure 3.6. The CM currents enter the flow in the same direction through the L and N branches into the

SMPS and exit through capacitive coupling with protective earth (PE). On small frequencies, this coupling is not such a problem, but as the frequency increases, the currents increase with it. Therefore the CM is a problem at high frequencies. When we come to the design, we have to abide by the Middlebrook's stability criteria (established by prof. R.D. Middlebrook). What it tells us is that for the EMI filter not to interact with the SMPS control loop, the input impedance of the SMPS must be much higher than the output impedance of the filter itself. Measuring the input impedance

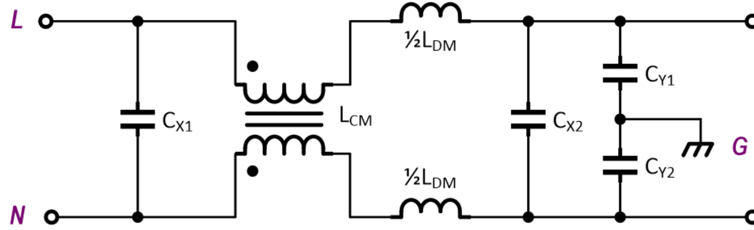


Figure 3.6: EMI filter circuit

Z_{IN} of the SMPS is not easily done since, for it to operate, it needs to have some capacitance on the input, and this capacitance is a part of the filter. We can estimate the impedance as follows:

$$Z_{IN} = \frac{V_{IN}^2 E_{ff}}{P_{OUT}} \tag{3.1}$$

The filters output impedance is calculated as follows:

$$Z_{OUT} = \sqrt{\frac{L}{C}}$$

The plasma arc responsible for metal arc welding can be modeled follows:

$$V_{ARC} = 20 + 0.04 \cdot I_{ARC} \tag{3.2}$$

Estimation obtained in [22]. V_{ARC} represents a peak voltage value across the arc. The expression 3.2 is necessary to calculate output power. In our case:

$$V_{ARC} = 20 + 0.04 \cdot 150 = 26\ V$$

Now we have all the values necessary for the impedance calculation.

$$Z_{IN} = \frac{375^2 \cdot 0.85}{150 \cdot 26} = 30.65\ \Omega \tag{3.3}$$

To abide by the Middlebrook's criteria, for the impedances will apply:

$$\frac{1}{10} Z_{IN} = Z_{OUT} \tag{3.4}$$

This way we are sure they won't interfere and it leaves us with:

$$Z_{OUTMAX} = 3.2\ \Omega$$

We use a reactance paper for calculating the values of the individual components. To do so, we need to establish our cut-off frequency f_{Coff}. Our converter's operating frequency is 100 kHz. There will be substantial noise at the 2nd and 3rd harmonics. We want to decrease that by about 40 dB. Therefore we choose our f_{Coff} one decade below the 3rd harmonic at 30 kHz. It is common to use CM choke's leakage inductance as the DM filters inductors to save components. The leakage inductance value is $L_L = 13.5\ \mu H$ in our case. Now we calculate the DM filters capacitors as follows:

$$f_{Coff} = \frac{1}{2\pi\sqrt{LC}} \tag{3.5}$$

The capacitor was in the end chosen to the value of 1 μF. Now we need to check whether or not there is a need for damping resistors. Damping resistor decreases the Q factor and thereby limits the ringing (impedance peak) at the resonance frequency. The Q factor is defined as follows:

$$Q = \frac{1}{R} \cdot \sqrt{\frac{L}{C}} \tag{3.6}$$

As shown in figure 3.2, there are three 560 uF capacitors on the input of the SMPS. Their total equivalent serial resistance (ESR) is around 80 mΩ. Therefore:

$$Q = \frac{1}{0.08} \cdot \sqrt{\frac{13,5 \cdot 10^{-6}}{1680 \cdot 10^{-6}}} = 1.12$$

We can see, there is no need for damping resistors. Finally we have to do is to determine the values of the CM capacitors. Typically the CM noise starts to appear around 5 to 7 MHz because the capacitance to chassis is quite low, and therefore the CM noise only appears on higher frequencies. If we assume 5 MHz and set the cut-off frequency 2 decades before, that leaves us with $f_{Coff} = 50kHz$. From there, we easily calculate the CM capacitor value as follows:

$$C = \frac{1}{4\pi^2 f^2 L_{CM}} = \frac{1}{4\pi^2 (50 \cdot 10^3)^2 3 \cdot 10^{-3}} = 3.37$$

In the end, two Y2 rated 2n2 capacitors were used. The last thing that needs to be mentioned here is the capacitor C_{X1} from figure 3.6. This component is a part of the DM filter. Its calculation is quite complicated and dependent on the input inductance of the source. The author used a simplified expression 3.7 and set the value on 0.47 uF.

$$\frac{1}{10\pi f_{SW}} < C_{X1} < \frac{C_{X2}}{5} \tag{3.7}$$

The EMI filter is a necessary part of the design, but the author is uncertain of the sufficiency in this case since the load is connected to the SMPS through long cables and our di/dt on them is quite substantial. We are not even talking about the fact that there's an arc at the end. (Credit [20].)

3.2 Forward transformer design

This section will cover the design of the power transformer for our forward based welding machine. The design of a power transformer is very much a multi-criteria problem. We are trying to keep the transformer's size at its minimum while keeping it from overheating due to the power throughput. The design is limited by the maximal temperature rise at the surface of the core.

$$\Delta T = R_{th} \cdot P_L \tag{3.8}$$

Where R_{th} is the thermal resistance (°C/W) and P_L power loss (W). In customer or industrial applications, a transformer temperature rise of 40-60°C may be acceptable, resulting in the maximal internal temperature of 100 °C. Losses are quite challenging to predict with accuracy, since the core loss data from the manufacturers are not always dependable, partly because measurements are made under sinusoidal drive conditions. In our case, we are dealing with a high-frequency rectangular-shaped waveform with high harmonics content. This fact makes the determination of eddy currents that much more difficult. The transformer losses should be examined under the worst-case conditions lasting over long periods of time, not under transient conditions. There are three major categories of losses:

- Core hysteresis losses
  They are a function of the frequency and flux swing. Under a fixed frequency operation, the flux swing is constant, and so are the losses regardless of changes in V_{IN} or output current.

- Core eddy current losses
  We can think of it as I^2R loss in the core material. If V_{IN} doubles, Peak I^2R loss quadruples, but since D is halved, average I^2R loss doubles. Thus core eddy current loss is proportional to V_{IN}. Therefore, the worst case is at high V_{IN}.

- Winding losses
  Consist of I^2R loss related to R_{DC} and frequency related loss R_{AC}. Due to the high-frequency operation, the proximity effect and the skin effect cause the current in the conductor to be unevenly distributed and increasing the effective resistivity. In our case, the R_{AC} is going to prevail. We use a Litz conductor to maintain a reasonable R_{AC}/R_{DC} and therefore make the skin and proximity effect related losses as low as possible.

The temperature rise is not only dependent on the losses but also on the thermal resistance, as shown in eq. 3.8. R_{th} has two components: internal

thermal resistance R_I between the heat sources and the transformer surface, and the external thermal resistance R_E from the surface to ambient air. We will mainly focus on R_E since most of the heat generated in the core is near the surface. Therefore the internal resistance is considerably smaller. The empirical equation used for R_{th} calculation with natural air convection (Credits [14]) is as follows:

$$R_{th} = R_E = 53 \cdot V_e^{-0.54} \tag{3.9}$$

There are two main approaches to design a transformer (using core geometry or area product). We will use the area product related calculations, because they seem the most logical and straightforward. First we will define the power supply parameters necessary for the design:

V_{IN} range	170 - 375 V
V_{OUT},I_{OUT}	26 V, 150 A
f_{SW}	100 kHz
Max. P_L	20 W
Max. temp. rise ΔT	60 °C
Cooling method	Forced convection

Table 3.1: Forward parameters

Now we should define the duty cycle limit D_{Lim} and normal duty cycle D_{Max} at low V_{IN}. The D_{Lim} is set by the topology to 0.5 and we will set $D_{Max} = 0.45$ to have a good reserve for dynamic response. Therefore:

$$V_{INmin} \cdot D_{Max} = 170 \cdot 0.45 = 76.5\ V$$

$$V_{INmax} \cdot D_{Lim} = 375 \cdot 0.5 = 187.5\ V$$

Now we calculate the maximal load output voltage plus the diode forward voltage drop using the equation 3.2:

$$V_{OUT} = 26 + 0.8 = 26.7\ V$$

With everything we know now, we can calculate the desired turns ratio n:

$$n = \frac{n_p}{n_s} = \frac{V_{INmin} \cdot D_{Max}}{V_{OUT}} = \frac{76.5}{26.7} \doteq 2.86 \tag{3.10}$$

3.2.1 Core selection

When it comes to selecting the right core, we have to decide on the material, shape, and the proper size.

Core shape

When choosing the shape of the core, its window configuration is essential. The window should be as broad as possible to minimize the number of winding layers. That results in lowering the R_{AC} related losses and leakage inductance. For the shape, three shapes have been considered. EE (EC, ETD), T (toroid), and planar. EE cores have a large window area in a reasonably wide configuration. Although after the full calculation of the transformer, including the necessary diameters of the windings, it was apparent it wouldn't be possible to manufacture it by hand or much larger core then needed would have to be used. Planar core would have to be manufactured by a third party, and since there was no available transformer in the catalog, it would have to be custom designed. That wouldn't just take a long time, but it also would be very costly for a small series. In the end, we were left with the toroid shaped core. It has the best possible shape from the magntic point of view since the magnetic flux path is completely enclosed in the structure. Its windings have to be uniformly distributed around the core. The winding area is very broad, resulting in minimizing the winding layers and getting the lowest possible leakage inductance.

Core material

When selecting the material, we need to take into consideration the switching frequency we work with. With power ferrites, the resistivity is higher with increasing frequency decreasing the eddy currents. The permeability is generally lower, causing higher magnetizing current and increasing the stress on the snubbers circuit. With metal alloy cores, the saturation flux density is higher, which is irrelevant in our case because the losses will limit the flux swing.
In our case, the author chose a CF139 (N87,3C94) power ferrite. It is one of the most commonly used power ferrites thanks to its possible use up to 300 kHz and low loss at high temperatures and high flux densities.

Core size

The core size selection is probably the most challenging part due to author's lack of experience in the transformer design. There are many variables in the estimation of the appropriate core size. The core power handling capability does not scale linearly with the area product or core volume.

Larger transformers must operate on lower power density since the volume producing heat increases faster than the core surface area that dissipates it. The following formula is used to estimate the area product needed:

$$AP = A_W A_E = \left(\frac{P_{OUT}}{K \cdot \Delta B \cdot f_{sw}}\right)^{\frac{4}{3}} [\text{cm}^4] \tag{3.11}$$

Where the coefficient $K = 0.014$ for the forward converter. This formula is also based on the current density $J = 4.2\ A/mm^2$ and the fill factor of 40%.

$$AP = \left(\frac{4005}{0.014 \cdot 0.15 \cdot 100 \cdot 10^3}\right)^{\frac{4}{3}} \doteq 50.95\ \text{cm}^4$$

After some elaboration the core T8530 was chosen. Its area product is larger, but it will be necessary to wind it by hand.

Core magnetic cross-section area - A_E:	3.42 cm^2
Core window area - A_W:	28.08 cm^2
Core volume - V_e:	77.71 cm^3
Area product - AP:	96.05 cm^4

Table 3.2: T8530 core parameters

Thermal resistance and loss limit

The core's datasheet doesn't contain the information about its R_{th}. We estimate it using eq. 3.9 and calculate the maximum power loss allowed.

$$R_{th} = 53 \cdot 77.71^{-0.54} = 5.05\ °\text{C/W}$$

$$P_L = \frac{\Delta T}{R_{th}} = \frac{60}{5.05} = 11.88\ \text{W} \tag{3.12}$$

The value in the eq. 3.12 applies for the natural air convection, which is not our case, therefore we rounded up to 20 W. Again, the author does not have much experience in this area, but 0.5 to 1% overall power loss seems like a reasonable assumption. The first version of the device will not function in an enclosed environment so we can evaluate the temperature stress. Let's temporarily split the power loss evenly between the core and windings.

$$P_{core} = P_{cu} = \frac{P_L}{2} = 10\ \text{W}$$

Magnetic flux swing

Knowing the maximum allowed power loss in the core, we are able to calculate the maximum power loss per cm^3:

$$P_v = \frac{P_{core}}{V_e} = \frac{10}{77.71} = 129 \text{ mW/cm}^3 \tag{3.13}$$

This value is compared with the graph in figure 3.7, which can be found in the ferrite manufacturers datasheet.

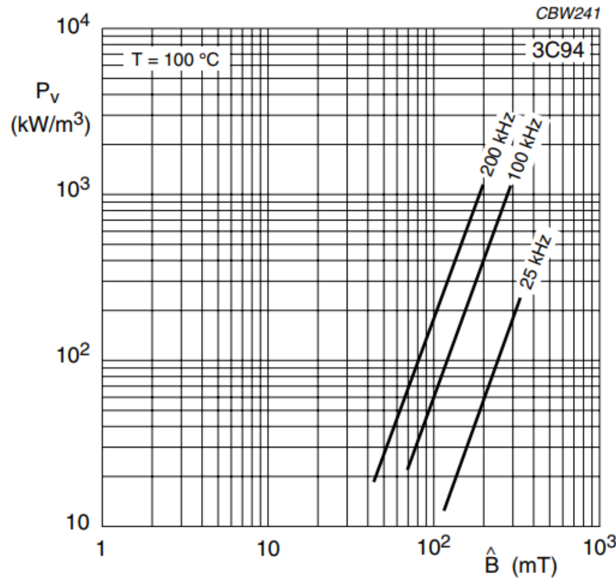


Figure 3.7: Core material power loss as function of peak flux density [1]

The maximum peak flux density is chosen at $\Delta B = 140$ mT.
Using Faraday's induction law, we can calculate the number of secondary turns:

$$n_s = \frac{V_{OUT} \cdot T}{\Delta B \cdot A_e} = \frac{V_{OUT} \cdot 1/f_{sw}}{\Delta B \cdot A_e} = \frac{26.7 \cdot 1 \cdot 10^{-5}}{0.14 \cdot 3.42 \cdot 10^{-4}} = 5.58 \tag{3.14}$$

The number of turns has to be a whole number. We can either round down, which will noticeably increase the volt/turn, flux swing, and thus core losses, or we can round up, which will increase winding loss. The decision was made to round up. Therefore:

$$\Delta B = 0.14 \cdot \frac{5.58 \ turns}{6 \ turns} \doteq 130 \text{ mT} \tag{3.15}$$

From the curve in figure 3.7, we get the final core loss P_v, which is 100 mW/cm^3 at $\Delta B = 130$ mT.

$$P_{core} = 0.1 \cdot 77.71 = 7.771 \text{ W}$$

Now let us calculate the primary turns, which finalizes our design when it comes to the core. We calculate the primary turns easily using the eq. 3.10.

$$n_p = n \cdot n_s = 2.86 \cdot 6 = 17.16 \approx 17 \text{ turns}$$

We recalculate the normal $V_{INmin}D_{Max}$ and ΔB under the worst case $V_{INmax}D_{Lim}$:

$$V_{INmin}D_{Max} = n \cdot V_{OUT} = \frac{17}{6} \cdot 26.7 = 75.65 \text{ V} \tag{3.16}$$

Therefore:

$$\Delta B_{max} = \Delta B \cdot \frac{V_{INmax}D_{Lim}}{V_{INmin}D_{Max}} = 0.13 \cdot \frac{187.5}{75.65} = 322 \text{ mT} \tag{3.17}$$

This value is satisfactory, and the core will avoid saturation since the manufacturer's datasheet states $B_{SAT} = 390$ mT.

3.2.2 Winding selection

We need to define the windings. The power loss in the windings is proportional to the load. Thus, the loss must be calculated at full load. At our frequency, the skin effect is substantial and has to be taken into consideration. The skin effect is a well-known phenomenon since the beginning of the 20th century and is caused by eddy currents induced in the conductor. The eddy currents in the center of the conductor flow in the opposite direction, and near the surface, they add to each other. Therefore, the current is being canceled in the center and is crowded in the outer skin. The skin depth is defined as the distance below the surface where the current density reaches value $1/e$ (or 37%) of its value on the surface. The relation between skin depth and frequency derivate for copper wire at 70°C is:

$$S = \frac{2837}{\sqrt{f}} \tag{3.18}$$

Where S is the skin depth in mils and f is frequency in Hz (Credit: [19]).

$$S = \frac{2837}{\sqrt{100 \cdot 10^3}} = 8.97 \text{ mils} \doteq 0.228 \text{ mm}$$

R_{DC} is defined as:

$$R_{DC} = \frac{\rho l}{A} = \frac{\rho l}{\pi \left(\frac{d}{2}\right)^2} \tag{3.19}$$

Where ρ is resistivity of the conductor, l is its length and A is the cross-section area. This tells us that with the increase in diameter, R_{DC} decreases. The R_{AC} is inversely proportional to the annular skin whose dept is S.

Thus as diameter increases, R_{AC} decreases. The use of Litz-wire with the same cross-section area yields much better R_{AC}/R_{DC} since the conducting annular skin total area increases. First we calculate the DC and AC rms current components through both windings (Credit: [7]):

$$I_{SecDC} = I_{OUT} \cdot D_{Max} = 150 \cdot 0.45 = 67.5 \text{ A} \tag{3.20}$$

$$I_{SecAC} = I_{SecDC} \cdot \left(\frac{1 - D_{Max}}{D_{Max}}\right)^{\frac{1}{2}} = 74.62 \text{ A} \tag{3.21}$$

$$I_{PrimDC} = \frac{I_{SecDC}}{n} = \frac{67.5}{2.86} = 23.6 \text{ A} \tag{3.22}$$

$$I_{PrimAC} = \frac{I_{SecAC}}{n} = \frac{74.62}{2.86} = 26.09 \text{ A} \tag{3.23}$$

When we know the currents through both windings, we can safely choose the wires. Since the primary benefit of the Litz conductor is the reduction of AC losses, the first consideration is the frequency of the design. The frequency determines not only the actual construction but also the individual wire gauge. The manufacturer recommended a single-wire diameter for 100 kHz applications which is equal to 0.1 mm (38 AWG). After the wire gauge has been determined, the ratio of R_{AC}/R_{DC} can be determined from the following formula:

$$\frac{R_{AC}}{R_{DC}} = H + K \cdot \left(\frac{N \cdot D_i}{D_o}\right)^2 \cdot G \tag{3.24}$$

Where H is a resistance ratio of individual isolated strands obtained from manufacturer's empirical data, N is the number of strands in the cable, K is constant depending on N (given by the manufacturer), and G is the eddy-current basis factor. G factor is calculated as:

$$G = \left(\frac{D_i\sqrt{f}}{10.44}\right)^4 = 0.00002155 \tag{3.25}$$

	Prim. winding	**Sec. winding**
AWG	10	1
Parallel	3	1
N	660	4500
D_i [cm]	0.1	0.1
D_o [cm]	0.26	0.7
R_{DC} [Ω/km]	3.6419	0.4692
R_{AC} [Ω/km]	4.6770	1.3355

Table 3.3: Transformer winding parameters

After some trying, the author finally came to the following solution for both

windings shown in table 3.3. Now we finalize the transformer designs with the calculation of the total power loss.

$$P_{Total} = P_{Core} + P_{Prim} + P_{Sec} = 7.77 + 3.76 + 11.49 = 23.02\ W \quad (3.26)$$

The transformer will dissipate approximately 23 W at full load conditions. Sadly the author wasn't able to manufacture such a transformer because purchasing an HF Litz-wire for a single transformer is near to impossible. Also the manufacturing a transformer with such parameters by hand would be very difficult. A purchased HF power transformer with sufficient parameters was used in the end, but the calculations were included since they are a significant part of the design.

Primary inductance - L_p:	97 mH
Secondary inductance - L_s:	5 mH
Leakage inductance - L_L	0.5 mH
Turns ratio - N:	45/10
Primary winding R_{DC}:	24 mΩ
Secondary winding R_{DC}:	1.42 mΩ

Table 3.4: Purchased transformer parameters

The author has not succeeded in finding out what material is used in the core of the purchased transformer. Therefore we are not able to calculate the core loss. The conduction losses of the purchased transformer will be much higher than our calculated transformer since it uses more turns of thinner solid copper wire on the primary and smaller diameter Litz wire with a larger diameter of the individual strands. As a result, the R_{AC}/R_{DC} ratio increases about 3-5 times. The transformer's power loss is estimated to about 65 W, and therefore the efficiency is estimated to be higher than 98 %. The output inductor section will calculate with the purchased transformer parameters. Credits for this section go to [7], [15] and [27].

3.3 Output inductor design

The design procedure of the output inductor is somewhat similar to the transformer's. With increasing frequency, the losses in the magnetic material increase significantly. However, the core power loss is dependent on the magnetic flux swing. Therefore, the loss is proportional to the change of output current ripple ΔI as shown in figure 3.8. Through the moderation of the ripple current, we moderate the losses.
First, we calculate the minimum duty cycle ratio:

$$D_{min} = \frac{V_{OUT}}{V_{INmax}} = \frac{26}{\frac{375}{4.5}} = 31.21\% \quad (3.27)$$

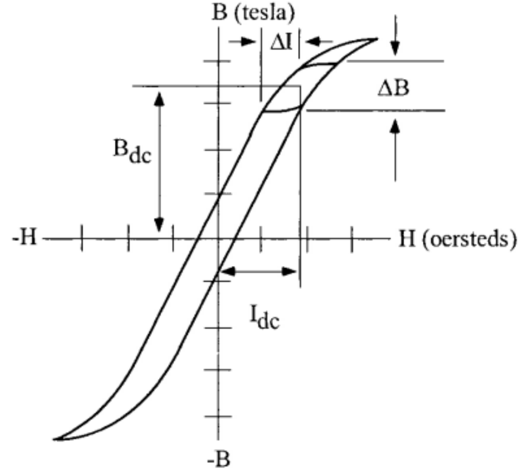


Figure 3.8: Typical output inductor BH loop [15]

To somewhat minimize the losses, we choose the ripple current $\Delta I = 0.15 I_{OUT}$. For this ripple, we calculate the minimum required inductance as follows:

$$L_{min} = \frac{T(V_{OUT} + V_f)(1 - D_{min})}{\Delta I} = 7.98\ \mu\text{H} \tag{3.28}$$

The output peak current will be $I_{pk} = I_{OUT} + \Delta I/2$. We need to calculate the energy-handling capability of the inductor, and from there, we proceed to the core choice of the core. The energy-handling capability is derived from:

$$E = \frac{LI^2}{2}[\text{W} \cdot \text{s}] \tag{3.29}$$

The energy-handling capability relation with AP is given by following equation:

$$AP = \frac{2E \cdot 10^4}{B_{max} \cdot J \cdot K} \tag{3.30}$$

For the window utilization factor $K = 0.4$, $B_{max} = 750$ mT and $J = 4.2$ A/mm^2:

$$AP = 16.85\ \text{cm}^4$$

Inductance decreases with increasing flux density B and magnetizing force H for various materials of different permeability values. The selection of the correct minimum permeability of the core is given by:

$$\Delta\mu = \frac{B_{max} \cdot MPL}{0.4 \cdot \pi \cdot W_a \cdot JK} = 29.5 \tag{3.31}$$

Where MPL is magnetic path length and W_a is the window area. A nanodust core T301-S-060A-BK was chosen:
Calculation of the turns is done through Al factor of the core:

$$N = \sqrt{\frac{L_{min}}{Al}} = 9.7 \doteq 10\ \text{turns} \tag{3.32}$$

Area product	Al factor	μ	Volume
41.41 cm^4	85 nH/N^2	60	45.3 cm^3

Table 3.5: Inductor core parameters

Now we can calculate the magnetic flux change B_{ac} in the core:

$$B_{ac} = \frac{0.4\pi \cdot N \left(\frac{\Delta I}{2}\right) \cdot \mu}{MPL} = 64.77\ \text{mT} \tag{3.33}$$

We recalculate the max for this core:

$$B_{max} = B_{dc} + \frac{B_{ac}}{2} = \frac{0.4\pi \cdot N \left(I_{OUT} + \frac{\Delta I}{2}\right) \cdot \mu}{MPL} = 780\ \text{mT} \tag{3.34}$$

We determine the thermal resistance of the core using eq. 3.9 and then, we can determine the total core loss and temperature rise using the core loss curves provided to us in the manufacturer's datasheet.

$$P_{Core} = 8.154\ \text{W}$$

$$\Delta T = R_{th} \cdot P_{Core} = 55.12\ ^{\circ}\text{C}$$

Usually, the same Litz conductor would be used as for the transformers secondary winding. However, since the author couldn't get any conductor, it had to be made by hand in ST's power lab in Prague. A Litz conductor used for the winding comes from an induction heater. The final DC resistance was measured with a result of 1.88 Ω/km which is quite a lot. The final conductor is isolated using silicone insulation with fiberglass providing insulation up to 4 kV. The Litz wire's parameters are following:

AWG	Parallel	N	D_i [cm]	D_o [cm]	R_{DC}[Ω/km]	l[m]
13	6	40	0.3	0.46	1.88	1.25

Table 3.6: Inductor winding parameters

As we can see, the core losses of the inductor are slightly higher than those of our calculated transformer. Even though the flux swing B_{ac} is much lower than in the transformer, the core losses are high. It is caused by the low core permeability(high magnetic reluctance). The conduction losses will be also higher due to the use of a Litz wire with fewer thicker strands. Credits [7], [15] and [17].

3.4 Auxiliary power supplies

There are multiple voltage levels necessary for the complete functionality of the welding SMPS circuitry. All the aux. power supplies with their output

voltages and power are listed in the table 3.7. The total power consumption estimate for all the peripheries is close to 8 W.

Type of supply	V_{OUT} [V]	P_{OUT} [W]
Non-isolated flyback	24 V	14
Isolated DC/DC	24 V	2
Buck	12 V	5
Linear	5 V	0.5
Linear	3.3 V	0.33

Table 3.7: Auxiliary supplies

3.4.1 Flyback converter design

As the AC/DC auxiliary supply, we used a non-isolated flyback converter based on an ST's VIPER26LD offline fixed-frequency controller and will operate in discontinuous conduction mode (DCM). When designing a flyback converter, it is good to start with the design of the coupled inductor since the power component ratings are bound to it. The turns ratio of the inductor defines the switches maximum V_{DS}, and output diodes reverse bias voltage. There are many ways to approach the calculations(e.g. [14]). In this case, the design of the inductor was done using software provided to the author by STM and the final parameters are displayed in the table 3.8. Also, the

	Material	Type	Gap	Al
Core:	CF 138	E20	0.3 mm	150 nH
	Inductance	**Turns**	**Wire**	
Primary:	3.9 mH	161	2x0.2 mm Litz	
Secondary:	66 μH	21	2x0.2 TIW	
Auxiliary:	42 μH	16	1x 0.1 Litz	

Table 3.8: Flyback coupled inductor

control loop compensation circuit was designed using ST's eDesign suite. The values of the individual components are displayed in the complete schematic of the flyback below.
The output diode maximum reverse bias voltage is calculated as follows:

$$V_D = V_{OUT} + \frac{V_{IN(MAX)}}{n} = 24 + \frac{375}{7.7} = \ 73 \text{ V} \tag{3.35}$$

It is necessary to use a fast diode on the output for efficiency reasons. ST's power Schottky diode series is rated up to 200 V. Since the maximum output

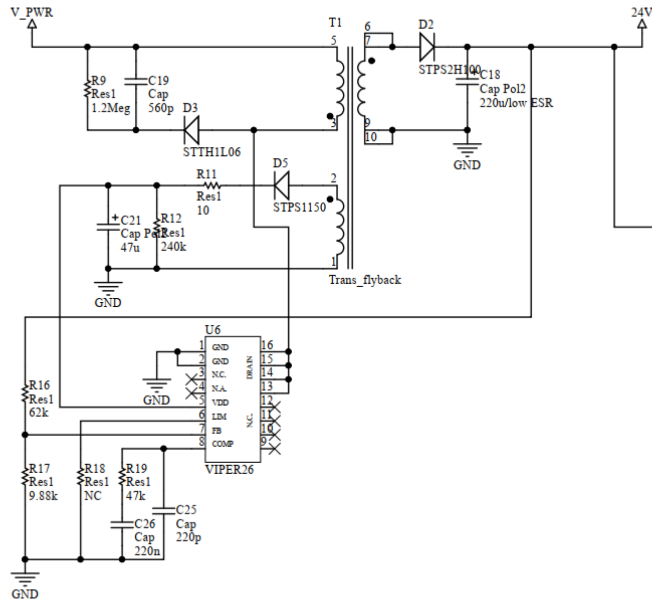


Figure 3.9: Non-isolated flyback circuit

current of the converter will be approx. 350 mA, the current rating is not an issue, and the STPS2H100 has been chosen.

For the MOSFET's voltage rating calculation, we have to take into consideration the leakage inductance on the inductor. Not all the magnetic flux generated by the primary penetrates the secondary winding (coupling factor < 1). From the circuit point of view, this creates one more inductor (L_L) put in series with the primary winding. L_L is charged with the primary winding but is not discharged into the load. Therefore, we need to discharge it into a snubber circuit consisting either or a parallel RC or TVS diode (transient-voltage-suppression diode, also called transil). From the efficiency and heat dissipation perspective L_L should be no more than 3% of L_P since the energy stored in L_L is dissipated as heat. The RCD snubber voltage can only be estimated since the leakage inductance can slightly vary. The following must apply for the overall MOSFET V_{DS}:

$$V_{DS} > V_{IN} + V_{Snubber} + V_{Reflected} \tag{3.36}$$

$$V_{DS} > 375 + 100 + (24 \cdot 7.7)$$

$$V_{DS} > 660 \text{ V}$$

The VIPER26 controller has an integrated MOSFET rated to 800 V. In the figure 3.10 at the turn-off of the MOSFET under light load conditions, we see quite a bit of oscillation. When the switch is ON, the current flows through the primary of the inductor. At the turn-off, an LC resonant circuit is formed by the inductor's L_L, the parasitic inductance of the traces, and transistor's internal drain-source capacitance (C_{DS}). Due to the presence of L_L and C_{DS}, a high frequency resonance takes place causing an excessive voltage stress

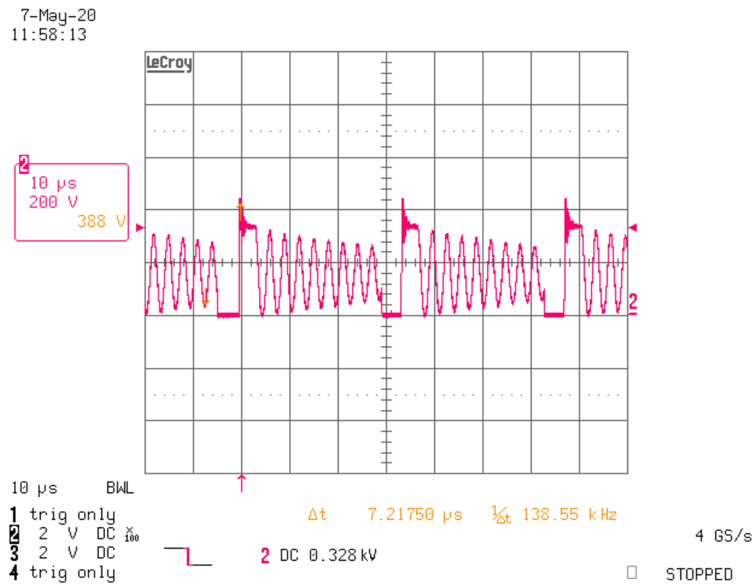


Figure 3.10: Flyback MOSFET V_{DS} waveform

on the MOSFET. As we can see in figure 3.11 the snubber circuit is already implemented, so the ringing is damped and acceptable. A further decrease of the ringing is possible through lowering the value of the snubber resistor or adding a gate resistor, thus decreasing dv/dt. However, both practices

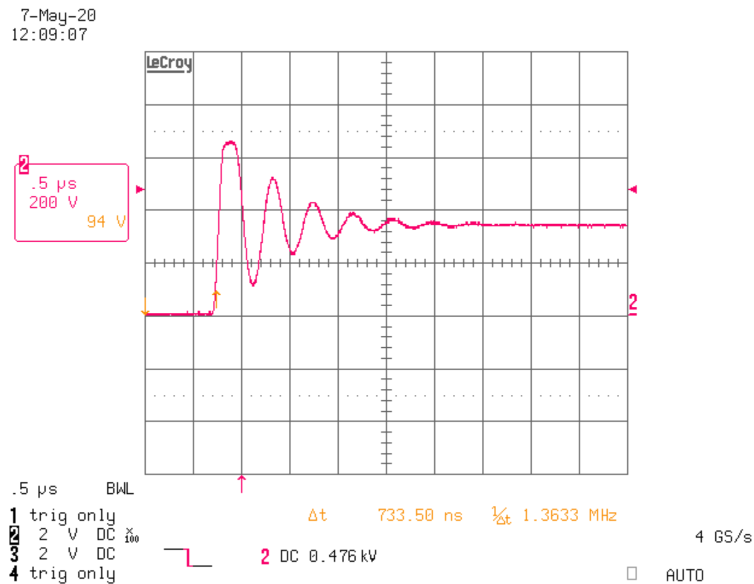


Figure 3.11: Voltage ringing at turn-ON

result in a decrease in overall efficiency. The author finds that lowering the ringing unnecessary since the voltage margin of the MOSFET is high enough. The secondary ringing visible on the waveform figure is caused by the leakage inductance of the coupled inductor. This ringing occurs when the current

through the secondary reaches zero. Credit [4]. The author also took some time to measure the flyback converter temperature at maximum output power to be sure it won't overheat while welding.

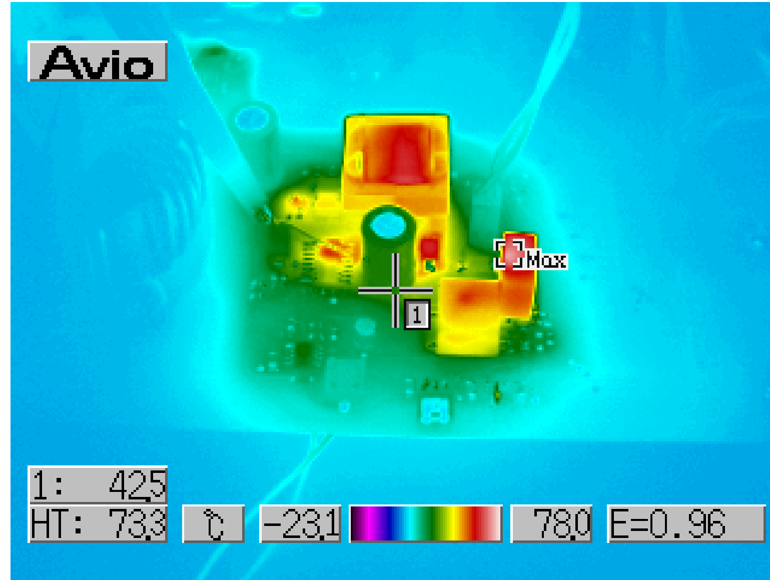


Figure 3.12: Flyback converter temperature measurement

The final temperature of under 75 °C at full load conditions (13 W) is satisfactory.

3.4.2 Buck converter

We use the 12 V supply branch for the majority of the control circuits. It is also used for powering the current transducer measuring the current on the output. The transducer secondary circuit is a current source outputting up to 100 mA. The ST's L6902 regulator operating in PWM mode at 250 kHz has been chosen. Its current output capability is 1 A. A 100 mΩ resistor is used to sense the current output, and the signal is fed back to the differential error amplifier (EA). Due to relatively low switching frequency, we are forced to choose a slightly larger inductor in exchange for better efficiency thanks to lower switching loss and MOSFET gate charge losses. The output inductor was calculated as follows:

$$L_{MIN} = \frac{V_{OUT} \cdot (V_{INmax} - V_{OUT})}{V_{INmax} \cdot f_{SW} \cdot K_{ind} \cdot I_{OUT}} = 327\ \mu\text{H} \tag{3.37}$$

Where K_{ind} is a coefficient representing inductor peak-to-peak current to the load. We chose $K_{ind} = 0.35$ and a 330 μH output inductor was used.

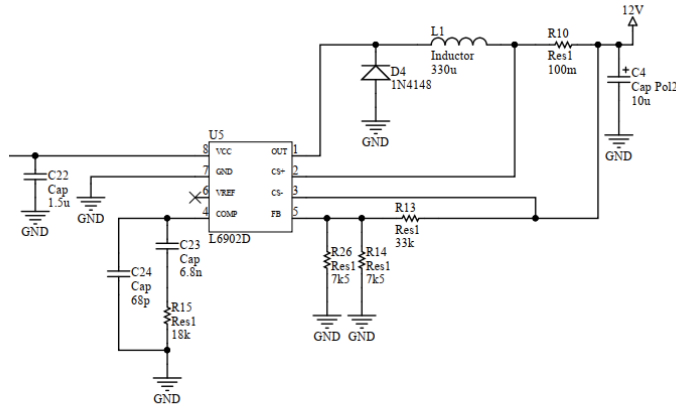


Figure 3.13: Buck converter schematic

3.4.3 Isolated DC/DC module

There are two isolated DC/DC power modules. Each module is responsible for powering one of the drivers in the half-bridge. It is essential for these modules to be able to supply enough power to the drivers at all times. The gate charge Q_g can be calculated by integrating the gate current over time.

$$Q_g = \int i_g dt$$

The energy E supplied to the gate in the turn-on period is:

$$E = \int V_g \cdot i_g dt$$

where, V_g is the modules supply voltage. Since the integral of V_g and i_g over time is $Q_g max$,

$$E = V_g \cdot Q_{gmax}$$

The energy E_g accumulated in the gate during the turn-on period is calculated as:

$$E_g = \int V_{gs} \cdot i_g dt = \int (V_g \cdot \frac{dQ_g}{dt} dt) = \int V_{gs} dQ_g$$

The average power consumption of the gate drive circuit P_g can be calculated by multiplying E by the switching frequency f_{SW}:

$$P_g = E \cdot f_{sw} = V_g \cdot Qgmax \cdot f_{sw} \tag{3.38}$$

$$P_g = 24 \cdot 162nC \cdot 100kHz = 0.39 \text{ W}$$

This brings us to the conclusion that 1 Watt modules are enough. The SIM1-2424 SIL4 modules have been used.
The 3.3 V and 5 V linear voltage regulators are used for powering the driver's primary side, LCD, and the MCU. Credit for this section goes to [5].

3.5 Control circuitry

The vast majority of the control circuitry is placed on a small PCB, which is connected to the mainboard as a module through board-to-board 2.54 mm pitch dual row header. In case of a layout error or new, improved version, only the small module has to be redesigned.

3.5.1 PWM controller

The ST's UC3845B fixed frequency current mode controller seems like the best option. An essential safety requirement was an internal duty cycle limitation to 50%. An external RC circuit connected to a precise reference easily sets the chip's oscillator frequency, which can go up to 500 kHz. We can access the controller's current sense comparator and both input and output of EA. This provides us with means for an easy primary and secondary current regulation.

3.5.2 Current control

The analog current control circuit is based on the TI's TS102/A chip. It includes two operational amplifiers, two comparators, and one voltage reference. There are two types of analog current control implemented in the welding machine:

- Primary
- Secondary

Primary current control

The primary control senses the primary peak current through a current sense transformer. This function serves a singular purpose of setting the duty cycle to zero if an overcurrent was to occur. The TRIAD's CST206-2A high-frequency current sense transformer was used. The transformer feeds

current to a shunt resistor shown in figure 3.14. The controller's current sense comparator senses the voltage over this resistor. The transformer has a

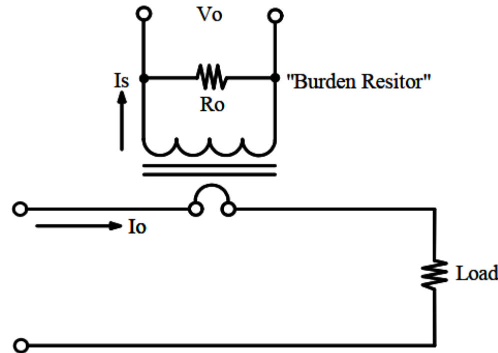


Figure 3.14: Current sense transformer circuit

1:200 turn ratio. The peak current through the primary will be up to 40 A at maximum load. The maximum allowed voltage at the input of the current sense comparator is 1-1.1 V. We have to take into consideration an approx. 10% error caused by the transformer temperature and frequency drift and the tolerance of the resistor. Therefore, to have some reserve, we set the maximum primary current to about 45 A. The resistor was chosen as follows:

$$I_{sec} = \frac{I_{prim}}{200} = \frac{45}{200} = 225 \text{ mA}$$

$$R_{shunt} = \frac{V_{shunt}}{I_{sec}} = \frac{1}{0.225} \doteq 4.44 \ \Omega$$

A 4.3 Ω resistor was used in this case.

Secondary current control

The secondary current regulation is carried out in a similar fashion. In this case, we use a potentiometer to set a reference voltage proportional to the feedback voltage induced by the desired output current. These two voltage levels are compared using op-amp U1C (for full schematic check the appendix figure A.8). The op-amp regulates the output of the PWM controller's internal EA through the diode D1 and therefore regulates the duty cycle of the controller. This time we used an active current transducer using Hall effect LEM LF 205-S creating a current feedback loop. Compared to the primary sense transformer, the transducer has superior accuracy when it comes to linearity and temperature drift. The recommended value for the shunt resistor is 68 Ω at the ambient temperature of 85°C. The conversion ratio of the transducer is 1:2000.

Control-loop compensation

The secondary control loop needs to be compensated. The purpose of the compensation of the error amplifier is to counter some of the gains of the control-to-output function that could cause instability of the power supply. The compensation network is placed in the Op-amp feedback as shown in figure 3.15 [12]. This compensation is generally known as type 2 compensation. Type 2 compensators are usually reserved for current-mode control compensation, or for converters that always operate in DCM. It is not an easy

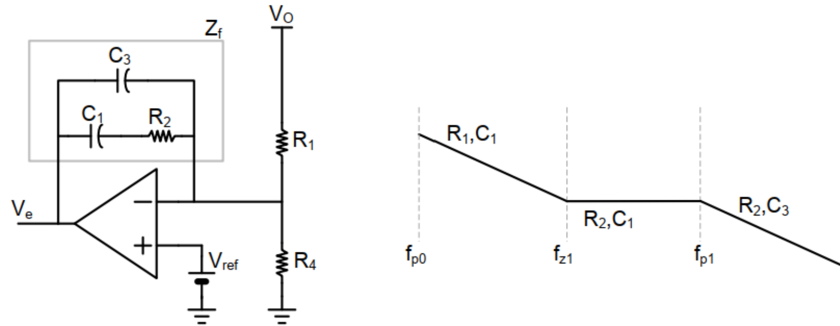


Figure 3.15: Op-amp compensation circuit [12]

task to simulate the control loop since we would have to make a precise model of transformer and others. Using this simple calculation, we can, at least to some degree, ensure the stability of the supply. The final values of the compensation circuit will be adjusted if instability was to occur. The simplified transfer function for the Op-amp loop is following [12]:

$$H(s) = \frac{\frac{\left(\frac{1}{sC_1}+R_2\right)\frac{1}{sC_3}}{\left(\frac{1}{sC_1}+R_2\right)+\frac{1}{sC_3}}}{R_1} \tag{3.39}$$

After some reconfiguration we are left with the desired transfer function:

$$H(s) = \frac{Z_f}{Z_i} = \frac{1 + C_1 R_2 s}{(C_3 + C_1)R_1 s + R_1 R_2 C_1 C_3 s^2} \tag{3.40}$$

The locations of the individual pole and zero are calculated as follows:

$$f_{p1} = \frac{1}{2\pi R_2 C_3}, f_{z1} = \frac{1}{2\pi R_2 C_1} \tag{3.41}$$

For the capacitors in the feedback should apply:

$$C_1 >> C_3$$

The common practice is to set the cross-over frequency somewhere from 1/10 to 1/5 of the f_{SW}.

Welding and short-circuit current

In the search for the most straightforward solution possible that would implement both the welding and short-circuit (SC) current setting, the author came across the solution displayed in figure 3.16 and 3.17(Credit: [21]).

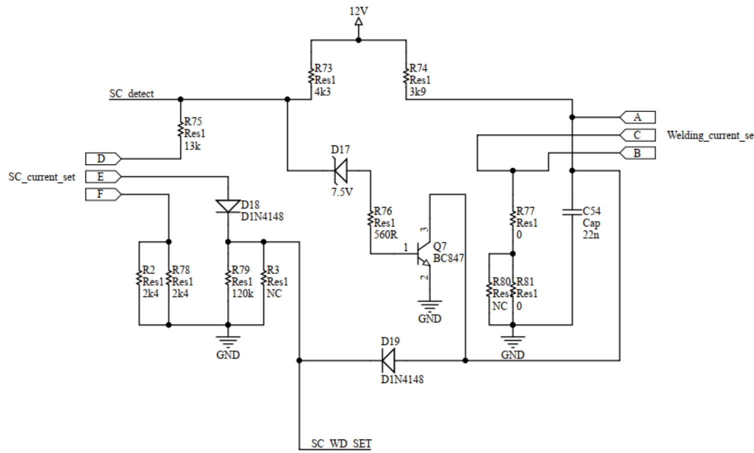


Figure 3.16: Welding and SC current setting circuit

There are two voltage dividers with potentiometers, each responsible for output current setting. The welding current is set at all times. In the case of SC condition on the output, which appears when the welding electrode touches the piece of metal being welded, the optocoupler on the output shown in figure 3.17 recognizes this condition causing the bipolar transistor Q_7 to turn-on and the SC voltage divider taking over as the reference for output current. The optocoupler circuit is designed so that its current consumption

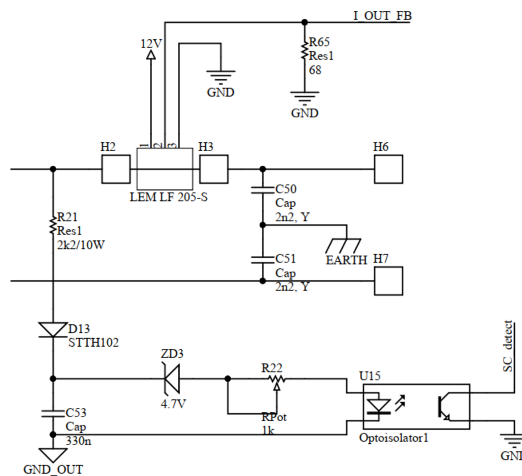


Figure 3.17: Output current measurement and short-circuit detection

is 25-40 mA depending on the transformer turns ratio used, but never higher.

The SC protection is an important feature preventing the welding electrode from sticking to the metal.

3.5.3 Thermal protection

The thermal protection is implemented for the MOSFETs and output diodes. We use two NTCs mechanically connected to the heatsinks of the mentioned components and creating a voltage divider. The divider is calculated so that all the components stay within the safe operating temperature ranges. The feedback signal is fed into a comparator with hysteresis shown in figure 3.18 that shuts down the output if the maximum set temperature is exceeded.

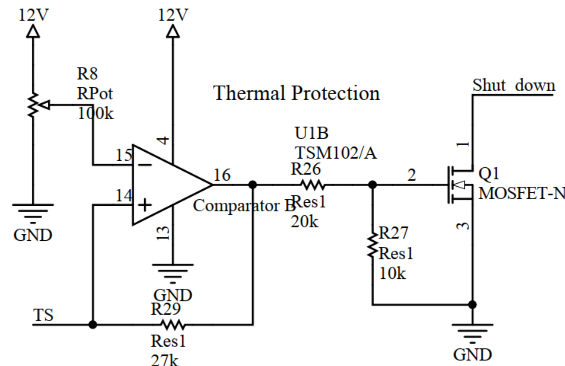


Figure 3.18: Thermal protection circuit

The general expression for reference voltage (V_R) in terms of input and output is:

$$V_R = \frac{V_{OUT} - V_{IN}}{R_1 + R_2} R_1 + V_{IN} \tag{3.42}$$

We rearrange for the input voltage:

$$V_{IN} = \frac{V_R(R_1 + R_2)}{R_2} - \frac{V_{OUT} R_1}{R_2}$$

From this, we determine the input voltage so that the reference voltage is equal to the positive power terminal of the comparator for both output states. These values are the low (V_{TL}) and high (V_{TH}) voltages of the hysteresis curve. Therefore:

$$V_{TL} = \frac{V_R(R_1 + R_2)}{R_2} - \frac{V_{CC} R_1}{R_2} \tag{3.43}$$

$$V_{TH} = \frac{V_R(R_1 + R_2)}{R_2} - \frac{V_{SS} R_1}{R_2} \tag{3.44}$$

Given these two expressions above, we can express one threshold voltage through the other:

$$V_{TH} = V_{TL} + \frac{(V_{CC} - V_{SS})R_1}{R_2} \tag{3.45}$$

From there we can express the resistor ratio:

$$\frac{R_1}{R_2} = \frac{V_{TH} - V_{TL}}{V_{CC} - V_{SS}} \tag{3.46}$$

And finally the reference voltage can be expressed as:

$$V_R = \frac{V_{TH}R_2 - V_{TL}R_1}{R_1 + R_2}$$

The high threshold $V_{TH} = 9.4\ V$ is determined by the maximum allowed temperatures. We set the low threshold voltage to half to allow the welding machine to cool down before put back to work. The resistor ratio is calculated using eq. 3.46.

$$\frac{R_2}{R_1} = 2.7 \Rightarrow R_1 = 10\ \mathrm{k}\Omega, \mathrm{R}_2 = 27\ \mathrm{k}\Omega,$$

The reference voltage will be set to $V_R = 6.8$ V. Credit [9].

3.6 Power components

The author picked the ST's SCTW100N65G2AG SiC MOSFETs [24] as the main switches in the forward converter. The parameters of the chosen transistors are shown in table 3.9.

Maximum V_{DS}	650 V
Maximum RMS current $I_D(100°C)$	70 A
Package of the component	TO-247
Maximum junction temperature T_j	200°C
Maximum on-resistance $R_{DSon}(200°C)$	30 mΩ
Thermal resistance junction-case R_{thj-c}	0.42 °C/W

Table 3.9: Paramteres of SCTW100N65G2AG

Thanks to the transistor's high current and thermal capability, we are able to avoid paralleling. For the functionality at the full intended power output, the author chose ST's STPS80170C[23] Schottky diodes. After the author

Maximum reverse voltage V_{RRM}	170 V
Maximum average current $I_F(150°C)$	2x40 A
Package of the component	TO-247
Maximum junction temperature T_j	175°C
Maximum forward voltage drop $V_F(125°C)$	0.74 V
Thermal resistance junction-case R_{thj-c}	0.5 °C/W

Table 3.10: Paramteres of STPS80170C

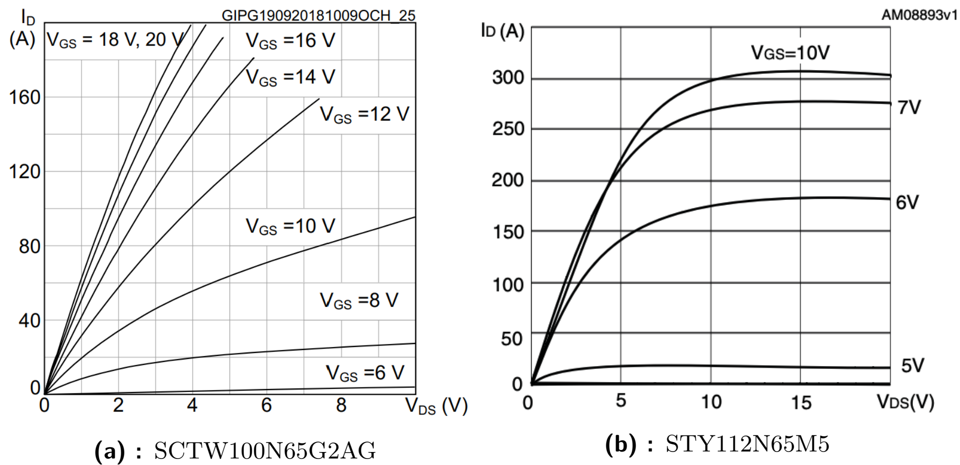
found out, it won't be possible to measure the full current output range of the welding machine, the decision was made to use the STPS60SM200C diodes instead.

Maximum reverse voltage V_{RRM}	200 V
Maximum average current $I_F(150°C)$	2x30 A
Package of the component	TO-247
Maximum junction temperature T_j	175°C
Maximum forward voltage drop $V_F(125°C)$	0.7 V
Thermal resistance junction-case R_{thj-c}	0.5 °C/W

Table 3.11: Paramteres of STPS60SM200C

3.7 Gate driving

When it comes to driving SiC MOSFETs, we need to take into consideration its gradual transconductance. It is causing the transfer from the ohmic to the saturation region to be not so well defined. We need to consider this in our application. For switching purposes, the ohmic region is the only possible mode of operation. It is evident from figure 3.19b that a slightly lower driving



(a) : SCTW100N65G2AG

(b) : STY112N65M5

Figure 3.19: Output characteristics of SiC and Si devices

voltage is not a problem for Si components since the curves for 10 V and 7 V are practically identical for the whole operation area of the device. The SiC devices are more sensitive to V_{GS}. From figure 3.19a, we can see that a decrease in V_{GS} from 20 V to 16 V causes a significant increase in R_{DSon}.

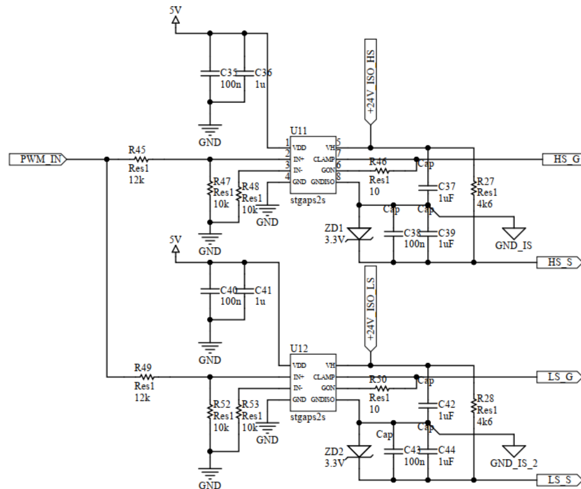


Figure 3.20: Driver circuits STGAP2S

In our application, we use +20 V, -3 V driving voltages. The negative driving

ensures a very fast turn-off. The maximum driving voltage of Si components is usually at least double the actual driving voltage. With SiC components, more precise driving is required since there's only a 10% reserve before the component is destroyed. There are two main ways to drive SiC transistors. One is using a gate drive transformer based circuit, and another one is using an isolated gate driver IC. The solution including the driving transformer offers very good parameters if designed well. The author chose a isolated gate-driver-based solution from figure 3.20 solely for time-saving reasons. STGAP2S is a single gate driver IC with isolation up to 1700 V. The driver has 4 A driving capability with up to 26 V rail-to-rail output and negative driving capability, making it ideal for driving SiC switches in our application. The active Miller clamp dedicated pin and thermal shutdown are also present.

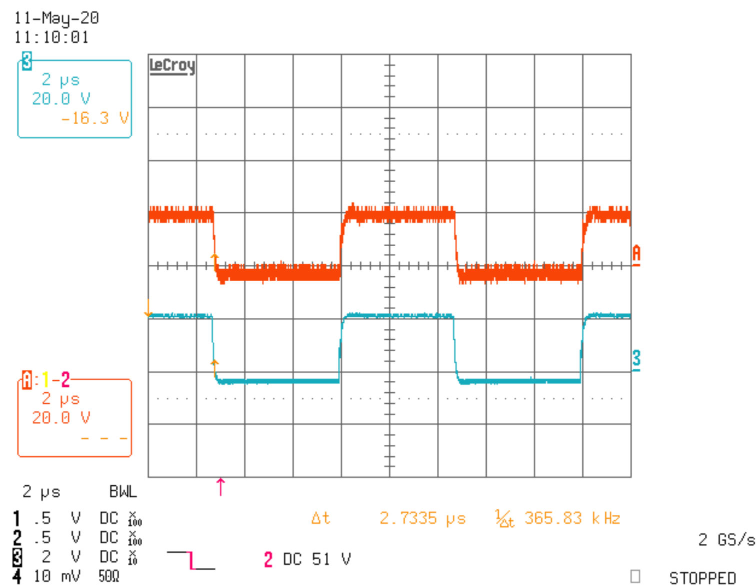


Figure 3.21: Driver output (no-load conditions)

From figure 3.21, we can see that the driving signals are in perfect alignment with each other and the negative driving is functional. The author had no access to a differential sonde. Therefore, the high side gate waveform has been measured with two different channels and plotted as an arithmetical difference on the oscilloscope.

3.8 Heatsink design

In this section, we will choose suitable heatsinks for the semiconductor components in our application. To be able to pick the adequate heatsink, we need to calculate the power loss in these devices. We begin with the power switches since that's where the most heat is dissipated. There are several loss components when it comes to MOSFETS.

- Conduction loss
- Switching loss
- Gate charge loss

We neglect the gate charge loss in this case. Conduction loss is the majority loss in our application, and it is a resistive loss caused by the $R_{DS(on)}$ of the channel. The calculation is for the worst possible conditions (full load). At full load, the device's junction temperature needs to be no more than 170°C. From the datasheet we know the value of $R_{DS(on)}(170°C) \doteq 31.5\ m\Omega$. Then:

$$P_{Con} = I_{RMS}^2 \cdot R_{DS(on)} = 35 \text{ W} \tag{3.47}$$

The MOSFET's switching time and with it related switching power loss estimated from datasheet parameters hardly ever match the results shown by an oscilloscope. This is due to the difference between measurement and application conditions. From ST's measurements of the SiC devices, we know the device is capable of $dV/dt = 60V/nS$ with the STGAP driver. This value will be used in the calculation of the switching losses. The following equation derived in [16] has been used to calculate the switching loss:

$$P_{SW} = \frac{1}{2} V_{IN} I_D (t_{SWon} + t_{SWoff}) f_{sw} \tag{3.48}$$

$$P_{SW} = \frac{1}{2} 375 \cdot 33.3(6.25 + 6.25) \cdot 10^{-9} \cdot 100 \cdot 10^3 = 7.8 \text{ W}$$

The overall power loss of one transistor is approx. 43 W. Now we proceed to the power loss of the output diodes. At full load, the diode's junction temperature needs to be no more than 150°C. The power loss on the output diodes is calculated as follows:

$$P_D = V_F I_F = 0.74 \cdot 150 = 111 \text{ W} \tag{3.49}$$

Therefore, the power loss of one package is approx. 28 W. Now, we can determine the heatsink. The common practice is to describe the heat dissipation

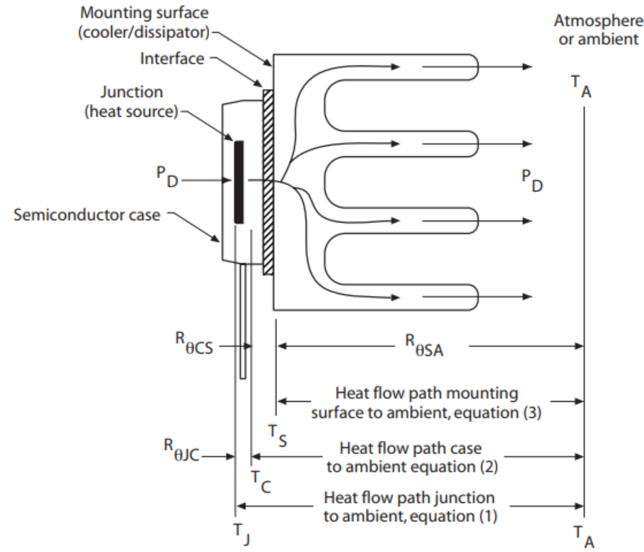


Figure 3.22: Heatsink heat flow path [2]

system as a network of resistors in series representing the individual thermal resistances.
The basic equation for heat transfer can be stated as follows:

$$P_D = \frac{\Delta T}{\sum R_\theta} = \frac{T_J - T_A}{R_{\theta JC} R_{\theta CS} R_{\theta SA}} \tag{3.50}$$

Where:
P_D - the dissipated power in watts
ΔT - temperature rise of the device's junction
$R_{\theta JC}$ - thermal resistance from junction to case of the semiconductor device
$R_{\theta CS}$ - thermal resistance through the interface between the device and the surface it is mounted on (heatsink)
$R_{\theta SA}$ - thermal resistance from the heatsink to ambient air (equal to the heatsink resistance)
The equation 3.50 is illustrated in figure 3.22. A Kapton tape thermal pad with thermal grease is used with both diodes and transistors, making the $R_{\theta CS} = 0.15\ °C/W$. A 0SA36:50:B heatsinks from Aavid Thermalloy have been chosen for our application. The thermal resistance for our type of heatsink (150 mm long) at air speed of 2 m/s was provided as follows:

$$R_{thn(150\ mm)} = R_{\theta SA} \cdot R_{thf} = 0.93 \cdot 0.312 = 0.29\ °C/W \tag{3.51}$$

Where:
R_{thn} is the final thermal resistance of the heatsink
R_{thf} is the coefficient of forced air speed [m/s]
From graphs of thermal performance ($R_{\theta SA}$ vs. length) provided by the manufacturer, we get the value of $R_{\theta SA}$ for our 50 mm long heatsinks.

$$R_{\theta SA} = 0.93 \cdot 2.15 \doteq 2\ °C/W$$

The heatsink would be insufficient at natural convection of the air. Therefore, we have chosen a small fan (EBM's 614NM) to be mounted on the side of the heatsinks providing airflow at a maximum speed of 4.84 m/s. Through the airspeed correction factor R_{Cf} provided by the manufacturer, we calculate the final R_{thn}.

$$R_{thn(50\,mm)} = R_{\theta SA} \cdot R_{thf} \cdot R_{Cf} = 2 \cdot 0.312 \cdot 0.55 = 0.343\ °C/W$$

Now we can calculate the maximal junction temperatures of individual components at full load using eq. 3.50:

$$T_{j(MOSFET)} = 40 + (0.42 + 0.15 + 0.343) \cdot 43 \doteq 80\ °C$$

The author thinks that the actual temperature rise could exceed the estimated value by as much as 20% in the case of the transistors, because the estimations are based on the same air convection through, all the fins of the heatsink. Our fan has a smaller diameter than the heatsink. When it comes to the diodes, it is not so obvious what final temperature we should expect since the air going through the transistor heatsinks and transformer is used. Based on that, we doubled an ambient air temperature used for calculating the diode T_j.

$$T_{j(DIODE)} = 80 + (0.5 + 0.15 + 0.343) \cdot 56 \doteq 135.6\ °C$$

This way the calculated value should be closer to reality. The heatsinks should be sufficient for some reasonable work cycle even at full load. Since a transformer with a higher turn ratio was used in the end, the power loss on the MOSFETs is significantly lower than expected due to the smaller primary current. Therefore the heatsink might be oversized for them. In this case, the author made it possible to transfer the fan on the output diode heatsinks to lower their temperature stress. Credits [2] and [11].

3.8.1 Fan PWM drive

A PWM circuit driving the fan is based on NE555 (displayed in A.9). The output frequency of the circuit is fixed, and the potentiometer R60 sets the duty cycle. This circuit was used for its convenience and easy implementation. In the later versions, an MCU generated PWM would be implemented. Mainly for the possibility of easy duty cycle adjustment based on the temperature feedback.

3.9 PCB design

The author used Altium Designer 19 for the design of the whole device. There are many proximity restrictions when it comes to the design of the primary side power paths.

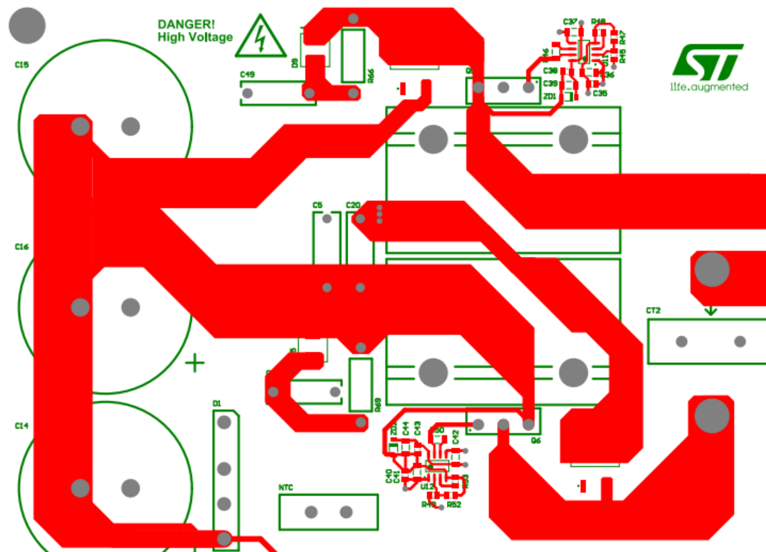


Figure 3.23: TOP-layer primary side power traces

The primary current loop needs to be as short as possible for noise reduction and proper functionality. The freewheeling diodes, snubber circuits, voltage spike suppressing folium capacitors, the input capacitors and the drivers need to be as close to the switches as possible for the same reason. The driver input signal traces should be of similar length to avoid introducing a phase shift between them. The traces of the input capacitors are in different layers to increase safety.

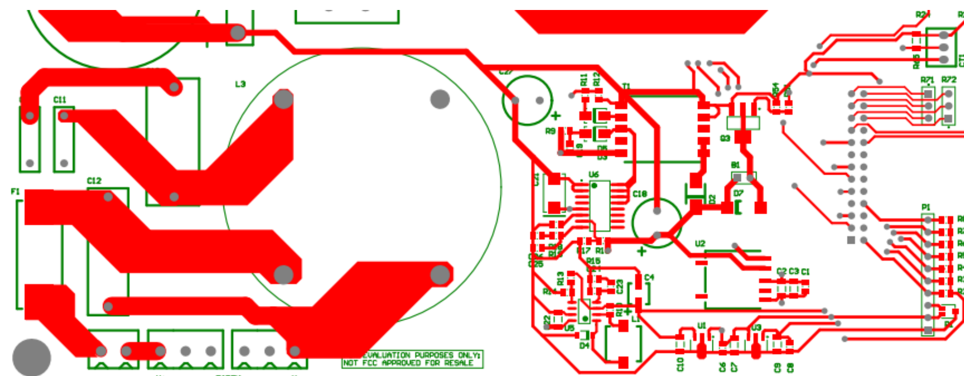


Figure 3.24: TOP-layer input stage and aux. supplies

As shown in fig. 3.24, the distances between traces at the input were kept at

least 5 mm apart for safety reasons. The compensation loops are also kept close to the ICs. The filtering capacitors are kept very close to their dedicated ICs to eliminate as much trace inductance effects as possible and give their internal power rail a clean voltage supply. Since the flyback converter is quite far from the input capacitors, the author placed an additional 4.7 μF/450 V electrolytic capacitor near it to ensure stable input voltage.
The heat dissipation is significant and needs to be taken into account. The board's secondary side power traces are unmasked and enforced with copper wires and solder to increase their current handling capability. The board dimensions are not the primary objective since the board serves a demonstration and evaluation purposes, but an effort to keep the board at a reasonable size was made. Decreasing the board size to its minimum would be one of the goals of the next version. Overall the power board PCB design is quite complicated but essential for the proper function of the supply. The whole power PCB design is shown in A.11 and A.12.

Chapter 4

Measurements

4.1 Efficiency measurement

One of the essential parameters of the SMPS is its efficiency. As the power source for our measurement, we use the Chroma 6530 3kW programmable AC power supply. Its maximum current output is 15 A, which is sadly not enough for measuring the full output range. At the input voltage of 230 V, it is possible to deliver a maximum of 2 kW into the SMPS. For the calculation of the efficiency, the input current and voltage, and further output current and voltage are measured. We use the power meter for the input parameters. For the output current measurement we use a Tektronix TM502A current sonde with 100 A range. This is an essential limiting factor when it comes to our ability of current, and therefore, power measurement. The output measurements are displayed on the oscilloscope LeCroy LT374M.

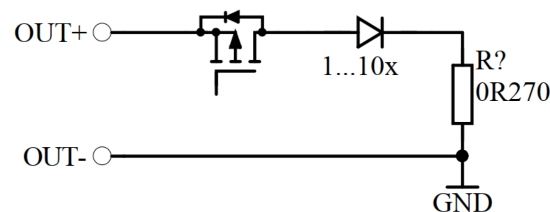


Figure 4.1: The schematic description of the load

The load has been made by hand in the laboratory and consists of MOSFETs connecting the load to the output, a variable number of diodes 4.2, and a resistive load 4.3. The diodes serve as a constant voltage component

preventing the welding output from triggering short circuit protection at low output currents.

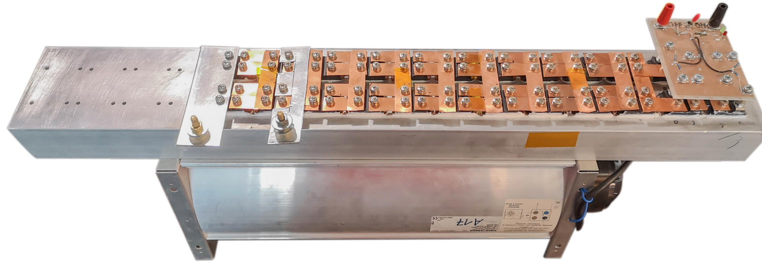


Figure 4.2: Semiconductor part of the load

The resistive part of the load is made of long iron screws put in series. There are two racks, each with a resistance of 0.135 Ω at 25 °C. The iron increases its resistance dramatically with temperature (up to 50% increase from initial value). This fact brings a slight inconvenience to the temperature and efficiency measurements since we are dealing with a constant-current source.

Figure 4.3: Resistive part of the load

In normal operating conditions, there are no output capacitors present.

The reason for this is their very fast discharge at the initial contact of the electrodes. In normal conditions, a rectangular current waveform (as shown in fig. 4.4) is present on the output.

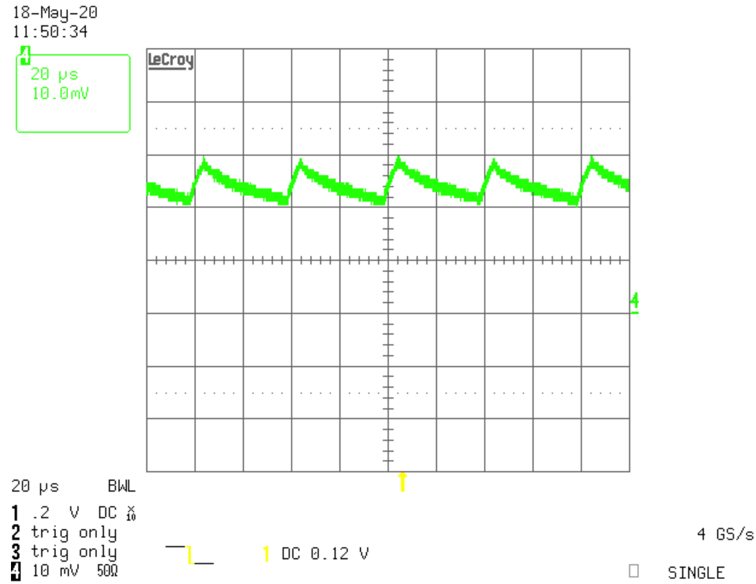


Figure 4.4: Output current waveform [20 A/div]

For the measurement only, two 220 μF capacitors were placed on the output to decrease the voltage and current ripple. This way, it is possible to approach the maximum current value without saturating the sonde.

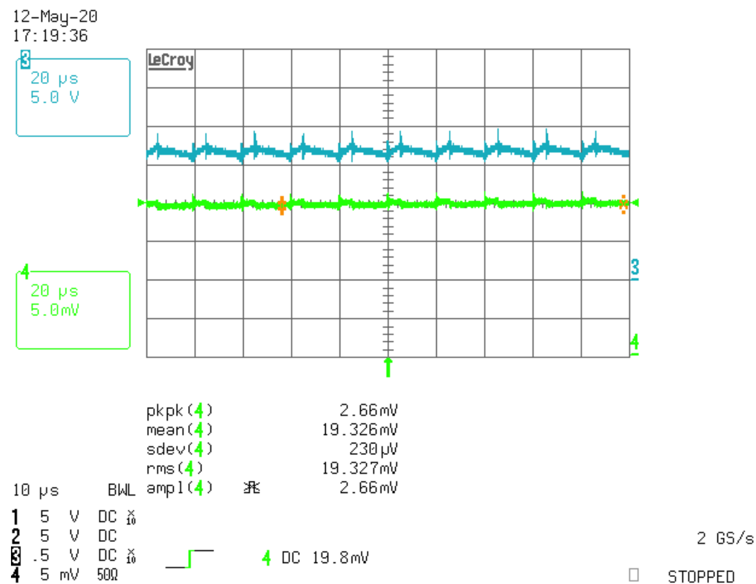


Figure 4.5: Maximum output current vs. output voltage [25 A/div]

In figure 4.5, we see the output voltage across the load (Blue) and output current (Green), where 1 mV represents 5 A. Therefore, the maximum mea-

sured RMS current is 96.64 A. We can notice that the sonde is reaching its saturation. The RMS current is most likely slightly higher. The final measured efficiency is displayed below.

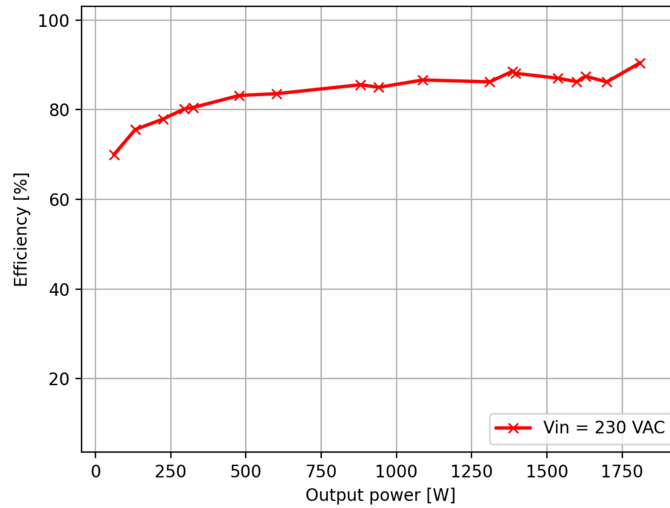


Figure 4.6: Welding machine's measured efficiency

Since the load's value drifts with the temperature rapidly, it was difficult to measure the efficiency with an acceptable level of accuracy. The input and output power reading has to happen at the same time.

4.2 Temperature measurements

The heat dissipation on a high power SMPS is considerable, making the temperature measurements using the thermal camera essential in our application.

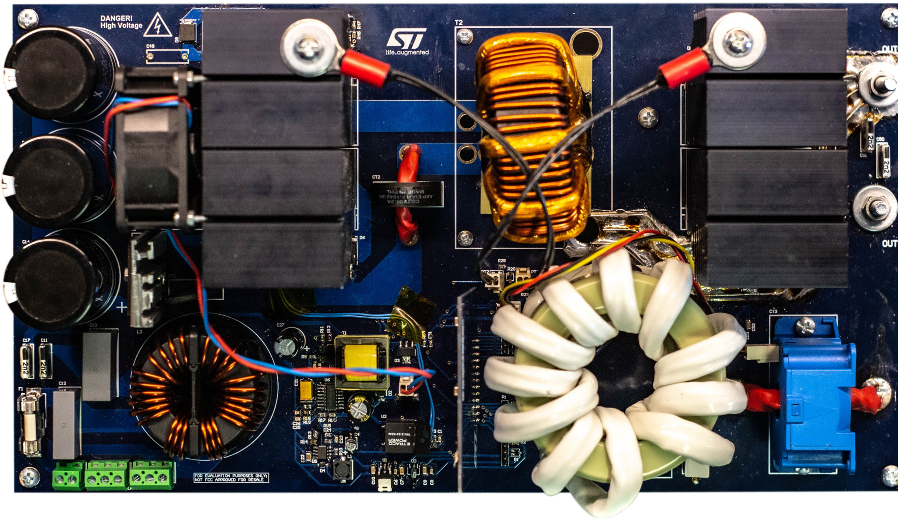


Figure 4.7: Final functional prototype (top view)

The pictures are used to determine the maximum work cycle of the welding machine at specific power output and adjusting the parameters of the device.

Figure 4.8: Temperature measurement with NTC at 1.5 kW

More importantly, it allows us to see flaws in the design that might cause

the device to fail. There were two flaws the author expected before the measurement. The input NTC and rectifier bridge were expected to overheat. The NTC was measured to confirm the suspicion. After the measurement, it was bypassed, since the inrush protection is implemented elsewhere.

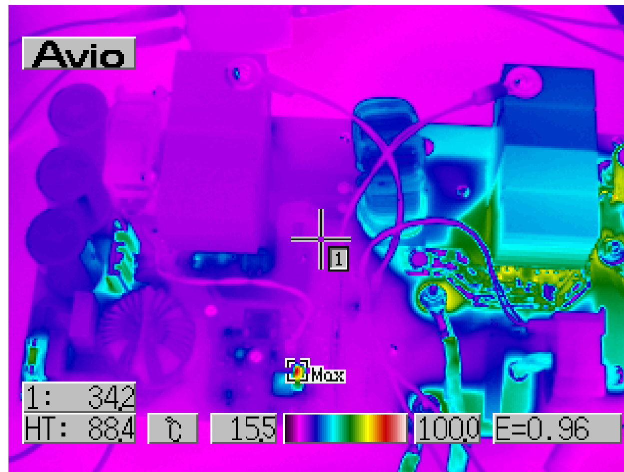


Figure 4.9: Temperature measurement at 1kW

In fig. 4.9 we can see that there are no significant problems with the heat at 1 kW of power throughput, although we can already notice the secondary power traces getting considerably warm. At 1.5 kW of power, we notice that the fuse temperature is very high. This needs to be addressed, and a larger

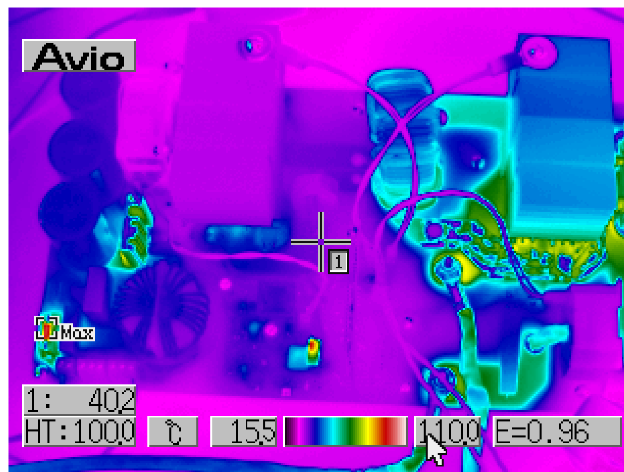


Figure 4.10: Temperature measurement at 1.5 kW

fuse with a higher power rating is needed. Also, a better fuse holder with a lower voltage drop would be appropriate. The secondary power traces further increased their temperature, which now, in some cases, exceeds 80°C, as we can see in fig. 4.11. The worst temperature is in the place where the inductor connects to the board. The conductive area for the connection on the TOP layer of the PCB is not large enough.

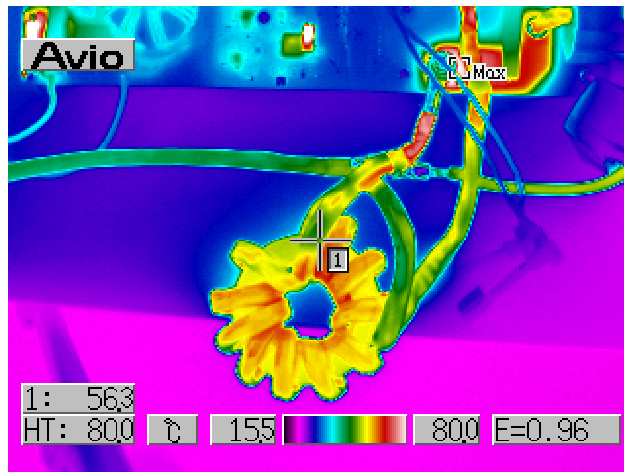


Figure 4.11: The output inductor at 1.5 kW

The inductor itself does not exceed 70°C at a current of 80 A, which is quite a good result considering the poor quality of the Litz wire used in the winding. The power loss could be further decreased by using a better quality conductor. The author made an error on the PCB, where he forgot to leave some space for the rectifier's heatsink. A piece of aluminum was screwed to it, providing at least some cooling, but as said before, it was expected to overheat at some point.

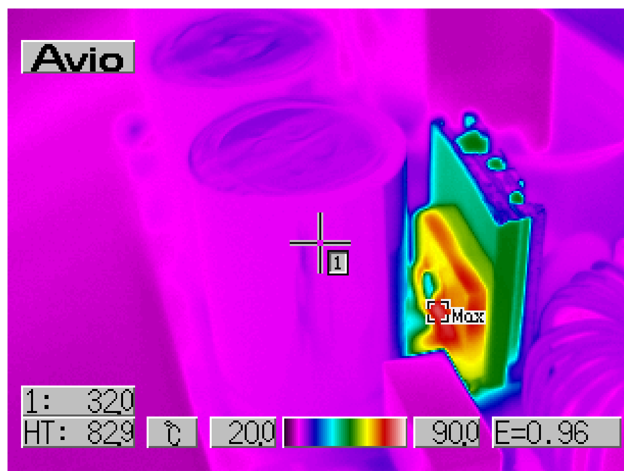


Figure 4.12: Temperature measurement of the diode rectifier at 1.5 kW

We can see that the bridge rectifier still has an acceptable temperature at 1.5 kW, but at higher power, a proper heatsink needs to be put in use. This problem could be temporarily dealt with by placing the rectifier from the bottom side of the board and attaching a more massive heatsink to it.

Chapter 5

Conclusion

In the first part of this thesis theory of the possible topologies and their principles was explained. The semiconductor components technologies and some of their parameters were also briefly mentioned. The second part includes the complete design and all the necessary calculations used in the process. A functional prototype from fig. 5.1 and 4.7, based on the design, was built and measured in the last part of the thesis.

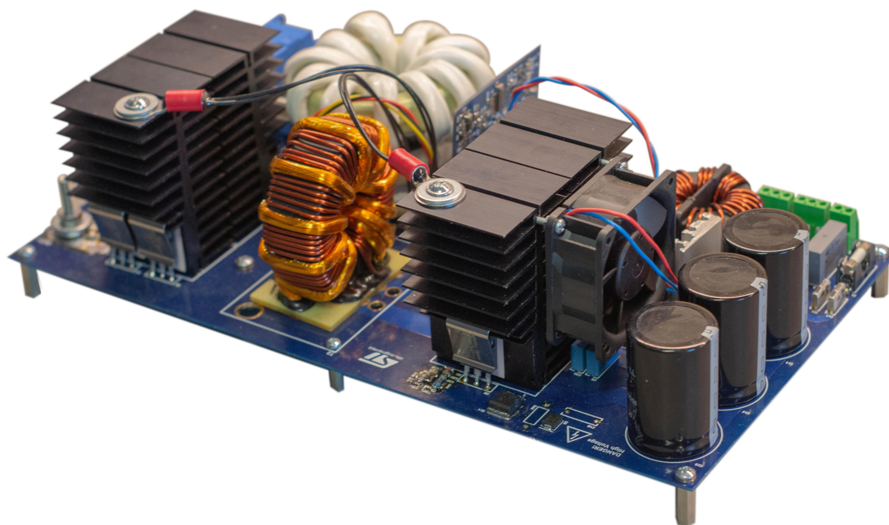


Figure 5.1: Final functional prototype (side view)

The converter's efficiency has been measured, reaching a satisfying result

of more than 85%. Sadly it was not possible to measure the full output range of the device. The temperature measurements showed that the welding inverter needs no significant adjustments for the output power up to 1.5 kW. While constructing the prototype, the author realized many things that should be improved and features that should be added in the second version to improve the quality of the device. In the future version, a 105 μm copper thickness should be used for all the traces. Also, the thickness of the PCB's dielectric should be increased to improve the board's sturdiness. The use of a proper heatsink for the bridge rectifier and a fuse with larger power handling capability is necessary for higher power outputs. Also, the power traces of the secondary side need to be adjusted to lower their temperature. In addition, the author would also like to implement some MCU features.

The author firmly believes that with the newly gained insights and all the specific improvements in mind, the device's second version would reach the full power output of 4 kW with reasonable temperature characteristics and efficiency.

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Manufacturing data

This chapter includes:

- Power board schematics
- Control board schematics
- Power board PCB
- Control board PCB

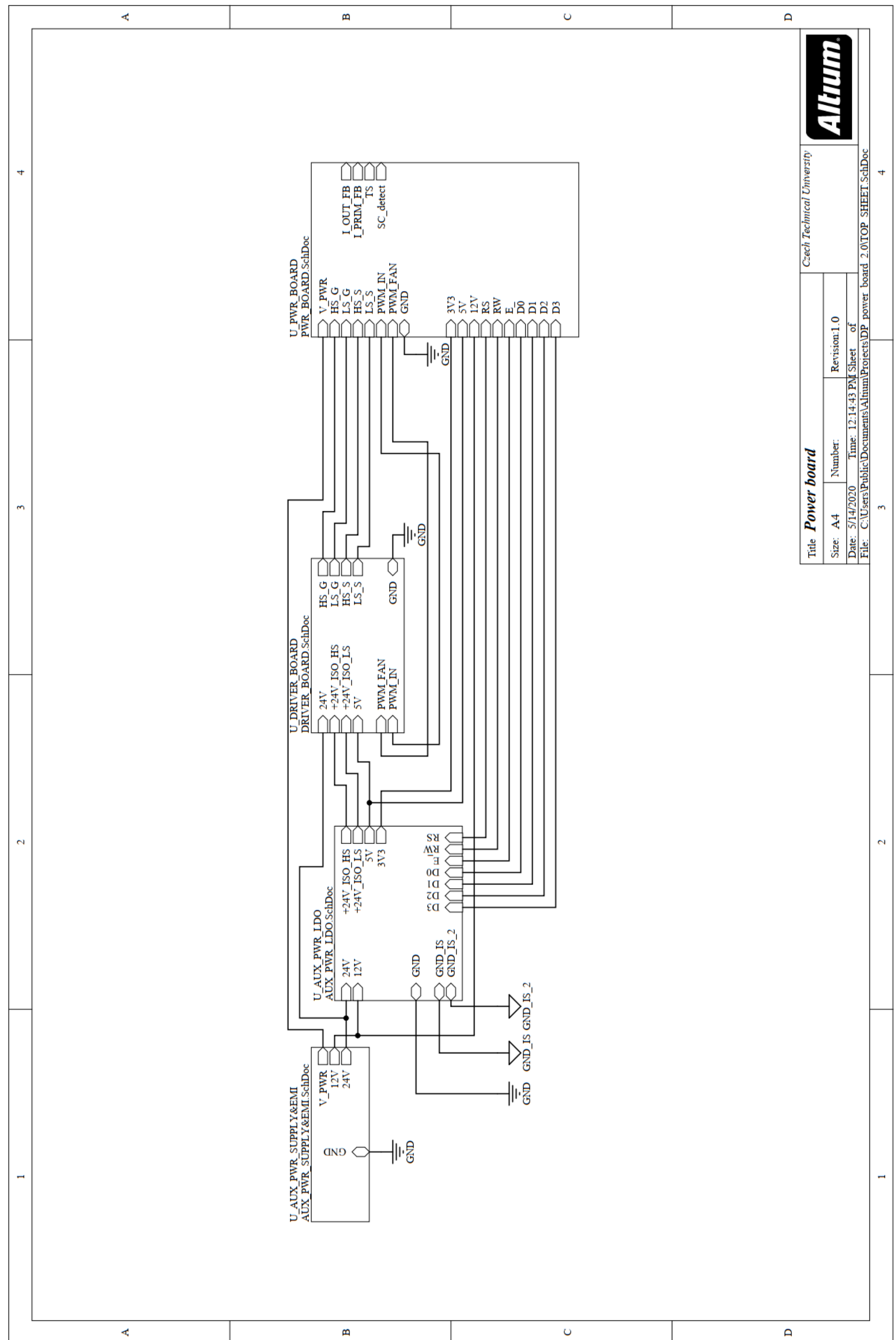

Figure A.1: Power board TOP-sheet

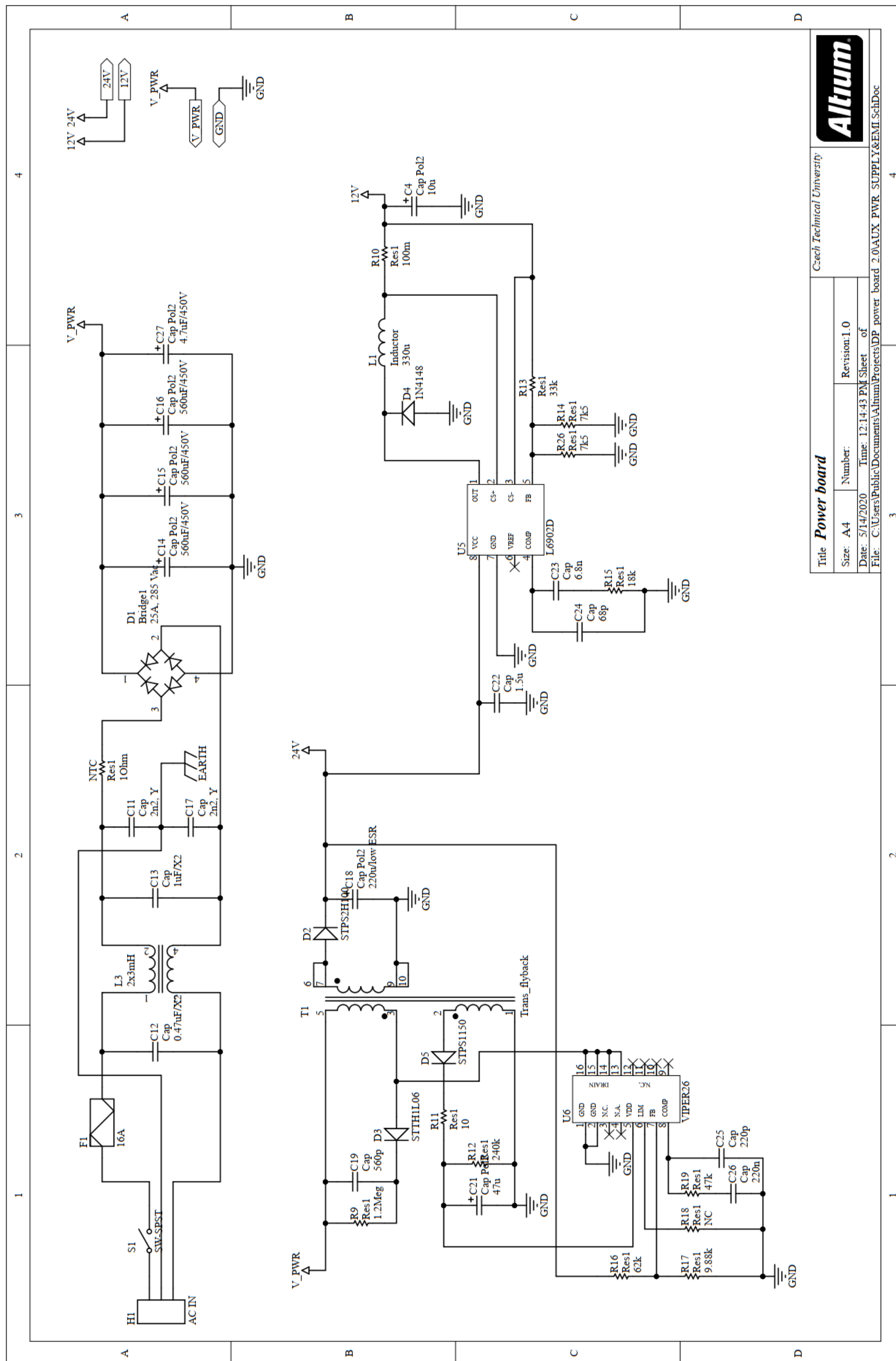

Figure A.2: Input stage schematic

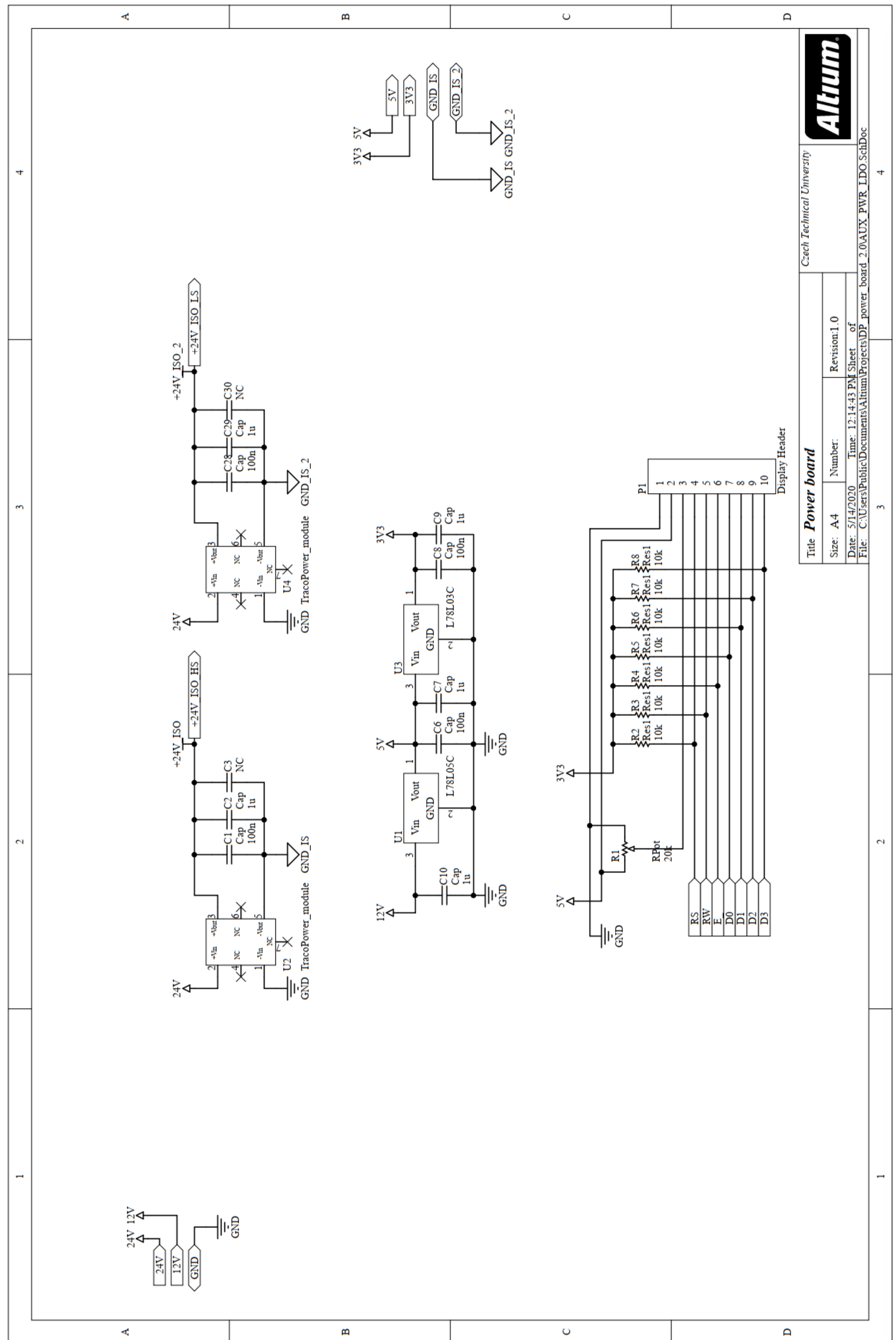

Figure A.3: Power module stage schematic

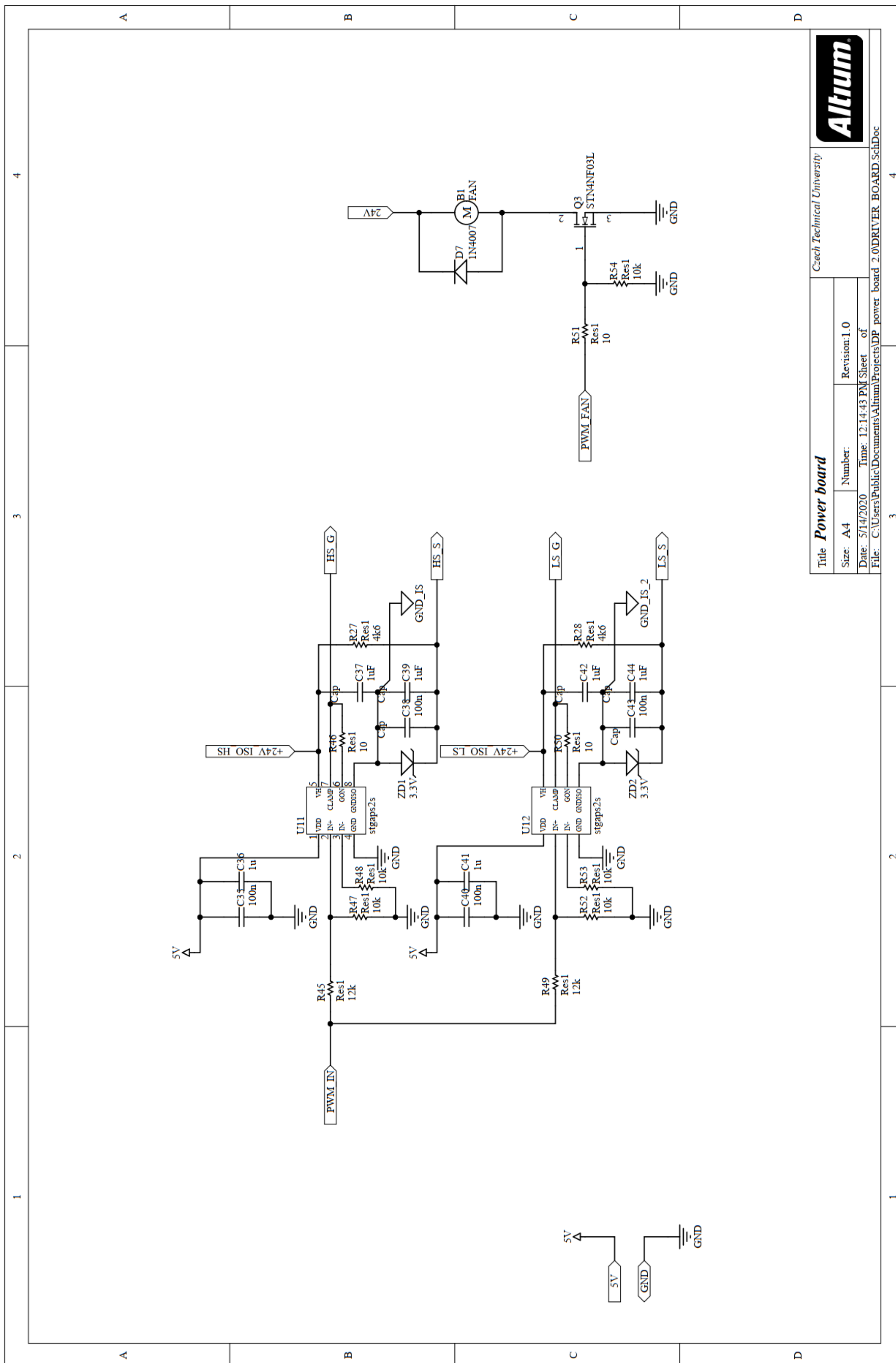

Figure A.4: Driver stage schematic

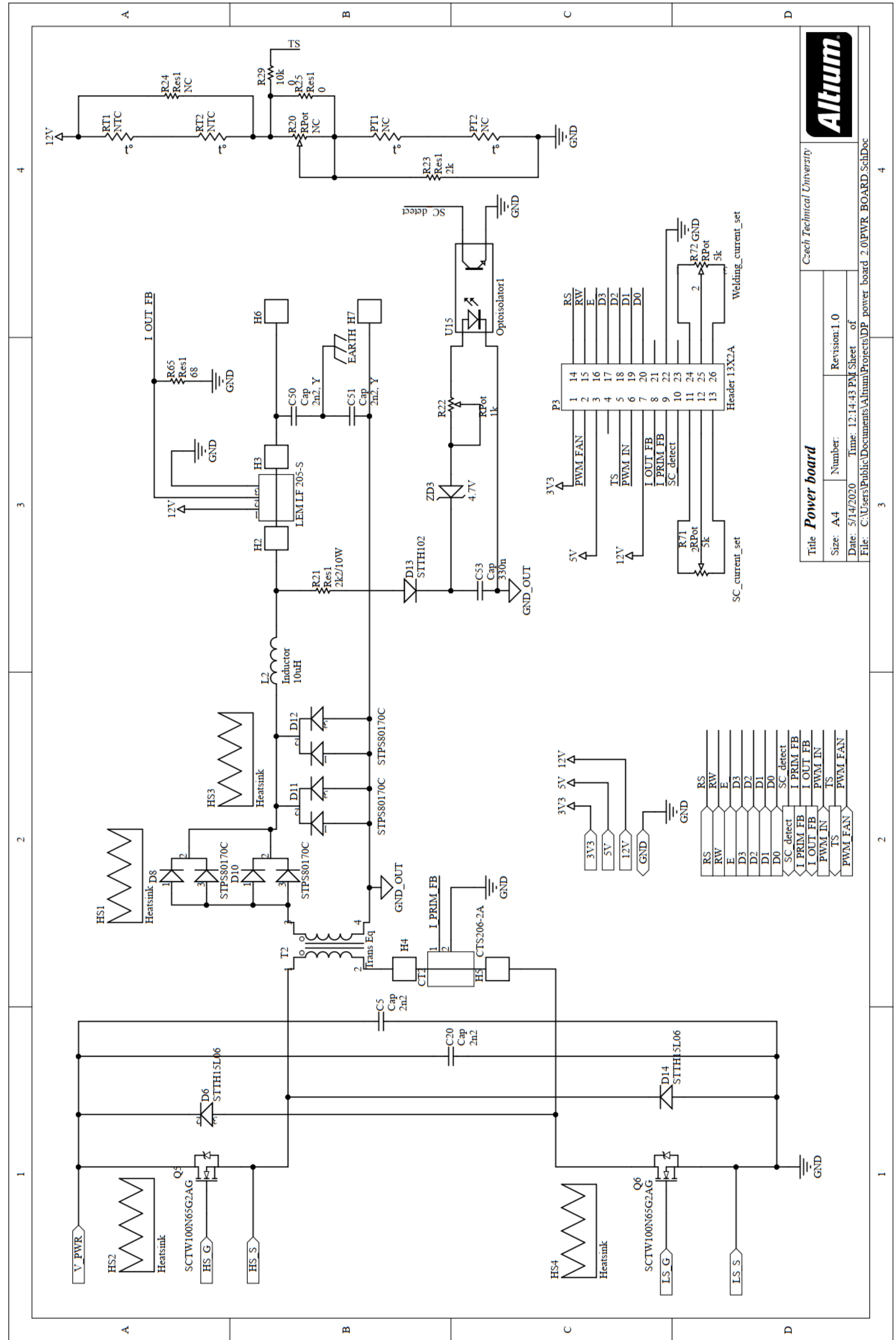

Figure A.5: Power stage schematic

Figure A.6: Control board TOP-sheet

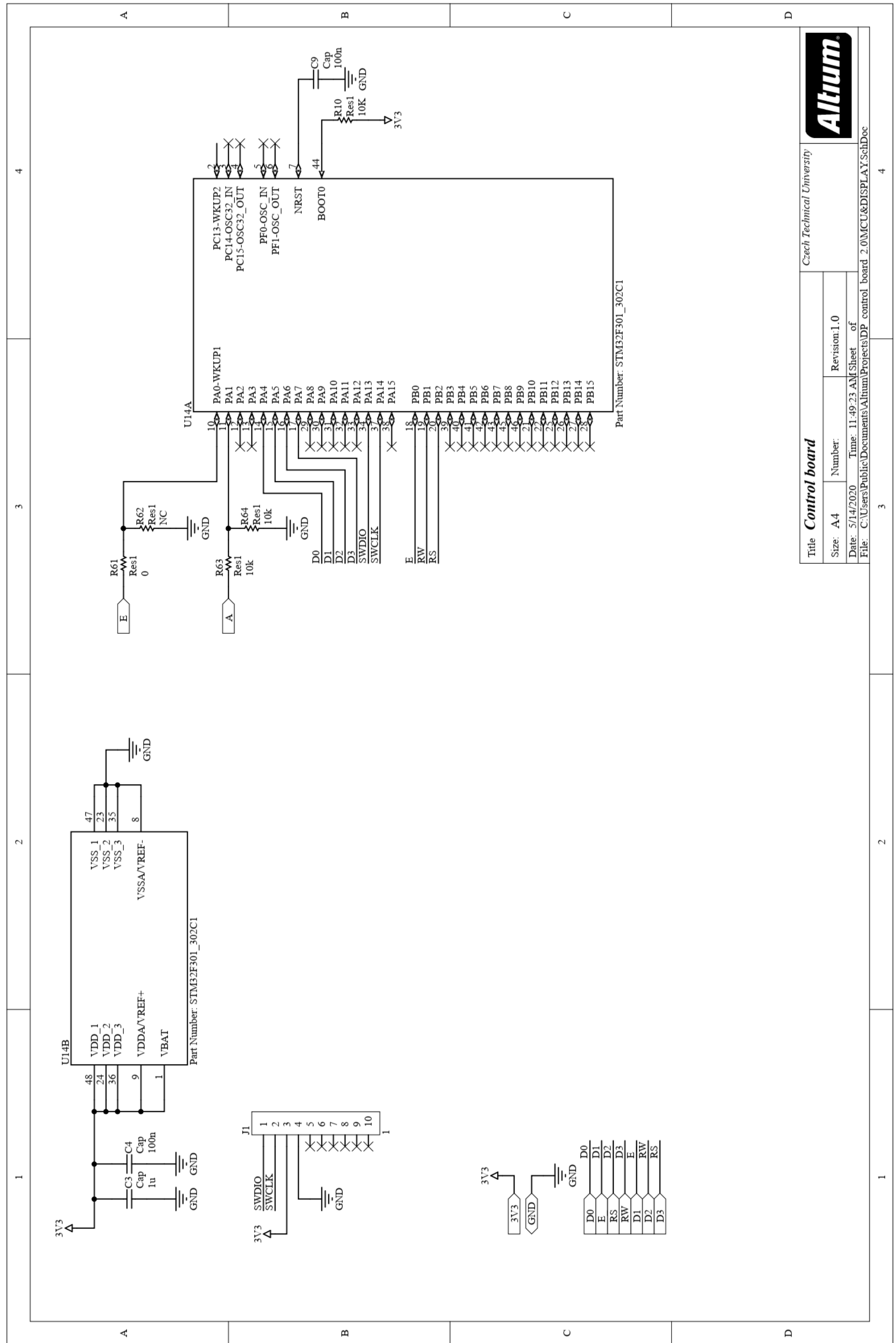

Figure A.7: MCU stage schematic

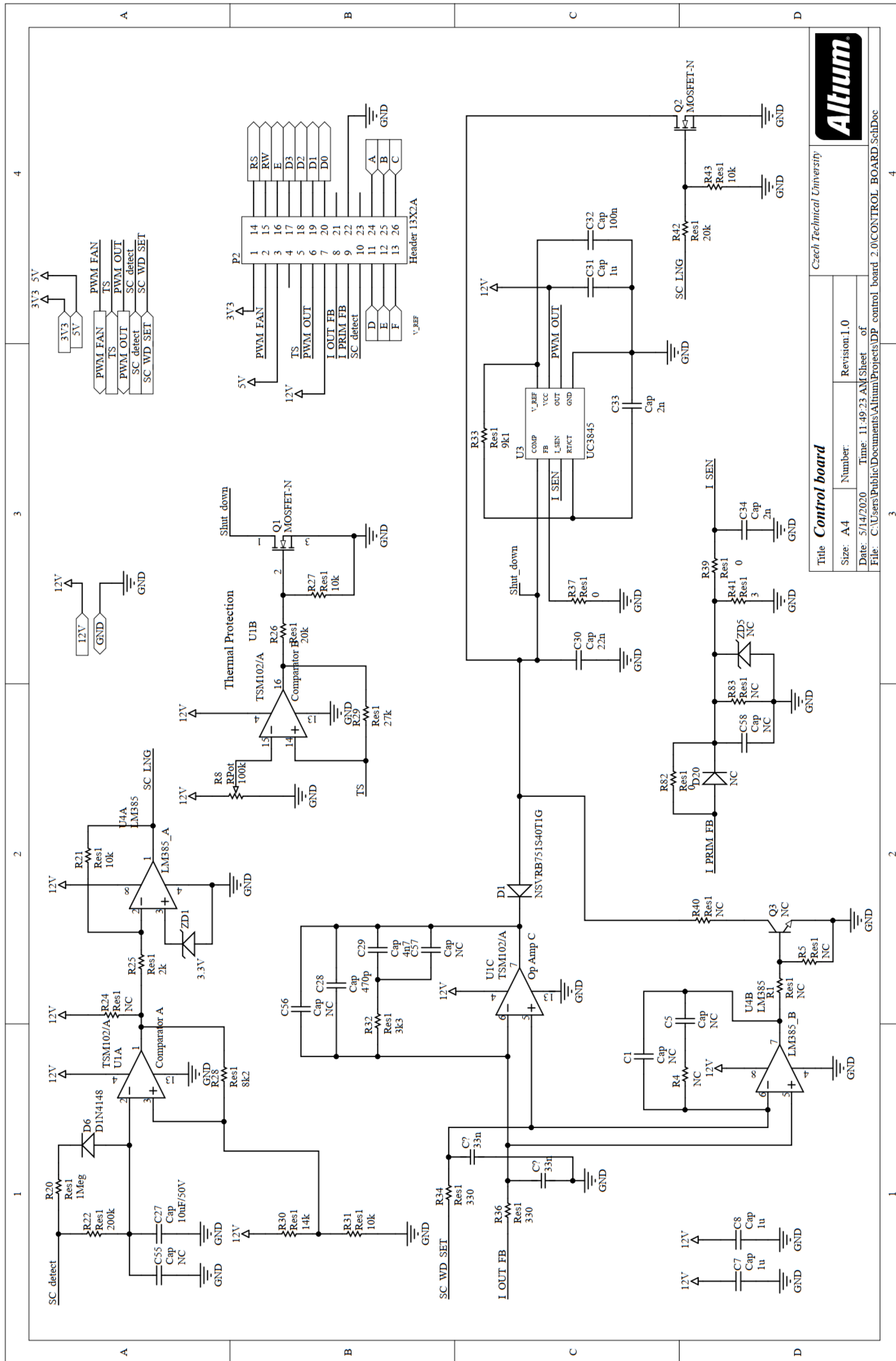

Figure A.8: Control stage schematic

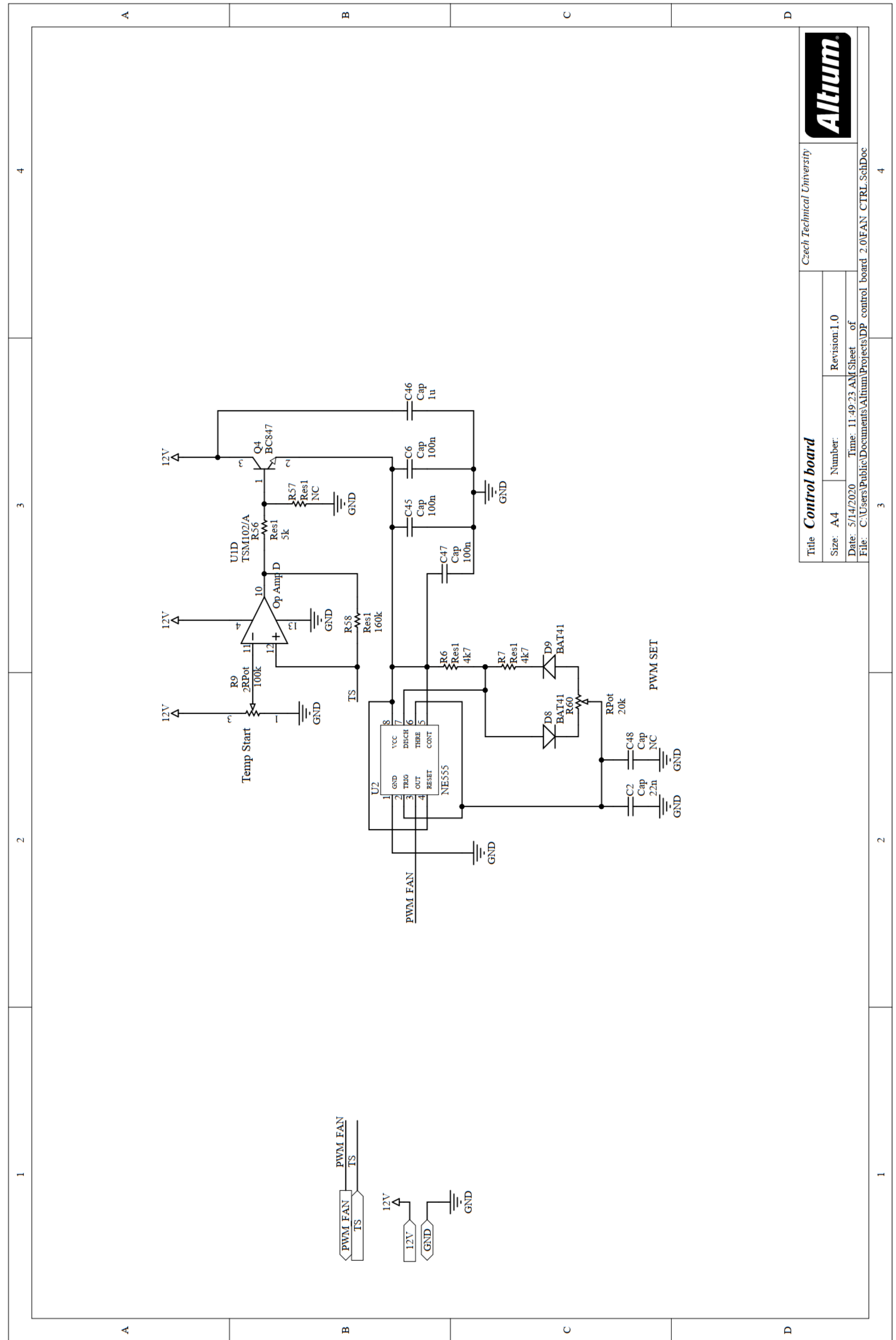

Figure A.9: Fan PWM stage schematic

Figure A.10: Welding and SC current stage schematic

Figure A.11: Power board TOP layer

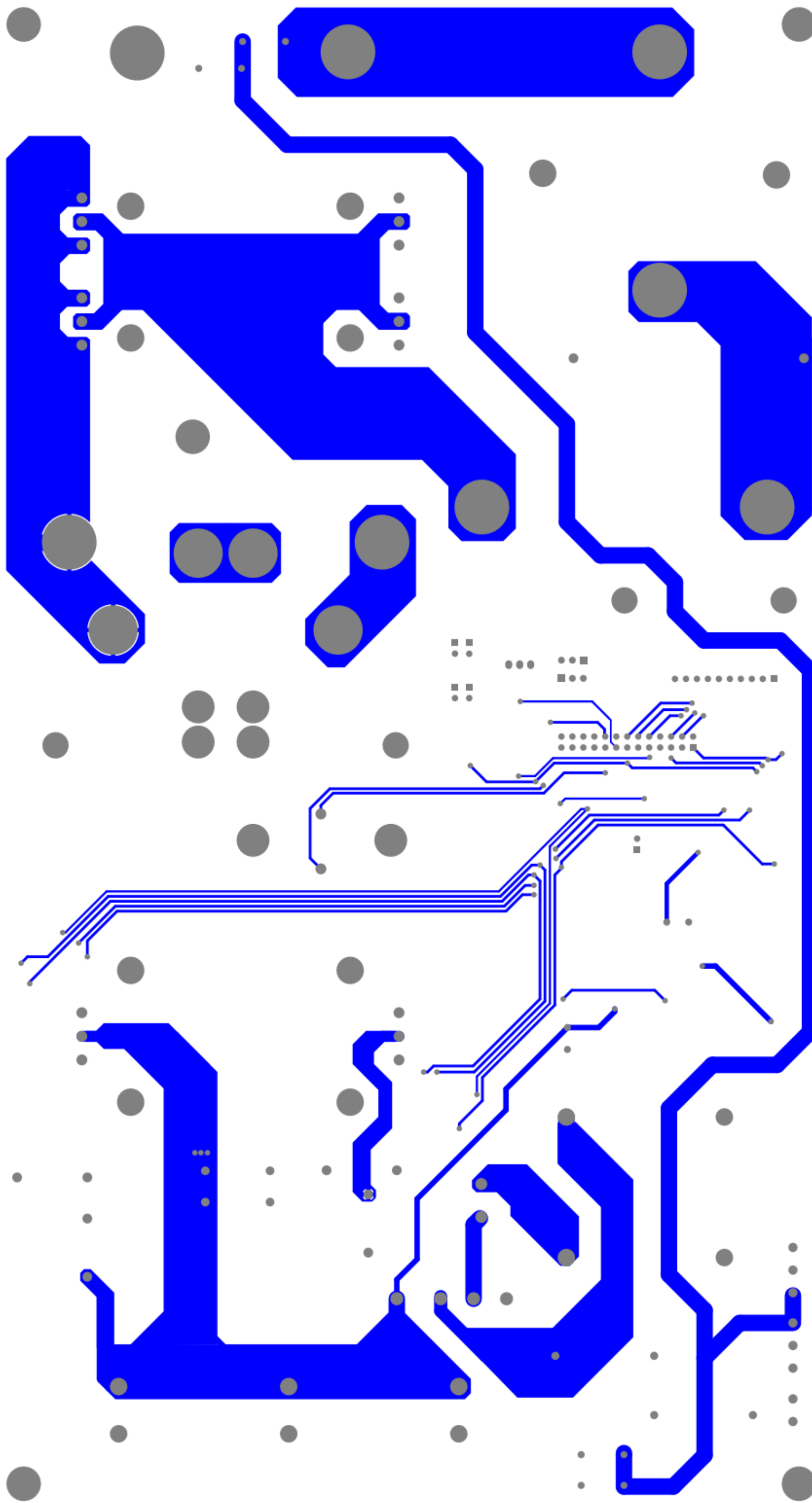

Figure A.12: Power board BOTTOM layer

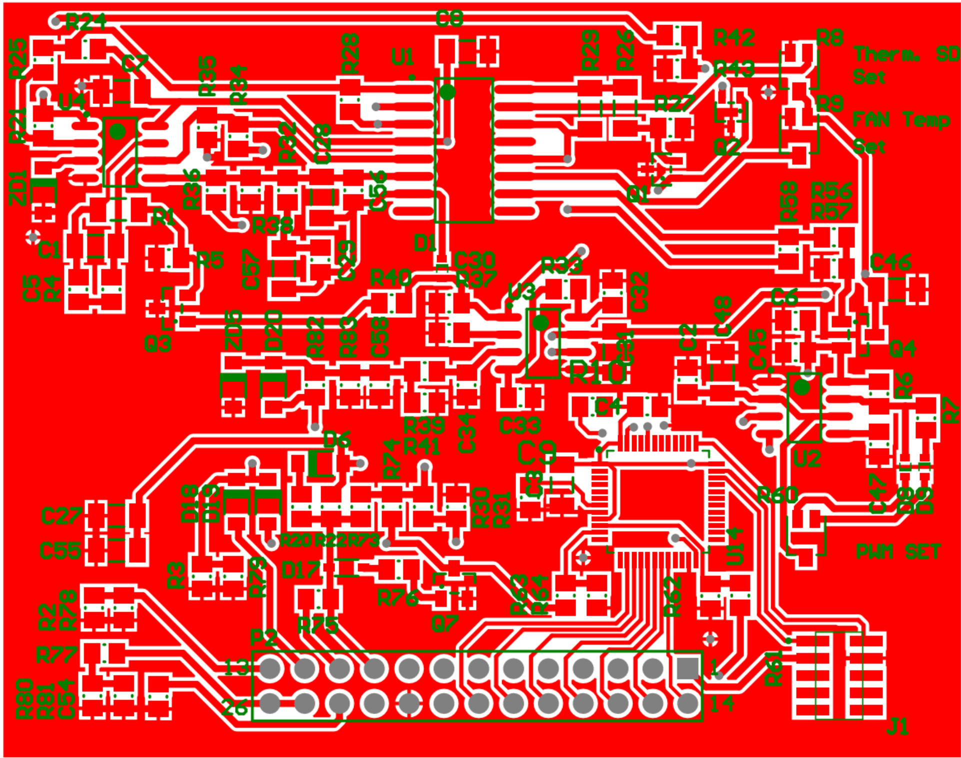

Figure A.13: Control board TOP layer

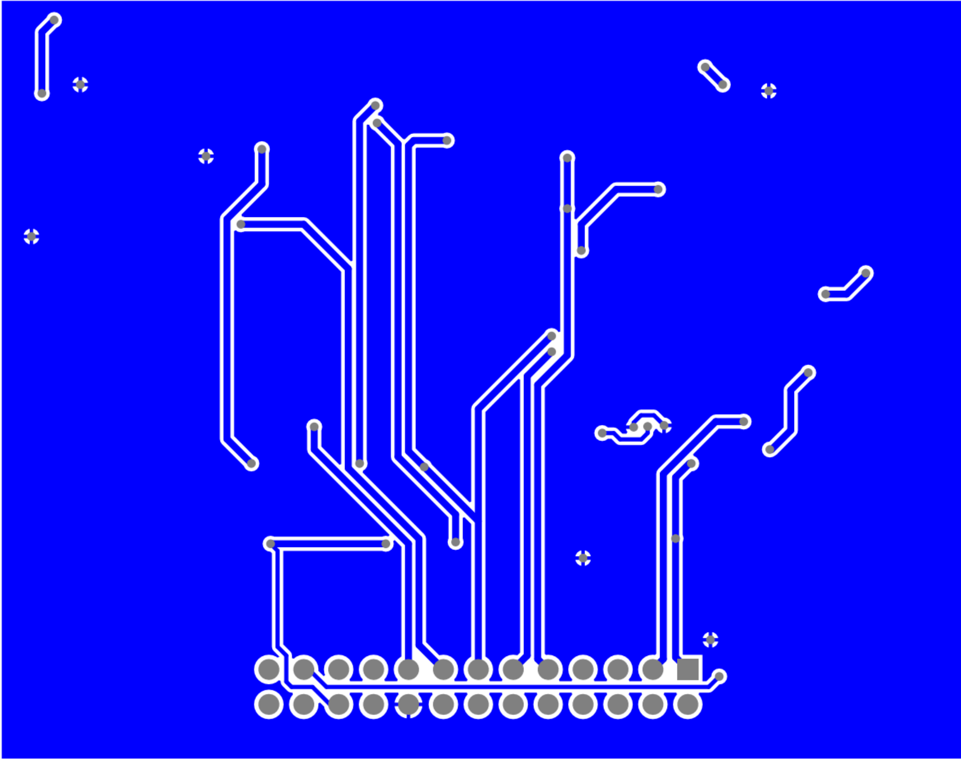

Figure A.14: Control board BOTTOM layer