Radiation Tolerant 8-bit Analog to Digital Converter with Successive approximation

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Abstract. *This paper brings implementation of 8-bit asynchronous analog to digital converter with successive approximation (SAR ADC) in 180 nm CMOS SoI technology. Radiation tests have proven that used technology is radiation tolerant up to 1 kGy. Layout in the used technology occupies 319 × 115 μm^2. The proposed SAR ADC consumes 295 μW from 1.8 V power supply at 4 MHz sampling frequency. Achieved ENOB is 7.81 bit and calculated figure of merit is 163 fJ/conversion-step.*

Keywords

radiation tolerant, SAR ADC, low power, asynchronous, fully-differential

1. Introduction

Modern electronics for special applications such as space applications, X-ray monolithic detectors, avionics, CERN experiments, etc. needs to be working in a radiation environment. Electronics in integrated circuits can be hardened by design, technology or layout techniques. This paper brings 8-bit SAR ADC in 180 nm SoI technology working in radiation environment up to 1 kGy. This maximum radiation value limits used technology [1]. The proposed design brings innovation of Harpe at al.[2] with improvements for radiation environment. The first improvement is the used SoI CMOS technology which is more radiation tolerant than classic bulk technologies [1]. The second improvement is using layout matched structures in combination with differential design which helps to eliminate single event effects (SEE). The third improvement is own customization of metal-oxide-metal (MoM) capacitor used in capacitor DAC of the SAR ADC. The figure of merit of the proposed design is 163 fJ/conversion step which is competitive value in comparison with existing published results, for example with references [3], [4], [5].

2. 8-bit SAR ADC circuit description

The 8-bit SAR ADC circuit design is described in detail by Harpe et. al [2]. In this section, only brief circuit description is provided and modifications are emphasized. A block diagram is shown in Fig. 1.

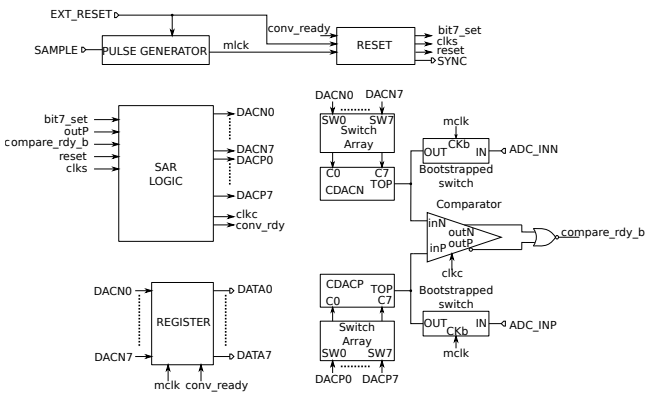

Fig. 1: 8-bit SAR ADC block diagram

The proposed design contains in comparison with [2] a pulse generator circuit which generates sampling pulse with adjustable length at rising edge of the SAMPLE signal. A bootstrapped switches [6] are used instead of transfer gates to improve the linearity of sampling signal into top plates of capacitor arrays. The output register latches data when conversion is finished. Data are latched until the next SAMPLE signal is received. Both of capacitor DAC's uses customized MoM capacitor shown in Fig. 2. Each of unit capacitor has dimensions 4.24x4.24 μm^2 with capacitance 4.5 fF. The proposed unit capacitor acts as a shielding box which improved linearity. A common centroid layout in the comparator is used. The common centroid layout in combination with fully differential ADC design mitigates SEE [7].

3. Results

Differential and integral non-linearities (DNL, INL) of the SAR ADC from simulations are shown in Fig. 3 and Fig. 4. These nonlinearities have been extracted from transfer

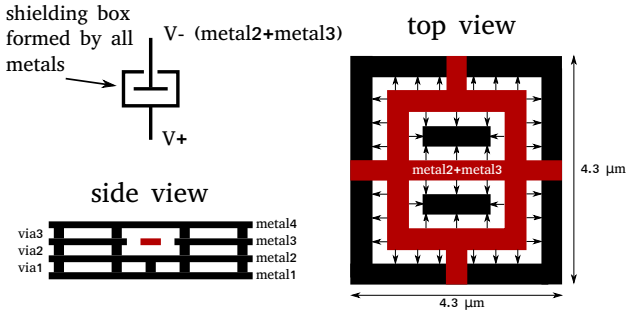

Fig. 2: The proposed MoM capacitor

function by gradually increased step of 1 mV (0.25 LSB) at the ADC input. The worse case DNL is held within 1 LSB and -0.5 LSB and for INL between 1 LSB and -2 LSB.

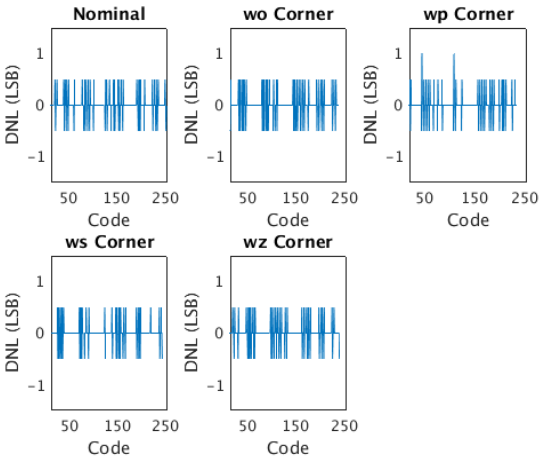

Fig. 3: Simulated DNL

The implemented prototype in 180 nm SoI CMOS technology is part of a monolithic pixel detector. For this reason, is impossible to measure SAR ADC directly and therefore only simulation results are provided. Measurements of the implemented prototype have revealed a problem with limited range of AD converter. The problem is caused by incorrect layout of PMOS voltage divider which sets reference of the fully differential amplifier which drives SAR ADC input. This failure resulting in the limited output voltage range of analog circuits driving the SAR ADC. The problem was understood and will be eliminated in future circuit re-design. However, the proposed SAR ADC seems to be working correctly.

Acknowledgements

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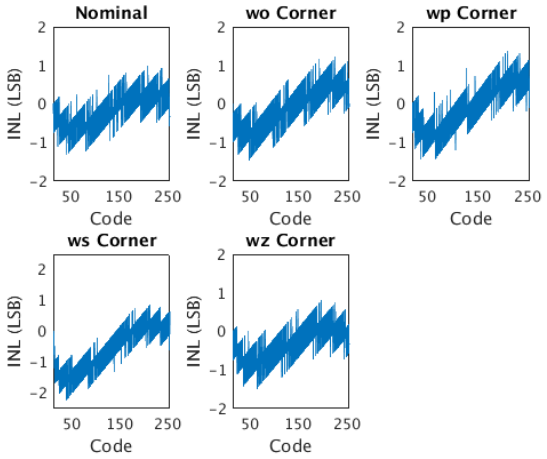

Fig. 4: Simulated INL

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Pavel Vancura was born in 1981. Master's degree in the field of Microelectronics completed in 2017 at the Czech Technical university in Prague (CTU), faculty of electrical engineering (FEE). Currently he is a PhD student at CTU FEE and he is also working at the Faculty of Nuclear Sciences and Physical Engineering Czech Technical University in Prague, department of Physics, as a scientific employee for development of semiconductor pixel detectors.