# Application of SiC MOSFET in Industrial Power Supplies

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master's thesis

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# ZADÁNÍ DIPLOMOVÉ PRÁCE

## I. OSOBNÍ A STUDIJNÍ ÚDAJE

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Studijní program: **Elektronika a komunikace**

Studijní obor: **Elektronika**

## II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

**Aplikace MOSFET tranzistorů na bázi SiC v průmyslových napájecích zdrojích**

Název diplomové práce anglicky:

**Application of SiC MOSFETs in Industrial Power Supplies**

Pokyny pro vypracování:

1. Zhodnoťte problematiku použití SiC MOSFET tranzistorů v průmyslových napájecích zdrojích.
2. Navrhněte měnič typu flyback s možností použití vysokonapěťových tranzistorů SiC, stejně tak jako tranzistorů Si. Vstupní napětí: 150 V DC - 1 kV DC, výstup 24 V, 100 W.
3. Simulujte a změřte spínací vlastnosti použitých tranzistorů. Analyzujte výsledky.
4. Otestujte funkčnost navrženého zdroje a změřte jeho parametry.
5. Porovnejte tranzistory SiC a Si podle účinnosti a teplotních měření.
6. Shrňte a zhodnoťe výhody použití Si či SiC tranzistorů.

Seznam doporučené literatury:

1) SHUR, Michael & collective; SiC Materials and Devices; World Scientific, 2006; ISBN: 9812773371
2) MOHAN, Ned; UNDELAND, T. M.; ROBBINS, W. P.; POWER ELECTRONICS – Converters, Applications, and Design; Wiley; 1995; USA; ISBN: 0-471-30576-6
3) STMicroelectronics; AN4671, Application note: How to fine tune your SiC MOSFET gate driver to minimize losses; 2015

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Datum zadání diplomové práce: **01.10.2019** Termín odevzdání diplomové práce: _____

Platnost zadání diplomové práce: **30.09.2021**

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podpis děkana(ky)

## III. PŘEVZETÍ ZADÁNÍ

Diplomant bere na vědomí, že je povinen vypracovat diplomovou práci samostatně, bez cizí pomoci, s výjimkou poskytnutých konzultací. Seznam použité literatury, jiných pramenů a jmen konzultantů je třeba uvést v diplomové práci.

17.12.2019
Datum převzetí zadání

[redacted]
Podpis studenta

# Acknowledgement

I would like to express many thanks to my supervisor Ing. Vladimír Janíček, Ph.D. for his suggestions and ideas towards this thesis. Also to STMicroelectronics Prague PowerLab, because without the collaboration this thesis most probably wouldn't exist.

A very special thanks go to Sanjin Kek and Magdalena Dědičová – for all the help and support during the development of this thesis!

# Declaration

I declare that the presented thesis was developed independently and that I have quoted all sources of information. This was made in accordance with the methodical instructions about ethical principles for writing academic thesis.

# Abstract

Key of this master's thesis is to analyze, simulate, compare and discuss the application of Silicon-Carbide MOSFET in industrial power supplies. With consideration to driving SiC MOSFET with usual PWM controllers. The whole problem is demonstrated on 24V 100W Flyback converter, same as a comparison with standard silicon-based MOSFET.



**Keywords**

SiC, SiC MOSFET, Industrial, Flyback



# Abstrakt

Záměr této diplomové práce je analýza, simulace, porovnání a diskuze aplikace tranzistorů MOSFET na bázi karbidu křemíku v průmyslových zdrojích. Pozornost je věnována řízení SiC MOSFETů standartními kontroléry. Celá problematika je popsána na 24V 100W měniči typu Flyback, stejně tak jako porovnání se standartním křemíkovým MOSFETem.



**Klíčová slova**

SiC, SiC MOSFET, Průmyslový, Flyback

# Contents

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# Abbreviations

| | |
|---|---|
| SiC | Silicon carbide |
| EMI | Electro-magnetic interference |
| WBG | Wide bandgap |
| FF | Fixed frequency |
| QR | Quasi-resonant |
| ST | STMicroelectronics |
| HV | High voltage |
| NTC | Negative temperature coefficient thermistor |
| SMD | Surface mount device |
| OCP | Overcurrent protection |
| CCM | Continuous-conduction mode |
| DCM | Discontinuous-conduction mode |
| SS | Soft-start |
| IC | Integrated circuit |
| AMR | Absolute maximum rating |
| PCB | Planar circuit board |
| $R_{sense}$ | Current sensing resistor |
| CMM | Common-mode |
| PSU | Power supply unit |
| DC | Direct current |
| AC | Alternating current |
| UVLO | Under-voltage lock-out |

# 1 Introduction

This diploma thesis focuses on comparison of Si and SiC based MOSFETs. The whole problem is demonstrated on 100W flyback converter with high input voltage range: from 150 $V_{DC}$ up to 1 $kV_{DC}$. After a brief introduction in the first chapter, the second chapter summarizes whole flyback design. The design is described thoroughly, because for valid measurement and data interpretation is necessary to understand it completely, know its limits and all parameters which can affect the measurement, mostly in a not preferable way.

The third chapter starts with Si and SiC MOSFET theoretical introduction. The necessity of different driving is discussed, therefore following section presents the idea of Gate-Drive module. There is also focus on losses estimation and from there efficiency prediction. Chapter four presents measurements and puts them in comparison with predicted / estimated values. As this is a multiple criteria problematic, each major one is included and measurements were optimized in order to separate them as much as possible for further observation.

Final evaluation of results is made in the last chapter, same as comparison of Si and SiC MOSFETs for this application based on measurements. Not only them, but the whole design is summarized for further optimization or improvements. As I firmly believe, all important data for closer observation or verification are attached in digital form on CD or in Attachments.zip for online version.

One more thing to say in the beginning: as this thesis is written in English, I'm going to use nomenclature typical for English-speaking countries, instead of Czech. This refers especially to voltage: *V* instead of *U*; any other possibly-different unit (e.g. duty cycle) will be described, so any misunderstanding is improbable.

## 1.1 About SiC

Silicon carbide is in recent years well known as one of wide bandgap semiconductors. Depends on polytype (which are approx. 250), bandgap can be up to 3.3 eV. Besides of that, its synthetic form is being used in industrial sector since the end of 19$^{th}$ century. With hardness of 9 of Mohs scale is one of the most hard synthetic materials. As a stable chemical compound with excellent physical properties silicon carbide finds its place in abrasive, grinding and cutting industry.

In electronics, first use of SiC is dated not so long after. When Henry H. C. Dunwoody patented his Wireless-telegraph system in 1906, a "wave-responsive device" (Figure 1) was a truly important component. This was nothing else than a primitive point-contact diode which obtained signal rectification. And – it was based on silicon carbide.

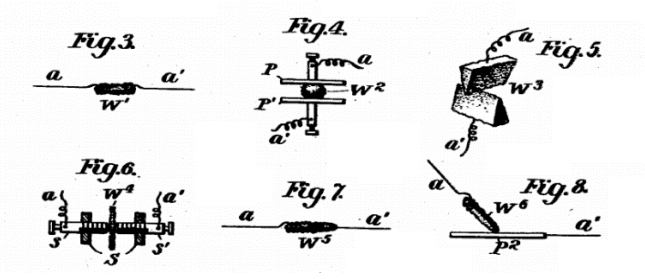



*Figure 1 Dunwoody's "wave-responsive device", w- parts are made of SiC; credit: [3]*

Soon after that (in 1907) yellow and blue electroluminescent emission of SiC crystal was found by H. J. Round. Another, a "pre-breakdown" emission, had been discovered by O. Losev in 1923. Opposed to these early inventions, not so many devices were based on SiC. Except LEDs, no other semiconductor devices were made widely until 1990s.

[1] [2] [3]

### 1.1.1 SiC as wide bandgap semiconductor

As semiconductors took their part in industrial sector, standard silicon parts shortly became insufficient for higher voltages. The debate on WBG semiconductors starts already in the 1950s and in the 1960, W. B. Shockley's *Introductory remarks on silicon carbide, a high-temperature semiconductor* was published [4].

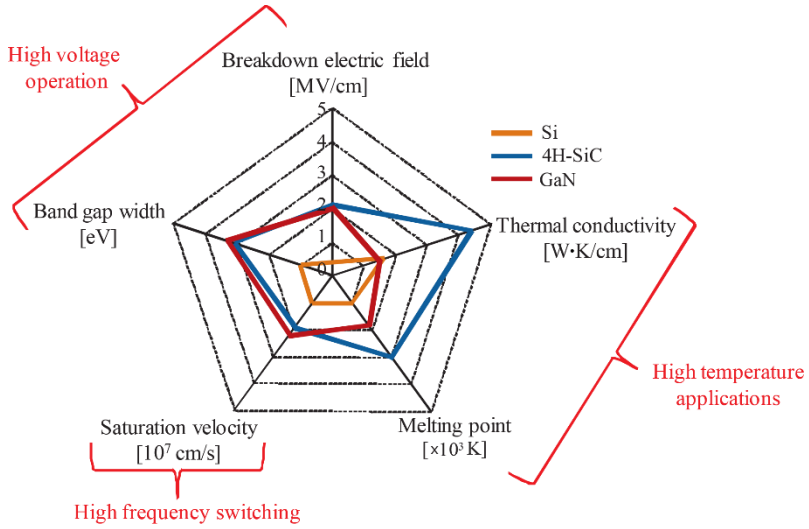



*Figure 2 Si, SiC and GaN comparison; credit: [4]*

Finding a different element or compound instead of silicon sounded well: wider bandgap is more or less proportional with higher breakdown electric field, thus components for higher voltage and / or with smaller chip could be made. Also, not only the bandgap doesn't make silicon the best material for power devices: as it's illustrated in Figure 2, Si can be easily beaten in other parameters too. It's not a big surprise that new materials such as aluminium nitride, gallium nitride and silicon carbide were tested. Even though WBG semiconductors are better (at least on paper), in these days' standard silicon components are still frequently used for high voltage applications.

It's mostly because the technology for Si components is well-known and proven after decades of production. Furthermore, this massive production decreases the price of Si chips. Opposed to, WBG semiconductors in the market starts from zero, with not as significant manufacturing progress as silicon industry. Just for illustration: Czochralski method is quite well known in electrical engineers' community as the only widely used method for making Si ingots. Those can be up to 2 m in height and weigh hundreds of kilograms. Unfortunately, this method is useless in SiC monocrystalline production. Instead, much more sophisticated and hence expensive Lely method is used. Based on sublimation an epitaxial growth in a low-pressure inert gas atmosphere, the result is quite poor compared to the Czochralski process: SiC *boules*[1] with maximum diameter 15 cm and useable height 20-25 mm, weighing not much more than one kilogram [5].

Yet another problem comes with SiC wafers: besides interstitial, substitution, vacancy or dislocation, another kind of defect appears in SiC boules – micropipe. Micropipes arise from vacancy, but of whole lattice, not a single molecule. Once this happens, they keep growing up

[1] Official term for product of Lely method instead of ingots for Czochralski method [2]

with the crystal. They also spread up to approx. 10 µm in diameter, so large area is affected (for illustration Figure 3).

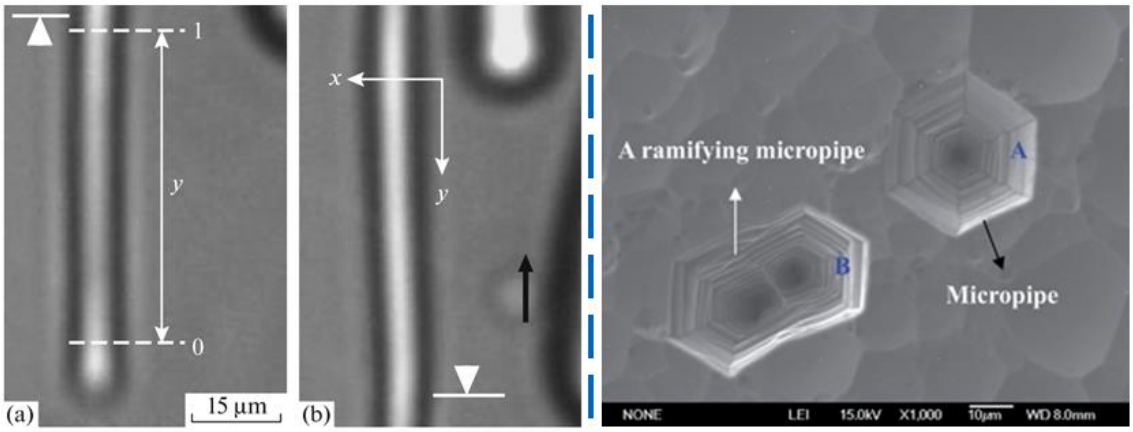



*Figure 3 Micropipes in transection (credit: [6]); cross-section (credit: [7])*

Combination of difficult Lely method and small boules make SiC wafer cost higher than silicon. Because of micropipes, not whole area can be used. This is critical mostly for high-power devices: the larger chip area is required, the bigger possibility of conflict with micropipe. Besides this disadvantage, thanks to its characteristics, SiC devices need a smaller chip area compared to their equivalent Si device.

[2] [4] [5][7]

## 1.2 Industrial power supplies

Converter designed in this thesis aims for usage in industrial sector as auxiliary power supply. Industrial units and machinery use mains directly, or power supplies mostly in range from tents kilowatts up to one megawatt. Except those primary PSUs very often another – auxiliary – power supplies are required. Those are used for another necessary purposes, i.e. user interface, control units, cooling etc.

There are many requirements on industrial power supplies, which are different from standard (home and office) designs. Most importantly:

- **Input Voltage:** In Europe, typical industrial mains voltage is 690 $V_{AC}$, also 400 $V_{AC}$ is frequently used, sometimes 500 $V_{AC}$. This design should be as versatile as possible, so it should work on 230 $V_{AC}$ mains too. DC-powered machinery, and so the DC mains, aren't unusual, but the voltage is sometimes specifically defined by the manufacturer. In photovoltaic sector, currently heavily used value is 1 $kV_{DC}$. Either way, auxiliary PSU often obtains safety functions, therefore they should handle undervoltage. Thus many of them have quite wide input voltage range.

- **Input transient voltage protection:** Especially heavy machinery may cause voltage transients to appear way more frequently than in standard mains. They can be caused also by natural events, but still industrial power supplies must manage stronger transient than home / office PSUs: up to 6 kV while the current may reach 3 kA [8]. This should be secured with a proper TVS, mostly varistor, same as all safety margins for component ratings should be respected.

- **Electromagnetic compatibility:** As any other device, industrial PSUs must fulfill EMC standards. For auxiliary PSU radiated emission is not so significant as from primary PSU

or the machinery, but still shielding (e.g. Faraday screen) should be used as a protection against it. This device is presumed to be used in Europe, so I will focus only on standard EN 55011 [9]. As design for industrial usage is in many ways more challenging, this may be the first easier part: as long as the factory (or any other industrial sector) have mains and ground-point different from residential and office buildings, milder Class-A limits applies to each device (milder for both radiated and conductive EMI). If this condition is not fulfilled, device is classified as Class-B and limits – if defined – are same as for standard devices.

- **Fusing, inrush limiting and protections:** Fuses have to safely break the circuit in every situation. This refers to higher voltage rating and because industrial mains have lower impedance, to higher breaking current capability too. As PSUs usually have some sort of capacitor bank, inrush current limiting must be secured, especially for voltage as high as 1 $kV_{DC}$. Protections depends on design specification, but output overload, input undervoltage and thermal are common for most of them.

SiC devices are usually used in industrial sector for high power application like motor control or already mentioned primary power supplies. Idea of this thesis is to analyze their usage in auxiliary power supplies, because in this field Si devices are still mostly used and according to specification, SiC might be better.

# 2 Flyback design

Converter designed in this thesis was developed in cooperation with STMicroelectronics as a prototype for testing SiC MOSFETs and as a potential evaluation board. Therefore, mostly ST semiconductors were used and tested. However, (as declared above) all designs, layouts and measurements were made by the author.

For evaluation purposes the board had to be easily modifiable, all parts accessible and versatile for another design ideas. Usage in industrial sector requires ultra-wide input range, besides fulfilling electromagnetic interference limits, even susceptibility must be particularly considered.

**Parameters:**

Input voltage: 150 $V_{DC}$ – 1 $kV_{DC}$; 180 – 690 $V_{AC}$

Output: 24 $V_{DC}$; 100 W; reinforced isolation

Besides smaller prototypes and special testing boards, two PCB designs were made. Gerber data for both of them are attached – \Attachments\Boards\v1 and \v2. First one was used as beta version for EMI optimisation, also few minor problems were solved using this board. Second version is the final version and – as I believe – flawless. Unless noted otherwise, v1 PCB was used for measurements (especially all presented efficiency data – they might slightly differ because of minor changes in the input section).

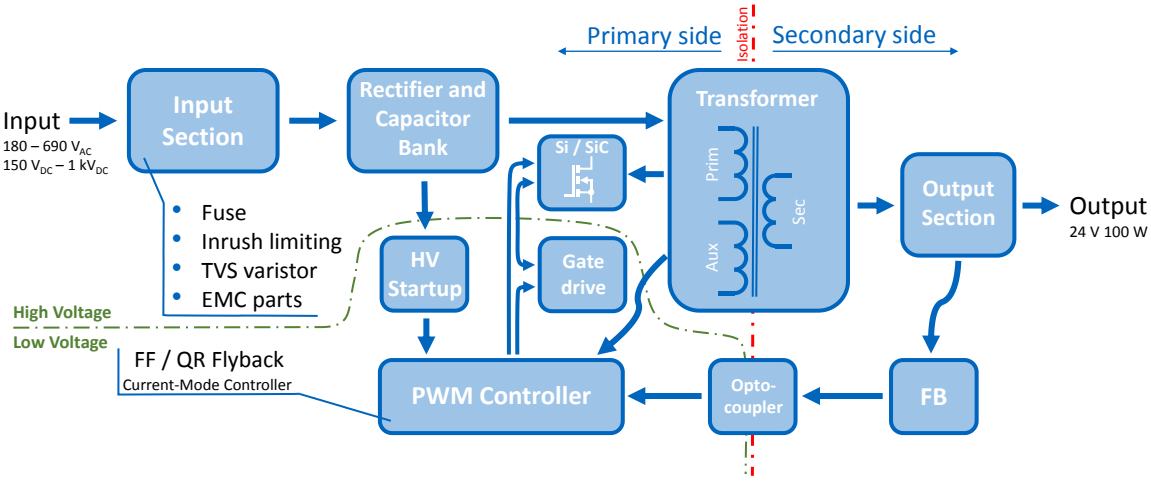



*Figure 4 Block diagram of designed converter*

Figure 4 simply describes designed converter. It's standard flyback topology, primary designed and tested for fixed-frequency operation, but also – revealed in subchapter 0– quasi-resonant mode was tested. It consists of three main (mostly independent) voltage circuits. First one in order of appearance from input is Primary side's High Voltage section (further under the abbreviation HV). This does not refer to definition of high voltage mains (≥ 1 $kV_{AC}$ or 1.5 $kV_{DC}$), but since the voltage potential to internal ground is usually times higher than in any other section (in this case almost 100times) there's a convention to call it *High Voltage*. It provides power distribution to the rest of the converter (except startup sequence) through main transformer.

Second circuit is Primary side's Low Voltage section (abbr. LV), from where the controller is powered and it also drives the power MOSFET. It's not isolated from HV (shares common ground) and during startup is directly powered from it via linear regulator (HV startup,

described in 2.3.1). Not so long after converter starts switching, auxiliary winding starts providing sufficient voltage and LV section is powered from it. The third circuit is the secondary side. This is the only stabilized voltage circuit (via feedback; abbr. FB) – input voltage is given and LV voltage is defined by auxiliary voltage (which consist of secondary winding voltage and transient voltage spikes) thus it can vary a lot. The secondary side is also isolated, so even the FB needs isolation, which is secured with standard optocoupler.

## 2.1 Brief review of Flyback operation

Flyback topology is one of the off-line converters category, mostly used for low-power applications up to 100 W. It is one-switch converter derived from buck-boost topology as its isolated version. Instead of other one-switch off-line converter – forward – it uses its *magnetic* for storing energy during on-time and discharging it to the output during off-time; forward uses magnetic as a transformer: during on-time primary voltage is transferred to the output according to Faraday's law, core flux is demagnetized during off-time. I wrote flyback *magnetic* instead of *transformer* intentionally: buck-boost uses an inductor to store energy and flyback does the very same thing, the only difference is another winding used for discharging this energy; it doesn't use Faraday's law (applied for transformers) for its primary purpose. Technically, as this component exists, flyback magnetic can be called *coupled inductor*, but I will use the standard term: flyback transformer (from any point of view except nomenclature there's no difference between them). What is more, while magnetic have more than one winding Faraday's law applies in every case, no matter if its use for energy transfer or not – so using term *flyback transformer* is definitely correct.

[21] [24]

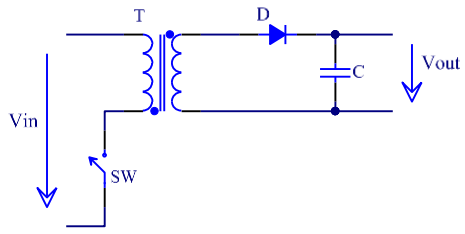



*Figure 5 Simplified flyback schematic*

Just to clarify a few terms used in this thesis, this paragraph summarizes flyback function. Principle schematic is shown in Figure 5. On the primary side (left), switch (MOSFET) turns on and starts charging the transformer **core flux Φ**, also the voltage applied to the winding $\mathbf{V_{prim}}$ is **reflected** according to Faraday's law with transformer **turn ratio n** to the secondary side as $\mathbf{V_{sec\_R}}$. According to switch state, two parts of each cycle are defined: **on-time** $\mathbf{t_{on}}$ and **off-time** $\mathbf{t_{off}}$; together forms **period** $\mathbf{T = t_{on} + t_{off} = 1/f_{SW}}$, where $\mathbf{f_{SW}}$ is **switching frequency**. During on-time, **output diode D** is reverse-biased, during off-time core flux is demagnetized through output diode into **output capacitor C**. Also part of off-time can be idle time $\mathbf{t_{res}}$: this represents the rest of off-time after the core is fully demagnetized and before the start of next on-time. During demagnetization, secondary winding acts like a current source of $\mathbf{i_{sec(t)}}$, which causes secondary winding voltage $\mathbf{V_{sec}}$ and its **reflection** to primary $\mathbf{V_{prim\_R}}$.

## 2.2 Input section

Every component had to fulfill voltage rating. Starting with input connector, then fuse, inrush current limiting NTC's, capacitors, surge protecting varistor, common mode choke and bridge rectifier. Picking a proper fuse was quite tricky – as written above, it must withstand inrush current while 1 kV is connected, but also current breaking capability must be sufficient.

For evaluation purposes standard sized fuses (e.g. 5x20 mm) are the best option, unfortunately, none of those had 1 $kV_{DC}$ rating – besides voltage value, especially classification for breaking DC not so many of them have. As a compromise, 2A ultra-fast 6,3x32 mm fuse with combined holder also for 5x20 mm was tested and used in the v1 version, but failed. After that, the only acceptable fuse cartridge (used in v2) with 1 kV rating is industrial 10x38 mm. Fuse selected was Littelfuse SPF 8A: it fulfils 1 $kV_{DC}$ rating and its current breaking capability is 20 kA, which refers for 1 $kV_{DC}$ input to overall impedance of short circuit and mains equal or higher than 50 mΩ, which I firmly believe is safe enough. Figure 6 shows the input section (without input capacitor bank connected to nets V+ and GND).

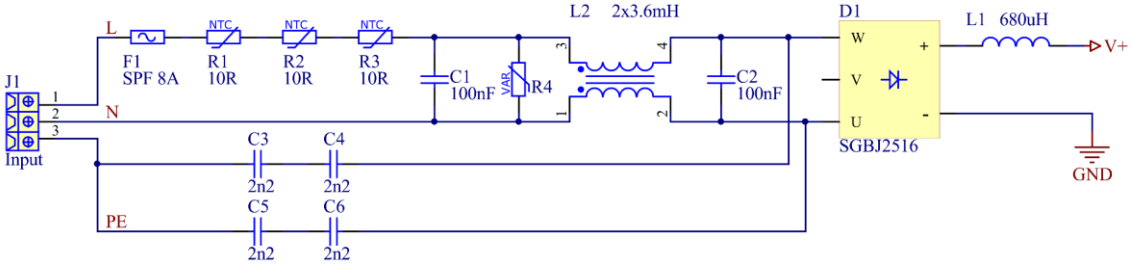



*Figure 6 Input section*

For inrush current limiting NTCs R1-R3 and choke L1 are used (L1 is also used as differential mode choke for EMC optimisation). There are three NTCs because of the voltage rating: 265 $V_{AC}$ for used EPCOS NTCs, which equals to amplitude of approx. 375 $V_{DC}$. For transient voltage suppressing varistor Littelfuse V1000LA160 was used with peak current rating 6,5 kA. EMI filter consist of C1-C6 and L2, this problematic is discussed in section 2.6. Instead of diodes 3-phase input bridge was selected to save space on the PCB, also it may be helpful for 3-phase adjustment.

Because input range starts at 180 $V_{AC}$, from known parameters input capacitance was calculated ≥40 µF (for 50Hz mains). Considering PCB requirements, two 68 µF / 400 V capacitors in parallel were put 3times in series, each pair is balanced with two 1206 SMD resistors in series (voltage rating of 1206 package is usually 200 or 250 V). Capacitor bank is shown in Figure 7 in section 2.3.1.

## 2.3 Chip selection

For versatility same as for high voltage the best option was the ST's L6566BH multimode controller. It allows both Fixed frequency (FF) and Quasi-resonant (QR) operation. Switching frequency during FF operation can be set by one resistor, same as maximum switching frequency for QR mode. It also includes many other features, like output overvoltage protection and input undervoltage protection useful for industrial power supplies.

[10]

### 2.3.1 High voltage startup

Although L6566BH's integrated high voltage startup allows 840 V as an absolute maximum rating, for this application it's still not enough. For this purpose, the circuit shown in Figure 7 was developed. Transistor Q1 acts as a simple voltage follower of voltage divided by input capacitors, approx. ⅔ of V+. While internal HV startup charging the VCC capacitor ($I_{MAX}$ 1.6 mA), the channel of Q1 is opened (Q1's threshold current is 250 µA) and acts as typical voltage follower.

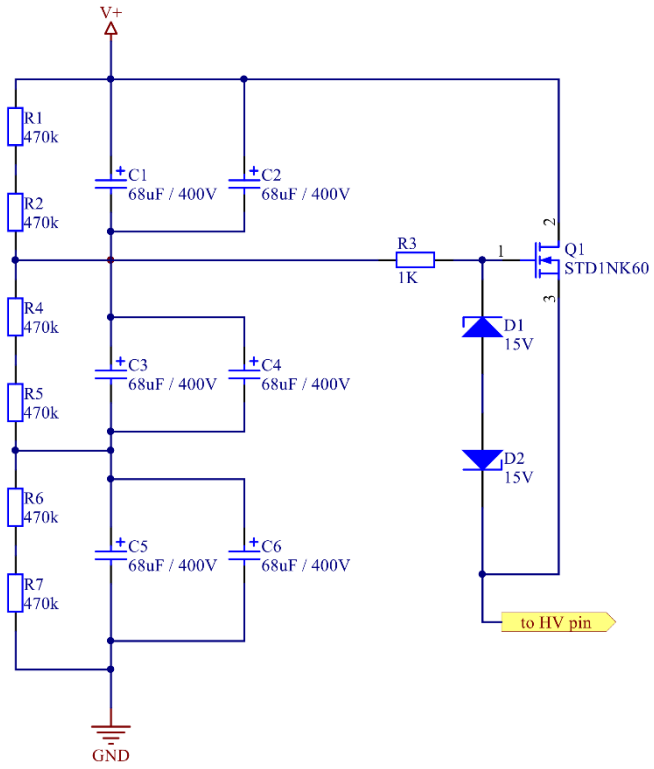



*Figure 7 HV startup circuit*

During off state HV pin voltage is biased only by leakage currents. Because those can variate by decades, it is necessary to protect both Q1 and HV pin by clamping Zener diodes D1 and D2.

Resistor R3 just fulfils the function of additional impedance in case of any voltage surges. It shouldn't affect any other function, only leakage currents may flow through, if any.

Technically, it is possible to connect HV pin directly between capacitors, but that's not fault-proof. It was tested, that if in case of some malfunction L6566BH's VCC is being continuously discharged and thus charged with HV pin, it unbalances the capacitors beyond safety limits. HV is not designed to provide power continuously, but failure of IC is still more acceptable than possible explosion of electrolytic capacitors.

[10] [11]

### 2.3.2 Soft-start and OCP

L6566BH uses one capacitor (connected to SS pin) for both soft-start and overcurrent protection. While starting, this capacitor is charged from zero voltage with current

$i_{SS}$ = 20 µA (typ.). Once $V_{SS}$ reaches 2 V, soft-start ends. During this period, setpoint for primary winding current rises from zero to maximum.

After soft-start, voltage stays at 2 V until overcurrent appears. If it does, capacitor is charged again with current exactly one quarter of the soft-start current $i_{SS}$. If overcurrent lasts long enough that $V_{SS}$ reaches 5 V, device stops switching. This allows covering the short-time overloading.

Even if this is quite handy feature for usual design, in this case it's not. During soft-start, L6566BH completely ignores COMP pin, to which feedback's optocoupler is connected. Also, while starting (output voltage is close to zero) converter operates in continuous-conduction mode. During on-time and for constant voltage, current through primary inductance can be described by following equation:

$$\frac{di_{(t)}}{dt} = \frac{v_{(t)}}{L} \rightarrow \Delta i_{Lprim} = V_{prim} \cdot \frac{t_{on}}{L_{prim}} \quad (1)$$

During off-time $t_{off}$ the core flux is being demagnetized into output according to the same equation (1), only transferred to the output: $t_{on} \rightarrow t_{off}$; $prim \rightarrow sec$. While starting output voltage is presumed equal 0 V, thus $V$ in the equation represents just voltage drop on output diode and series resistances. (This is very simplified – e.g. no rise of the output voltage is counted in – but for demonstration purposes it's ok.) Hence even for short $t_{on}$ during startup core flux might not be fully demagnetized into output. To be exact, the continuous-conduction mode does not have to occur by definition, but it does because of the design parameters (demonstrated in Figure 8: in the middle is the 16th pulse and already in *quite deep*[2] CCM).

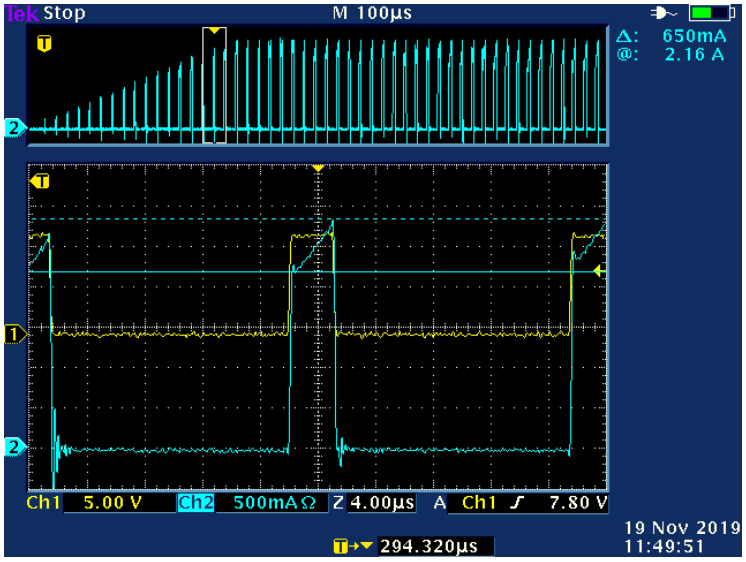



*Figure 8 CCM while starting (in: 150 $V_{DC}$,; loaded)* ***Yellow*** *–* $V_{GS}$ ***Blue*** *-* $I_D$

On-time $t_{on}$ (to reach current setpoint) is inversely proportional to $V$, which is given by input voltage: for highest $V_{IN}$ is the shortest, for lowest the longest. Considering FF operation, shorter on-time means longer off-time. Therefore, for higher input voltage a higher amount of core flux can demagnetized into output current during off-time. Because of that, output voltage reaches its nominal value faster. This also variates depending on load: for no load just output capacitors are charged and output voltage rises much faster. In every case must soft-start ends before nominal output voltage appears (most critical is 1 kV input and no-load), otherwise (because L6566BH ignores COMP pin), overvoltage occurs, which is no doubt insufficient condition.

To prevent this, it is obvious that soft-start time must be set for maximum input voltage and no load, therefore for other conditions overload state is triggered. This can last maximum

[2] *Quite deep* according to $\Delta I_{prim}/I_{prim\_avg}$

6times longer than soft-start (SS capacitor is charged from 2 to 5 V with quarter current). The most extreme conditions are 1 kV input and no-load (as mentioned above) and 150 V input and full-load.

In QR mode, instead of CCM during soft-start and DCM later, converter senses core demagnetization and then switches. Hence problem with soft-start is quite different, but still based on similar principle. To reach current setpoint, $t_{on}$ is again inversely proportional to input voltage. Equation (1) for $t_{on}$ is still valid, but with one difference: each period $i_{Lprim}$ rises from zero to current setpoint. Nevertheless, for each current setpoint $t_{off}$ is independent of input voltage. Off-time is defined by equation (2) where $i_{Loff}$ is the actual value of primary winding current when transistor turns off and $V_{sec}$ is voltage on secondary winding (actual output voltage + diode forward voltage drop) and $n$ turns ratio.

$$t_{off} = \frac{\Delta i_{Lsec} \cdot L_{sec}}{V_{sec}} = \frac{n \cdot i_{Loff} \cdot \frac{L_{prim}}{n^2}}{V_{sec}} = \frac{i_{Loff} \cdot L_{prim}}{V_{sec} \cdot n} \tag{2}$$

While sensing the core demagnetization, it's for sure that $\Delta i_{Lsec}$ drops down to zero, so it is correct to substitute $\Delta i_{Lsec}$ with $n \cdot i_{Loff}$ (considering ideal coupling). From equations (1) and (2) is obvious that not off-time but frequency changes. Besides this difference, soft-start problem for QR mode is the same: for higher input voltage and less or zero load output voltage rises faster.

As it eventuated from measurements and testing, soft-start capacitor could be designed for one exact board to cover all conditions, but because charging current $i_{SS}$ can differ up to ±30% it's impossible to design one exact value with safe margins. In other words, one exact capacitor was found suitable for one exact board to cover both extremes, but with nearly no margin. Any variation even within capacitor tolerance may lead to malfunction. Utility designed to resolve the problem is demonstrated in Figure 9: this circuit allows to separate these two functions. Capacitor C3 acts as usual soft-start capacitor and it's calculated to cover high input voltage and no-load cases. With fully loaded output and/or lower input voltage OCP is triggered. After reaching approx. 3.1 V (Vref/2 + $U_{D2}$), soft start current starts charging divider consisting of C4 and C1. L6566BH's pin Vref is sink-source, so even if this current (5 µA typ., 6.5 µA max) would make any difference, it wouldn't matter. The function of D1 is described in the next paragraph. D2 is standard diode instead of Schottky diode for one simple reason: leakage current of ceramic capacitors C1 and C4 wouldn't balance the divider quick enough. While they are imbalanced after startup, any other short-durational overloading triggers immediately overload protection. To prevent this, balance resistors might be connected in parallel with capacitors, or D2 should be standard diode: as they have times higher reverse leakage current than Schottky diodes, capacitor divider is discharged back to balance.

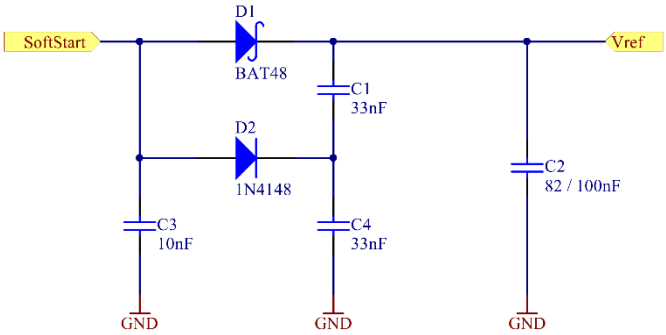



*Figure 9 Soft-start circuit*

D1 can be used to set preferable state: as described in L6566BH's datasheet [10] both overvoltage and overcurrent protections can lead to auto-restart or latch. If the protection is triggered, IC stops switching and waits until VCC falls below the turn-off threshold and proceeds to a new start-up sequence. In case auto-restart is enabled, then starts switching again, otherwise stays latched until it's restarted externally (disconnecting mains, discharging VCC to zero, etc.).

Auto-restart for OCP is enabled by clamping SS pin to less than 6.4 V (typ.), e.g. to $V_{REF}$ pin which is implemented with D1 in Figure 9.

[10] [12]

## 2.4 Flyback transformer

Design of flyback transformer is good example of multiple-criteria problematic: core size, core magnetic, turns ratio, wire diameter, isolation, layers (interleaved or non-interleaved), also radiated EMI problematic may be included (shielding, start of winding, orientation). Professional flyback transformers are designed via software including all these parameters, but it can be also calculated and designed with good precision using only few equations.

In flyback design many components are bounded together, including transformer: from transformer parameters ratings for primary switch (i.e. Si / SiC MOSFET in this case) and output diode are defined. MOSFET maximum Drain-Source voltage and diode reverse voltage are defined with turns ratio. Turns ratio can define duty cycle, to which are bounded peak currents for both transistor and diode. To calculate the transformer, following parameters are necessary:

- **Switching frequency:** switching losses are proportional to switching frequency, but increase with the square of input voltage. Since input voltage is up to 1 kV, in order to minimizing them switching frequency was selected quite lower: **$f_{SW}$ = 51,3 kHz**
- **Mode of operation: Discontinuous, Fixed-Frequency**
- **Input voltage: 150 V – 1 kV**
- **Output: 24 V, 100 W**

There are many approaches to calculate flyback transformer, often working with voltage related equations (e.g. [24]), but I prefer the approach from the current point of view. Many parameters have been neglected in order of simplicity and are discussed later. As first should be mentioned transformer coupling factor: until further notice, it's considered ideal, i.e. k = 1.

It is wise to set maximum power as a boundary condition to DCM, then parameters bounded with duty cycle can be defined easily. Considering linear permeability thus linear inductance, both primary and secondary winding currents have a triangular shape – Figure 10.

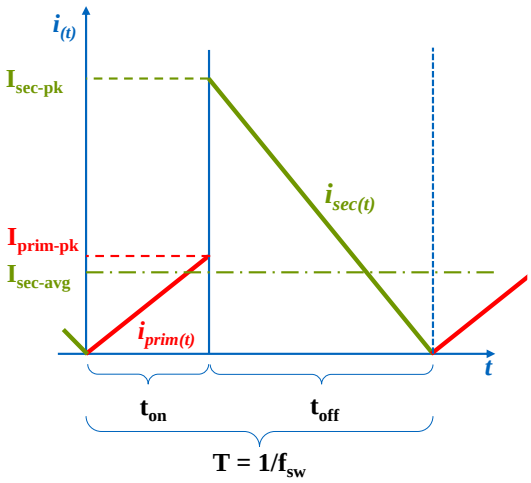



*Figure 10 Currents in boundary DCM*

### 2.4.1 Transformer calculation with consideration to other components

Because of DCM, the output power can be determined as inductor energy per time, i.e. multiplied by switching frequency:

$$P_{sec} = \frac{1}{2} {I_{sec-pk}}^2 \cdot L_{sec} \cdot f_{sw} \tag{3}$$

$P_{sec}$ stands for power provided by secondary winding, i.e. output power $P_{out}$ + all losses on the secondary side (mainly on output diode). While those losses are almost purely voltage drops and not leakage currents (current for feedback is neglected), output current $I_{out}$ equals to secondary winding average current (substituting with eq. (1) and eq. (3)):

$$I_{sec-avg} = \frac{P_{sec}}{U_{sec}} = \frac{1}{2U_{sec}} {I_{sec-pk}}^2 \cdot L_{sec} \cdot f_{sw} = \frac{1}{2U_{sec}} {I_{sec-pk}}^2 \cdot \frac{t_{off} \cdot U_{sec}}{I_{sec-pk}} \cdot f_{sw} = \tag{4}$$
$$= \frac{1}{2\cancel{U_{sec}}} {I_{sec-pk}}^{\cancel{2}} \cdot \frac{t_{off} \cdot \cancel{U_{sec}}}{\cancel{I_{sec-pk}}} \cdot \frac{1}{T} = \frac{1}{2} \cdot \frac{t_{off}}{T} \cdot I_{sec-pk}$$

It is obvious from Figure 10 that $I_{sec-avg}$ because of a triangular shape is equal to ½ of $I_{sec-pk}$ during $t_{off}$ and $t_{off}/T$ is just averaging over the whole period. Since core flux is caused by current through primary winding, $I_{prim}$ and $I_{sec}$ are proportional with turns ratio ($N$ means number of turns):

$$I_{sec-pk} = n \cdot I_{prim-pk};\ n = \frac{N_{prim}}{N_{sec}} \tag{5}$$

and as magnetic flux unit Weber can be written as V·s, duty cycle $D$ can be calculated as:

$$D = \frac{t_{on}}{T} = \frac{n \cdot V_{sec}}{n \cdot V_{sec} + V_{in}} \tag{6}$$

All equations above presumed ideal state and only output diode losses were included. Now from required output parameters output current Isec can be calculated according to (4). It is wise to include all losses (estimated or calculated) and add them with some power margin (e.g. 10%) to $P_{sec}$: in case that the converter is loaded during startup with nominal load, due to low output voltage core can't be properly demagnetized and converter couldn't start. Also power consumption from any other winding (auxiliary in this case) must be included. Setting this increased $P_{sec}$ to boundary condition of DCM requires one more parameter: the input voltage for equation (1). This should be set for minimum operating voltage, therefore for any higher voltage on-time for current setpoint shortens, so operation in DCM is guaranteed.

All these parameters are bounded with duty cycle and/or turns ratio; the best way to select them is with series of iterations. Also reflected voltages are bounded with them, therefore in this part of transformer design it is good to focus on primary side MOSFET and output diode too. Current relations are defined in equations above; maximum diode voltage $V_D$ is:

$$V_D = V_{sec-R(max)} + V_{out} = \frac{V_{in(max)}}{n} + V_{out} \tag{7}$$

For MOSFET voltage rating it's necessary to include transformer leakage inductance (coupling factor $k < 1$). This is caused by non-ideal coupling between primary and secondary winding, from circuit point of view it's correct to include it as another inductance put in series with primary inductance. It means that it's charged with primary inductance, but not discharged into output, therefore it must be discharged in different way. There are two common options – called snubber – to secure this, first is parallel RC combination, second is transil; both with diode in series to dissipate only the energy from leakage inductance. Transformer is usually designed to have leakage inductance in range 1.5 – 3%, so discharging leakage inductance in short time is presumed. In first circuit, the energy is mostly transferred to the capacitor and in the rest of off-time dissipated on the resistor. The disadvantage is – besides sometimes worse efficiency – that leakage inductance can slightly vary, thus can its energy and so the maximum capacitor voltage: maximum snubber voltage can be only estimated, not defined. Second option – transil – defines

the maximum snubber voltage nearly independent of dissipated current. Because this design often nears to the limits of safe operation, this is quite necessary. Transil should be selected for: a) safely discharging leakage inductance; b) having as small as possible leakage current with applied $V_{prim\text{-}R}$ (for efficiency reason). Overall MOSFET voltage is $V_{in(max)} + V_{snubber}$.

Voltage reflected on primary winding ($V_{prim\text{-}R}$) during demagnetizing through secondary is proportional to turns ratio:

$$V_{prim-R} = n \cdot V_{sec} \tag{8}$$

It is obvious that some compromise must be done: there is an effort to lower maximum rated voltage for both components (for lower price and better parameters), but for diode it means maximizing turns ratio (eq. (7)), but for MOSFET the opposite (eq. (8)). For the same reason it is wise to minimize effective / average currents though them – and this also refers to the exact opposite rule of turns ratio for both of them (eq. (5)).

In design like this, where output diode power dissipation is not negligible, component selection tends to Schottky output diode instead of standard one. In general, Schottky diodes have absolute maximum reverse voltage 200 V or lower, for operation conditions (i.e. ~80% of AMR) 160 V. This actually makes design slightly easier: one parameter is defined and iterations to select the best duty cycle or turns ratio have one value to relate to. From this parameter and defined parameters equation (7) can be calculated: turns ratio n = 7,35, which means that n ≥ 7,35 have to be used for Schottky diode. All other parameters mentioned above can now either be calculated or are already defined.

### 2.4.2 Core, bobbin and wire selection

As parameters written above were all bounded together, core, bobbin and used wires are bounded similarly. Since primary inductance and its current is defined, the only core limit is maximum magnetic flux density[3] $B_{max}$. As written in the beginning of this subchapter, linear permeability was considered for all calculations. To obtain this, core magnetic flux density B must be lower than $B_{sat}$. More precisely, permeability is dependent on B (so is inductance), but for B nearing $B_{sat}$, permeability starts decreasing rapidly (depends on used core material). This is called core saturation and $B_{sat}$ is usually defined for 10% or 30% inductance / permeability loss. Including real-world parameters makes situation more complicated. Each core size defines bobbin on which wires are wounded. To minimize losses, wire must have some thickness and from calculations defined number of turns: it may easily happen that the windings simply didn't fit into the bobbin. Same as in previous part, a few iterations are needed to find the best solution.

Before focusing on wires, it's necessary to calculate magnetic flux density to see if selected core can be used (or – if feasible – it needs iterations for ideal air gap). Just a reminder, equations and relations presented here are just simplifications – more or less – valid for flyback transformer design; overall magnetic relations are more complex. First, leakage inductance is neglected again, so inductor linkage flux[4] is presumed equal to: $\Psi = N \cdot \Phi$; even if this is not matter-of-fact [21]. Using this, inductance can be defined from core parameters as shown in equation (9) ($A$ is core cross-section area, $l$ is core effective length and $\mu$ is core permeability):

$$L = N^2 \cdot \mu \cdot \frac{A}{l}\,; L = N^2 \cdot A_l \tag{9}$$

The right part of equation (9) is just it's modification (used also in this design) where $A_l$ is inductance factor. The un-modified equation includes permeability, which can be seen as

[3] This is also called just *B-field* [24], I would rather stick to more precise name *magnetic flux density* [20]
[4] Also marked as $\lambda$ sometimes

function of temperature or magnetic field strength (*H*), thus inductor current: if any simulator is used for the design, this allows to calculate inductance more precisely for magnetic flux density nearing to $B_{max}$. If core with air gap is used (bellow is mentioned why it's purposeful for flyback), this equation is still valid, only it's easier to calculate using reluctance. Nevertheless, it leads to cross section of the air gap.

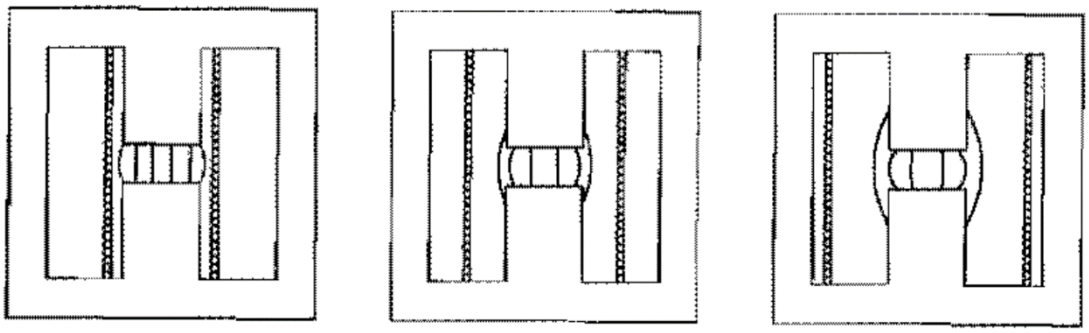


*Figure 11 Magnetic field vectors in air gap; credit: [25]*

One of many estimations made – and yet not named – is considering core permeability much higher than air permeability, so the magnetic can be described as *discrete* circuit: that means magnetic field is limited by core dimensions, thus all vector loops are inside the core. This can't be used for any air magnetic circuit (including air gap), because it has no borders. In Figure 11 is demonstrated how magnetic field vectors can change depending on winding distance. In this case modified or non-modified version of equation (9) can be used: inductance factor ($A_l$) is defined by manufacturer for each air gap. It is also possible to estimate or calculate air gap reluctance, but in neither case can inductance be calculated just as function of current (just from permeability function): with permeability loss also both of these parameters change.

Two previous paragraphs outline one of many phenomena of flyback transformer design. As far as I'm familiar with this problematic or as it can be found in the listed literature in Bibliography & Sources, there are only two ways of design: using same or similar equations as I present in this thesis (including more or less parameters and estimating the effect of the rest), or design aided by simulation tools, mostly of magnetic behavior. Therefore: in this case phenomena like mentioned above can be taken into consideration, but not precisely calculated. Estimating discrete magnetic again, core flux density is given by following equation:

$$B = \frac{L \cdot I}{N \cdot A} \tag{10}$$

where *A* is effective core cross-section area. If equation (9) is substituted into (10), it can be demonstrated why it's useful to choose core with air gap:

$$B = \frac{L \cdot I}{N \cdot A} = \frac{N^2 \cdot A_l \cdot I}{N \cdot A} = \frac{N \cdot A_l \cdot I}{A} \tag{11}$$

Since inductance and current are defined from section 2.4.1, core air gap can be set for minimum core flux density. As *B* is proportional to number of turns, inductance increases with $N^2$ so preferred value can be set. Back to the bounded parameters idea: minimizing *B* is good because of lower hysteretic losses and it also provides capacity for potential overloading, but more turns means longer wire, thus bigger parasitic resistance.

Not only wire length must be included into winding losses – skin effect (current displacing to the wire surface due to eddy currents; principle shown in Figure 12) can be a major issue. Proper calculation includes Kelvin's equation, which is Bessel function of a complex argument. Whole calculation is possible only directly from Maxwell's equations and not necessary for demonstration of the problematic [21]. The limit state for wire gauge is considered as $\delta = d/2$; where $d$ is wire diameter and $\delta$ is skin depth defined as:

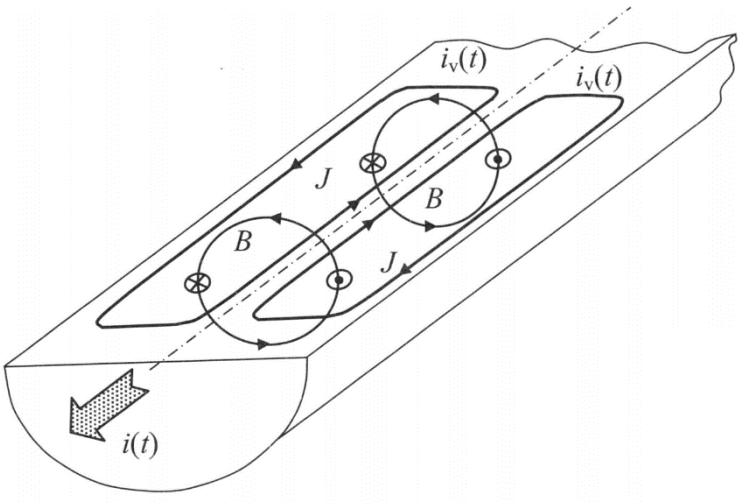



*Figure 12 Skin effect in round wire; credit: [21]*

$$\delta = \sqrt{\frac{2\rho}{\omega \cdot \mu}} \tag{12}$$

modified to the limit frequency:

$$f_{max} = \frac{4\rho}{\pi \cdot \mu \cdot d^2} \tag{13}$$

[21]

where $\rho$ is resistivity of used wire and $\mu$ its permeability ($\mu_{Cu} \approx \mu_0$).

This might be critical especially for secondary winding: as illustrated in Figure 10, high *di/dt* ratio is expected as primary-side MOSFET switches off. According to Fourier's series, higher harmonics are generated to achieve this shape. As secondary winding peak current may rise up to tens of amperes in this case, skin effect could negatively affect efficiency. It's recommended to choose wire diameter with $f_{max}$ at least 10times higher than fundamental harmonic, which period is $2 \cdot t_{off}$. As $f_{max}$ is inversely proportional to $d^2$, selecting proper gauge makes a big difference: $f_{max}$ is approx. 17 kHz for $d$ = 1 mm, but over 1,7 MHz for $d$ = 0,1 mm (copper wire, resistivity $\rho$ = 1,75 μΩ·cm).

Wire selection includes proper insulation. For basic isolation using insulating tape between windings is often sufficient as winding-to-winding insulation; distance between wires and any other conductor (another wire, ferrite core) must be fulfilled also. In this case standard double-coated wire can be used, but for reinforced isolation it is necessary to use triple insulated wire (TIW) at least for one side. Additional isolation layer worsens the insulation factor:

$$k_i = \frac{d_{Cu}^2}{d^2} \tag{14}$$

[21]

where $d_{Cu}$ is the conductor diameter (copper) and $d$ whole wire diameter. TIW wire requires more space in bobbin than standard wire and also increases leakage inductance: as there is space between turns (exactly $l_{space} = d - d_{Cu}$) magnetic field around wire can enclose the loop in this space which worsens the coupling with core.

Referring back to Figure 11 and to the previous paragraph (reinforced isolation is required), in designed transformer two main things worsen leakage inductance (besides air gap effect): using TIW and position of winding. Position effect can be reduced by interleaving the layers: half of primary – secondary – the rest of primary instead of stacking secondary over primary can make a difference. As in one-switch flyback topology leakage inductance energy is just dissipated, lowering it improves efficiency. This also includes another disadvantage: primary-to-secondary capacitance caused by transformer is nearly doubled. Besides of minor negative effect on efficiency, this might cause trouble for EMI; further discussed in subchapter 2.6.

[19] [20] [21] [24] [25]

### 2.4.3 Designed transformer

Output power 100 W is in general maximum power reasonable for one-switch flyback topology: as leakage inductance (typically ~3%) energy is only dissipated, another topology is adequate. To improve efficiency, interleaved transformer design was selected. For lower skin effect primary winding is wounded two times with thinner wire and secondary winding with litz: cable tangled from 100 µm wires. All specifications are below:

**Core:**
- Material: CF138
- Type: ETD34
- Gap: 1,1 mm
- $A_l$: 143 nH

**Primary:**
- $L_P$: 585,7 µH
- Turns: 64
- Wire: 2x TIW 0,2 mm

**Secondary:**
- $L_S$: 9,15 µH
- Turns: 8
- Wire: 6x Litz 40x 0,1 mm

**Auxiliary:**
- $L_P$: 3,58 µH
- Turns: 5
- Wire: 1x TIW 0,1 mm

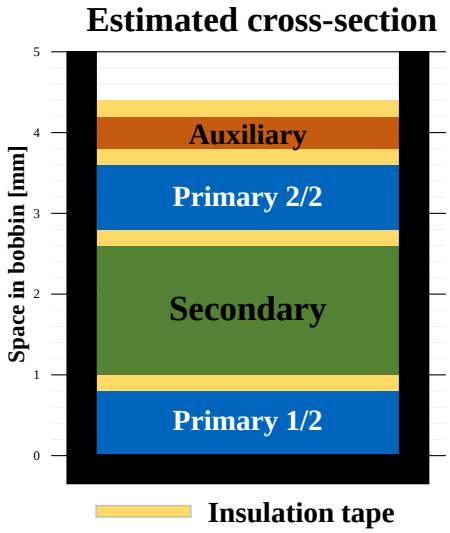



*Figure 13 Winding layers*

For minimum input voltage and from specification duty cycle $D = 56{,}9\%$ was calculated, primary winding peak current $I_{prim\text{-}pk} = 2{,}84\ A$, thus maximum magnetic flux density $B_{max} = 268\ mT$. For ETD34 is cross-section area $A = 97{,}1\ mm^2$ [26], but this number is the best achievable option: in case there is little offset between two halves of core this area decreases. For correction factor 0,9 $B_{max}$ grows up to approx. 300 mT. As illustrated in Figure 14, this is the maximum reasonable core flux density – as both permeability and $B_{max}$ are dependent on temperature, there must be some

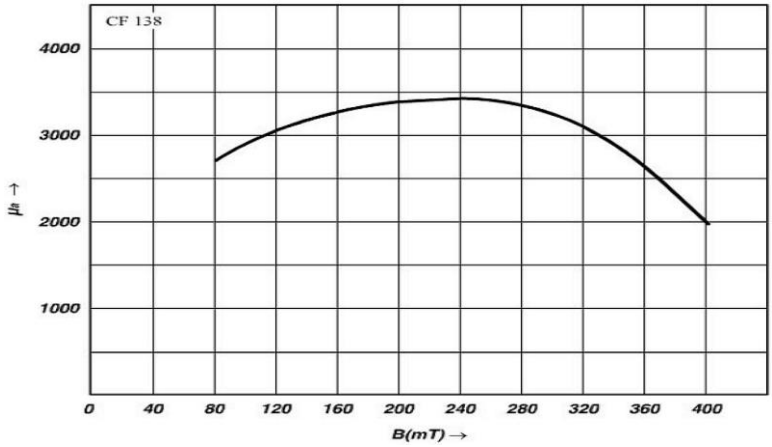



*Figure 14 CF138 permeability vs magnetic flux density; credit: [26]*

margin left. Output diode voltage drop was taken from datasheet [18] as 0,8 V, thus output current $I_{sec}$ = *4,89 A* for secondary winding peak current $I_{sec\text{-}pk}$ = *22,7 A*. As output power is defined 100 W, margin for losses and startup is 17,4 W (or %), which should be enough.

## 2.5 Final schematic and PCB layout

Final schematic is shown on the next page in Figure 16 or is located in \Attachments\Boards\v1 and \v2. This is the schematic for v2 board, the only difference from v1 is soft start circuit (discussed above in 2.3.2), first version had only SS capacitor. Also input section is slightly different: v2 was modified for final EMI components. As design was made for universal use and modifiability, many components are marked with *N/A* – not assembled. Photography of both boards is in Figure 15 – nearly the same schematic, layout slightly improved, very similar look.

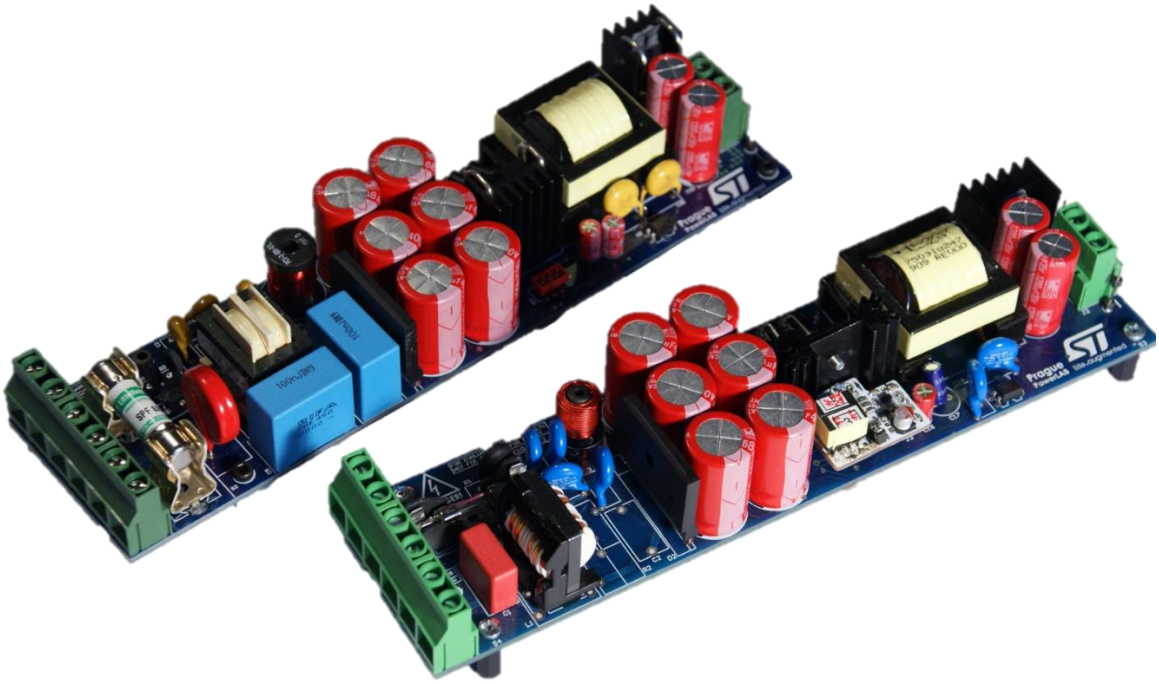


*Figure 15 Board v1 in the front with connected Gate-Drive module (revealed later in subchapter 3.2) and board v2 in the behind already with better fuse and final EMI components*

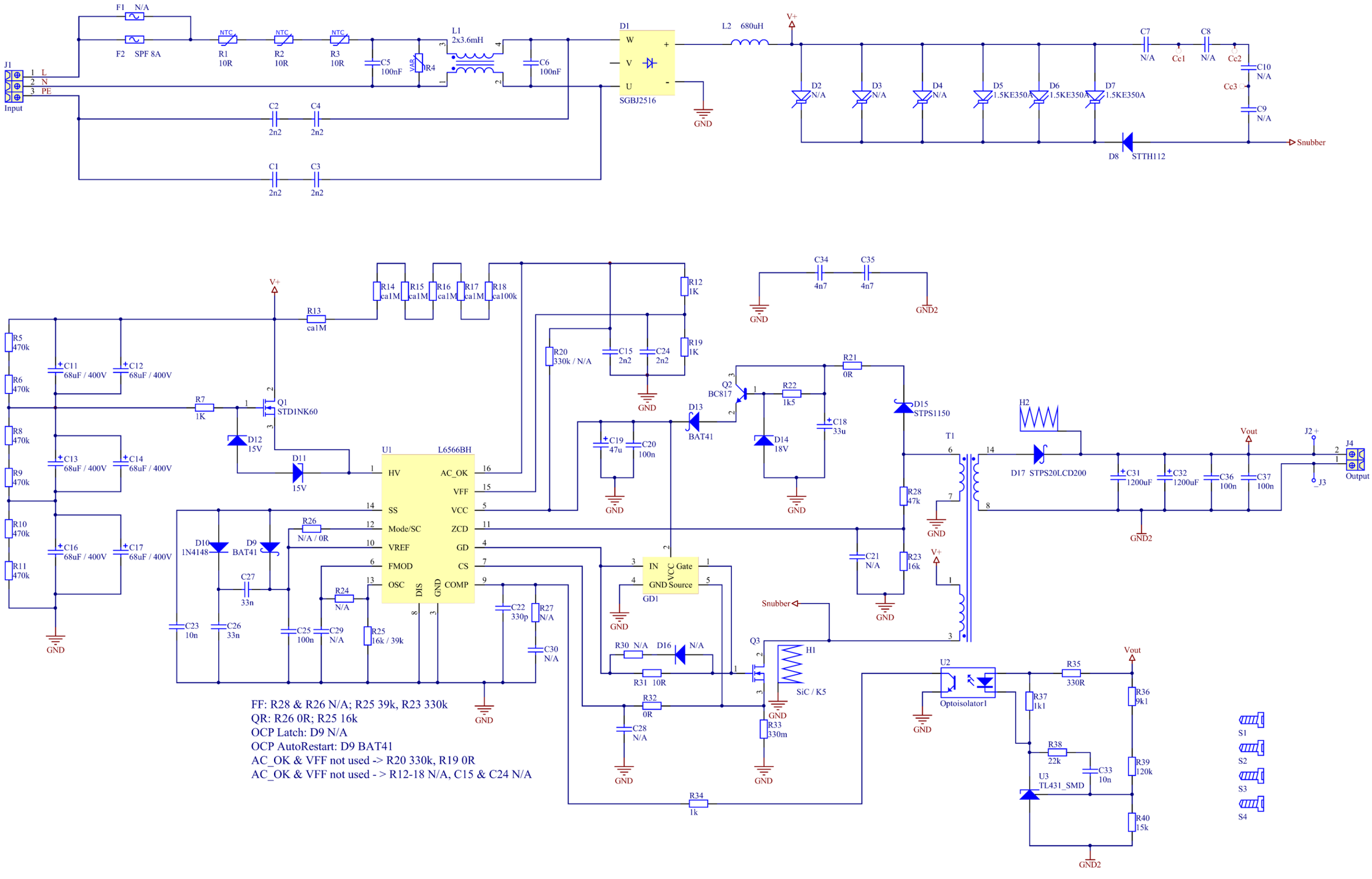



*Figure 16 Final schematic of flyback converter*

Both PCBs for v1 and v2 were routed in accordance with basic analog design rules, Primary side's LV ground is star-topology, the rest of design tends to daisy-chain topology according to the schematic (this is important especially for blocking capacitors). Primary side's LV and HV ground are connected together on the pad of the current sensing resistor for most precise current sensing. Special consideration was given to clearance according to applied voltage: input stage was routed with reinforces clearance and creepage, the rest with functional; between primary and secondary side both were optimized as wide as possible (on v2 board there is even a slot hole under optocoupler). All PCB GERBERs are located in \Attachments\Boards\v1 and \v2.

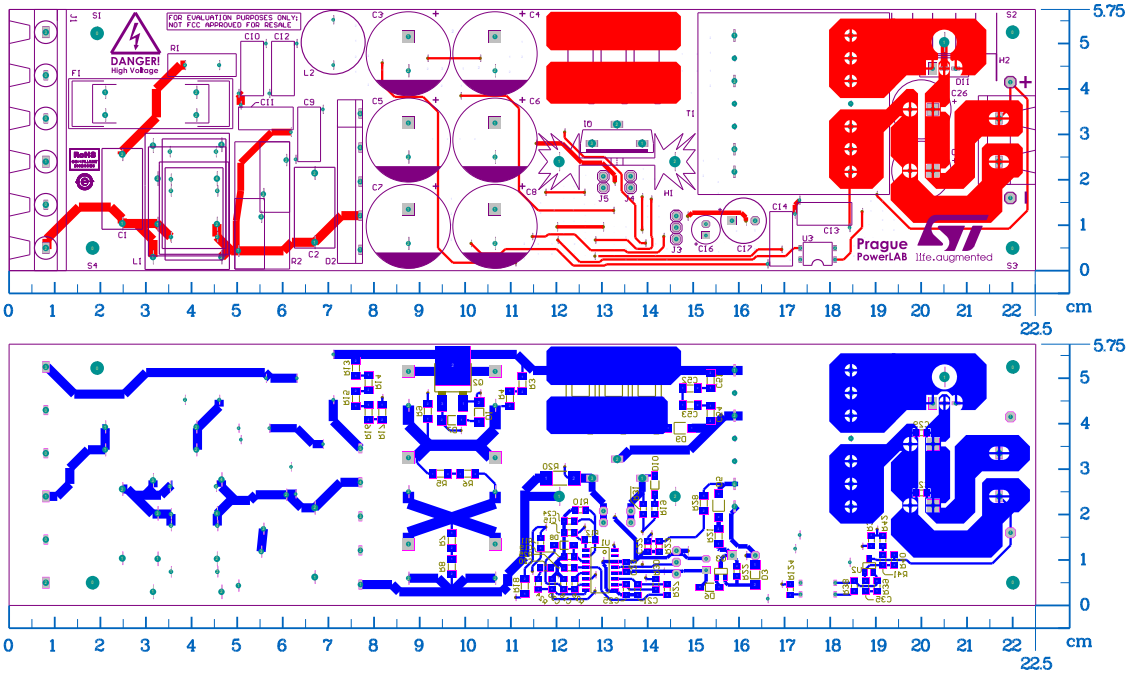



*Figure 17 PCB layout for v1 - TOP layers are on the top, BOT on the bottom (not mirrored)*

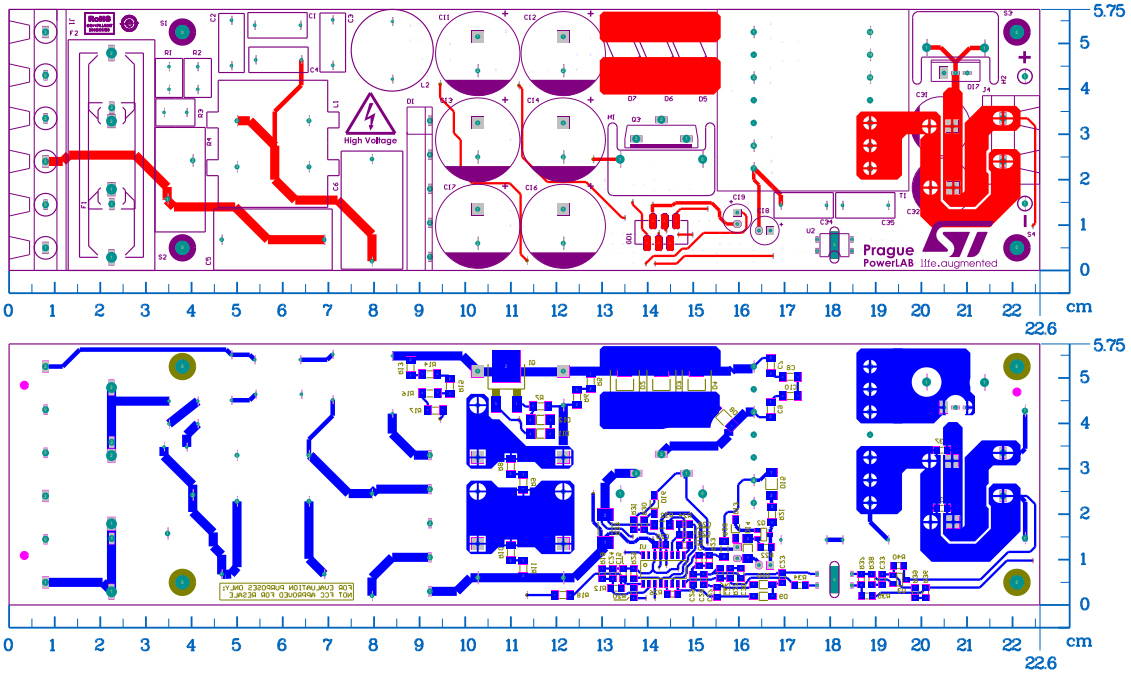



*Figure 18 PCB layout for v2 - TOP layers are on the top, BOT on the bottom (not mirrored)*

## 2.6 EMI optimization

This converter was designed for industrial usage; therefore, it must fulfill CISPR's EN 55011 standard [9]. As this converter creates radio-frequency interference as its side effect, it belongs to category 1. This category is further divided into classes A and B according to mains star point: if any residential or office building is connected to the same star point, Class-B limits must be fulfilled (which are same as for any other home or office device), otherwise Class-A limits applies (which allows to radiate higher values). As this is not defined by converter specification (and also for versatility purposes) design was optimized for rigorous Class-B limits. The design is only an evaluation board of auxiliary power supply: for non-laboratory usage (possible scenario after evaluating, testing and certification) it will be probably mounted together with another machinery parts in metal enclosure. Therefore, all EMI measurements focuses only for conductive, not for radiated EMI. Whole problematic was fine-tuned on v1 board, v2 board has final footprints for components listed below and in Bill of Materials.

As shown in Figure 6 or in Figure 16, input section contains components for standard EMI filter topology. Capacitors C1 – C4 are safety Y1 capacitors; because C5 and C6 are already fused, there's no necessity for class X safety rating. As common mode choke one of Coilcraft's 3750 Vrms was selected, again to fulfill voltage rating. Several chokes were tested, the best performance was made with E3502 combined with C5 and C6 both 100 nF. After proper component selection, conductive EMI was measured for input voltage 230 $V_{AC}$ and 100W load, shown in Figure 19:

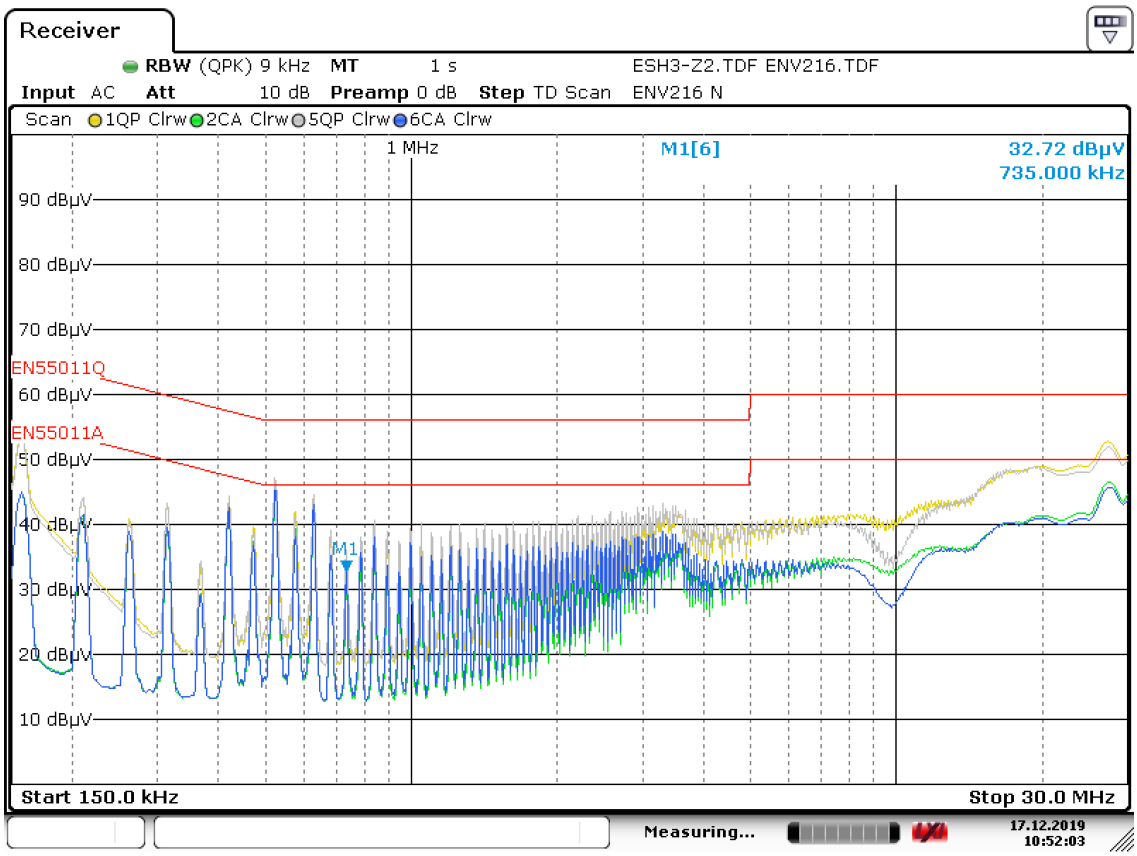



*Figure 19 Conductive EMI measurement; Yellow: Quasi-peak L, Green: Average L, Gray: Quasi-peak N, Blue: Average N*

### 2.6.1 Further improvements

As revealed in Figure 19, the design meets the EN 55011 EMI standard. It is also true that the margin to the limits for frequencies 500-650 kHz is not as extensive as preferable. Due to component tolerance and/or their aging (e.g. capacity loss for electrolytic capacitors) sooner or later the limits might be exceeded. Therefore, several ideas were tested for the possible third version, if solution on v2 would be found insufficient.

The first step was PCB design: this is the only cost-free option (besides testing same-cost components from different manufacturers). As mentioned above, the input section on the first v1 board was made for testing purpose, so universal or not big enough footprints were used. Furthermore, routing was made – as I firmly believe – properly. Therefore, I presume (and as written bellow based on measurement) that different input section routing on boards v1 and v2 have no effect at all on conductive EMI.

Additionally – what I believed that might have an effect – was input capacitor bank routing. As shown in Figure 20 – a), v1 was routed for optimal decomposition of switching current ripple stress. This topology allows to load capacitors in parallel nearly equally (this topic is discussed in [23]).

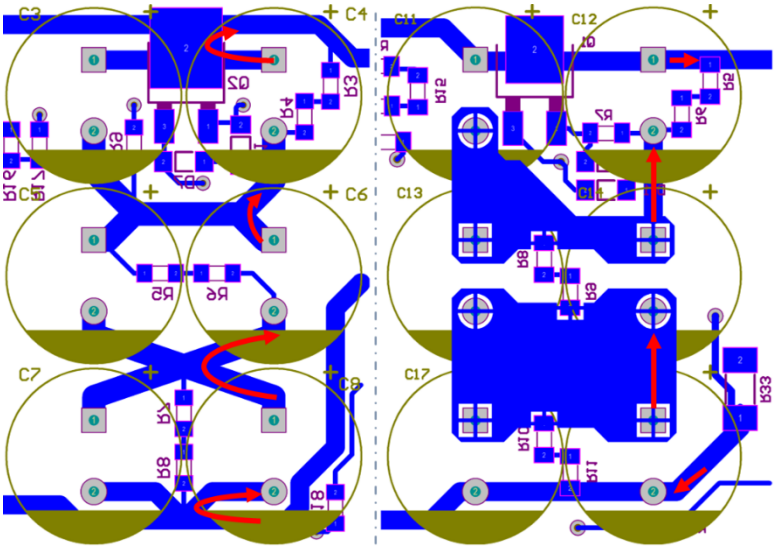



*Figure 20 - a) v1 routing* *b) v2 routing*

However, this adds parasitic inductances in series with capacitors and (what's worse) parasitic inductance between supply rails (V+, GND) and capacitor bank (estimated current flow is sketched with red arrows in Figure 20 Figure 20). That makes direct path for ripple from primary switch (on the right side) to the input section (on the left side) and capacitor bank is connected via branch. This effect shouldn't apply at all for switching frequency 51.3 kHz, but may negatively affect the EMI results for frequencies 500-650 kHz.

To confirm that, second board v2 was designed to minimize areas of parasitic inductances placing capacitor's pins directly into supply rails and connecting them with polygons instead of X- or H-shaped routes. Again, as demonstrated in Figure 20 – b) with red arrows, the ripple should be directly eliminated with the right side triple-series capacitors (as much as their parasitic inductance and resistance allows it) and then the rest with others on the left. This also causes undesirable disparity of stress on the first and second triplet, but mainly on higher frequencies and on switching frequency 51,3 kHz it should be negligible.

As the main problem seems to be the average and not the quasi-peak value, a further comparison is focused only on the average value. Also as traces for L and N are nearly the same for lower frequencies, only L are shown for better clarity.

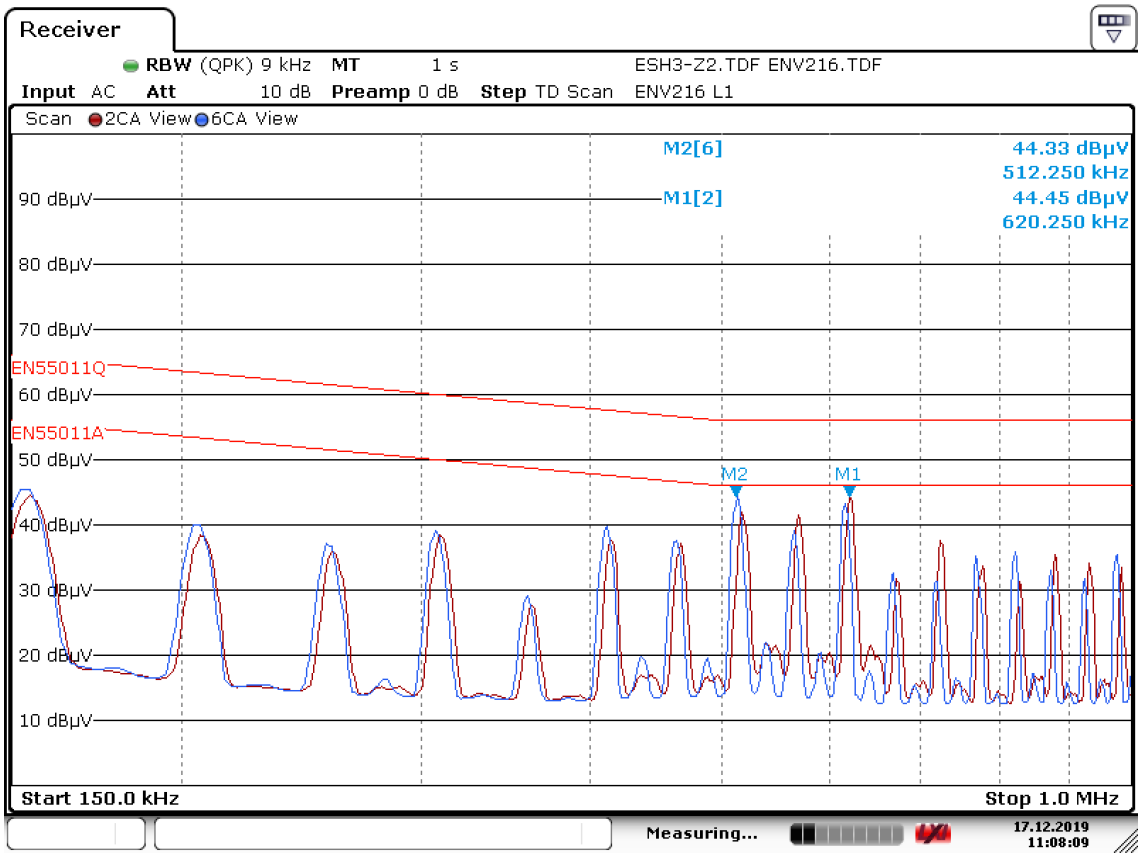



*Figure 21 PCBs EMI comparison: v1 – dark red (marker M1), v2 – blue (marker M2)*

New PCB layout made some difference, but instead of suppressing the problem it only transfers it to another frequency spike. As the amplitudes are almost identical (markers in Figure 21), the age-related question remains. Besides this effect v2 version has some differences on frequencies above 1 MHz, but as they are deeply below the limit, Figure 21 shows only range of interest.

After different layout didn't make huge difference, another focus was then on capacitor bank: quite common phenomenon of electrolytic capacitors is their low resonant frequency value, after which they show inductance behavior – impedance increases with frequency ([23]). This can be obtained by bypassing them with ceramic capacitors (typically 100 nF), because their resonant frequency is usually higher by orders. Unfortunately, used capacitors (Würth Elektronik 860241381006) have no simulation model or measured resonant frequency in their datasheet to verify this theory. Additionally, it was disproved with measurement – for frequencies around 1 MHz was approx. 1dB drop, but no difference in band 500-650 kHz.

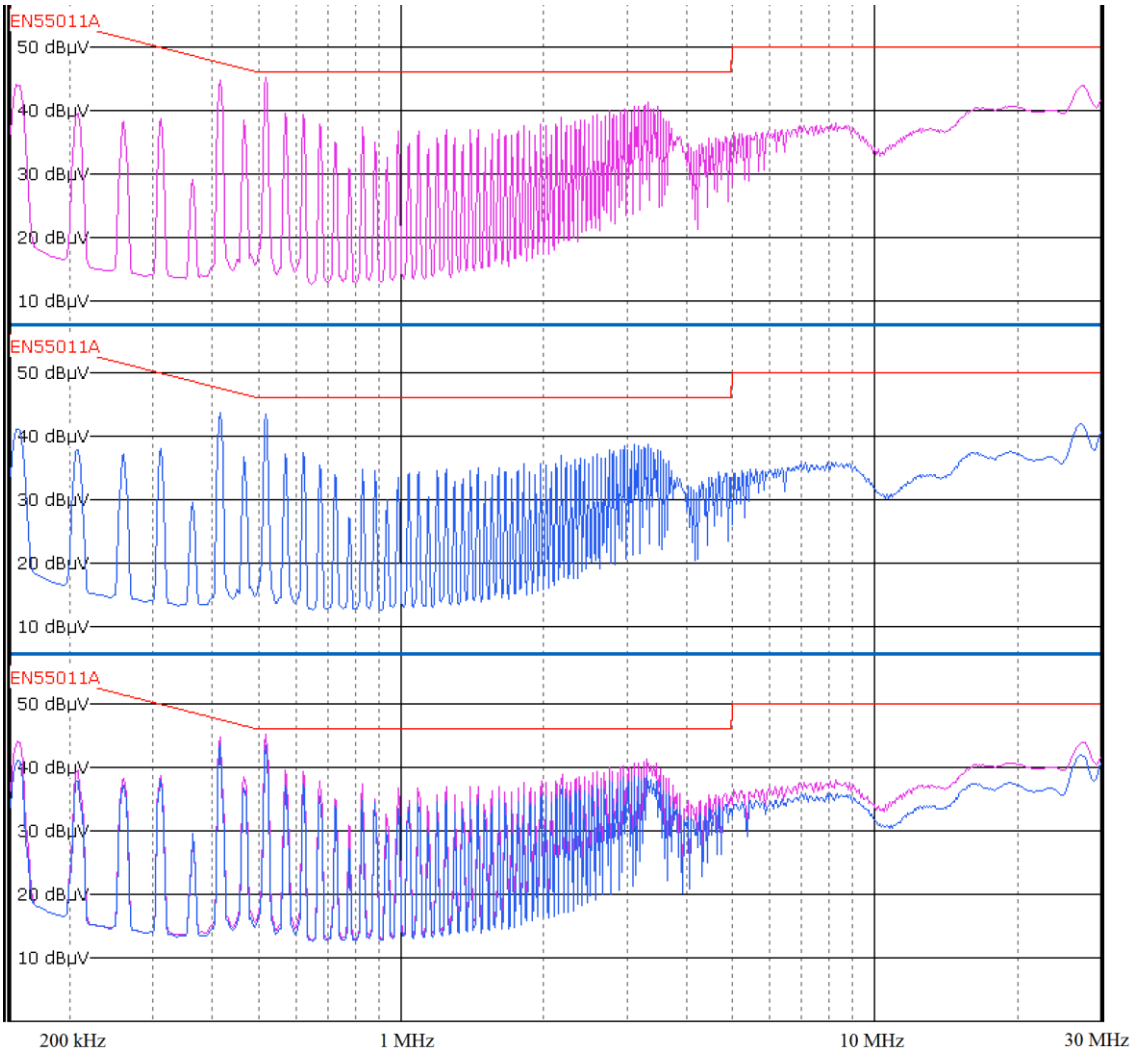



*Figure 22 Additional comparison: Top – standard capacitor bank; Middle – triple capacitor bank; Bottom - both*

Even if this was not sufficient improvement, it proves one thing: used electrolytic capacitors have in this band still low impedance. To see their effect, another triplet of capacitors in series was added – results are demonstrated in Figure 22: on the top standard v2 board (average L); in the middle v2 with three triplets of capacitors in series; on the bottom both together. In the observed band spikes drop about approx. 2-3 dB, which is quite good result: considering simple impedance divider, lowering the impedance to ⅔ gives drop -3,52 dB. Also, if the component aging worsens conductive EMI above limits, adding another capacitor triplet could solve the problem.

As was mentioned in 2.4.2 interleaving primary and secondary layers in transformer may worsen EMI, this is in my opinion the result. Before EMC optimization, capacitors C34 and C35 (used for bypass of primary and secondary grounds) were 2.2 nF. The results were horrible and increasing their values to 4.7 nF made a huge improvement. Their purpose is to lower the effect of transformer primary-to-secondary capacitance. Therefore, I presume the problem is the interleaving. Higher value might help, but then the design probably wouldn't meet requirements for safety isolation mains-to-output (sometimes titled *Line Leakage*). There is usually the limit 210 µA; for maximum AC voltage 690 V and frequency 100 Hz (50 Hz after rectification) current through C34 and C35 is already approx. 102 µA. Leakage current wasn't measured, but considering leakage currents through transformer isolation, converter might be near the limit even with this values.

# 3 Analysis of SiC driving and switching

## 3.1 Problematics of driving SiC MOSFET

Currently, typical power MOSFETs for switching applications can be driven with 10V Gate-Source square wave. Even if 10 V for $V_{GS}$ is often enough, they can withstand much higher voltage. Most of the standard power converter's ICs for use with external MOSFET are designed for these conditions. Driving SiC MOSFET may be slightly difficult, especially with one of these ICs. This whole problem is described below in this subchapter.

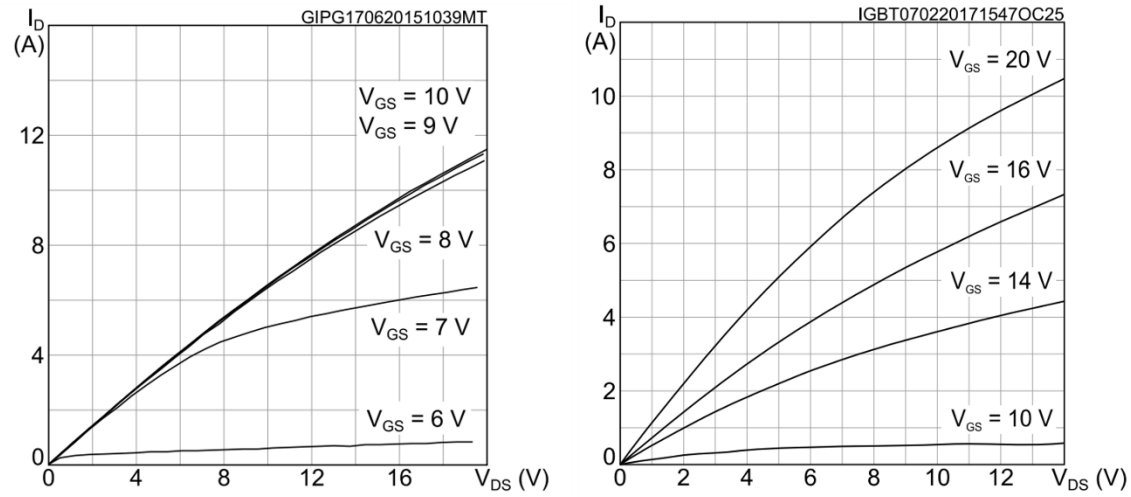



*Figure 23 - a) STW12N150K5 output characteristics b) SCT1000N170 output characteristics; credit [8] [9]*

For switching purposes, operation in resistive region is the only acceptable mode during on-time. As mentioned, for most MOSFETs – e.g. for the measured one STW12N150K5 – 10 V of $V_{GS}$ is enough to reach resistive region for any rated current. As it's obvious from output characteristics in Figure 23 slightly lower voltage shouldn't be a big problem either - curves for $V_{GS}$ 9 V and 10 V are nearly identical and the one for 8 V is still very similar. Opposed to Si, SiC MOSFETs are more sensitive to Gate-Source voltage (Figure 23 - b). This makes their switching more difficult: double value of $V_{GS}$ is required same as it's precise value – 20% decrease (which is quite common tolerance) makes an unpleasant growth of on-time resistance – traces for $V_{GS}$ 20 V vs 16 V.

Besides output characteristics, another parameter of Gate-Source voltage must be taken into consideration. The absolute maximum rating of STW12N150K5's $V_{GS}$ is ± 30 V, which is 3times more than ideal switching voltage. In case of any inappropriate handling or any voltage surges Gate is protected with clamping Zener diodes. The situation with SCT1000N170 is quite more complex: $V_{GS}$ AMR is just + 25 V and – 10 V. With ideal On-time $V_{GS}$ = 20 V there is not much headroom to AMR, exactly 25% (opposed to 200% of Si's MOSFET).

In general, ICs with external MOSFET use $V_{GS}$ driving range approx. 10 V and higher. IC used in measured design of this diploma thesis (L6566BH) has its high-level range clamped to 15 V. Since it has no Gate voltage booster, minimum high-level voltage can be slightly lower than minimum operating voltage, which can decrease to 7.2 V. This may happen only for light-load, so Drain current limit will be the lowest possible and no damage threatens the MOSFET.

[13] [14] [19]

## 3.2 Design of Gate-Drive module

All circumstances described above require a complex solution of driving SiC MOSFET. The driving circuit must provide stable voltage with exact amplitude 18-20 V and no more: the absolute maximum rating of $V_{GS}$ is not allowed for permanent operating condition; margin approx. 20% is recommended, hence maximum operating $V_{GS}$ = 20 V. This must be guaranteed even for the very first pulse after start-up.

Of course, simplicity and reliability are significant parameters, but low power consumption is very important: while starting, whole low-voltage section of primary side is powered from pre-charged VCC capacitor. Before auxiliary winding starts providing power, whole system must work properly and with low power consumption, so there's enough energy in the capacitor to span the delay.

It's obvious that some form of voltage booster will be necessary. Many of ICs use sort of charge pump with bootstrap capacitor, but this was evaluated as unsuitable solution. First, charge pump design for this application with discrete components (no suitable IC was found) might be considered as not as simple as required. More importantly, if the bootstrap capacitor gets discharged – e.g. in case of some malfunction – SiC transistor may operate in saturation region, which will be (most probably) destructive.

### 3.2.1 Design topology and schematic

Instead of charge pump, transformer voltage booster shown in Figure 24 was designed. Whole concept was developed as simple Gate-Drive module which can be connected to the main PCB. With this solution it's easy to convert the board from driving Si MOSFET to driving SiC: just one resistor is soldered out (R31 in schematic) and GD module is connected. This is useful for valid comparison between Si and SiC MOSFETs: the very same components are used for different measurements, so any deviation from nominal value (which may affect the measurement) wouldn't differ.

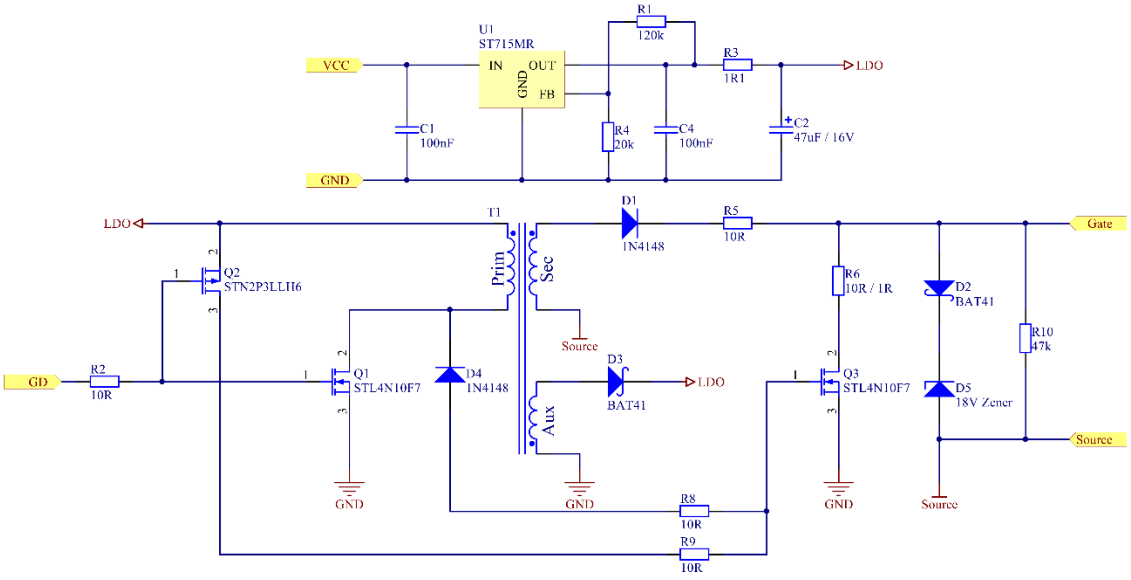



*Figure 24 Gate-Drive module schematic*

Voltage stabilization is provided by linear voltage regulator U1 and the transformer's turns ratio. The LDO's bus voltage was set to 8.75 V: as for operating conditions L6566BH needs at least 9.4 $V_{VCC}$, the bus should be stable even near UVLO. Purpose of R3 is to increase the impedance of C2, so no problems with stability of U1 caused by driving capacitive load should occur.

During on-time, circuit can be described as forward converter: Q1 is switched on and voltage approx. $V_{LDO}$ is applied on the primary winding. This voltage is transformed to the secondary winding according to Faraday's law:

$$V_{prim} = N_{prim} \cdot \frac{\mathrm{d}\Phi}{\mathrm{d}t};\ V_{sec} = N_{sec} \cdot \frac{\mathrm{d}\Phi}{\mathrm{d}t} \rightarrow V_{sec} = V_{prim} \frac{N_{sec}}{N_{prim}} \tag{15}$$

Dots mark the winding's start and all windings are placed over each other with the same sense of rotation, thus core flux and voltage have the same polarity. Transformer T1 is considered ideal, so primary and secondary winding flux is the same. No-gap core was used for maximum inductance, so leakage flux is negligible. $V_{sec}$ is applied through D1 and R5 to the Gate of the SiC MOSFET. As $V_{GS}$ must be at the exact value, the end of the secondary winding is connected directly to the Source. D2 and D5 are protective clamp diodes against rising edge spikes caused by resonance between winding's inductance and parasitic capacitance.

Usage of transformer instead of charge pump is indeed an advantage: $V_{GS}$ can be applied directly between Gate and Source, so voltage drop on current sensing resistor ($R_{sense}$) wouldn't affect it. This might be handy in case of unexpected overcurrent caused for instance by main transformer saturation – until the controller switches off, $V_{GS}$ is still securing the best operating conditions. Besides satisfactory $V_{GS}$ guarantee during on-time, this topology can cover another inconvenience: if any malfunction cause power consumption from the secondary winding of the Gate-Drive, it will be compensated thanks to Faraday's law. In the worst case (e.g. short circuit), GD module will discharge controller's VCC capacitor which will lead to an undervoltage protection.

During off-time, Q3 switches on and clamps the Gate with R6 to GND. Instead of connecting its Source to the SiC transistor's Source, GND was chosen because otherwise especially in case of overcurrent (and thus $R_{sense}$ voltage drop), $V_{LDO}$ (referenced to GND) can't guarantee satisfactory $V_{GS}$ for Q3 to switch on. Because of that, in case of extreme overcurrent voltage drop on $R_{sense}$ could reach value of SiC negative $V_{GS}$ AMR. This should never happen as L6566BH second level OCP (which immediately shuts the MOSFET down) triggers at 1 V (typ.). To prevent even this case, D2 can be replaced with another Zener diode with breakdown voltage ~3,5 V.

Since core flux Φ is charged during on-time, it is necessary to provide demagnetization. For this purpose, there is third winding: auxiliary. After on-time, circuit can be viewed as flyback converter: core flux was charged with primary winding and D3 have been blocking the reflected voltage. During off-time, current $i_{aux}$ starts flowing through auxiliary winding and diode D3 and charges the LDO bus. With this feature, almost all energy stored in the magnetic of T1 will be recuperated back into the LDO bus, so low power consumption is achieved.

Last important component is the resistor R10: this is the startup protection for the SiC. As input voltage is connected, the slope of $V_{DS}$ can charge Gate through Miller capacitance $C_{GD}$. As $C_{GD}$ is already charged, only 2 nC for $C_{GS}$ are needed, so $V_{GS}$ can easily grow above threshold voltage and lead to MOSFET destruction. VCC is not charged yet and thus Q3 can't discharge it.

[20] [21] [22]

### 3.2.2 Gate-Drive transformer design

EP cores are mostly used for driving transformers, because of their compact design and low leakage inductance. First step to design transformer for this exact purpose is to set number of primary winding turns. This can be calculated from modified equation (10) using equation (1):

$$B = \frac{L \cdot I}{N \cdot A} = \frac{L \cdot \frac{V \cdot t_{on}}{L}}{N \cdot A} = \frac{V \cdot t_{on}}{N \cdot A} \tag{16}$$

With modification from eq. (16), core flux density is independent of inductance or winding current. This is very important: as EP core consist of two halves and probably no-gap core will be used (for minimum leakage inductance), precise inductance can't be defined – there will always be gap between the core halves, only almost negligible. As mentioned with flyback transformer design, there can be some offset or dust particles between them and the gap will emerge, therefore inductance lowers. For fixed frequency operation it's easy to set the maximum $t_{on}$: L6566BH have limited maximum duty cycle to 75%, so for switching frequency 51,3 kHz $t_{on}$ = *14,6 µs*. In previous section the voltage was also defined as $V_{LDO}$ = *8,75 V*. *A* is the cross-section area of the core, for EP10 it's 11,3 mm$^2$ and for EP7 10,3 mm$^2$. Again, it should be multiplied with correction factor covering possible offset. Because the equation estimates linear inductance and neglects voltage drops, *N* should be set for $B < B_{max}$ with reasonable margin.

As Primary turns are calculated, secondary turns are defined with eq. (15). Auxiliary winding turns need to provide proper demagnetization during off-time. This can be calculated from eq. (16), but correct way is to mention one other equation to prove it:

$$\Phi = B \cdot A \tag{17}$$

If we set $V_{prim\_on\text{-}time} = V_{aux\_off\text{-}time}$ (voltage drop on D3 just adds margin) and consider maximum duty cycle 75%, from equation (16) necessary primary-to-auxiliary turns ratio is calculated as ⅓. Unfortunately, this was found insufficient for EP7 core due to its parasitic capacitance. This phenomenon is demonstrated in Figure 25: Gate-Drive module was driving SiC MOSFET, the duty cycle was set with generator. Purple trace (Ch3) shows voltage on the auxiliary winding for D = 60%. During off-time, $V_{aux}$ starts rising but very slowly, then provides partial recuperation and starts decreasing similarly. This makes estimation based on equation (16) invalid, so auxiliary winding has to have slightly lower number of turns. This is one possible approach, another is lowering parasitic capacitance, for instance by interleaving layers with insulation tape or lowering the number of turns for every winding. The last option may collide with maximum core flux density and there might have been not enough space for interleaving with tape. To avoid this, another core (and/or core magnetic material) can be used.

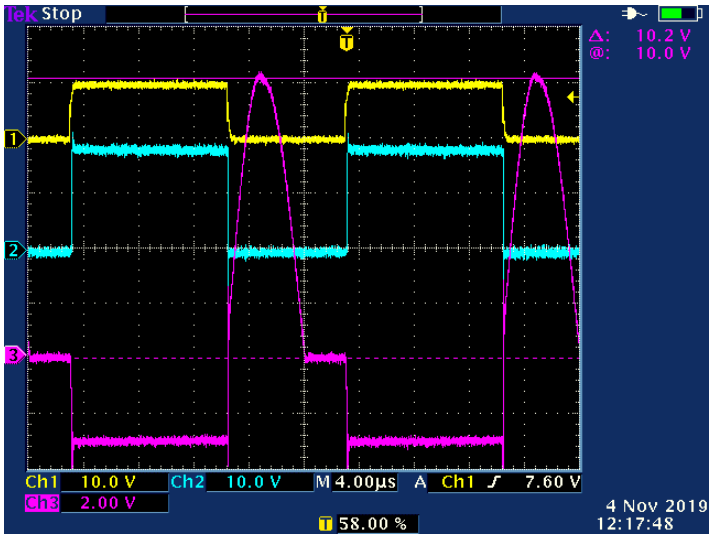



*Figure 25 Parasitic capacitance effect; 1 - generator, 2 - $V_{GS}$, 3 - $V_{Aux}$*

Follows from the above, two Gate-Drive transformers were designed. Both were suitable for duty cycle up to 75% and minimum switching frequency approx. 20 kHz. First uses the EP7

core, second EP10 – unfortunately, hand-made laboratory prototyping was not repeatable with same – or even sufficient – results for the EP7. However, with more precise procedure this design may be suitable. Parameters for EP7 type:

Core: EP7; CF138; no gap
Primary: 60 turns; 0.08 mm
Secondary: 120 turns; 0.08 mm
Auxiliary: 19 turns; 0.08 mm

Parameters for EP10 type:

Core: EP10; CF297; no gap
Primary: 55 turns; 0.1 mm
Secondary: 125 turns; 0.1 mm
Auxiliary: 18 turns; 0.1 mm

Primary to secondary turns ratio for EP7 and EP10 is different: EP7 was powered from 9V supply rail, EP10 from 8.75 V.

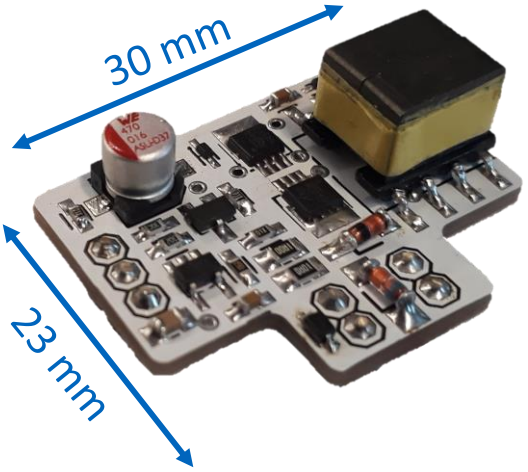



*Figure 26 Gate-Drive module for board v1*

Gate-Drive module designed for board v1 is shown in Figure 26 (EP7 transformer is assembled). For all measurements with SiC the GD module with EP10 transformer was used. To prove his addition had negligible effect, following table shows its power consumption for selected duty cycles:

| Duty cycle [%] | 20 | 30 | 40 | 50 | 60 | 70 | 75 | 77 |
|---|---|---|---|---|---|---|---|---|
| Current consumption [mA] | 7.84 | 8.64 | 9.43 | 10.17 | 10.89 | 11.66 | 14.67 | 28.49 |

*Table 1 Gate-Drive module power consumption*

Stand-by current for VCC = 12 V was measured 65.9 µA.

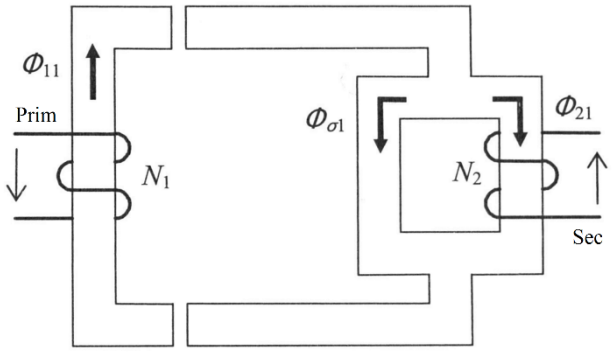



*Figure 27 Hopkinson's law illustration; credit: [21]*

Another approach to solve problem with parasitic capacitance was tested: cores with air gap. Because only difference is lower inductance, i.e. higher peak currents, parasitic capacitance should have been charged fasted. Unfortunately, this made no beneficial impact. And, what is worse, according to Hopkinson's law, if core flux splits, loading the winding affects the flux distribution (Figure 27; if secondary winding is shorted, $\Phi_{21} = 0$). This doesn't apply to core, but to primary winding magnetic flux. In this case is the split is caused by non-ideal coupling factor (= leakage inductance) and with additional core gap this effect strengthens. As a result of that, secondary voltage ($V_{GS}$) was not as stable as in Figure 25 (light blue Ch2), but slowly decreased with on-time. Because $V_{GS}$ for SiC must be strictly kept, this was identified as potential fatal flaw: with longer on-time Drain current increases, therefore any saturation region operation becomes more significant.

## 3.3 Focus on MOSFET parameters

As mentioned in first and second chapter, designed flyback was intended for direct comparison of SiC MOSFET vs Si MOSFETs – first intention of cooperation with STMicroelectronics was testing their SCT100N170 SiC MOSFET. To prove (or disapprove) its advantages similar MOSFETs from STM were selected, their most important (AMR) parameters are listed in Table 2. **As their full names are quite long and sometimes very similar, for better clarity and simplicity they are going to be labeled with abbreviation further in this thesis!** Output capacitance $C_{oss}$ comparison is set for estimated $V_{DS}$ of $400V_{AC}$ input: 560 $V_{DC}$.

| MOSFET ID | Abbr. | $V_{DS\text{-}AMR}$ [V] | $I_{Dcont.\ 25°C}$ [A] | $R_{DS\text{-}on\ 25°C}$ [Ω] | $C_{oss}$ [pF] |
|---|---|---|---|---|---|
| STW12N170K5 | **Mos1** | 1700 | 5 | 2.3 | 30 |
| STW3N170 | **Mos2** | 1700 | 2.6 | 7 | 23 |
| SCT1000N170 | **SCT** | 1700 | 6 | 1 | 15 |
| STW12N150K5 | **Mos3** | 1500 | 7 | 1.6 | 33 |
| STW21N150K5 | **Mos4** | 1500 | 14 | 0.7 | 70 |

*Table 2 Compared MOSFETs; source: [16][17][14][13][15]*

SiC MOSFETs have in general lower $R_{DS\text{-}on}$ and $C_{oss}$ for the same rating as Si based. According to the rating, closest to SCT is Mos1, but with higher $R_{DS\text{-}on}$. Mos2 is underrated for this application, but for higher input voltages may give good results because of its low $C_{oss}$ capacity. Unfortunately, STM didn't make any similar 1700V MOSFETs, so two 1500V were selected: Mos3 and Mos4. Both of these can't be used for 1 kV input, but for voltages approx. 900 $V_{DC}$ and lower might give good results because of their low $R_{DS\text{-}on}$.

These parameters are useful barely for gross comparison, but can reveal that these MOSFETs are at least similar and useable in this application. More interesting – and discussed later in this chapter – are variations of parameters like on-state resistance and output capacitance with voltage and/or temperature. As it shows up, important can be also Gate charge and intrinsic Gate resistance, which are closely observed in subchapter 4.3.

## 3.4 Losses estimation and simulation

Main sources of losses in the designed converter are presumed to be input stage, primary MOSFET, transformer (and its leakage inductance) and output diode. For Si versus SiC comparison this section focuses on MOSFET losses estimation only. Major losses caused by transistor are due to $R_{DS\text{-}on}$ and output capacitance $C_{oss}$. Losses on $R_{DS\text{-}on}$ are caused by primary winding current according to Joule's first law. As this current is proportional to output load, so are these losses – further called resistive. Losses caused by output capacitance depend only on switching frequency, not load (except burst mode): energy stored in the capacitance is dissipated every time MOSFET switches on – hence switching losses. Since the converter operates in DCM, switch-on losses consist almost exclusively of energy stored in $C_{oss}$ and parasitic capacitance.

### 3.4.1 Resistive losses

Simulating each MOSFET for every input voltage and output power would be time-consuming, so losses will be just estimated from known or measured parameters. What is more, for precise simulation more parameters have to be included: for instance, knowing the point of switching is necessary, but it is given by oscillations on transformer, which are quite complex

problematic. Estimating linear $R_{DS\text{-}on}$, resistive losses can be calculated using the following equation:

$$P_{res} = R_{DS-on} \cdot I_{RMS}^2 \tag{18}$$

Effective current $I_{RMS}$ is defined with the equation below:

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i_{(t)}^2 dt} \tag{19}$$

For linear current rise during on-time, it can be modified using equation (1) as:

$$\begin{aligned} I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i_{(t)}^2 dt} = \sqrt{\frac{1}{T}\int_0^{t_{on}} i_{(t)}^2 dt + \int_{t_{on}}^{t_{off}} 0 dt} = \sqrt{\frac{1}{T}\int_0^{t_{on}} \left(\frac{U \cdot t}{L}\right)^2 dt} = \\ = \sqrt{\frac{1}{T}\left(\frac{U}{L}\right)^2 \int_0^{t_{on}} t^2 dt} = \sqrt{f_{SW} \cdot \left(\frac{U}{L}\right)^2 \cdot \frac{t_{on}^3}{3}} = \\ = \sqrt{f_{SW} \cdot t_{on} \cdot \frac{\left(\frac{U \cdot t_{on}}{L}\right)^2}{3}} = \sqrt{f_{SW} \cdot t_{on} \cdot \frac{I_{prim-pk}^2}{3}} \end{aligned} \tag{20}$$

This modification allows to calculate expected $I_{RMS}$ through $R_{DS\text{-}on}$ from output power: as the output voltage is regulated, it can be set just as 24 V. Thus output current can be determined directly from output power as $I_{out} = P_{out}/24$. Using equations (5) and (4) $I_{prim\text{-}pk}$ can be calculated from $I_{out}$. For each input voltage on-time can then be determined using equation (1). Before that, expected losses were added to output power (simplified principle which considers ideal converter with losses connected as additional load to output) to set on-time more precisely. The expected losses were derived from measured average efficiency, same for every MOSFET – listed in Table 3 on next page.

| Estimated efficiency [%] | | | | | | |
|---|---|---|---|---|---|---|
| | | $P_{out}$ [W] | | | | |
| | | **10** | **25** | **50** | **75** | **100** |
| $Uin_{DC}$ [V] | **150** | 84 | 85 | 86 | 86 | 85 |
| | **250** | 83 | 85 | 85 | 85 | 84 |
| | **320** | 83 | 85 | 86 | 86 | 86 |
| | **560** | 79 | 84 | 86 | 86 | 87 |
| | **700** | 76 | 83 | 86 | 86 | 87 |
| | **840** | 73 | 81 | 84 | 85 | 86 |
| | **900** | 70 | 79 | 84 | 85 | 86 |
| | **1000** | 67 | 78 | 83 | 84 | 86 |

*Table 3 Estimated efficiency*

Little skip forward, this table refers to input voltages and output powers for which the measurements were made – DC: 150 V, 900 V and 1 kV; AC: 180 V, 230 V, 400 V, 500 V, 600 V (AC inputs were converted to DC as $\sim\sqrt{2}\cdot V_{AC}$). 690 VAC was also measured, but its equivalent DC value is close to 1 kV, so it wasn't included in loss estimation: resistive losses are minor for high input voltages and main intention of MOSFET related switching losses is voltage dependence of output capacitance Coss – which is almost constant in this case.

As $R_{DS\text{-}on}$ is temperature dependent, also temperature must have been estimated (again on previous measurements): for $P_{out}$ 10 W and 25 W 50°C, 75°C for 50 W and 100°C for 75 W and 100 W. This is rough estimation, but not so far from real values – junction temperatures calculated from measured package temperature are listed later in Table 12. Values for $R_{DS\text{-}on}$ according to datasheet are listed below:

| | $R_{DS\text{-}on}$ [Ω] | | | | |
|---|---|---|---|---|---|
| **Temp.** | **25°C** | **50°C** | **75°C** | **100°C** | **125°C** |
| **Mos1** | 2.30 | 2.88 | 3.45 | 4.19 | 4.89 |
| **Mos2** | 7.00 | 8.40 | 10.15 | 12.25 | 14.70 |
| **SCT** | 1.00 | 1.05 | 1.08 | 1.15 | 1.25 |
| **Mos3** | 1.60 | 1.95 | 2.40 | 2.96 | 3.57 |
| **Mos4** | 0.70 | 0.85 | 1.05 | 1.30 | 1.58 |

*Table 4 Temperature variations of $R_{DS\text{-}on}$; source: [16][17][14][13][15]*

For every MOSFET resistive losses were calculated according to equation (18) for each measured input voltage and output power.

### 3.4.2 Switching losses

As mentioned above, during every switch-on cycle energy stored in output capacitance is dissipated. Not only this capacitance, but also parasitic capacitances of the transformer and PCB. Opposed to $C_{oss}$, these can't be changed with different MOSFET, but the intention of including them is comparison of their part in switching losses to $C_{oss}$. Parasitic capacitance was calculated from resonant frequency with leakage inductance. The measurement was done with oscilloscope Tektronix TDS3054B and generator Agilent 33250A according to [21], resonant frequency was determined $f_0$ = 5,69 MHz. Leakage inductance was measured with Rhode & Schwarz HM8118 as 7,84 µH for frequency 50 kHz on primary winding (secondary and auxiliary winding shorted).

This was measured on the very same board with MOSFET Gate and Source soldered to Drain[5] between nets Snubber (Drain) and V+. Resonant frequency for LC circuit is defined with equation:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{21}$$

from which was parasitic capacitance calculated as 100 pF. This is the capacitance with connected probe and will be further called $C_{p\text{-}p}$, which is equal to parasitic capacitance $C_p$ and probe capacitance added in parallel. Probe capacitance was measured with HM8118 as 13 pF, it should be said that this is probably affected by not negligible measurement uncertainty. Nevertheless, for losses estimation the parasitic capacitance $C_p$ as 87 pF was included.

Output capacitance is typically function of $V_{DS}$ and is grossly nonlinear. The huge variation is mainly caused by space charge region – as it gets wider with $V_{DS}$, Drain neutral region gets smaller, thus smaller area of it can be seen as electrode of $C_{oss}$. Opposed to $R_{DS\text{-}on}$, this remains consistent with temperature. As demonstrated in Figure 28, for low voltage it is almost four orders higher than its final value. As the axes are logarithmic, it's not so easy to see that the main difference in value of $C_{oss}$ is for $V_{DS}$ lower than few volts. Energy stored in $C_{oss}$ used for losses estimation is considered for $V_{DS}$ equal to V+ rail, i.e. all oscillations already faded away. This is good approximation for higher input voltage, but it has its limits for $V_{in}$ = 150 $V_{DC}$: this was previously set as a boundary condition for DCM, so any oscillation even can't start. Including $V_{DS}$ in range of 150 – 1000 V also doesn't mean any advantage: $C_{oss}$ change is not so significant, but stored energy is defined by whole $C_{oss}$ curve including the initial value.

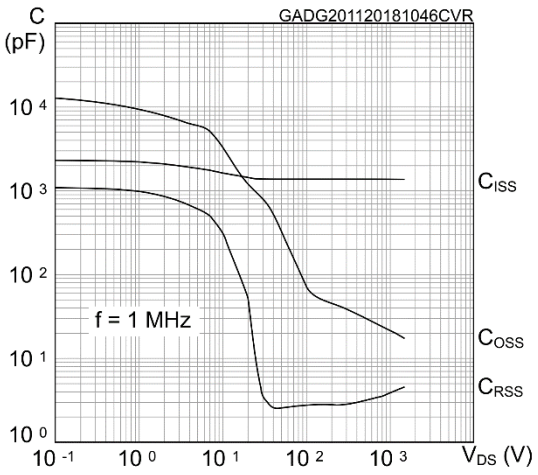



*Figure 28 Parasitic capacitances of Mos1, credit: [16]*

[19]

There are three main approaches to define this capacitance: first defines it as described above – as a voltage function. This is mostly measured with DC voltage applied between Drain and Source ($V_{GS}$ = 0 V) with additional (resistive) impedance and with another AC generator (usually with frequency 1 MHz and negligible amplitude). This is often listed in datasheets for specific voltage and also as a voltage-dependent chart. From this value it's possible to calculate for instance oscillations with parasitic inductance. However, calculating switching losses as energy stored in this capacitance according to eq. (22) is completely incorrect.

$$E_C = \frac{1}{2} C \cdot V^2 \tag{22}$$

*"It would appear that some of the inconsistencies in the (...) voltage-dependent capacitors stems from not properly defining the "capacitance" in use"* [27]. As this is discussed

[5] To eliminate effect of its parasitic capacitances but also include the capacitance of insulation pad between TO-247 (Drain) and heatsink (GND).

out in this source as a sort of true statement (two possible definitions of capacitance as a nonlinear charge storage element), it's wise to determine the energy directly from definition:

$$E_T = \int_0^T v(t) \cdot i(t)\, dt \tag{23}$$

where the capacitance voltage nonlinearity is applied to the current as:

$$i = C(v)\frac{dv}{dt} + v \cdot \frac{d\big(C(v)\big)}{dt} \tag{24}$$

This refers to the second point of view at output capacitance: as energy related, often designated as $C_{o(er)}$ – this is value of equivalent capacitance which stored energy (for defined voltage, usually 80 % of $V_{DS\text{-}AMR}$) is equal to energy stored in output capacitance. From $C_{os(er)}$ it is possible to calculate switching losses according to (22); unfortunately, this is sometimes not listed in datasheets as a voltage-dependent chart (in this case, it wasn't for SCT, Mos2 and Mos4).

To determine this energy the same way for every transistor, simulation circuit using SPICE models was selected as the best option (demonstrated in Figure 29; $V_{DS}$ – green, $I_D$ – blue, $E_{Coss}$ – red). The simulation calculates energy defined by eq. (23). This has two consequences: first, definition of *C(v)* used in eq. (24) as a continuous function is not necessary (SPICE approximate this function by lookup table defined in the model) and second, not only $E_{Coss}$ is calculated as another two possible losses are included – leakage current and weak inversion (subthreshold) operation. Leakage current can be definitely neglected for short integration period *T*, but the second depends on $V_{DS}$ slew rate. Even if Gate is connected to Source, it has its intrinsic resistance and Miller capacitance to Drain. Charge through $C_{GD}$ is stored in Gate and discharged with $R_G$. $V_{GS}$ caused by this effect is not negligible for higher slew rate (it can near to threshold, typ. for ≥ 50 V/ns) and may cause rise of $I_D$. Simulation was optimized for shortest possible integration period for which another lowering of slew rate had no effect on integrated energy. In this case I pronounce another losses as sufficiently negligible for this purpose, so the integrated energy was stated as $E_{Coss}$ and is listed in table below:

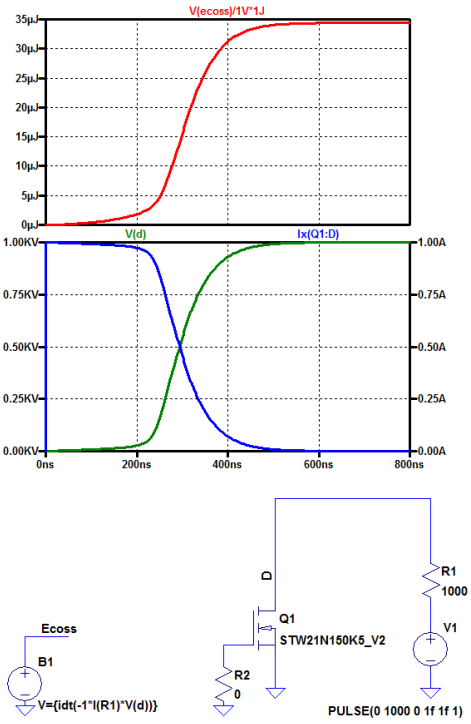



*Figure 29 $C_{oss}$ energy (Red trace) simulation*

| | $E_{Coss}$ [µJ] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **$V_{DS}$ [V]** | **150** | **250** | **320** | **560** | **700** | **840** | **900** | **1000** |
| **Mos1** | 2.19 | 3.14 | 4.00 | 7.51 | 10.06 | 12.79 | 14.06 | 16.31 |
| **Mos2** | 0.73 | 1.55 | 2.27 | 5.31 | 7.48 | 10.01 | 11.21 | 13.42 |
| **SCT** | 0.39 | 0.85 | 1.24 | 2.86 | 3.99 | 5.29 | 5.91 | 7.04 |
| **Mos3** | 2.46 | 3.60 | 4.53 | 8.63 | 11.38 | 14.60 | 16.02 | 18.46 |
| **Mos4** | 4.63 | 6.74 | 8.55 | 16.21 | 21.42 | 27.12 | 29.85 | 34.41 |

*Table 5 Simulated $C_{oss}$ energy*

As switching losses are proportional only to switching frequency and not output power, for used switching frequency $f_{SW}$ = 51.3 kHz following losses caused by $C_{oss}$ were stated:

| | $P_{Coss}$ [W] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **$V_{DS}$ [V]** | **150** | **250** | **320** | **560** | **700** | **840** | **900** | **1000** |
| **Mos1** | 0.11 | 0.16 | 0.21 | 0.39 | 0.52 | 0.66 | 0.72 | 0.84 |
| **Mos2** | 0.04 | 0.08 | 0.12 | 0.27 | 0.38 | 0.51 | 0.58 | 0.69 |
| **SCT** | 0.02 | 0.04 | 0.06 | 0.15 | 0.20 | 0.27 | 0.30 | 0.36 |
| **Mos3** | 0.13 | 0.18 | 0.23 | 0.44 | 0.58 | 0.75 | 0.82 | 0.95 |
| **Mos4** | 0.24 | 0.35 | 0.44 | 0.83 | 1.10 | 1.39 | 1.53 | 1.77 |

*Table 6 Estimated switching losses caused by output capacitance*

### 3.4.3 Losses estimation

According to previous two sections, for each used MOSFET resistive and switching losses were calculated for every input voltage and output power listed in Table 3. Overall losses for maximum output power are shown in Figure 30 on the next page. Pcoss represent losses due to output capacitance and Pres the resistive losses. For comparison switching losses caused by parasitic capacitance – Pcp (measured in previous section) are also added. As Mos2 is slightly underrated for this application, it's included only for input voltage 500 $V_{AC}$ and higher. The reason why it is even included in the measurements is further discussed in the next chapter.

From Figure 30 it can be seen that for higher voltage resistive losses decrease, because $I_{RMS}$ is proportional to on-time which becomes shorter. On the other hand, as capacitive losses grow with square of voltage (for linear capacitance), they rise from almost negligible for low voltage to major ones for higher voltage.

Another interesting factor is output capacitance to $R_{DS-on}$ ratio, for instance described on Mos4: due to small $R_{DS-on}$ losses for low voltage are the lowest of all Si-based MOSFETs. This, unfortunately, entails higher output capacitance, therefore more significant losses for higher voltages: besides underrated Mos2, it's the worst for input voltage 600 $V_{AC}$ and higher.

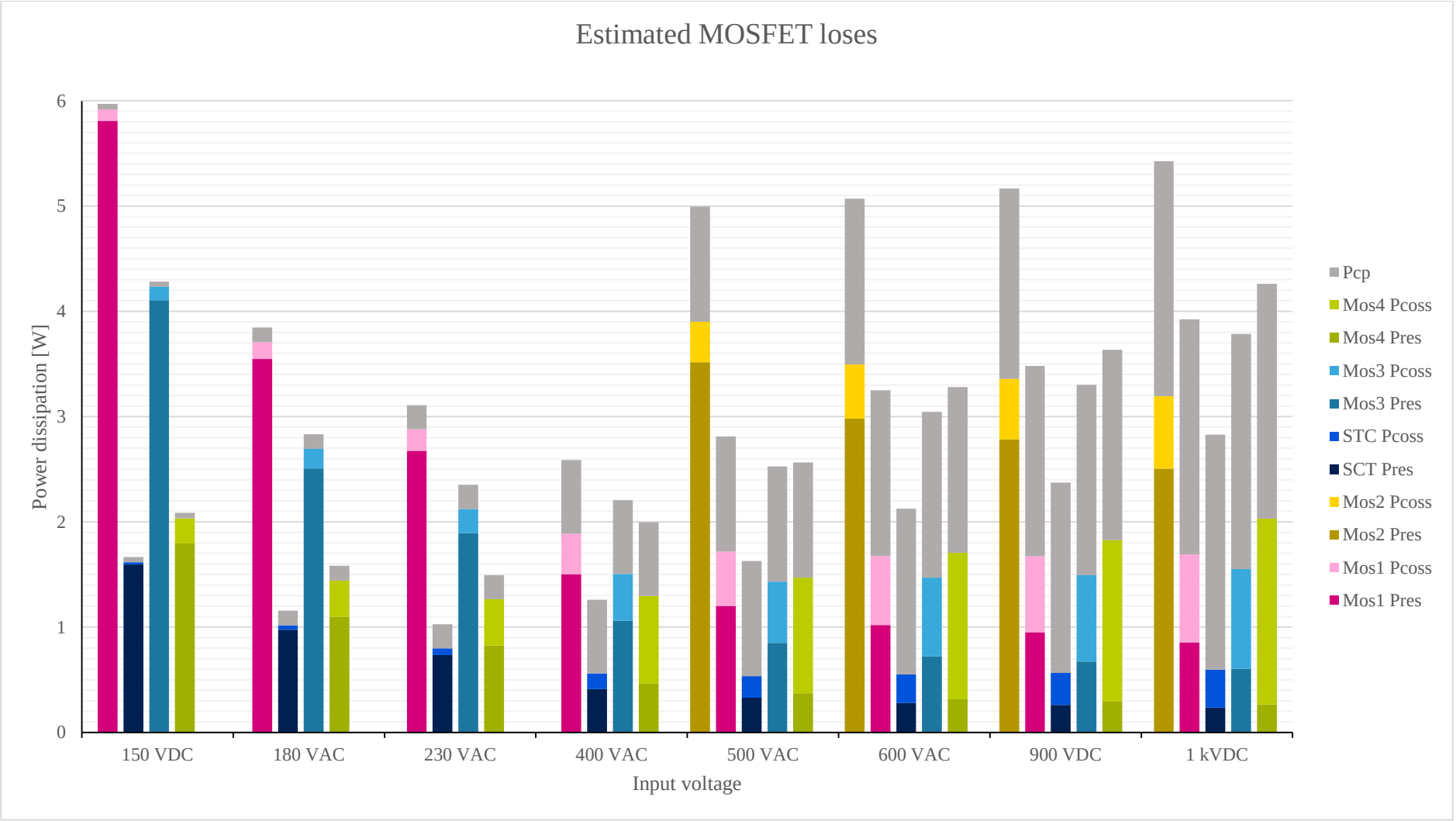



*Figure 30 Estimated MOSFET losses*

# 4 Si vs SiC

## 4.1 Efficiency measurement

In following subchapters few selected results and measurements, which I have found noteworthy, are extensively discussed. All efficiency measurement are shown in Appendix A or can be found as raw data in \Attachments\Efficiency.xlsx. All power measurements were made on Norma 4000 – High Precision Power Analyzer using its serial port to read all the data in the same time.

### 4.1.1 Lower input voltages

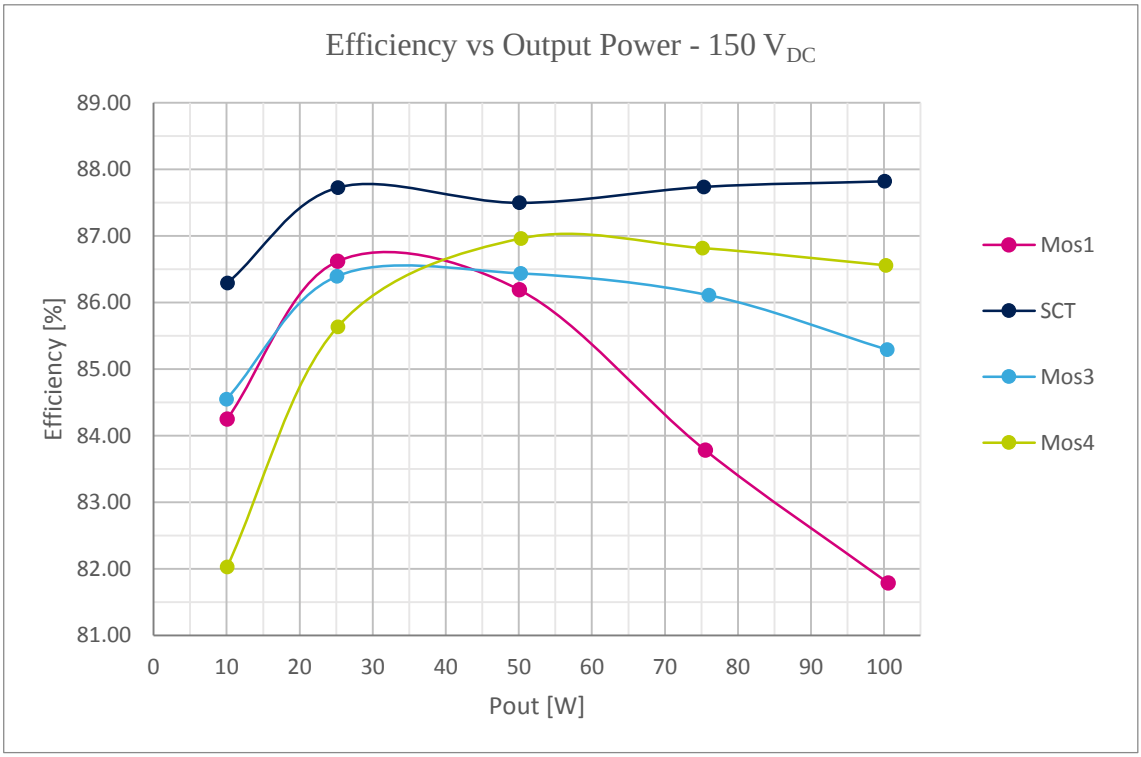



*Figure 31 Efficiency for $V_{in}$ = 150 $V_{DC}$*

As reviled in previous chapter, for lower input voltages significant losses on primary MOSFET are caused by its $R_{DS\text{-}on}$. It can be seen in Figure 31: efficiency for 75W and 100W $P_{out}$ are conclusively in order by $R_{DS\text{-}on}$. Worse Mos4's results for $P_{out}$ = 10 W and 25 W are probably caused by switching losses – they are proportional to switching frequency and input voltage, not output power. In this case, as input voltage is low, all parasitic capacitances should be included. Not only discussed $C_{oss}$: output capacitance definitely took its part, but as listed in Table 6, losses caused by it are estimated to just 0.24 W. Mos1 and Mos3 have this estimation very similar: 0.11 W and 0.13 W; they also have nearly the same efficiency result, only in opposite order – Mos1 has worse $R_{DS\text{-}on}$. Taking the difference for losses caused by $C_{oss}$ between Mos3 and Mos4 gives 0.11 W, which for 10W load means 1.1 % worse efficiency. The remaining one percent for this load is probably at least partially hidden in Mos4's higher Gate charge. As this is also highest of all used MOSFETs, for used $R_G$ = 10 Ω (R31 in schematic) discharging the Gate takes longer, thus Mos4 stays in saturation longer during switch-off. This phenomenon is closely observed further in 4.3.3.

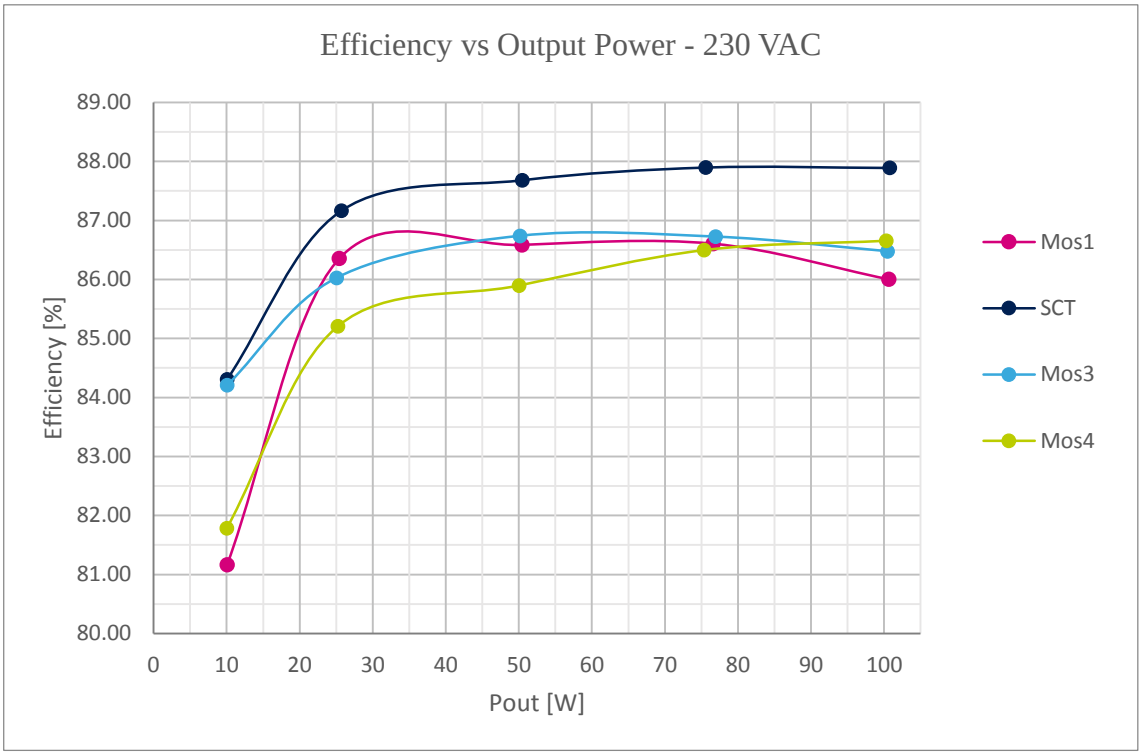



*Figure 32 Efficiency for $V_{in}$ = 230 $V_{AC}$*

For in Europe quite common input voltage 230 $V_{AC}$ effect of high $R_{DS\text{-}on}$ for Mos1 diminishes as on-time became approx. two-times shorter (equation (1); effective V+ rail voltage is expected 320 V). As shown in Figure 32, Mos1 is still the worst for full power, but the difference is minimized.

### 4.1.2 Midrange input voltages

Previously mentioned input voltage 230 $V_{AC}$ is standard phase-to-neutral voltage derived from 400$V_{AC}$ three-phase system. Efficiency trend for this voltage is similar to the next value of measured input voltage – 500 $V_{AC}$. As for this one it is finally possible to include Mos2 with results that can be pronounced valid (thermal stability despite high temperature, operation at least on borders of AMR, not above), efficiency for 500 $V_{AC}$ is demonstrated in Figure 33. It can be seen that Mos2's $R_{DS\text{-}on}$ still makes important losses as used light load is more or less equal to others, but for full load there's approx. 4% distinction between them. Reflecting its $R_{DS\text{-}on}$, which for measured junction temperature (revealed later in 4.5.1) 133.9°C is enormous 15.4 Ω, indicates why it can't be used for lower voltages. Not just because of longer on-time, thus higher $I_{RMS}$, even simplified primary winding current in equation (1) is in this case far from reality: for the reason that voltage estimated to be constant falls down by 43.7 V for peak current 2.84 A.

What is more, for midrange input voltages Si-based MOSFETS reduced the lead of SCT and for 50W and 75W loads even bounced ahead of it. As this is not boundary condition as the case of Mos4 for $V_{in}$ = 150 $V_{DC}$, it's hard or nearly impossible to determine the reason why. Another little skip forward: further in 4.1.3 & 0, same as in 0 is discussed the effect of point of switching – 50W and 75W loads were the worst possible cases (discussed later) for SCT.

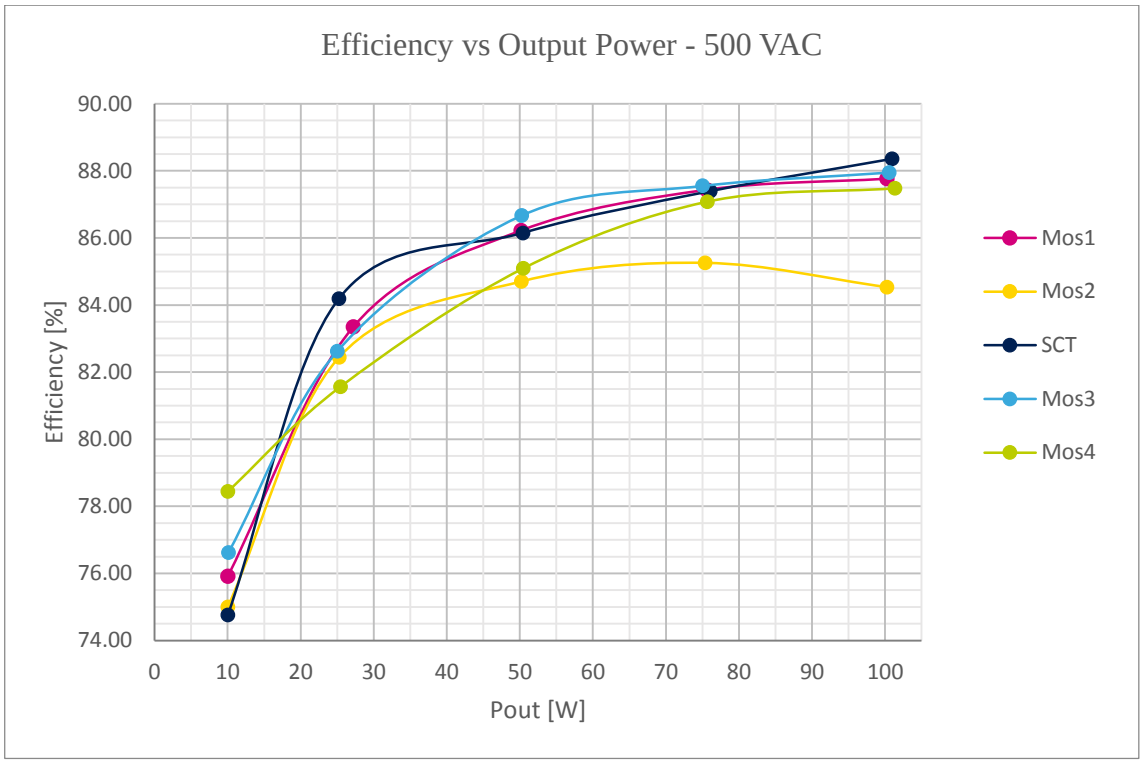



*Figure 33 Efficiency for $V_{in}$ = 500 $V_{AC}$*

### 4.1.3 Higher input voltages

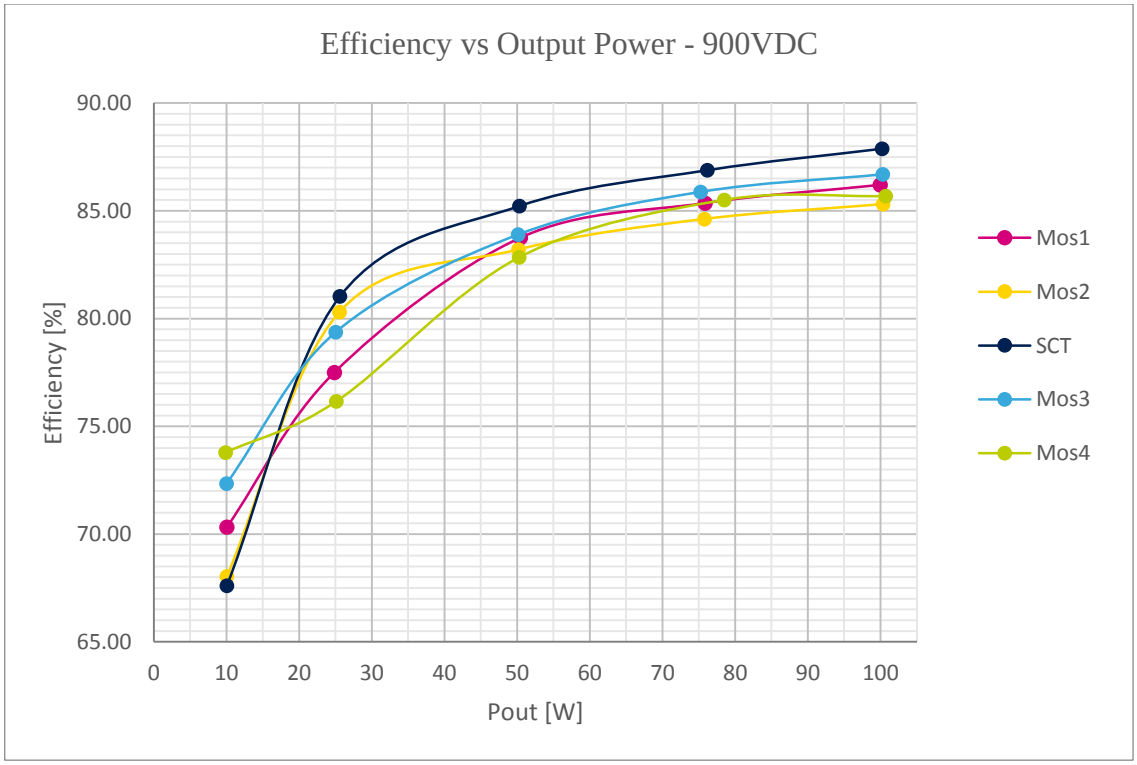



*Figure 34 Efficiency for $V_{in}$ = 900 $V_{DC}$*

Besides light load operation, for higher input voltages SCT takes the lead back. 900 $V_{DC}$ is the highest input voltage for which is flyback operation within AMR of all used MOSFETs; efficiency measurements is shown in Figure 34. Worse efficiency for 10W load is caused by

switching losses and other losses that are invariable with the load. Alike as Coss energy, they can be also voltage dependent: for instance, output diode (D17 in schematic) leakage current might also participate as it rises with reverse voltage reflected from primary, but it is of the order of miliwatts or even lower (estimating junction temperature $\leq 50°C$ for 10W load [18]). Another more significant loss came up with capacitor bank's balancing resistors – as they should stick to Ohm's law, it's less complicated principle. According to it for input voltage 900 $V_{DC}$ their power consumption equals to 0.29 W, which can be seen as not so much, but for 10W load it means instant 2.9% efficiency drop.

One more problem with 10W load can be better described using efficiency results for 1 kV input as there are only three measured transistors:

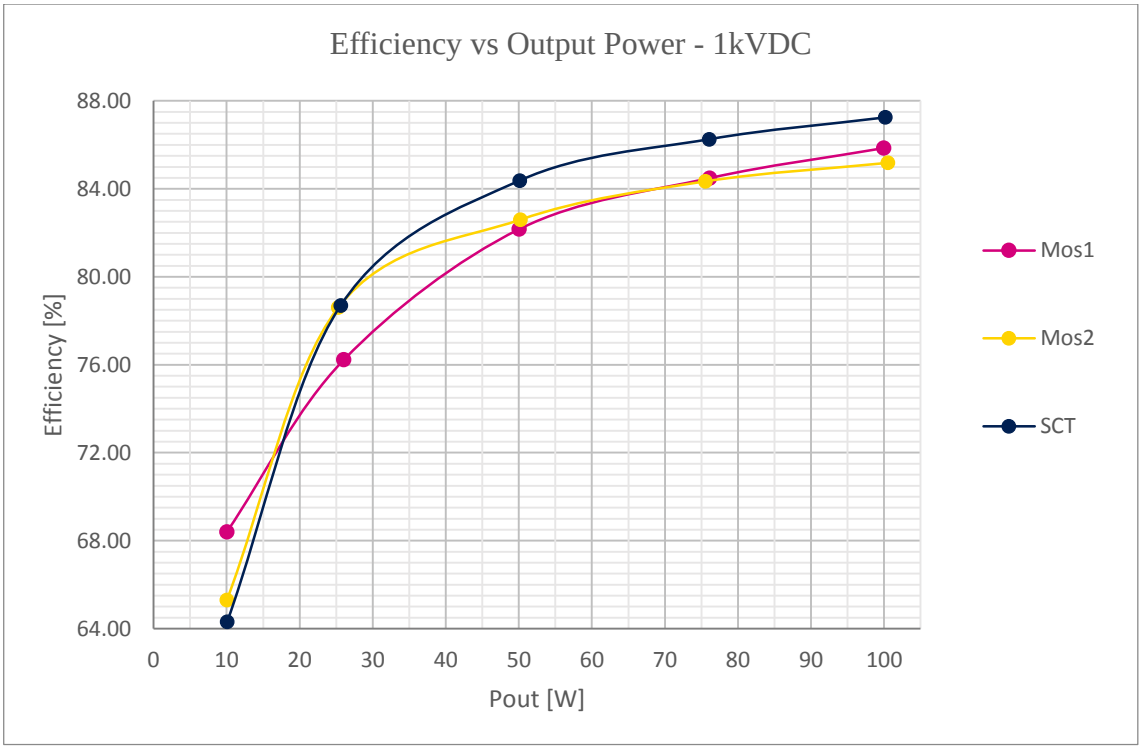



*Figure 35 Efficiency for $V_{in}$ = 1 $kV_{DC}$*

As another losses (not related to used transistor) should remain the same, it's interesting that SCT has the worst 10W efficiency. It could be caused by $R_{DS\text{-}on}$ in case of Mos2, but probably not and definitely not in case of SCT. As SCT have additional Gate-Drive module, but even considering 10mA consumption and 25 $V_{VCC}$ (both heavily overestimated), the efficiency loss should be just 2.5% and not at least 5% as seen in Figure 35. It is also true that GD module power consumption is mostly independent of input voltage so it should be observed for lower voltages too.


*Figure 36 Indirect transformer voltage measurement*

To uncover this phenomenon, it is necessary to know switching relations. These were measured indirectly – shown in Figure 36: if no exact value of voltage is required, this is the best option. Because it is used as sort of electrical field probe, any effect of it can be neglected. Otherwise, if probe was connected directly to Drain, it entails

parasitic capacitance and resistance to the circuit. This configuration was used for oscillations measurement discussed further in this chapter, where any additional capacitance could easily unbalance the oscillations.

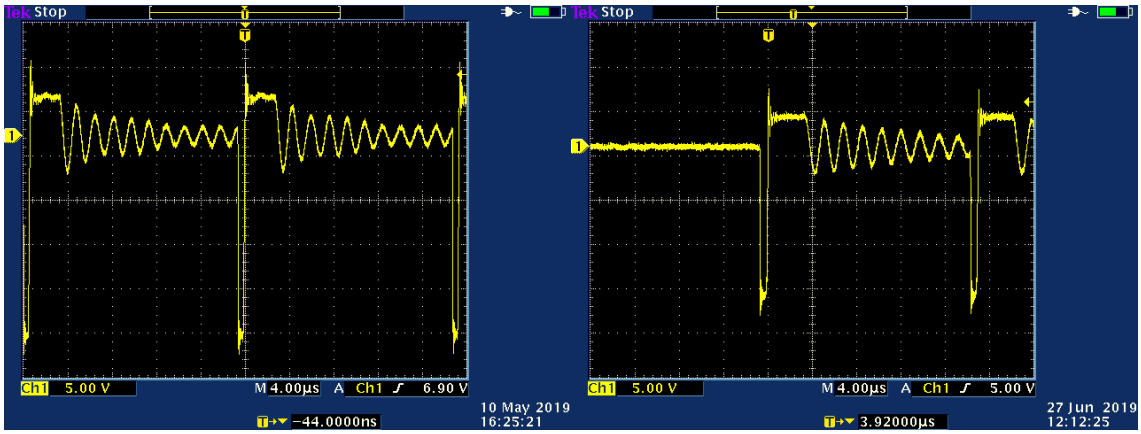



*Figure 37 Switching of a) SCT b) Mos1*

Result is revealed in Figure 37: Mos1 as the only one operates in Burst mode ([10]). This allows to reduce switching losses and as they are significant for input voltage as high as 1 kV, it makes a huge difference. In my opinion, the first area of interest – the $R_{DS\text{-}on}$ for Mos2 and the GD module for SCT – is probably the cause of normal operation instead of Burst mode, especially in case of SCT.

## 4.2 Assessment of losses estimation

In previous chapter subchapter 3.4 was dedicated to the losses estimation based on $R_{DS\text{-}on}$ and $E_{Coss}$. It is possible to divide the estimation into two categories: voltage dependent and load dependent. As each measured point was also estimated, it is not necessary, but results are more informative. Voltage dependent comparison focuses on full load for each input voltage. Because non-predictable phenomena – for instance burst mode or point of switching – wouldn't show up or are minor for full load, this estimation should be more precise.

Load dependent estimation aims to predict trend of efficiency for different load. This was done according to input voltage. The goal wasn't simply predicting the trend for each transistor, but to put them in comparison; see, if any one can be better for lower load and worse for full load. As this prediction has the same format as efficiency revealed in previous subchapter, it's presented here and put together with the measurements instead of presenting it in 3.4.3 and discussing results here.

### 4.2.1 Full load estimation

Because $R_{DS\text{-}on}$ and $E_{Coss}$ should be responsible for major transistor-related losses, MOSFETs were ranked with number according to them: higher losses → lower rank and vice versa. Same procedure was made with efficiency results for 100W load: better efficiency → higher rank. These two numbers are compared in following table according to input voltage recalculated to $V_{DS}$. Pred. stands for predicted loses and Meas. for rank based on measurement:

| **Efficiency rank** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **$V_{DS}$ [V]** | | **150** | **250** | **320** | **560** | **700** | **840** | **900** | **1000** |
| **Mos1** | **Pred.** | **4** | **4** | **4** | **4** | **4** | **3** | **3** | **2** |
| | **Meas.** | **4** | **4** | **4** | **2** | **3** | **3** | **3** | **2** |
| **Mos2** | **Pred.** | X | X | X | X | **5** | **5** | **5** | **3** |
| | **Meas.** | X | X | X | X | **5** | **5** | **5** | **3** |
| **SCT** | **Pred.** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| | **Meas.** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **Mos3** | **Pred.** | **3** | **3** | **3** | **3** | **2** | **2** | **2** | X |
| | **Meas.** | **3** | **3** | **3** | **3** | **2** | **2** | **2** | X |
| **Mos4** | **Pred.** | **2** | **2** | **2** | **2** | **3** | **4** | **4** | X |
| | **Meas.** | **2** | **2** | **2** | **4** | **4** | **4** | **4** | X |

*Table 7 Comparison of Efficiency vs Losses estimation*

Thanks to $C_{oss}$ energy estimation with capacitance nonlinearity taken into account (same as thermal variation of $R_{DS\text{-}on}$) losses estimation corresponds with measurements very accurately. Table 7 might suggest like that SCT is just overrated and Mos2 underrated for the application, but that is a misinterpretation. According to raw datasheet's numbers all transistors are similar. SCT took the first place mainly because its $R_{DS\text{-}on}$ grows with temperature not so fast as for Si-based MOSFETS; also output capacitance energy is times lower. Furthermore, the table shows only rank for 100W load – SCT was sometimes surpassed by others for lower output power. The best results were occasionally achieved with not so big advance: two times with less than one percent.

Main reason why Mos2 was included is to demonstrate that for high input voltage is important low output capacitance, even for a price of awfully high $R_{DS-on}$. I would pronounce this statement proven even with the result taken into consideration: besides the first applicable input voltage ($500V_{AC}$), the gap was always less than 1% for full load. For lower loads, results were even better: 3times second place for 25W load and once for 50 W. Reviewing the results, from my point of view Mos2 is effective equivalent to other used MOSFETs for higher input voltage.

For two input voltages the estimation was not absolutely accurate as Mos1 and Mos4 estimated ranks were swapped. Aimed at first case – 400 $V_{AC\_IN}$ i.e. $V_{DS}$ = 560 V – even Mos3 was leaped. Well, this is true just on paper: measured efficiency differs by 0.03 %, which I consider appropriate to count them as the very same value. The deviation might be neglected with statement that this was just gross estimation, but let's focus on the problematic more deeply. The midrange input voltages tested the estimation to the limits and – as it seems – went even beyond: difference between the best and the worst in losses prediction is only 1.33 W. The measurement was even closer – just 0.6% difference. As SCT is the only one not swapped or leaped, it will be set as reference.

| | Meas. [%] | Pred. [W] | Eff. drop [%] | Estim. eff. [%] | Diff [%] | $Q_G$[6] [nC] |
|---|---|---|---|---|---|---|
| Mos1 | 88.00 | 2.59 | -1.33 | 87.04 | 0.96 | 37 |
| SCT | 88.37 | 1.26 | X | X | X | 14 |
| Mos3 | 87.97 | 2.20 | -0.95 | 87.42 | 0.55 | 47 |
| Mos4 | 87.79 | 2.00 | -0.74 | 87.63 | 0.16 | 89 |

*Table 8 400 $V_{AC\_IN}$ efficiency analysis*

Parameters of interest are listed in Table 8: first column is measured efficiency and second estimated losses. Third column is difference in losses estimation toward to SCT (in Watts) which should be – for 100W load – proportional to efficiency in %. Based on third column and measured SCT's efficiency fourth column shows estimated efficiency. The next one is difference between this estimation and measurement. Last column shows datasheet value of total Gate charge $Q_G$, which is in my opinion the reason for wrong prediction. This was taken just as pure datasheet number, not as a $V_{DS}$ function: but as the measurement conditions were similar and in this case it's just for comparison, it doesn't matter much.

As mentioned before, during switch-off MOSFET partially operates in saturation region. With the same Gate resistor higher Gate charge means longer operation in saturation. The prediction was wrong in exact order of total Gate charge: Mos4 should be better than Mos3 and this better than Mos1. However, as for midrange input voltages $R_{DS-on}$ is not so critical and switching losses are still not so high, losses caused by operation in saturation region probably take important part in efficiency.

For 500 $V_{AC\_IN}$ / 700 V of $V_{DS}$ it's the same effect – as the gap between Mos1 and Mos4 is even tighter in both prediction and measurement, any additional loss can easily make a difference. Table 8 reveals another quite interesting fact: SCT was selected as reference from which efficiency for others was estimated (based on losses). As SCT has the lowest total Gate charge and additive losses are proportional to it, the difference between measured and predicted efficiency (column 5 - Diff) should be negative, but it isn't. In next subchapter I discuss the saturation region effect more deeply and I insist that it's a valid theory, so there must be another principle of SCT efficiency drop off. Gate-Drive module definitely participates, but not in major way – as predicted in 3.2.2. In my opinion, this might be caused by inaccuracy in datasheet and/or SPICE model: SCT's used in measurements in this thesis were engineering samples, not for

[6] Values taken from datasheets [16] [17] [14] [13] [15]

market production. Reviewing chapter one, SiC devices manufacture process is quite complicated, thus variation from typical parameters listed in datasheet is probable. Because I was unable to measure $R_{DS\text{-}on}$ or $C_{oss}$ curve more precisely, this is just a theory.

### 4.2.2 Estimation of efficiency depending on the load

The goal of the estimation was to determine efficiency trend of transistors for each input voltage. As discussed above, just three parameters were included: $R_{DS\text{-}on}$, $C_{oss}$ and parasitic capacitance. Because input of 150 $V_{DC}$ is boundary condition with several unpredictable effects, estimation wasn't so precise. For 230 $V_{AC}$ the result was better – demonstrated in Figure 38:

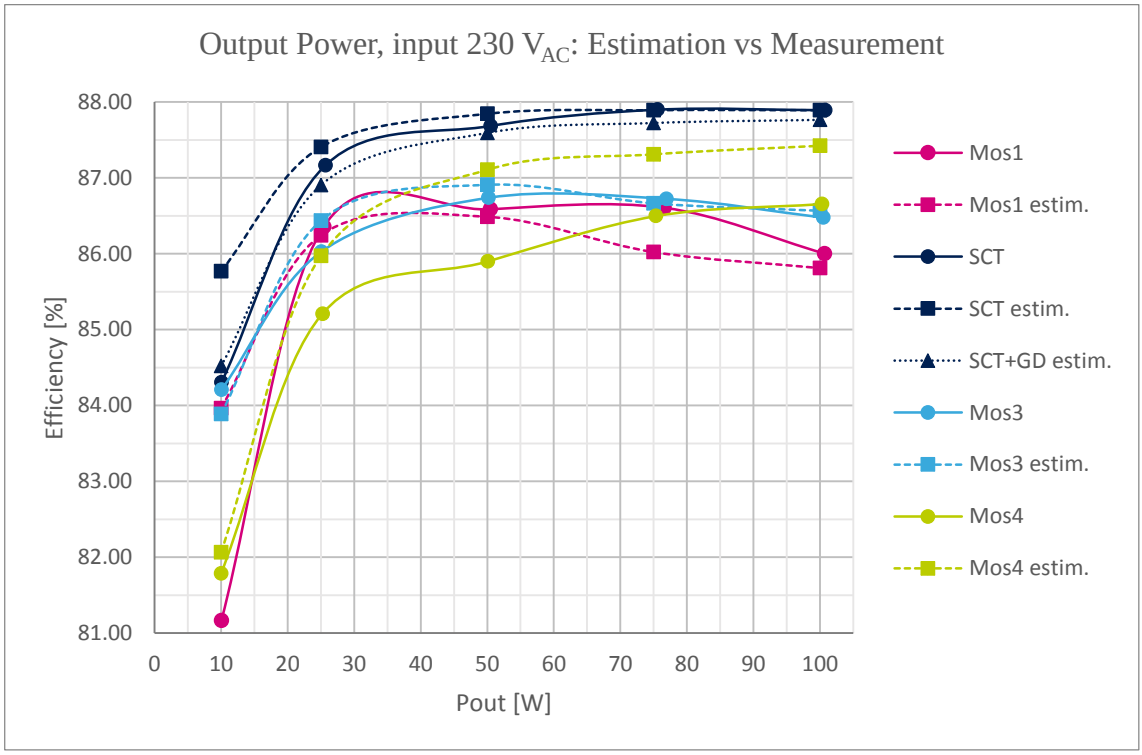



*Figure 38 Estimation vs measurement for 230$V_{AC}$ input*

Chart shows measured data (the very same as in Figure 32) with full lines and round points. Estimated values are represented with square points connected with dashed lines. The data was connected according to the following procedure: losses were recalculated as an efficiency drop, therefore the trend should be the same. Second step was shifting the traces along the efficiency axis – full load for SCT was chosen as a reference point, to which estimated and measured values were set equal. All traces were shifted by the same offset to fulfill this condition.

Estimated efficiency for SCT was surprisingly inaccurate for 10W load. As an attempt to correct it, estimated power consumption of Gate-Drive module was included. This was determined (based on measurement – Table 1, expected VCC voltage and duty cycle) to be 125 mW. As this mainly affects low load, the value should correspond to 10W load. Because the change with duty cycle was minor, it was added as constant to all SCT points. This trace is named SCT+GD estim. (triangular points and dotted line) and tracks measured efficiency more accurately. Efficiency of other transistors was estimated more precisely except for Mos4 and 10W load of Mos1. Effects besides the wrong estimation are discussed later for both: in 0 *the worst possible case of switching for FF operation* is revealed and this applies for Mos1 with 10W load. This is also partially the case of Mos4, but I believe that another phenomenon – an operation in saturation region during switch-off (4.3.2) – might be more significant.

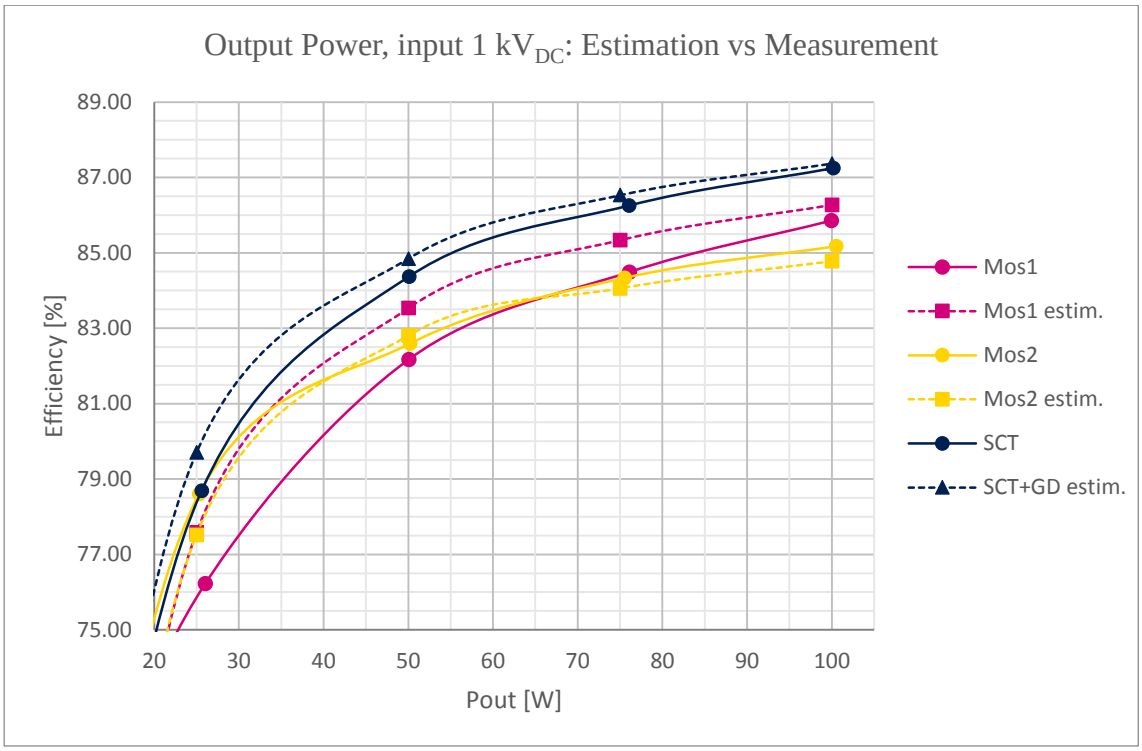



*Figure 39 Estimation vs measurement for 1kV$_{DC}$ input*

For higher input voltages the estimation was similarly precise as for 230V$_{AC}$ input. Unfortunately, there were some differences, especially one already discussed with no satisfying explanation: for input of 500 V$_{AC}$ shown in Figure 33 Mos3 was noticeably better than SCT for loads of 50 and 75 W. Estimation predicted the efficiency better for SCT – Mos3 was estimated slightly worse than measured, but main difference was for the SCT. These and others input voltages are not demonstrated here because of worse charts clarity and no other informative reason. For further observation measured and estimated data are located in digital attachment \Attachments\Efficiency.xlsx and \Losses.xlsx.

Upper boundary condition is presented instead in Figure 39 – the 1 kV$_{DC}$ input. Because of burst mode and point of switching estimation for 10W load differs a lot. The rest of values was estimated better: besides Mos1 measurements track the prediction quite accurately. Mos1 efficiency measurement for 1kV$_{DC}$ input was sort of *bad luck*: its point of switching was always around upper peak of oscillation, which causes higher switching losses (illustrated in Figure 40). This *bad luck* was compensated for 10W load: because burst mode and lower peak switching its 68.4% efficiency was above any other measured or estimated for 1 kV$_{DC}$.

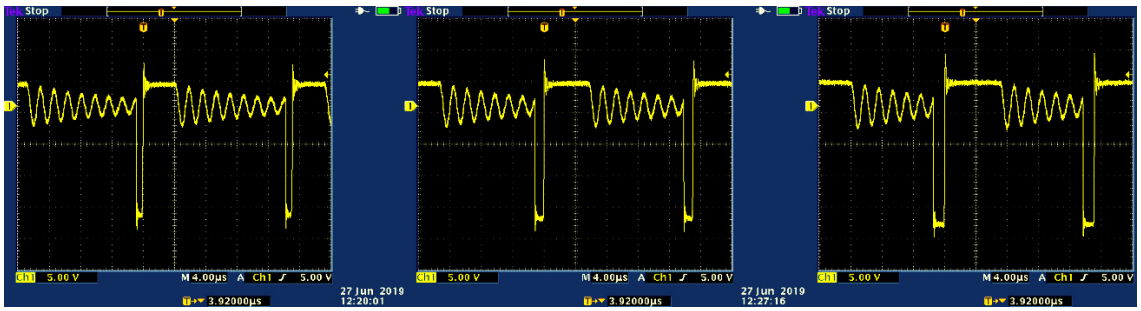


*Figure 40 Mos1 a) 25W load* *b) 50W load* *c) 75W load for 1kVDC*

## 4.3 Switch-off behavior

Switching behavior is important parameter for every transistor. As mentioned in subchapter 3.4, only switch-off behavior is interesting since the converter operates in DCM; therefore, this section reveals only them.

### 4.3.1 Slew rate

If listed in datasheet, this parameter defines maximum allowed slew rate of $V_{DS}$ for safe operation. Also, it can be limited by transistor's maximum frequency, which can negatively affect switch-off behavior. None of this shows up as important in this application – because switching frequency was selected reasonably low and primary winding peak current should not exceed 2.84 A.

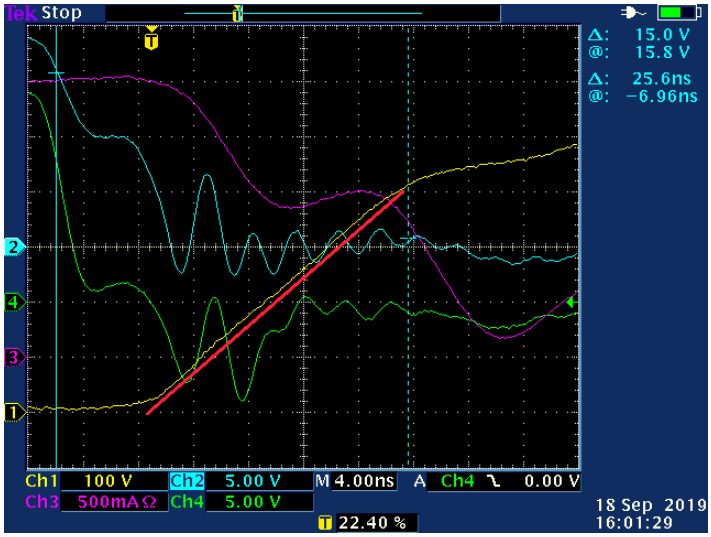
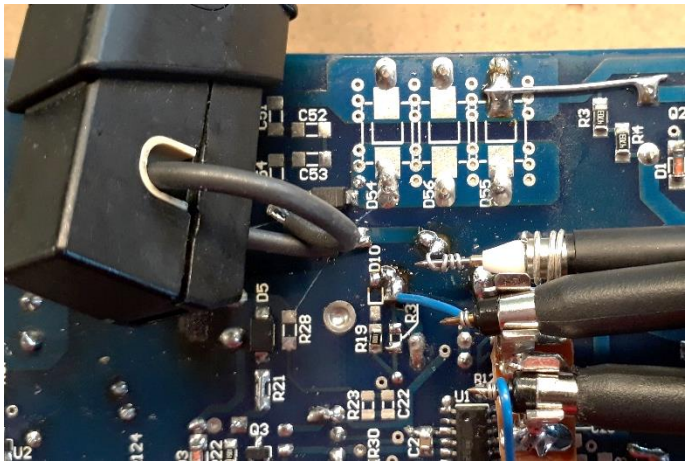



*Figure 41 SCT slew rate; Ch1 – $V_{DS}$*

This is demonstrated in Figure 41, which shows SCT's switch-off . Yellow trace is $V_{DS}$, which after channel switching off starts rising almost linearly. Red line next to it is equivalent slope of Drain current charging parallel combination of $C_{oss}$ and transformer capacitance. This was measured for full load and for every used transistor with more or less same result. Therefore, slew rate effect for this application was neglected.

### 4.3.2 Operation in saturation region




As mentioned in 3.4 and also previously in this chapter, during switch-off transistors operate in saturation region. Not all energy flowing into transistor is dissipated, part of it is stored in output capacitance. Theoretically, both parts should be dissipated: losses caused by saturation are dissipated during switch-off, energy stored in $C_{oss}$ during switch-on. Hence energy flowing into MOSFET calculated by definition (eq. (23)) should be equal to overall switching losses. Unfortunately, this is not correct estimation as $V_{DS}$ after switch-off and before switch-on (thus $C_{oss}$ energy) differs – immediately after switch-off there is voltage spike caused by leakage inductance + reflected secondary voltage. Therefore, intention was to at least partially separate losses caused by saturation and $C_{oss}$ to determine if statements in previous subchapter were correct. This requires special consideration to used probes: to minimize their parasitic inductance, they were connected with as small input loop as possible – illustrated in

Figure 42. Also time skewness caused by various probe cables and electronics in current probe was corrected. Following signals were measured: Gate-Drive (before $R_G$, output from GD module or directly from controller), Gate voltage, Drain voltage and Drain current. From Drain voltage and current instant power was calculated, from this waveform energy was calculated according to eq. (23).

All measurements were made for 150 $V_{IN}$, hence Mos2 was not included. Switch-off transient can be divided into three parts: first is normal operation, MOSFET is fully switched on and current is rising. Second – transistor starts limiting current, thus $V_{DS}$ starts rising. The third part starts when no current flows through channel – current charges just Coss and starts decreasing as it charges also transformer capacitance, which is excluded from measured circuit. This is highlighted in Figure 43, borders between parts are approximately set by red cursors.

*Figure 42 Probes connection*

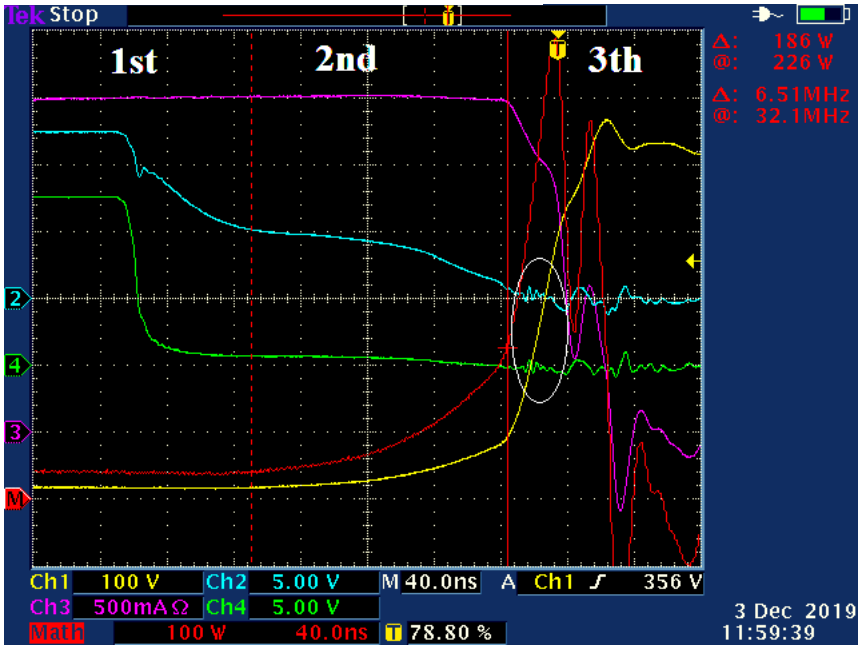



*Figure 43 Measured switch-off of Mos4 ($R_G$ = 10 Ω); Ch1 – Drain, Ch2 – Gate, Ch3 – Drain current, Ch4 – Gate-Drive, Math – Ch1·Ch3*

To determine losses caused by saturation, instant power from exported Math waveform was integrated according to equation (23). Proper selection of integration bounds was indeed a question. More precisely the upper one, lower one is defined as a border between the first and the second part of switch-off transient – moment when current stops rising. For overall switch-off energy measurement (sometimes listed in datasheets) moment when instant power drops to zero (or very close to it in case of no oscillation) is usually selected as upper bound. Unfortunately, in this case current was measured with current probe using ferromagnetic core, i.e. additional inductance was added. Therefore, huge oscillations appear as $C_{oss}$ creates resonant circuit with it. Using this upper bound also includes $E_{Coss}$ in its maximum value – for saturation losses determination is $E_{Coss}$ subtracted, but any inaccuracy of this energy causes bigger error of the determination. Two calculations were made: one with upper bound described above and another as border between second and third part. The second approach brings more trustworthy results and is presented here; first one was rejected as not applicable for this measurement, mainly because of the oscillations and $E_{Coss}$ inaccuracy.

Border between second and third part – i.e. upper bound – was defined right before minor oscillation on Gate (inside white circle in Figure 43, visible on Ch2 and Ch4). This is in my

opinion not caused by the closure of the channel (as similar oscillations are observable during closure of PN junction). It would make them the border by definition, but channel should be closed already (Mos4 threshold is ≥ 3 V). Until this point MOSFET could operate in subthreshold region. These might be oscillation between Gate capacitance and parasitic inductance of pins and PCB traces at the end of Gate-discharging transient. Selecting this as upper bound should include even subthreshold region and as $E_{Coss}$ is still tiny, any wrong estimation of it shouldn't matter much.

Finally, to determine the switch-off losses, another two approaches were selected. As they both have its limits, they were chosen to be the minimum and maximum of possible range of losses. They are calculated for $R_G$ = 10 Ω as the efficiency was measured for this value – results are in Table 9. First approach uses another $R_G$ = 1 Ω – total switch-off energies are listed in third column $E_{off}$. As lower $R_G$ discharges the Gate faster, thus less time is spent in saturation, energy for lower resistance is also lower. As any other parameter has not changed, losses caused by saturation have to be always equal or higher to the difference between these two energies. Therefore, this was stated as minimum energy dissipated in saturation – 7th column $E_{sat\_min}$.

| | | $E_{off}$ [µJ] | $V_{DS\_stop}$ [V] | $E_{Coss}$ [µJ] | $E_{pr}$ [µJ] | $E_{sat\_min}$ [µJ] | $E_{sat\_max}$ [µJ] | $P_{sat\_max}$ [W] |
|---|---|---|---|---|---|---|---|---|
| Mos1 | 10 Ω | 10.294 | 125 | 1.940 | 0.1016 | 0.629 | 8.252 | 0.423 |
| | 1 Ω | 9.665 | | | | | | |
| SCT | 10 Ω | 0.512 | 40 | 0.048 | 0.0104 | 0.259 | 0.453 | 0.023 |
| | 1 Ω | 0.253 | | | | | | |
| Mos3 | 10 Ω | 9.419 | 100 | 1.960 | 0.0650 | 0.678 | 7.394 | 0.379 |
| | 1 Ω | 8.742 | | | | | | |
| Mos4 | 10 Ω | 13.289 | 100 | 3.640 | 0.0650 | 0.050 | 9.584 | 0.492 |
| | 1 Ω | 13.239 | | | | | | |

*Table 9 Determination of saturation losses*

The second approach uses just energy measured for $R_G$ = 10 Ω, from which any other known energies are deducted: energy stored in output capacitance (5th column $E_{Coss}$) and energy stored in the connected probe capacitance (this was measured as 13 pF in 3.4.2). $E_{Coss}$ was simulated and as probe capacitance is assumed linear, its energy (6th column $E_{pr}$) was calculated simply using eq. (22). Maximum possible dissipated energy $E_{sat\_max}$ was calculated by subtracting these energies from $E_{off}$, thus multiplying by switching frequency results in maximum power $P_{sat\_max}$.

### 4.3.3 Further observation of saturation losses and limits of used method

Losses caused by saturation described in previous section should be in range listed in Table 9. As the range is quite wide, it requires few comments. Starting with Mos4, according to measurement it is possible that it has the lowest saturation losses $E_{sat\_min}$. Taking its Gate charge and efficiency measurement into consideration, this seems to be highly improbable. Reason for this result is simply the limit of used method. As $E_{sat\_min}$ was stated using two different Gate resistors, it presumed that time of Gate discharging is mainly proportional to this resistance. Especially in case of Mos4 another two parameters are important: Gate driver sink current

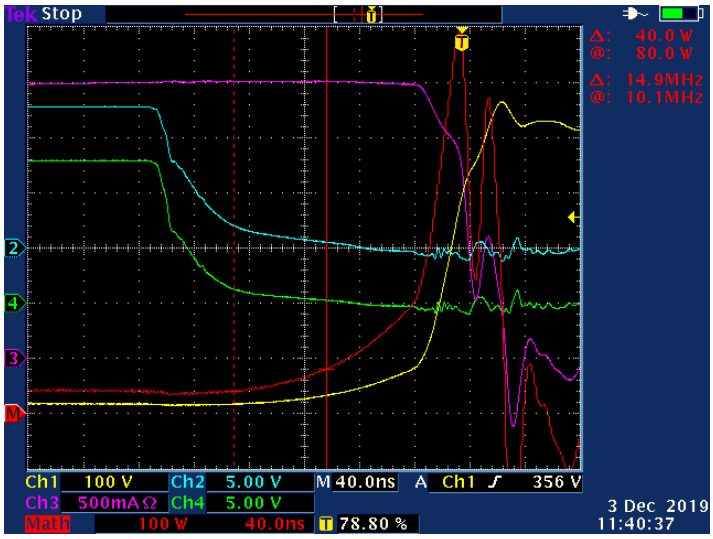



*Figure 44 Mos4 switch-off with 1Ω gate resistor; Ch1 – Drain, Ch2 – Gate, Ch3 – Drain current, Ch4 – Gate Drive, Math – Ch1·Ch3*

capability and Mos4 intrinsic Gate resistance. L6566BH's internal Gate driver provides sink current 0.8 A (min) which is usually sufficient, but in this case it also affects the result. Previously in Figure 43 Gate drive (Ch4 – Green) drops closely to zero in less than 10 ns, thus its sink current capability has minor effect. Whereas with 10Ω $R_G$ this takes approx. 50 ns (Figure 44) and because the voltage difference between Gate (Ch2) and Gate drive (Ch4) is less than one volt (it ought to be mentioned that Ch2 is shifted above Ch4 by 1 div.), it seems to be limited by sink current capability. It is also true that this has little effect as it happens almost only during first part of switch-off transient (defined previously in 4.3.2), therefore it is excluded from $E_{off}$ integral.

Intrinsic Gate resistance might be more impressive: Gate trace (Ch2) in Figure 43 falls below Mos4 Gate threshold voltage (min 3 V) later than in Figure 44, but counting in the effect of voltage drop on intrinsic Gate resistance makes them very similar. Taking $Q_G$ from datasheets (listed in Table 8) as linear capacitor (which is not) charged to $V_{GS}$ = 10V (and 20 V for SCT) it could be simplified as RC circuit with intrinsic resistance and its time constant $\tau = R \cdot C$ can be calculated: 21.4 ns for Mos4, 14.1 ns for Mos2 and Mos3 and 6.7 ns for SCT. These values are useful only for comparison as Gate charge is also highly nonlinear (illustrated in Figure 45). However, this points at important fact: time for discharging this capacitor (3times $\tau$, approx. to 5%) nears to time of switch-off. To determine minimum achievable switch-off time this was simulated again for Mos4 and it turns out to be 126 ns for $I_D$ = 2.5 A; nearly the same value as measured with 1Ω $R_G$ and not so far from 10Ω $R_G$ either. As both of test conditions are close to the limit value, it's not a surprise that their difference stated as minimal energy of saturation losses $E_{sat\_min}$ is so low. Theory that this is caused by the saturation instead of charging $C_{oss}$ (which would explain why lowering $R_G$ didn't have any effect) was also confirmed by the simulation: using negative voltage to switch Mos4 off shortened the transient to approx. 80 ns.

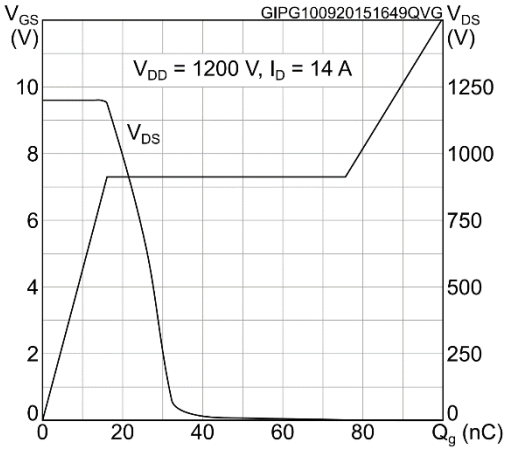



*Figure 45 Mos4 Gate charge vs $V_{GS}$; credit: [15]*

Theory that operation in saturation region has affected efficiency results, especially in case of Mos4, have been discussed for 150$V_{DC}$ input (Figure 31) and 400$V_{AC}$ input (Table 7 & Table 8). This is more interesting for 400$V_{AC}$ input because of the miscalculation of losses estimation (Mos4 and Mos1 swapped their estimated order – 2 and 4; skipping Mos3 on the third). Subtracting estimated maximum power caused by saturation ($P_{sat\_max}$ in Table 9) from the efficiency would solve the skipping of Mos3, but not the order swapping. Based on previous two paragraphs, Mos4 saturation losses are probably close to $P_{sat\_max}$. This is not true in case of Mos1, therefore assuming its $P_{sat\_max}$ as half would solve the swapped order phenomenon. Unfortunately,

this is not correct assessment as I can't make any estimation where in the stated range the energy dissipated due to saturation is located.

As for Mos4 $E_{sat\_min}$ was calculated lower than expected, for SCT opposite problem was revealed despite its low Gate charge. This most probably uncovers another limit of this measurement: used equipment. Current probe used for this measurement was Tektronix TCP202A with 50 MHz bandwidth, which might be insufficient for this purpose. It was measured that used probe is capable of transfer sine wave up to 80 MHz, but with lower amplitude. Also phase delay variates a lot with higher frequency. Switch-off transient of SCT is shown in Figure 46 and as it can be seen many phenomena are above 50 MHz bandwidth: for instance the most significant Gate oscillations have frequency of approx. 260 MHz. For illustration time axis is 4 ns per divide, period of 50 MHz is 5times higher. As Tektronix provides no information about TCP202A slew rate, it is my firm belief that in combination with bandwidth current was measured inaccurately in case of SCT and actually it decreased faster than in Figure 46.


*Figure 46 SCT switch-off with 1Ω $R_G$; Ch1 – Drain, Ch2 – Gate, Ch3 – Drain current, Ch4 – Gate Drive, Math – Ch1·Ch3*

## 4.4 Quasi-resonant operation

Quasi resonant, also called boundary-condition mode, senses transformer core demagnetization after off-time and switches on subsequently. Opposed to fixed-frequency converter, switching frequency changes with any factor affecting core flux: mostly input voltage and output load. Advantage of this mode is for instance lower secondary winding peak current for lower load (as there is no *wasted* idle time $t_{res}$, frequency increases, thus from eq. (3) lower secondary peak current). Benefit of this is lower current ripple into output capacitors, but mainly lower average current through output diode, which means lower losses. Also quasi-resonant can't go to CCM as its operation consist of sensing core demagnetization. On primary side, the effect for lower load can be disputable in this case: resistive losses decrease with higher frequency as on-time shortens. On the other hand, this increases switching losses, because they are proportional to frequency instead of load.

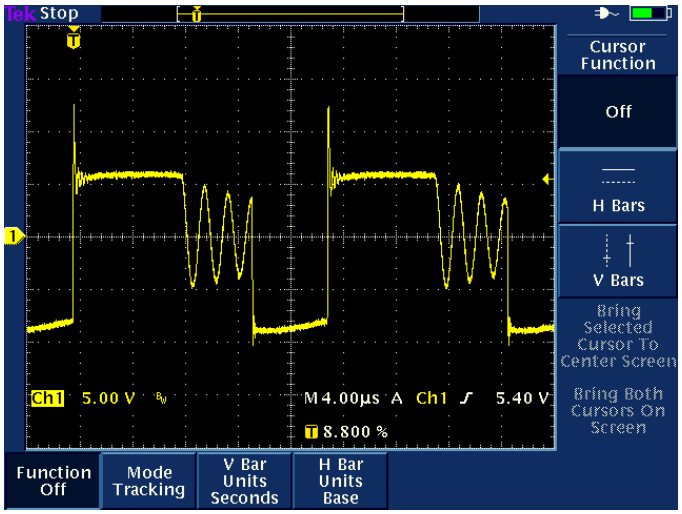



*Figure 47 Fixed-frequency switching*

Reason why this was taken into consideration for this application is the way of demagnetization sensing: L6566BH uses auxiliary winding voltage falling below zero. After discharging core flux, primary winding parasitic capacitance (as this is usually the major one) starts oscillating with leakage inductance and this is transformed to other windings. This oscillation can be seen in Figure 47 with another character typical for fixed-frequency operation: converter might switch on during upper peak of oscillation, therefore dissipates higher $C_{oss}$ energy. As switching in QR is triggered by negative-going edge falling below defined value (−50mV in this case), with additional process delay switch-on usually comes out around lower peak → minimum $C_{oss}$ energy is dissipated. The delay between triggering and switching is discussable, but even if it was negligible, it still switches during the lower half of oscillation. For entire input voltage range and for any load, point of switching for FF converter in relation to oscillation can be considered absolutely random, thus it should be proportional to the average value of the oscillation. As QR always switches bellow this value, its overall efficiency should be better.

### 4.4.1 Comparison between QR and FF

To verify statement in last sentence of previous section, efficiency for quasi-resonant mode was also measured. This was compared mainly between SCT, Mos3 and Mos4, because Mos3 was better than SCT for midrange input voltages with 50W and 75W loads and Mos4 have the highest output capacitance. As switching frequency in QR mode grows with lower load, there is an upper limitation on it. As soon as the converter reaches this point, it starts operating in *valley skipping* mode: additional delay regulated with feedback is put before triggering, for lower load switch-on is delayed by $n$ oscillation periods ($n$ = 1, 2, 3, …) hence it's called valley skipping. For shorter delay it is casual QR operation as $n$ = 0. For light load burst mode on the limiting frequency is enabled. For first testing, the limitation was set to 100 kHz.

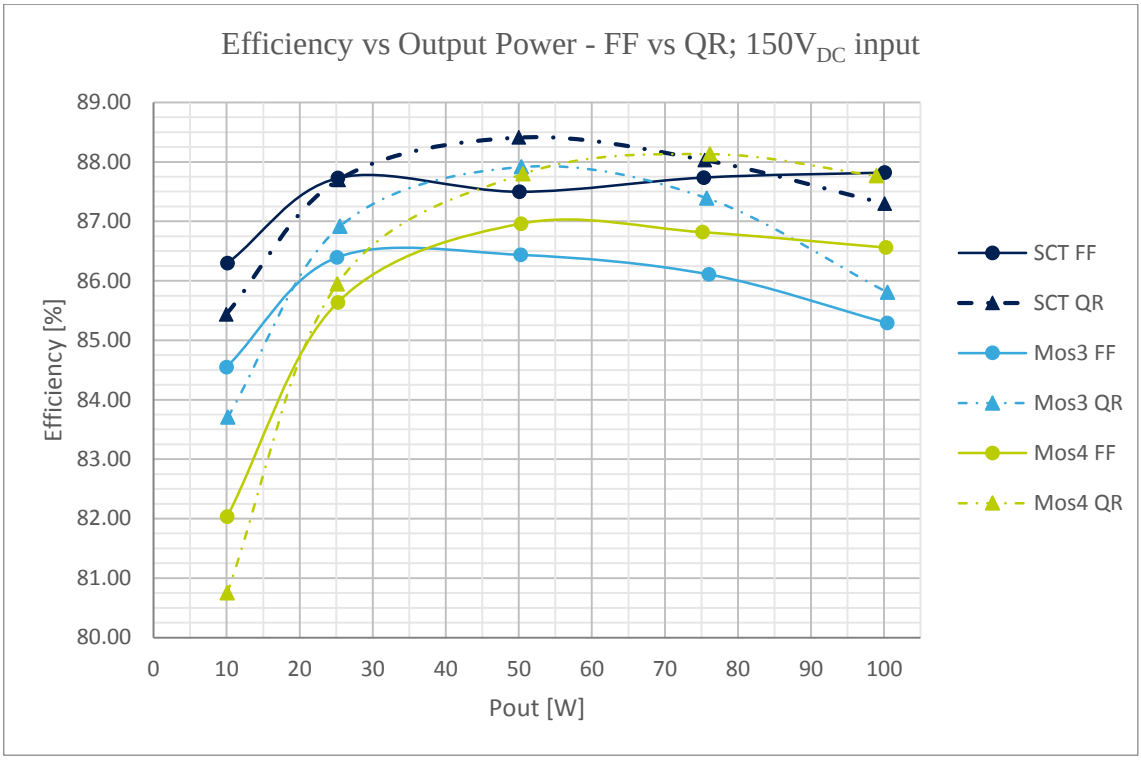



*Figure 48 Comparison FF vs QR for input voltage 150 $V_{DC}$*

Starting with SCT, the difference is about almost 1% better efficiency for 50W load. This might be indeed pure effect of QR, because for fixed frequency this was exactly the case of worst possible switching: the upper peak of oscillation. However, this may sound improbable as SCT has the lowest $C_{oss}$ losses and the input voltage is low. It is also true that not only $C_{oss}$ can affect it – as revealed before, transformer parasitic capacitance has major effect and also resistive losses might change. To observe this, another losses estimation was made.

From indirect measurement demonstrated in Figure 49 – a) was stated that for fixed frequency SCT switches on at $V_{DS}$ approx. ¾ of voltage plateau, which consist of input voltage and reflected secondary voltage. Considering secondary winding voltage 24.5 V (including diode drop), $V_{DS}$ at the point of switch-on was calculated as 259.5 V, thus for 87 pF of parasitic capacitance it means 0.15W loss. As predicted, this is higher than $C_{oss}$ losses, which are 0.04 W. On-time for FF operation was 8 µs, thus resistive losses were equal to 0.6 W. Consequently, overall SCT losses were estimated as 0.79 W.

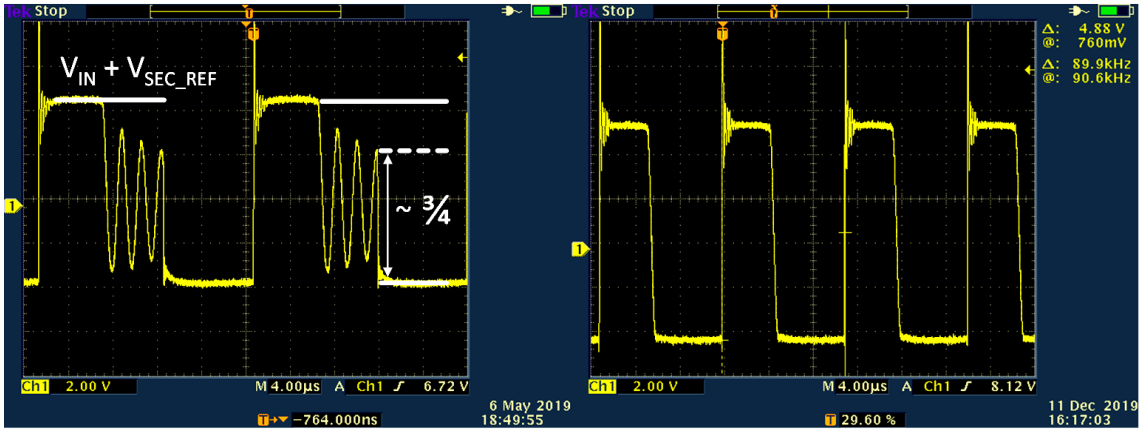



*Figure 49 a) fixed-frequency switching* *b) quasi-resonant switching*

From Figure 49 – b) it's obvious that also resistive losses decrease as on-time shortens to just 6 µs. The result of this is 25% drop to 0.45 W. Furthermore, thanks to switching during lower oscillation peak, switching losses should be minimized. Considering them as negligible, benefit of QR according to estimation is 0.34 W, which means for 50W load 0.68 % better efficiency. Besides MOSFET effects, output diode could have improved the efficiency either: lower average current means lower losses and as D17 is a Schottky diode, losses caused by reverse recovery charge (typical for PN diodes, proportional to switching frequency) do not apply.

The way of demagnetization sensing is partially a disadvantage for full load. This applies to SCT and especially for Mos3: as at least one eight of oscillation period has to appear to trigger another switch-on (additional delay nears it to one quarter), switching frequency is lower for QR than for FF. This effect also extends both on-time and off-time in order to transfer the same power using lower switching frequency – eq. (3) and (5). It is also possible that for input voltage 150 VDC and full load the power margin wasn't adequate and converter operated in soft CCM. Switching frequency reduction caused by QR wasn't so dramatic as it is illustrated in Figure 50 – just slightly above 5 %. However, as resistive losses rise with square of $I_{RMS}$ and this is proportional to on-time, it has negative effect on efficiency: for SCT QR is worse than FF, for Mos3 the benefit of QR for full load is much lower than for 50 and 75 W. This didn't affect Mos4 so much because of its low on-state resistance and high $C_{oss}$ – effect of lower $f_{SW}$ was probably more significant on switching losses than on resistive.

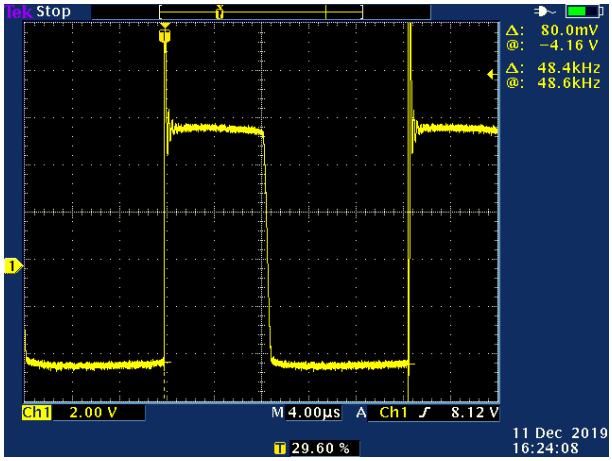



*Figure 50 SCT switching for 100W load, QR and 150 $V_{IN}$*

Another disadvantage is obvious for low load: as limit of switching frequency was set to 100 kHz and QR operates near there for 10W load (valley skipping mode, according to frequency of oscillation $f_{SW}$ is marginally lower), switching losses are almost double as for $f_{SW}$ = 51.3 kHz.

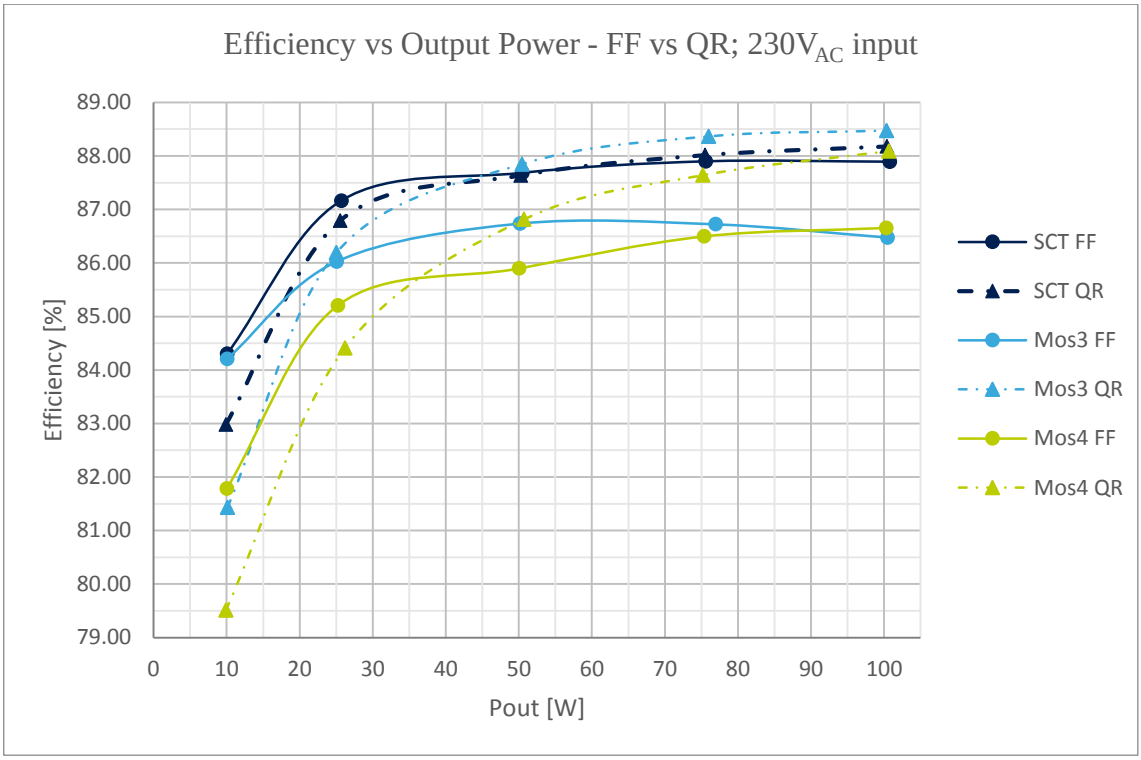



*Figure 51 Comparison FF vs QR for input voltage 230 $V_{AC}$*

As circumstances caused by boundary condition of lowest input voltage and full load won't apply for any other input voltage, the benefit of QR remains even for 100W output power; efficiency demonstrated in Figure 51. Unfortunately, there is noticeable drop for lower loads as switching frequency rises and with it switching losses. Comprehensive analysis of the results (especially for full load) wasn't feasible because for input voltage 230 $V_{AC}$ voltage ripple on input capacitors is huge. As a result, $V_{DS}$ and switching frequency variates, therefore without statistical distribution precise determination of resistive and switching losses effect is impossible. For full load switching frequency variated in range 80-100 kHz for all measured transistors.

Nevertheless, QR improved efficiency mostly for Mos3 and Mos4, but effect on SCT was marginal. The reason why might be the following: first – for full load – despite to huge voltage ripple on input capacitors, SCT switches mostly around lower oscillation peak – Figure 52. With same inference as done before for 150 $V_{DC\_IN}$ voltage should be approx. 75 V/div. Considering point of switching in Fig. 47 as 200 V and first lower peak as 140V, losses for FF caused by parasitic capacitance are 89 mW and 31 mW by $C_{oss}$. Assuming QR switching with average frequency 90 kHz and during first lower peak, these losses are 77 mW, respective 32 mW (higher value is due to $f_{SW}$, $C_{oss}$ energies are 605 nJ for $V_{DS}$ = 200 V and 350 nJ for 140 V). Lower resistive losses can explain the 0.29% better efficiency. For lower loads the oscillations are more damped, therefore lower variation from average value. Considering FF switching for lower loads

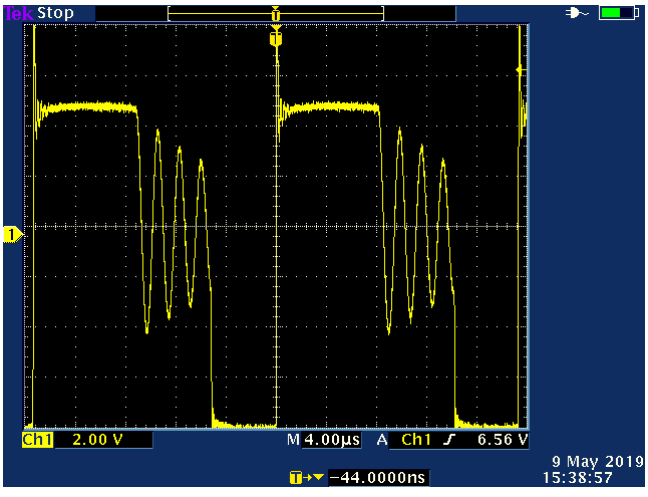



*Figure 52 Switching of SCT for FF, full load and 230$V_{AC}$ input*

always around 325 V (rectified input voltage), overall switching losses were estimated before as 299 mW. This should lead to maximum possible QR switching losses reduction of 179 mW, which means 1.79% rise of efficiency for 10 W. Reviewing the results, the effect is almost the opposite.

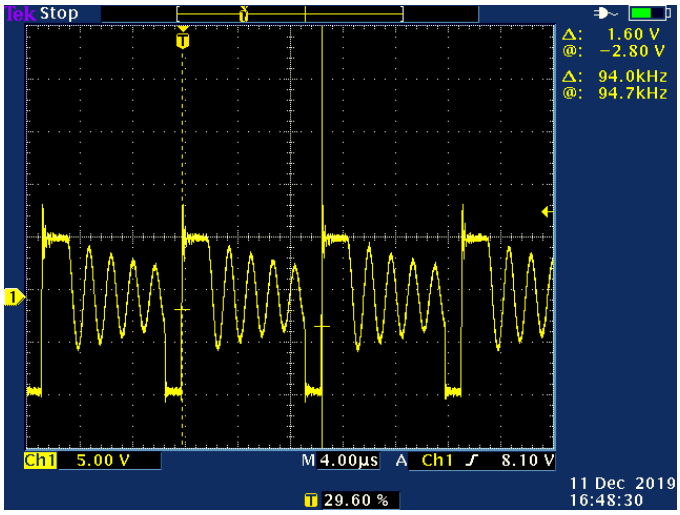



*Figure 53 Switching of SCT for QR, 10W load and 230$V_{AC}$ input*

Truth is, that the estimation is correct about the maximum possible reduction, but this is not achievable. As switching frequency reached the limit already for full load, for lower loads converter is forced to operate in valley skipping mode or burst mode. In Figure 53 the case for 10W load is shown – point of switching is during fifth lower peak, which means that $V_{DS}$ should be above 200 V (as this was the voltage of fourth lover peak previously). However, assuming it as 200 V with switching frequency 94 kHz, switching losses are 220 mW, hence the maximum benefit is only 79 mW, but perhaps less as $V_{DS}$ was underestimated. Additionally, Gate-Drive module power consumption was measured for $f_{SW}$ = 51.3 kHz and not for every possible frequency of QR. However, power consumption grows with $f_{SW}$ slightly more than proportionally: besides standard switching losses, recuperation doesn't work for higher frequencies and lower on-time (because of the parasitic capacitance effect; discussed in 3.2.2 – Figure 25). The effect of GD module is questionable: it is true that higher frequency worsens power consumption, but shorter on-time should have the opposite effect. Either way it lowers 10W efficiency by 1% for every 100 mW of power consumption and based on its measurement (Table 1) it definitely can be around 100 mW.

For Mos3 the situation is different: first, its point of switch-on for full load drifts between both lower and upper peaks. More importantly – due to higher output capacitance and $R_{DS\_ON}$ the effect of QR is better. Switching losses for average oscillation voltage and FF are 461 mW; theoretical maximum benefit of QR for 90 kHz is 253 mW. As this is only minor improvement, significant change is due to resistive losses: for full load they were estimated as 2.51 W for FF, from indirect measurement for QR were recalculated as 1.42 W. Including both, estimated efficiency is 1.34% better for QR than for FF. For measured efficiency the difference is 1.99% which seems correct: calculations were made for the same conditions, but lower power dissipation means lower transistor junction temperature, thus lower $R_{DS\_ON}$ and lower losses.

Additional improvement of efficiency due to thermal drift of $R_{DS\_ON}$ is in my opinion key factor of better results for Si-based transistors (Mos3 and Mos4), especially for full load. SiC technologies have usually lower thermal variation of $R_{DS\_ON}$ than Si, described on used SCT in Table 4: there is 25% rise of on-state resistance for junction temperature 125°C in comparison to 25°C. The highest one is for Mos4: 225%. This ought to be the reason of efficiency improvement for QR despite low $R_{DS\_ON}$ for Mos4 – the lowest on-state resistance of used transistors is just for 25°C. With estimated switching losses of 667 mW for Mos4 there can be partial improvement also in this field, however QR can lower them just to 469 mW (considering point of switching as before 140 V and switching frequency 90 kHz). Unfortunately, for lower load it's the same situation as described before with SCT in Figure 53, which explains the same drop as for others.

### 4.4.2 Effect of voltage and maximum frequency on QR

In previous section QR was presented as beneficial, at least for Si-based MOSFETs. It was shown that switching during lower peak can reduce switching losses, but as for low voltage resistive losses were estimated to be dominant (Figure 30; 3.4.3), main improvement was due to lower on-time. For midrange and high input voltage point of switching should be more important: switching losses grow with voltage, linear part grows with square. As effect on SCT was rather marginal, for Si transistors potential to take the first place in efficiency for midrange $V_{IN}$ was expected, because Mos3 had already better efficiency for lower load and the gap was very close.

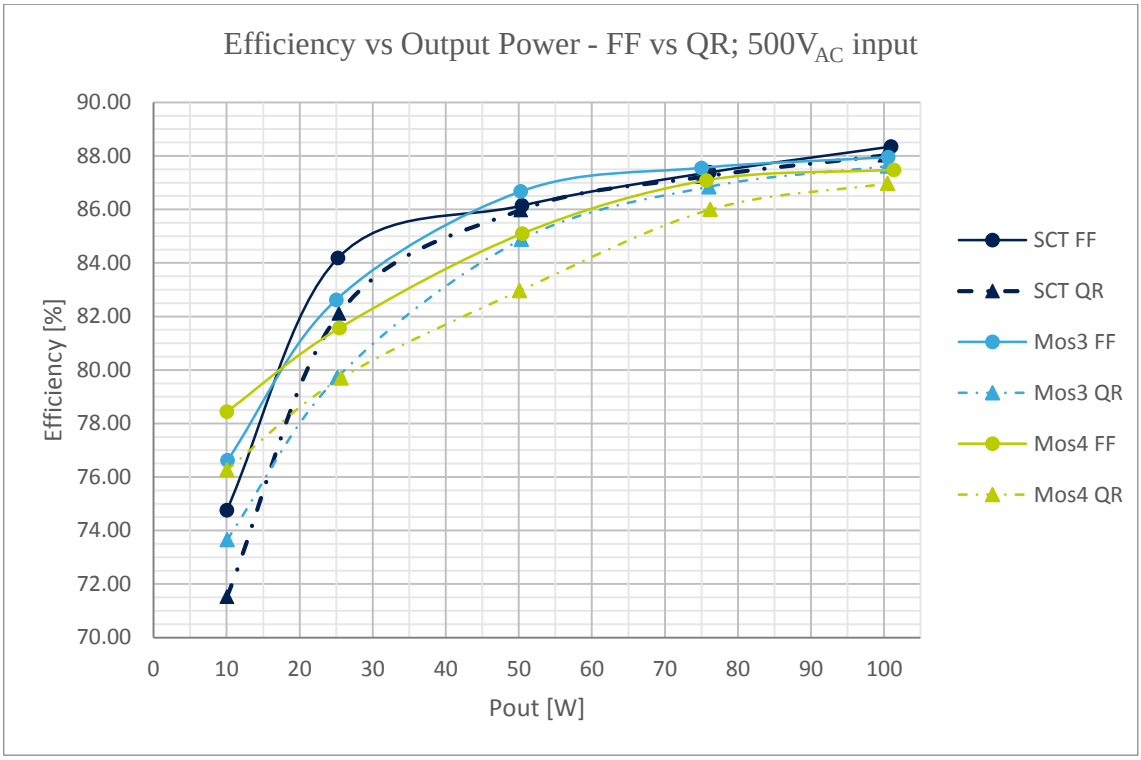



*Figure 54 Comparison FF vs QR for input voltage 500 $V_{AC}$*

The results were not so good, but expectable – for input voltage 500 $V_{AC}$ not a single point of measurement was better for QR than FF (Figure 54). The reason why is simple: as QR reached the limit of switching frequency already for input voltage 230 $V_{AC}$, for higher input voltage it is forced to operate in valley skipping mode even for full load. Described on Mos3 shown in Figure 55 with approx. 260 V/div.: point of switching is 580 V which means for $f_{SW}$ = 98.4 kHz switching losses are 2.32 W, while for FF with lower $f_{SW}$ they were just 1.68 W. Unfortunately, on-time was not the point of interest while the measurement was done, thus for better accuracy it was estimated again as 1.62 µs. Hence QR resistive losses are 0.60 W while for

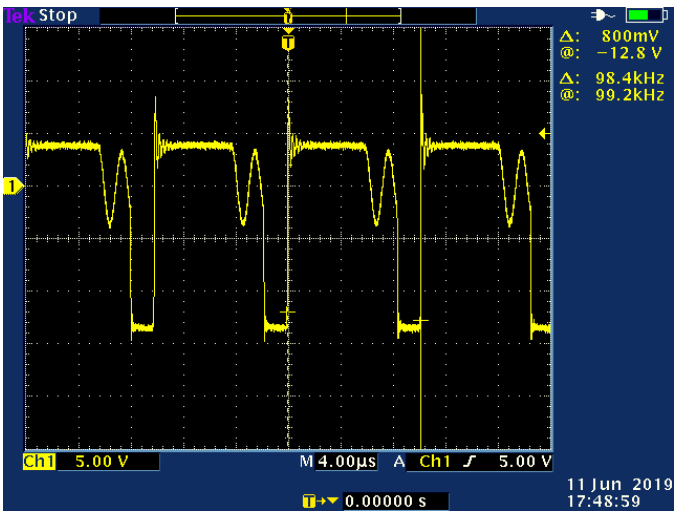



*Figure 55 Switching of Mos3 for QR, full load and 500V$_{AC}$ input*

FF they were estimated to be 0.85 W. Overall losses difference is 0,39 W and difference in efficiency is 0,34%, which validates this estimation as quite precise. As switching frequency remains similarly near the limit even for lower load, switching losses can only increase as voltage of lower oscillation peak grows up with another valley skipped. This makes QR even worse for lower loads than FF.

Effect described for $V_{IN}$ = 500 $V_{AC}$ is the same for any other higher input voltage. 400 $V_{AC}$ is the last input with beneficial QR efficiency, but negligible and only for load ≥ 50 W. As this is mainly because of switching losses, another measurement was done with frequency limit of 60 kHz.

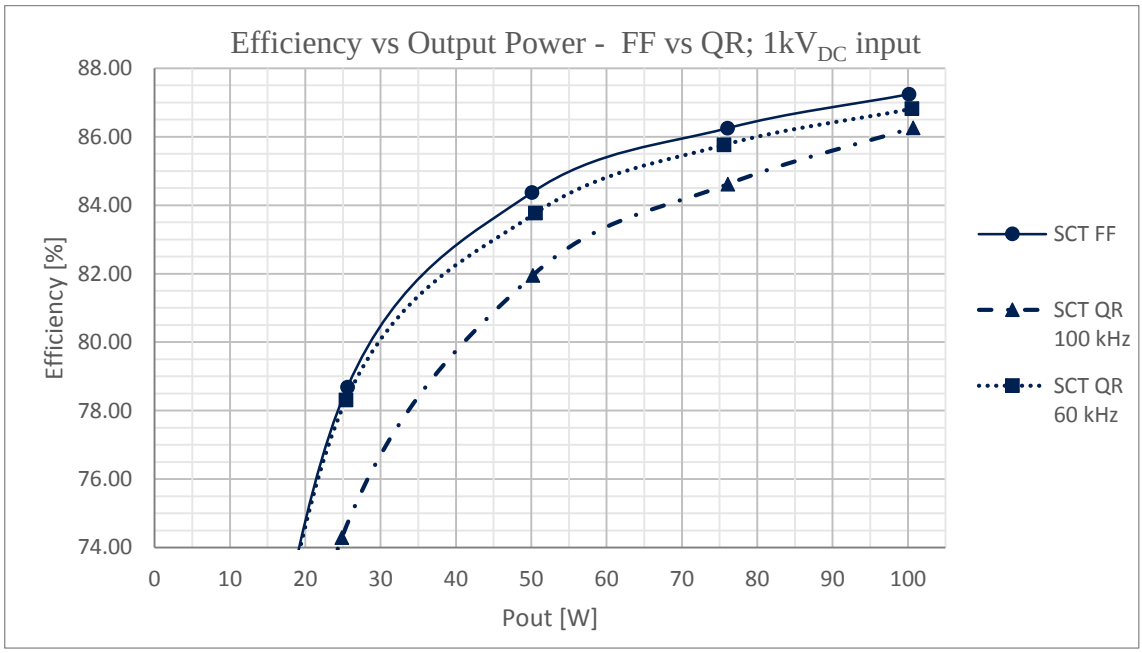



*Figure 56 Comparison of QR 100 kHz and 60 kHz with FF, 1kV$_{DC}$ input*

Switching losses for each transistor are given by point of switching and switching frequency. As amplitude of oscillation is given by reflected secondary voltage (which remains the same), for higher input voltage the effect of lower peak switching is not so advantageous as for e.g. 150 $V_{DC}$, for which the switching losses could have been neglected. With still significant energy of parasitic capacitances for lower oscillation peak, switching losses are mainly caused by switching frequency – demonstrated in Figure 56. Therefore, for high input voltages efficiencies are ordered by switching frequency, if FF's point of switching was near the upper peak, it caused just efficiency drop, not swapping the order. Unfortunately for QR, this happens only for 10W load. This is not shown for purpose of better clarity; the values are FF: 64.3%, QR 60 kHz: 64.0%, QR 100 kHz: 58.6%. The effect is also so marginal because oscillations are more damped with more periods skipped – even for full load, QR 60 kHz switches during the fifth lower peak as illustrated in Figure 57.

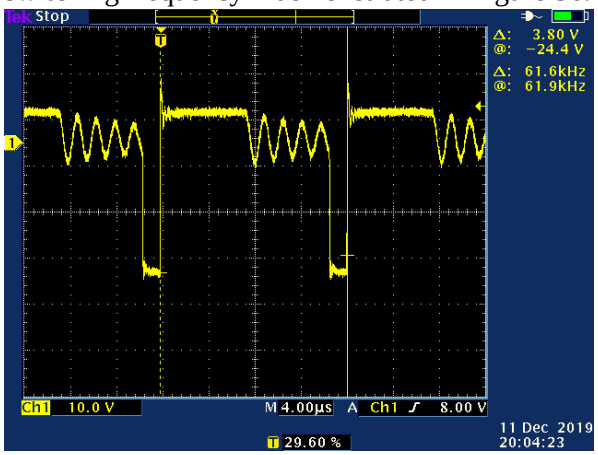



*Figure 57 Switching of SCT for QR 60 kHz, full load and 1kV$_{DC}$ input*

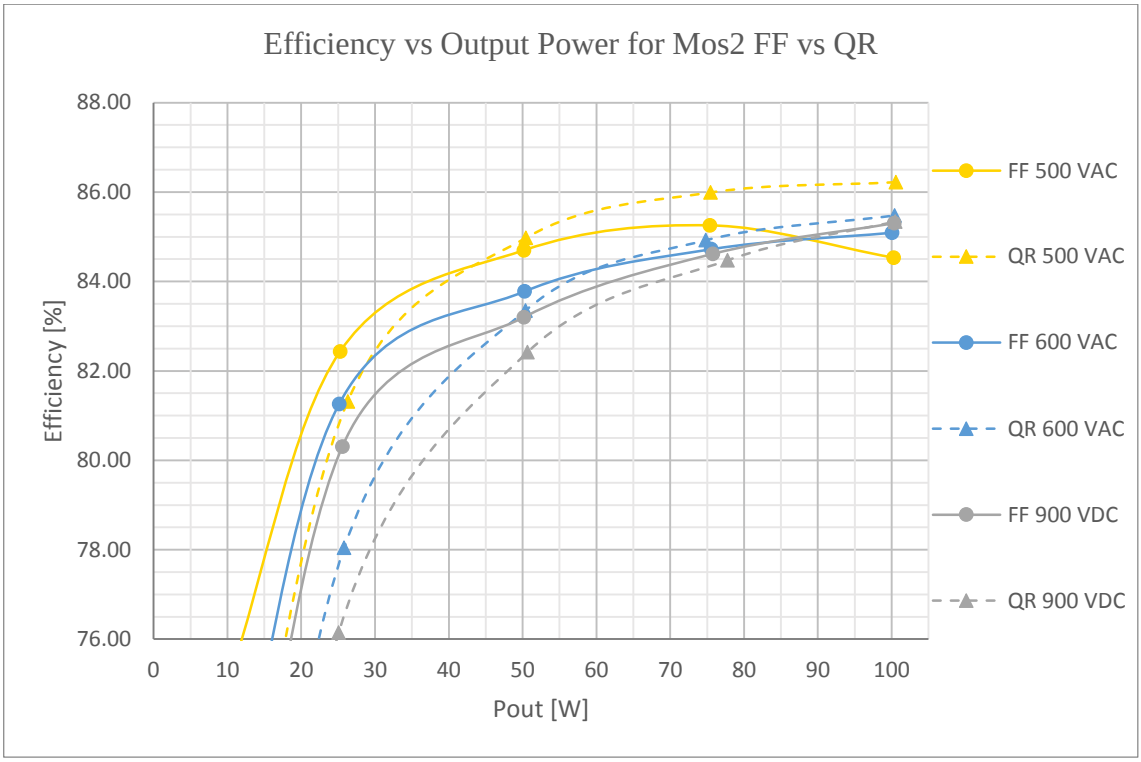



*Figure 58 Effect of QR on Mos2*

Last mention about QR focuses on Mos2: as this transistor was underrated for this application due to its high on-state resistance, QR highly improved resistive losses. Unfortunately, as resistive losses are significant for lower voltages (for which Mos2 is not applicable), the effect is obvious only for $500V_{AC}$ input. With low output capacitance compared to other Si transistors higher switching losses were overtaken by improvement of resistive losses. In lesser extent this effect remains for $600V_{AC}$ input; full-load efficiency is also slightly better for $900V_{DC}$. As switching losses increase, for 1kV input it's the same result as described before for others.

## 4.5 Thermal measurements

As efficiency and point of switching were measured together, temperature of MOSFETs package was also measured. Temperature was measured only for rough comparison and no special adjustments for valid operation were made (for instance measurement in climate chamber). As it can be seen from dates on oscilloscope screenshots, measurements were made during long period. All measurements were made under safety cover with vents, thus with at least similar measurement conditions. Ambient temperature under the cover was measured only once with Fluke 189 multimeter using standard K-type thermocouple as 23.8°C. As this was done in air-conditioned laboratory it shouldn't differ so much. Results presented here are not informative about the exact value as they might be affected by external conditions, but the trend should have been preserved.

Board v1 uses SK 104 from Fischer Elektronik shortened to 30 mm as its MOSFET heatsink (H1 in schematic). As this was customized, thermal resistance is not defined, but it's in range between 11 °C/W and 14 °C/W as those are the values for length 38.1 mm, respective 25.4 mm. Nevertheless, these are values of thermal resistance for free air cooling but on PCB other components worsen it. Figure 59 shows the situation: heatsink in the middle is right between the transformer and capacitor bank. As capacitors only decrease air convection, transformer heats its ambient due to winding and core losses. In front of heatsink there is the triplet of transils, their power dissipation in percent is approximately equal to leakage-to-primary inductance ratio (also in percent). Leakage inductance was measured as 7,84 µH, i.e. 1.34%; hence for full load transils power dissipation is approx. 1.52 W for efficiency 88%. They probably cause huge air temperature rise on this side of heatsink. From back side of the heatsink Gate-Drive module for SCT is connected or the place is left open for others. GD module only worsens the air convection as its power consumption is low. In Figure 59 there is also strange temperature drop on the heatsink top side: as its height was reduced, this area is not black anodized as the rest and under certain angle its emissivity decreases. It is not a temperature drop but just misinterpretation considering constant emissivity.


*Figure 59 Thermal measurements on board v1 with thermographic camera; Mos1 690$V_{AC}$ input, full load*

As board and components used for measurements were the same, negative thermal effects on heatsink were very similar for all transistors. Therefore, transistor junction temperature should depend only on its losses and thermal resistance. Considering the same thermal resistance of isolation pad, the only different parameter is junction to case, as this is mostly given by chip area:

| | Thermal resistance [°C/W] | | | | |
|---|---|---|---|---|---|
| | Mos1 | Mos2 | SCT | Mos3 | Mos4 |
| $R_{thj\text{-}case}$ | 0.5 | 0.78 | 1.46 | 0.5 | 0.28 |
| $R_{thj\text{-}amb}$ | 50 | 50 | 50 | 50 | 50 |

*Table 10 Thermal resistance of used MOSFETs; source: [16][17][14][13][15]*

### 4.5.1 Junction temperature

Thermal resistance junction to ambient ($R_{thj-amb}$) is the same for all MOSFETs and it is overwhelmingly higher than junction to case ($R_{thj-case}$). $R_{thj-case}$ defines thermal resistance to packages thermal pad, but $R_{thj-amb}$ includes all paths, not only thermal pad. Because of the huge difference in their values, following estimation is possible: most of thermal energy is carried away from junction via thermal pad. As chip area of used transistors is most probably smaller than area of thermal pad by two orders or maybe more, in junction to ambient thermal resistance most of energy is transferred from the chip to the rest of package also via thermal pad. As air temperature in front of the MOSFET is already heated by heatsink and transils, package temperature should be approximately the thermal pad temperature because only small amount of heat is transferred by package surface. I admit that this is rough and inappropriate estimation for precise measurement, but in this case it should be sufficient and maybe not so inaccurate.

Temperature of the package was measured in the point marked 1 in Figure 59. This is more or less location of the chip, so it was used as reference. Unfortunately, thermographic camera wasn't available for all measurement, so instead of it thermocouple was used. Despite to the best efforts (i.e. connecting it directly to the package and isolating it from the ambient) measured data was later found incorrect. The meaning of this measurement is its connection with efficiency and point of switching. Because of their lower priority measurements were not repeated once more with thermographic camera and are marked as X in the following table:

| | **Package temperature [°C] for full load** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **Fixed-Frequency** | | | | | **Quasi-Resonant** | | | | |
| **Input** | Mos1 | Mos2 | **SCT** | Mos3 | Mos4 | Mos1 | Mos2 | **SCT** | Mos3 | Mos4 |
| 150 VDC | 126.8 | N/A | 70.0 | X | X | 106.5 | N/A | 54.9 | 105.9 | 70.3 |
| 180 VAC | 118.2 | N/A | 60.0 | X | X | X | N/A | 49.1 | 75.9 | 66.4 |
| 230 VAC | 99.0 | N/A | 57.0 | 80.2 | 78.1 | 69.5 | N/A | 50.4 | 72.6 | 71.5 |
| 400 VAC | 82.3 | N/A | 62.0 | X | X | 75.0 | N/A | 56.2 | 79.1 | 82.8 |
| 500 VAC | 83.9 | 130.0 | 72.0 | X | X | 88.9 | 106.0 | 65.2 | X | 94.3 |
| 600 VAC | 100.0 | 122.0 | 73.0 | X | X | 95.7 | 114.7 | 74.3 | X | 113.3 |
| 690 VAC | 105.5 | 120.0 | 82.0 | N/A | N/A | 102.3 | 118.2 | 87.4 | N/A | N/A |
| 900 VDC | 103.2 | 122.0 | 76.0 | 99.5 | 98.6 | 99.0 | 106.9 | 82.8 | 115.0 | 122.6 |
| 1 kVDC | 105.5 | 120.0 | 86.0 | N/A | N/A | 110.6 | 119.6 | 95.2 | N/A | N/A |

*Table 11 Measured package temperatures*

| | **Estimated junction temp. [°C]** | | | | | **Temperature drop on $R_{thj-case}$ [°C]** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Input | Mos1 | Mos2 | **SCT** | Mos3 | Mos4 | Mos1 | Mos2 | **SCT** | Mos3 | Mos4 |
| 150 VDC | 129.8 | N/A | 72.4 | X | X | 3.0 | N/A | 2.4 | X | X |
| 180 VAC | 120.1 | N/A | 61.7 | X | X | 1.9 | N/A | 1.7 | X | X |
| 230 VAC | 100.6 | N/A | 58.5 | 81.4 | 78.5 | 1.6 | N/A | 1.5 | 1.2 | 0.4 |
| 400 VAC | 83.6 | N/A | 63.8 | X | X | 1.3 | N/A | 1.8 | X | X |
| 500 VAC | 85.3 | 133.9 | 74.4 | X | X | 1.4 | 3.9 | 2.4 | X | X |
| 600 VAC | 101.6 | 126.0 | 76.1 | X | X | 1.6 | 4.0 | 3.1 | X | X |
| 900 VDC | 104.9 | 126.0 | 79.5 | 101.2 | 99.6 | 1.7 | 4.0 | 3.5 | 1.7 | 1.0 |
| 1 kVDC | 107.5 | 124.2 | 90.1 | N/A | N/A | 2.0 | 4.2 | 4.1 | N/A | N/A |

*Table 12 Estimated junction temperatures*

From measured temperature, thermal resistance $R_{thj-case}$ and estimated losses for FF junction temperatures in Table 12 were calculated.

Junction temperatures correspond with estimated losses and measured efficiency. Package temperature was almost always measured for steady state or at least slowly changing state. This is the case of Mos1 for input voltages 150 $V_{DC}$ and 180 $V_{AC}$ – for both it was found thermally unstable. After reaching junction temperature approx. 130°C, thermal function of on-state resistance acts like positive thermal feedback: as it grows with temperature, additional resistive losses start heating acceleration.

Focus on thermal parameters revealed one disadvantage of SCT: as its $R_{thj\text{-}case}$ is almost two times higher than for underrated Mos2 (and even higher for any other), despite the lowest dissipated power temperature drop on $R_{thj\text{-}case}$ is quite high. As parameters of used transistors were compared in 3.3 – Table 2, total power dissipation AMR ($P_{TOT}$) wasn't listed (as this isn't very important for this application – switching on this frequency and so the transients are more limited by safe operating area and thermal impedance). Based on previous comparison of parameters SCT can be classified as slightly better or around middle, but according to $P_{TOT}$ it is the weakest. With $P_{TOT}$ = 120 W (all are for $T_{case}$ = 25°C) it is only at ¾ of Mos2 160 W, less than half of Mos1 & Mos3 250 W or deeply below Mos4 446 W. As SiC allows minimizing chip area with similar parameters as for Si devices (discussed in 1.1.1), this is the negative effect – maximum voltage or current same as on-state resistance were comparable, but $P_{TOT}$ not: maybe because of different technology, or maybe because of thermal resistance given by chip area.

### 4.5.2 Other thermal measurements

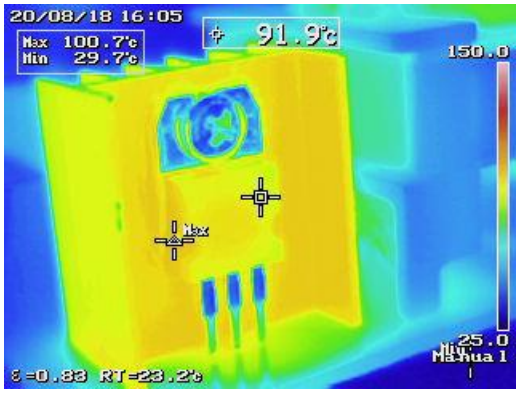



*Figure 61 Output diode temperature, full load*

Besides MOSFETs, whole board was monitored with thermographic camera. Further comments are meaningful only to two parts: output diode and capacitor bank. As output diode affects efficiency, its thermal pad temperature was measured as 100.7°C. Output diode losses for full load were estimated according to following equation:

$$P = 0.65 \cdot I_{F-AV} + 0.016 \cdot I_{F-RMS}^2 \quad (25)$$ [18]

as 4.04 W. Using the same approach, junction temperature was estimated to be 108°C. According to this and datasheet [18] average forward drop was determined as 0.8V for full load. Opposed to output diode, capacitor bank shouldn't affect efficiency, but heat from MOSFET can negatively affect its lifetime and/or time stability. As heatsink is placed right next to capacitor C6, there is considerable heat transfer – illustrated in Figure 60. Capacitor temperature is approx. 60°C, which is much more than others – for not affected capacitors it is around ambient temperature. Nevertheless, as this is just evaluation board and used capacitors have rated load life of 10000 hours at 105°C / 400 V, I pronounce the design as still adequate for given purpose.


*Figure 60 Capacitor bank temperature*

# 5 Conclusion & Summary

Starting with converter, it was designed properly and board v2 can be used as evaluation board. Every used component meets voltage requirements, starting with semiconductors, through passive components and ending with input terminals and fuse holders. As compliance with EMC standards is important for any final design, special consideration was given to this problematic. PCB was routed with consideration to creepage and clearance according to reinforced isolation between primary and secondary side. Not so many words were written about feedback – this uses standard voltage reference TL431 and was optimized on prototype for best stability. As optocoupler is low-cost PC817 with wide range of transfer current ratio (abbr. CTR, depends on manufacturer, typ. 50-600%), intention was stability independent on CTR. This was achieved with excellent output voltage regulation – maximum swing of 14.8 mV, demonstrated in Figure 62.

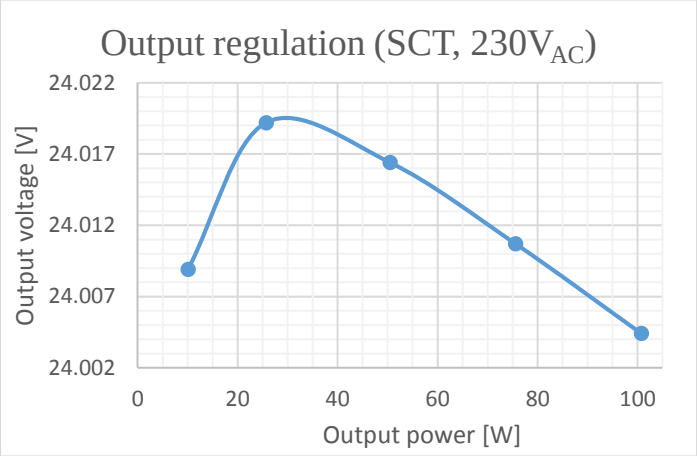



*Figure 62 Output regulation*

The main goal of comparing Si vs SiC MOSTETs was efficiency, as this is often important parameter for every converter. Losses were estimated for each point of measurement using three parameters: on-state Drain-Source resistance and output capacitance energy of the transistors and parasitic capacitance of the PCB and the transformer. Because efficiency can be affected by several unpredictable effects, estimation was chosen instead of simulation. Nevertheless, as the estimation was based on simulated or precisely calculated parameters, the results were in my opinion very good: for full load only 5 of 34 estimations were wrong, which means precision over 85%. Excluding the 0.03% difference in measurements the number drops to 4 of 34 and these four cases were later revealed as quite specific: as the smallest difference in losses was predicted (0.59W) and small difference was also measured (0.21%), any additional effect may change it. In this case it was most probably caused by Gate charge and operation in saturation region during switch-off.

Not only efficiency was taken into consideration, also switching behavior was closely observed. Intention of measurement and simulations was determination of switching losses, consisting of energy stored in output capacitance and operation in saturation region during switch-off transient. The second mentioned was most probably found significant for Mos4 and it might be the reason for its efficiency being lower than expected. SCT proved that in general SiC transistors are faster than Si: its switch-off transient was fastest with lowest energy dissipated in saturation region. This was achieved besides obvious limitation of used equipment: I firmly believe it was even better than measured.

From efficiency measurements SiC transistor SCT came as winner: this was partially predicted with losses estimation, but was sometimes overtaken by Si-based transistors. This happened mostly for low load, but two times for half load and once even for 75W load. Industrial power supplies are quite specific because of their necessary input voltage range, in this case from 150 $V_{DC}$ to 1 $kV_{DC}$. It was proven that for lower input voltage mainly low on-state resistance is

important, but for higher input output capacitance matters more. Good efficiency results just exposed another advantages of used SiC MOSFET: combination of low $R_{DS-on}$ and output capacitance makes it perfect for this application. Not only the value of on-state resistance, but most importantly its thermal characteristic: the growth with temperature was 25% for 100°C difference opposed to over 200% increase for Si transistors. Therefore, if resistive losses caused significant warming, they remained similar. In case of others the growth of $R_{DS-on}$ doubled them, for two inputs leading in thermal instability (Mos1). With the maximum junction temperature 50°C better than Si transistors SiC is the best choice for used purpose.

Using SiC MOSFET in this application was possible only because of Gate-Drive module. Designed for robustness necessary in industrial sector it should cover any danger that threatens the SiC. Effort was also given to lowering power consumption which is indeed marginal for higher loads. It is difficult to calculate it as the consumption is current-type and VCC voltage can variate. Most probably it is in range of 100-200 mW for most cases. Unfortunately, this results in efficiency drop noticeable especially for 10W load. GD transformer was also observed very closely during design, because it includes recuperation feature. This was a challenge to optimize and thanks to it power consumption was not so high for longer on-time.

Converter was designed for fixed-frequency operation. The switching frequency was chosen as 51.3 kHz, which is optimal: intention was to lower it as possible for minimal switching losses, but another lowering wouldn't be possible with ETD34 core or with such a low leakage inductance. Because of DCM, there was no need of slope compensation and also switch-on losses could be neglected. Besides fixed-frequency, quasi-resonant mode of operation was also tested. QR is in general presented as beneficial because (in case of proper point of switching feature; like L6566BH) it lowers switching losses and for lower load also the resistive ones. This was validated as true statement for lower input voltages, especially for Si transistors. Unfortunately, and as expected, for higher input voltages the effect was opposite. Because switching frequency is proportional to input voltage, this caused enormous switching losses. Limiting the frequency closely to 51.3 kHz improved the efficiency, but it was still worse than for fixed-frequency. Overall effect of QR was in my opinion slightly more negative than positive. Because it is easy to switch the L6566BH from FF to QR (and vice versa) and the same components can be used for both FF and QR, it would be interesting to implement simple FF/QR switch for the final product: the mode would be selected according to expected input voltage and any deviation of it may in the worst case just cause worse efficiency.

Thermal measurements revealed expected results, but also pointed out potential design flaw for final design: the heat effect on capacitor bank. Thanks to further calculation with thermal results, maximum total power dissipation and thermal resistance junction-to-case were found interestingly worse for used SiC transistor. These wouldn't make any difference in this application but might be important in the one with higher dissipated power. And this is the final conclusion of Application of SiC MOSFETs in Industrial Power Supplies: besides this potential disadvantage they are today quite common in high-power applications, but not so much in applications similar to the one presented in this thesis. As overall results were overwhelmingly better for SiC than for Si transistors, it sounds unreasonable. The reason might be the driving. It is my firm belief that used Gate-Drive module is perfect for this application, but causes worse efficiency for light load. If parameters like exact $V_{GS}$ value or covering any possible malfunction wouldn't be required, it could be designed as for instance charge pump with much lower power consumption and revealed the benefits of SiC even for lower loads.

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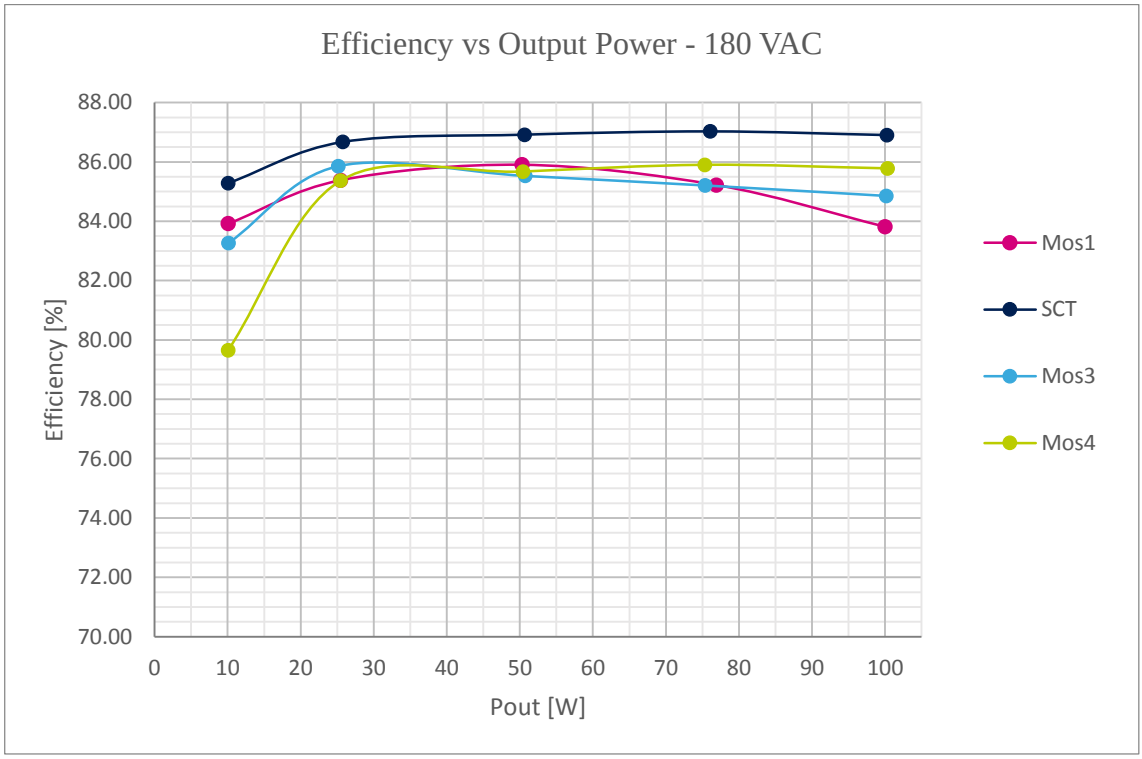
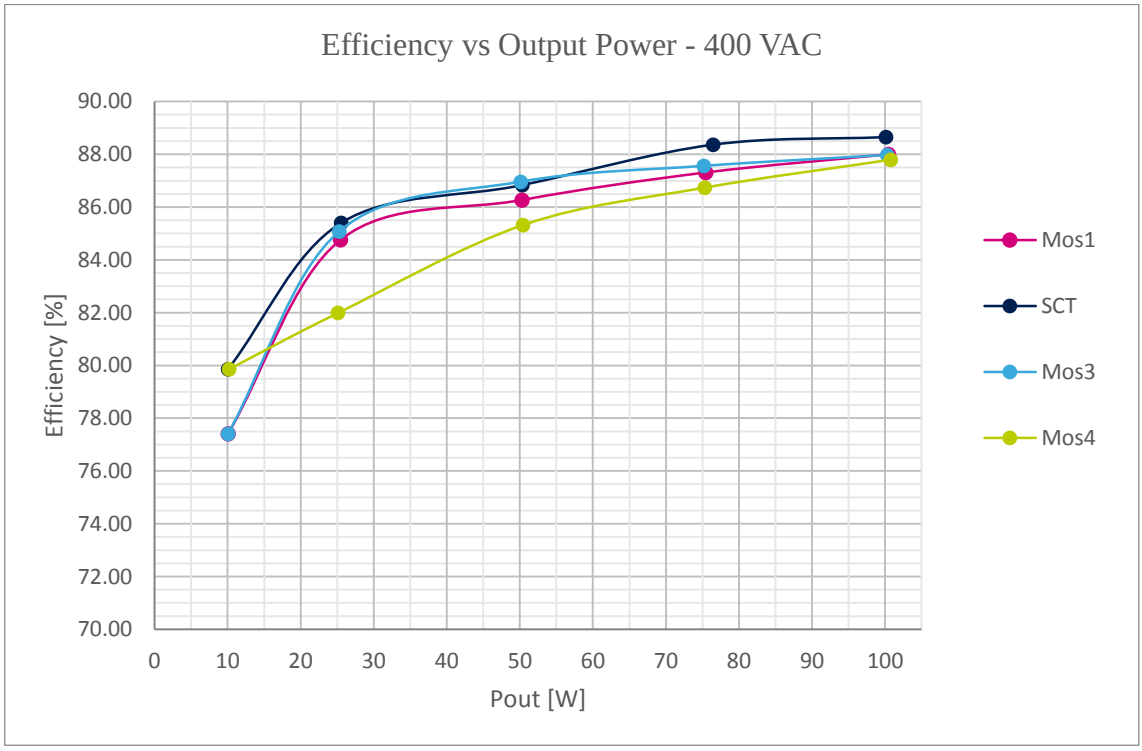
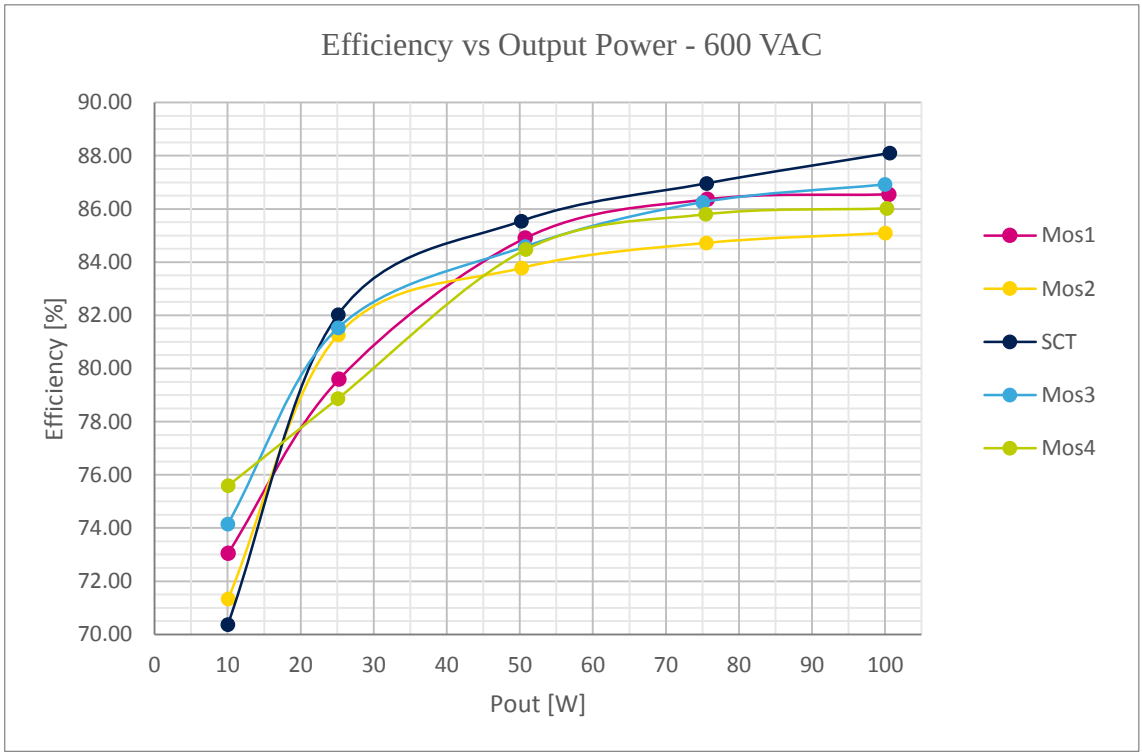
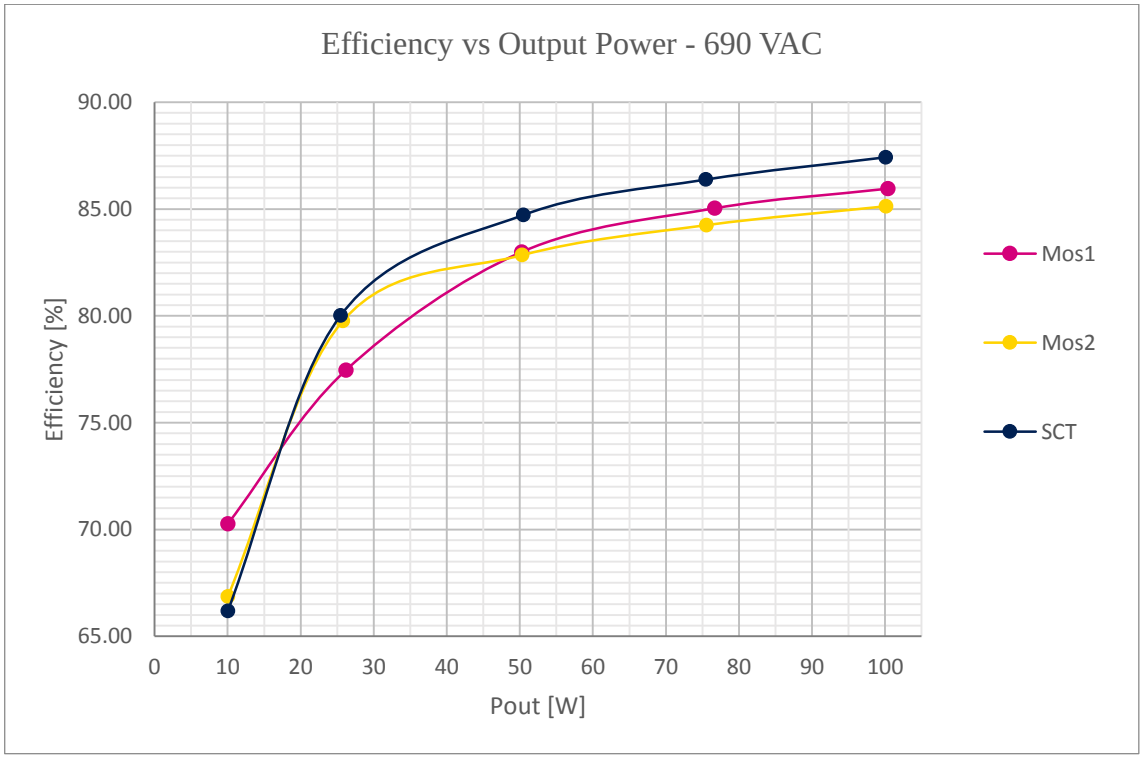
# Appendix A – The rest of efficiency measurements




Efficiency vs Output Power - 600 VAC
90.00
88.00
86.00
84.00
82.00
80.00
78.00
76.00
74.00
72.00
70.00
Efficiency [%]
0
10
20
30
40
50
60
70
80
90
100
Pout [W]
Mos1
Mos2
SCT
Mos3
Mos4


Efficiency vs Output Power - 690 VAC
90.00
85.00
80.00
75.00
70.00
65.00
Efficiency [%]
0
10
20
30
40
50
60
70
80
90
100
Pout [W]
Mos1
Mos2
SCT

# Appendix B – Digital content

In folder \Attachments or archive Attachments.zip are following files and directories:

Losses.xlsx – Excel sheet with losses estimation

Efficiency.xlsx – measured efficiency data

\Spice – contains SPICE models of simulated transistors

\Boards

\v1 – contains schematic, GERBER data and BOM for board v1

\v2 – contains schematic, GERBER data and BOM for board v2