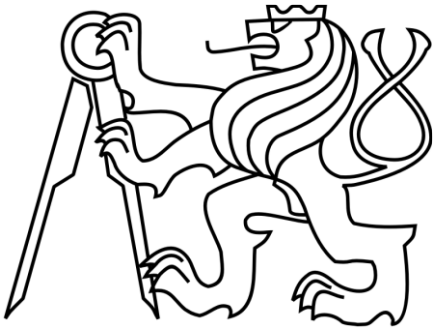
Czech Technical University in Prague

Faculty of Electrical Engineering

Department of Microelectronics



Master's thesis

Design of an RC Oscillator for Automotive Applications

Author: Bogdan Miasoiedov

Supervisor: prof. Ing. Miroslav Husák, CSc.

2019

ZADÁNÍ DIPLOMOVÉ PRÁCE

I. OSOBNÍ A STUDIJNÍ ÚDAJE

Příjmení: **Miasoiedov** Jméno: **Bogdan** Osobní číslo: **439644**

Fakulta/ústav: **Fakulta elektrotechnická**

Zadávající katedra/ústav: **Katedra mikroelektroniky**

Studijní program: **Elektronika a komunikace**

Studijní obor: **Elektronika**

II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

Návrh RC oscilátoru pro automobilové aplikace

Název diplomové práce anglicky:

Design of an RC Oscillator for Automotive Applications

Pokyny pro vypracování:

1. Proveďte rozbor stávajícího stavu řešení obvodů RC oscilátorů pro automobilové senzorové aplikace, v přehledu se zaměřte na výhody a nevýhody, pro další řešení vyberte vhodnou architekturu obvodu.
2. Navrhněte obvod RC oscilátoru v technologii I4TE společnosti ON Semiconductor. Pro návrh využijte standardní postupy, tj. analýzu, simulace a eventuálně návrh layoutu. Základní požadované parametry pro návrh obvodu jsou: stabilita frekvence +/- 2 % v celém teplotním rozsahu od -40 oC do 175 oC, malá proudová spotřeba, dobrá fázová stabilita, možnost přesného nastavení frekvence oscilací, aby bylo možné kompenzovat vliv výrobního rozptylu parametrů součástek. Návrh a simulace proveďte v prostředí Cadence s použitím Spectre simulátoru.
3. Vyhodnoťte dosažené parametry navrženého obvodu a shrňte základní poznatky dosažené při návrhu.

Seznam doporučené literatury:

1. Neumann, P., Uhlíř, J.: Elektronické obvody a funkční bloky (I, II), ČVUT 2001
2. MARTIN K. JOHNS A.D: "Analog Integrated Circuit Design", New York Wiley-& Sons Inc. 1997.
3. LAKER K., SANSEN W.: "Design of Analog Integrated Circuits and Systems", New York, McGraw Hill 1994.
4. GREGORIAN R., THEMES G. : "Analog MOS Integrated Circuits For Signal Processing ", New York Wiley-Interscience 1984.

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Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) diplomové práce:

Datum zadání diplomové práce: **28.01.2019** Termín odevzdání diplomové práce: _____

Platnost zadání diplomové práce: **20.09.2020**

prof. Ing. Miroslav Husák, CSc. podpis vedoucí(ho) práce	podpis vedoucí(ho) ústavu/katedry	prof. Ing. Pavel Ripka, CSc. podpis děkana(ky)

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23.05.2019
Datum převzetí zadání

Podpis studenta

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Declaration

I declare that I have elaborated the presented thesis independently and that I have provided all the used information sources in accordance with the Methodological Guidance on Compliance with Ethical Principles in the Preparation of University Final Thesis.

Date: ……. ……

Bogdan Miasoiedov

Abstract

The thesis is aimed on the integrated relaxation oscillator design for automotive applications, that are characterized by harsh operation conditions and high robustness requirements.

Literature research was conducted to acquire necessary theoretical basis for comparative study of the recently proposed integrated oscillator designs to choose the oscillator architecture utilizing integrated-error feedback for the implementation.

High-level model simulations were conducted to predict negative influences on the system performance and to suggest blocks optimal parameters for the design.

The implementation of the designed blocks was discussed, and simulation results of the critical parameters were presented.

The designed oscillator simulations proved the consistency of the integrated-error feedback concept for practical realization. However, the designed system needs further improvements.

Key words: automotive electronics, relaxation oscillator, IEF

Abstrakt

Tato práce je zaměřena na návrh integrovaného relaxačního oscilátoru pro automobilové aplikace, které jsou charakteristické extrémními provozními podmínkami a vysokými požadavky na robustnost.

Z dostupné literatury byla provedena rešerše, která umožnila postihnout nezbytný teoretický základ pro komparativní studii nedávno představených designů integrovaných oscilátorů a také pomohla navrhnout architekturu oscilátoru, která v implementaci zahrnuje princip IEF.

Za účelem předpovězení negativních vlivů na výkon systému a optimálních parametrů bloků byly provedeny simulace vysokoúrovňového modelu.

V práci je diskutována implementace jednotlivých bloků a prezentovány výsledky simulace kritických parametrů.

Simulace navrženého oscilátoru prokázaly konzistenci konceptu IEF pro praktickou realizaci. Realizovaný systém však potřebuje další vylepšení.

Klíčová slova: automobilová elektronika, relaxační oscilátor, IEF

Contents

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List of acronyms

ADC	Analog-to-digital converter
BER	Bit error rate
ISO	International Organization for Standardization
EMC	Electromagnetic compatibility
IC	Integrated circuit
CMOS	Complementary metal-oxide-semiconductor
MIMC	Metal-insulator-metal capacitor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
LPF	Low-pass filter
VCO	Voltage-controlled oscillator
FOM	Figure of merit
DT	Dynamic threshold
ST	Switched resistor
TC	Temperature coefficient
IEF	Integrated-error feedback
Op-amp	Operational amplifier
HLM	High-level modeling (or “high-level model”)
DC	Direct current

1 Introduction

The share of electronics in the price of a modern automobile has gained almost 15% over the last two decades, and it is expected that the growth will continue and even enhance its rate [1]. It is a good indication of an increase in the amount and complexity of electronic systems in cars.

Therefore, the sensor systems, being a significant part of the modern automotive electronics, expand and are utilized in an increasing number of applications. These systems actively exploit digital signal processing employing ADC units. ADCs require accurate clock signals, since the deviations of the clock frequency cause the rise in bit error rate (BER) of the converters. Taking into account that many of the automotive sensor applications are directly or indirectly related to safety (ISO 26262), design of the precise clock generator is of great importance, what can be a challenging task, because automotive electronic systems are exposed to extreme environmental conditions (e.g. wide temperature range, big variations of the power supply voltage etc.).

Requirements for speeds of operation, electromagnetic compatibility (EMC), low power dissipation, small dimensions have made integrated circuits (ICs) a dominant solution in automotive electronics. Therefore, clock generators gained an additional limitation concerning their architecture, they have to be integrated and occupy little area on the chip to withstand adequate production costs.

This thesis is aimed at designing the integrated clock generator (oscillator) in I4TE technology from the company ON Semiconductor through discussion of the problematics, conduction of the literature research and realization of the chosen architecture by means of the Cadence software.

1.1 Oscillators in general

Oscillator is a system that generates a periodic signal out of a constant one, which is mostly provided, in case of integrated electronics, by a reference voltage or current source. A timing reference is required to be present in the system, since time can be “measured” only through the quantity that varies in time.

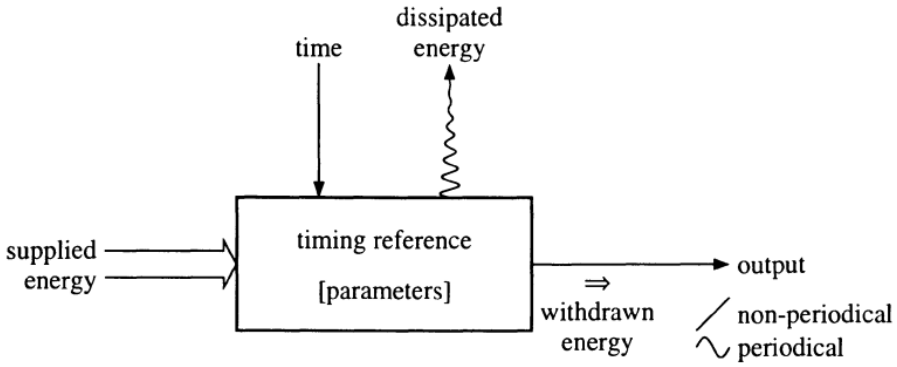

Figure 1.1 Block diagram representing an oscillator in general. The image is taken from [2].

Figure 1.1 illustrates a general view [2] on any oscillatory system. In this figure, the energy is supplied to start the system and maintain its operation, since there are no components in electronics that do not dissipate energy. It can also be seen that time modulates the system and, at the output of the system, the influence of time can be measured in the form of either a periodical or a non-periodical time-variant signal. So, it is an indirect time sensor that can be used as a timing reference. Also, we can

understand that transfer of the timing information to the output is dependent upon two things: the parameters of the timing reference, and the energy supplied to it.

There are two major groups of the timing references: linear and non-linear systems. The non-linear timing references are poorly studied and are difficult to model. Moreover, linear systems are supposed to have better performance over the non-linear ones [3].

It is known that a linear system can be modeled by means of the corresponding pole-zero plot, what is the most convenient way for the timing references modeling as well. These systems can have different orders (mostly first or second, rarely third order, in practical oscillatory systems), based on the number of poles representing them. The pole-pattern can also say about the system functioning principle and features, e.g. whether the transfer of timing information to the output of the timing reference is only determined by the parameters of the timing reference, or also by the supplied energy.

It turns out that the most appropriate solution is the first-order timing reference, for the design of the integrated oscillator used as a clock generator for ADCs. The reason is that cost-effective CMOS technology used in commercial production excludes a series of common components in second-order systems. For example, crystal resonators, having the best noise performance; integrated inductors; and the electromechanical resonators. Moreover, there are possibilities to build the second-order integrated oscillator using available in CMOS passive components and blocks, such as transconductors, resistors and capacitors, but the process variation of the integrated components parameters and harsh ambient conditions in automotive applications complicate the tunability and degrade the performance of such a system. Similar notions can be applied to exclude ring oscillators from the consideration. Therefore, the objective of this thesis is a study of theory, popular topologies of the first-order oscillator and consecutive application of this knowledge to implement the system with parameters stated in the task, Section 1.2.

1.2 Design goals

The design goals extracted from the thesis task are listed below:

- frequency stability ±2 % in whole temperature range from -40 ^{o}C to 175 ^{o}C;
- small current consumption;
- good phase stability (small jitter);
- opportunity for precise frequency setting to compensate production process deviations of components parameters (trimming).

Additional features include that the power supply voltage is not stable, varying in the range of 2.7-3.6 V, and the designed block can utilize available on the chip stable band-gap voltage source, supplying 1.21 V with 3% tolerance to the nominal value.

1.3 Structure of the thesis

Section 2 introduces theory that is used throughout the thesis.

In Section 3, popular realizations of the integrated relaxation oscillator are review, and the most appropriate topology is chosen and modeled in Section 4. The implementation is discussed in Sections 5 and 6.

The information sources are referenced by numbers in square brackets, and the equations are referenced by numbers in round brackets.

Numbering of figures in the thesis employs two numbers separated by dot: the first one corresponds to the number of a first-level section, the second one corresponds to the number of the figure in this first-level section. The figures section number in Appendices is “0”. The same approach is applied for tables. Equations, however, are numbered successively over the whole thesis.

2 Theoretical prerequisites

Implementation of any system requires understanding of operation principles of this system, as well as good knowledge of the available tools, components, their properties etc. This section contains the first-order oscillator description using high-level models. These models allow to understand the properties of different architectures of the considered oscillator system (such as noise performance, tunability etc.), compare them and choose the most appropriate topology for the implementation.

2.1 First-order oscillator model

First-order oscillator (or relaxation oscillator) employs a system that contains only one pole, which is the timing reference of the oscillator (Section 1.1). Since the single pole can only be somewhere on the real axis, three situations can be distinguished: the timing pole is either in the left or the right half plane, or it is exactly situated at the origin, Figure 2.1. The bottom part of Figure 2.1 depicts transient responses of these three pole patterns. Any of them can create timing information (time-variant signal) from a constant and so form the first-order oscillator core. The one pole timing reference transfers timing information to the output signal amplitude. [2], [4]

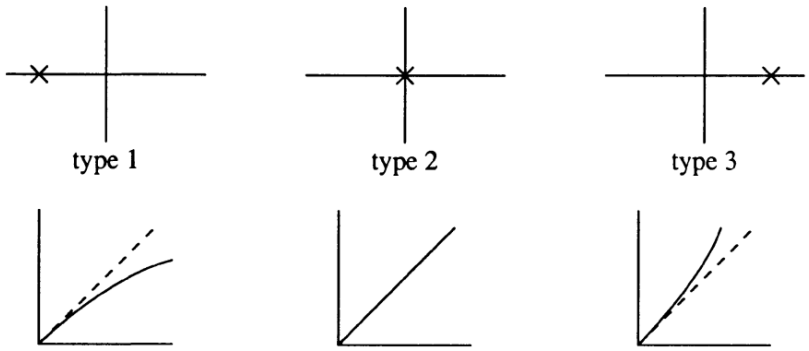

Figure 2.1 Three types of the first-order systems. Their pole-patterns on top and corresponding impulse responses on bottom. The image is taken from [2].

The transfer function from time to a measurable signal (e.g. t → V, t → A or t → Q) is determined by the surrounding electronics. The ideal relation between time and the output signal is linear, which is the type 2 system in Figure 2.1, [2]. In this case the relation between the time and the signal level is given by (1):

$$E_o(t) = \int_0^t \alpha \, d\tau \qquad (1)$$

In (1) α is the integration constant and it determines the rate of change of the output signal (angle α in the right part of Figure 2.2), which is directly proportional to time. Due to this relation, first-order systems are called integrators and basically oscillators of the first class are based on it.

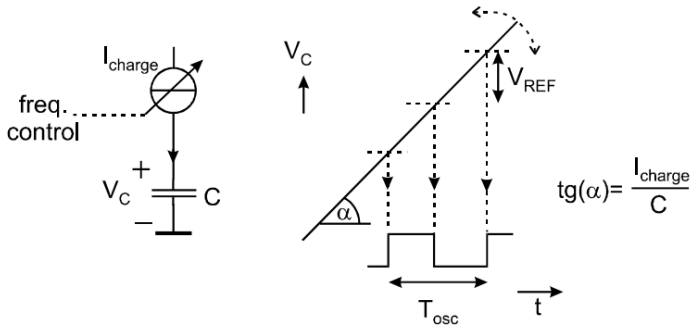

Figure 2.2 Principle of equidistant level discrimination in the first-order oscillator. The image is taken from [5].

However, a sole integrator cannot form a complete system, it only generates the time-variant signal. This signal is not periodic, and it requires additional non-linear time-invariant system to handle it and turn into oscillations. The idea is depicted in Figure 2.2. The non-linear system has to discriminate equidistant levels of the output signal corresponding to the reference voltage, what is usually done by a comparator. The system also has to have a memory block to store the previous "level" from the integrator for adding to the reference offset (V_{REF} in Figure 2.2 and E_{off} in the left side of Figure 2.3). Figure 2.3 (the left side) depicts the principle (here comparator generates periodic pulses that trigger memory to store new integrator levels, the right side of Figure 2.3). It may become obvious now that the duration of the oscillation period (hence the frequency) can be controlled by the integration constant α and reference offset E_{off}, (2).

$$T = \frac{E_{off}}{\alpha} \tag{2}$$

Nevertheless, the above described system is impossible in practice. Output of the real integrator is limited by the power supply. The possible solution is to change the sign of the integration constant on each interval leading to the design of the one integrator first-order oscillator. [2]

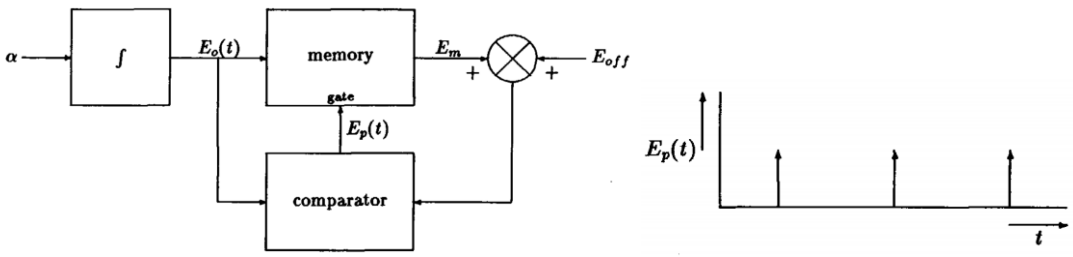

Figure 2.3 Principle of the first-order oscillator to the left; periodic pulses, generated by the comparator block to the right. The image is taken from [4].

2.1.1 One-integrator oscillator

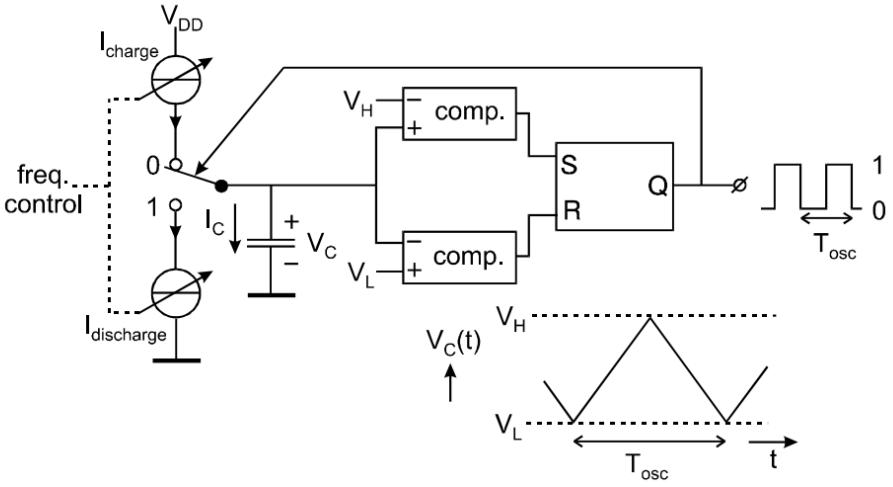

Figure 2.4 First-order regenerative oscillator with one integrator and its capacitor voltage waveforms. The image is taken from [5].

Figure 2.4 shows the principle utilized in a first-order oscillator that uses just one integrator to generate the time variant signal. The integrator is built by the capacitor and charging current source. When the current source is ideal, the integrator is a timing reference with a single pole location in the origin (Figure 2.1, Type 2). Due to limited power supply the simplest implementation of the necessary periodical discharging states is the use of a current equal to the charge current, but with opposite sign. The comparators decide when the sign of the integration constant (the current) must be inverted via the comparison of the output signal of the integrator with two threshold voltage levels V_H and V_L. The sign-inversion of the integration constant is performed by the memory, as its state directly controls the direction of the capacitor current. The memory stores the sign value (the memory is binary), since a sign-inversion of the capacitor current directly inverts the slope of the capacitor voltage causing the regeneration of the comparator. If no memory is utilized, the system will not function properly: capacitor voltage would get stuck at one of the threshold levels. The memory can be implemented by a Schmitt trigger, a flip-flop or a comparator with hysteresis. A first-order oscillator that uses a regenerative memory to store the sign-value of the integration constant is called a regenerative oscillator. [2], [4], [5]

2.1.2 Sawtooth oscillator

The regenerative sawtooth oscillator is an improvement to the basic regenerative oscillator. It allows to take the regenerative memory block out of the timing pass, to perform so-called memory bypass [6], using 2 integrators that work in orthogonal phases. This approach is not unique for memory bypass, there are other approaches too, but according to Gierkink [5], it is the easiest way.

A typical example of the sawtooth oscillator is the symmetrical two-integrator oscillator. In this topology two integrators produce a time variant signal continuously. Theoretically, one integrator can act as the sign memory for the other integrator and vice versa, so the regenerative memory can be taken out of the timing path, since it exposes the system to additional sources of the frequency error. However, it has a problem: the stabilities of amplitude and frequency will become dependent on each other, what can be overcome by precisely defining the initial state of the integrator before each cycle. For example, by resetting the integrator before each charging phase. Whenever the first integrator is being reset, its integrating action has already been taken over by the second one, so the reset-phases

do not have to be a part of the period of oscillation. So, the period of oscillation is defined by the rising slopes of the integrator outputs and the threshold level, since the second integrator can start its integration when the output of the first integrator reaches a pre-defined threshold level. [2], [4], [5]

The author of [5] presented some common topologies of the sawtooth oscillator, Figure 2.6 and Figure 2.7. The oscillator depicted in Figure 2.6 has some of the advantages described above, but it still has the regenerative memory in the timing path (no memory bypass). In this topology, the timing of the oscillation period is determined only by rising ramps of the capacitor voltages and a single threshold level V_{REF}. The falling edges of the capacitor voltages are not time-critical; the only condition is that the capacitor is discharged before the start of its next charging cycle. When the voltage across capacitor C_1 crosses the threshold level, the memory changes state and C_1 is discharged while C_2 starts charging. As well as for the basic first-order oscillator of Figure 2.5, a regenerative memory is necessary. Its function here is to store the information about which capacitor needs to be charged and which one needs to be discharged.

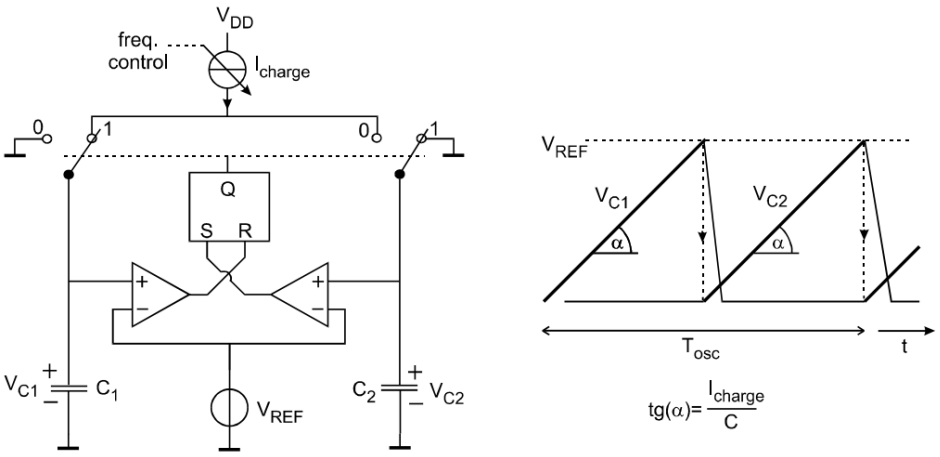

Figure 2.5 The two-integrator oscillator to the left and its capacitor voltage waveforms to the right. The image is taken from [5].

Figure 2.7 provides a modified schematic of the oscillator depicted in Figure 2.6. The comparators output toggling directly switches the integrators to charge, so the regenerative memory has been removed from the timing path. The memory here introduces a delay before a capacitor can be discharged after reaching the reference voltage V_{REF}. So, the capacitor voltages are allowed to pass the threshold level to some extent. Another function of the regenerative memory is secure storage of the new state, but due to the OR gate the action is performed parallel to the comparator. [2], [4], [5]

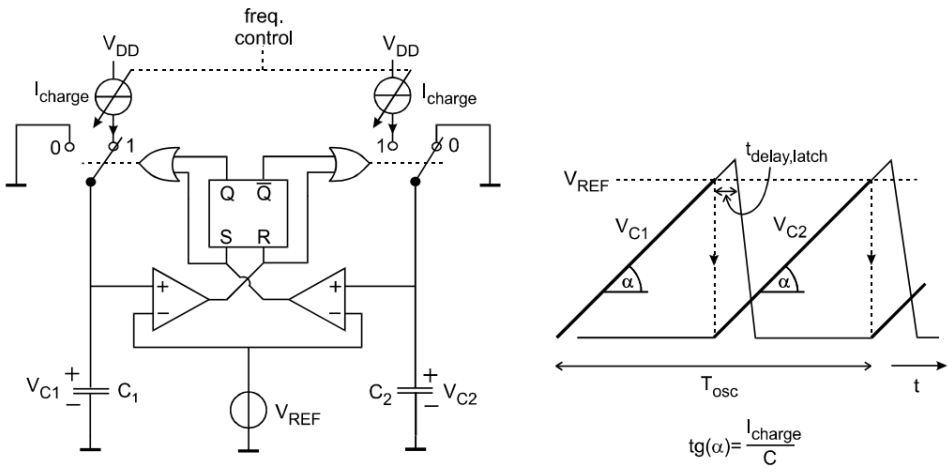

Figure 2.6 Regenerative two-integrator oscillator with memory bypass to the left and its capacitor voltage waveforms to the right. The image is taken from [5].

2.1.3 Discussion on the model

The introductory part in Section 2.1 reveals the principles of the periodical signal generation by the relaxation oscillator from the timing reference. A key role in the operation and performance belongs to the integrator being this timing reference. It is shown that the integrators can be of the 3 different types, Figure 2.1, and each of these types causes certain implications on the oscillator. Looking at Figure 2.1, comparing impulse responses of the different oscillator types, we can say that the most appropriate type for practical design is the type 2 integrator, since it implies linear relation between time and amplitude. It provides better tunability of the charging ramp, what is important for the practical design, since the slope of this ramp has linear relation to the output frequency of the oscillator, Section 2.1.1 and Section 2.1.2.

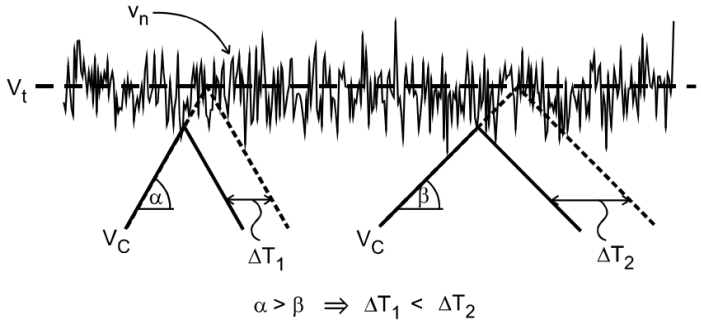

Figure 2.7 Dependence of timing error on the integration constant. The image is taken from [5].

Figure 2.7 depicts the issue of all the relaxation oscillators. The oscillation period is directly proportional to the voltage reference, whose variations due to noise directly degrades the precision of the oscillation period. Also, the figure presents a relation of the integration constant to the reference voltage noise impact: the greater the slope, the more accurate the oscillation period is with respect to the reference voltage noise.

In similar way the integration constant, defining the slope of the charging waveform, can affect the precision. Figure 2.2 depicts that the integration constant corresponds to the following relation (3).

$$tg(\alpha) = \frac{I_{charging}}{C} \quad (3)$$

Since the capacitor is a passive component, the noise of the charging current $I_{charging}$ directly causes the error.

The basic oscillator shown in Section 2.1.1 is more impacted by the issue than the topologies presented in Section 2.1.2, since it depends on the two reference levels and two slopes, Figure 2.4.

Another issue is the regeneration delay in comparators and memories, as well as degradation of the charging slope in the vicinity of the point, where the integration changes its sign. Considering the degradation of the slope, the systems from Section 2.1.2 are again more advantageous then the oscillator from Section 2.1.2, because the sawtooth oscillator discharges quicker and the degradation affects the slope during much shorter time. Moreover, the oscillator in Figure 2.6, as opposed to the system in Figure 2.5, has its "critical point" higher than the reference level, so in that respect it is even better.

However, the oscillators considered in Section 2.1.2 consist of two branches, each defining the duration of a half period. It can cause a problem, since the branches in practice will have mismatch and it will negatively affect the duty cycle.

2.2 Noise modeling of the relaxation oscillator

Noise of the oscillator is a most important issue that a designer has to deal with, when implementing any kind of oscillator system. Relaxation oscillator is no exception and it has its own specificity in this problem. One of the main differences from e.g. harmonic oscillators is that the noise measures more commonly used for relaxation ones are in time domain. Therefore, the authors (e.g. [2], [4], [5]) mostly start discussion on the issue from introduction of different measures of noise and relation between them, in order to present a tool for comparing oscillators of different kinds.

The parameter commonly used for noise characterization of the relaxation oscillator is called jitter. This measure is often defined by the normalized one-period time error (often expressed in ppm) [5], [7]:

$$jitter = \frac{\sigma_{\Delta T_{osc}}}{T_{osc}} \quad (4)$$

The problem of this definition is that it is limited to consideration of white noise, since in the case of 1/f noise [8], very important in CMOS technology, this measure becomes non-convergent and different definitions are needed. The author of [5] simplified his noise models for white noise and so the above given relation is acceptable for them. However, in [2], [4], a different approach was used, the authors considered noise in spectral domain and the above presented definition is not required in their considerations.

Appendix A presents a brief description of the 1/f noise phenomena and an overview of the technique to reduce this kind of noise, introduced in [5].

It is obvious from the principles of relaxation oscillator, that the most prominent sources of noise in these systems are fluctuations of the reference voltages for the comparator and fluctuations of the current sources, charging the capacitors and defining the integration constants. Verhoeven [2], [4] and Gierkink [5] omitted consideration of the regenerative circuit in the noise modeling or deriving relations for noise of the oscillator, because thorough analysis would then lead to complicated calculations. In [5], this simplification is called "First crossing approximation":

It suggests that the first crossing of the reference level (plus noise) by the capacitor voltage invokes an immediate and infinitely fast regeneration. It is assumed that the process of regeneration itself introduces no additional jitter. [5]

Noise models presented in [2], [4] have a number of simplifications, but still they are able to show a relation, on the high design level, between the topology of the relaxation oscillator and the spectral noise shape. Section 2.2.1 presents an overview of this proposal.

A little bit different approach on the noise modeling [5] is presented in Section 2.2.2. Unlike Verhoeven [4], Gierkink [5] derived expressions of jitter in relation to the real components of the oscillators (e.g. parameters of a comparator).

2.2.1 Verhoeven's high-level modeling of spectral noise shapes

Even though it seems that first-order oscillator principle is rather simple and straightforward, there are plenty of ways to implement it. Verhoeven showed in his dissertation [4] and with colleagues in the book [2], that it is possible to consider different topologies of the first-order oscillator on the high modeling level, classify different architectures based on these models, and describe noise of the oscillator based on these models.

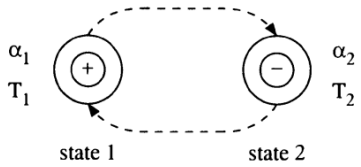

Figure 2.8 A state machine, describing basic function of the relaxation oscillator. The image is taken from [2].

The idea is that any first-order oscillator is an integrator or a system of several integrators that switch between certain states, so the oscillator is basically a state machine, that has different kinds of states, transitions between these states and triggers that cause the transitions. It is not necessary to describe all the classification to show the idea of noise modeling, presented by the author, so the most general and basic consideration is shown in Figure 2.8. Here the state machine has 2 states, that basically represent the states the one integrator relaxation oscillator has: state 1 is a phase, when the integrator has positive integration constant α_1 and duration of the state is T_1; in state 2 the integrator has negative integration constant α_2 and the state duration is T_2, Figure 2.9.

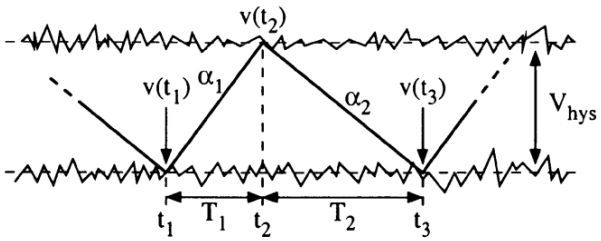

Figure 2.9 Generalized waveform of the integrator in relaxation oscillator with depicted comparator reference levels fluctuations. The image is taken from [2].

Noise sources

In linear systems, the noise behavior is commonly described by equivalent voltage and current noise sources at the input of the system. The noise behavior of the first-order oscillator cannot be described in this way as it can make transitions from one state to another. As the behavior of the system in both states is not the same, the noise behavior in both states can also change from state to state. When,

for instance, the sign of a current source is switched (to switch the sign of the integrated constant), the sign of the associated noise source can also be switched, depending on the implementation. Of course, the same holds for the voltage sources. So, there are noise sources that switch together with the state transitions and there are noise sources that do not switch together with the state transitions. Verhoeven [4] denoted these sources as correlated noise sources and uncorrelated noise sources respectively. It should be noted that the word correlation is used here to denote a correlation with the state of the oscillator, rather than to denote a mutual correlation between noise sources.

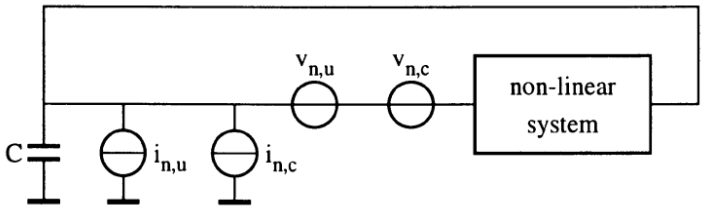

Figure 2.10 The four basic noise sources in a first-order oscillator by Verhoeven. The image is taken from [2].

Four basic noise sources can be distinguished in a first-order oscillator, since the effect of state correlation increases the number of required equivalent sources by a factor of two. They are shown in the noise model depicted in Figure 2.10. The noise sources with a subscript 'c' are correlated to the switching action whereas the noise sources with a subscript 'u' are uncorrelated to the switching action in the oscillator. If the noise sources in the active part of the circuit are white with respect to the oscillation frequency, all noise sources can be transformed to the input of the active circuit. [2]

Sampling system to describe first-order oscillator

Next step in [4] was the representation of the first-order oscillator as a sampling system.

A first-order oscillator is not a simple continuous-time system: it consists of states, between which the oscillator makes transitions, that are discrete-time events. The timing information in a first-order oscillator is contained in signal levels: the integrator output, comparator levels etc. So, the samples of these signal levels, taken at the transition moments, play an important role in noise models, since the period, frequency or duty cycle of the oscillation can be evaluated by taking a specific combination of samples taken at different transition instances.

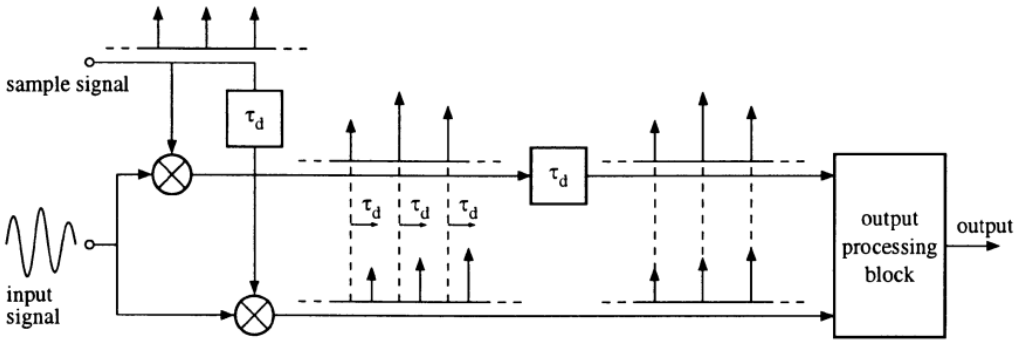

Figure 2.11 An example of the sampling system extracting timing information of the oscillator. The image is taken from [2].

Figure 2.11 presents an example of the sampling system that extracts timing information of the oscillator based on the above described procedure. As the sample pulses for one of the samplers are delayed by a time τ_d, the samples at the output of the samplers are samples from the input signal at different moments. To enable processing of these samples, an extra delay τ_d has to be inserted into

one of the signal paths. After this delay, the samples of the input signal, that were originally taken at different moments, now coincide, so the samples can be fed to the continuous-time output processing block. In this block, the desired calculation can be done on the two samples. Although this description is theoretically correct, the characteristics of the system cannot easily be evaluated. Z-domain analyses can be used to describe systems taking equidistant samples but are less suitable to describe this problem. Furthermore, the presence of more samplers also makes it hard to describe the system.

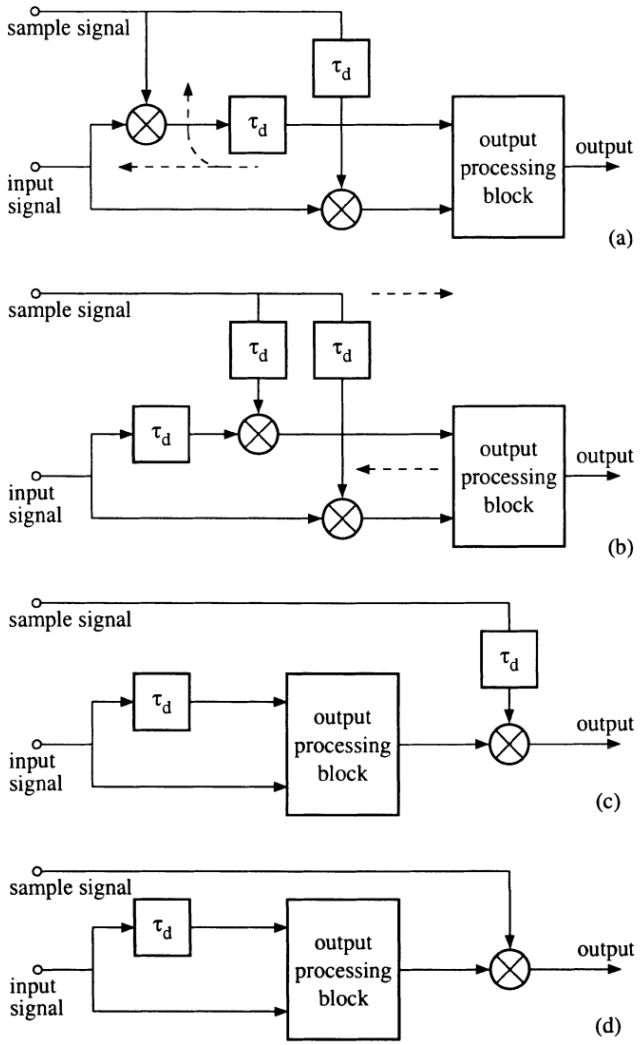

Figure 2.12 Transformations of the system from Figure 2.11 to enable simpler description of the sampling system. (a) Original system. (b-d) Consecutive transformation steps. The image is taken from [2].

However, it is possible to conduct certain transformations of the system from Figure 2.11 to simplify it, Figure 2.12. In the first step of the transformation, depicted in Figure 2.12b, the delay at the output of one sampler is pushed through the actual sampler, so that delays are now present both in the signal path in front of the sampler and in the sample path. Now, the samples in both branches are taken at the same time, so the first problem is solved. In the next transformation step, the complete output processing block is pushed through the sampling action and we end up with the system of Figure 2.12c. The output processing block now operates on the complete, continuous-time input signal and a delayed version of it. The samples are now taken after the output processing block. When the sampling moment does not have a specific phase relation to the input signal, the delay in the sample path can be omitted to yield the system of Figure 2.12d. The left part of the system, the delay section and the

processing section, can be considered in the s-domain using filter models. After that, the output of the system is sampled, what can also be easily described. [2]

Period/frequency noise caused by uncorrelated noise voltage sources

The assumption for all models was made by the author in [2]:

When the noise voltages in the oscillator are relatively small with respect to the total voltage swing of the oscillator signal, the transition moments in the noisy oscillator are approximately equal to the transition moments in a (fictitious) noise-free oscillator. Then, we can assume that the noise voltages at both instants are approximately equal:

$$V(t_n) = V(t_n^*) \tag{5}$$

In (5), t_n^* is the moment of the transition in the (fictious) noise free oscillator.

The following condition must hold for the assumption to be valid:

$$\frac{dV(t_n)}{dt}(t_n - t_n^*) \ll V_{hys} \tag{6}$$

where V_{hys} is the voltage swing between the two reference levels, Figure 2.9.

The relative variation of the period ζ was given by:

$$\zeta = \frac{t_n}{T_0} = \frac{1}{V_{hys}}\left[-d_{c_0} v_n(t_1^*) + v_n(t_2^*) - \left(1 - d_{c_0}\right) v_n(t_3^*)\right] \tag{7}$$

where T_0 is a total period of the noise-free oscillator ($T_0 = T_1 + T_2$ in Figure 2.9); t_n is a change of the period caused by noise; $v_n(t_1^*)$, $v_n(t_2^*)$ and $v_n(t_3^*)$ are noise voltages at transition instances 1, 2 and 3 respectively in Figure 2.9; d_{c_0} is the duty cycle of the oscillator.

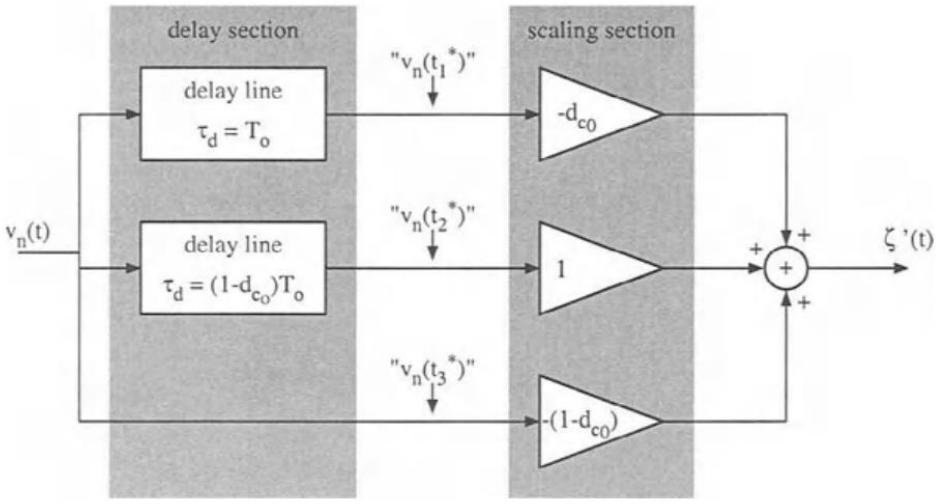

Figure 2.13 The sampling system to describe equation of the relative variation of the oscillator period in case of uncorrelated noise voltage source. The image is taken from [2].

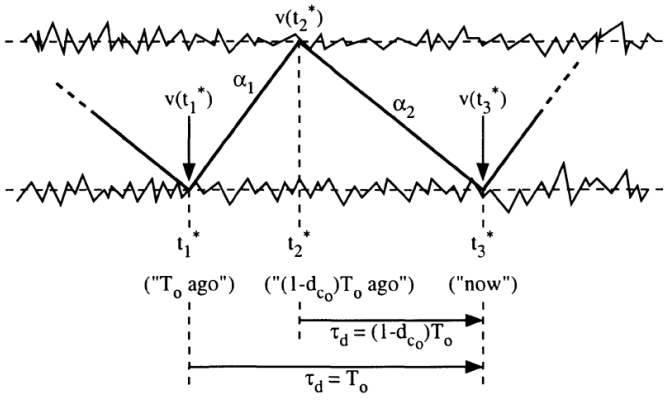

Figure 2.14 Application of the sampling system model to describe the oscillator. The image is taken from [2].

Figure 2.13 presents an example of the sampling system mentioned earlier (Figure 2.12d) that describe the oscillator relative period variation due to noise, ζ, expressed above by the equation. Figure 2.14 depicts a relation of the system to the integrator waveform, where the meaning of those delayed transition instances can be clearly seen.

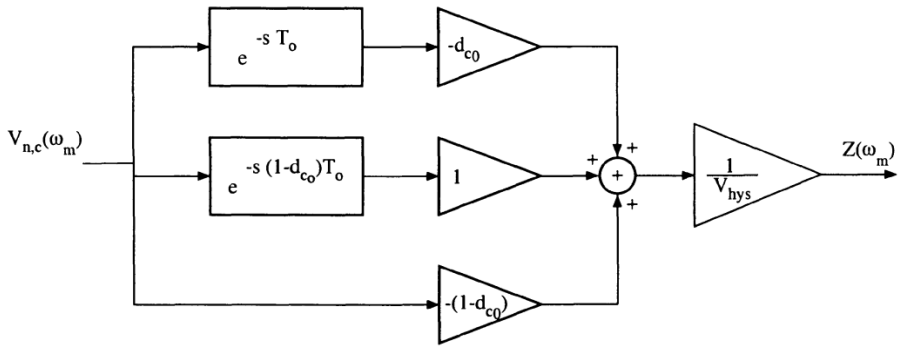

Figure 2.15. The filter that corresponds to the relative variation of the oscillator period due to noise in frequency domain. The image is taken from [2].

The sampling system, depicted in Figure 2.13, is in time domain, but the noise is generally expressed in frequency domain. So, it is possible to perform Laplace transform on the sampling system and obtain a filter, which is depicted in Figure 2.15. The equation of the filter response is

$$|H(j\omega_m)| = \frac{1}{V_{hys}}\left|-d_{c_0}e^{-j\omega_m T_0} + e^{-j\omega_m(1-d_{c_0})T_0} - \left(1-d_{c_0}\right)\right| \qquad (8)$$

and in case of duty cycle of 0.5, the equation can be simplified to

$$|H(j\omega_m)| = \frac{1}{V_{hys}}\left[1-\cos\left(\pi\frac{\omega_m}{\omega_0}\right)\right] \qquad (9)$$

The spectrum of the filter, presenting oscillator noise caused by the uncorrelated voltage noise source, is illustrated in Figure 2.16 for the case of duty cycle that equals to 0.5. It can be seen that even frequency components and DC components of the noise source have no influence on the operation. Another conclusion to be made is that 1/f noise (Appendix A), having dominant frequency components close to DC, can be taken out of consideration.

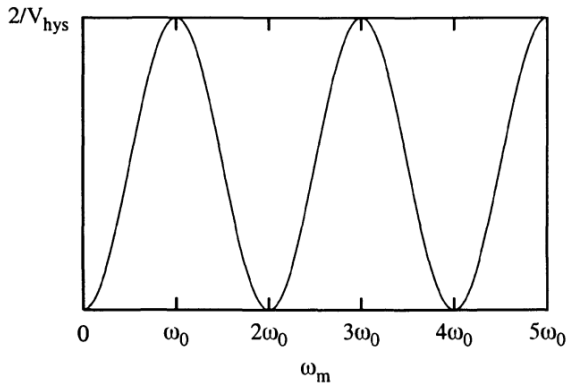

Figure 2.16 The modulus of the transfer of the filter from Figure 2.15, for the case when duty cycle is equal to 0.5. A DC noise source has no influence, noise components with a frequency close to the carrier frequency have maximal influence. The image is taken from [2].

As it was mentioned, the sampling system describing noise effect on the oscillator period relative variation is based on the model shown in Figure 2.12d, which has sampling of the output performed once every cycle. This sampling affects the oscillator frequency/period variation and Verhoeven [4] referred to Bennet model of noise (certain representation of white noise), which is described as the sum of an infinite number of sinusoidal components having equal amplitudes $\hat{v}_{n,u}$, differing frequencies and a random phase, to derive following expressions for the mean $\overline{\omega}_n$, the standard deviation σ_{ω_0} and the maximum deviation of the frequency $\Delta\omega_{0,peak}$, related to noise component with the frequency ω_m; duty cycle of the oscillator is supposed to be 0.5:

$$\overline{\omega}_n(\omega_m) = 0 \tag{10}$$

$$\sigma_{\omega_0}(\omega_m) = \frac{1}{2}\sqrt{2}\frac{\hat{v}_{n,u}}{V_{hys}}\omega_0\left[1-\cos\left(\pi\frac{\omega_m}{\omega_0}\right)\right] \tag{11}$$

$$\Delta\omega_{0,peak}(\omega_m) = \frac{\hat{v}_{n,u}}{V_{hys}}\omega_0\left[1-\cos\left(\pi\frac{\omega_m}{\omega_0}\right)\right] \tag{12}$$

Another important effect worth mentioning is so called “folding of noise”. The idea is depicted in Figure 2.17. The white noise (e.g. of uncorrelated voltage source) passes through the filter described earlier and the output from the filter is sampled with the frequency of the oscillator. The process can be described by convolution of the output of the filter with the sequence of sample pulses spaced at intervals equivalent to the sampling frequency. It can be seen that resulting spectrum is composed by frequency components ‘folded’ back to lower frequencies, e.g. frequency component of ω_0 is folded back to DC. This folding is only limited by the bandwidth of the system (the noise conversion bandwidth, N_{cb}), since real oscillators cannot have infinitely fast transition between states. [2]

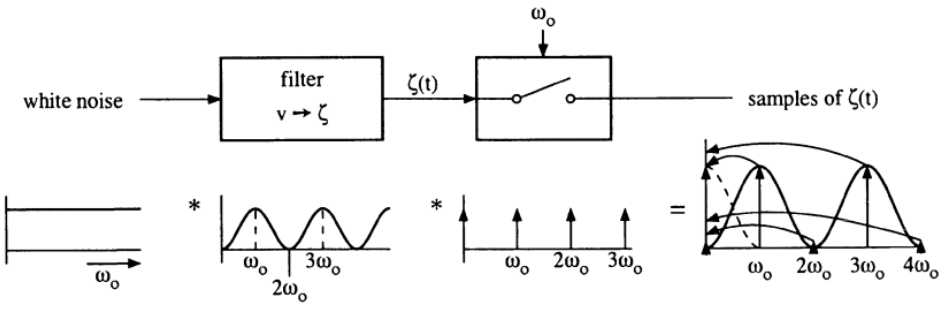

Figure 2.17 The sampling affecting the noise spectrum of the oscillator. The image is taken from [2].

Period/frequency noise caused by correlated noise voltage sources

The procedure of creating noise model of the oscillator with correlated noise voltage sources to switching action is very similar to the case presented above (uncorrelated noise voltage sources). The only difference is that we have to take into account that the sign of the voltage source is changed on each cycle. Therefore, the resulting equations are different, and the filter output characteristic is different, which is depicted in Figure 2.18. It can be seen in the figure that in the case of a correlated noise voltage, the influence of DC components is large, whereas the influence of noise sources close to odd multiples of the oscillation frequency is minimal. The author denoted that it means that 1/f noise can pass through the filter, as 1/f noise components cause low-frequency variations of the oscillator frequency.

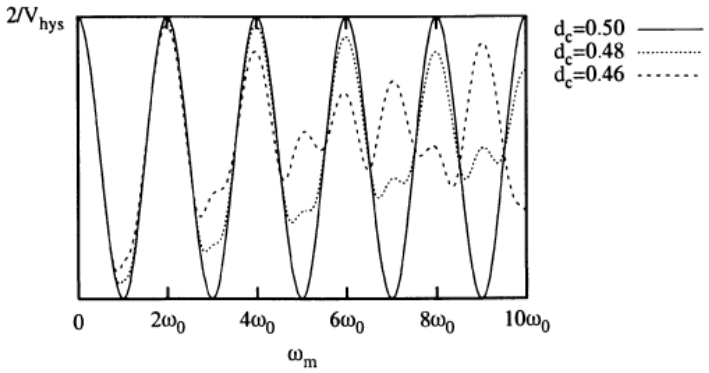

Figure 2.18 The modulus of the transfer of the filter corresponding to the model of oscillator noise caused by the correlated noise voltage source (d_{c_0} is duty cycle). The image is taken from [2].

Period/frequency noise caused by uncorrelated noise current sources

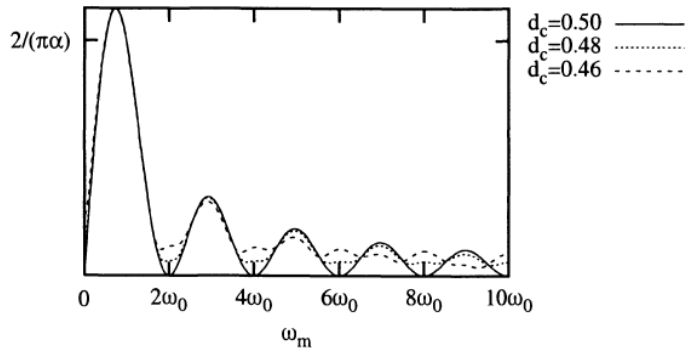

Figure 2.19 The modulus of the transfer of the filter corresponding to the model of oscillator noise caused by the uncorrelated noise current source (d_{c_0} is duty cycle). The image is taken from [2].

Figure 2.19 represents the transfer of the filter, modeling effect of the uncorrelated noise current source on the frequency of oscillator. The low-frequency components of the noise source do not affect the oscillator frequency, so 1/f noise is not the dominant cause of frequency deviations. It can be seen that the noise components close to even multiples of the oscillator frequency are suppressed.

As it was already mentioned, components around multiples of the oscillation frequency are folded back to DC due to “folding of noise” effect (Figure 2.17), what happens for current noise as well, but according to [2], if the current source is integrated, this effect is much less visible than in case of voltage noise sources.

Period/frequency noise caused by correlated noise current sources

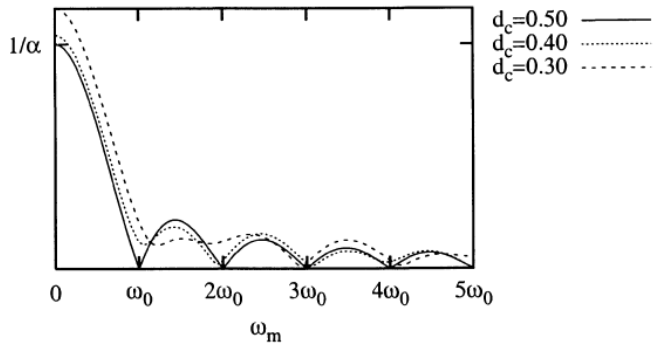

Figure 2.20 The modulus of the transfer of the filter corresponding to the model of oscillator noise caused by the correlated noise current source (d_{c_0} is duty cycle). The image is taken from [2].

Figure 2.20 represents the transfer of the filter, modeling effect of the correlated noise current source on the frequency of oscillator. The low-frequency components of the noise source affect the oscillator frequency. It can be seen that the noise components close to odd multiples of the oscillator frequency are suppressed.

2.2.2 Gierkink's jitter

Gierkink's discussion on jitter (in [5]) starts with the assumption that most noise sources, appearing in the relaxation oscillator circuit, can be represented by an equivalent noise source that is either (Figure 2.21):

- a current noise source i_n in parallel with the capacitor charge current I_{charge};
- a voltage noise source v_n in series with the reference voltage V_{REF}.

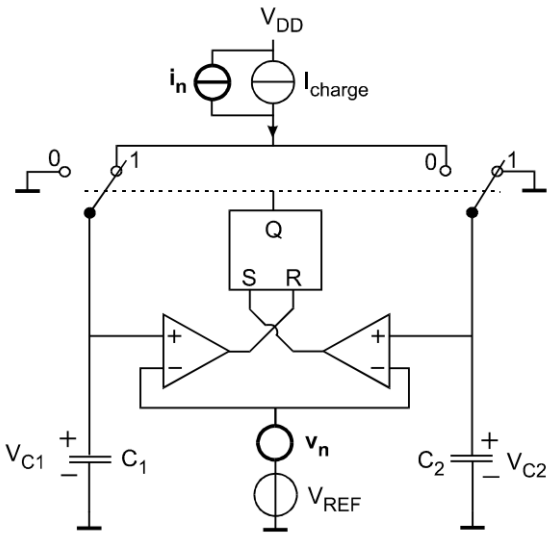

Figure 2.21 Sawtooth relaxation oscillator with the noise source considered by Gierkink in [5]. The image is taken from [5].

Jitter due to current noise in parallel with charging current

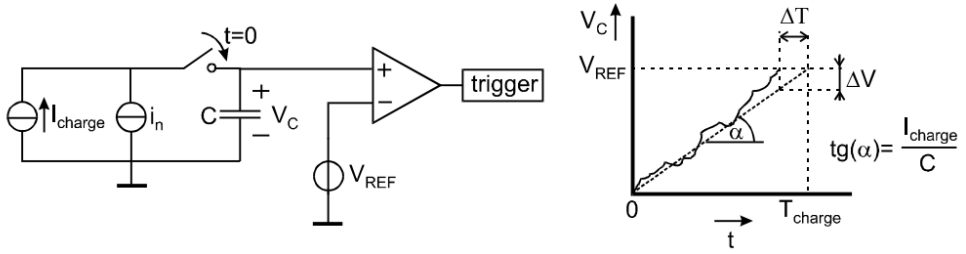

Figure 2.22 Signal model and capacitor voltage waveform in case of a noisy charging current, considered in [5]. The image is taken from [5].

Figure 2.22 depicts the model (and the waveform of it) used by Gierkink [5] to derive the expression for the jitter caused by noise current source located in parallel to the charging current source. The derived expression for the considered normalized one-period jitter is

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}}\right)_{i_n} = \frac{\sqrt{\frac{S_{i_n}}{2} f_{osc}}}{I_{charge}} \quad (13)$$

where S_{i_n} is the power spectral density of the noise from the noisy current source; f_{osc} is the oscillation frequency; I_{charge} is the charging current.

It can be seen that the noisy current noise contributes to jitter by effective noise bandwidth that equals $f_{osc}/2$.

Nevertheless, the author denotes that, assuming white noise, the timing errors made in successive periods are uncorrelated, so the variance $\sigma_{\Delta T}^2$ of the timing error ΔT, that occurs after an interval $\tau = n \cdot T_{osc}$, is proportional to n:

$$\sigma_{\Delta T}^2(\tau = n \cdot T_{osc}) = n \cdot \sigma_{\Delta T_{osc}}^2 \quad (14)$$

where $\sigma_{\Delta T_{osc}}^2$ is variance of the one-period timing error.

Gierkink showed that the above-mentioned time-domain behavior (14) can be related to the phase noise spectrum and the following proportionality is obtained:

$$S_\varphi(f) \propto f^{-2} \quad (15)$$

where $S_\varphi(f)$ is the frequency dependency of the power spectral density of phase fluctuations.

Jitter due to voltage noise in series with reference voltage

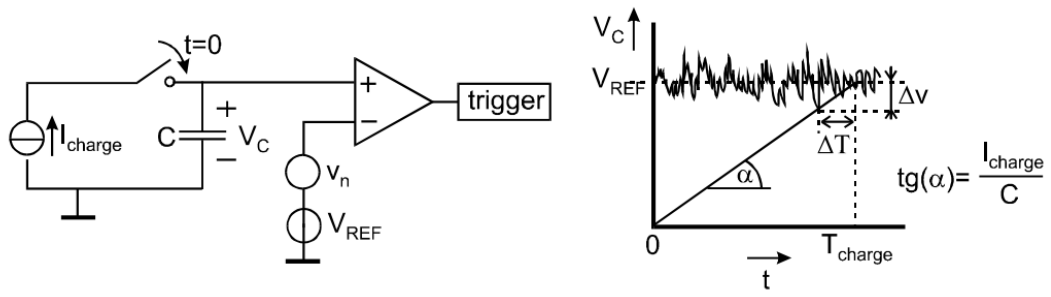

Figure 2.23 Signal model and capacitor voltage waveform in case of a noisy reference voltage, considered in [5]. The image is taken from [5].

Figure 2.23 depicts the model (and the waveform of it) used by Gierkink to derive the expression for the jitter caused by noise voltage source located in series with the reference voltage source. Figure 2.24 gives a simplified circuit of the comparator that was used in jitter calculations by the author, since Gierkink considered effects of parasitic capacitors and comparator differential pair switching time.

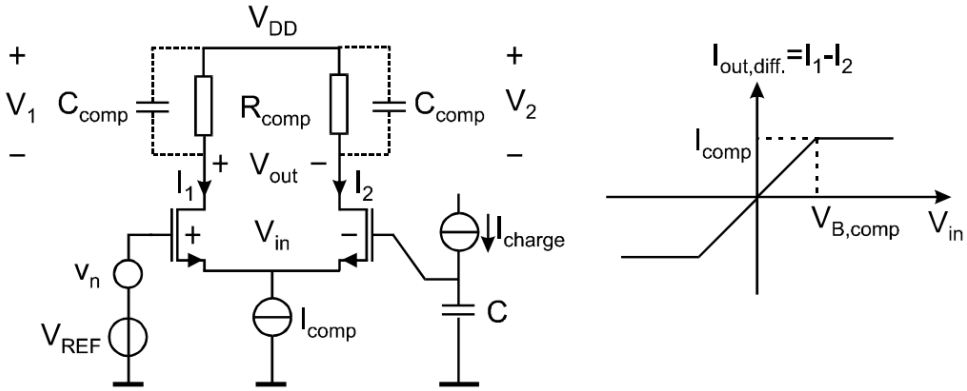

Figure 2.24 The comparator model and the linearized transfer function of its differential pair, used by Gierkink [5] to derive jitter in case in of a noisy reference voltage. The image is taken from [5].

Jitter of the oscillator with comparator without parasitic capacitors was given in [5] by:

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}}\right)_{v_n} = \frac{\sqrt{\frac{S_{v_n}}{2} \cdot B_n}}{V_{REF}} \qquad (16)$$

where S_{v_n} is power spectral density of the reference voltage noise; B_n is the noise source bandwidth; V_{REF} is reference voltage. So, the jitter due to voltage noise v_n in series with decision level V_{REF} is related to the signal-to-noise ratio of the decision level.

There were two cases considered in [5], concerning effect of the parasitic RC-combination at the output node of the comparator model from Figure 2.24. One case is when the delay $\tau_{comp} = R_{comp} \cdot C_{comp}$, given by the mentioned RC-combination, is much smaller than the switching time of the comparator's differential pair $T_{switch,diff.pair}$; another case is when the delay is much greater than the comparator differential pair switching time.

When $\tau_{comp} \ll T_{switch,diff.pair}$, the jitter was given by

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}}\right)_{v_n} = \frac{\sqrt{\frac{S_{v_n}}{2} \cdot B_{n,comp}}}{V_{REF}} \qquad (17)$$

where $B_{n,comp}$ is the noise bandwidth (single sided) of the comparator, which was given by

$$B_{n,comp} = \frac{1}{R_{comp}^2} \int_0^\infty \frac{R_{comp}^2}{1+\left(2\pi f \cdot R_{comp} C_{comp}\right)^2} df = \frac{1}{4 R_{comp} C_{comp}} \quad [Hz] \qquad (18)$$

where R_{comp} and parasitic C_{comp} form the RC-combination at the output of the comparator, Figure 2.24.

When $\tau_{comp} \gg T_{switch,diff.pair}$, the jitter was given by

$$\left(\frac{\sigma_{\Delta T_{osc}}}{T_{osc}}\right)_{v_n} = \frac{\sqrt{\frac{S_{v_n}}{4}\cdot\frac{1}{T_{switch,diff.pair}}}}{V_{REF}} \quad (19)$$

where $T_{switch,diff.pair}$ is the switching time of the comparator differential pair.

Comparison of jitter caused by noisy current and voltage

The above-considered jitters, caused by noisy current or reference voltage, contributed to the total jitter of the oscillator and Gierkink discussed the relation of this contributions to the optimal design of the oscillator in [5].

First, the noise was approximated by the thermal noise of a resistor, leading to

$$S_{i_n} = \frac{4kT}{R_{n,i}} \qquad [A^2/Hz] \quad (20)$$

$$S_{v_n} = 4kTR_{n,v} \quad [V^2/Hz] \quad (21)$$

As it was mentioned earlier, Gierkink [5] discussed two situations, concerning the jitter of the noisy voltage source, and it turned out that the most practical design implies that $\tau_{comp} \ll T_{switch,diff.pair}$, since in that case the oscillator would have higher control linearity, what can, for example, simplify trimming for reduction of process variations.

Implying jitter caused by noisy voltage for the case when $\tau_{comp} \ll T_{switch,diff.pair}$, the resistor noise model and expression for the total jitter

$$\left(\sigma_{\Delta T_{osc}}\right)^2 = \left(\sigma_{\Delta T_{osc},i_n}\right)^2 + \left(\sigma_{\Delta T_{osc},v_n}\right)^2 \quad (22)$$

Gierkink [5] derived the jitter ratio:

$$\left(\frac{\sigma_{\Delta T_{osc},v_n}}{\sigma_{\Delta T_{osc},i_n}}\right)^2 = \frac{B_{n,comp}}{f_{osc}} \cdot \frac{P_{diss,I_{charge}}}{P_{diss,V_{REF}}} \quad (23)$$

where $P_{diss,I_{charge}}$ and $P_{diss,V_{REF}}$ are the powers dissipated in realizations of charging current source and reference voltage source respectively.

Since condition $\tau_{comp} \ll T_{switch,diff.pair}$ was assumed, the following must be valid

$$B_{n,comp} \gg f_{osc} \quad (24)$$

So, to reduce the total jitter, the design must imply that

$$P_{diss,V_{REF}} \gg P_{diss,I_{charge}} \quad (25)$$

3 Review of recent proposals

This section describes the state-of-art realizations of relaxation oscillators. These realizations employ different design techniques for jitter, temperature and process variations compensation in the oscillators. So, the following review can pose a benefit for my design. Moreover, the goal of this section is to find the most appropriate architecture to implement the oscillator corresponding to the requirements stated in Section 1.2.

The chosen designs represent major ideas in achieving the most optimal performance of the integrated relaxation oscillator. It would be fair to mention that the field possesses a wider range of proposals, which mostly employ similar principles as the designs considered below. However, there are also quite exotic topologies (e.g. [9]–[13]) that are not considered in the following discussion, but having been studied during the literature research were denied as candidates for my design topology.

3.1 Relaxation oscillator employing voltage averaging feedback

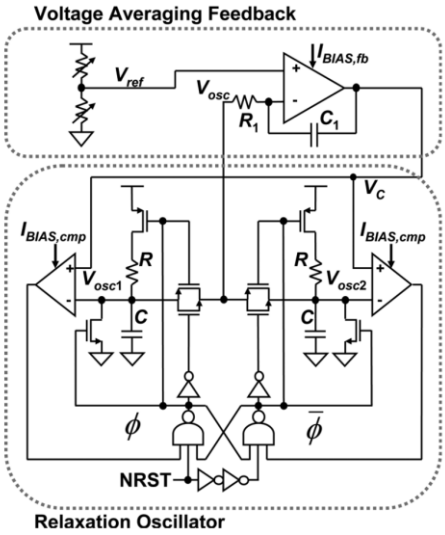

Figure 3.1 The oscillator structure proposed in [14]. The image is taken from [14].

One of main issues of relaxation oscillator accuracy is the comparator delay (t_d) variation, and a simple way to overcome it is shortening of t_d to the level that it can be neglected. However, this approach leads to an increase in power supplied to comparators (and increase of noise bandwidth of the comparators, Section 2.2.2). Figure 3.1 depicts the oscillator structure proposed in [14] [15], comprising voltage averaging feedback to achieve both accuracy and low power dissipation by maintaining whole oscillator waveform including t_d. This design solves an issue of the delay variation, since the oscillation is independent on the comparator delay t_d, and also the structure does not contain integrator biasing current sources, reducing the effects of aging and flicker noise.

3.1.1 The design considerations

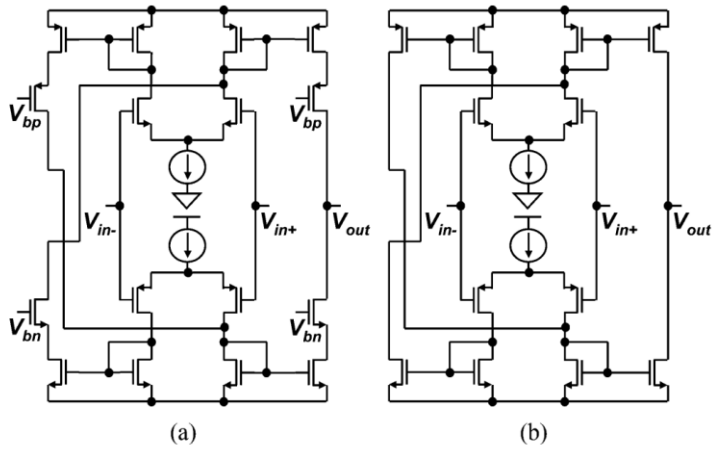

Figure 3.2 Circuit schematics of (a) feedback amplifier and (b) comparator, that are utilized in [14]. The image is taken from [14].

Figure 3.2 presents the topologies of the feedback amplifier and the comparator, used for realization of the design proposed in [14], for rail-to-rail input and easiness to obtain enough phase margin.

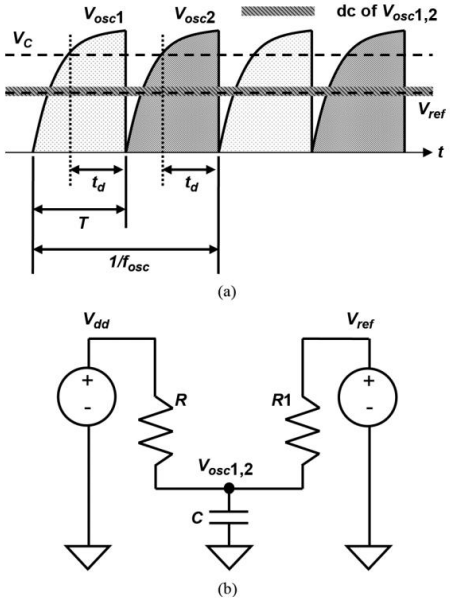

Figure 3.3 (a) Waveform and (b) modeling of oscillation in [14]. The image is taken from [14].

In Figure 3.1 the relaxation oscillator part is considered as a voltage-controlled oscillator with a control signal V_C. Oscillation waveforms V_{osc1} and V_{osc2} are summed up to V_{osc} and transferred to the active filter part. At this condition, the active filter maintains DC voltage of whole oscillation at the reference voltage V_{ref} as shown in Figure. 3.3(a). Figure 3.3(b) depicts the half circuit simplification of the oscillator, leading to the following relation (26) (under condition $R_1 \gg R$ and considering that V_{ref} is generated by a voltage divider of rail-to-rail voltages):

$$\frac{(1-\alpha)T}{RC} = 1 - e^{-\frac{T}{RC}} \quad (26)$$

where T is period of oscillation and

$$\alpha = \frac{V_{ref}}{V_{dd}} \quad (27)$$

The above-presented equation (26) underlines that the oscillation frequency is just defined by a time constant RC and a coefficient α (27). The variation of t_d has little effect on T, because the voltage averaging feedback automatically adjusts V_C to keep the equilibrium of

$$\frac{1}{T}\int_0^T V_{osc1,2}(t)dt = V_{ref} \quad (28)$$

The oscillation frequency neither has any sensitivity to V_{dd}, since α is fixed by the resistor divider.

The oscillation frequency is tunable by applying a digital trimming configuration to the resistor divider (adjusting α), which compensates absolute variations of R and C. The sensitivity to temperature is dominated by R, if we consider Metal-Oxide-Metal capacitor in standard CMOS processes, so the resistor has to be temperature compensated (e.g. by combining resistors with the temperature coefficients of opposite signs).

3.1.2 Start-up sequence

This section provides the start-up sequence of the proposed oscillator design in [14], the description is related to Figure 3.1:

1. V_C are set as a certain voltage (e.g., V_{ref}) at the reset state (where NRST is "Low"). V_{osc1} and V_{osc2} are pulled down to "Low" by NMOS devices with "High" input from the SR-latch.
2. There is the time difference to start-up two NANDs in the SR-latch by an inverter-delay line and the left-side NAND is firstly released from the reset state and this time difference outputs a "Low" signal. Therefore, the capacitance of the left-side half-circuit starts to be charged and to rise V_{osc1}. At this time, the left-side transfer gate is shorted and V_{osc1} is transmitted to the LPF (low-pass filter) as V_{osc}.
3. When V_{osc1} exceeds V_C, the left-side comparator pulls down the output itself to "Low" and the output of the left-side NAND rises up to "High" again. Then, V_{osc1} is pulled down to "Low", the output of the left-side comparator returns to "High" and the left-side transfer gate is opened to stop transmission of V_{osc1}.
4. When the output of the left-side NAND is "High", the right-side NAND changes the output itself to "Low" because its inputs are all "High", and V_{osc2} of the rightside half-circuit starts to rise and to be transmitted to the LPF as V_{osc}.

   In the same manner as the left-side half-circuit, when V_{osc2} exceeds V_C, the right-side comparator pulls down the output itself to "Low" and flips the SR-latch output, which results in pulling down of V_{osc2} to "Low". The right-side transfer gate is shorted and transmission of V_{osc2} to the LPF is stopped. Then, the output of the right-side comparator returns to "High".

   "Low" output of the left-side NAND causes V_{osc1} to rise again.

The circuit (Figure 3.1) oscillates as a multi-vibrator iterating the above steps from 3 to 6. Settling waveforms of V_{osc1} and V_{osc2} are transmitted alternately to the LPF. Then the DC voltage of the waveform is virtually shorted to V_{ref} by the active filter.

3.1.3 Sensitivity to the reference. Noise reduction

The equation (26), expressing dependence of T on α and RC, was used in [14] to consider sensitivity of the oscillation period variation due to variations of α:

$$\frac{\partial T/T}{\partial \alpha} = \frac{1}{\frac{RC}{T}\left(1-e^{-T/RC}\right)-e^{-T/RC}} \quad (29)$$

Since the above equation (29) is too complicated to extract a solution as a function of α, a numerical analysis was conducted by the authors of [14], which led to the following result: the minimum theoretical sensitivity of 3.351 at $\alpha = 0.535$ for any RC and V_{dd}.

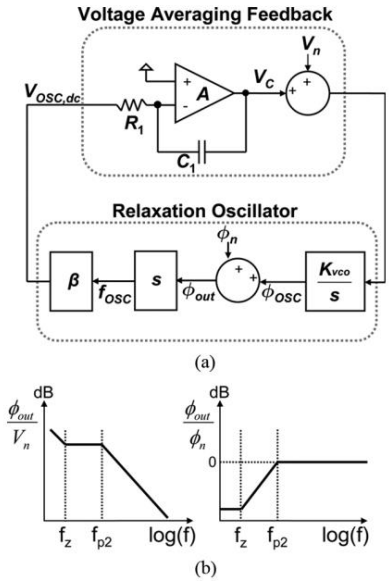

Figure 3.4 (a) Noise transfer model and (b) noise transfer gains from two dominant noises to phase noise, of the design proposed in [14]. The image is taken from [14].

Also, in [14] it is claimed that the proposed voltage averaging feedback reduces the flicker noise due to its closed-loop structure. Figure 3.4 illustrates the noise transfer model of the relaxation oscillator with voltage averaging feedback and the resulting transfer characteristics of two dominant noises. The relaxation oscillator part is modeled as a voltage-controlled oscillator (VCO), where the frequency gain is K_{VCO} and the periodic integration $V_{osc,dc}$ of V_{osc} is proportional to the input voltage V_C with a coefficient β. Dominant noises from an active filter and a VCO are transferred to the phase noise by their closed-loop transfer functions respectively and summed up by RMS manner at φ_{out}. The benefit of the voltage averaging feedback is that the low offset frequency part of phase noise of the VCO part is suppressed by negative feedback effect. This means that the voltage averaging feedback concept allows to use small transistors in comparators for accurate oscillation with low power.

3.1.4 The performance

The oscillator considered in [14] was fabricated in $0.18\ \mu m$ standard CMOS process with $R = 65\ k\Omega$, $C = 200\ fF$, $R_1 = 1\ M\Omega$, $C_1 = 1\ pF$, and $\alpha = 0.54$. The active area is $0.04\ mm^2$.

Table 3.1 presents summary of the measured parameters of the oscillator proposed in [14].

Process	$0.18\ \mu m$ CMOS
Area	$0.04\ mm^2$
Frequency	$14\ MHz$
Power supply voltage	$1.8\ V$
Current consumption	$25\ \mu A$
Figure of merit (FOM) [16]	$-146\ dB$ @ $100\ kHz$, $-146\ dB$ @ $4\ kHz$
Variation with power supply voltage	± 0.16 % @ 1.7 to 1.9 V
Variation with temperature	± 0.75 % @ -40 to $125\ ^{\circ}C$

Table 3.1 Performance summary of the oscillator in [14].

3.2 Relaxation oscillator employing a feedforward period control scheme

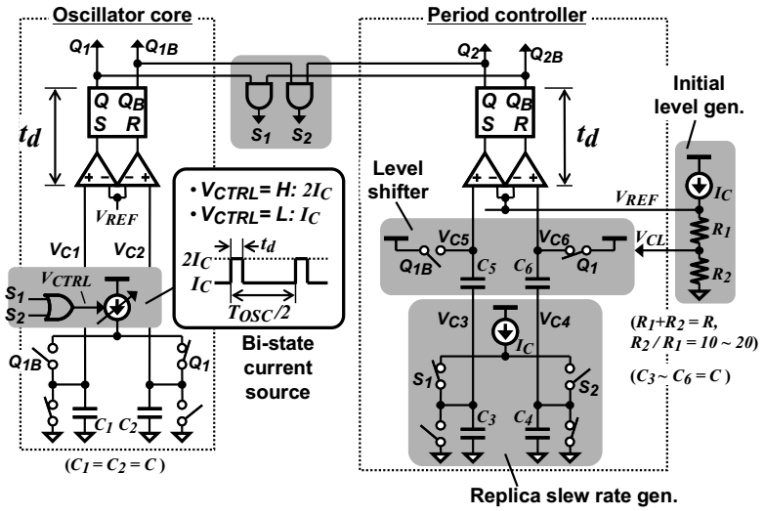

Figure 3.5 Schematic of the relaxation oscillator with feedforward period control scheme. The image is taken from [17].

Figure 3.5 presents the realization proposed in [17]. The idea is to provide a very short start-up time with low power consumption and low frequency error. The circuit consists of an oscillator core and a period controller, which cancels feedforward delay t_d of the regenerative circuit (comparator + SR-latch), since this delay varies with temperature, especially in the case when biasing current is kept low to reduce power consumption.

3.2.1 Comparator and SR-latch delay cancellation

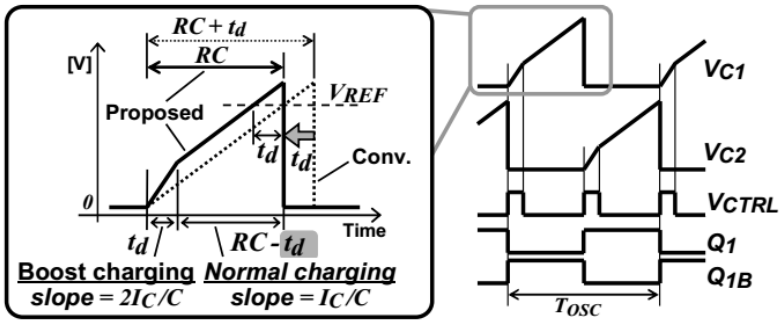

Figure 3.6 Waveform of the capacitor voltage in the feedforward period control scheme. The image is taken from [17].

The feedforward delay t_d cancelling is performed by switching the charging current I_C digitally instead of by means of analog threshold voltage control. It can be seen in Figure 3.6, that by shifting t_d ahead of the timing at which the comparator input level reaches V_{REF}, the half period can be made to be equal $R \cdot C$, so the oscillation is insensitive to t_d. The t_d shift is performed simply by doubling the charging current during t_d at the beginning of every half cycle of oscillation (boost charging). The determination of the degree to which t_d should be shifted and the switching of charging current are handled by the oscillation period controller.

The oscillator core in Figure 3.5 employs bi-state current source for boost and normal charging. The measurement of t_d at the beginning of every half period is done by replicas of the comparator and the SR-latch in the period controller. The initial reference level for the replica comparator inputs (V_{C5} and V_{C6}) is set to V_{CL}, which is slightly lower than V_{REF} because the replica comparator must operate immediately after the oscillator core output toggling. The input signals to the replica and core comparators have to have the same slew rate, because the delay will vary depending on the slew rate. Therefore, the design in [17] contains an initial level generator, a level shifter and a replica slew rate generator in the period controller, Figure 3.5.

3.2.2 The period controller operation

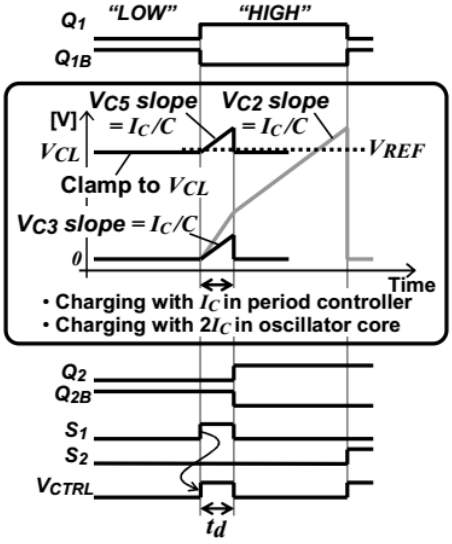

Figure 3.7 Waveforms of the period controller in the design proposed in [17]. The image is taken from [17].

The waveforms shown in Figure 3.7 represent a single period operation in the period controller. When the oscillator core output signal (Q_1) is in the "LOW" state, capacitor C_3 is fully discharged, and the replica input signal V_{C5} is clamped to V_{CL}. When Q_1 changes to "HIGH" state, the clamp switch is open, and capacitor C_3 begins to be charged with charging current I_C. The capacitor voltage V_{C3} has the same slew rate as that of the oscillator core in normal charging. Because capacitor C_5 stores its charge, V_{C5} also has the same slew-rate, and its voltage level can be represented as $V_{C3} + V_{CL}$. After Q_1 enters the "HIGH" state and t_d has subsequently elapsed, the replica SR-latch output (Q_2) changes to "HIGH" state. A control pulse V_{CTRL} that is in the "HIGH" state during t_d is generated by a simple logical operation using core and replica latch outputs, and the oscillator core comparator input (V_{C2}) is then charged with the boost charging current ($2I_C$).

3.2.3 The performance

The authors of [17] fabricated the oscillator with their proposed design in 90nm CMOS technology. The active area is $0.12\ mm^2$. The capacitors had negligible temperature dependence, since they were of Metal-Oxide-Metal type. The resistors temperature dependency was compensated by combining resistors with temperature coefficients having opposite signs.

Measurement results depicted in Figure 3.8 prove that the period control scheme can successfully reduce the frequency variations due to changes in temperature and supply voltage to, respectively ± 0.68 % and ± 0.82 %.

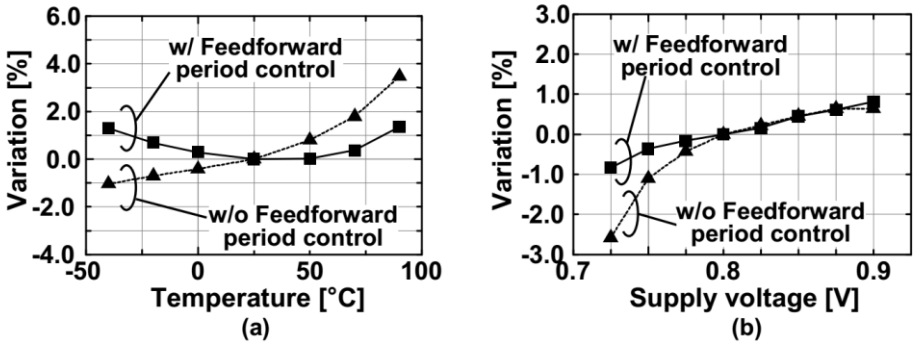

Figure 3.8 Measured frequency variation of the oscillator in [17] with respect to (a) temperature, (b) supply voltage. The dependencies are shown for the circuits with the enabled and disabled feedforward period control. The image is taken from [17].

Table 3.2 presents summary of the measured performance of the oscillator, proposed in [17]. As it was mentioned by the authors of [17], their design is advantageous for certain applications over the design reviewed in Section 3.1, since it has much shorter start-up time (measured 1 cycle for the architecture in [17] as opposed to simulated 140 cycles for the architecture in [14]).

Process	90nm CMOS
Operation frequency	100 kHz
Power consumption	0.28 µW
Start-up time	1 cycle
Variation due to temperature	±0.68 % @ -40 to 90 °C
Variation due to power supply voltage	±0.82 % @ 0.725 to 0.9 V

Table 3.2 Performance summary of the oscillator in [17].

3.3 Relaxation oscillator employing dynamic threshold and switched resistors

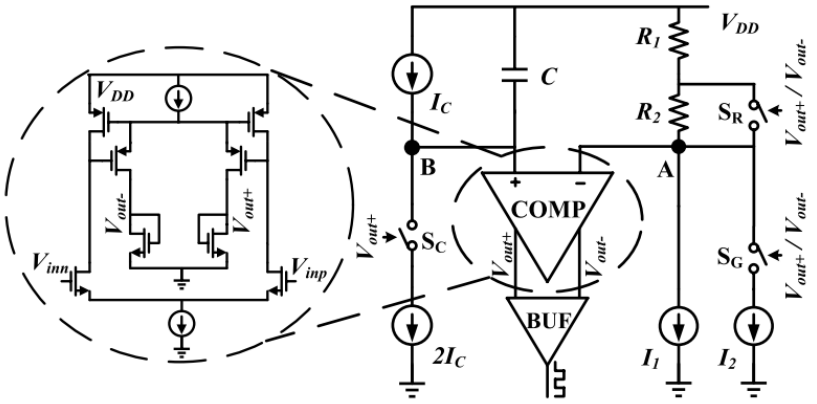

Figure 3.9 Schematic of the relaxation oscillator with dynamic threshold. The image is taken from [18].

Figure 3.9 demonstrates the topology of the relaxation oscillator, presented in [18], that utilizes dynamic threshold and switched resistors technique. The idea is to reduce the dependence of the output frequency on the power supply without application of the band-gap voltage reference, which occupies big area on the chip and contributes to higher power consumption.

The function of the oscillator is based on the principle discussed in Section 2.1.1, since it employs only one integrator. However, the voltage thresholds (V_H and V_L in Figure 2.4), defining a time instance of the comparator regeneration, are dynamic to insure good stability.

3.3.1 Dynamic threshold technique

The description of the dynamic threshold (DT) technique in [18] is as follows (Figure 3.9):

1. At the beginning of power on, V_A, the voltage of node A in Fig. 3.9, rises quickly to $V_H = V_{DD} - I_1 \cdot R$, while V_B, the voltage of node B, grows slowly with I_C due to the large capacitor load. During this interval, the comparator output keeps the switches off.

2. When $V_B > V_A = V_H$, the comparator output flips over and turns the switches S_C and S_G on. Then, V_A drops rapidly to $V_L = V_{DD} - (I_1 + I_2) \cdot R$. At the same time, the charges in capacitor are drained out resulting in a decrease of V_B. The state of oscillator changes to the discharging phase.

3. When $V_B < V_A = V_L$, the comparator output turns the switches off again. Thus, the state of the oscillator returns to the charging phase.

So, as it can be seen the threshold voltage levels are not static and the resulting oscillation period has a form of

$$T = 2R \cdot C \cdot \frac{I_2}{I_C} + 4t_p \quad (30)$$

where t_p is a delay of the comparator.

The authors of [18] suggested that the delay of their comparator was $1.74\ ns$ with temperature drift of $12.81\ \%$ from $-40°C$ to $120°C$, so they claimed that it had a negligible impact on the frequency stability, but the major contributor to the power consumption. Figure 3.10 presents the simulated waveforms of voltages V_A and V_B by the authors.

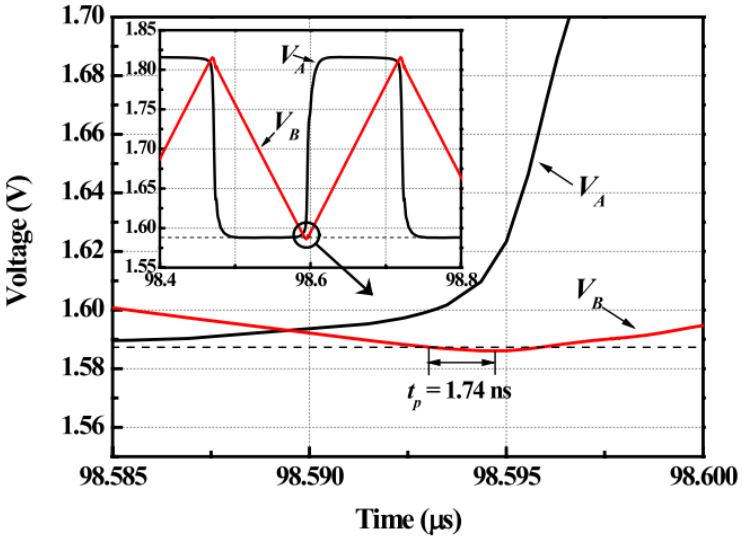

Figure 3.10 Simulation waveform of the voltages of nodes A and B in Figure 3.9, presented by the authors of [18]. The image is taken from [18].

3.3.2 Switched resistors technique

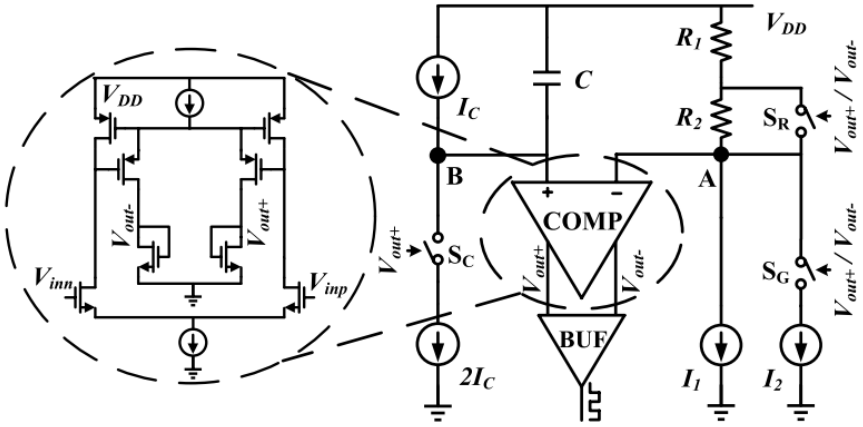

Figure 3.11 Schematic of the relaxation oscillator with dynamic threshold and switches resistors. The image is taken from [18].

Figure 3.11 depicts the modification of the topology depicted in Figure 3.9 by employing the switched resistors (ST) technique, proposed in [18]. The idea is to compensate the temperature variation of the oscillation frequency, since, according to (30), it depends on the resistor value. The principle realized in ST technique is the application of the two resistors defining the threshold levels V_H and V_L, so that these thresholds are not changed relative to each other. The ST technique allows to utilize resistors with temperature coefficients (TCs) of the same and opposite sign, the difference will be in the switching of S_R and S_G.

3.3.3 The performance

The authors of [18] implemented their design in $350\ nm$ standard CMOS process. The performance of their system is illustrated in Table 3.3.

Technology (μm)	0.35
Area (mm^2)	0.05
Frequency (MHz)	4
Current consumption (μA)	280 @ 3 V
FOM $(\mu W/kHz)$	0.21
Power supply sensitivity $(\%/V)$	0.6 @ 2.4 to 4
Temperature sensitivity $(ppm/°C)$	53.9 @ -30 to $120°C$

Table 3.3 Performance summary of the oscillator in [18].

3.4 Relaxation oscillator employing IEF

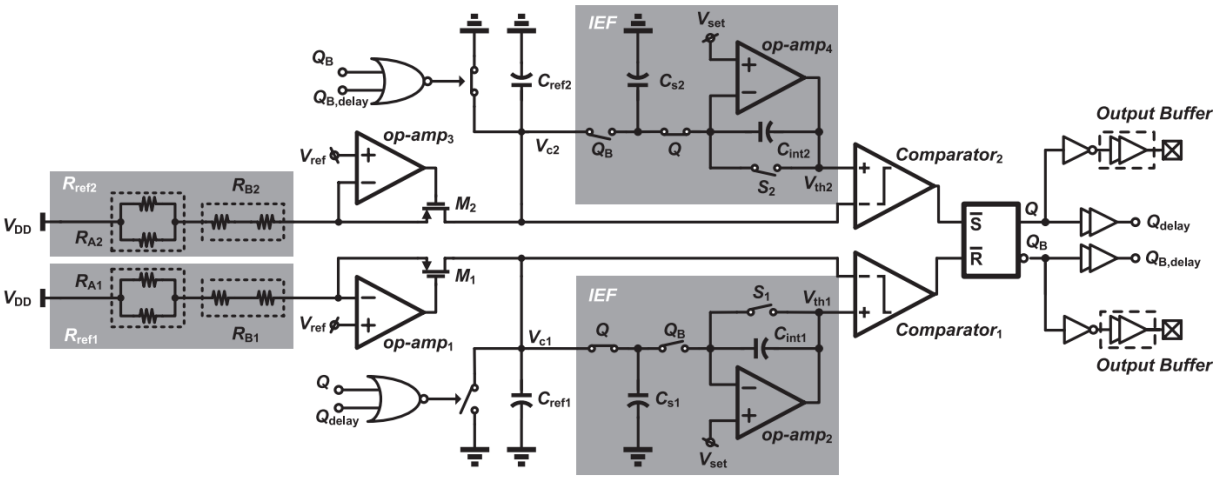

Figure 3.12 Schematic of the relaxation oscillator with IEF. The image is taken from [19].

The authors of [19] presented an architecture of the relaxation oscillator that utilizes the Integrated-error Feedback (IEF) technique, Figure 3.12. The idea of this topology is to compensate the comparators offset by dynamic adjustment of the reference voltage level (peak voltage of the reference capacitor is sampled and fed to the integrator block of IEF) . The design employs a current

source based on resistors with the temperature coefficients of opposite sign to generate precise charging current. The topology corresponds to the studied sawtooth two-integrator oscillator in Section 2.1.2 and depicted in Figure 2.5.

3.4.1 IEF application

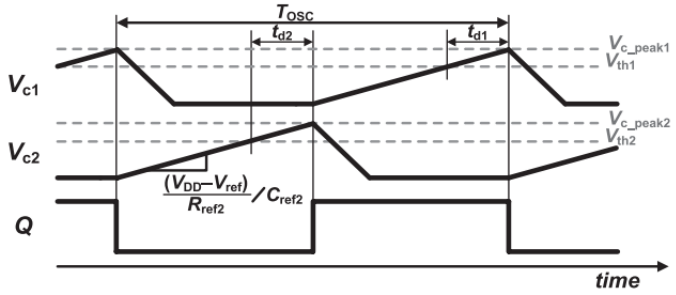

Figure 3.13 Timing diagrams of relaxation oscillator with a delay t_d. The image is taken from [19].

If we compare the topologies presented in Figure 3.12 and Figure 2.5, it will become clear that the only difference is the utilization of the reference voltage. In Figure 2.5 it is supposed that the reference level is fed to the comparator directly and is stable during the operation. The oscillator with IEF, however, utilizes sampling of the peak voltage V_{c_peak} (Figure 3.13) of the reference capacitors C_{ref1}, C_{ref2} (Figure 3.12) and integrates the overshoots of the capacitors ($V_{c\_peak} - V_{set}$, where V_{set} is the nominal reference level) to reduce the references fed to the comparators and keep V_{c_peak} at the same level as V_{set}, Figure 3.14.

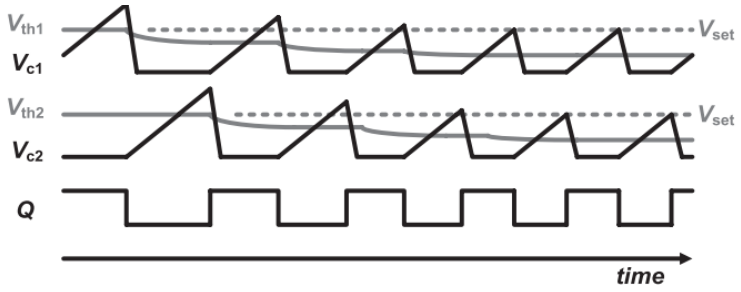

Figure 3.14 Waveforms of the oscillator with IEF. V_{set} is the nominal reference level; V_{c1} and V_{c1} are the voltages of the reference capacitors; V_{th1} and V_{th2} are the output voltages of the IEF blocks; Q is the output of the oscillator. The image is taken from [19].

The authors of [19] described the function of IEF by means of the signal processing block scheme depicted in Figure 3.15.

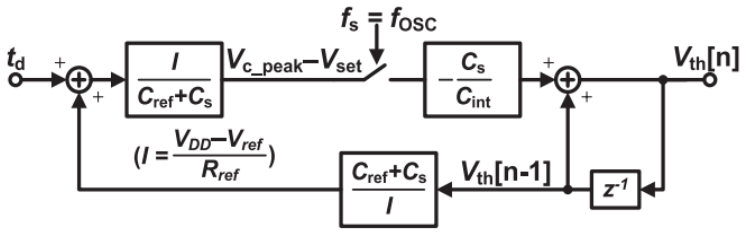

Figure 3.15 Model of IEF. t_d is the delay of the comparator with the logic circuits; C_{ref} is the reference capacitance; C_s is the sampling capacitance; C_{int} is the IEF integrator capacitance; V_{set} is the nominal reference level; V_{c_peak} is the peak voltage of the reference capacitor; V_{th} is the output voltage of the IEF block; I is the charging current. The image is taken from [19].

The model from Figure 3.15 has a transfer function of (description of the quantities can be found in the description to Figure 3.15):

$$H(z) = \frac{V_{th}(z)}{t_d(z)} = \frac{-\frac{I}{C_{ref}+C_S}\cdot\frac{C_S}{C_{int}}}{1-z^{-1}\left(1-\frac{C_S}{C_{int}}\right)} \quad (31)$$

According to the digital signal processing theory, the feedback of the system, in Figure 3.15 with the transfer function (31), can be considered stable when the following inequality is valid:

$$\left|1-\frac{C_S}{C_{int}}\right| < 1 \Rightarrow 0 < C_S < 2\cdot C_{int} \quad (32)$$

It can be clearly seen from Figure 3.14, that the system needs certain settling time to reach stable oscillation period. In [19], the relation for the number of operating cycles N was derived:

$$N > \frac{log_{10}(0.1\%)}{log_{10}\left(\left|1-\frac{C_S}{C_{int}}\right|\right)} \quad (33)$$

3.4.2 The effect of sampling capacitor

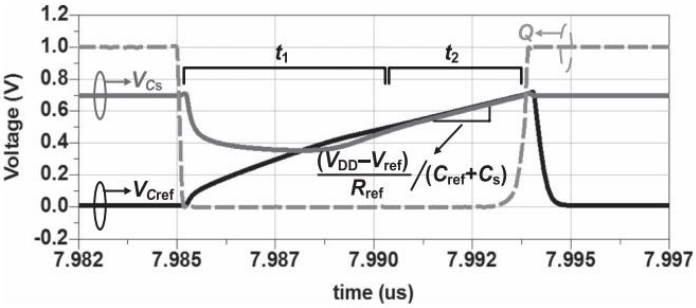

Figure 3.16 The effect of sampling capacitor in the oscillator with IEF. The image is taken from [19].

As it can be understood from Figure 3.12, the sampling capacitor participates in the integrator charging. The authors of [19] considered to use the sampling capacitor 4 times smaller than the reference one. Figure 3.16 demonstrates the effect of the sampling capacitor on the reference capacitor voltage waveform in the design presented in [19]. We see that the sampling capacitor affects the charging slope. The following relation expresses the impact of C_S on the charging period (quantities are taken from Figure 3.16):

$$t_1 + t_2 = \frac{V_{set}\cdot(C_{ref}+C_S)-V_{set}\cdot C_S}{I} = \frac{V_{set}\cdot C_{ref}}{I} \quad (34)$$

where I is the charging current.

So, C_S only affects the charging slope and has no influence on the oscillation period of the oscillator. However, there is a switch between C_S and C_{ref}, which has $4\text{-}mV$ tracking error voltage in the implementation in [19]. This error results in a frequency offset and a residual temperature coefficient of the oscillator. [19]

3.4.3 The performance

The afore-described topology was fabricated in a $90\text{-}nm$ general-purpose CMOS process by the authors of [19]. Table 3.4 presents the measured parameters of the oscillator.

Process (nm)	90
Frequency (MHz)	51.3
Power supply voltage (V)	0.8
Power consumption (μW)	18
Temperature coefficient $(ppm/°C)$	21.8 @ $-$ 20 to 100°C
Freq. variation due to power supply (%)	$\pm$0.53 @1.2 to 0.8 V
Area (mm^2)	0.027
Phase noise (dBc/Hz)	$-$83.3 @ 1 MHz offset
RMS of jitter per period (%)	0.45
FOM (dB)	192

Table 3.4 Performance summary of the oscillator in [19].

3.5 Discussion on the studied proposals

The afore-presented practical designs are described and explained separately, and their presented advantages were claimed by the authors. However, the primary goal of the research in Section 3 is to find the most appropriate topology and ideas to use them in my implementation of the oscillator according to the task. Therefore, further subsections contain detailed discussion of the presented topologies with respect to each other and theoretical insights described in Section 2.

3.5.1 Performance summary

The performance summaries of [14], [17]–[19] are summed up in the following Table 3.5.

Principle	Voltage averaging feedback	Feedforward period control	DT and SR	IEF
Reference	[14]	[17]	[18]	[19]
Process	0.18 μm CMOS	0.09 μm CMOS	0.35 μm CMOS	0.09 μm CMOS
Freq. (MHz)	14	0.1	4	51.3
P. s. voltage (V)	1.8	–	3	0.8
Power cons.	45 µW	0.28 µW	840 µW	18 µW
Variation on temp.	± 0.75 % @ -40 to 125 °C	± 0.68 % @ -40 to 90°C	53.9 ppm @ -30 to 120°C	21.8 ppm @ -30 to 120°C
Variation on p. supp.	± 0.16 % @ 1.7 to 1.9 V	± 0.82 % @ 0.725 to 0.9 V	± 0.6 % @ 2.4 to 4 V	± 0.82 % @ 0.725 to 0.9 V
Area (mm^2)	0.04	0.12	0.05	0.027
Start-up time	140 cycles	1 cycle	1 cycle	147 cycles, 3.3 µs

Table 3.5 Comparative performance summary of the designs from [14], [17]–[19].

The first thing that can be noticed, when looking at the Table 3.5, is that the power consumption of the oscillator from [17] has an extremely low value, compared to the designs with other topologies. However, the topology of the oscillator from [17] implies usage of the two-integrator oscillator with its replica (Figure 3.5), what increases the power consumption. The design from [19] is implemented in the similar technology and utilizes two-integrator oscillator too, being without any replica it consumes 64 times more power. So, the power consumption of the design from [17] is considered as outlier and is ignored.

The noise performances of the presented topologies are not compared, since the authors expressed them in different measures. Also, there is no reason to compare the area occupation of the designs, since they are implemented in different technologies.

Comparing the performance parameters in Table 3.5, we can see that the oscillator presented in [19] is the most outstanding. However, it has a disadvantage of the long start-up (3.3 µs), what is not critical for the purpose of the automotive design.

3.5.2 Comparative analysis

The analysis of the measured results, of the designs implemented by the authors, in Section 3.5.1 gives a good outlook on the possibilities of different approaches. However, the technology I have at my disposal has surely different features, and it is a big question whether the best topology from articles would have similarly good performance when implemented in I4TE. Therefore, the comparative analysis, based on the theory from Section 2 and practical considerations for automotive design is presented.

Considering the discussion in Section 2.1.3, we can estimate that the DT design proposed in [18] (Section 3.3) has greater susceptibility to the reference voltage noise compared to the other presented topologies ([14], [17], [19]), since it implements the topology of the one-integrator oscillator (Figure 2.4), as opposed to the two-integrator oscillator (but without memory bypass in [14], [17], [19], Figure 2.5). The topology with the voltage averaging feedback [14], however, is problematic in that respect as well, since it implies charging from the power supply through the resistor and the slope of the capacitor voltage waveform is enormously degraded in the vicinity of the decision point, Figure 3.3a. Moreover, the integrator employed in this design corresponds to the type 1 (Figure 2.1) from Section 2.1, and as it was discussed the tunability is degraded as well.

The problem of the comparators mismatch can be considered in the two-integrator oscillator, being utilized in [14], [17], [19]. However, the topology with IEF in [19] has dynamical compensation of the comparators influences by applying IEF separately to each comparator. Even though the principle applied in the voltage averaging feedback topology in [14] has similar concept, its reference is common to both comparators and the mismatch cancelation is absent. As for the topology with the feedforward control [17], it employs 4 comparators, so the mismatch issue is even more critical.

The noise modeling by Verhoeven [4], discussed in Section 2.2.1, allows to predict the impact of the 1/f noise on the presented topologies. Using the classification of the noise sources by the correlation to the switching action of the regenerative oscillator in [2], [4] (Section 2.2.1), we can conclude that all the presented topologies in Sections 3.1-3.4 employ current sources uncorrelated to the switching action, then the systems shape the current noise by the response depicted in Figure 2.19, and the impact of 1/f noise from the current sources is minimal. As for the reference voltage noise, the system with DT [18] has the reference correlated to the switching action, Figure 2.18, and it can be seen that 1/f noise of the voltage reference, in this case, has a great influence. The other topologies in [14], [17], [19] does not suffer from 1/f noise of the voltage reference, since their reference voltage sources are uncorrelated to the switching action (the noise shaping depicted in Figure 2.16).

Expression (14) from the Section 2.2.2 suggests that the amount of jitter is directly proportional to the number of decision points for the comparator. In that relation, the feedforward control scheme [17] has the worst prediction, since it has twice as more decision points than other presented architectures, Figure 3.6.

Section 3.1.3 described the effect of flicker (1/f) noise reduction in the oscillator with voltage averaging feedback. The authors [14] claimed that the proposed voltage averaging feedback reduces the flicker noise due to its closed-loop structure. If we consider the topology with IEF [19] (Figure 3.12), we can notice that IEF employs closed-loop structure as well, and basically IEF is a kind of distributed voltage averaging feedback for two comparators, so similar noise reduction is expected.

4 High-level modeling

Considering topologies reviewed in Section 3, it can be understood that the relaxation oscillator is a complex system employing a number of different blocks. And, it would be extremely difficult to start analyzing it directly from the lowest (transistor) level, since the general parameters and influences, considered at the high-level design, would become relative to each low-level component (e.g. transistor) used in the design, and the procedure would become extremely complicated. Therefore, a top-down approach is followed in the analysis through the high-level modeling (HLM).

4.1 The chosen topology for the implementation

The literature research in Section 3 overviews recent proposals for the integrated relaxation oscillator design and allows to utilize already tested and practically implemented approaches. The conclusion, coming from the research, postulates that the most appropriate architecture of the oscillator design (Section 3.5), according to the requirements in the task, is the relaxation oscillator with IEF, presented in [19]. Therefore, the oscillator implementation in this thesis is based on the topology from the article.

The chosen architecture is depicted in Figure 3.12 and the description of the operation can be found in Section 3.4. The following relation defines the oscillation period for the system (based on the Figure 3.12):

$$T_{OSC} = 2 \cdot \left[\frac{C_{ref} \cdot V_{th}}{(V_{DD} - V_{ref})/R_{ref}} + t_d \right] \quad (35)$$

where C_{ref} is the reference capacitance; V_{th} is the reference voltage for the comparator from the output of IEF; V_{DD} is the power supply voltage; V_{ref} is the reference voltage for the current source (op-amp1 and op-amp3 in Figure 3.12); R_{ref} is the reference resistance for the current source; t_d is the delay time of the comparator.

The charging current in (35) is defined by

$$I = (V_{DD} - V_{ref})/R_{ref} \quad (36)$$

Considering that the IEF is invoked to compensate the delay t_d after the settling, the relationship (35) can be simplified for the nominal state of operation to

$$T_{OSC} = 2 \cdot \left[\frac{C_{ref} \cdot V_{set}}{I} \right] \quad (37)$$

where V_{set} is the peak level of the charging ramp for the systems without delays, but, in the considered system, it is fed to IEF.

So, according to (37), the frequency of the oscillator is defined primarily by C_{ref}, I and V_{set}, as in the ideal case of the two-integrator sawtooth oscillator.

4.1.1 Recommendations on the design

Relationship (37) shows that frequency of the oscillator directly depends on and suffers from the variation of the quantities: C_{ref}, I and V_{set}. In the article [19], the charging current was defined as shown in (36), employing temperature compensated resistance R_{ref}. This approach allows to reduce the impact of the reference voltage and the current source variations by defining V_{set} as

$$V_{set} = V_{DD} - V_{ref} \quad (38)$$

So, substituting (38) to (36) and then to (37) gives

$$T_{OSC} = 2 \cdot R_{ref} \cdot C_{ref} \quad (39)$$

Relationship (39) implies that the frequency of the oscillator will be stable in case of temperature and process compensation of the reference resistance and capacitance. The process compensation can be performed by trimming (digital adjustment of the resistor divider, capacitor divider, or the current mirror ratio). The temperature compensation of the resistor can be performed as in [19] by utilization of the resistors with the TCs having opposite sign. Another approach is the utilization of the resistors and capacitors having negligible variations with temperature (to keep the frequency error within the 2-% range as stated in the task).

The authors in [19] discussed the influence of the sampling capacitor C_s on the charging ramp of the oscillator, Section 3.4.2, Figure 3.16. It was shown that the sampling capacitor, being 4 times smaller than the reference one (C_{ref}), does not affect the period of the oscillation, but it degrades the charging ramp in the initial phase of charging. As it can be seen from Figure 3.16, the slope of the charging ramp decreases in this process. It is clear that the higher the value of the sampling capacitor, the longer is the phase of ramp degradation and the smaller is the slope. According to the discussion in Section 2.1.3, the impact of the reference voltage noise is greater when the slope is smaller, so the sampling capacitance has to be chosen much lower than the reference capacitor value.

Section 3.4.2 brings us another design recommendation concerning the switches between capacitors C_s and C_{ref}. In [19], it was mentioned that the switch between C_S and C_{ref} has $4\text{-}mV$ tracking error voltage in their implementation and this error results in a frequency offset and a residual temperature coefficient of the oscillator. Therefore, the lowest on-resistance of this switch must be insured.

Inequality (32) suggests the stability criterion of the IEF and has to be taken into account in the practical design.

4.2 Simulation of HLM

The Spectre simulator was used to conduct the analysis by implication of the general idealized high-level blocks (i.e. operational amplifiers, comparators etc.). This section reveals the results in that respect and the effects of common negative features of the high-level blocks on the system operation.

4.2.1 The set-up

The simulation of HLM, conducted in Spectre simulator, employed only the transient analysis with default settings for convergence. The analog part of the system with IEF was assembled in schematics view of the Cadence software with ideal blocks. The logic circuits employed in the simulation circuit were the real transistor-based blocks, that are described in Section 5.1.

Figure 4.1 depicts the schematics view of the HLM simulation set-up. The set-up differs from the circuit in Figure 3.12 by the application of the SR-latch with non-inverted inputs, and hence the comparators produce logical ‘high’ to trigger the latch. In HLM set-up, the reference capacitors CREF1 and CREF2 are charged by the ideal current sources CURR1 and CURR2 correspondingly, so the reference current source is not modeled, since it is clear from (37) that it has a direct influence on the frequency stability.

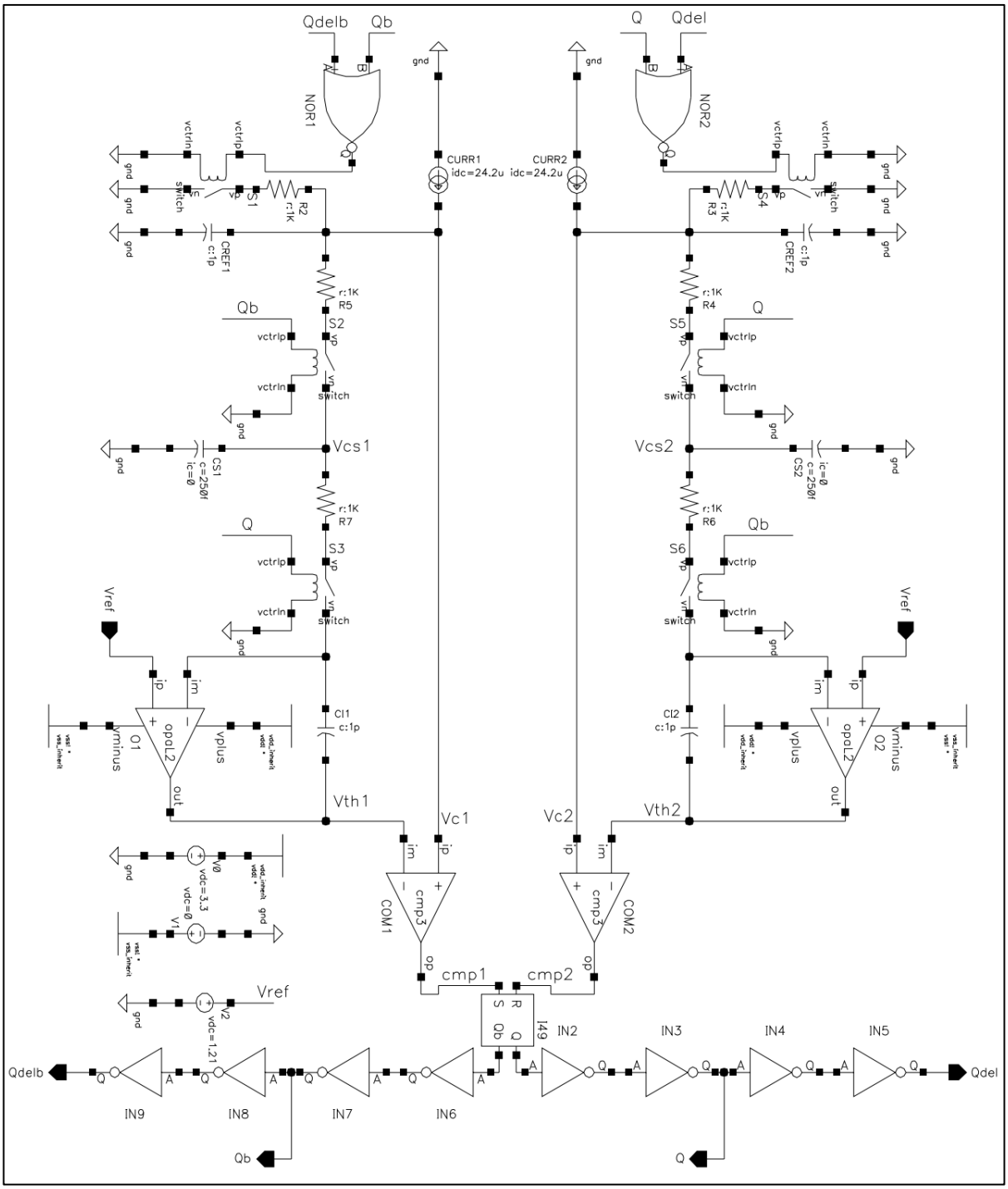

Figure 4.1 The schematics view of the HLM simulation set-up.

The op-amps O1 and O2 with the ideal capacitors CI1 and CI2 in the negative-feedback loop model the IEF blocks. The capacitors CI1 and CI2 are set to 1 pF, as well as CREF1 and CREF2. The sampling capacitors CS1 and CS2 are set to 250 fF (1/4 ratio to the reference capacitor value; same ratio as applied by the authors, who proposed IEF). So, the relationship (32) is valid and the IEF blocks are supposed to be stable. The ideal DC voltage source V2 defines the reference level Vref for the IEF blocks, it is set to 1.21 V, what corresponds, according to the task (Section 1.2), to the band-gap voltage reference that will be available on the chip. The ideal current references CURR1 and CURR2 were set to 24.2 µA to simulate 10-MHz frequency simulation (relationship (37)). The DC source V0 sets the power supply voltage, required for the logic blocks, to 3.3 V. The threshold voltages of the ideal

switches S1, S2, S3, S4, S5, S6 are set to 2 V. These switches have the resistors of 1 kOhm value connected in series to model the non-ideality of the real switches.

Parameter	Description	Value
AdB	Differential gain (dB)	70
Fc	Cut-off frequency (MHz)	1
Rin	Input differential resistance (MOhm)	1
Vos	Input offset voltage (V)	depending on the simulation
SR	Slew-rate (MV/s)	1
Kdump	Output voltage dumping factor (-)	20

Table 4.1 Parameters of the ideal op-amp block employed in HLM.

Table 4.1 shows the settings of the op-amps blocks O1 and O2. Table 4.2 presents the settings of the comparator blocks COM1 and COM2.

Parameter	Description	Value
Vhigh	Hight level voltage (V)	3.3
Vlow	Low level voltage (V)	0
tdel	Propagation delay (ns)	depending on the simulation
trise	Rising edge duration (ns)	3
tfall	Falling edge duration (ns)	3
hystp	Positive hysteresis (V)	0
hystn	Negative hysteresis (V)	0
Vos	Input offset voltage (V)	depending on the simulation

Table 4.2 Parameters of the ideal comparator block employed in HLM.

As it can be seen from scheme in Figure 4.1, the HLM did not include any start-up circuitry. The start-up was realized by the initial conditions setting: 0 V at the negative input terminals of the both op-amps; 0 V at the output terminal Q of the SR-latch; 3.3 V at the output terminal Qb of the SR-latch.

4.2.2 Verification of the concept

To verify the concept chosen for the implementation the simulation with the following settings was conducted: tdel = 20 ns, Vos = 0 V for both comparators; Vos = 3 mV for both op-amps.

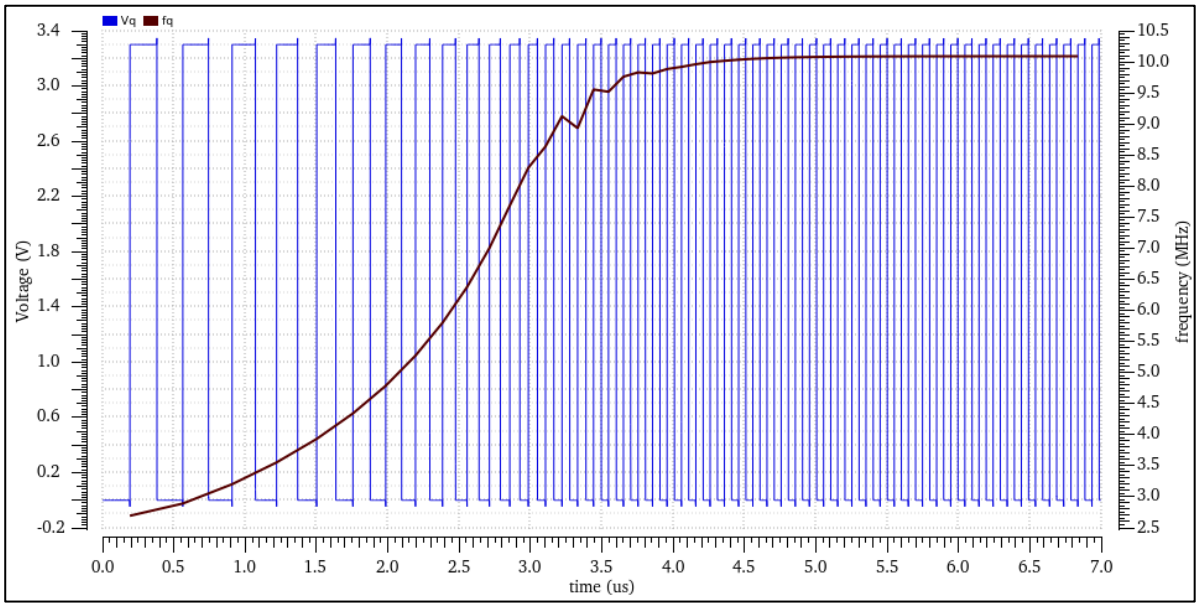

Figure 4.2 The output waveform of the oscillator (voltage of the Q terminal in Figure 4.1) – blue (Vq), and the frequency waveform of Vq – red (fq). Conditions: tdel = 20 ns, Vos = 0 V for both comparators; Vos = 3 mV for both op-amps.

The output waveform of the oscillator at the terminal Q (Figure 4.1) is presented in Figure 4.2, with its frequency over time. The output frequency of the oscillator, in fact, reaches the predefined value, overcoming the 20 ns delay of the comparators, after some settling time as was expected in the conceptual overview, Section 3.4. Even though the predefined value was 10 MHz, and it is slightly higher in the plot, this inaccuracy can be neglected, since the effect of the equivalent on-resistance of the discharging switches (resistors R2 and R3 in Figure 4.1) is not considered in the relationship (37), and the values of R2 and R3 would be significantly lower than 1 kOhm in practical design.

The compensation process is depicted in Figure 4.3. The plot contains waveforms of the charging capacitor CREF1 voltage and the reference voltage Vth1 for that capacitor, being produced by IEF. It can be seen that the reference level is adjusted dynamically, and the peak voltage of the capacitor is kept at 1.21 V after the settling.

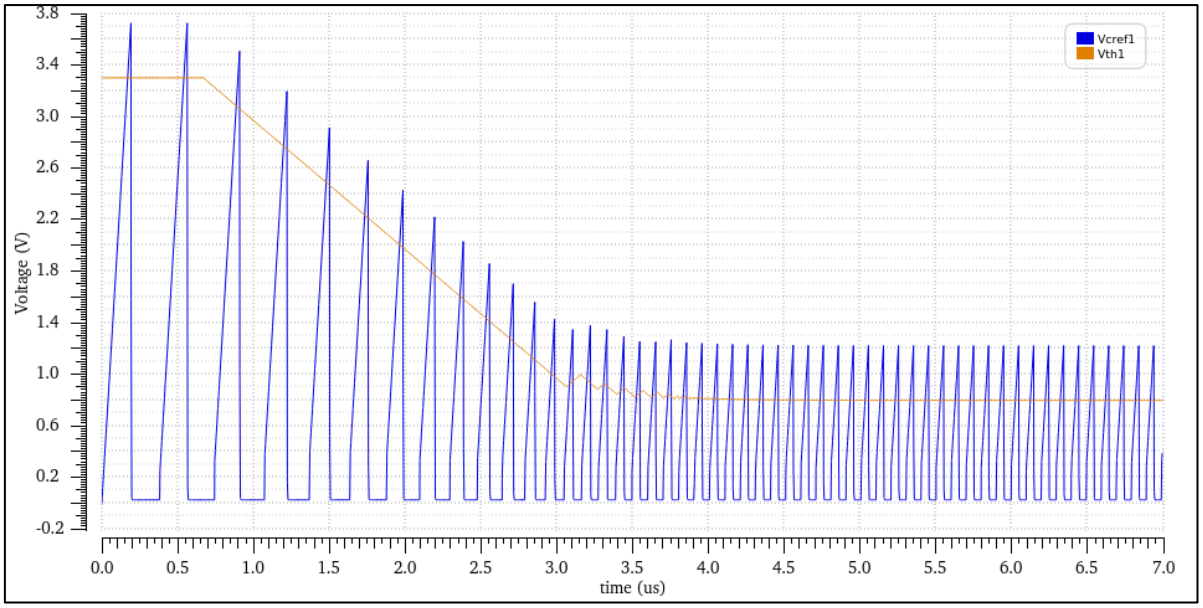

Figure 4.3 The voltage waveform of the reference capacitor CREF1 (Figure 4.1) – blue (Vcref1), and the output voltage waveform of IEF block connected to CREF1 (node Vth1 in Figure 4.1) – orange (Vth1). Conditions: tdel = 20 ns, Vos = 0 V for both comparators; Vos = 3 mV for both op-amps.

4.2.3 Impact of the switches internal resistance

The simulation for this section was conducted with the following settings: tdel = 2 ns, Vos = 3 mV for both comparators; Vos = 3 mV for both op-amps.

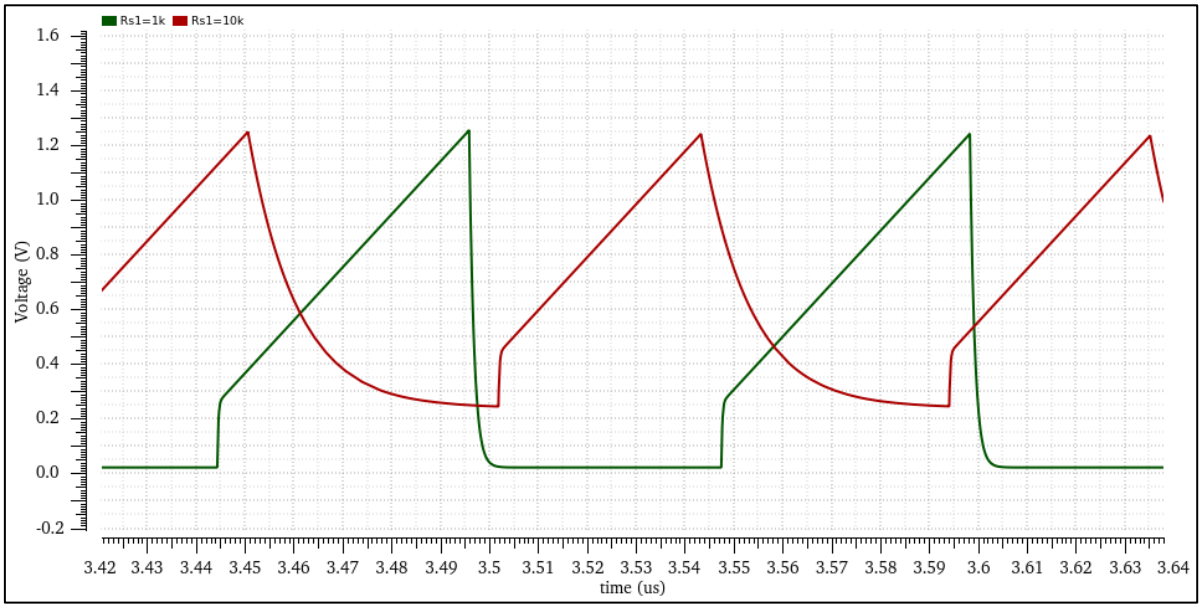

Figure 4.4 The voltage waveforms of the reference capacitor CREF1 with the resistor R2, at the discharging switch S1, of: 1 kOhm – green (Rs1 = 1k), and 10 kOhm – red (Rs1 = 10k). Conditions: tdel = 2 ns, Vos = 3 mV for both comparators; Vos = 3 mV for both op-amps.

The impact of the internal resistance (R2) of the discharging switch (S1) was inspected by comparing the voltage waveforms of the reference capacitor CREF1 depicted in Figure 4.4. High on-resistance of the switch degrades the waveform of the capacitor (red waveform in Figure 4.4) by preventing it from the complete discharge, so the initial voltage at the capacitor before every charging cycle is not at 0 V. It shortens the charging phase and increases the output frequency of the oscillator. Moreover,

considering that the internal resistance is always dependent on the temperature, this process introduces an additional factor of the frequency drift.

Also, the influence of the internal resistance (R5) of the switch (S2), which is located between the reference and sampling capacitors: CREF1 and CS1, was tested. Figure 4.5 depicts the waveforms of the voltages at the capacitors CREF1 and CS1, when the resistor R5 is set to 10 kOhm. The slope of the voltage of the capacitor CREF1 is degraded and the sampling of the peak voltage at CREF1 is not correct. It implies that the IEF function will be corrupted, resulting in the poor comparator propagation delay compensation, and again – additional frequency drift on temperature changes.

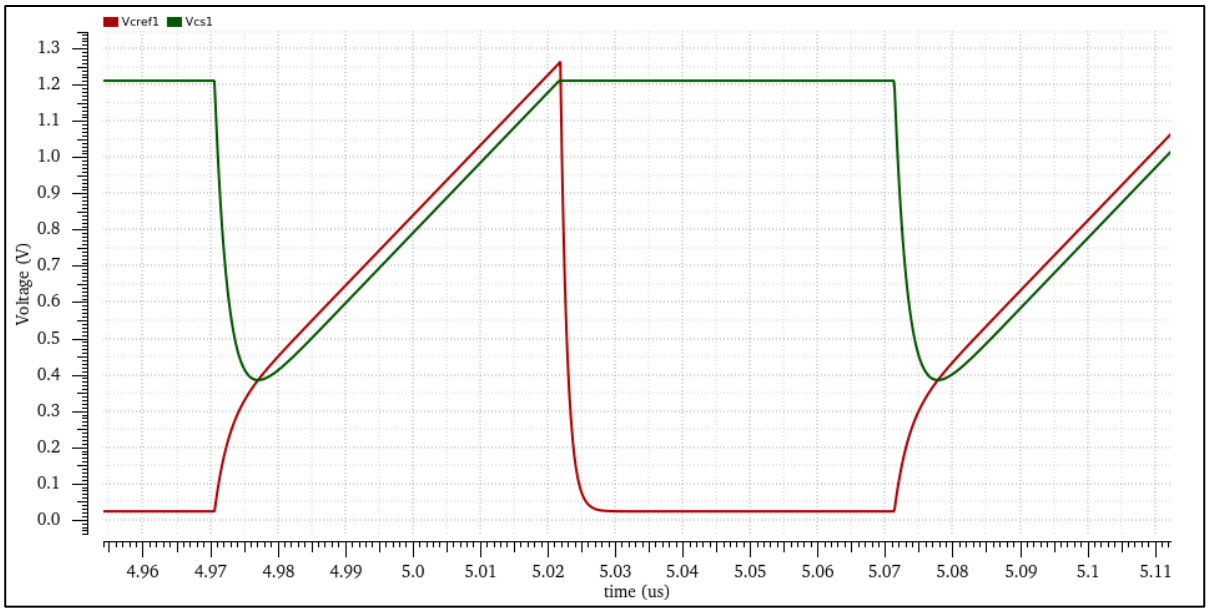

Figure 4.5 The voltage waveforms of the reference capacitor CREF1 – red (Vcref1), and the sampling capacitor – green (Vcs1), when the internal resistance (R5) of the switch (S2) between these resistors is set to 10 kOhm. Conditions: tdel = 2 ns, Vos = 3 mV for both comparators; Vos = 3 mV for both op-amps.

4.2.4 Impact of the comparators matched and mismatched offsets

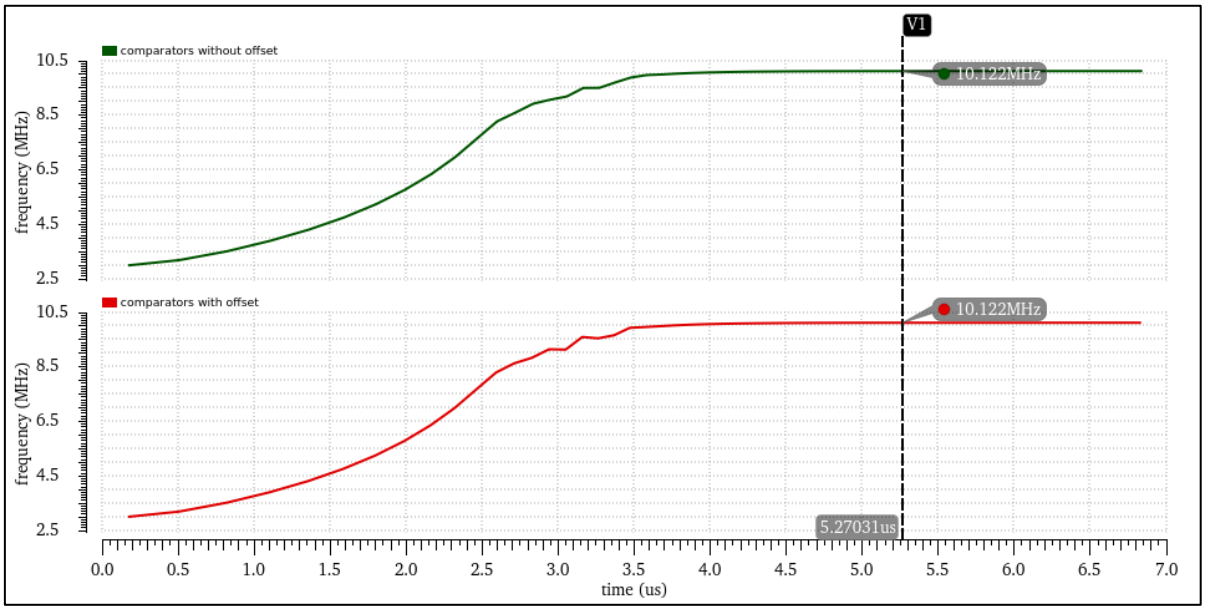

Figure 4.6 The oscillator frequency over time for the case of comparators without offset – green, and with offset – red. Conditions: (1st run) – tdel = 1 ns and Vos = 0 V for both comparators, Vos = 0 V for both op-amps; (2nd run) – tdel = 1 ns and Vos = 10 mV for both comparators, Vos = 0 V for both op-amps.

The function of IEF was inspected on the matter of cancelation of the matched comparators offsets. The results are shown in Figure 4.6. After the settling, the oscillator frequency of the system with comparators offsets is equal to the frequency of the system without offsets. The comparator offset is compensated, since, given the same charging slope of the reference capacitors every cycle, it can be considered as a part of the propagation delay.

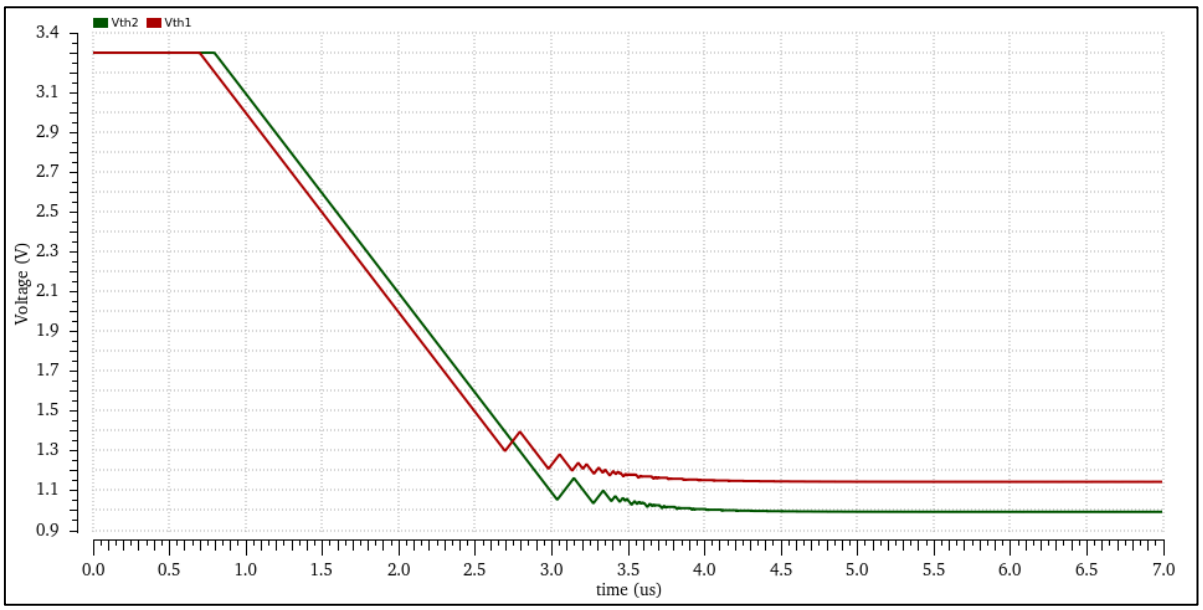

Figure 4.7 The voltage waveforms (Vth1 – red and Vth2 – green) from the outputs of the IEF blocks of two different branches of the system. Conditions: tdel = 2 ns, Vos = 1 mV for the comparator COM1; tdel = 10 ns, Vos = 5 mV for the comparator COM2; Vos = 3 mV for both op-amps.

The mismatch between comparators was modeled by introducing different propagation delays and offsets to the blocks COM1 and COM2. The adjustments of the reference voltage levels by the IEF

blocks is shown in Figure 4.7. Figure 4.8 demonstrates the reference voltage levels and the charging capacitors voltage waveforms after the system is settled. It can be seen that the capacitors waveforms are identical and have their peaks at 1.21 V. So, the IEF effectively handles comparators mismatch by the reference voltage adjustment.

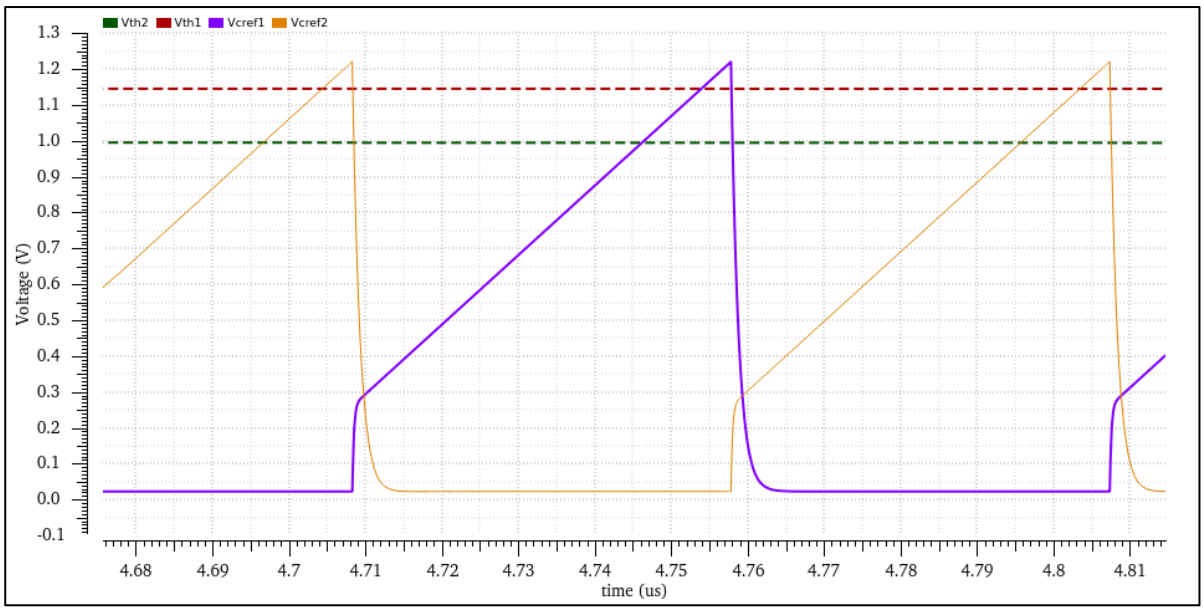

Figure 4.8 The voltage waveforms (Vth1 – red and Vth2 – green) from the outputs of the IEF blocks of two different branches of the system, and sampling capacitors CREF1 – purple (Vcref1), CREF2 – orange (Vcref2). Conditions: tdel = 2 ns, Vos = 1 mV for the comparator COM1; tdel = 10 ns, Vos = 5 mV for the comparator COM2; Vos = 3 mV for both op-amps.

4.2.5 Impact of the mismatch between the operational amplifiers

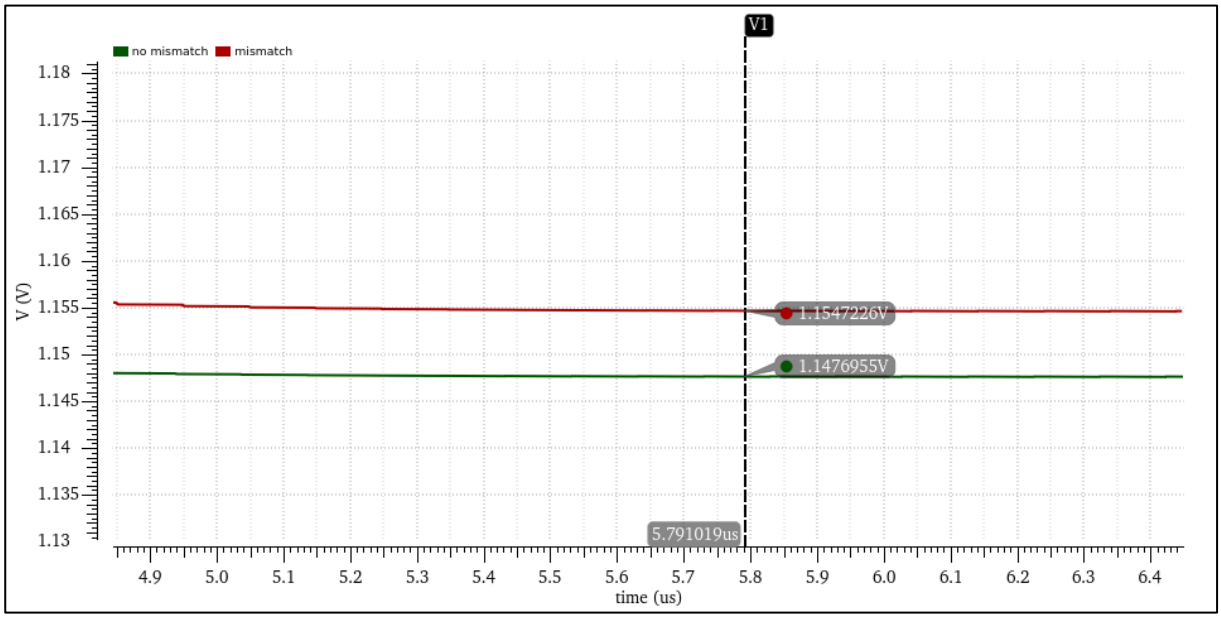

Figure 4.9 The voltage waveforms of Vth2 when the op-amps are matched – green, and mismatched – red, after the settling. Conditions: tdel = 2 ns, Vos = 3 mV for both comparators; Vos = 10 mV (3 mV, when simulating matched op-amps) for OA2 and Vos = 3 mV for OA1.

As follows from the simulations depicted in Figure 4.9 and Figure 4.10, when the operational amplifiers in the IEF blocks have the mismatched offset voltages, this mismatch directly transfers to the difference of reference voltages in two branches of the oscillator (Vth1 would correspond to Vth2, when the op-amps are matched). It leads to the corruption of the oscillation duty cycle, Figure 4.10. The simulation in Figure 4.9, also, shows that even if the op-amps are matched, their offset voltages degrade the adjustment of the correct compensated reference voltages for the comparators. So, the op-amp offset voltages have to be minimized in the practical implementation.

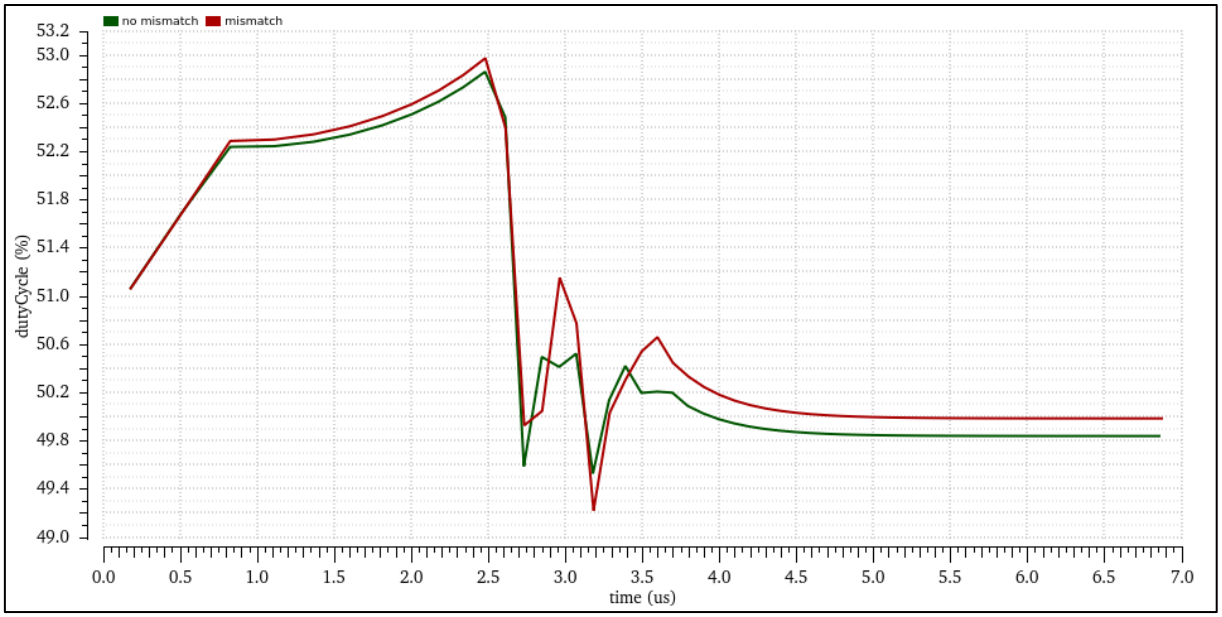

Figure 4.10 Duty cycle of the oscillator output when the op-amps are matched – green, and mismatched – red. Conditions: tdel = 2 ns, Vos = 3 mV for both comparators; Vos = 10 mV (3 mV, when simulating matched op-amps) for OA2 and Vos = 3 mV for OA1.

4.2.6 HLM summary

The topology utilizing the IEF technique was chosen, based on the literature research, to implement the system corresponding to the task. For that matter, the design recommendations were postulated in Section 4.1.1.

The HLM simulations showed that the application of IEF is, in fact, a valid approach to compensate the influence of the comparator offset voltage and propagation delay in basic two-integrator sawtooth oscillator. Moreover, the simulations proved that the chosen topology is able to cope with the mismatches of the comparators, successfully compensating them.

However, it was noted that the offset voltage between the operational amplifiers impacts the reference levels fed to the comparators and caused the corruption of the duty cycle. Also, the HLM simulations uncovered the negative consequences of the internal resistance of switches on charging ramp of the reference capacitor and sampling precision.

5 Block design

The implemented blocks correspond to the original proposal of the authors of IEF approach [19], but with slight differences.

For example, it was decided that the operational amplifier of the same topology will be used all over the system: in the current reference source, and in integrators of IEF blocks. However, the SR-latch was chosen with non-inverted inputs to have the comparators regenerating to the 'high' state in the point of decision. Because during the simulations of the comparator block, it was found that the chosen architecture has smaller propagation delay, when switching to the 'high' state.

The simulations, shown in this section, were performed in Spectre simulator. Their goal is to show the prediction of the most important parameters of the designed blocks and their influence on the system performance, according to the HLM, Section 4. The designed blocks parameters ignored in this consideration were set to the standard reasonable values (e.g. DC amplification of the op-amp, output and input voltage range of the op-amp etc.).

There were only 2 types of transistors employed in the design: PMOS and NMOS from the same family.

The designing procedure included the following consecutive steps: choosing the appropriate topology, rough hand calculation of the components parameters (i.e. MOSFETs dimensions, resistors values, capacitors values etc.) for optimal performance, adjustments of the components parameters based on the simulations.

The process variations were simulated via inclusion of the corners for the considered technology. The general description of the considered corners is shown in the following Table 5.1.

Component type	**Corners employed in the simulations**
NMOS and PMOS	both Slow, both Fast, Fast NMOS – Slow PMOS, Fast PMOS – Slow NMOS, voltage output high, voltage output low
Resistor	highest value, lowest value
Capacitor	highest value, lowest value

Table 5.1 Overview of the process corners employed in the simulations.

5.1 Logic devices

The considered design requires just several logic blocks: an inverter, a NOR gate and a SR-latch.

The designs of the inverter and the NOR gate were already available from the libraries of the company ON Semiconductor. But, basically, they were implemented in the most classical way.

The SR-latch was built using the available NOR gates, Figure 5.1.

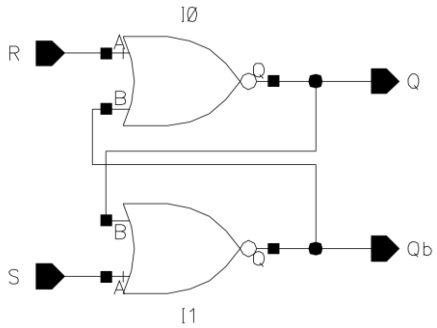

Figure 5.1. The schematic view of the implemented SR-latch.

The simulation was conducted just on the designed SR-latch to estimate roughly its slew rate. Figure 5.2 depicts the result and it can be clearly seen that there is no reason to worry about the delays caused be the latch, since it does not drive any loads. The same conclusion can be done in respect to the inverter and the NOR gate, since their operation speed is faster than the speed of the SR-latch.

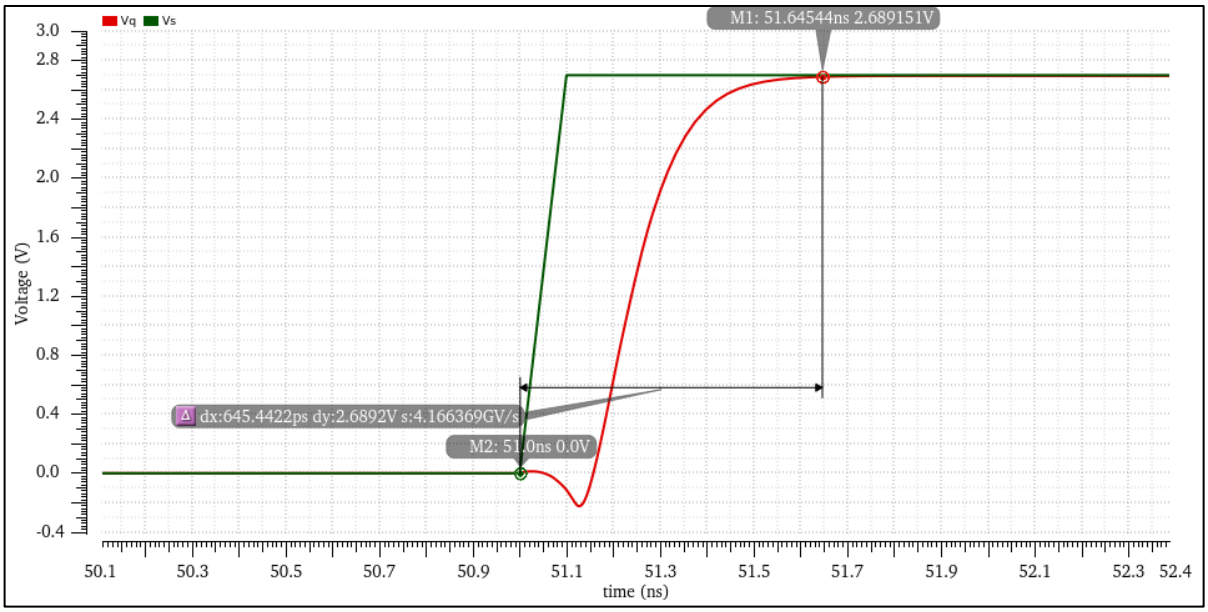

Figure 5.2. Slew rate of the SR-latch in nominal conditions and power supply voltage of 2.7 V.

All the logic devices were put in one block to spare some space on the canvas, when assembling the whole system. Further in the thesis the logical block will correspond to the schematic in Figure 5.3. When compared to the HLM schematic in Figure 4.1, it is clear what functions are presumed in the block in Figure 5.3. However, there is the slight modification: transistor switches M30 and M31, whose function is the start-up (the same nodes were pushed to the same voltages in HLM simulation by settings of the initial conditions).

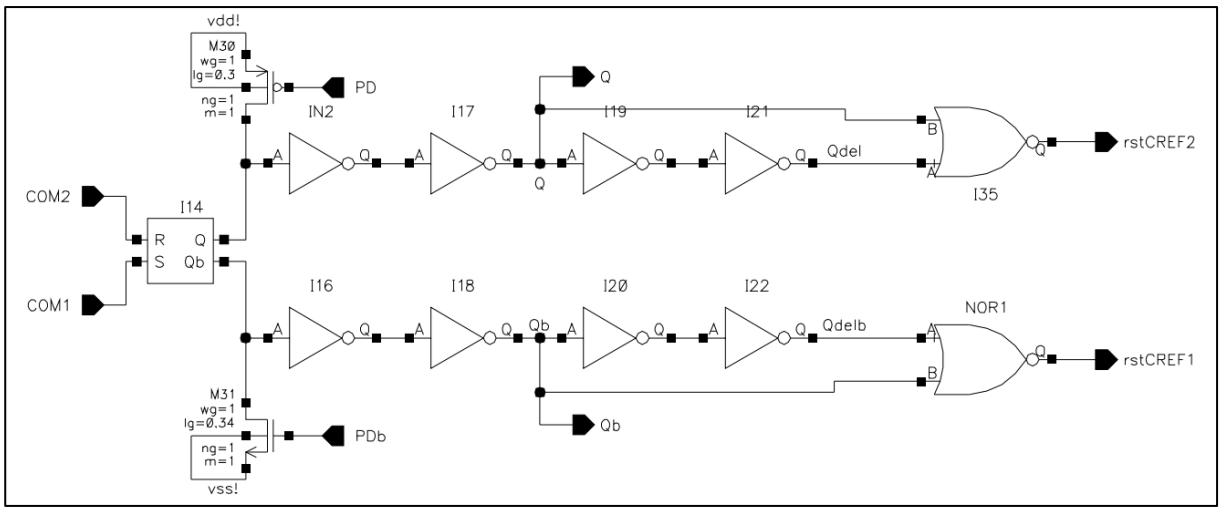

Figure 5.3. Logic block of the implemented design.

5.2 Operational amplifier

As it was mentioned, the same op-amp block is supposed to be replicated all over the design. In opposite to the original design in Figure 3.12, only one op-amp provides the charging current reference source, which is later replicated for both reference capacitors by the current mirror. The other two op-amps are employed in the IEF blocks.

In order to simplify the design procedure, the folded-cascode topology was chosen, Figure 5.4. The reason is that the folded-cascode op-amp has its dominant pole, defined by its output impedance, so the stability compensation is done by the load capacitance C_L (Figure 5.4) without any Miller effects and right-half-plane zeroes.

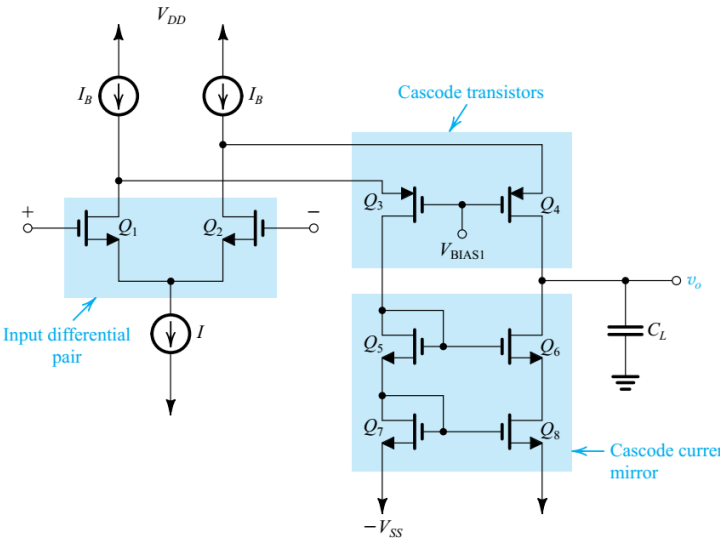

Figure 5.4. Principle circuit of the folded-cascode op-amp. The image is taken from [20].

Figure 5.5 depicts the designed op-amp. It was decided that the amplifier will be biased by typical 5 µA from the PMOS. As it can be seen, the cascode transistors Cosn1 and Cosn2 are biased by the voltage drop on the resistor R0 plus saturation voltage of Mn1. It was decided to implement the cascoded current mirror at the output stage by the wide-swing topology to increase the output voltage range, while at the same time utilize benefits of the ordinary cascode (as e.g. in Figure 5.4), since, as it was

estimated during HLM that the op-amp offset is critical in the IEF. This cascode was biased by the diode-connected transistor Bp0 with long channel.

The circuit, also, has power down switches M0, PDn0, PDp1, PDp2 and PDp3, which assure the shutdown of the current mirrors in the circuit.

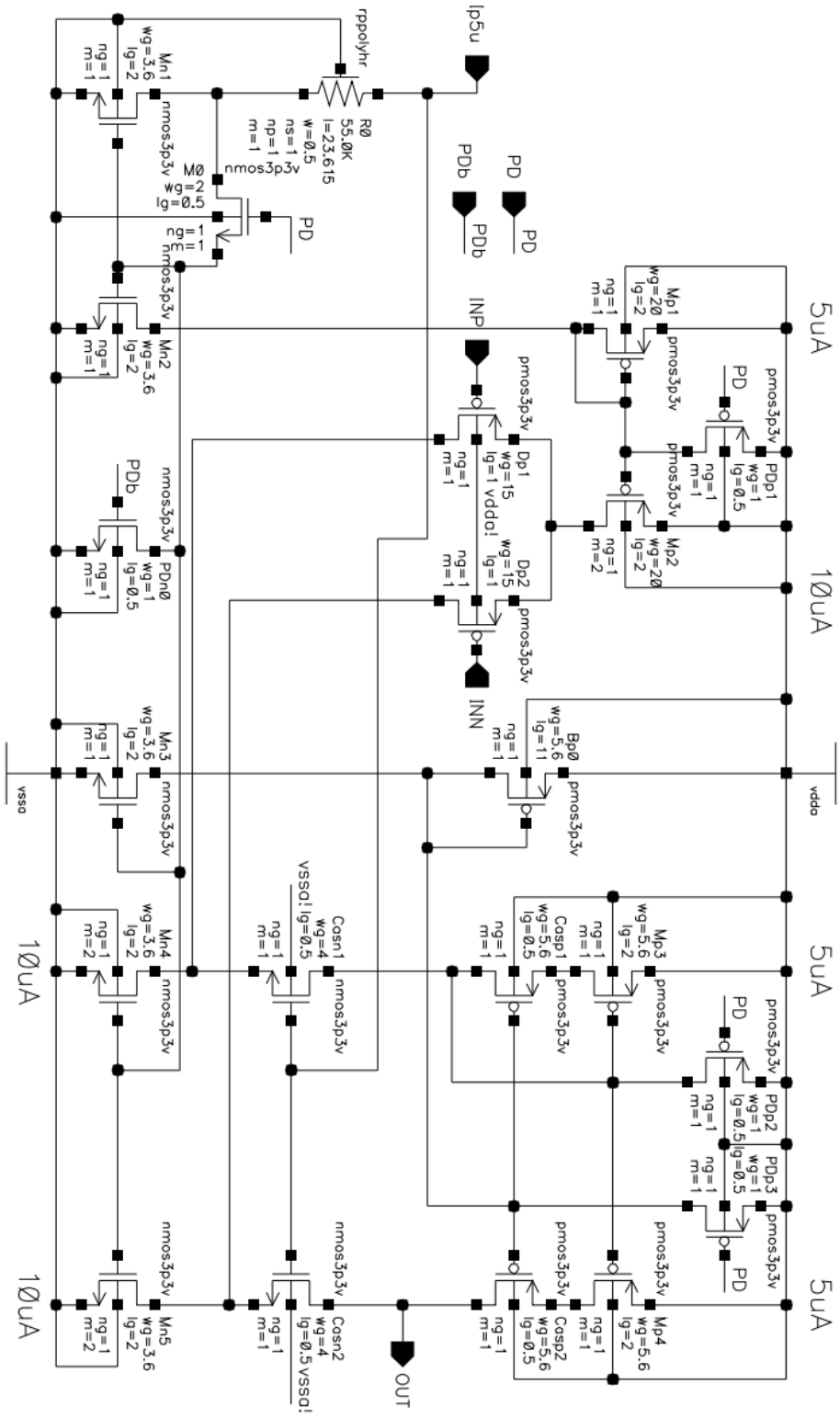

Figure 5.5 The designed op-amp block. The dimensions of the components are depicted (for NMOS and PMOS: wg – channel width, lg – channel length, m – number of transistors in parallel, ng – number of gate-fingers).

5.2.1 Offset voltage

As it was mentioned and uncovered in Section 4.2.5, the op-amp offset directly affects the reference level at the output of IEF, so the primary goal in designing the op-amp was to reduce the offset voltage to the minimum, which is caused by the currents mismatch in the branches of the circuit. So, it was insured that all the transistors in current mirrors are well-saturated and cascode transistors are sufficiently biased. Also, the channel lengths of the transistors in current mirrors were set to sufficiently high value.

The set-up for the offset simulation is shown in Figure 5.6. The simulation was performed by DC analysis in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V (at DC voltage source V1, Figure 5.6). The biasing current was fed to the op-amp by the current-controlled current source F0, which replicates the current flowing through the DC voltage source V2 and the Rppoly resistor R0, what is done to model the biasing current variations with process variations. The process variations were considered by the corner analysis.

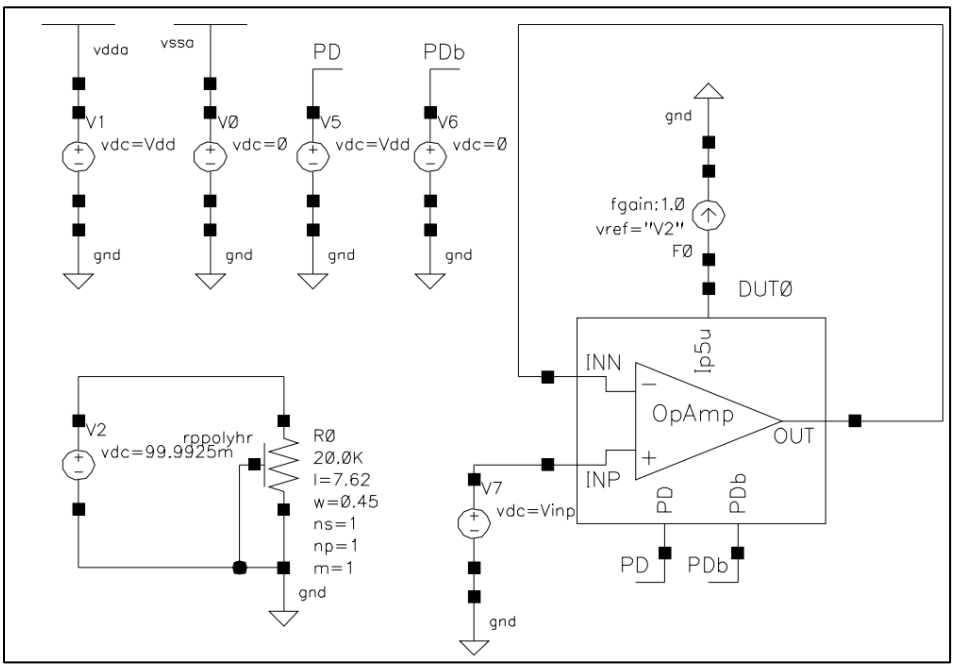

Figure 5.6 Simulation set-up for the op-amp offset estimation.

The offset voltage was taken as a difference of voltages between the node at the output of the op-amp and at the positive terminal. And, the result for the worst corner was 343.2 µV, what can be considered as a negligible value.

However, the corner analysis applies the process variation model on all the components simultaneously and the effects of mismatches cannot be seen. Therefore, the Monte Carlo analysis was undertaken for the same corner, temperature and power supply variations. The results are in Figure 5.7. It can be estimated that for the confidence interval of 5 standard deviations, commonly applied for automotive design, the op-amp offset voltage can reach up to 13 mV.

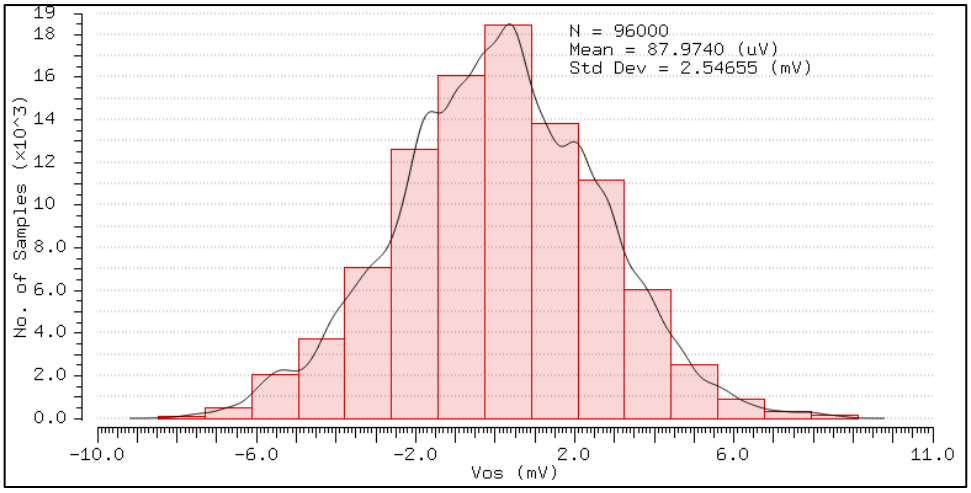

Figure 5.7 The statistics of the op-amp offset voltage simulated by the Monte Carlo analysis over process (all the considered corners), temperature (-40°C and 175°C), power supply (2.7 and 3.6 V) and mismatch variations.

Also, it has to be noted, this kind of offset simulation is also dependent on the op-amp gain, so it was adjusted in the design as well.

5.3 Comparator

As it was mentioned and analyzed in Section 4.2, the comparator negative features like offset and propagation delay are well compensated by the IEF. But, looking at the waveform in Figure 3.16, we can conclude that the reference capacitor should be switched during the time interval t_2, when its charging ramp is linear. Since in the interval t_1 of the charge exchange with the sampling capacitor, the charging ramp slope is degraded, what increases susceptibility to noise, as it was mentioned earlier in the thesis in Section 2.1.3. It implies that the propagation delay of the comparator should be smaller than t_2.

On the other hand, according to the Gierkink's jitter derivation in Section 2.2.2, the faster the comparator is, the greater its noise band is. So, the comparator speed has to be optimized accordingly.

5.3.1 The topology

The topology used for the comparator realization is presented in Figure 5.8. It is based on the classical two stage amplifier with the buffer at the output stage to improve the speed. The systematic offset is compensated by the adjustment of transistors P0 and Mp1, Mp2 to have the same saturation voltage. The "power down" switch M19 ensures logical "0" at the output of the comparator, when power down is active (PDb = "1"). The comparator requires 5-uA biasing current from PMOS, as the op-amp.

The comparator slew rate is affected by the currents flowing through the branches and by dimensions of the transistors Mp1, Mp2, P0, since the node at the gate of P0 defines the dominant pole of the circuit. At the same time, the non-systematic offset of the system is dependent on the dimensions of the same transistors: the smaller the dimensions, the higher the offset. Since both the offset voltage and the slew rate affect the overall propagation delay of the comparator in the considered application, the dimensions of Mp1, Mp2 and P0 were optimized, using the simulation in the following Section 5.3.2.

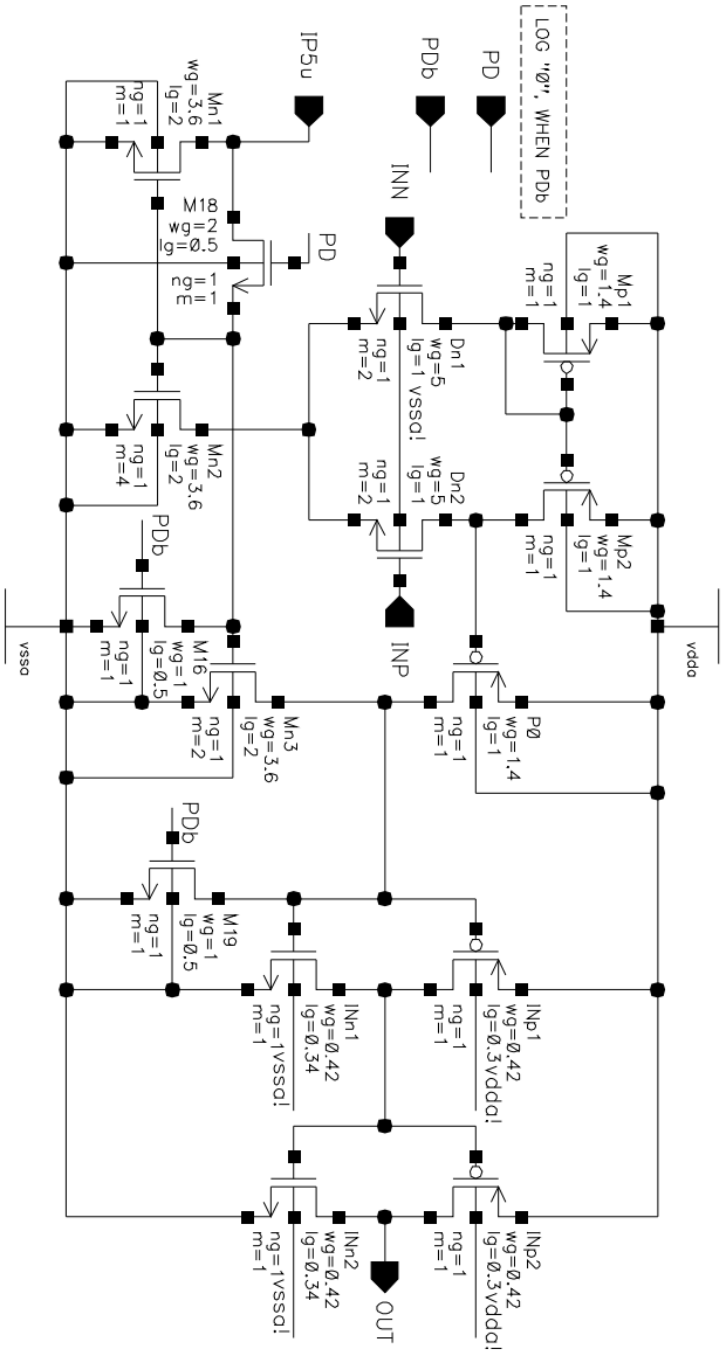

Figure 5.8. Schematic of the implemented comparator. Power down sets the initial value of the comparator to logical 'low'.

5.3.2 The simulation

Figure 5.9 presents the set-up to simulate the propagation delay of the designed comparator. The simulation was performed in transient analysis with the default settings on accuracy and convergence, in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters. The variation of the biasing current was modeled by the Rppoly resistor as in Figure 5.6. The output terminal of the comparator was connected to the SR-latch to model the real load capacitance, the comparator encounters in the complete system. The negative terminal of the comparator was fed by the reference voltage 1.21 (as in the task), the positive one was fed by the voltage source V4 that modeled the ideal charging ramp of the reference

capacitor at 10 MHz operation. The delay was determined as a time interval between the point, where the voltage ramp from V4 reaches the reference level of 1.21 V, and the point, where the output of the comparator reaches a half of the power supply voltage.

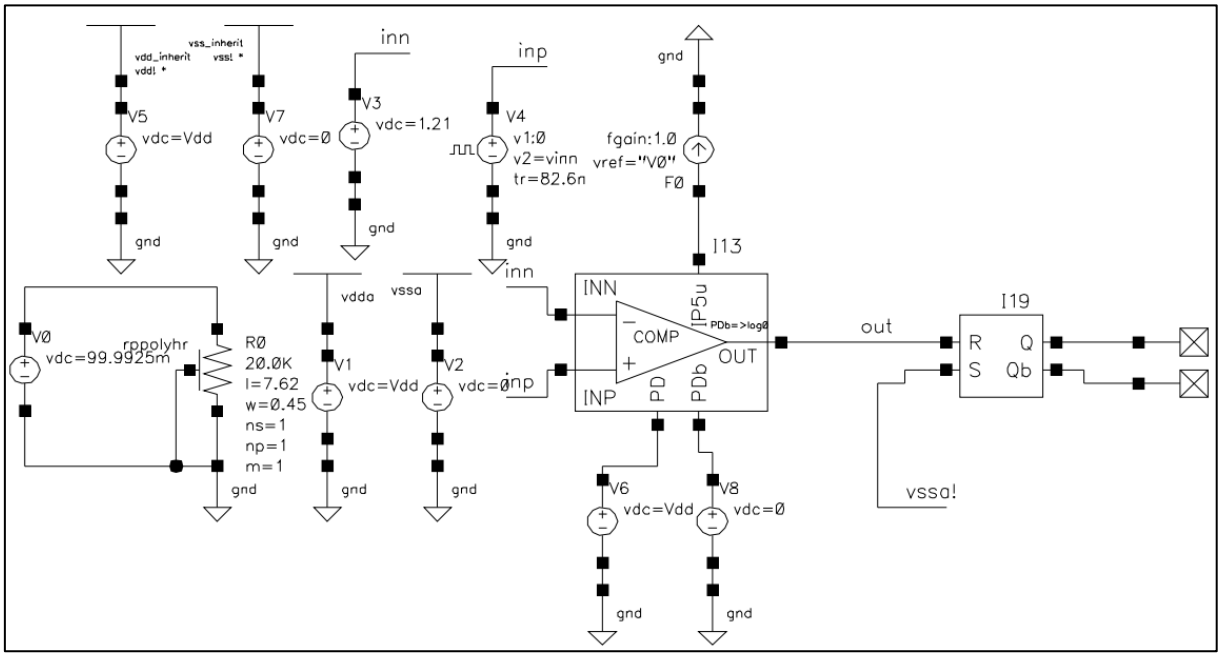

Figure 5.9. The simulation set-up for the comparator. The input is fed with a voltage ramp of the same slope as expected in the complete system.

Figure 5.10 depicts the result of 7 ns and the waveforms from the voltage source V4 and output of the comparator for the worst corner (capacitors: lowest value, MOSFETs: slow, resistors: highest value, temperature: 175 °C, power supply voltage: 2.7 V). The result is acceptable, since the charging ramp of the reference capacitor in 10-MHz system lasts 50 ns.

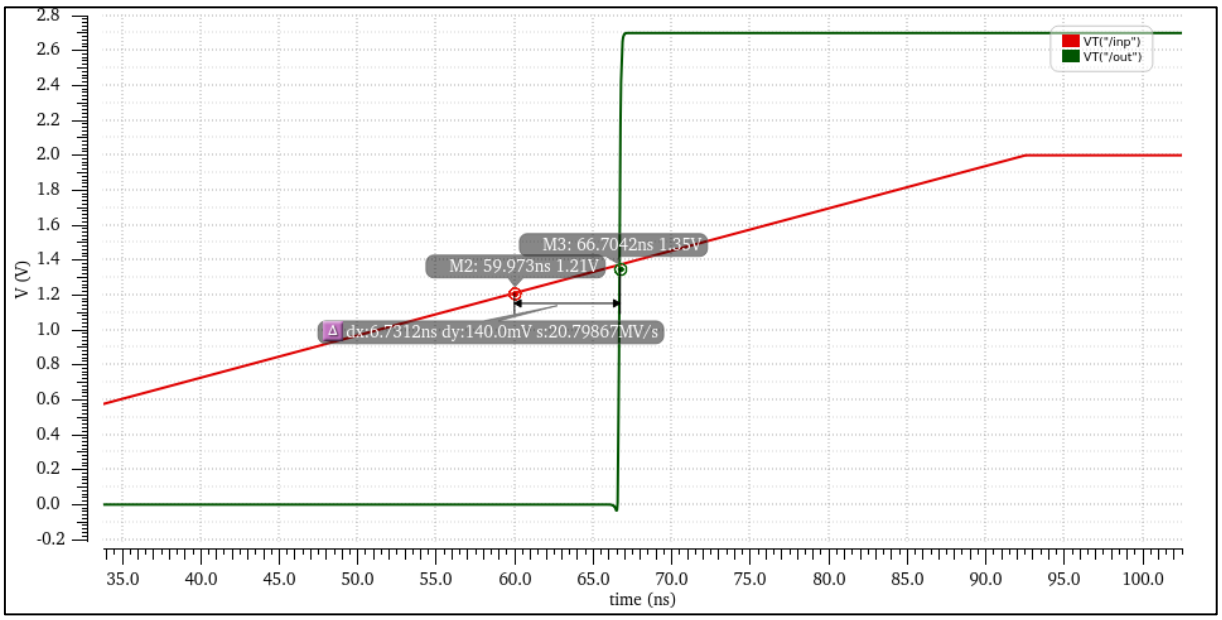

Figure 5.10. Simulation waveform of the comparator for the worst corner. V4 voltage waveform (Figure 5.9) – red; comparator output voltage waveform – green. The resulting propagation delay is approximately 7 ns.

5.4 Charging current source

Figure 5.11 presents the designed current source. It is implemented by the afore-mentioned operational amplifier, that senses voltage drop of the R1 resistor and keeps it at the reference level (of 1.21 V) by setting the gate voltage of the PMOS M1. The topology differs from the more common approach, e.g. depicted in Figure 3.12, where the op-amp keeps the voltage at the resistor through the voltage follower. The reason is that when the more traditional approach was tested, it turned out that at the lowest value of power supply voltage of 2.7 V the op-amp upper output voltage limit was too small to keep the NMOS, connected as a voltage-follower, in saturation region, or the enormously huge NMOS had to be used. That problem was caused by the fact that 1.21 V at the source of NMOS caused too severe body effect.

The ideal resistor R1 is supposed to be replaced by the trimmed resistor divider with small temperature coefficient.

The PMOS transistors at the output have the dimensions to reduce mismatch (caused by λ-effect) and to produce 25-µA reference current, when the reference voltage of 1.21 V is applied. However, these transistors will be trimmed as well to enhance the trimming range of the oscillator output frequency.

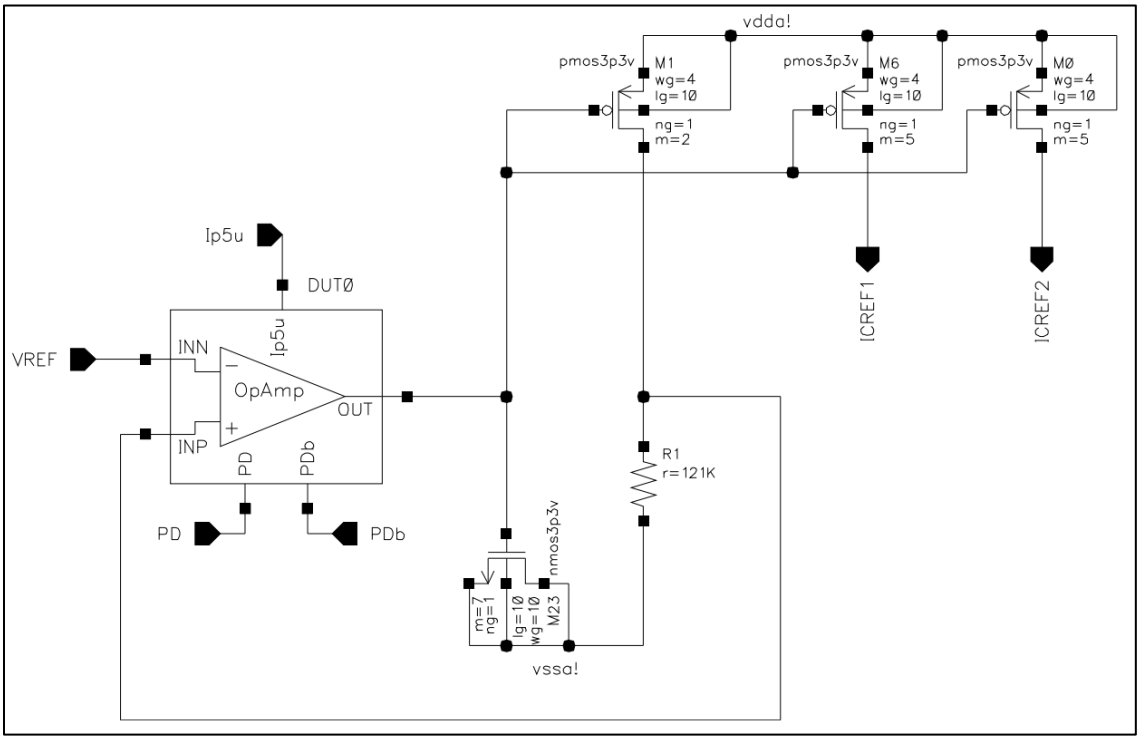

Figure 5.11 The schematic of the implemented current reference. The NMOS M23 is a compensation capacitor. The resistor R1 is ideal, since trimming is expected.

5.4.1 The simulation

Figure 5.13 depicts the set-up of the designed current source simulation. The DC and stability analysis (stb) from Spectre simulator were employed in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters. Voltage source V7 is a current probe for the stb analysis. The op-amp is biased by the modeled current source, the same way as in previously described simulations. The DC simulation was used to estimate the dependence of the output current on process and temperature variations, when the ideal (or the trimmed resistor with negligible TC) resistor R1 is utilized.

Figure 5.12 depicts the result of the stb analysis of the designed current source for the worst corner (capacitors: lowest value, MOSFETs: fast nmos – slow pmos, resistors: lowest value, temperature: -40 ^{o}C, power supply voltage: 2.7 V). It can be seen that the phase margin exceeds 60^{o} (the system is considered to be stable).

DC simulations showed that the output current varies in the range of 25.03-25.05 µA (over all the corners, temperature, power supply voltage), so its error is negligible.

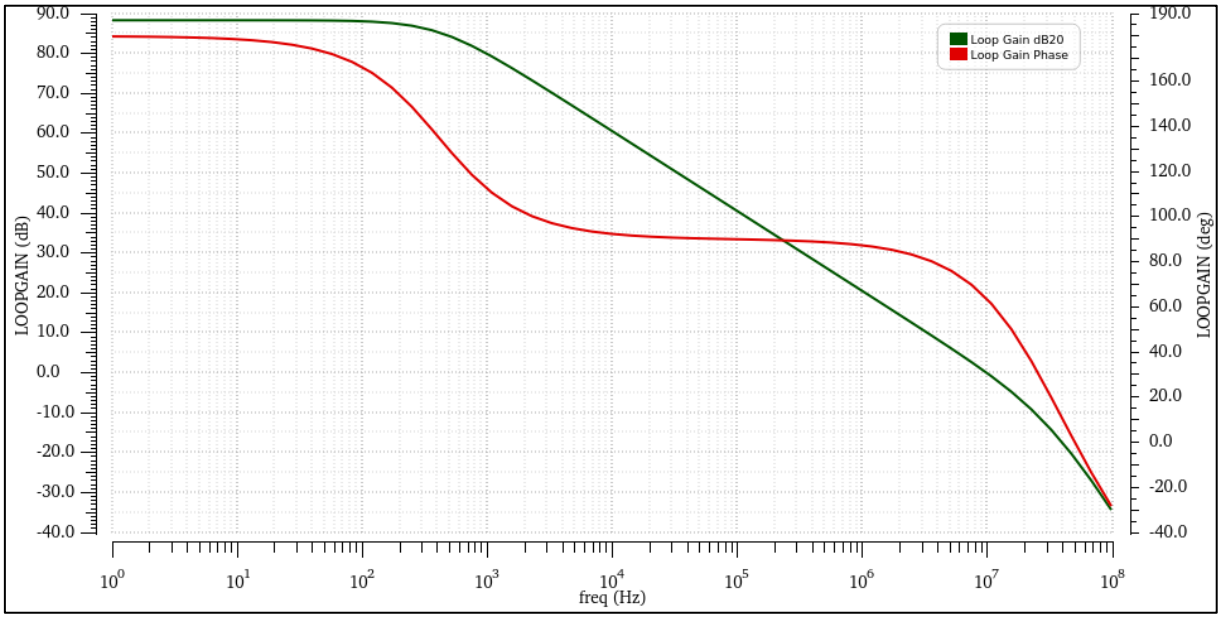

Figure 5.12 The worst corner simulation result, of the designed current source, with the phase margin of approximately 60^{o}.

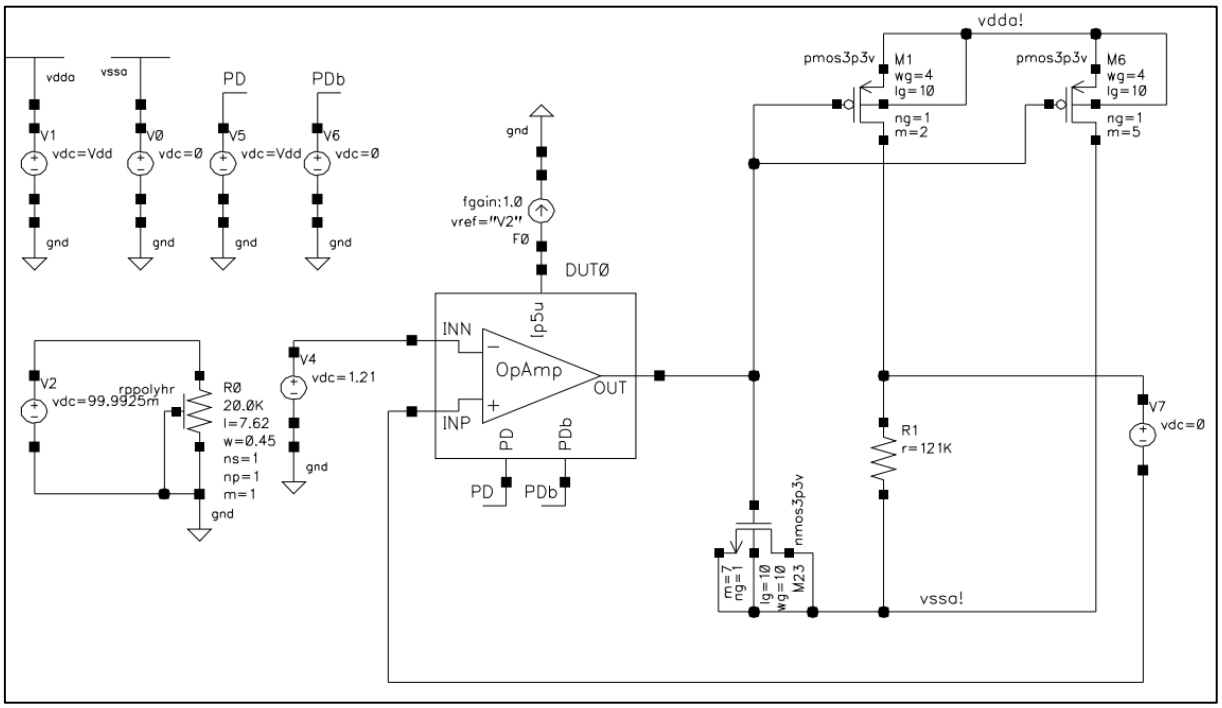

Figure 5.13 Simulation set-up to estimate frequency stability and precision of the designed current source.

5.5 The IEF block

Figure 5.14 presents the IEF block used in the design. The capacitor in feedback is implemented by the NMOS transistor. The capacitance of the transistor is not stable over voltage and temperature variations, but the capacitor in the feedback of IEF just has to integrate the voltage error of the reference capacitors. And, its inaccuracy has an influence only on the settling time, (33), and on the IEF system stability, (32). Given that the condition (32) is satisfied and the settling time is not a critical issue, it is presumed that the inaccuracy of the feedback capacitor has no impact on the system performance and can be ignored.

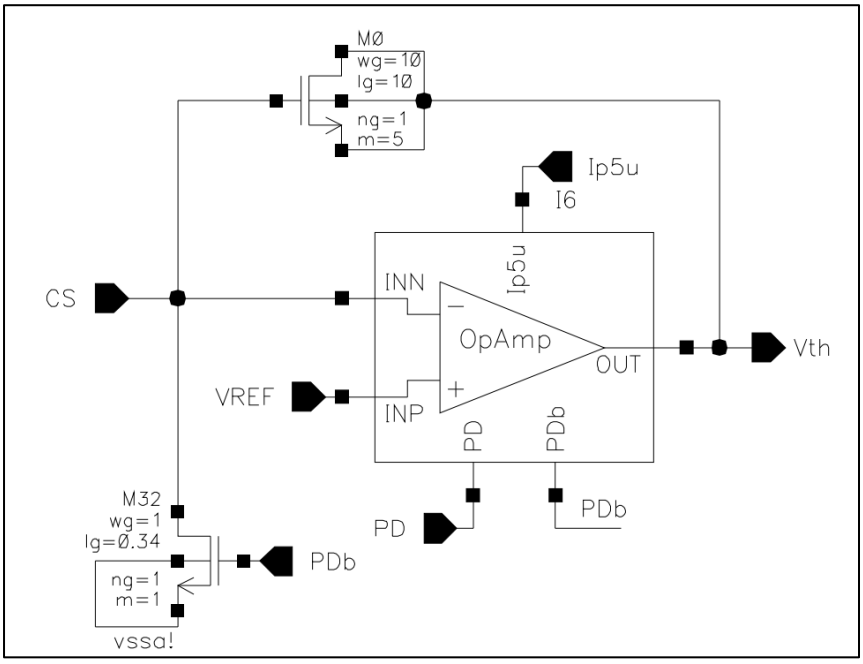

Figure 5.14 Implemented IEF block. The op-amp is taken from Section 5.2, NMOS M0 is feedback capacitor, NMOS M32 is a power down switch for the initial state setting. Pin CS is a connection to the sampling capacitor through the switch, pin VREF is a connection to the voltage reference defining the charging capacitors peak voltage, pin Vth is an output of the IEF block defining the reference voltage for the comparator.

5.5.1 Stability of IEF

Figure 5.15 presents the set-up for the IEF block stability simulation (stb analysis) in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters. Voltage source V3 is a current probe for the stb analysis. An ideal resistor R4 having 100 MOhm was added to close the DC feedback loop for the stb analysis. The op-amp is biased by the modeled current source via Rppoly resistor.

NMOS M1 is a sampling capacitor and an ideal resistor R1 models the on-resistance of the switch between the sampling capacitor and the IEF block.

The simulation results showed that the worst corner suggests phase margin of 89 °, so the systems is stable.

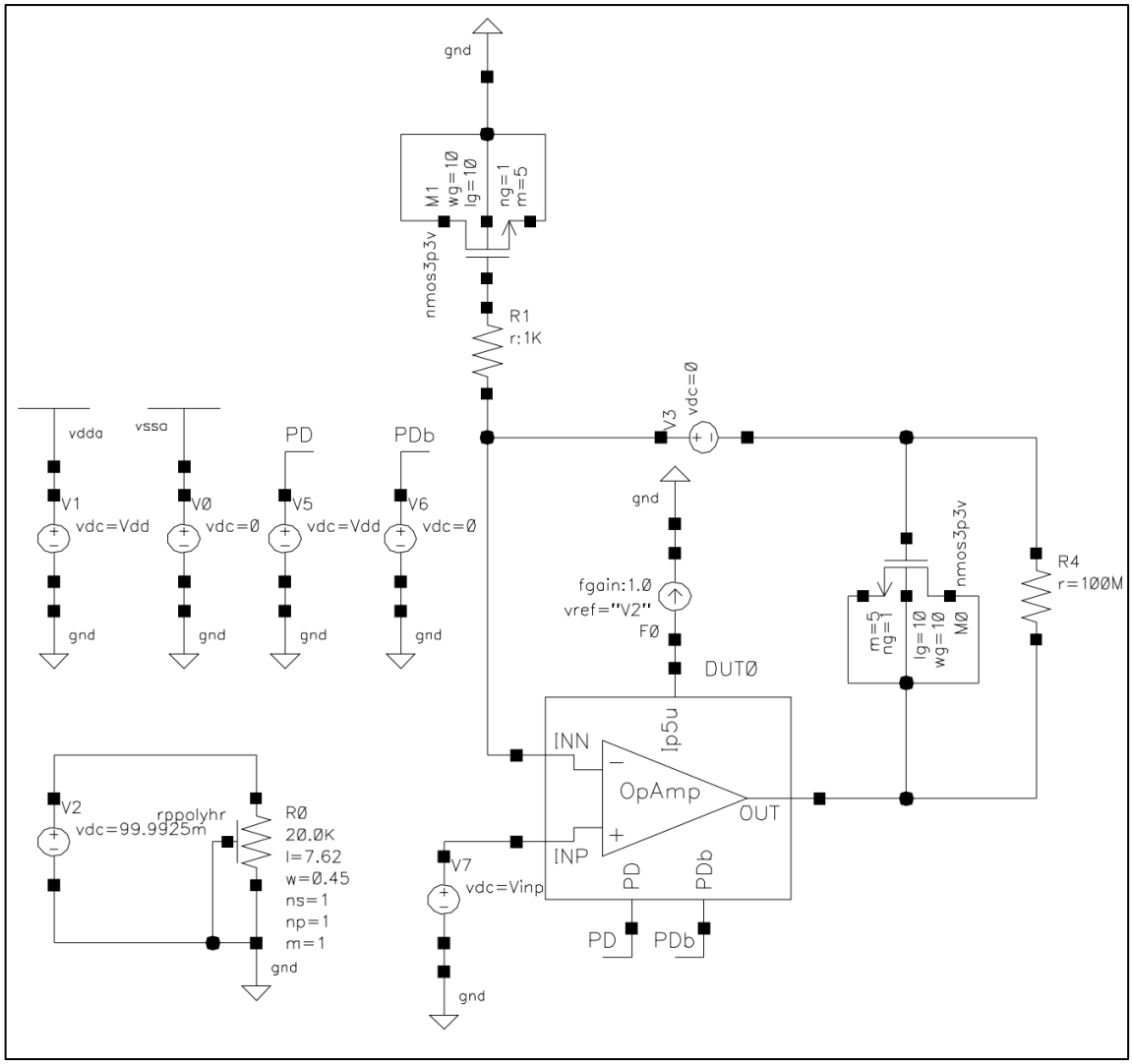

Figure 5.15 Simulation set-up for the IEF block stability analysis.

5.6 Switches

According to HLM, Section 4.2.3. The internal resistance of the switches has detrimental effect on the performance of the oscillator. Since the switches are implemented by MOSFETs, the resistance can be minimized by correct adjustments of the MOSFET channel dimensions.

The longer the length of the MOSFET channel, the higher is its resistance. So, in my design, the channels lengths of all the MOSFETs in the switches were set to minimum values. Further reduction of the MOSFET channel resistance was performed by increasing of the channel width.

5.6.1 Discharging switch

The switch, whose task is the discharge of the reference capacitor (S1 and S4 in Figure 4.1), was realized by the single NMOS with wide channel, M7 in Figure 5.16. The dimensions of this NMOS were chosen, so that the reference capacitor is discharged at the level of units of mV.

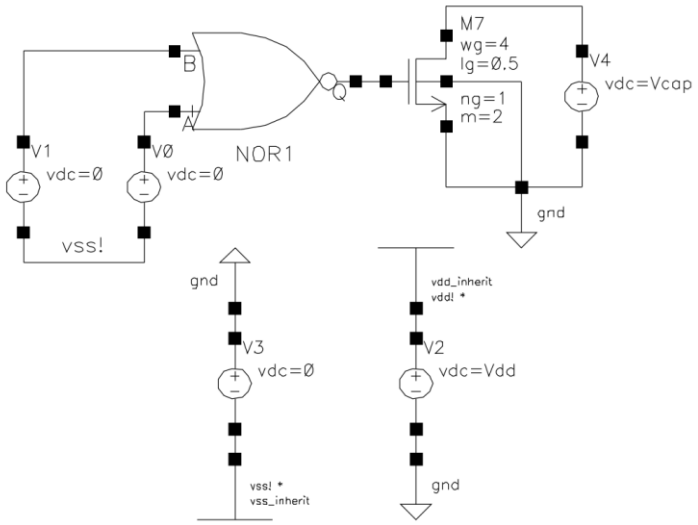

Figure 5.16 Simulation set-up for the discharging switch NMOS M7. DC voltage source V2 sets the power supply voltage (2.7 V and 3.6 V), V0 and V1 are set to 0 V to trigger the NOR gate to the 'high' state (so the switch M7 sees the same voltage on its gate as in the system).

Figure 5.16 shows the simulation set-up used to predict the maximum on-resistance of the considered switch. The simulation was performed in DC analysis in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters. The voltage of the V4 source was swept in the range of 0 to 1.5 V. The resistance was calculated as a ratio of the voltage and the current at the drain of M7. Further, the maximum value of the resistance was considered.

It turned out, that given the chosen dimensions of M7, the largest on-resistance of the switch over all the variations (temperature, power supply, process) was 1.1 kOhm for the following corner: power supply – 2.7 V, capacitors – the highest value, MOSFETs – low voltage output, resistors – the highest values, temperature – 175 °C.

If we consider the time constant τ of the RC-circuit, based on the on-resistance of the switch and the reference capacitor of 1 pF, we get τ = 1.1 ns. And, after the time 5τ = 5.5 ns (what is much shorter time than the half period of 50 ns), the reference capacitor is discharged to 0.6 % of its initial voltage. So, it is presumed that the internal resistance of the designed discharging switch will not affect the oscillator performance.

5.6.2 Charge transfer switch

Another critical switch is located between the reference capacitor and the sampling one. Figure 5.17 presents the implementation of it (its symbolic view is in Figure 5.18). It is known that the charge between the sampling and reference capacitors flow in both direction during different phases of operation. Therefore, the decision was to imply the 'transfer gate' switch, having stable low on-resistance.

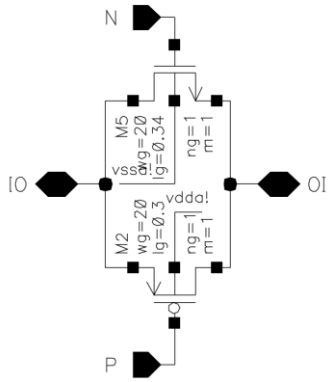

Figure 5.17 Switch applied between sampling capacitor and the reference one, as well as, IEF block.

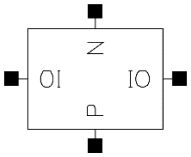

Figure 5.18 The symbolic view of the switch from Figure 5.17.

Figure 5.19 presents the simulation set-up to determine the on-resistance of the charge transfer switch. The simulation was performed in DC analysis in the temperature range of -40°C to 175 °C, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters. The voltage of the V0 source was swept in the range of -1.5 to 1.5 V. The resistance was calculated as an absolute value of the ratio of the voltage and the current at the pin IO of the simulated switch. Further, the maximum value of the resistance was considered.

The maximum value of the on-resistance of the switch turned out to be 303 Ohm, what is considered to be a sufficiently low value, since in the HLM simulations the 1 kOhm value was giving the acceptable performance. The worst corner has the following description: power supply – 2.7 V, capacitors – the highest value, MOSFETs – slow, resistors – the highest values, temperature – 175 °C.

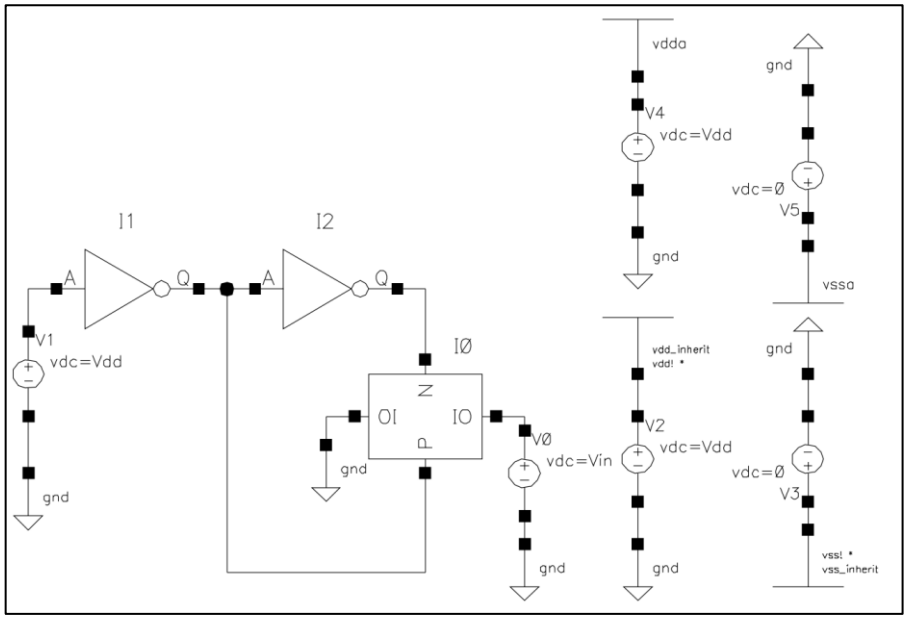

Figure 5.19 The simulation set-up of the charge transfer switch.

6 The complete system

The complete system was realized based on the blocks from Section 5, following the structure in HLM. The schematic of the implemented oscillator is shown in Figure 6.2.

The circuit contains current mirrors (encircled by dashed line in Figure 6.2), that provide biasing current to the comparators and the blocks based on the op-amps. Power-down control and the start-up are enabled through the inverter IN0.

As it can be seen, the reference capacitors CREF1 and CREF2 were implemented by the ideal capacitors from the default library in Cadence, since their capacitances directly affect the oscillation frequency and the trimming is expected for process compensation. The reference capacitors value was set to 1pF. The reference resistor in current charging source was, also, modeled by the ideal component from the default library, implying the same considerations on trimming.

The sampling capacitors were implemented by NMOS transistors CS1 and CS2. As it was discussed in Section 5.5, when the feedback capacitor was presented, the NMOS transistor connected as a capacitor shows big variations with temperature and process. However, the sampling capacitor does not have strict requirements on the accuracy, since its only function is the memorization of the reference capacitor previous peak voltage. The dimensions depicted in the figure insure that the capacitances of CS1 and CS2 are around 250 fF under nominal conditions. This is exactly 1/4 of the reference capacitor, so the same approach was used as in the original article on the oscillator utilizing IEF, Section 3.4.

The logical block outputs rstCREF1 and rstCREF2 trigger the discharging switches M18 and M20, connected to the reference capacitors.

Other employed components and blocks were presented in the preceding Section 5 and their place and function in the system was discussed in the HLM in Section 4.

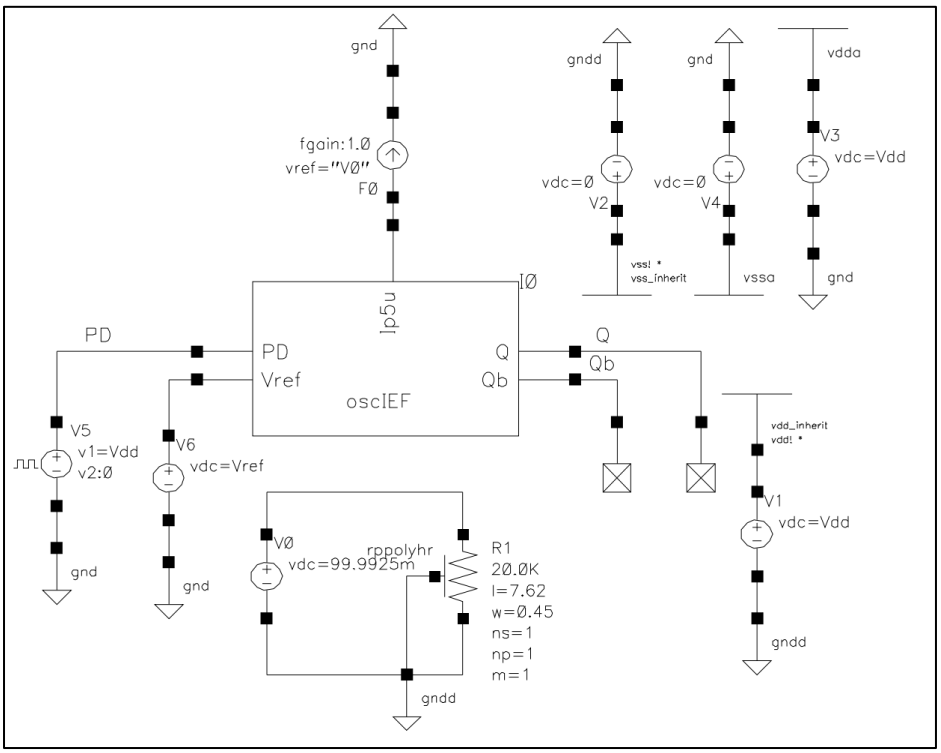

Figure 6.1 The simulation set-up of the complete system depicted in Figure 6.2.

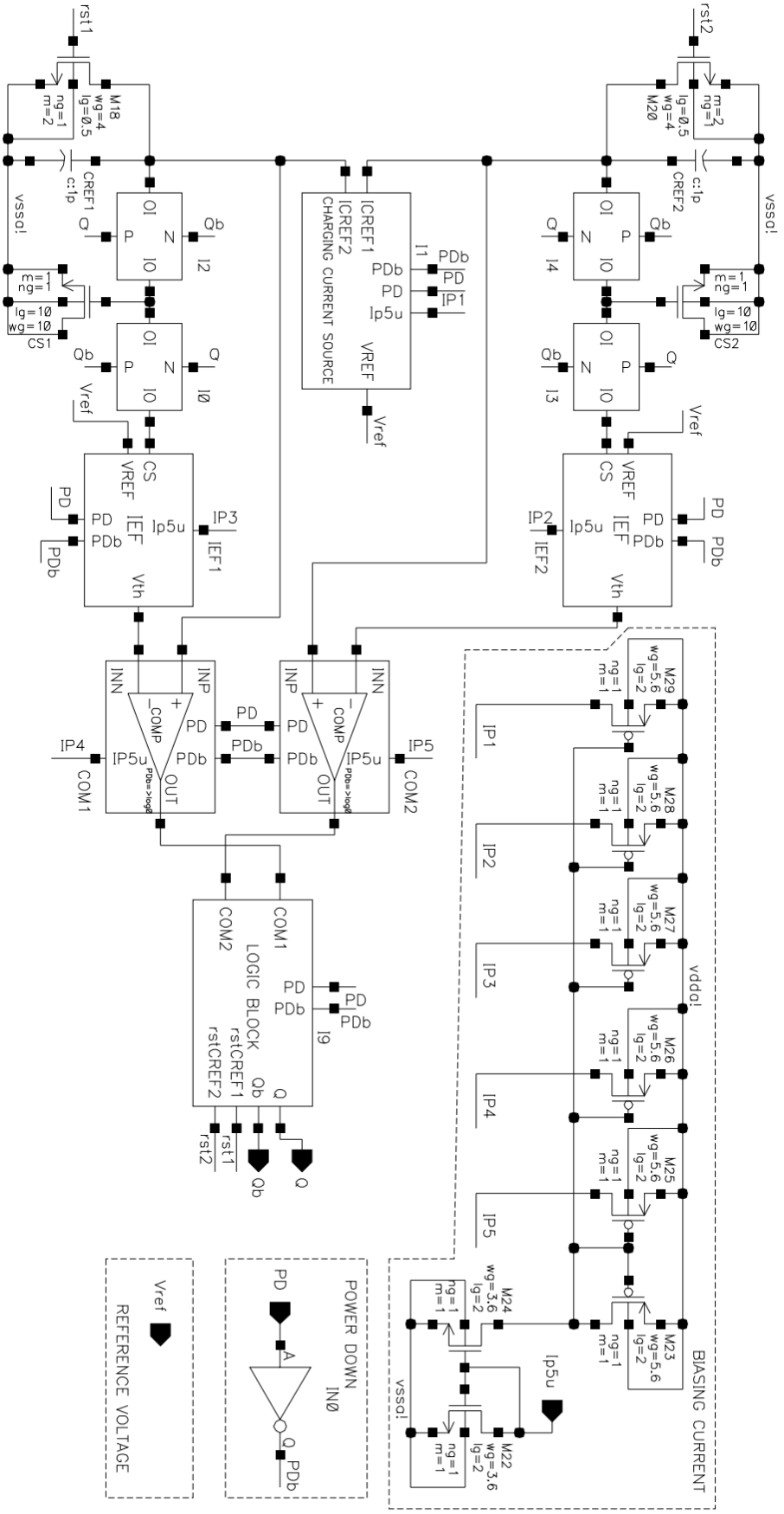

Figure 6.2 The designed sawtooth relaxation oscillator with IEF.

6.1 The simulation

The simulation of the complete oscillator is presented to show the overall performance of the system, since prediction of the performance based on the simulations of the blocks cannot assure correct results. Moreover, the designed blocks simulations in Section 5 were conducted to estimate the most important parameters, based on the previous theoretical study and the HLM, but it is possible that those considerations were not correct.

6.1.1 The set-up

The set-up for the oscillator simulation is depicted in Figure 6.1. The DC voltage source V3 supplies voltage to the analog part of the system, when the source V1 does the same for the digital part. The controlled current source F0 supplies biasing current required for the comparators and the op-amps, with modeled variations on temperature and process using resistor R1 as described in simulations in previous sections. The voltage source V6 sets the reference voltage that is supposed to be available from the band-gap voltage source. The pulse voltage source V5 defines the waveform of the power-down and the start-up (the rectangular waveform starts with 0 V and then after 10 µs a wide pulse of the power supply voltage takes place, enabling the circuit).

The simulation was performed in transient analysis with default settings on accuracy and convergence, in the temperature range of -40ºC to 175 ºC, power supply voltages Vdd = 2.7 V and 3.6 V and corners of the process variations of the components parameters.

6.1.2 The results

Figure 6.3 demonstrates function of the power-down signal. The oscillations start after it reaches 'high' state.

The simulation results showed that the highest obtained frequency of the oscillation is 9.295 MHz and the lowest is 8.153 MHz in all the variations. Figure 6.4 depicts the output waveform for the highest simulated frequency.

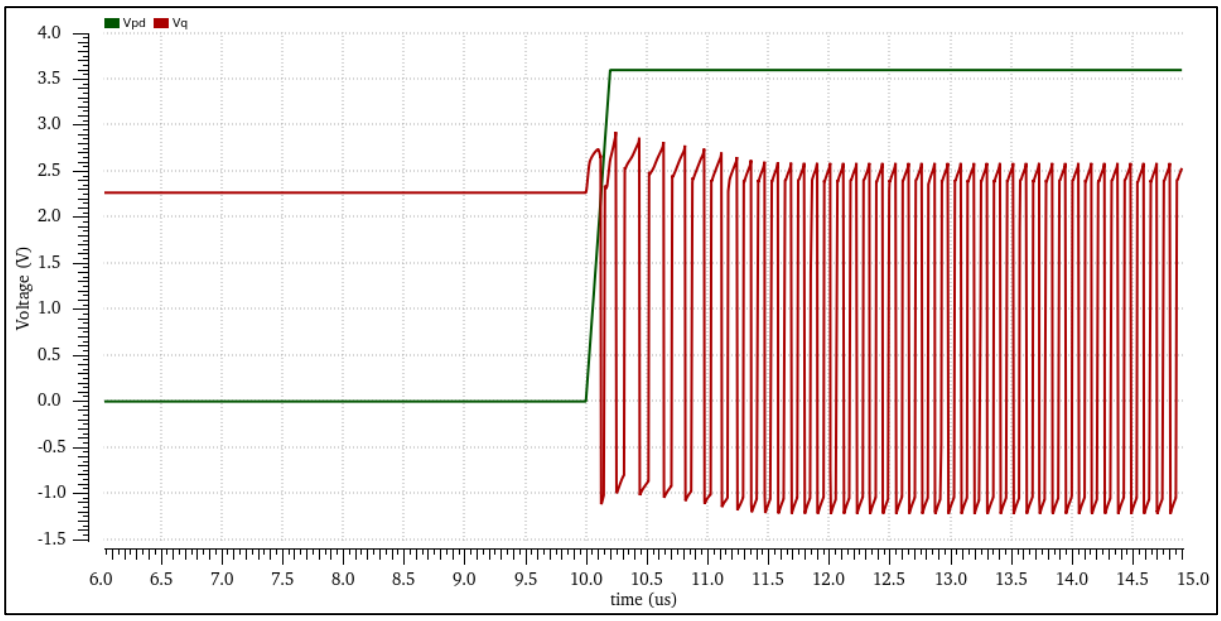

Figure 6.3 The simulated oscillator output waveform corresponding to the frequency of 9.295 MHz – red (Vq), and power-down signal – green (Vpd).

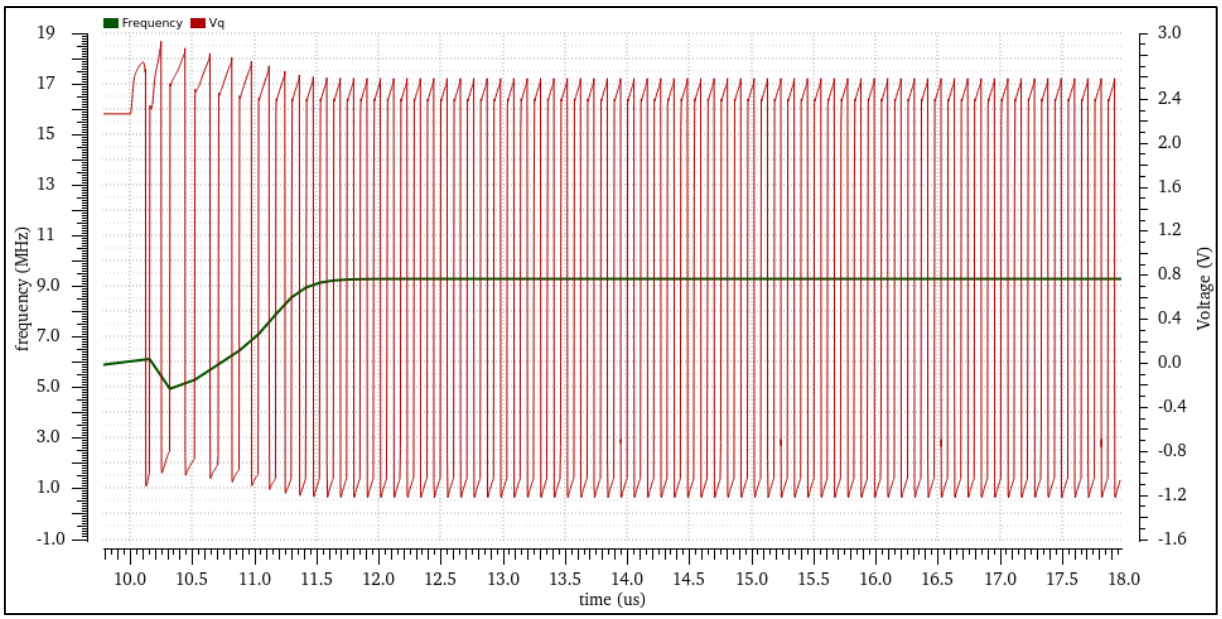

Figure 6.4 The simulated oscillator output waveform corresponding to the frequency of 9.295 MHz – red (Vq), and its frequency over time – green.

It is depicted in Figure 6.5, that the oscillator, for the corner producing 9.295 MHz, behaves in the same way how it was described in the HLM in Section 4: the threshold level (red "Vth1" in Figure 6.5) for the comparator is adjusted dynamically and the reference capacitor peak voltage is kept at 1.21 V after the settling.

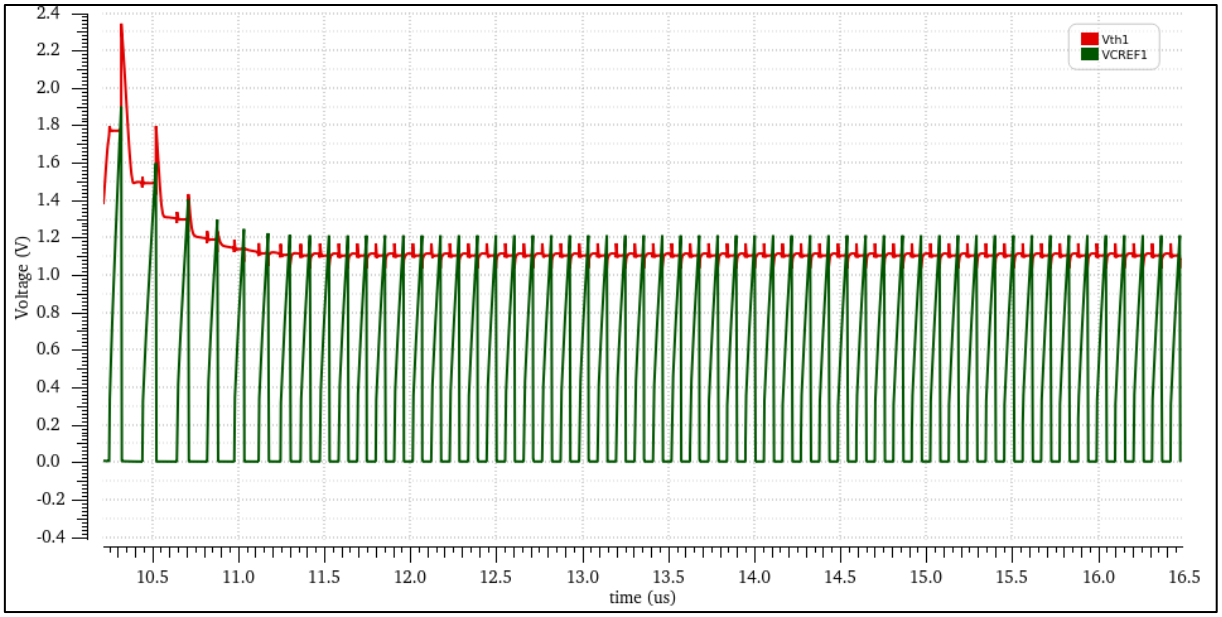

Figure 6.5 The simulated voltage waveform (corresponding to the corner producing frequency of 9.295 MHz) of the charging capacitor CREF1 (Figure 6.2) – greed (VCREF1), and the dynamic voltage reference for the comparator – red (Vth1).

However, the simulation results also contained corners, for which the system was not producing any oscillations. The example is shown in Figure 6.6. It can be seen that the output from the SR-latch is switched only after the power-down signal goes 'high'.

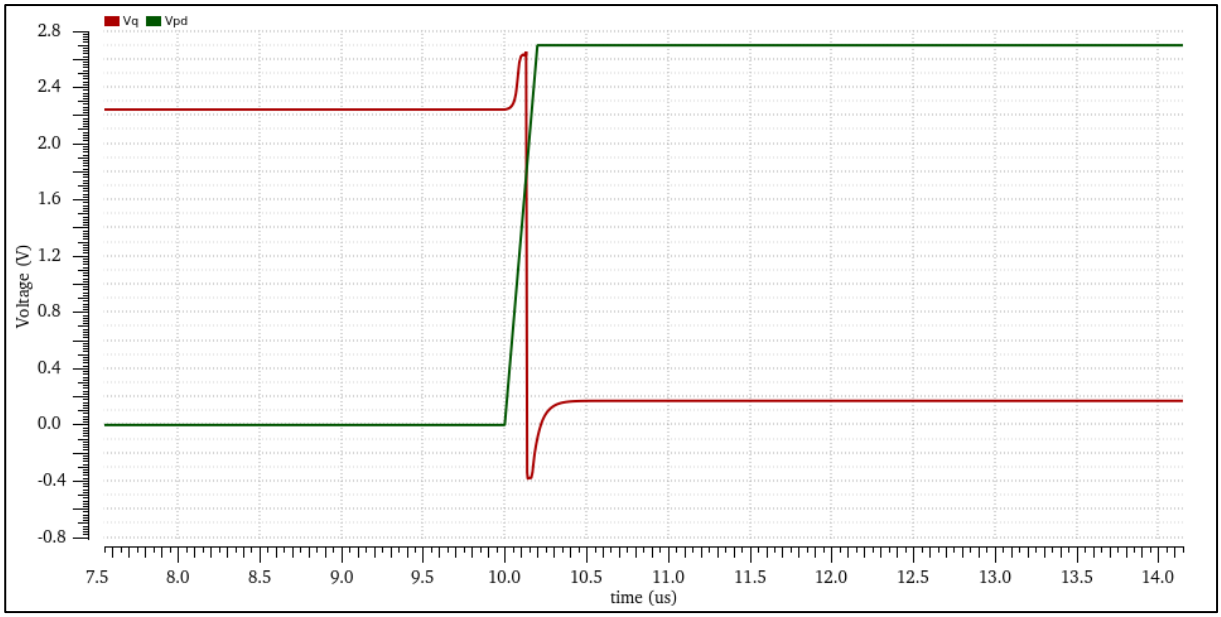

Figure 6.6 The simulated oscillator output waveform corresponding to the “faulty” corner – red (Vq), and power-down signal – green (Vpd).

6.1.3 Discussion on the results

The simulation results showed that the system does not provide the expected performance.

The issue, depicted in Figure 6.6, suggests that the comparators do not produce trigger signal for the SR-latch. It can be caused by the insufficient biasing of the comparators in certain corners, since the biasing current source in simulations was modeled based on the variations of the resistor from the considered technology.

A similar issue can cause large frequency variation for the other “working” corners.

There is also another unconsidered problem in the design. The switches employed in the circuit were designed based on the HLM considerations in Section 4. The HLM simulation in Section 4.2 modeled switches by the ideal ones with the series resistors. However, the effect of input capacitance of the switches was not considered. When the switch is large, it has lower on-resistance, but its capacitance on the gate becomes significant and varies with process and temperature, causing variations of the delay.

7 Conclusion

The initial phase of the thesis was aimed on the theoretical basis, needed for the understanding of processes in relaxation oscillator. The first-order oscillatory systems were classified according to their topology and its relation to occurrence of different negative effects. Great attention has been paid to the noise modeling of the relaxation oscillator.

Theoretical considerations enabled me to conduct qualitative comparison of the integrated relaxation oscillator topologies, presented in recent publications. It turned out that the approach of integrated-error feedback showed the best performance based on the measurement results presented by the authors. Moreover, this concept employed two-integrator sawtooth oscillator structure, which according to the theoretical review was advantageous in relation to its noise performance. Also, the idea of IEF does not require too fast comparators (with small propagation delay), so the comparators can have smaller noise bandwidth and current consumption.

The oscillator with IEF was modeled in Spectre simulator using ideal blocks, what helped to define the effects of the employed blocks features on the stability of the oscillation frequency. And, the obtained results were used in the practical design.

The implementation of the oscillator was done by subsequent design of its blocks. Each block was designed to meat the requirements postulated by the authors who proposed IEF, as well as the requirements found during the simulations of the high-level model, based on the ideal blocks. The simulation descriptions and results of the separate blocks in the thesis included only the most important parameters directly influencing the oscillator performance, and the results were proven to be acceptable.

Unfortunately, when all the blocks were assembled in the complete system, the simulations showed that the oscillator does not have the expected performance: the frequency instability with process, temperature and power supply variations was too high, it produced periodical signal within the frequency range of 8.153 to 9.295 MHz. Also, it was found that in certain corners in the analysis, the oscillator did not produce any periodical signal. As it was discussed in Section 6.1.3, the reason may be in the insufficient biasing of the comparators.

So, certainly the design has to be improved. And, it should include additional blocks to set precise charging current reference for any process variations: the digitally trimmed reference resistor with temperature compensation by employing resistors with TCs of different sign, and digitally trimmed current mirror to increase the setting control range. Also, the layout of the design is supposed to be realized. It can induce further adjustments for area optimization and higher immunity to parasitic capacitances, inductances etc.

Despite the unwanted simulations results of the designed oscillator, during the work on this thesis, I obtained broad theoretical knowledge concerning relaxation oscillators, as well as, plenty of practical skills and experience, what is a good basis for my future studies and practical employment.

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Appendices

A. Reduction of 1/f noise in MOSFET under switched bias condition

The 1/f noise is a random process defined in terms of the shape of its power spectral density $S(f)$. The power or the square of some variable associated with the random process, measured in narrow bandwidth, is roughly proportional to reciprocal frequency (Figure 3.27) [8]:

$$S(f) = \frac{constant}{|f|^{\gamma}}, \tag{40}$$

where $0 < \gamma < 2$ and usually γ is close to 0.

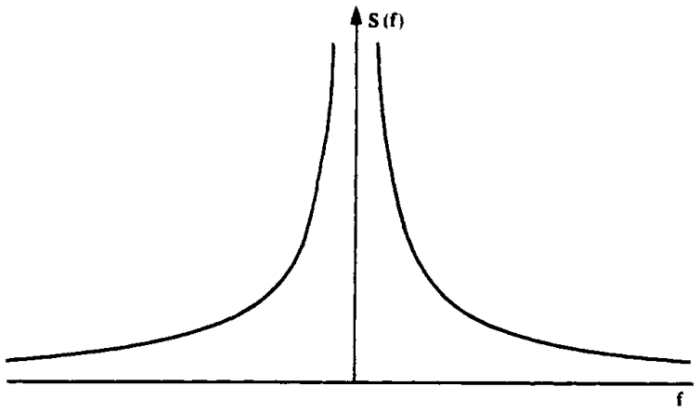

Figure 0.1 The power spectral density of 1/f noise. The image is taken from [8].

The above-presented definition is rather general, since this kind of noise is present in different physical processes. Of course, the point of interest in this work is the 1/f noise in MOSFET. The author of [21] referred to this kind of noise in MOSFET as flicker noise and presented one of mechanisms of its occurrence:

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many "dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface , some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. [21]

Gierkink's dissertation in [5] has a chapter devoted to the discussion of the phenomenon, when the intrinsic 1/f noise of a MOSFET during the transistor active phases can be reduced significantly by switching off the transistor periodically. In fact, utilization of this effect can potentially improve the design of the oscillator. So, a review of an experiment (described in [5]), that demonstrates and proves the phenomenon, is presented below.

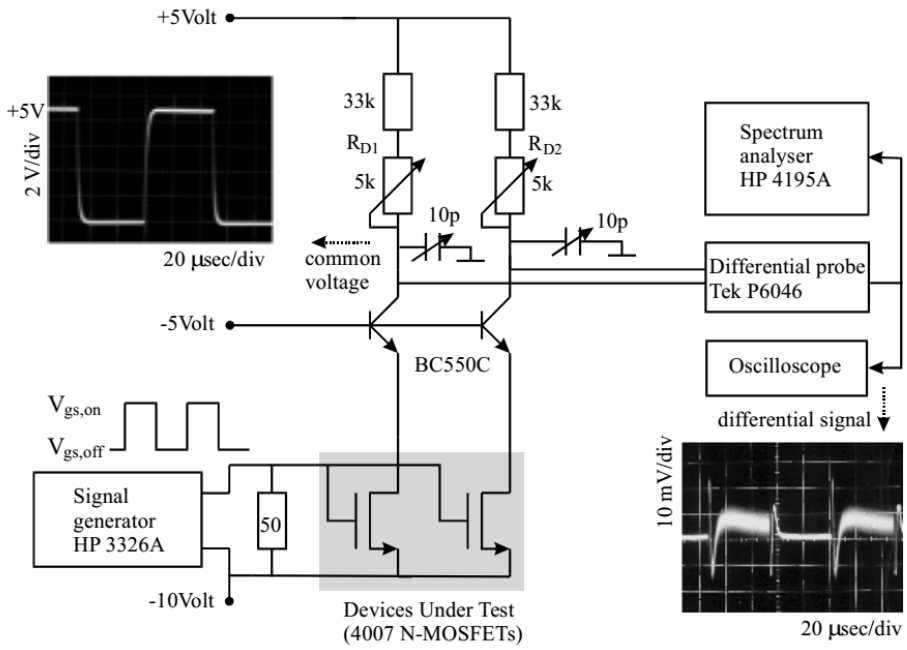

Figure 0.2 The measurement setup, presented in [5], to measure MOSFET noise under switched bias conditions. The image is taken from [5].

Figure 0.1 depicts the measurement setup for MOSFET noise measurement under switched bias condition. The setup exploits the high common mode refection ration of a differential probe, what enables to measure small differential noise currents superimposed on much larger common mode switched bias currents of two equal MOSFET devices under test. The bipolar cascode transistors supply the drain of the MOSFETs with an almost constant voltage and conduct the MOSFET drain currents to resistors R_{D1} and R_{D2}, that convert tested MOSFET channel currents to voltages. Switched bias conditions are established by driving gate-source voltages of the two tested devices by a common 50%-duty-cycle square-wave signal with a maximum voltage level V_{GS_on} and an adjustable minimum voltage level V_{GS_off}, which is below the threshold voltage. So, the differential probe in an ideal situation senses the differential voltages that is dominated by the noise current of the tested transistors in the "on" state. However, mismatches in the tested transistors large-signal characteristics and finite common mode rejection of the differential probe result in a residual switching signal at the output of the probe (Figure 0.1 – the right photograph). The author of [5] claims that resistive and capacitive trimmers were provided to equalize the common signals and thus minimize the differential residual to sufficiently low values so as to be below the input dynamic range of the spectrum analyzer. Moreover, the periodic nature of the switching signal results in spectral peak, that can be predicted and taken out from 1/f noise contributions. The noise floor estimation and verification of the observed results were done by replacing tested MOSFETs by BJTs with emitter resistors operating at the same bias current as the tested transistors. The noise floor was claimed to be more than 10 dB below the tested transistors noise in all the measurements.

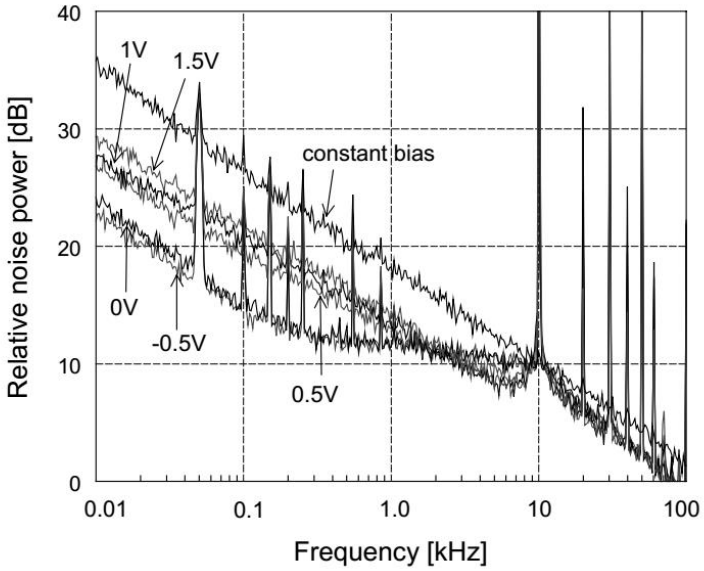

Figure 0.3 Measured baseband 1/f noise for constant and switched bias conditions, [5]. Measured device: HEF 4007 NMOS; switching parameters: $f_{switch} = 10\ kHz$, 50% duty cycle, $V_{GS\_on} = 2.5\ V$, V_{GS_off} is indicated on the plot for different curves. The image is taken from [5].

Figure 0.2 and Figure 0.3 shows the measured noise spectra of the HEF 4007 NMOS by the above-described setup. An arbitrary reference power level was chosen in defining the vertical scale in the figures. The upper curves on both figures show the measured noise spectrum with constant biasing at a gate-source voltage of 2.5 V ($V_T \approx 1.9\ V$); the remaining curves show the noise spectrum of the devices switched periodically between $V_{GS\_on} = 2.5\ V$ and V_{GS_off} (the values are indicated for different curves in the figures) with 10 kHz in Figure 0.2 and 2 MHz in Figure 0.3.

Modelling the 50% duty-cycle switching operation as a simple modulation action, a 6-dB noise reduction is expected in the 1/f noise spectrum below the switching frequency. This is because the overall noise power is halved and distributed in the spectrum around DC and multiples of the switching frequency. However, the measurements show an additional anomalous reduction in the 1/f noise spectrum. Remarkably, the amount of noise reduction is dependent on the gate-source voltage in the off-state, even if it is well below the threshold voltage V_T. The maximum additional reduction appears at minimum V_{GS_off} and is about 8dB at 1kHz in Figure 0.2. Also the same effect can be seen in Figure 0.3: in the experiment for 2 MHz switching frequency, a large reduction in 1/f noise is observed, more than the expected 6 dB due to the 50%-duty-cycle switching. [5]

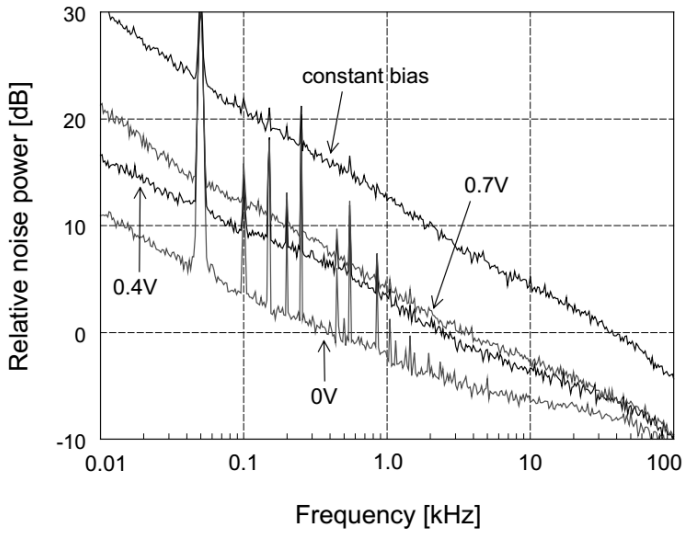

Figure 0.4 Measured baseband 1/f noise for constant and switched bias conditions, [5]. Measured device: HEF 4007 NMOS; switching parameters: $f_{switch} = 2\ MHz$, 50% duty cycle, $V_{GS\_on} = 2.5\ V$, V_{GS_off} is indicated on the plot for different curves. The image is taken from [5].

The principle for reduction of 1/f noise in MOSFET devices offers an additional design improvement for the developer. However, as it was noted by Gierkink in [5], the technique has certain limitations. It can be used only in cases when the transistor has to be in on-state just for an interval of time. Nevertheless, the operation principle of relaxation oscillator and generation of the periodical signals by the oscillator, assume that MOSFET devices in the design can be biased periodically and utilize this noise reduction technique.