Master's Thesis

Czech Technical University in Prague

F3

Faculty of Electrical Engineering
Department of Electric Drives and Traction

Design of an electric powertrain for the *Formula Student*-class vehicle

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Supervisor: Ing. Jan Bauer, Ph.D.
Field of study: Electrical Engineering, Power Engineering and Management
Subfield: Electrical Machines, Apparatuses and Drives
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MASTER'S THESIS ASSIGNMENT

I. Personal and study details

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II. Master's thesis details

Master's thesis title in English:

Design of an electric drivetrain for the Formula Student-class vehicle

Master's thesis title in Czech:

Návrh elektrického pohonu vozidla Formula Student

Guidelines:

1) Describe the existing drivetrains in eForce's vehicles.
2) Do a research of motors, power electronics and control strategies suitable for use in an electric drivetrain.
3) Design and develop a motor controller usable in a Formula Student-class vehicle.
4) Verify the developed prototype in an existing vehicle.

Bibliography / sources:

[1] Design of Drive for Formula Student Car, František Pech, master's thesis
[2] Control of the Formula Student Car Electric Drive, Miroslav Rýzek, master's thesis
[3] Design of Rotating Electrical Machines, Juha Pyrhonen; Tapani Jokinen; Valeria Hrabovcova, ISBN: 978-0-470-69516-6
[4] LEONHARD, Werner. Control of electrical drives. 3rd ed. Berlin: Springer, 2001.

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Ing. Jan Bauer, Ph.D. Supervisor's signature	Head of department's signature	prof. Ing. Pavel Ripka, CSc. Dean's signature

III. Assignment receipt

The student acknowledges that the master's thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the master's thesis, the author must state the names of consultants and include a list of references.

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Date of assignment receipt	Student's signature

Acknowledgements

Thesis of this magnitude could not originate without help of my colleagues, friends and family.

I would like to thank my supervisor Ing. Jan Bauer, Ph.D. for his valuable consultations and support in creation of this thesis.

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Finally, and most importantly, I would like to thank my family, my girlfriend and my friends for their unwavering support in my study endeavors...

Declaration

I hereby declare that the presented thesis is my own work and that I have cited all sources of information in accordance with the *Guideline for adhering to ethical principles when elaborating an academic final thesis*.

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Stanislav Tomášek

In Prague, 24. May 2019

Abstract

This thesis' main objective was to design and develop a functional motor controller for usage in a Formula Student competition vehicle of the eForce FEE Prague Formula team.

Work is split into several chapters. Exploring a drivetrain development progression in the team, presenting a needed theory for a motor controller development and giving a detailed overview of the designed device. The last chapters are dedicated to evaluation of the design.

Thesis had explored a new methodology in a phase current sensing, providing a significant precision while allowing for a low cost and compact design. Overall aim was to create a simple, robust and cheap solution.

Verification of the design was performed in the laboratory environment of the faculty in order to ensure preparedness for integration into the vehicle.

Further work will focus on control strategy improvements and final integration into the team's vehicles.

Keywords: electric vehicle, electric motor, PMSM, rotational sensor, resolver, hardware development, PCB, motor controller, VSI, IGBT, current sensing, shunt resistor, micro-controller, programmable logic, sigma-delta modulation, embedded software, C/C++, FreeRTOS, motor control, field oriented control, eForce, Formula Student

Supervisor: Ing. Jan Bauer, Ph.D.

Abstrakt

Hlavním úkolem této diplomové práce bylo navrhnout a postavit funkční prototyp frekvenčního měniče pro použití ve vozidlech týmu eForce FEE Prague Formula, soutěžícího v mezinárodní inženýrské soutěži Formula Student.

Práce je členěna do několika kapitol, kdy je nejdříve prozkoumán již v minulosti provedený vývoj v týmu. Dále je vystavěna potřebná teorie pro vývoj frekvenčního měniče. Další kapitola detailně popisuje provedený vývoj zařízení. Poslední kapitoly se věnují zhodnocení navrženého měniče.

Diplomová práce také prozkoumala nové možnosti v měření fázových proudů, umožňující vysokou přesnost při zachování nízké ceny a kompaktních rozměrů. Celkovým cílem bylo navrhnout jednoduché a robustní zařízení s nízkou výrobní cenou.

Ověřování návrhu bylo provedeno v laboratořích fakulty pro ujištění připravenosti navrženého měniče pro nasazení do vozidla.

Práce bude pokračovat na vylepšování řídícího algoritmu a postupné integraci do týmových vozidel.

Klíčová slova: elektrické vozidlo, elektrický motor, PMSM, senzor úhlové polohy, resolver, vývoj hardware, DPS, frekvenční měnič, napěťový střídač, IGBT, měření proudů, bočník, modulace sigma-delta, mikrořadič, programovatelná logika, software, C/C++, FreeRTOS, řízení motorů, vektorové řízení, eForce, Formule Student

Překlad názvu: Návrh elektrického pohonu vozidla Formula Student

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Chapter 1

Introduction

With electric vehicles becoming a larger item and a perspective for satisfying ever-increasing requirements for ecological mobility, the development of a battery-operated electric vehicle drivetrains becomes a more and more perspective field.

The Formula Student competition is one of the prestigious events, tasked with giving university students interested in motorsport an opportunity to work on a real engineering tasks, mirroring those found in a true engineering firm.

This thesis describes a theory, design, development and actual prototype realization with testing of a crucial part within any battery-operated electric vehicle – the motor controller. This is done within entire context of competition, the team, its vehicles, and a current state-of-the-art.

Thesis also aims at experimenting with alternative solutions for phase current measurements and simple implementations of various circuits in the design.

Both sections on the FSAE and eForce are taken and updated from my bachelor's thesis.[1]

1.1 Formula Student competition

A family of an engineering student competitions held every year in many countries across the globe. The objective is to annually develop and build a Formula-class vehicle according to competitions' rules and compete against other student teams under a supervision of experts from the automotive, engineering and business fields.

Individual competitions are split into events. Those are categorized into two groups – static and dynamic.

Static events are concerned with presentation of the vehicle and entire project on both engineering and business grounds. Dynamic events are tasked with stressing the vehicle in actual racing. Each event has a predefined weight in points, team claiming the highest sum of said points is the winner.

Altogether the official competitions are aggregated by the *WRL* in which every participating team is ranked against other teams.

Competitions' primary objective is to provide engineering students interested in motorsport and technology with a practical experience on the engineering design, hands-on development, project presentation and teamwork.

To this date, more than 600 teams from entire world take part in more than 10 instances of the competition.

1.1.1 History

Original competition was founded in the early 1980s' by the Society of Automotive Engineers in the USA. During the 1990s' competition "arrived" into the continental Europe and many new teams originated, primarily in the Germany and neighboring countries.

Originally only a combustion drivetrain vehicles were eligible for entering. In the 2010 a decision was made for allowing vehicles with electric drivetrains to enter the competition to address a renewed interest of the automotive industry in the electric vehicles.

Newest addition to the vehicles' categories are *driverless* vehicles, which must compete with using only automatic control without pilot intervention. To promote this category, the vehicles does not need to satisfy a first-year vehicle rule, necessitating only needed modifications to accommodate the automatic systems. Both combustion and electric vehicles can be modified for this category.

1.1.2 Rules

In order to specify requirements for vehicles designed and manufactured by the teams and the course of the competitions, a set of an official rules is released

every year. By modifying and releasing them every year the competitions stays "fresh" even for the advanced teams and forces them to continue their development, much like the less advanced teams.

Comparing FSAE rules against other (professional) formula-based motorsport rules e.g. the official *Formula F1* rules, the FSAE rules are far less stringent to the actual design of the vehicles and are focused primarily on securing safety of the competitions' participants.

The thesis will constantly make references to a competition's rules in order to back its design decisions. This will be done by using a follwing notation[SECTION RULE]. The design was performed with a 2019 edition of *Formula Student Germany's* rules.[2]

1.2 eForce FEE Prague Formula team

1.2.1 History

The first FSAE team at the Czech Technical University in Prague was the *CTU CarTech* under the Faculty of Mechanical Engineering, established in the 2009.

Electric "sister" team, the *CTU CarTech Electric* was established as a reaction to concession of the electric drivetrain in the competition at 2010 under the Faculty of Electrical Engineering, more precisely the Department of Electric Drives and Traction.

Since then the team had split into *CTU CarTech* and *eForce FEE Prague Formula* teams to define boundary between combustion and electric drivetrains more clearly.

1.2.2 Team

The eForce team consists of a roughly 30 students from both FME and FEE of both bachelor and master study programmes. Team members are classified into 4 groups according to their specialization and/or interest – Mechanical systems (*MES*), Electrical systems (*ELS*), Project group (*PRG*) and the IT group.

Each group has a designated leader who is answering directly to the *Team captain*. The "buffer" between the team and the faculty is the *Faculty adviser*.

To this date, the team had built seven vehicles and successfully competed with them across the Europe and the America. The eForce stays the only Czech team building FSAE-class electric drivetrain vehicles.

One of the greatest eForce's strengths is the in-house research and development of every vehicles' part, thus giving the team competitive edge over other teams when presenting the engineering design, adaptability to changing conditions during competitions or troubleshooting.

More information about the FSAE competitions, its rules and the eForce team can be found on their official website.[3]

Chapter 2

Electric drivetrain

The electric vehicle's drivetrain of a Formula Student vehicle is composed of several functional blocks. This section will provide basic overview of individual blocks with references to other team members' created designs for their theses.

- **Accumulator** – stores energy used by both vehicle's tractive system and low-voltage systems.
- **Motors** – perform conversion from electric energy to mechanical in order to drive the vehicle.
- **Mechanics** – concerned with transmitting the motors' power to the vehicle's wheels. Due to having motor per each wheel a mechanical differential is not required to properly split the power.

  P. Sucháček had described and designed mechanics used in the *FSE.04x*'s drivetrain.[4] F.Pech's master thesis also provide overview of used mechanical parts in Formula Student vehicles' drivetrain.[5]
- **Motor controllers** – used to convert accumulator's DC supply into power capable of driving the used motors. Motor controllers in *eForce*'s vehicles implement toque-based *Field oriented control*.

  Description of the newest motor contorller will be a primary objective of this thesis. Previous motor controllers are described in M. Rýzek's master's thesis[6] and F. Pech's bachelor's thesis.[7]
- **Traction control** – while motor controllers govern individual motors, the traction control is tasked with setting the motor controllers' parameters and setpoints (being a superior control) in order to provide a vehicle handling based on a throttle pedal pressure, steering wheel angle, wheel slip angle and various other parameters.

  Treatment of this subject can be found in both S. Divín's theses[8][9] and M. Lászlo's master's thesis.[10]

2.1 Energy storage

The current electric vehicles store energy mainly in rechargeable accumulators (secondary batteries).

Generally speaking, the batteries store electrical energy using chemical reaction within an electrolyte during *charging*. Reverse process of electrical energy extraction from the batteries' electrolyte is called *discharging*.

Detailed information on batteries function can be found in various books or articles thanks to a great focus and interest sparked by electric vehicles' expansion.[11]

The eForce's vehicles utilize lithium-ion battery technology thanks to their superior energy-to-weight ratio. The lithium-ion batteries can be further divided by specific lithium-ion chemistry. Current vehicles use *NMC* chemistry in cylindrical batteries (18650 form factor) manufactured by *Sony* under brand family *VTC*.

The individual cells are connected in a series-parallel combination into individual segments (or *stacks*). These stacks must have their maximum terminal voltages below 120V and contained energy must not exceed 6MJ due to a safety concerns.[EV 5.3.2]

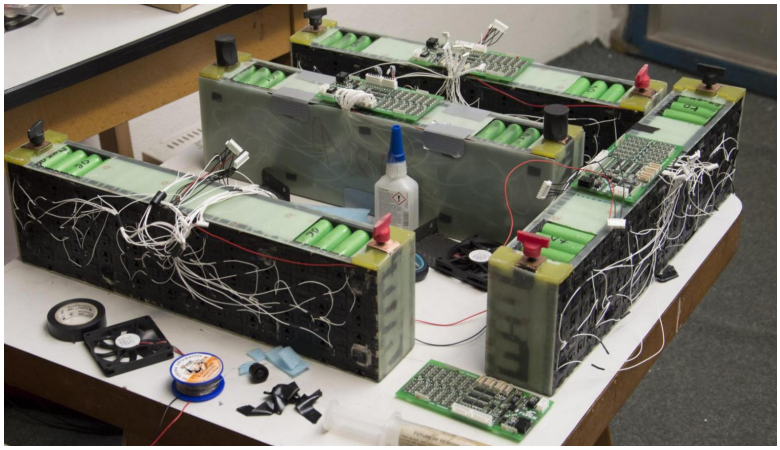


Figure 2.1: Individual segments of the fourth generation vehicle's accumulator pack.

Stacks must be placed within accumulator pack enclosure whose electrical[EV5.4] and mechanical[EV 5.5] requirements are set by extensive rules. Individual stacks must have their parameters monitored by an accumulator management system (AMS), in our case called BMS.

The BMS measure voltages and temperatures across the stack's cells in order to ensure safe operating conditions with respect to over-temperature, over-voltage and under-voltage states. BMS also help to manage charging of the batteries by balancing the voltage across the cell segments. Design and development of the BMS units was detailed in J. Mánek's bachelor's thesis[12], M. Rýzek's bachelor's thesis.[13]

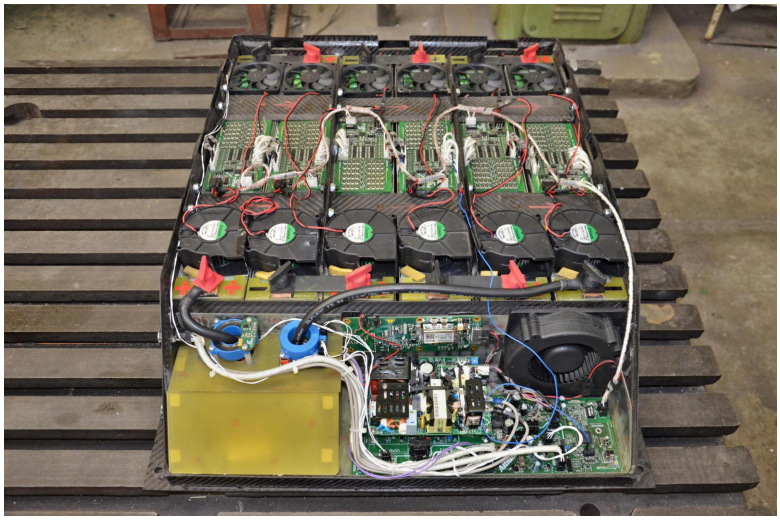


Figure 2.2: Accumulator pack of the fourth eForce's vehicle generation with individual stacks and control electronics visible.

A complete battery packs were described in A. Podhrázský's bachelor thesis[14] and J. Nohejl's master's thesis.[15]

Fuel cell technology for use in traction is still in infancy and while the research into this technology shows significant promise, the batteries are readily available for a large-scale manufacture and integration into electric drivetrains. Another aspect is that the Formula Student rules explicitly forbid usage of a fuel cells.[EV 5.2.2]

2.2 Electric motors

Electric motors are devices used to convert electrical energy into mechanical energy. Unlike combustion engines, electric motors can freely convert energy in opposite direction without a need for any specialized equipment.

Their function is primarily governed by two physical laws. The Lorentz force and a Faraday's induction law with Lenz's law.

The Lorentz force defines force exerted on a current-carrying conductor of finite length, placed in an external magnetic field.

$$\vec{F} = l \cdot \vec{I} \times \vec{B} \tag{2.1}$$

Faraday's induction law describes electromotive force generated on the conductor present in changing magnetic field flux. Lenz's law added a proper direction for the generated EMF. It can be thought of as an opposing reaction of the conductor to the changing magnetic flux.

$$\varepsilon = -\frac{\partial \Phi}{\partial t} \tag{2.2}$$

The electric motors can be divided by various criteria, most common is the type of electric power which the motor is capable of working with, dividing between AC and DC motors.

Formula Student vehicles use predominantly an AC synchronous motors with permanent magnets in either PMSM, or BLDC configuration, thanks to their high power-to-weight / torque-to-weight ratios. Some teams utilize a DC motors and more advanced teams experiment with usage of a reluctance motors.

The *eForce* team use a four permanent magnet synchronous motors in their vehicles since fourth vehicle generation. These motors are developed and manufactured in conjunction with our sponsor *TGDrives*.

Exact description of an electric motors function is out of this thesis' scope. The F. Pech's master thesis[5] discusses a motor design for use in team's vehicles. Proper mathematical treatment of electric motors alongside with common motors construction can be found in[16].

2.3 Power electronics

In order to generate an alternating current capable of powering the used AC motors from the vehicle's accumulator pack DC supply, a semiconductor power inverter must be used.

The described inverter is of voltage type (VSI). Schematic of a three-phase VSI can be found below with a connected motor.

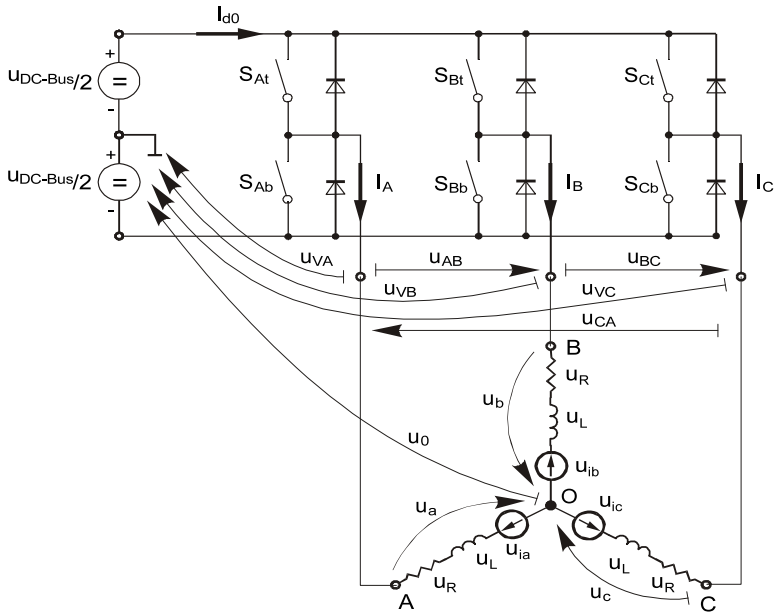


Figure 2.3: Schematic of a 3-phase voltage source inverter.[17]

The VSI is consisted of a fully controlled semiconductor switches which allow to govern both turn on and turn off instants. Usable silicon devices for the VSI construction are following.

- **BJT** – bipolar junction transistor
- **MOSFET** – metal oxide semiconductor field-effect transistor
- **IGBT** – insulated-gate bipolar transistor
- **GTO** – gate turn-off thyristor
- **IGCT** – integrated gate-commutated thyristor

Selected switch must fulfill certain criteria for a given application.

- *Blocking voltage withstand* – inductive load switching can lead to a significant overvoltage spikes being applied to the semiconductor. In order to prevent a permanent damage the semiconductor, it should be dimensioned to at least 1.5× battery voltage.
- *Current capability* – must respect expected load of the VSI for a specified time with a cooling consideration.

- *Switching frequency* – primarily governed by used switch technology, higher switching frequency increase switching losses but allow for a better control, shifting of EMI to a higher frequencies, reducing signal filtering requirements, and acoustic noise lowering. Higher switching frequencies also increase iron losses in the connected motors and increases skin effect in conductors.
- *Switching times* – also governed by used switch technology, faster switching can increase EMI and requirements for a higher-quality DC-link capacitors to prevent semiconductor damage due to an uncontrolled switching spikes. On the other hand, it lowers the switching losses.

It can be seen that selecting optimal switch is a complex task, involving many variables and design decisions.

2.3.1 BJT

The BJT are transistors which allow governing the flowing current across them by applying current into their control (base) terminal – a current controlled transistors.

They're characteristic by their low saturation voltage drops which limit conductive losses. This would make them ideal for a power electronics use. Unfortunately their low control terminal impedance coupled with low β factor makes them unusable for a VSI applications.

Their usage lies primarily in a linear circuits in which the current flow must be closely regulated.

2.3.2 MOSFET

The MOSFETs are first of the discussed semiconductor switches which are usable in the VSI application. They are a voltage controlled transistors, capable of a fast switching with a sufficient reverse voltage rating to work in a high-voltage, tractive applications.

In this section an N-channel, enhancement type MOSFET will be primarily described.

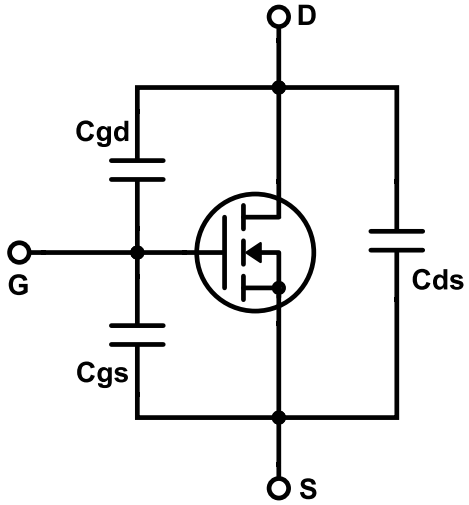


Figure 2.4: Schematic of an N-channel MOSFET with marked major capacities.

The MOSFET is controlled by applying voltage between its gate and source terminals.

To turn on the component a voltage source must be applied to the gate terminal, once the voltage on the gate capacitor rises above component's threshold value (usually denoted as $V_{G(th)}$) the MOSFET will start to open. The current through the device will begin to increase while the gate capacity will continue to be charged.

Once the gate capacity is charged to certain level a *Miller plateau* of the turn-on phase is reached, where the voltage across the transistor begins to fall, this change in the gate-drain voltage creates a sink for current flowing into the gate, stopping increase of the gate capacitor. This is a primary mechanism behind a turn-on losses in the MOSFET transistors.

After the drain-source voltage reaches its minimum, a gate-source voltage can be charged to the final voltage of the driver, finalizing the turn-on.[18]

During the device on-state the losses are governed by the declared conductive channel's resistance $R_{DS(on)}$ and a flowing current I_D

$$P_d = R_{DS(on)} \cdot I_D^2 \tag{2.3}$$

from above equation it can be seen that turn-on losses scale with a second power of the flowing current.

In order to turn-off the component an inverse process to the described turn-on must be done.

Two issues come with the fast turn off. First are linked to package's stray inductances coupled with a high $\frac{di_D}{dt}$ rates, which are capable of slowing down the turn-off process by increasing the applied V_G.

In case of a bridge configuration of the VSI these delayed turn-offs can cause cross conduction even to the point of both phase leg devices' destruction.

Another possibility of improper turn-off comes from already described *Miller effect*. When the V_{GD} voltage starts to rise, a displacement current can

flow across the C_{GD} through a gate resistor R_G, generating voltage capable of turning the MOSFET back on. This is another problematic state in a bridge configuration.[19]

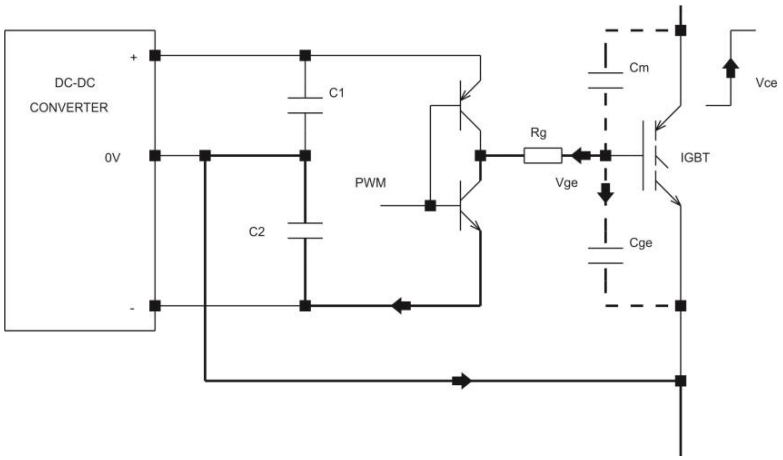


Figure 2.5: Schematic illustrating *Miller*-induced turn-on.[19]

A negative drive voltage for turn-off is desirable to keep V_G low and consequently allow to exploit a fast switching action of the MOSFETs.

2.3.3 IGBT

IGBTs are a functional combination of the previously described BJT and MOSFET.

While having a high-impedance control terminal, allowing for a high switching speed, typical for MOSFET, it takes a low saturation voltage drop from the BJTs which help it in limiting the conduction losses.

Both turn-on and turn-off mechanisms are therefore identical to the MOSFET. While the on-loss is set by the saturation voltage characteristic $V_{CE} = f(I_C, \tau, \ldots)$, instead of the MOSFETs' $R_{DS(on)}$.

2.3.4 Thyristors

Controllable thyristors are also usable for a VSI implementation. Relative to previously described devices, they allow controlling powers well into megawatt range but without capability for a fast switching found in transistor-based semiconductors.

Driving of the *GTO* thyristors also require complicated circuitry to facilitate safe turn-off, a requirement which has been largely removed by the *IGCT* thyristors.

Their large power capability is therefore exploited only in heavy traction (e.g. trains) or a power transmission devices.

2.3.5 DC-link capacitors

The DC-link capacitors are a critical part of the VSI.

Their function is to provide a low-impedance path for a switching currents and by this attenuating overvoltage spikes, eliminating voltage drops on the DC-link input and reducing ripple current causing excessive EMI.

DC-link capacitors should also be equipped with a *discharge circuit*, removing stored charge from the capacitors after battery unplugging to alleviate any danger to the possible maintenance.

2.4 Motor controller

The motor controller aggregates functionality needed to govern a motors' function.

They contain power electronic stage needed to convert battery-supplied electric energy into electric energy accepted by the AC motors of the vehicle to facilitate their function. In order to perform this conversion they must implement a control strategy with needed interfaces for measurement of various quantities needed for selected control.

Following sections will describe individual blocks in detail.

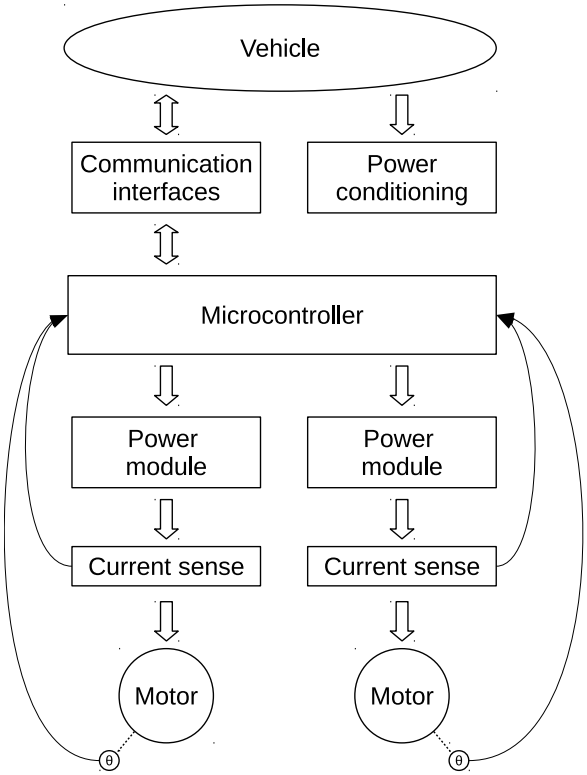


Figure 2.6: General architecture of the eForce's motor controllers.

Single motor controller in eForce's vehicles usually drives a complete axle, necessitating to provide control for 2 motors simultaneously. By having four motors in vehicles, a two motor controllers are required per vehicle.

Reason for driving two motors from single controller is to reduce overhead from duplicating needed circuitry for any vehicle unit (communication bus, low voltage power stage) and to prevent mutual interference from a separate but closely-positioned switching power stages, which occurred in motor controllers of the second vehicle generation.

2.5 Control algorithms & strategies

The motor controller strategies are tasked with controlling the parameters of the individual components within the motor controller in order to facilitate function of the connected motor(s).

These algorithms are usually implemented in the embedded micro-controller, thanks to the spread of fast and affordable computing power.

The AC motor control strategies can be split into scalar control or vector control methods.

2.5.1 Scalar control methods

Scalar control, also called *V/Hz* or *U/f* is the simplest AC motor control method, applicable primarily on induction motors, giving ability to control motor's angular velocity by setting the generated output frequency with relation to the generated flux. It is suitable for a testing or a low-end applications without need for a dynamic control.

This control do not require any measurements and is therefore considered as an open-loop control method.

The AC motors' rotating speed is dependent on the voltage vector frequency and a motor construction (number of pole pairs), as described by the following equation

$$\omega = \frac{2\pi \cdot f}{n_{pp}} \tag{2.4}$$

alternatively for rotations per minute

$$n = \frac{60 \cdot f}{n_{pp}} \tag{2.5}$$

The scalar control's input is a requested angular velocity. This velocity is translated into the frequency by above equations and fed into integrator to obtain instantaneous angle of the voltage vector.

Voltage vector magnitude is obtained from a requirement to keep the motor flux constant, which is expressed by the following relation

$$\Phi \approx \frac{U}{f} \stackrel{!}{=} \text{const} \tag{2.6}$$

leading to the linear expression for the voltage

$$U = k \cdot f \tag{2.7}$$

where k is a constant representing machine's flux. This leads to a following voltage-frequency dependency.

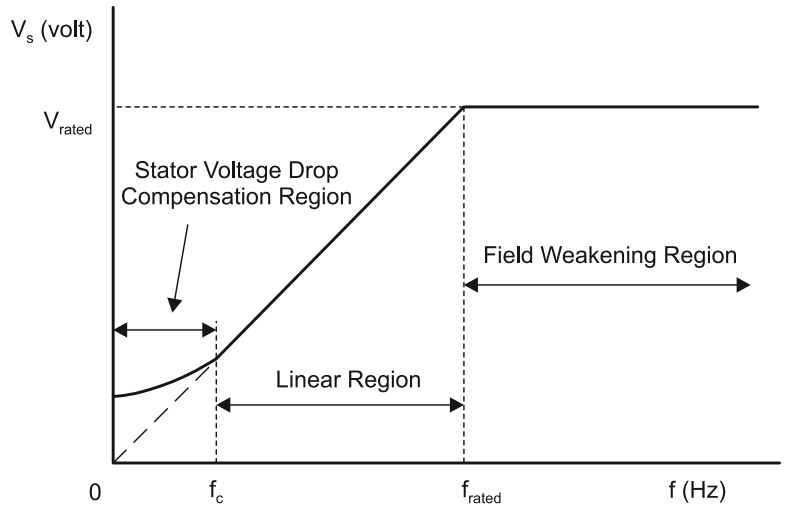


Figure 2.7: Voltage-frequency plot of the described scalar control.[20]

In the frequency close to the $f = 0$Hz a voltage must be compensated for by setting a higher voltage in order to generated flux needed to allow for a motor start-up.

If an application requires a higher rotational speed than the voltage supply allow, a further increase in frequency will lead the machine into a field-weakening region in which the torque sharply drops due to a reduced magnetic flux.

Both angle from the integrator and calculated voltage are fed into a modulator, which generates switching patterns for motor controller's power electronics.

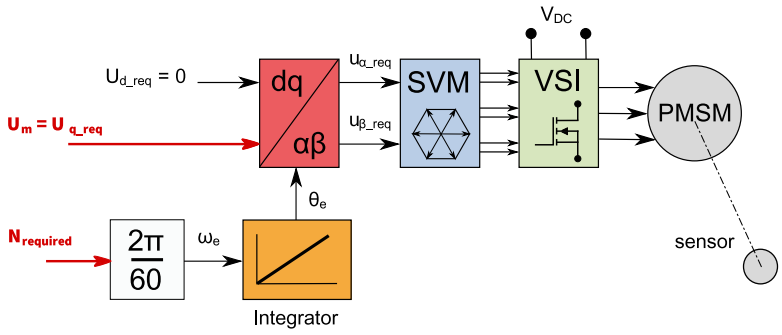


Figure 2.8: Block schematic of the described scalar control.[21]

Applications utilizing synchronous machines must be provided with an angular position sensor in order to allow for a synchronization of the voltage vector with the rotor flux. Operation without angular sensor is still possible albeit only at low speeds and without significant loads, leaving this control strategy viable only for a simple testing.

More information on scalar control can be found in a J. Sixta's bachelor thesis[22] detailing design and development of a motor controller utilizing

this control strategy.

2.5.2 Vector control methods

The vector control methods rely on mathematical transformations to transform motor quantities into vector form.

There are two major transformations used to perform these conversions, first one is the *Clarke transform*.

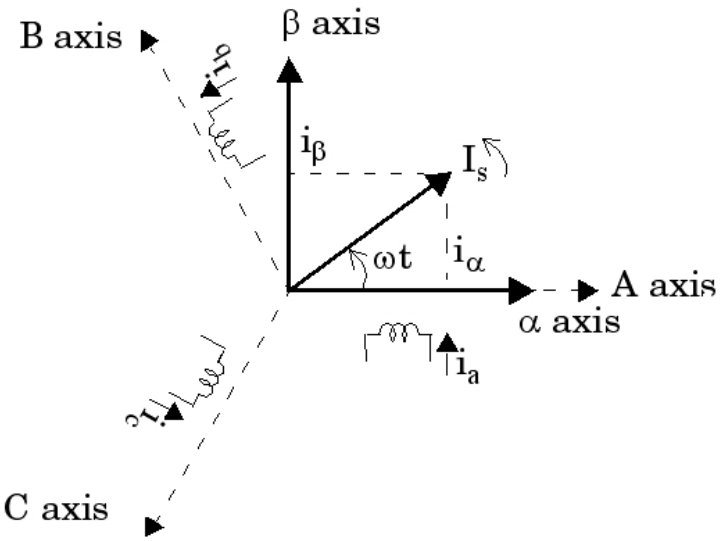


Figure 2.9: Illustration of Clarke transform performed on 3-phase system.[23]

Clarke transformation takes an arbitrary phase count quantity in rotating frame (current, flux, voltage) and transforms them into orthogonal system in a same rotating frame. Clarke transform for a 3-phase system is following

$$\begin{pmatrix} a_\alpha \\ a_\beta \\ a_0 \end{pmatrix} = k_T \cdot \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \cdot \begin{pmatrix} a_a \\ a_b \\ a_c \end{pmatrix} \tag{2.8}$$

where $a_{\{a,b,c\}}$ are arbitrary phase quantity, the $a_{\{\alpha,\beta\}}$ are transformed phase quantities. a_0 is associated with unsymmetrical input 3-phase system, in case of a balanced system $a_0 = 0$.

k_T is a transformation constant, used to set transform into invariant forms by following constants

- $k_T = 1$ – physical unit conserving transform
- $k_T = \frac{2}{3}$ – vector magnitude conserving transform
- $k_T = \sqrt{\frac{2}{3}}$ – power conserving transform

An inverse Clarke transform can be also defined by following equation, with respective transformation constants becoming inverse.

$$\begin{pmatrix} a_a \\ a_b \\ a_c \end{pmatrix} = k_T^{-1} \cdot \begin{pmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{pmatrix} \cdot \begin{pmatrix} a_\alpha \\ a_\beta \\ a_0 \end{pmatrix} \tag{2.9}$$

The Clarke transform can be further simplified by considering a balanced system and to work with only 2 measurements of quantities which is a commonly used transform variant in motor controllers.

Second used transformation is the Park transform, taking a transformed system from Clarke transform in a rotating frame and transforming it into a different rotating frame. The commonly used rotating reference frames in motor control are following.

- $\alpha\beta 0$ – stator reference frame
- $dq0$ – rotor flux reference frame
- $kl0$ – rotor reference frame

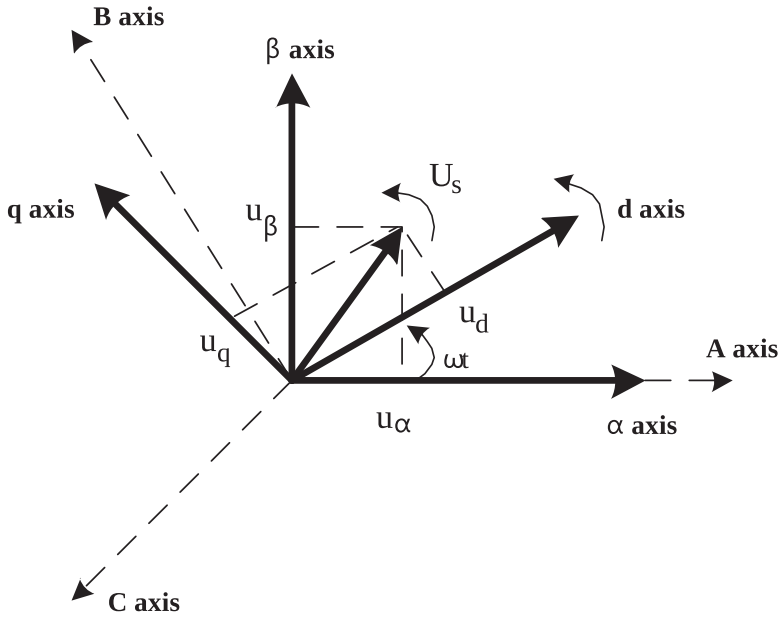


Figure 2.10: Illustration of Park transform in a $\alpha\beta 0 \rightarrow dq0$ form.[24]

Equations for the Park transformation in a general reference frame $xy0$, rotating at the angular velocity ω of instantaneous angle θ between $\alpha\beta 0$ and $xy0$ reference frames ($\alpha\beta 0 \rightarrow xy0$) are

$$\begin{pmatrix} a_x \\ a_y \\ a_0 \end{pmatrix} = \begin{pmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} a_\alpha \\ a_\beta \\ a_0 \end{pmatrix} \tag{2.10}$$

and for inverse Park transformation ($xy0 \rightarrow \alpha\beta0$)

$$\begin{pmatrix} a_\alpha \\ a_\beta \\ a_0 \end{pmatrix} = \begin{pmatrix} \sin(\theta) & \cos(\theta) & 1 \\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 1 \end{pmatrix} \cdot \begin{pmatrix} a_x \\ a_y \\ a_0 \end{pmatrix} \tag{2.11}$$

Field oriented control

The Field oriented control (or Vector control) is capable of controlling both machine's flux and torque. Its direct form was first described in early 1970s by F. Blaschke.

Field oriented control can be further split into direct and indirect forms, depending on which methods were used in acquiring the rotor angle.

This is achieved by performing both previously mentioned transformations on two selected phase currents and a known rotor position, in order to acquire currents in $dq0$ rotor flux frame for synchronous machines, or $kl0$ rotor frame for induction machines which must be adjusted for slip angle to acquire $dq0$ frame currents. This operation is called *decoupling*.

Reason for this is to convert AC motors' torque control into a torque control similar to the separately excited DC motor control, whose instantaneous produced torque is described by following equation

$$T_e(t) = k \cdot \phi(t) \cdot i_a(t) \tag{2.12}$$

where Φ is an excitation magnetic flux and I_a is the armature current. The instantaneous torque relation for transformed AC motor is

$$T_e(t) = \frac{3}{2} n_{pp} \left(i_q(t) \cdot \phi_d(t) - i_d(t) \cdot \phi_q(t) \right) \tag{2.13}$$

for a synchronous machine with permanent magnet excitation, the second part of the equation can be considered zero. Final equation for the transformed torque becomes

$$T_e(t) = \frac{3}{2} n_{pp} \cdot i_q(t) \cdot \phi_d(t) \tag{2.14}$$

this torque equation is now roughly equivalent to the separately excited DC machine one, allowing to use a same regulator structure.

To control the machine's torque, these currents are subtracted from set references, acquiring current errors which are fed into current regulators. Both regulators provide a voltage request in dq frame on which the inverse transformations are performed to obtain individual phase voltage requests.

These phase voltages are finally sent to the modulator which provides switching times for the VSI.

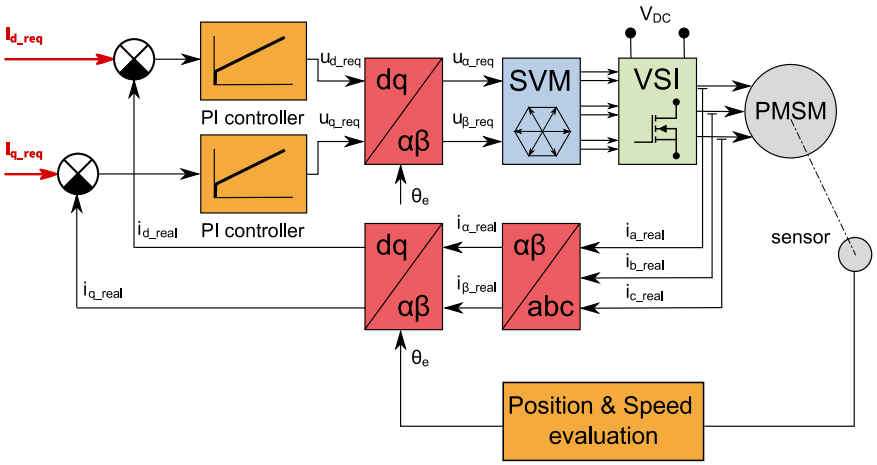


Figure 2.11: Block schematic of the described field oriented control.[21]

The described control allows for a highly dynamic performance with capability of full motor torque at standstill. Dynamic performance is limited by the bandwidth of used components (current measurement) and subsequent current regulators.

Vector control on the other hand requires a precise rotor position reading in order to properly decouple the torque and flux in the measured machine's currents and to generate a valid modulation vectors.

Direct torque control

Unlike previously described vector control, the direct torque control in its unmodified form can be used only with asynchronous motors and therefore will be described only in brief.

Direct torque control was first described in the 1980s separately by M. Depenbrock's patent[25] as a *Direct sef-control* and I. Takahashi & T. Noguchi's article[26]. Currently most DTC implementations follow the I. Takahashi and T. Noguchi's description.[27]

The DTC also uses Clarke transformation to convert phase currents and voltages into orthogonal base but it does not perform a Park transform.

The phase currents and voltages are fed into mathematical model of the controlled motor which provides with a torque and flux information alongside with a current flux sector. The flux magnitude and orientation is obtained by integrating the voltage vector.

These signals are fed into hysteresis controllers, comparing the calculated quantities with set references and producing a sector change information in order to keep the vectors in desired tolerance bands. The controllers' outputs are fed into look-up table which selects a valid switching combination for the power electronics.

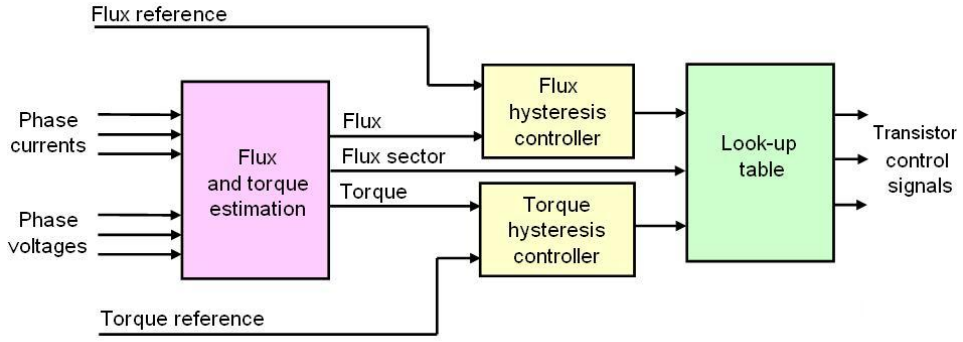


Figure 2.12: Direct torque control simplified block diagram.[27]

DTC can provide even higher dynamic performance than the FOC thanks to not using any complex regulators.

Switching frequency of the power elements is variable thanks to having to switch only when vectors diverge from required tolerance band. It can be controlled by specifying width of the tolerance band. On the other hand, it cannot be used with synchronous machines due to not being synchronized to the machine's rotor position. This can be alleviated by modifying the control by discarding its lookup table for a space vector modulator.[28]

2.6 Control electronics

Control electronics of the motor controller is tasked with implementation of selected control strategy with need to provide conditioned power supply, communication interfaces, sensor interfaces and switching pulses.

2.6.1 Embedded micro-controller

The micro-controller (MCU) contains a program, implementing selected control. Current micro-controllers contain various of peripherals which help in motor controller design.

Most commonly used peripherals are timers which are capable of PWM generation in order to trigger switchable components in the VSI.

Analog-to-digital converters are used for phase current or angular sensor reading. Digital-to-analog converters are commonly utilized for debugging or special sensor excitation.

Communication interfaces embedded directly in the MCU allow to reduce bill-of-materials needed to implement communication with superior control systems.

2.6.2 Phase current sensing

Current sensing is critical in order to be capable to govern torque generated by the electric machines. Commonly used measurement strategies are either based on magnetic or resistive sensing.

The magnetic sensors utilize a magnetic field generated by flowing current through conductors. The magnetic sensors utilize Hall effect in which the conductor's magnetic field is captured by a magnetically permeable core. This magnetic field is applied transversely to a hall sensor on which a Hall voltage is generated. This voltage is conditioned and filtered in order to output a current reading.

While being a non-invasive and inherently galvanically separated from measured conductor, they are plagued with a low measurement bandwidth and if not properly compensated for, with a significant offset drifts.[29]

Resistive measurement of the currents rely on a voltage drop done by current passing through resistance, governed by Ohm's law. By using a precisely manufactured resistors made from thermally stable compounds (e.g. Manganin or Constantan) offering a low resistance drift with temperature a high precision can be obtained.

Problems arise with needed galvanic isolation of the measurement and losses incurred by Joule losses. The galvanic separation can be nowadays ensured with various means, by either use of isolation amplifiers or with an isolated delta-sigma modulators.[30]

2.6.3 Angular position sensing

To perform a *decoupling* needed for FOC's torque control, described in previous section a precise rotor position must be known.

Again, there are various sensor types, usually utilizing optical or magnetic means of operation. The design will describe a *resolver* which is an absolute position sensor mounted in all of our vehicles' motors.

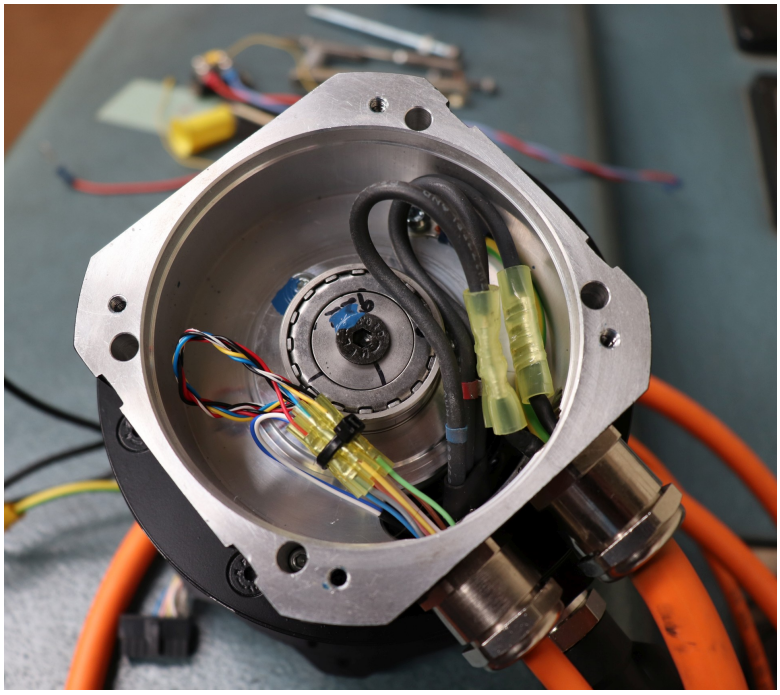


Figure 2.13: Photograph of a resolver attached to the motor's shaft.

The resolver is an electrical machine, very similar to a transformer. The primary winding is placed on the stationary part of the resolver. It transfers a high-frequency (kilohertz) sinusoidal excitation signal to the rotating part of the resolver. Excitation signal can be described mathematically as

$$u_{exc}(t) = U \cdot \sin(\omega t) \tag{2.15}$$

where ω is the excitation's signal angular frequency.

On the rotating part, either a winding is placed which first receive the excitation signal across the air gap, transferring it to a secondary winding – brushless resolver. Or by using a special shape of the rotor, on which the winding is not necessary – a variable reluctance resolver.

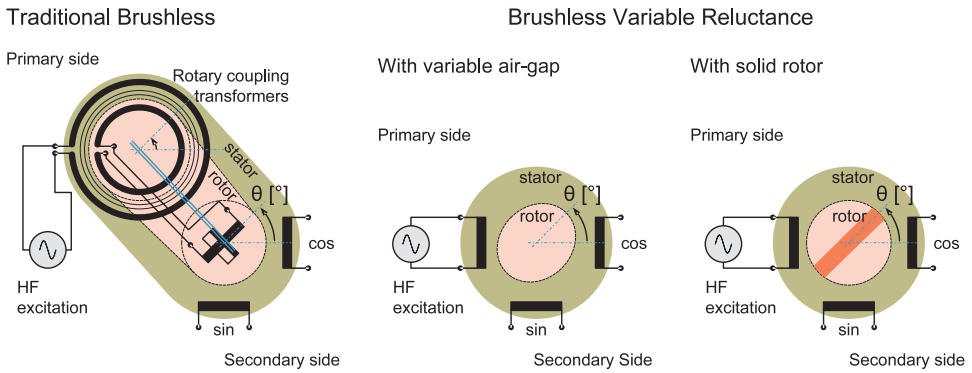


Figure 2.14: Illustration of various resolver constructions.[31]

Back on the stationary part, a two secondary windings are present with a 90° electrical angle displacement. They are called sine and cosine winding and their voltage relations can be expressed with following equations

$$u_{sin}(t) = T \cdot \sin(\omega t) \cdot \sin(\theta(t)) \tag{2.16}$$

$$u_{cos}(t) = T \cdot \sin(\omega t) \cdot \cos(\theta(t)) \tag{2.17}$$

taking from these relations a resolver can be considered as a modulator which superpose a sine and cosine of the shaft angle onto an excitation signal $\sin(\omega t)$ with a certain transformation ratio T.

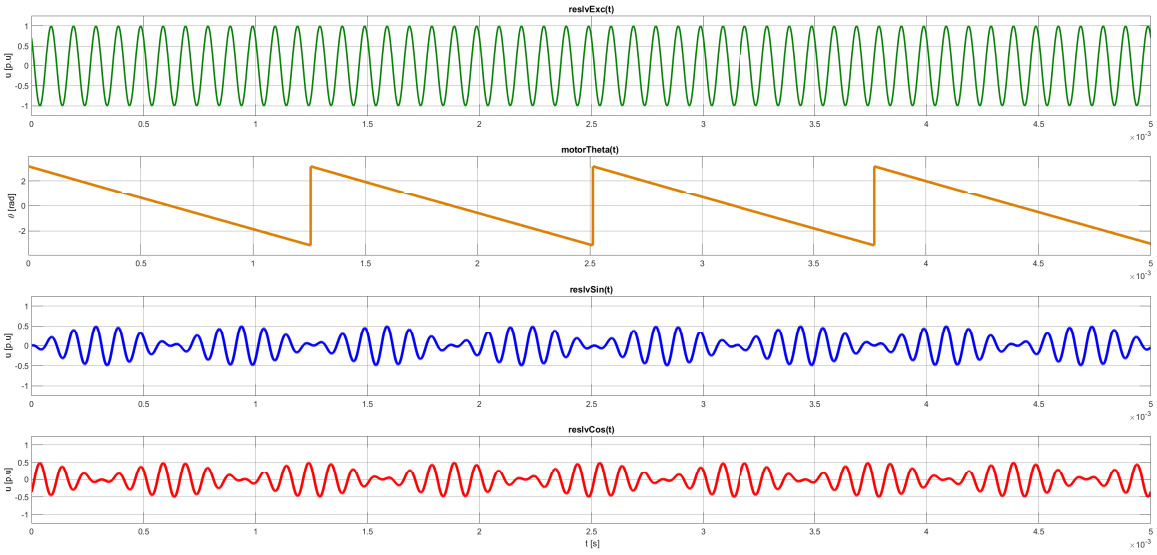


Figure 2.15: Example of resolver's signals with respect to the excitation and angle.

Resolver angle can be obtained by sampling the resolver's sine and cosine signals, demodulating the carrier excitation and applying an arctan function to these signals. This is only a rudimentary operation, prone to noise distruption. Therefore, an *angle tracking observer* (ATO) is used to obtain a noise-free information from the resolver.

The ATO is consists of a phase-locked loop with input signal filtering to obtain precise angle and angular velocity by estimation from measured resolver data. The exact theoretic treatment of the ATO is out of this thesis' scope, but can be found in [32] or [33].

Chapter 3

Motor controller power electronics

The power electronics circuit board is placed directly on the power modules. It facilitates isolation of the power supply and control signals for the power modules, phase currents measurement, DC-link capacitors housing alongside with their discharge and voltage measurement circuitry.

Power electronics board encompasses following functional blocks. Each block will be discussed further in the text.

- Intelligent power modules.
- Phase leg drivers.
- Shunt-based phase currents measurement.
- DC-link
  - low voltage power supply
  - capacitors
  - voltage measurement
  - discharge circuitry
- High power connectors.
- Control board interface.

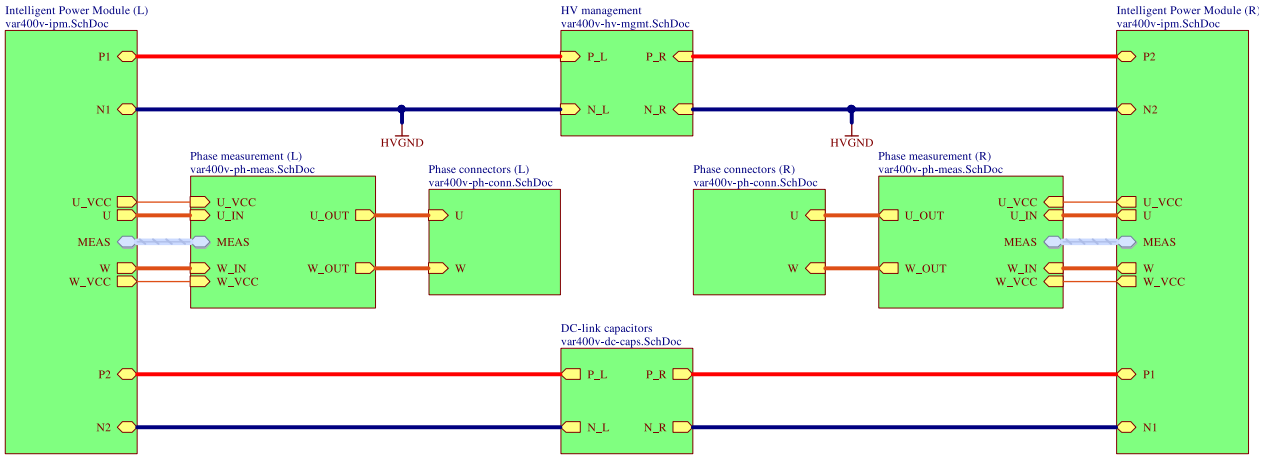


Figure 3.1: Top level schematic diagram of the motor controller's power board.

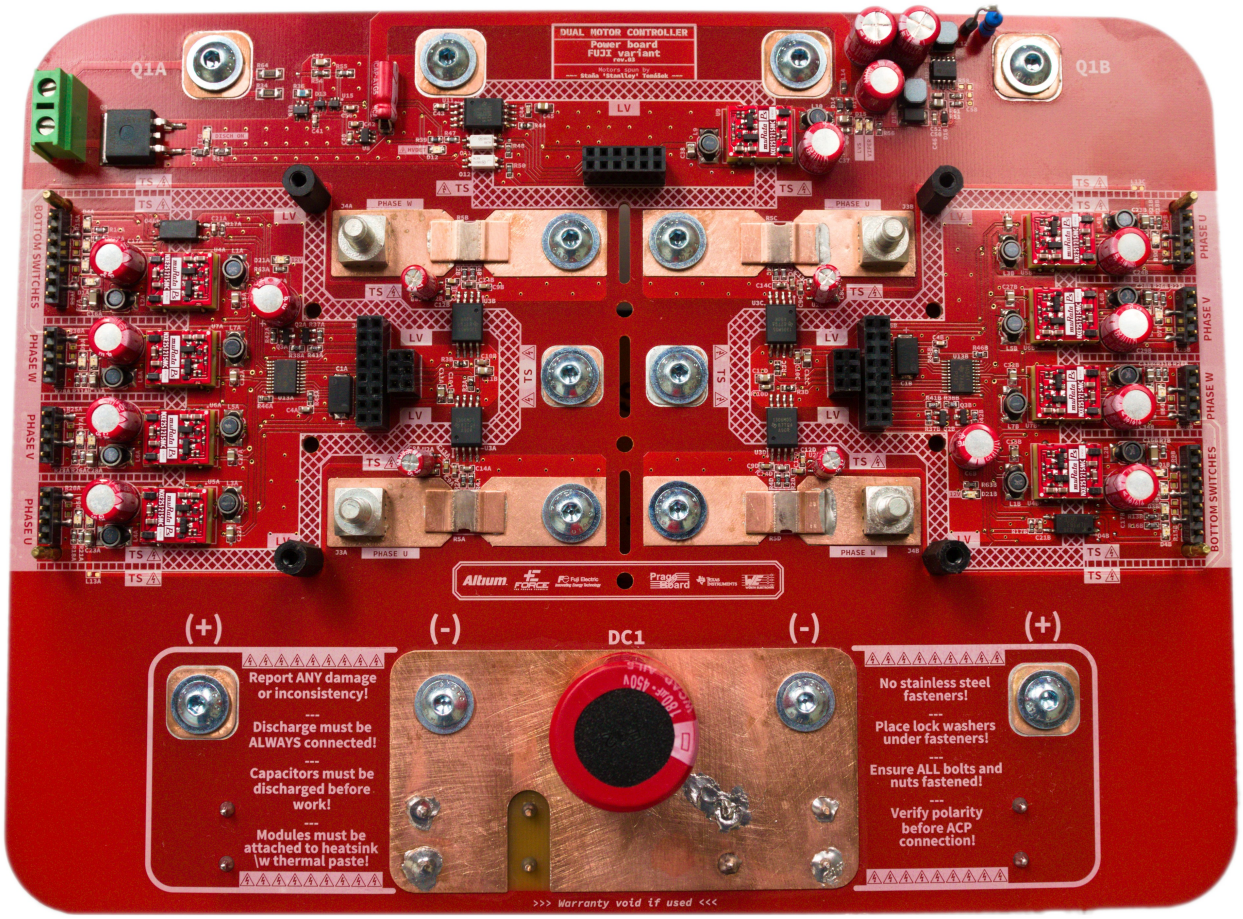


Figure 3.2: Motor controller's power board.

3.1 Intelligent power modules

The mainstay of the motor controllers' power electronics part are undoubtedly the power modules. The design uses the *6MBP300VEA060-50* intelligent power modules manufactured by the *Fuji Electric*.

Main advantage of these modules is that they already contain a power driver stage of the IGBT transistor switches alongside with the thermal, desaturation, overcurrent, deadtime and supply voltage protections.

The data sheet allows input voltages up to 600 volts, therefore voltages on the DC-link can reach up to 400V[1] with a continuous peak current values of 300 amperes and tolerance of a short spikes[2] up to 600A. The contorl circuitry requires only unipolar 15V power for both upper and lower drivers. [34]

The manufacturer uses same package for power module versions with 1200V-capable silicon. This would allow reaching maximum allowed tractive system voltage of the Formula Student competition without significant modifications in the current motor controller design.

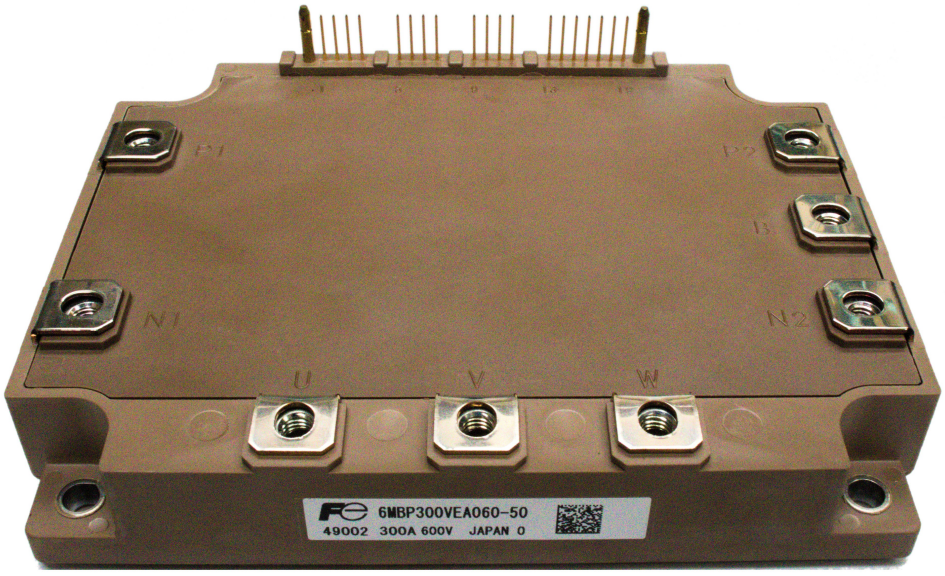


Figure 3.3: Photograph of a used power module.

3.2 Phase leg drivers

Thanks to the integration of IGBT drivers into the power modules, the design only needs to address the galvanic isolation requirements of drivers' power supplies and control signals. Both upper and lower drivers of the IGBT transistors must be galvanically isolated from both other phases and motor controller's low voltage systems.

[1] safety factor 1.5
[2] 1ms

3.2.1 Power isolation

Power isolation is accomplished by a *NXJ1*[35] isolated DC/DC converters and *NXE2*[36] for bottom IGBT driver respectively. Selected converters can provide up to 1 watt (converters used for bottom drivers up to 2W) power output at 15V with 12V input voltage.

To maintain simplicity of the design, the converters are push-pull based without a feedback signal across the isolation. This results in a minimal loading requirement (10% of the specified current) to maintain the output voltage in a defined range.

Primary selection characteristics for these components were an extremely low isolation capacitance, high isolation voltage rating and a broad isolation gap of the components' packaging while keeping the component low-profile. The cost of the component is also lower against the competitor products of comparable parameters. This led to a scarcity of the component on the market.[3]

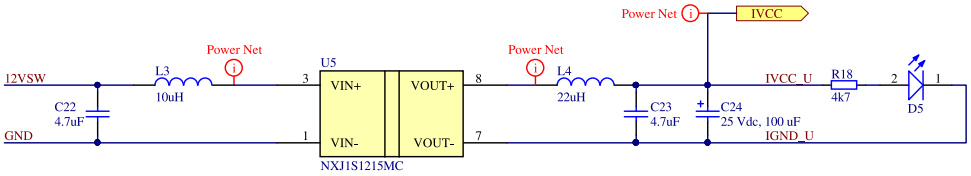


Figure 3.4: Schematic of a single 1W isolated DC/DC converter implementation.

The implementation of said converters into motor controller's design was inspired directly from the provided datasheets. Both input and output filters are not mandatory for devices' function, but they should prevent excessive EMI conduction and radiation into other circuitry and also to reduce output voltage ripple.

The components' parameters were selected with respect to the expected current flow, present voltage with safety margin and datasheet's guidelines. Aluminum polymer-based bulk capacitor will provide an ample charge reserve, coupled with capacitors' low ESR rating. This will help to maintain a steady voltage in the driver circuit.

3.2.2 Gate signal isolation

Power modules' application note[37] specify usage of the *HCPL-4505 optocoupler*[38] to properly isolate the gate drive signals.

The current trend in the high speed / high power signal isolation is to abandon optical isolators in favor of the digital isolators. Main reasons for this are lower cost, lower power consumption and higher signaling rates compared to the optical isolators.

[3] Due to these availability problems, the *NXJ1* DC/DC converters were drop-in replaced by the *NXE2* DC/DC converters in FSE.08's motor controllers.

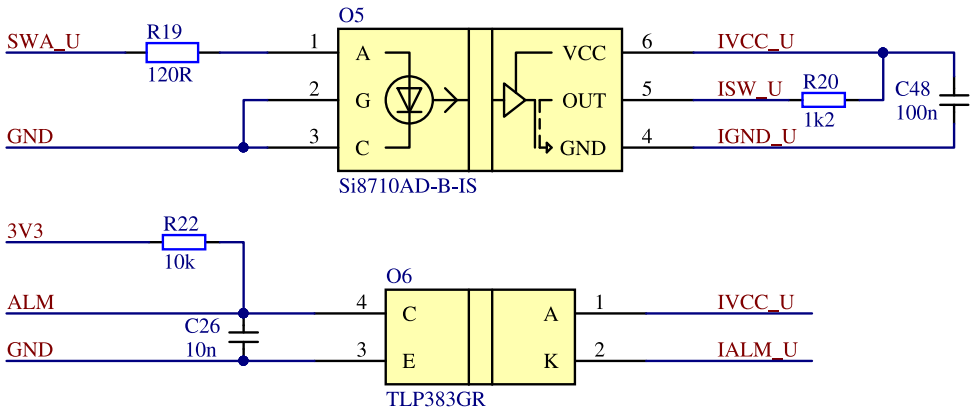


Figure 3.5: Schematic of a single IGBT channel signals isolation.

3.3 Shunt-based phase currents measurement

As per theory, electric motors require measurement of (phase) currents for precise torque control regardless of selected control strategy. Three phase AC machines with symmetric machine assumption (3.1) need to measure two of the phase currents to properly reconstruct the third current.(3.2)

$$i_a(t) + i_b(t) + i_c(t) = 0 \tag{3.1}$$

$$i_c(t) = -i_a(t) - i_b(t) \tag{3.2}$$

To measure phase currents using shunts a number of considerations must be addressed. Firstly, selection of shunts themselves must reflect expected phase current alongside with required shunt dropout versus dissipated power (Joule losses) into consideration. This is a design trade-off between measurable signal levels (3.3) and dissipated heat from the shunt.(3.4)

$$U_{sh} = I_{ph} \cdot R_{sh} \stackrel{!}{=} \max \tag{3.3}$$

$$P_d = I_{ph}^2 \cdot R_{sh} \stackrel{!}{=} \min \tag{3.4}$$

Next step is to select a signal acquisition and isolation method. Due to using a high side (floating) shunt measurement, the isolator's common mode transient immunity characteristics must respect used power semiconductors' switching slew rates. This is a primary reason why isolated amplifiers are not suitable for this measurement method due to ease of switching noise's coupling into shunts' low-level analog signal.

Therefore, a progressive method using an isolated sigma-delta modulator was chosen for motor controller design. The analog front-end alongside with analog-to-digital converter circuitry is positioned on the shunt's isolated side. Shunt's dropout voltage is converted using sigma-delta modulator into a high frequency, 1-bit digital signal. This signal is afterwards sent across the isolation barrier, alleviating the concerns for any interference on modulated analog signal.

Digital signal is then freely routed across the device to a micro-controller containing suitable *sinc* digital filter which decimates the high frequency 1-bit digital signal into lower frequency, multiple-bit signal. Other methods of 1-bit stream processing are higher-order analog filters or a 1/0 counters which are frequently used in fast, non-programmable over-current detection circuits.

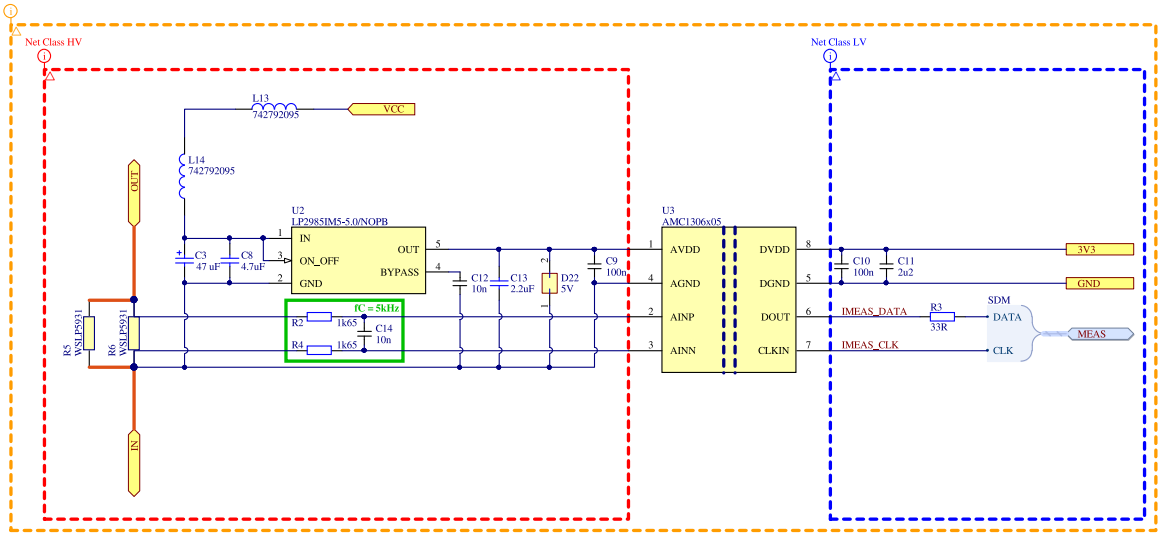


Figure 3.6: Schematic of a single phase current measurement.

Implementation of the shunt-based phase current measurement relies on two parallel-connected shunts `R5` and `R6` manufactured by *Vishay Dale* of a total resistance 150μΩwith a combined 20 watts of maximum allowed power dissipation. These resistors are manufactured from a thermally stable alloy whose declared resistance drift is below 20ppm/°C. Total declared component's drift with leads is 175ppm/°C. Additional drift can be expected from the soldering and the copper reinforcement on the circuit board.

Shunts' signal bandwidth is limited in order to suppress switching noise influence using a first order differential RC filter consisting of `R2`, `R4` and `C14`. This signal is converted to 1-bit stream using an *AMC1306* isolated sigma-delta modulator with a full scale, bipolar conversion range of ±50mV with declared output precision of 13.6 ENOB at 78kSPS.

The modulator itself contains signal isolation circuitry to allow for a compact measurement solution. Device's isolation specifications are very generous and allow working voltage up to 1500V. Modulator also contains a circuitry allowing detection of a missing power supply in order to prevent erroneous control actions.[39]

Other versions of the device posses built-in low-drop regulator, negating a need for an external one at the expense of a larger integrated circuit package.[4] Some versions employ LVDS or a *Manchester coded* signalling to improve signal integrity and reduce EMI problems of a pure CMOS signaling. While both being sound prospects for a modern motor controller, the used

[4] *AMC1304*

micro-controller does not posses a LVDS interfaces or a Manchester decoding interface of a sufficient throughput.

Power to properly operate the modulator is taken from the upper IGBT driver isolated DC/DC converters. Due to a long traces needed to route the power from control circuitry to the shunts a two chokes `L13` and `L14` were added to both beginning and end of the power carrying trace to suppress any noise and to decouple switching DC/DC supplies from sensitive modulator. To keep the supply voltage in a proper levels an electrolytic capacitor `C3` of an adequate capacity is used to stabilize decoupled voltage.

Filtered input voltage is then reduced to the modulators' acceptable levels by using a low-dropout regulator `U3`. The ceramic capacitors `C8` and `C13` are required for stability of the regulator. Capacitor `C12` serves to further improve regulation and noise suppression capabilities of the device. Suppressor diode `D9` is a protection measure to prevent ESD-related damage to the device, which was a concern in the prototype version of the power board.

3.4 DC-link capacitors and circuitry

The DC-link section of the motor controller's power board encompasses capacitors themselves, measurement of both exact and safe voltages, discharge circuitry and power stage.

3.4.1 Low voltage power supplies

The DC-link's power stage's primary objective is to provide power to operate auxiliary circuitry.

The 15V rail used to power discharge IGBT is derived from 2 distinct DC/DC converters. This is to allow for a DC-link domain function even without vehicle's low voltage power supply availability and to provide a certain level of redundancy.

First converter is the isolated DC/DC converter of already discussed *NXJ1* series. Its input power is derived directly from the motor controller's internal 12V rail and functions autonomously alongside the vehicle's low voltage supply.

Second converter is a *STMicroelectronics* manufactured *VIper01* series high-voltage switching mode power supply. Alongside being a SMPS, the component incorporates a high-voltage start-up circuitry with a MOSFET semiconductor switch of $800V_{DS}$ breakdown rating, allowing it to function directly from the tractive system voltage levels. While its primary purpose is to act as a start-up source for a mains-powered flyback converters, it can be easily converted to a self-powered step-down converter configuration. Start-up procedure of the DC/DC converter alongside its reference schematic for a self-powered application is detailed on the figures below.

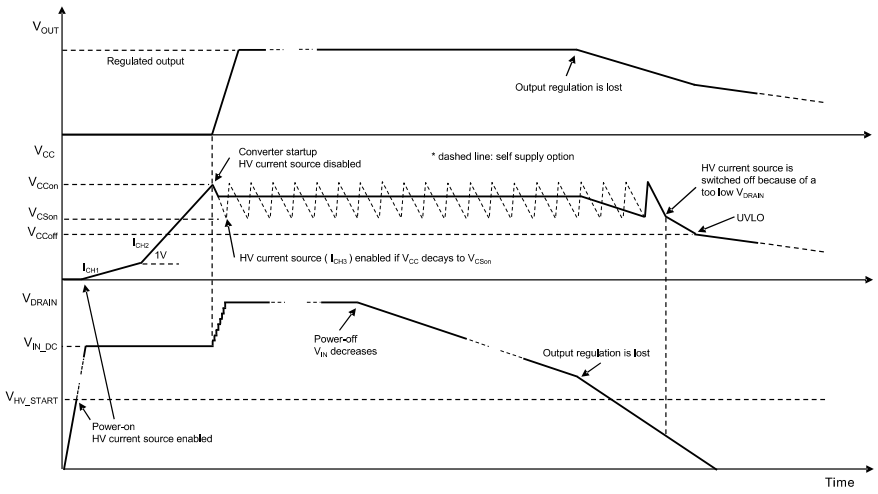


Figure 3.7: Diagram of the *VIper01* integrated circuit high voltage start-up, operation and turn-off.[40]

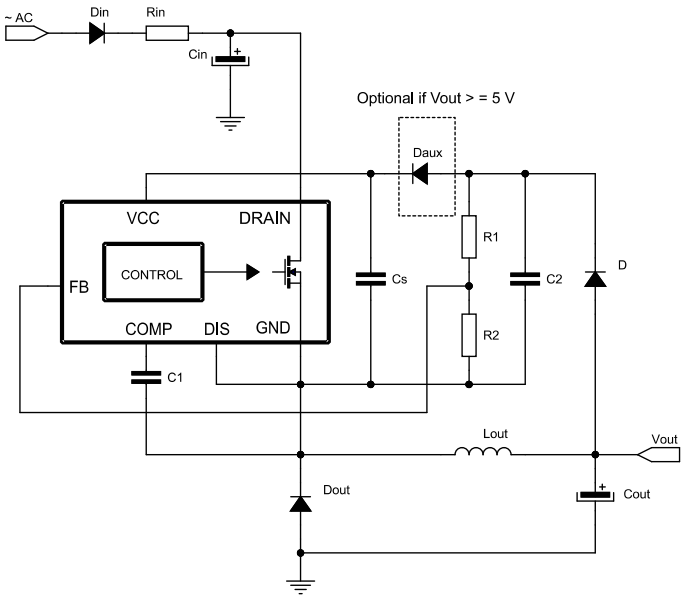


Figure 3.8: *VIper01* in a self-powered buck converter configuration.[40]

Converter's internal high voltage start-up source begins its operation at 18V threshold voltage V_{HV_START}. The high voltage supply starts after passing this threshold and supplies current which gradually charges the C_S capacitor. After reaching V_{CCon} threshold, the start-up regulator is turned off and the integrated circuit will begin its regulation of the output voltage by switching the internal MOSFET.

In case of the self-powered configuration, the C_S capacitor is constantly discharged by the device's operation. It must be periodically recharged by restarting the high-voltage power source after reaching the V_{CSon} voltage in order to keep the chip working.[40]

Motor controller's design uses a following implementation based off the manufacturer's application note.[41]

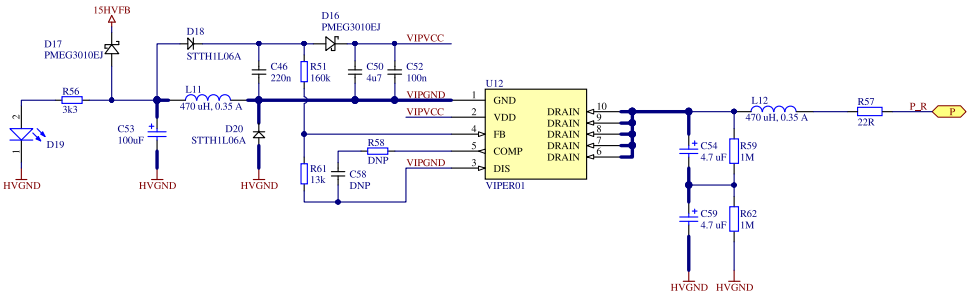


Figure 3.9: *VIper01* circuit implemented in the DC-link domain power stage.

The input of the device is protected by resistor `R57` with a silicon diode[5]. Inductor `L12` with capacitors `C54` and `C59` serve as a switching noise filter and a bulk capacity for the device's operation. Resistors' `R59`,`R62` purpose is to equalize voltage on the serially connected, input bulk capacitors. Capacitors `C50` and `C52` store charge needed for device's operation from the high-voltage start-up source, being equivalent to the C_S component of the reference.

Inductor `L11` and aluminum polymer capacitor `C53` are output components of the SMPS. `D20` is a Schottky diode for current flow direction during MOSFET switch being off. Diode `D16` allows for recharging of the C_S capacitor from the SMPS' output.

Resistors `R51` and `R61` attenuates output voltage for input to the device's error amplifier, setting the output voltage level at 16V. `R58` and `C58` can be used for further tuning of the regulator's closed loop response, they are not fitted on the current board revision.

Output diode `D17` is used to OR *VIper's* output with the *NXE1*.

3.4.2 Capacitors

DC-link capacitors are used to stabilize input voltage to the IGBT modules. As per theory the capacitors' role and consequently configuration is twofold.

First is to provide readily available power supply/sink for switching semiconductors. This is accomplished by using multiple film capacitors of *C4AQ* series manufactured by the *Kemet*.

Film capacitors are generally prominent by their low ESR/ESL rating, giving them capability to deliver/absorb massive current spikes[6] without heating or damage.

While their negligible parasitic characteristics are effective for a fast charge delivery, they can cause significant problems when coupled with parasitics of the vehicles' accumulator pack and input leads by emergence of resonant circuits.

[5] not explicitly drawn in the schematic

[6] used components allow up to $336A_{pk\text{-}pk}$ and $16A_{rms}$ at 10kHz

In order to suppress resonant behavior of described circuit, a secondary electrolytic capacitor is added in parallel to the film capacitors in order to raise series resistance of the motor controllers from the accumulator's point-of-view, therefore reducing resultant resonant circuit's Q factor. For this purpose a single[7] radial electrolytic capacitor from *Würth Elektronik* with declared capacity of 150µF.

The capacitor dimensioning was done by two methods. First method was to ensure reasonable voltage drop during switching and a ripple current capability of the capacitors. Design methodology and used equations are described in following article[42]. Second calculations were performed to ensure resonance-free operation. This is described in the Miroslav Rýzek's master thesis[6].

Argument may arise to size the DC-link capacitors' total capacity (capacitive reactance) to an amount which will not resonate at selected switching frequency. This is a plausible strategy for applications where the both power sources' and sinks' parasitic characteristics are already well-known by either precise simulation or exact measurement. Unfortunately, the team must design and construct accumulator pack in tandem with motor controller while both parasitic characteristics are unknown at the time of design and are only estimated from previous designs' measurements.

3.4.3 Voltage measurement

To increase motor control possibilities, a voltage measurement of the DC-link capacitors is often added to allow for a various control improvements e.g. power limitation or battery voltage drop compensation.

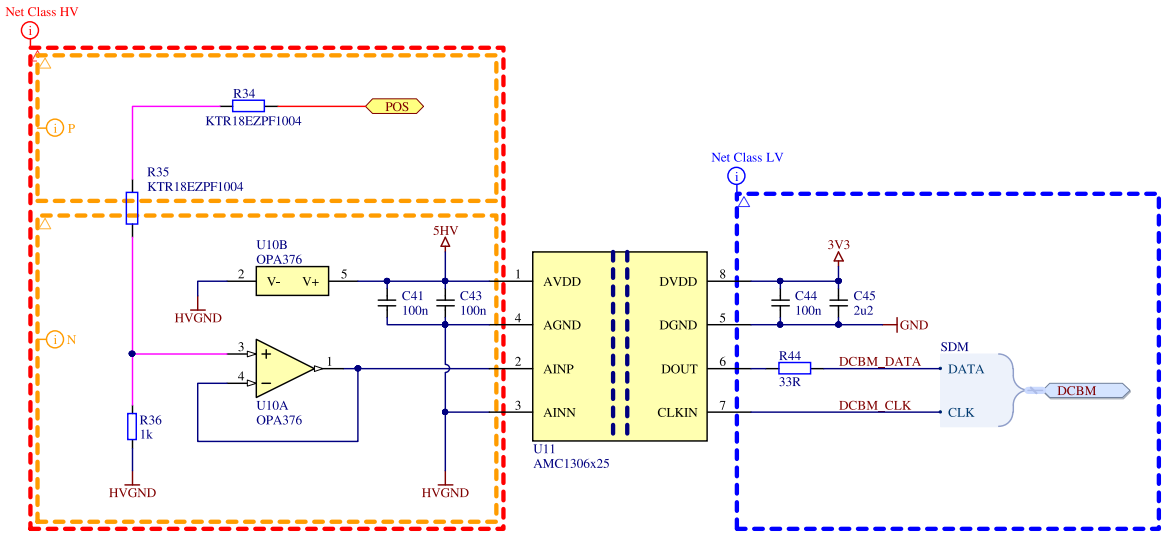


Figure 3.10: Schematic of a DC-link voltage measurement.

Measurement is realized by a voltage divider consisting of a precise, high-

[7] two in series for the 600V capable power board

resistance resistors to reduce DC-link voltages to processable levels. High-ohmic, automotive grade resistors of the *KTR18* series provide required precision coupled with a high voltage operation capability up to 500V and a standard 1206 SMT resistor housing. For the bottom divider resistor a high voltage rating is not required.

Following equation was used to set values of upper resistors in the divider.

$$U_{\Sigma\Delta(in)} = U_{DC(max)} \cdot \frac{1}{2 \cdot R} \tag{3.5}$$

$$2 \cdot R = \frac{U_{DC(max)}}{U_{\Sigma\Delta(in)}} \tag{3.6}$$

Resultant resistor value is in kilo-ohms. Two resistors in series are used to allow for better heat dissipation and 1kV capability for envisioned 600V accupack.

For the analog-to-digital conversion an already described integrated circuit *AMC1306* in its 250mV input range variant was selected.

The analog input of the circuit is not connected directly to the bottom resistor but through an operational amplifier in a voltage follower configuration. Reason for this is due to the divider resistor having comparable impedance to the input (22kΩ) of the converter. The resultant circuit will degrade the accuracy of the conversion. Voltage follower will decouple the divider's impedance from the converter.

Used operational amplifier's circuitry could be also modified to increase resolution of the measurement by doubling the divider's output voltage by biasing the operational amplifier in order to exploit bipolar conversion capability of the converter. This modification would require a bipolar supply of the operational amplifier and a precise reference for bias.

3.4.4 High voltage detector

The Formula Student rules require for a monitoring of safe voltage levels of the tractive system. Rules clearly specify that voltage must be measured in enclosures with DC-link capacitors and accumulator relay output.[EV 4.10.13] This measurement must be done strictly by hardware without any software intervention.[EV4.10.8]

To satisfy these requirements a following circuit was devised to compare the DC-link voltage against safe levels and to pass information about circuitry function.

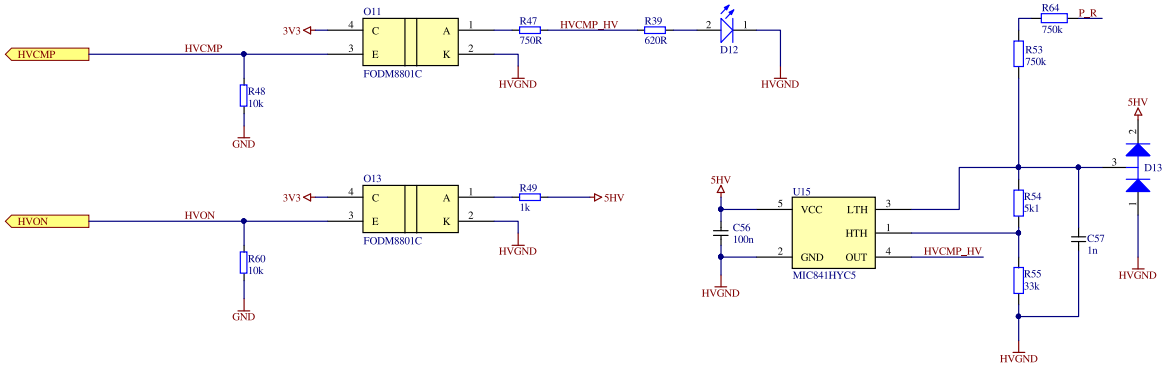
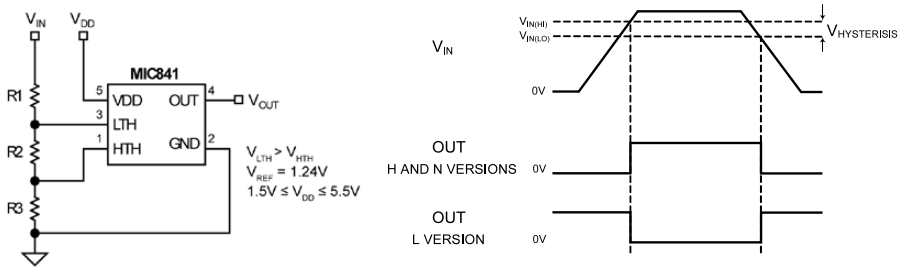


Figure 3.11: High voltage detector circuitry schematic.

The *Microchip* manufactured *MIC841*-series comparator with hysteresis is core of this circuit.[43] Hysteresis is a desirable feature for comparator to prevent output oscillations due to noise on the input pins.[44]

The DC-link capacitor voltage is first attenuated by resistive divider composed of resistors `R64`, `R53`, `R54` and `R55`. Capacitor `C57` alongside with upper resistors forms a low-pass RC filter with a cutoff frequency of 106Hz. The divider's maximum output voltage is clamped by the `D13` dual diode, preventing damage to the comparator.



(a) : Reference schematic. **(b) :** Waveforms of output configurations.

Figure 3.12: *MIC841* comparator reference material.[43]

The high and low comparator thresholds are set by the resistor values with respect to the comparator's internal reference, according to the following equations.[43]

$$\mathrm{V_{IN(LO)}} = 1.24 \cdot \frac{\mathrm{R1} + \mathrm{R2} + \mathrm{R3}}{\mathrm{R2} + \mathrm{R3}} \tag{3.7}$$

$$\mathrm{V_{IN(HI)}} = 1.24 \cdot \frac{\mathrm{R1} + \mathrm{R2} + \mathrm{R3}}{\mathrm{R3}} \tag{3.8}$$

both equations were evaluated simultaneously with 1.5MΩupper resistance to limit power dissipation, 60V high threshold to fulfill rules requirement and a 50V low threshold. Resultant component values were adjusted to fit the available resistor series in our team stockpiles, while providing rules-required high voltage level detection.

Second monitored signal is a primitive indication of a 5 volt power rail function, subsequently 15V discharge-powering power rail function. Both rails

could be fitted with the same comparators in open-drain output configuration to allow for a more precise evaluation of the voltage levels.

Both signals are transferred across the isolation barrier using the *FODM8801C* optocouplers. These parts' selection criteria were low cost, good supplier availability and solid CTR characteristic. Their function is not to relay any fast signals, nor the signals positioned on the floating potential of the IGBT gate-drivers, therefore this part selection was not strictly performance-oriented.

The receiving side of the optocoupler is a non-inverting configuration with pull-down resistors to set defined level during optocoupler off-time. Further processing of the high voltage detector signals will be discussed later.

3.4.5 Discharge

The discharge circuitry is a safety feature required to remove any charge from the DC-link capacitors during tractive system inactivity to allow for maintenance and a safe manipulation with the vehicle. It is also required and specified by the competition's rules.[EV 4.9][EV 6.1.5]

While the previous motor controller used relays to facilitate this functionality, the new design uses a N-channel IGBT. This design choice was to allow for a higher voltage on the DC-link capacitors thanks to a higher blocking voltage tolerance of the semiconductor switches without heavy cost and space investments needed for a relay of equivalent voltage tolerance. Silicon also does not suffer from stucking and allows for a much higher current flow and current breaking capability.

Primary drawback of the new solution is general nonexistence of "normally closed" semiconductor switch which would not require a nontrivial drive circuitry. The depletion-mode field-effect transistors (JFET or P-channel MOSFET) which are currently commercially available semiconductors exhibiting "normally closed" function, require negative gate voltages for a proper turn-off, defeating simplicity of a semiconductor driving.

This has led to the implementation of a high-voltage DC/DC converter to provide offline power supply, drawing power directly from the DC-link capacitors, which in turn powers the gate of the N-channel discharge switch.

Total capacity of the DC-link capacitors for one motor controller is 330μF. This capacity must be discharged below 60V within 5 seconds to comply with the rules. Following procedure was used to select proper resistor values and power rating.

Voltage on the discharged capacitor in time is characterized by the following equation

$$u(t) = U_0 \cdot e^{-\frac{t}{R \cdot C}} \tag{3.9}$$

by solving the equation for resistance by plugging-in the values of maximum voltage, allowed voltage with discharge time and DC-link capacitance, a maximum discharge resistor value can be obtained. For currently used DC-link configuration, the discharge resistor's value must not exceed roughly

8kΩ[8] to be able to discharge DC-link capacitors within required time.

For the motor controller design, a total discharge resistance value of 4000Ωwas selected. By plugging in the selected resistance value back into equation (3.9) a discharge time will be obtained, resulting in a discharge time of 2.504 seconds.

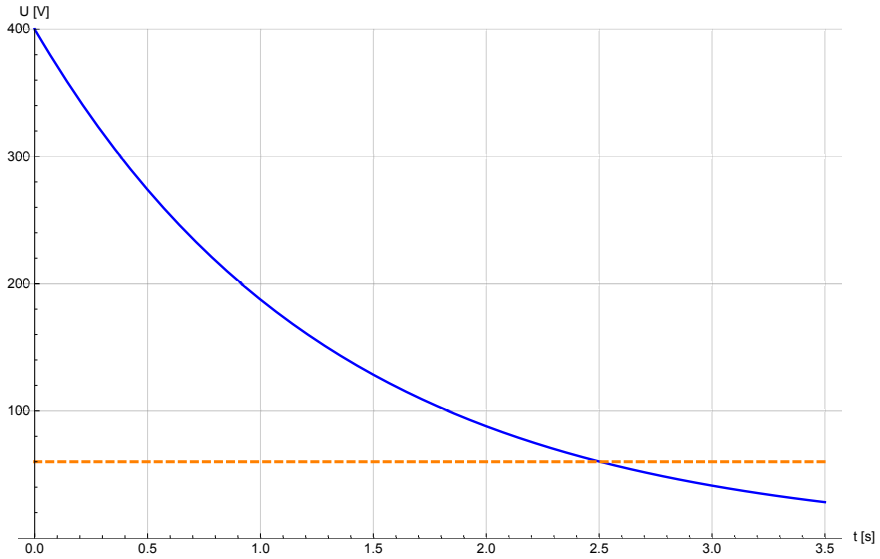


Figure 3.13: DC-link capacitor voltage-time discharge plot with 60V threshold marked.

The theoretical maximum current flowing through the circuit at the switching instant can be calculated from the Ohm's law, alongside with a required power rating of the discharge resistors.

$$I = \frac{U_0}{R} = 100\,\mathrm{mA} \tag{3.10}$$

$$P_d = \frac{U_0^2}{R} = 40\,\mathrm{W} \tag{3.11}$$

Selected resistor values will allow to discharge both motor controllers' DC-link capacitors in case of single discharge resistor set failure, while roughly satisfying the rules. The exact discharge time will be influenced by additional loads on the DC-link capacitors and parasitic characteristics of used components.

[8] exactly 7986.59Ω

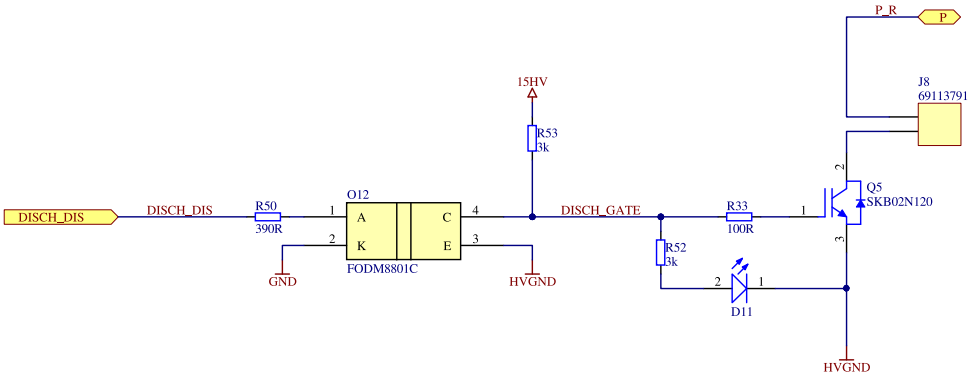


Figure 3.14: DC-link capacitor discharge circuitry schematic.

Capacitors' energy is dissipated in the resistors connected to the board through a 7.5mm connector with a sufficient voltage rating. Discharge resistors are of *PWR221T-30* series manufactured by *Bourns*. They allow for a continuous power dissipation of 30W if connected to a properly sized heatsink. The resistors are also capable of withstanding voltage of 2kV, satisfying the voltage dimensioning rule.[EV4.9.1]

A two 2kΩ resistors of mentioned product line are connected in series and secured to the IPM heatsink to allow for a proper heat dissipation without risking damage to the components even in the event of a direct connection to the accumulator pack. Two resistors are used to ensure proper power rating with applied power derating coefficients for expected working temperature up to 85°C.

Discharge circuit is switched by the *SKB02N120* IGBT manufactured by *Infineon*. Maximum permissible collector-emmiter voltage is 1200V, which readily allows maximum competition's tractive system voltage of 600V. Selected IGBT has a declared continuous collector current capability of 4A at 85°C case temperature. This characteristic greatly surpasses expected peak currents during discharge. The component is available in *TO-263* standard packaging, providing sufficient power dissipation.

The discharge circuitry operation is controlled by a signal from the accumulator pack control unit. A signal to turn off the discharge switch is relayed across the isolation by using the previously described *FODM8801C* optocoupler. When current is applied to the optocoupler's input diode, the output transistor pulls the IGBT gate below its gate threshold voltage, effectively turning it off.

3.5 High power connections

The motor controller's function requires a connection to both accumulator pack for DC power input and a two 3-phase AC outputs for driven motors. Spatial configuration of these connections' terminations is dictated primarily by the IGBT module packaging.

The DC-link power input to the IGBT module can be realized from either

side of the package, providing variability to the input connector location. Motor outputs' position is defined by associated phase current measurement.

3.5.1 Motor outputs

The IGBT power output is led through the previously described shunt resistors for phase current measurement and subsequently through the output connector to the motors. Unmeasured phase is connected directly to the power module via lug leading to the output connector.

The measured phases are equipped with the *Würth Elektronik's WP-SHFU Press-Fit* terminals, allowing lug connection with declared continuous current draw up to 180A. These terminals are stamped directly into the circuit board. Terminal stamping also mechanically secures the copper reinforcement of the phase traces. Lug is secured by using a M5 nut with a washer to prevent loosening of the joint and to satisfy competition's requirement for positive locking in high-current path.[EV 4.5.13][T 10.2]

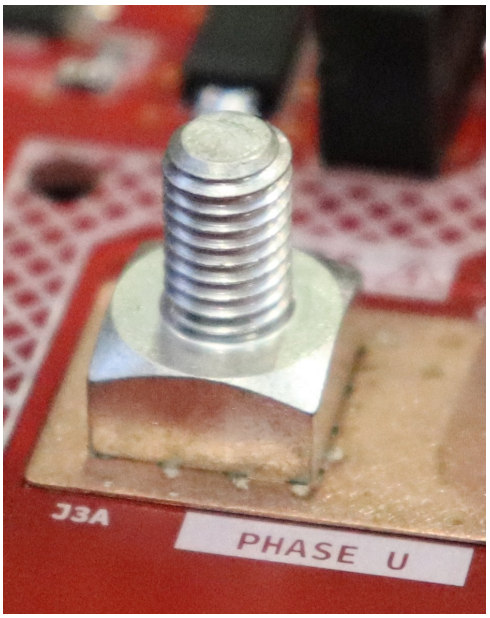


Figure 3.15: Photograph of a stamped *Press-Fit* terminal in a power board's phase conductor.

3.5.2 Accumulator pack input

Accumulator pack input power leads do not posses similar terminals. The lugs are connected directly to the IGBT's DC-link input terminals, which are in turn interconnected together via DC-link capacitors. Reason for this design is to allow various input connector locations in the motor controller's enclosure.

Input power is drawn through a ferrite core in a bid to reduce electromagnetic interference of the device on rest of the vehicles' electronic equipment.

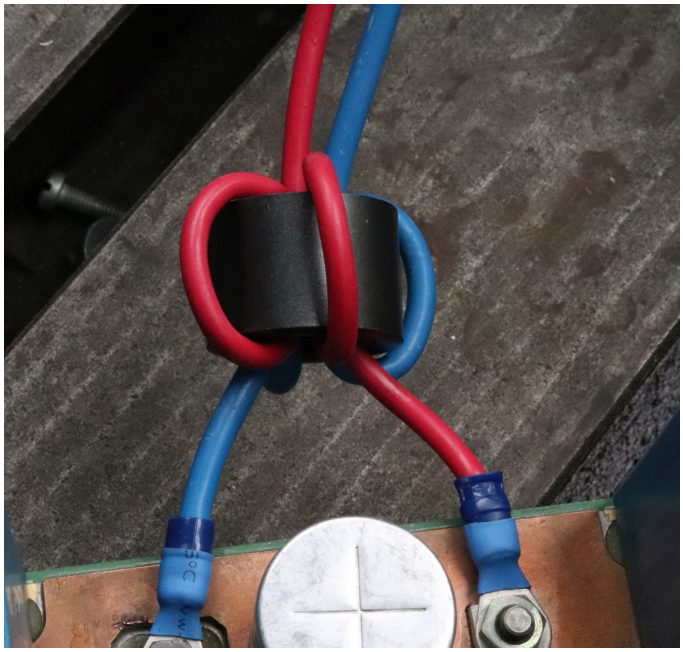


Figure 3.16: Photograph of a ferrite bead wound in a prototype board setup's DC-link input.

3.6 Control board interface

Control board is providing the power board with low-voltage power and control signals needed to switch individual IGBTs and discharge control.

The power board in turn relays information on sensed phase currents, DC-link voltage, safe voltage levels, diagnostic signals and board's unique identification.

This interface is realised by five 2.54mm (100 mil) connector family, the power board uses a socket form of the connector. This is due to their availability and simplicity of integration.

Two of the connectors are located close to the signal isolation and with purpose to relay trigger pulses and diagnostic signals of the power modules.

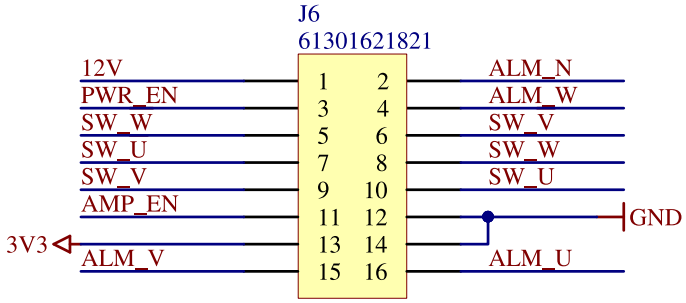


Figure 3.17: Interface connector for the power modules' signals.

A high side switch made from discrete MOSFET cascade is placed for trig-

gering function of the isolated DC/DC converters alongside to the decoupling capacitors for both of the 12V and 3.3V power rails.

To offload the isolator driving from the micro-controller, an octal buffer *SN74AHC541* is used. This buffer has inputs and outputs grouped on the same sides, allowing for a straightforward design on the circuit board. The output enable input of the buffer is used to control the switching pulses directly from the safety chip.

Second set of two connectors are placed closer to the sigma-delta modulators, and they transfer the modulated current signal alongside with necessary clocking signal from the micro-controller. These two sets of connectors are located in close vicinity.

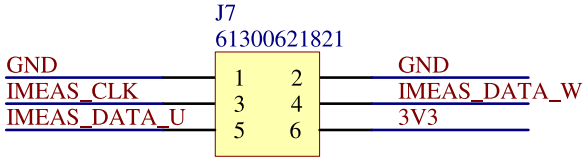


Figure 3.18: Interface connector for the sigma-delta modulators.

Last connector is located on the top of board close to the DC-link management circuitry. Again, a decoupling capacitors are placed in vicinity to decouple the circuitry from long traces and connector itself. An EEPROM memory is also located in this circuit to allow for an individual power boards identification.

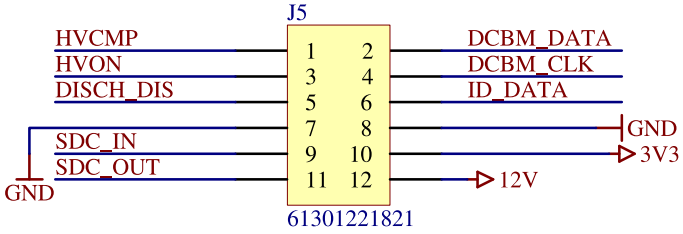


Figure 3.19: Interface connector for the sigma-delta modulators.

3.7 Printed circuit board

Actual design of the power board was primarily dictated by the IGBT modules' terminal positions and a required galvanic isolation between low-voltage and tractive systems.

Isolation separation is specified in the competition's rules with respect to the working voltage ranges and specific configurations.[EV 4.3.5] It should be noted that the rules' required separation is much larger than a distance required by the standards[9] for devices of a comparable configuration.

To satisfy rules and to allow for design utilizing 600V accumulator pack a 4mm isolation between low voltage and tractive system was selected. A Isolation distance is marked by hatched silkscreen print on the board.

[9] e.g. IPC-2221B

Unlike the previous motor controller which used magnetic sensing of the phase currents, the new design needs to accommodate the current sensing shunts directly on the circuit board.

This resulted in positioning of the power modules to have their phase outputs facing each other, located in the center of the motor controller, while the control terminals are located on the periphery of the circuit board. This arrangement provided enough space for the placement of the current sensing shunts with associated circuitry and a required isolation.

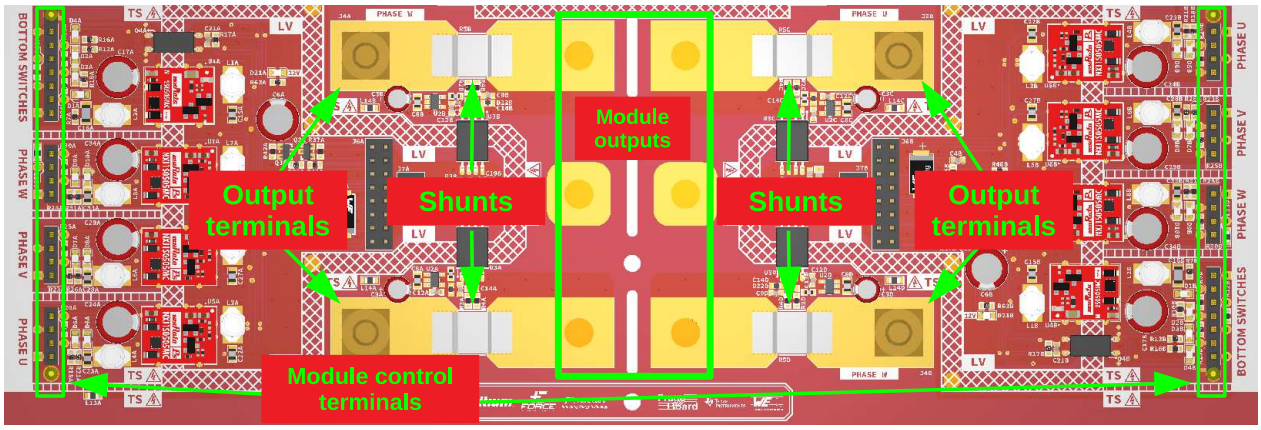


Figure 3.20: Render of the power board design with power elements marked.

The shunts are located close to the phase outputs, roughly in the first quarter of the power module-designated space. Shunts are sensing currents on the first and third (outer) phases. Space left by the second (middle) phase is used by the sigma-delta modulators' circuitry. Shunt outputs are then routed to the described *Press-Fit* terminals.

To allow for a copper reinforcement of the current-carrying traces, the solder mask had to be removed from said traces to permit subsequent copper soldering.

Power and signal isolation for the modules is located in vicinity of the IGBT control terminals.

Thanks to power/signal isolation and phase measurement was made in *multi-channel* mode, the *Altium Designer* allows for copying of the circuit board design of individual blocks. This allowed for a fast design of the power board without need for an excessive design repetition.

Free space between the shunts and power/signal isolation is used by power conditioning, IGBT trigger signal buffering and control board interface connector.

DC-link capacitors are located on the lower side of the circuit board, close to the power modules' DC-link terminals. The film capacitors placed on the bottom side of the board, facing the power modules. This is to reduce height of the motor controller by utilization of the combined height of power modules and associated heat exchanger. Electrolytic capacitor is facing upright thanks to its height being roughly equal to the total height of the control board.

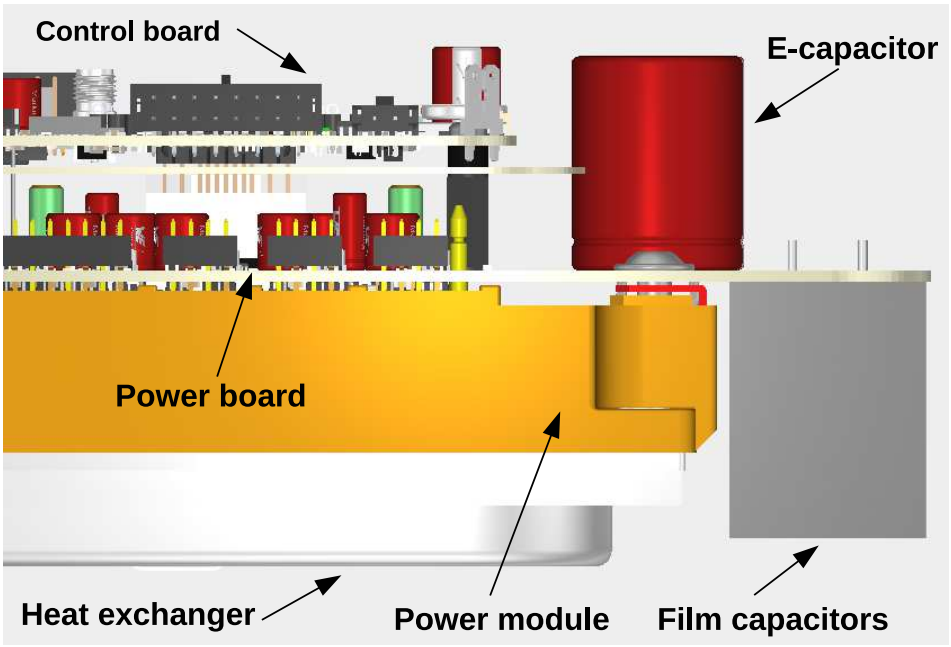


Figure 3.21: Isometric rendering of the DC-link capacitors' positions and clearances within the motor controller.

This circuit board section also depends on the copper reinforcement to allow for a high current flow, therefore its silk screen must be unmasked during manufacture.

The DC-link management circuitry is located on the upper side of the board, close to the modules' power terminals. Right power module side houses the low-voltage power conversion circuitry. This low-voltage power is routed to the left power module side which contains the DC-link voltage measurements and discharge circuitry. Space left between these circuit board sections is used by the controller board interface.

Manufactured circuit board uses a laminate with a stronger base copper to allow for a smaller cross-section of the reinforcement copper. The board was initially intended to be manufactured with 105µm strong base copper, but a manufacturing constraints allowed only for 70µm. Solder mask color was selected for purely aesthetic purposes.

Chapter 4

Motor controller control electronics

The control electronics circuit board is physically placed above the power electronics circuit board. As the name suggests, the board takes care for controlling the motor controller's functions.

Control electronics board encompasses following functional blocks. Each block will be discussed further in the text.

- Input power protection, filtering and conversion.
- External signals protection.
- Micro-controller implementing motor control algorithm alongside with associated functionality.
- Trigger pulse generation for power modules.
- Fault reading from power modules.
- Delta-sigma modulator clock generation and digital filter.
- Resolver excitation and processing.
- Fail-safe circuitry.
- Vehicle shutdown circuit interface.
- High voltage detector signal output.
- CAN bus communication interface.
- Isolated USB communication interface.
- SD card storage.
- Identification memories interface.
- Temperature sensor reading.
- Coolant pump control.
- Debug and programmer interfaces.

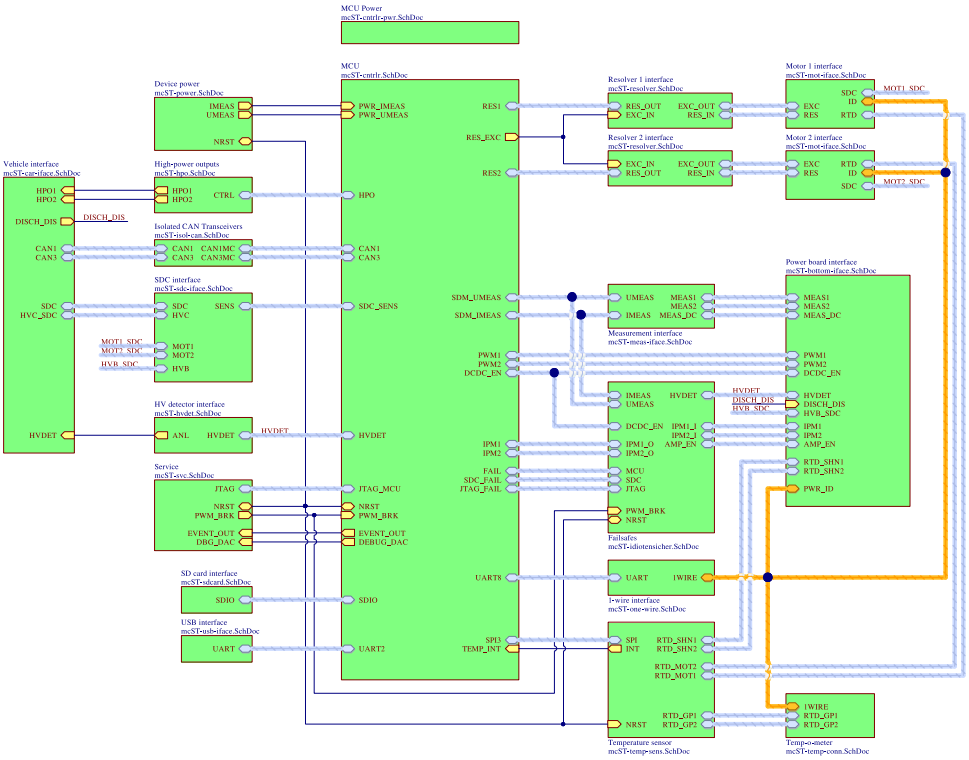


Figure 4.1: Top level schematic diagram of the motor controller's control board.

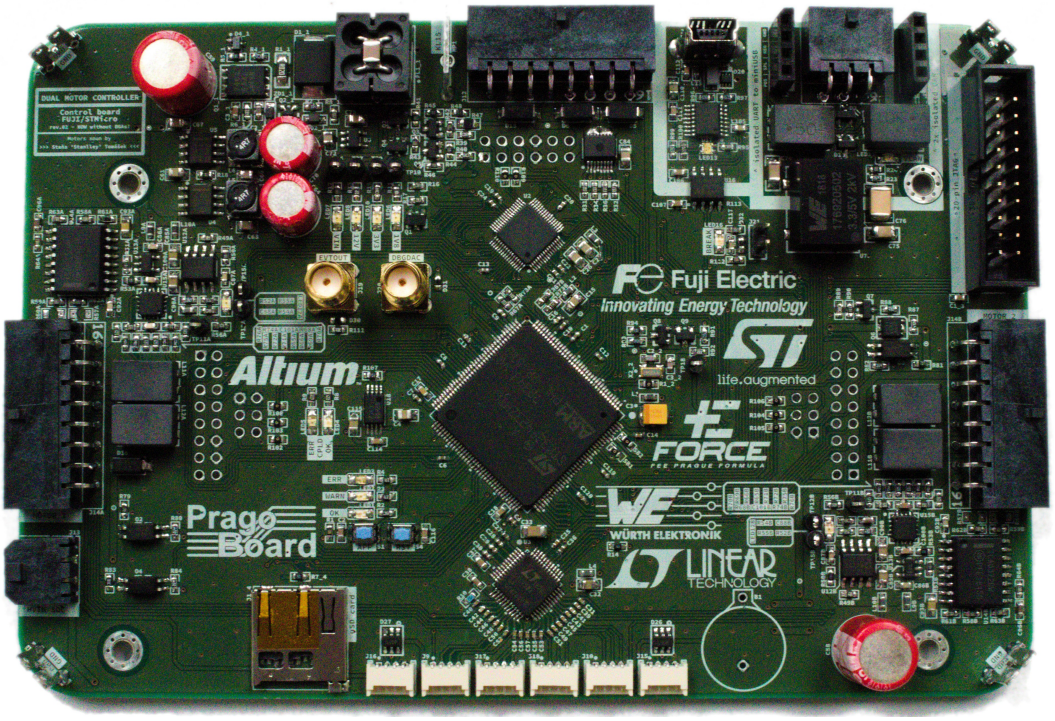


Figure 4.2: Motor controller's control board.

4.1 Input power

Motor controller's components require multiple conditioned voltage rails. The input voltage from the vehicle is usually between 24 and 26 volts. This input voltage is first filtered by using a dedicated EMI filter. Reason for this is to prevent interference on the circuitry from external units and importantly not to release any noise back into the vehicle.

The filtered input voltage is taken through silicon diode to prevent polarity inversion on the input. Afterwards the voltage is clamped not to exceed valid input range of subsequent DC/DC converters' circuitry.

Input voltage magnitude is measured using a voltage divider accompanied by clamping diodes to prevent analog-to-digital converter damage. Current draw of the unit is also measured by using shunt with a high gain differential amplifier. Both of these measurements are taken for diagnostic purposes.

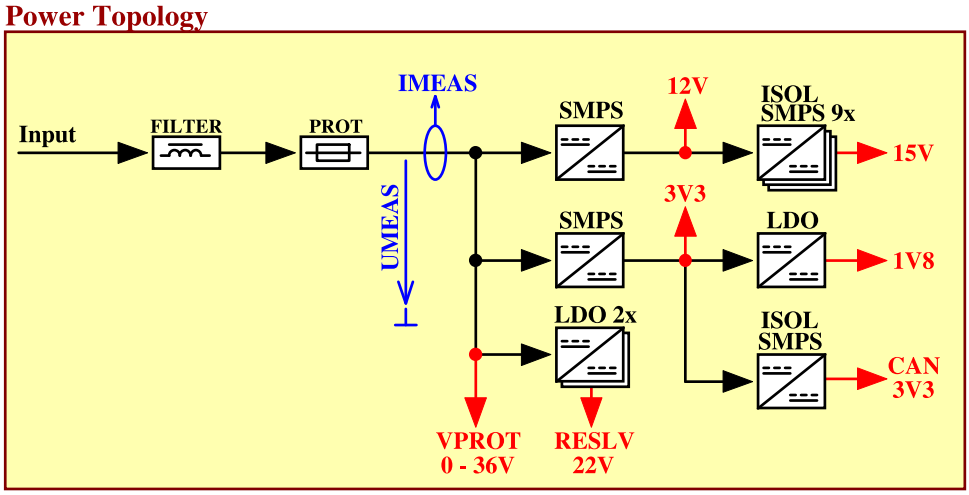


Figure 4.3: Topology of low voltage supply circuitry.

4.1.1 Switched-mode DC/DC converters

In order to convert input voltage into voltage levels required by controller's circuitry with a high efficiency a switched-mode power supply topology was chosen.

The 12V rail is being actively used by isolated DC/DC converters of the power board. Therefore, the output power rating should be at least 10W to sufficiently power all the IGBT drivers. This results in roughly 1A current requirement on the DC/DC converter. The 3.3V digital rail is used by most of the motor controller's circuitry. A nominal load current of 800mA was calculated for this power rail. Maximum load of the 3.3V rail should not reach 1.5A.

For supplying the aforementioned rails a *LMR33620* synchronous step-down converter manufactured by *Texas Instruments* was selected. Selection criteria for this component were a monolithic solution with integrated transistor

switches, sufficient input voltage tolerance, continuous current rating of at least 1.5A to allow for a loading headroom and a switching frequency of at least 1MHz to limit the sizes of associated inductors.

Inductance value was selected with respect to the switching frequency and consequently allowed current ripple. Inductor current rating must satisfy maximum load current of the converter in order to not saturate the core and thermally stress the inductor due to a joule losses in the winding.

The selected device also possesses capability of a synchronous rectification to lower conduction losses on the diode and already contains a compensation network to ease implementation of the converter. Unfortunately the manufacturer does not offer a fixed-voltage versions of the controller and therefore the converter must be outfitted with a feedback network.

The bottom feedback resistor values are different for different rail voltage. Converter already contains a compensation network and therefore the capacitors in the feedback are not fitted. Upper compensation capacitor is only a placeholder for a case of feedback trimming.

Power good functionality is used with the 3.3V regulator to control reset of the subsequent digital circuitry. During the regulator startup, the reset pin is held low, keeping the circuits in reset state until the output voltage is asserted to be stable. This is to ensure that the digital circuits work with proper voltage levels.

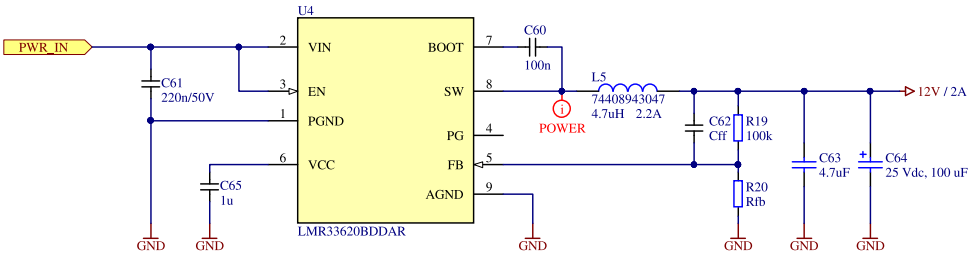


Figure 4.4: Schematic of a switched-mode power supply implementation.

4.1.2 Low dropout regulators

Low dropout regulators are used in the design where either a low voltage drop alongside a low power draw is expected (1.8V rail) or a very low noise levels are required (resolvers' analog circuitry).

The 1.8V rail is used to power the core of a safety integrated circuit. Maximum expected current draw was calculated to be approximately 100mA. For this purpose a *TLV75518P* series low dropout regulator with a fixed voltage option was selected. As with any other LDO, a low ESR ceramic capacitors are required on both input and output of the converter for a stability reasons.

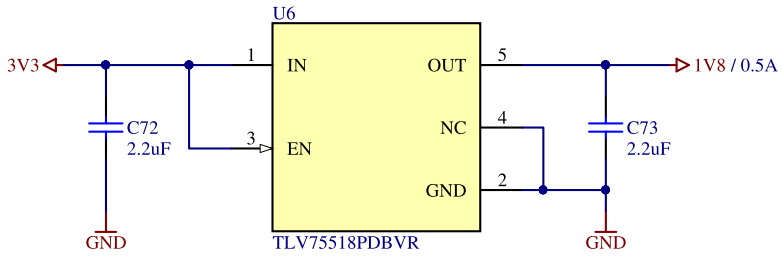


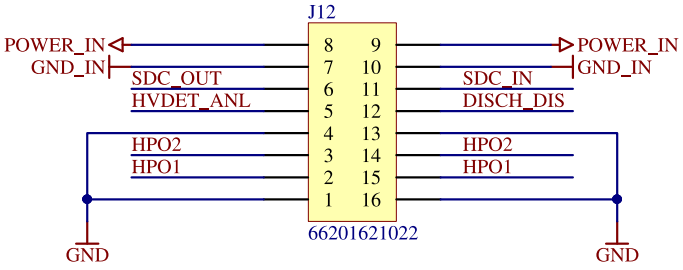
Figure 4.5: Implementation of a low dropout regulator for the 1.8V rail.

4.2 External signals

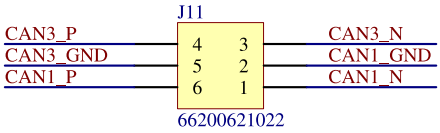
Besides the input power from the low-voltage supply of the vehicle, the motor controller requires other control signals and buses connections for proper operation. Thesis will discuss every one separately in detail, alongside with their respective circuitry and software implementation.

Signals from the vehicle are routed from input connector of the device's enclosure into 2 internal connectors.

First connector encompasses primary power input, shutdown circuit connection, high voltage detection, discharge control signal and a controlled power outputs. Second connector is routed into separate part of the board, taking care of the CAN bus communication.



(a) : Power and signals connector.



(b) : CAN bus connector.

Figure 4.6: Vehicle-side connectors of the motor controller.

Each motor use a single cable to connect resolver, temperature sensor and shutdown circuit to the motor controller. These signals must be kept separate from the high-voltage harness in order to maintain the separation of the low voltage and tractive systems.[EV 4.3.2]

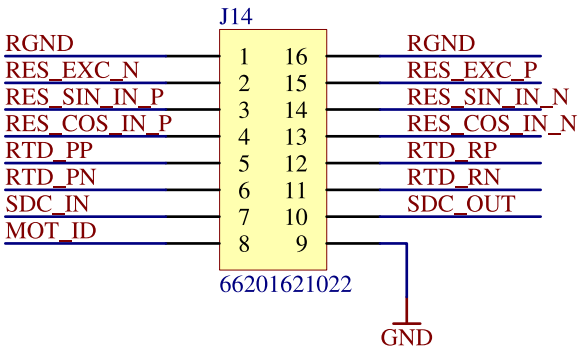


Figure 4.7: Single connector for a motor's signal harness.

The high voltage input connector from the accumulator pack also requires a shutdown circuit interlock. To extend diagnostic capabilities of the motor controller, a separate connector is used to provide for a clearly defined sensing point.

All the formerly mentioned connectors use *MF-30*-based components. Their current carrying capabilities, manufacturer and suppliers abundance and most importantly ruggedness, makes them a favorable choice. Strength of their connection very often necessitates for a considerable force or tools to disconnect.

4.3 Micro-controller

The motor controller employs a *STMicroelectronics* manufactured micro-controller *STM32F423ZH* to facilitate primary motor control, communication with other vehicles' units and various other auxiliary functions, which will be described later in text.

From hardware viewpoint, the selected micro-controller is packaged in a 144-pin *LQFP* with 0.8mm lead pitch.

The micro-controller requires a steady 3.3V power rail to allow for a proper. This is accomplished by capacitor decoupling as per the device's specifications.

Also, the micro-controller requires external capacitors for operation of its internal regulator, providing voltage for the device's core, thus eliminating the need for an external one.[45]

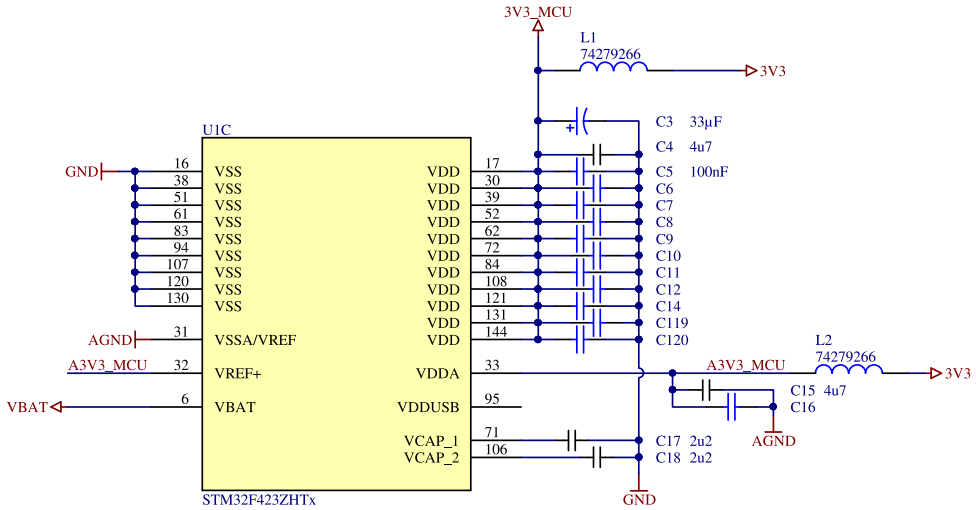


Figure 4.8: Power stage schematic of the used micro-controller.

General reason behind proper decoupling of the high-speed digital integrated circuits is to prevent excessive voltage drop caused by long power traces' inductance, coupled with a high frequency switching operation of these devices. Problems with electromagnetic compatibility may also arise with insufficiently decoupled digital devices.

Micro-controller also requires a two clock sources. While the micro-controller contains its own clock source, its precision is not sufficient to operate high speed peripherals. For the first clock source, a high-speed, high-precision clock is sourced from a 16MHz oscillator.

Second clock source is a low speed crystal used by the Real-time clock peripheral for keeping accurate track of the time, used for auxiliary or debugging purposes. Crystal is used to allow for RTC operation from the backup battery source, even with vehicle's low voltage supply being offline.

Overall, the motor controller uses 88 pins out of the 114 available signal pins of the micro-controller. Following peripherals are used in the micro-controller for motor controller operation.

- `TIM1` and `TIM8` – Advanced control timers generating the PWM signals controlling two VSI. See 3.6
- `TIM4` and `TIM5` – Standard timers used for reading diagnostic signals of the power modules. See 3.6
- `DFSDM1` and `DFSDM2` – Sigma-delta modulator filter for voltage and current reading. See 4.5, 3.3 and 3.4.3
- `CAN1` and `CAN3` – Intra-vehicle communication. See 4.9
- `ADC1` – Reading of analog signals, especially the resolvers. See 4.6
- `DAC` – Resolver excitation generation and debug information. See 4.6 and 4.16

- `SDIO` – SD card native interface. See 4.11
- `SPI3` – Temperature sensor IC communication interface. See 4.13
- `USART2` – Advanced UART for communication with diagnostic hardware. See 4.10
- `UART8` – Basic UART for 1-wire interface implementation. See 4.12
- `SYS` – Programming and debug interface. See 4.15

4.4 Power board interface

Interface for the power board is a direct counterpart to the previously described one in section 3.6.

To reiterate, the interface uses a 2.54mm connectors family thanks to their availability and simplicity of integration. Control board is equipped with a header form.

In order to fit the power board components underneath the control board, the control board is placed higher than a classic 2.54mm connector pin length allows. This necessitated in using a longer headers with some mechanical adjustments.

4.5 Delta-sigma modulator interface

The delta-sigma modulators utilize two high-speed signals for its function. Clock signal specifying modulator clocking rate is generated by the host. Data signal representing modulated measured data at the provided clock frequency is sent by the modulator back into the host.

The current sense modulators are physically located on the power board within two groups, where each group reads phase currents of a single motor. Due to a physical length of trace needed to properly route the signal a concern was raised to possible problems with signal integrity and electromagnetic interference.

A high speed, low jitter, fan-out output dual clock buffer *CDCLVC1102* was added to the design to alleviate these concerns and to reduce load on the micro-controller.

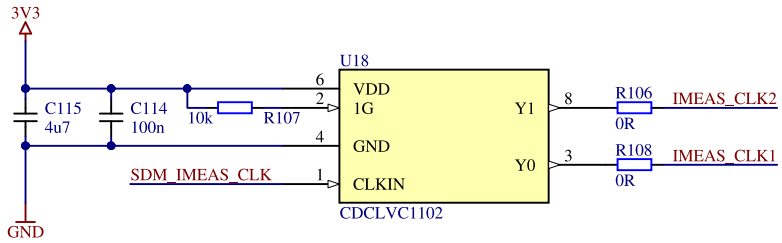


Figure 4.9: Clock buffer for phase current measuring modulators schematic.

Modulators' outputs are led directly to the micro-controller without need for a buffering.

Both of these signals were routed with high-speed design in mind, by setting the trace width for characteristic impedance of 50Ω and by reducing amount of vias. Both measures are to improve the signals' quality.

The traces also posses a resistor placeholders to allow for impedance trimming in case of a signal integrity problems. In default state a 0Ω resistor is placed to bridge the empty placeholder.

4.6 Resolver interface

Motors manufactured by the *TG Drives* company for our vehicles employ resolvers as an angular position sensor.

Resolvers are known for their mechanical and electrical ruggedness, small size and low cost compared to other angular position sensors. On the other hand, they require more complex analog circuitry in the design to generate excitation signal and subsequent signal processing.

This motor controller design contains two identical resolver processing blocks. Primary objective was to create a simple solution without requirement for a bipolar power supply.

The resolvers' excitation input usually requires a sinusoid signal with amplitude of 4 to $7V_{rms}$ with a frequency of a several kilohertz. Excitation signal base is generated by a micro-controller's digital-to-analog converter. The base signal is differentially amplified and applied to the primary winding.

Datasheet values for the *RE 15-1-A15*[46] resolver used in our motors state $7V_{rms}$ excitation voltage at frequency of 10kHz with current draw of 36mA.

In order to properly design an analog amplifier stage, a resultant peak to peak voltage must be known. This will also determine parameters of the power stage.

Following equation was used to calculate peak-peak voltage

$$U_{pk-pk} = 2\sqrt{2} \cdot U_{rms} \tag{4.1}$$

$$U_{pk-pk} = 2\sqrt{2} \cdot 7 \doteq 19.8V \tag{4.2}$$

This is also a minimum power supply voltage of resolver interface circuitry to properly drive the resolvers' primary winding.

4.6.1 Excitation amplifier

Excitation amplifier is tasked with amplifying the micro-controller's DAC output from $3V_{pk-pk}$ to the calculated resolver excitation level of $19.8V_{pk-pk}$.

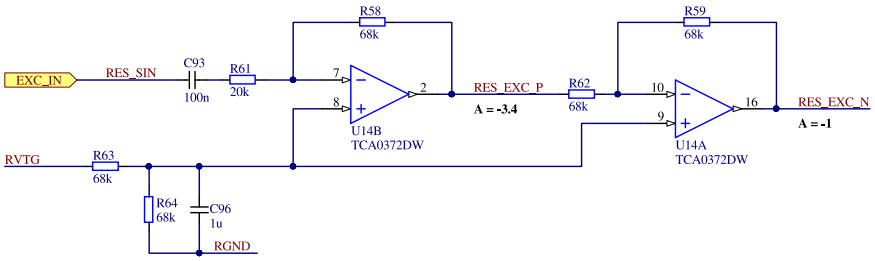


Figure 4.10: Excitation amplifier schematic of the resolver interface.

The *TCA0372DW* dual operational amplifier is used as a power amplifier for the current hardware revision. Previous iteration of the control board used the *ALM2402-Q1*. Reason for change was higher allowable input voltage, output current, higher slew rate capability and lower cost at the expense of automotive qualification and over-temperature diagnostic output.

Both amplifiers are connected in inverting voltage amplifier configuration, forming a single-ended to differential converter. Their amplification gain and consequently output to input voltage relations are following

$$A_{U14B} = -\frac{R58}{R61} = -3.4 \tag{4.3}$$

$$A_{U14A} = -\frac{R59}{R62} = -1 \tag{4.4}$$

$$U_{out} = 2 \cdot A_{U14A} \cdot A_{U14B} \cdot U_{in} \tag{4.5}$$

Values of the resistors were chosen to allow for a bias current to flow into the amplifier inputs and to fit into the available resistor series (E24). By connecting the resolver's primary winding between the `RES_EXC_P` and `RES_EXC_N` differential outputs, the resultant gain becomes A=6.8.

The excitation input signal `RES_SIN` from the micro-controller's digital-to-analog converter must be first deprived of the DC component to allow for a proper amplification. This is accomplished by using high-pass RC filter composed of `C93` and `R61` with cutoff frequency of $f_p \approx 80$Hz.

To operate the amplifier from unipolar supply, the amplifier must be properly biased to satisfy the following condition

$$V_{ol} \leq V_{bias} + A \cdot V_{dac} \leq V_{oh} \tag{4.6}$$

V_{ol} and V_{oh} voltages which specify allowed output voltage swing after which an output voltage clipping will occur. The power amplifiers are rarely manufactured with rail-to-rail operation capability, therefore the allowed voltage swing does not correspond to the applied power supply rails. Allowed voltage swing is also inversely dependent on the load of the amplifier output.

$$V_{ol} > 0V \tag{4.7}$$

$$V_{oh} < V_{cc} \tag{4.8}$$

4.6.2 Signal processing

In order to process the resolver's position in the micro-controller, the differential input signals carrying modulated position in sine and cosine components must be converted from differential to single-ended signals and brought into analog-to-digital converter's valid input range.

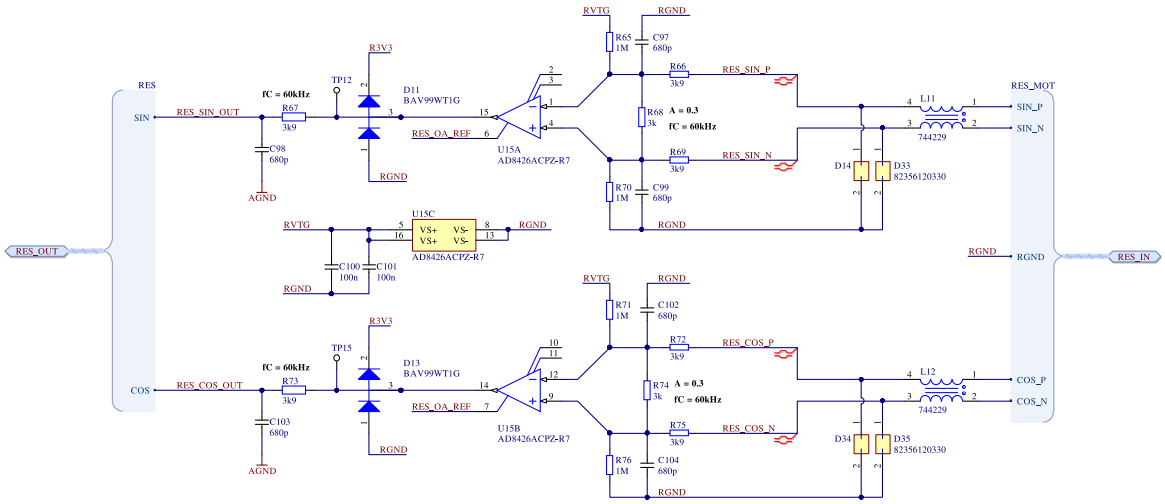
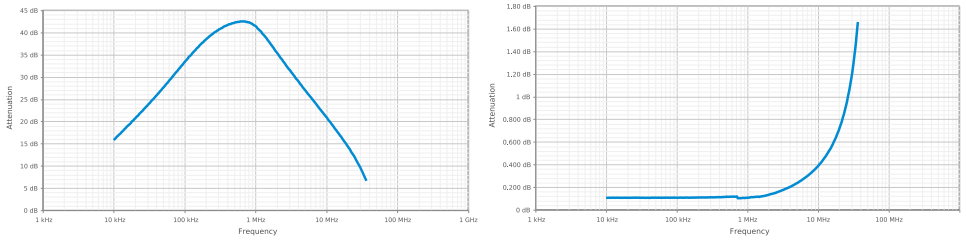


Figure 4.11: Resolver signal processing circuitry schematic.

The resolver's signals are first routed through common-mode chokes `L11` and `L12` to remove picked noise on the resolver cable. While the usage of shielded twisted-pair in the resolver harness significantly reduces any noise, these chokes are extra measure to prevent EMI from coupling into the measurement or rest of the board. Their common mode attenuation at the 10kHz frequency of interest[1] is declared to be 16dB while differential attenuation at the same frequency is negligible.



(a) : Common mode. **(b) :** Differential mode.

Figure 4.12: Signal attenuation of the selected common-mode choke.

The common mode attenuation rises to roughly 40dB at 1MHz after which the parasitic effects of the component's capacity begins to reduce its effectiveness. Arising problem with a common-mode choke usage is an introduced phase shift of the signal, caused by inductive reactance. This shift must be compensated for later in the micro-controller's firmware.

[1] switching noise from the power modules

A transient voltage suppressor diodes D14, D33, D34 and D35 protect sensitive analog circuitry from electrostatic discharge events arising from device handling or hot connection (disconnection) of the resolver.

Most of the integrated circuits' specifications claim possession of ESD suppression measures on their pins but it is still a good design practice to add an extra measure of protection on the devices' circuit board inputs.

Differential voltage dividers formed by resistors R66, R68, R69 for sine component and R72, R74 and R75 for cosine component attenuates the resolver output voltages into range accepted by the micro-controller's analog inputs. The selection of resistor values is realized by the set of following equations

$$\mathrm{A} = \frac{\mathrm{U}_{\mathrm{adc(pk-pk)}}}{\mathrm{U}_{\mathrm{res(pk-pk)}}} = 0.3 \tag{4.9}$$

$$\frac{\mathrm{R68}}{\mathrm{R68} + \mathrm{R66} + \mathrm{R69}} = \frac{\mathrm{R74}}{\mathrm{R74} + \mathrm{R72} + \mathrm{R75}} = \mathrm{A} \tag{4.10}$$

$$\mathrm{Z}_{\mathrm{tot}} = \mathrm{R68} + \mathrm{R66} + \mathrm{R69} = \mathrm{R74} + \mathrm{R72} + \mathrm{R75} \geq 10\mathrm{k}\Omega \tag{4.11}$$

first and second equations set attenuation of the dividers to convert from resolver output voltage level to analog-to-digital converter in the micro-controller. Third equation adds requirement for a large enough input impedance in order not to excessively load the resolver. Actual values were selected to fit the manufactured series of resistors. The required attenuation of these dividers can be also calculated alternatively, by taking half of the total calculated gain of the power stage and calculating the reciprocal value.

The capacitors C97, C99 and C102, C104 alongside with previously selected resistors form a low pass filter to remove unwanted high frequencies from the resolver signals.

To convert a differential signal provided by resolvers, a differential or an instrumentation amplifier is usually used.

The instrumentation amplifiers can be viewed as a superset of differential amplifiers. Alongside a differential amplifier, they contain two other operational amplifiers to offer high input impedance and a matched set of passive components to provide tightly matched parameters. Instrumentation amplifiers are capable of high amplification rates (A > 10 000) and provide a very high common mode signal rejection.

Their matched parameters allow for a low DC offset, low noise and negligible gain and offset drift for very precise measurements of low-voltage sensors – strain gauges, temperature sensors, etc.

For the control board design an *AD8426* dual instrumentation amplifier was selected for its high input voltages tolerance, single-ended supply & rail-to-rail operation, unity gain capability, high common-mode rejection and a compact packaging of two amplifiers into a single integrated circuit.

Again, due to requirement of a unipolar supply of resolver analog circuitry, the instrumentation amplifier's input and output must be properly biased in order not to distort the resolver signals. Input biasing is done using resistors R65, R70 and R71, R76 whose values put bias directly between power supply rails to prevent the resolver signal from swinging beyond power supply rails.

Output biasing is accomplished by applying half of analog-to-digital converter supply voltage[2] to the amplifier's reference input pin. Reference voltage is generated by using a resistive divider and a simple voltage follower.

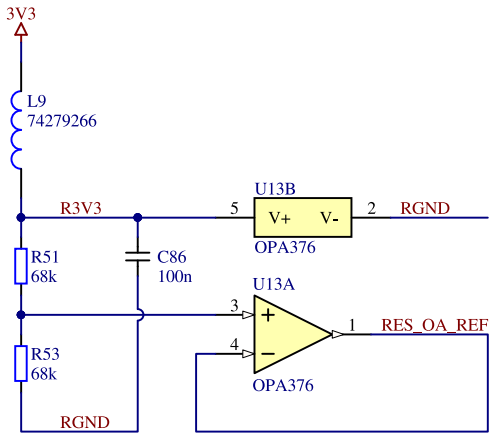


Figure 4.13: Reference voltage generator for instrumentation amplifier.

Amplifiers are being fed from a 20V supply voltage. In case of resolver output problem (open circuit, rail short circuit), their output voltage can reach destructive levels for the micro-controller's analog-to-digital converter. To prevent these damaging conditions reaching micro-controller, the amplifiers' outputs are routed through a dual clamping diodes `D11` and `D13` which will limit the voltage to a tolerable input range. These out-of-range voltage levels are evaluated on the firmware level and lead to an error signalization.

RC filters placed directly before the analog-to-digital converter serve a dual-purpose. First is to act as an anti-aliasing filter to prevent higher harmonics from interfering with resolver signal. The second purpose is to act as a low-impedance source for the analog-to-digital converter input thanks to filters' close physical proximity to the input pin of the micro-controller.

Care must be taken to not overload the instrumentation amplifiers with excessive capacitive load. This overloading will lead to amplifier instability, causing output voltage oscillations. Design tackles this issue by using a low capacitor value, which is still order of magnitude larger than analog-to-digital converter's input capacitor, and a large resistor value which "shields" the amplifiers from capacitive load.

4.6.3 Power supply

The resolver interface circuitry is primarily of analog nature, therefore use of a low noise DC/DC converter is desirable. Thanks to a low current requirement a linear regulator can be considered for this application instead of a "noisy" switched-mode converter.

[2] In this case a filtered digital supply voltage.

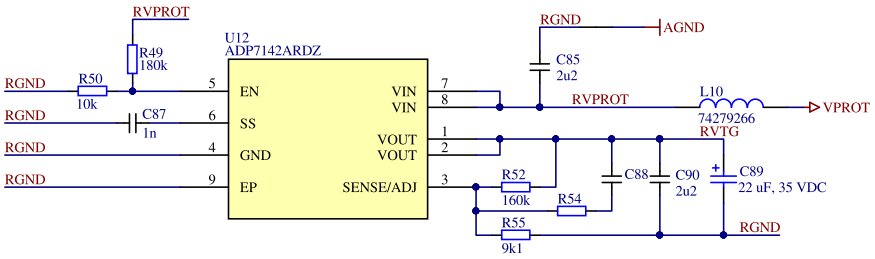


Figure 4.14: Schematic of the low dropout regulator in the resolver interface.

An *ADP7142ARDZ*[47] adjustable, low-dropout regulator was selected to provide a low noise power supply to the resolver analog circuitry. Selected regulator allows for input voltages up to 40V, providing enough headroom for the vehicles' voltage bus. Heat generated by a dissipative action of the regulator is transferred by exposed pad package directly to the ground plane of the circuit board.

The output voltage is set using resistor divider whose component values are calculated by following equation

$$U_{out} = 1.2 \cdot \left(1 + \frac{R52}{R55}\right) \tag{4.12}$$

selected resistor values sets the output voltage at 22.3V.

Due to the power amplifier not being rail-to-rail the voltage must be higher than required 19.8V in order to allow for amplifier output reaching desired levels. Typical allowed voltage swing with respect to the supply voltage and load current is declared in the power amplifier's datasheet to be 1.3V below and above supply rail voltages at 1A load.

Nevertheless, the load current is not expected to approach the specification levels. Therefore, the allowed voltage swing will be much closer to the supply rails.

Regulator possesses enable function with hysteresis to ensure proper input voltage level for output voltage stabilization. Enable threshold is set by a resistor divider by `R49` and `R50` respectively. Enable threshold is calculated by following relation

$$U_{in(en)} = \left(\frac{R49}{R50} \cdot 1.2\right) + 1.2 \tag{4.13}$$

Also a soft-start function is present to reduce current inrush on the device start-up. Time for device start-up is determined by the value of `C87`.

To achieve further reduction of a regulator output voltage noise a circuit composed of `C88` and `R54` whose values are selected to keep the error amplifier close to the unity gain can be used. Complete calculation procedure is elaborated in the device's documentation.

In order to ensure regulator's stability both input and output capacitors are required. Device's specifications recommend a ceramic capacitor of capacity at least 2.2µF. Additionally an aluminum-polymer capacitor was added to the device's output to further enhance transient and noise performance.

A ferrite bead L10 in the regulator's input is used to decouple the regulator and subsequent analog circuitry from switching noise of the switching-mode power supplies in the motor controller's power cascade. It is also making possible to create split ground planes for resolvers' analog circuitry.

4.7 Shutdown circuit interface

The shutdown circuit is a safety feature required in all of the Formula Student-class vehicles. Their exact specifications and requirements vary across the individual vehicle classes.[CV 4][EV 6][DV 1.5]

Generally speaking, it is a string of serially connected safety elements[3] powered initially from the accumulator pack control unit. Its purpose in the electric vehicles is to provide power to close the accumulator isolation relays, providing tractive power to drive the vehicle.

Should any of the elements become actuated, the power holding the normally open accumulator relays will cease to flow, causing the relays to open and in turn contain the tractive power within the accumulator pack.

The motor controller contains several of these elements (interlocks) which primarily ensure that the power and control connectors are properly secured.

State of every interlock in the controller is being actively sensed by the control and safety circuitry. The motor controller design also allows for breaking the shutdown circuit by dedicated high-side switch.

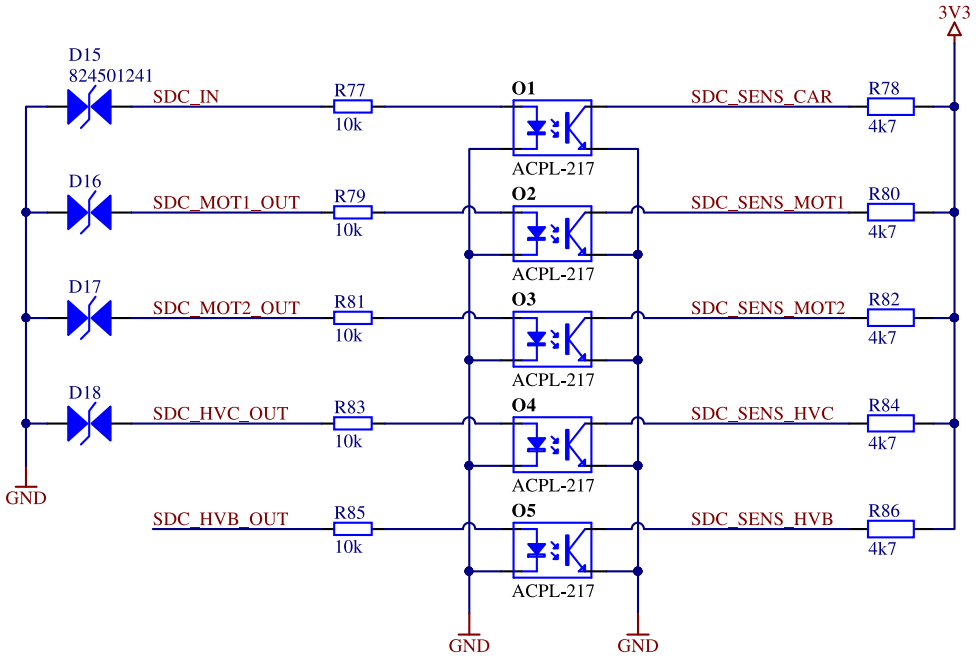


Figure 4.15: Schematic of the motor controller's shutdown circuit interlocks sensing.

[3] shutdown buttons, interlocks, safety devices

Each monitored interlock which exits the motor controller's circuit boards is protected by a TVS diode to prevent damage to the sensing optocouplers. Signal from the shutdown circuit point is routed to the transmitter diode of the sensing optocoupler through a current limiting transistor.

Output levels of the optocoupler invert actual state of the measured point. Signals are pulled up by the resistors in order to set a defined voltage level.

Initial shutdown circuit measurement point comes from vehicle connector. Next interlock is on the power board. Following interlock is for both of the first motor connectors. Unlike the previous motor controller, the current design aggregates both connectors into one sensed point – a remnant of a proposition to merge both power and control harnesses.

Next interlock is the accumulator pack power input to the DC-link capacitors. Final interlock is the second motor's connectors.

Interlock sensing sequence directly copies connector locations on the control board. It can be simply reconstructed by starting from vehicle connector facing 12 o'clock, and going across the output connectors in counterclockwise direction.

Before the shutdown circuit exits the control board, a P-MOSFET based high side switch allows for a termination of the signal, based on a logic within the safety chip. This functionality can be completely bypassed by shorting the prepared solder bridge.

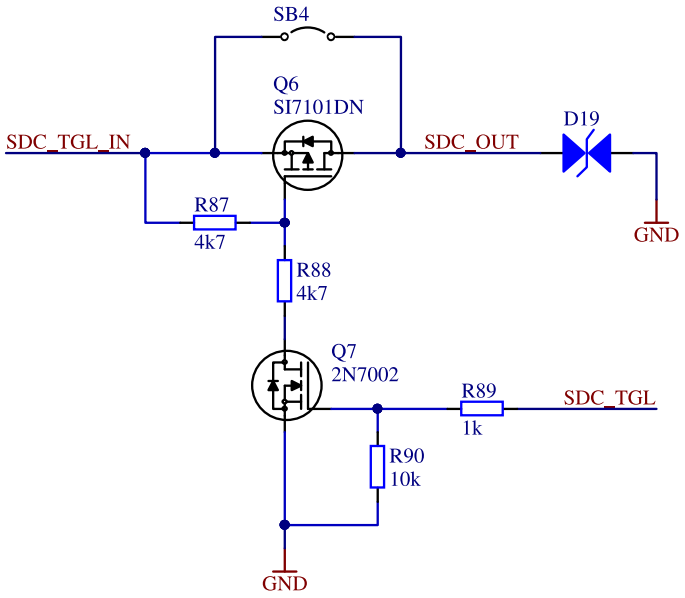


Figure 4.16: Schematic of the motor controller's shutdown circuit high side switch.

4.8 High voltage detector

The high voltage detector circuitry is a method devised to satisfy the TSAL related rules which require a dedicated voltage monitoring of every DC-link

capacitor set within enclosure, connected into vehicle's tractive system. This monitoring must be done purely in hardware without any software processing or intervention.[EV 4.10.2][EV 4.10.8][EV 4.10.13]

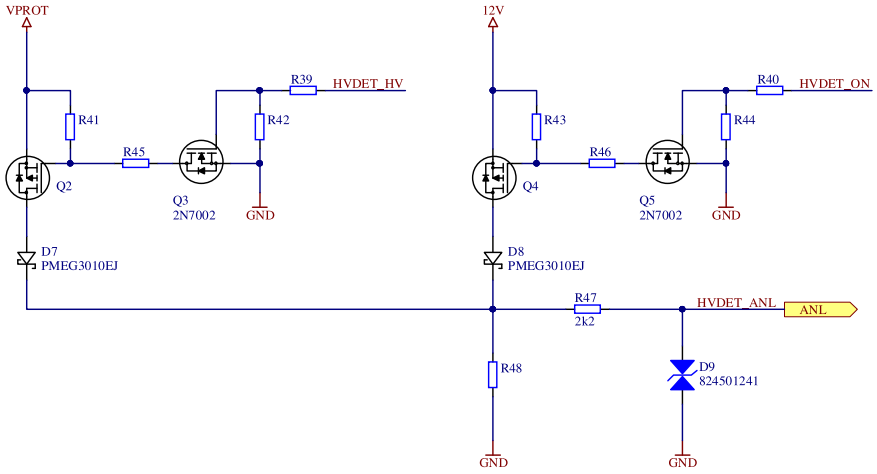


Figure 4.17: High voltage detector interface schematic.

`HVDET_ON` and `HVDET_HV` are signals originating from the power board's high voltage detection circuitry. See **??**. These signals are used to trigger discrete high side switches which toggle either 12V or 24V to the output pin. `D7` and `D8` schottky diodes are used to prevent shorting of the switched power rails via MOSFET intrinsic diodes. Pull-down resistor `R48` defines 0V level output in case of both high side switches being off. `R47` limits current flow in case of fault on the signal line. `D9` will clamp voltage spikes generated by long leads' inductances, decreasing a possibility of the ESD damage to the sensitive silicon devices.

This circuit is a new addition to the motor controllers' design and some concerns were raised about voltage level transmission's noise immunity. Should these problems actually occur, the circuit would have to be modified in order to use current-based transmission by usage of e.g. voltage controlled-current source (*VCCS*) circuit.

Processing at the TSAL side is also done in hardware by using analog comparators for state resolution and discrete logic gates to trigger individual LED diode arrays signalizing tractive system voltage level and a vehicle state. TSAL requrirements are clearly defined in the competition's rules.[EV 4.10]

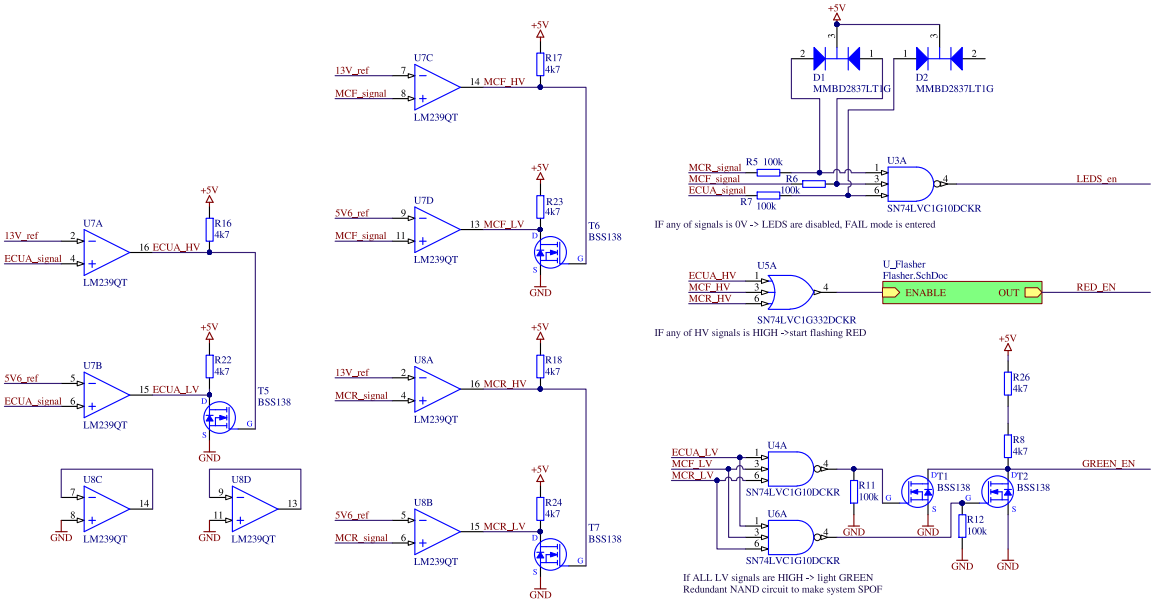


Figure 4.18: TSAL-side level detector and logic schematic.
Courtesy of Bc. Jan Mánek

It is a common practice in a certain competitions' technical inspections to test the functionality of this circuit by pushing the vehicles equipped with a permanent magnet-based motors with deactivated tractive system to induce voltage larger than 60V in the inverters' DC-link capacitors. Once the TS voltage, which is directly measured by scrutineers on the TSMP rises above the 60V threshold, the TSAL must react correctly in order to pass the scrutineering.

4.9 Isolated CAN interface

As mentioned in introductory chapters, the eForce's vehicles use CAN bus for inter-bus communication. Motor controllers actively use both CAN buses present on the vehicles, distinct from most other units which utilize only the primary bus. The secondary CAN bus is usually dedicated directly to the traction control systems.

The galvanically isolated CAN bus implementation was a team's requirement in a bid to increase ruggedness and reliability of the CAN bus in a strongly EMI-influenced environment of the electric vehicle. Its implementation had become mandatory to all units in the newest vehicle.

Implementation consists of power and signal galvanic isolators whose function is to separate motor controller and the actual CAN bus with transceivers converting between the unipolar CAN signals and the differential signal transmitted across the *CAN physical layer*.

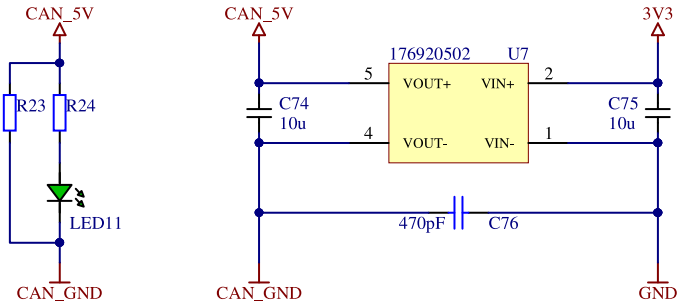


Figure 4.19: Isolated DC/DC converter of the galvanically isolated CAN bus.

The *MagI3C-FISM* isolated DC/DC converter from *Würth Elektronik* was selected for power isolation part. Primary considerations were a 3.3V operation on the unit side, 5V output on the bus side, appropriate power rating, low-profile/industry-standard packaging and a simplicity of the integration. Operation of the DC/DC converter is signalized by a LED diode.

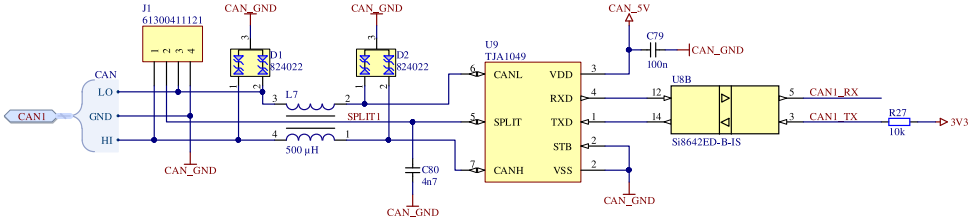


Figure 4.20: Single channel of galvanically isolated CAN bus.

For the CAN bus' signal isolation a *Sillicon Labs' Si864x* series quad digital isolator in a 2/2 configuration[4] was used. This part was selected thanks to its high data throughput (up to 150Mbps), low cost, supplier availability and wide selection of input/output configurations.

The used CAN bus transceivers are *TJA1049*[48] from *NXP*. Their selection was based on their availability in the team's supplies but can be freely exchanged for a different device thanks to their industry-standard packaging/pin-out. This transceiver allows up to 5Mbps signaling rates specified by the newest *CAN FD* standard, contains ESD and EMI suppression measures and is qualified for an automotive applications by compliance to the *AEC-Q100* specification.

4.10 Isolated USB interface

To allow for online parametrization, tuning and diagnostics an isolated USB interface was added to the design. USB is transformed into basic UART by means of USB to UART integrated circuit. The UART is then simply transferred across the galvanic isolation and processed by the micro-controller.

[4] two input and two output isolated channels

While an USB isolator is a commercially viable integrated circuit, simplicity of the UART can help in a difficult debugging situations without a need for complex setup of the USB peripheral in the micro-controller.

Isolation requirement is set in the competition's rules which clearly require galvanic separation of any connected external equipment to a tractive system-connected control units.[EV 4.3.7]

A Mini-USB connector was selected for the design thanks to its small size while still retaining mechanical ruggedness. A "B" type of the connector is used to comply to the USB specification requiring a "B" type connector for *downstream* devices.[49][50]

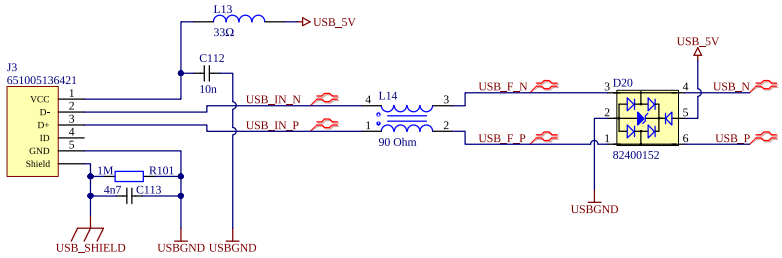


Figure 4.21: USB connector with input filtering and ESD protections.

The connector's leads are firs led through protections and decoupling needed to ensure proper operation of the subsequent circuitry.

Connector itself contains shield ground and signal ground. Termination of a shielded cable is always a space for spirited discussion among the engineers.[51]

The design opted for implementation of both high value resistor with small capacitor in parallel, connected to the signal ground, effectively leaving the shielding open-circuited except for high-frequency signals, which will be shorted to the ground through the capacitor.[52] Should any problems arise, the components can be easily removed or replaced.

Power filtering is accomplished by combination of ceramic capacitor `C112` and ferrite bead `L13`.

Signal conditioning is realized by common mode choke `L14` of 90Ω impedance, matching the impedance of used twisted pairs in the USB cabling. To protect the integrated circuit from damage, a `D20` diode array combining both signal TVS and a power clamp diodes was added to the circuit.

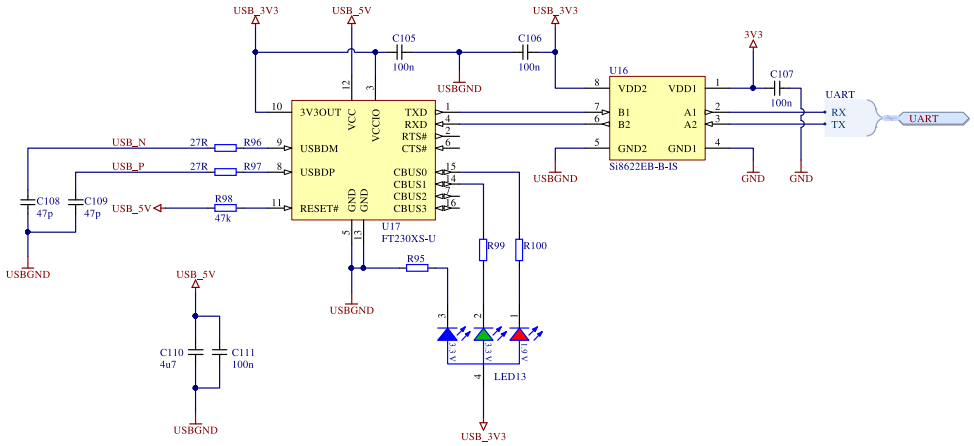


Figure 4.22: USB to UART interface with galvanic isolator integrated circuit.

The *FT230X* integrated circuit was selected for the USB to UART conversion part. It allows a direct operation from the USB power rail without a need for an external regulator.

Protected USB signal is routed through a 27Ω resistor and 47pF capacitor to prevent any signal integrity problems with using a long cable. 5V bus power is routed into the `VCC` pin of the integrated circuit.

The chip contains an integrated dropout regulator to stabilize and to power the entire isolated circuitry. Also, a RGB LED diode was added to the design to indicate function of the circuit.

To isolate the USB from rest of the board a *Silicon Labs' Si8622* digital isolator is used in 1/1 configuration. This isolator's parameters are similar to the previously described *Si864x*.

4.11 SD card storage

The SD card slot was added into the design to allow for removable diagnostic data capture and parameterization of the motor controller functionality without need for device reprogramming.

To connect SD cards to the device, a board must be fitted with a proper slot. SD cards come in variety of form factors. While being different, the electrical interface is consistent among them, specified by the *SD Association*. Nowadays the most commonly encountered form factor is a *microSD* card.

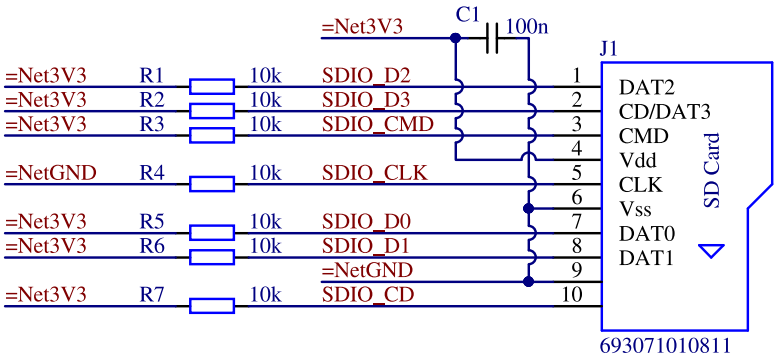


Figure 4.23: *microSD* card slot schematic design.

Micro SD cards' signals require defined levels during its entire operation. This is ensured by adding resistor pull-ups and pull-downs in the design. A decoupling capacitor is a must for a proper power conditioning.

The block schematic uses an Altium Designer's feature called *device sheets* to allow for a design reuse by different boards. This is why the net names use parametric notation (starting with equal symbol) to allow for real net name substitution in a design instantiating this block.

From an interface viewpoint, the SD cards utilize a high speed serial bus. In its 4-bit version the bus consists of 4 data lines, clock line and command data line. Additionally, a single line is used to detect presence of the card in the slot by GPIO of the micro-controller.

Used micro-controller supports a SD cards' native interface with bus widths up to 8 bits and declared maximum clock frequency of 48MHz. This can be stretched up to 50MHz without impairing interface's functionality.

By using 4-bit with bus, a theoretical maximum throughput of 200MHz can be reached, translating into 25MBytes/s of raw data throughput. Needless to say, these calculations do not consider for any overhead.

4.12 Identification memory interface

To uniquely identify connected motors and power boards to the control board, a concept of identification memories was implemented. It is currently used in e.g. printer cartridges or consumer electronics.

Every motor and power board will carry an EEPROM memory, which alongside a writeable area contains a unique, immutable identification number. This number can be freely read and used to identify connected devices.

The design uses a *DS2431* memories manufactured by *Maxim Integrated*. They utilize a *1-wire* serial bus. As the name suggests, the devices need only a single wire for communication and a connection for ground return path, power is relayed by the communication itself by using communication signal energy to charge internal capacitor.

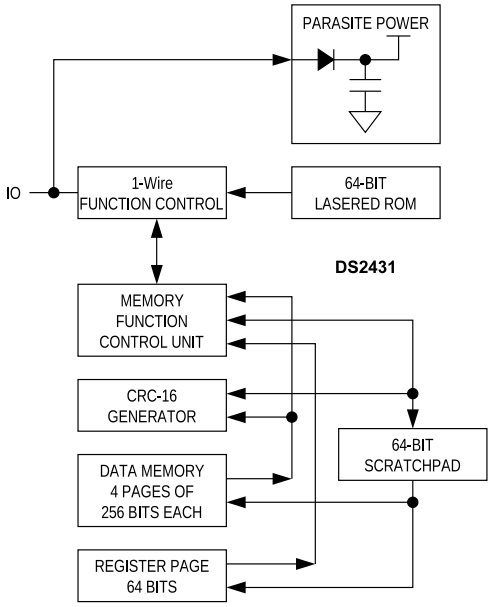


Figure 4.24: Block schematic of the used memory, illustrating the *parasite power supply*.[53]

It is possible to connect multiple devices onto a single bus while maintaining communication with all of the connected devices. Conceptually it is a single-master, multi-slave bus. The 1-wire bus can be also used for a digital temperature sensors reading in the motor controller.

More relevant information about this bus and communication protocol can be found in the Application Note 1796.[54]

Used micro-controller does not explicitly contain an interface peripheral for 1-wire bus, but a standard UART peripheral can be readily used with a slight hardware modification.

The UART of the micro-controller is a two wire bus with push-pull output for data transmission and an input pin for data receive. By using an open-drain buffer circuit (or integrated circuit), it can readily work with the 1-wire bus as illustrated in the manufacturer's application note. This note also details method of UART peripheral adaptation to the 1-wire communication.[55]

4.13 Temperature sensors

Used electric motors contain an *KTY84* series, a silicon-based, resistive temperature sensor with positive temperature coefficient.[56]

Also a motor controller itself contains several resistive temperature sensors to ensure proper working temperatures.

To successfully read these sensors, an integrated solution was selected to reduce complexity of the circuit board. The board employs a *LTC2983* multi-sensor measurement system with ability to measure multiple temperature sensors of various standard types – thermocouples, thermistors and resistive temperature sensors.

This integrated circuit allows to measure up to 20 reconfigurable analog inputs with measured data conversion by pre-programmed coefficients[5], fault detection of converted sensors. Device also contains a current source for resistor-based temperature sensors excitation. Communication with the host system is realized by a standard SPI communication interface.

From hardware viewpoint the device requires proper decoupling of the power inputs and a higher value capacitors for proper operation of internal power regulators.

Documentation also suggests placing a low value, precision capacitors on the analog inputs for noise suppression. A precision sense resistor must be added in order to allow sensing of the resistive temperature sensors – used integrated circuit employs ratiometric sensing. The SPI communication interface needs a pull-up resistor on its chip select line to prevent spurious control actions during host inactivity.

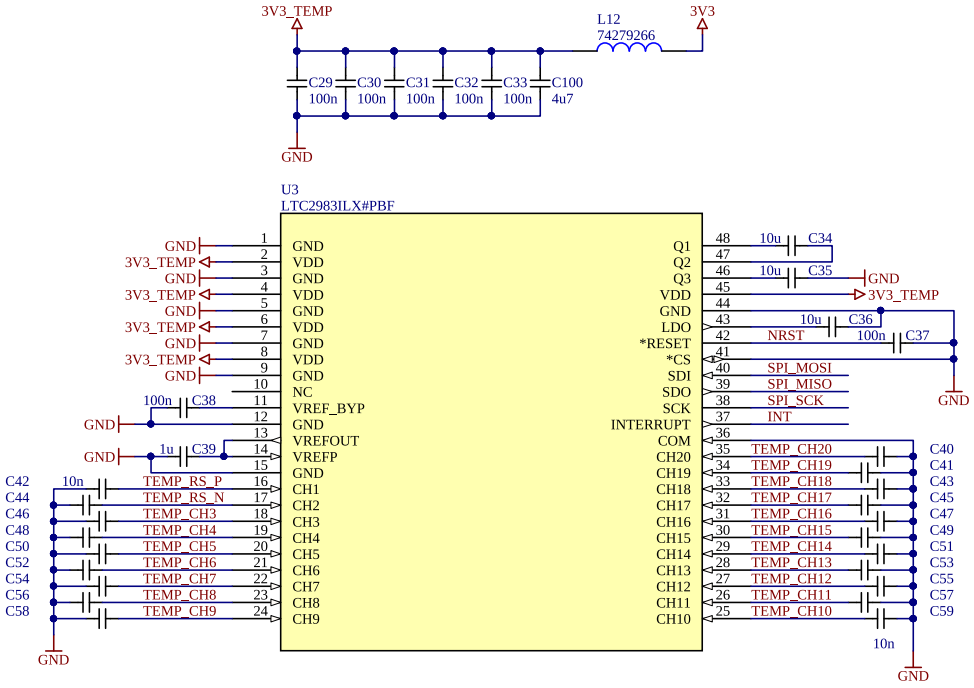


Figure 4.25: Schematic of *LTC2983*'s implementation in the design.

4.14 Coolant pump control

While a pump control will not be under motor controller's supervision for the newest vehicle, it is a required feature for maintaining compatibility with older vehicles. Power output switching is realized by using a *VND7020* dual high side switch manufactured by *ST Microelectronics*.

Since all the vehicles have been retrofitted with pumps working with 24V power input, it is not necessary to provide multiple rail selections.

[5] with ability to enter custom coefficients

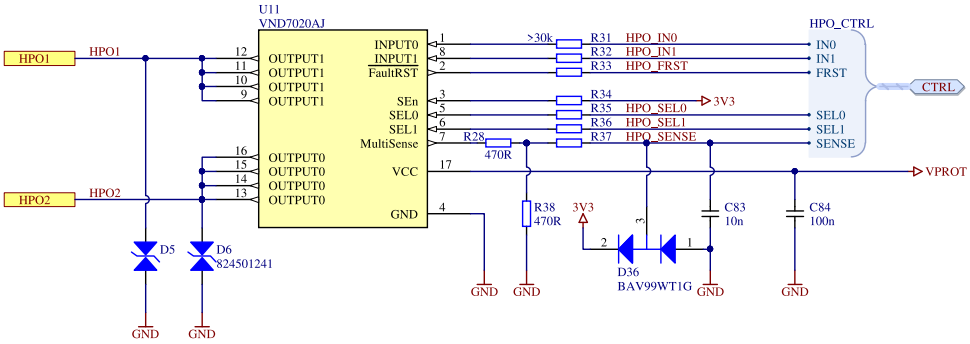


Figure 4.26: Schematic of the high side switch for coolant pump control.

The high side switch's power input is derived from motor controller's protected vehicle bus. Outputs of the switch are protected by TVS diodes to prevent inductive spikes from damaging the chip. Switch's operation is controlled by a micro-controller's GPIO pins. To protect micro-controller from various transients resulting from load switching, resistors of at least 30kΩ were calculated to be added in series with the signal lines. Individual switch outputs are toggled by applying voltage to the `INPUT0` and `INPUT1` pins.

Circuit also possesses an ability to sense both channels' current flow, input voltage level and chip's temperature. These can be read by analog-to-digital converter via `MultiSense` pin.

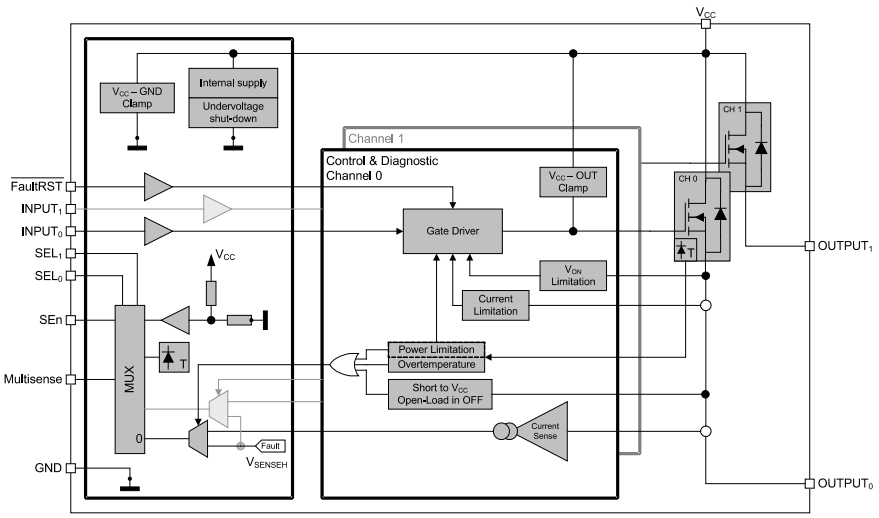


Figure 4.27: Block diagram of used high side switch.[57]

Resistive divider on the `MultiSense` analog output is necessary for keeping readout of the `VCC` voltage within ADC's acceptable levels. It is also necessary to convert current flow provided by internal current mirror into voltage levels readable by the ADC. Transfer functions for these signals can be obtained from device's specification.[57]

These diagnostic outputs are multiplexed into a single pin, and they can

be selected individually by applying voltage to the SE0 and SE1 pins.

Additional measure of the ADC protection is a clamping diode D36. Analog signal is finally filtered and stabilized by a combination of R37 and C83. It is placed close to the analog-to-digital converter input to ensure noise-free signal sensing.

4.15 Programming interface

To allow for firmware and configuration loading a programming interface must be added. These usually range from several test-points on the boards to dedicated connectors or even whole programming probes, integrated on the circuit boards.

The used micro-controller can utilize two programming interfaces – JTAG or SWD.

JTAG (IEEE 1149.7) is an industry standard for debug and programming probe serial interface. It can be found on most of the current embedded systems (microcontrollers, microprocessors, programmable logic devices, complex integrated circuits, etc.). Originally was designed as a test probe interface (*boundary scan*) for inspecting connections between test probe-unreachable integrated circuits.

The JTAG can be used in daisy-chain configuration, where individual integrated circuits form a *chain* in which the data is consecutively passed unit after unit. Basic JTAG uses 4 lines for operation – data in (TDI), data out (TDO), clock (TCK) and mode select (TMS), additionally a reset pin (TRST) is added to allow for hardware reset from the debugging probe. More information on JTAG can be found either in the standard or on the internet.[58][59]

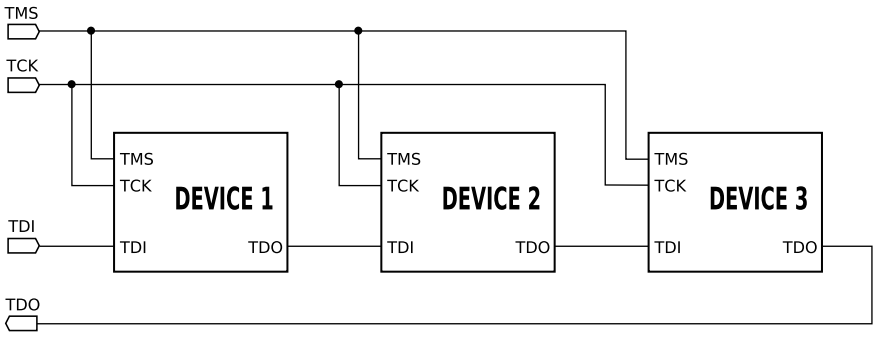


Figure 4.28: JTAG chain example.[59]

Serial wire debug interface (SWD) is a reduced variant of the JTAG used by ARM processors. It utilizes only clock (TCK) and mode select (TMS) lines for its functionality. It cannot be daisy chained.

The motor controller's control board's design selected programming connector approach, winning with its simplicity and variability of programming probe use.

A 20-pin, 2.54mm box connector was selected thanks to being present on the official *ST-Link V2* programming probes supplied by the micro-controller

manufacturer. The connector accommodates both JTAG and SWD interfaces alongside with 3.3V rail voltage sensing, reset, and needed ground connections. It can be also used for safety chip configuration loading.

Programming connector circuitry also includes TVS diodes for digital signal protection and necessary pull-up and pull-down resistors to satisfy JTAG level requirements.

4.16 Debug interface

In order to give insight into motor controller's function a two *SMA* connectors with direct connection to the second DAC channel and event output of the processor were added. These can be connected to an oscilloscope to allow for real-time reading of requested variable and/or event.

Previous revision of the board used a *BNC* connector for the DAC output but it has proven to be quite bulky. On the other hand, a *BNC* – *BNC* pigtails are quite common, unlike the *BNC* – *SMA*.

Again, due to being an output connector from the board, a TVS diodes are placed on both outputs to prevent damage. The event output is a high speed digital output which if applied to a coaxial cable without proper impedance matching would cause a signal integrity problems. Therefore, a low value resistor is placed in series with this line before entering the *SMA* connector.

4.17 Printed circuit board

Much like the power board, the control board was also designed in the *Altium Designer*. To accommodate high component integration on a relatively small board area, a four layer printed circuit board stack-up was selected for the design.

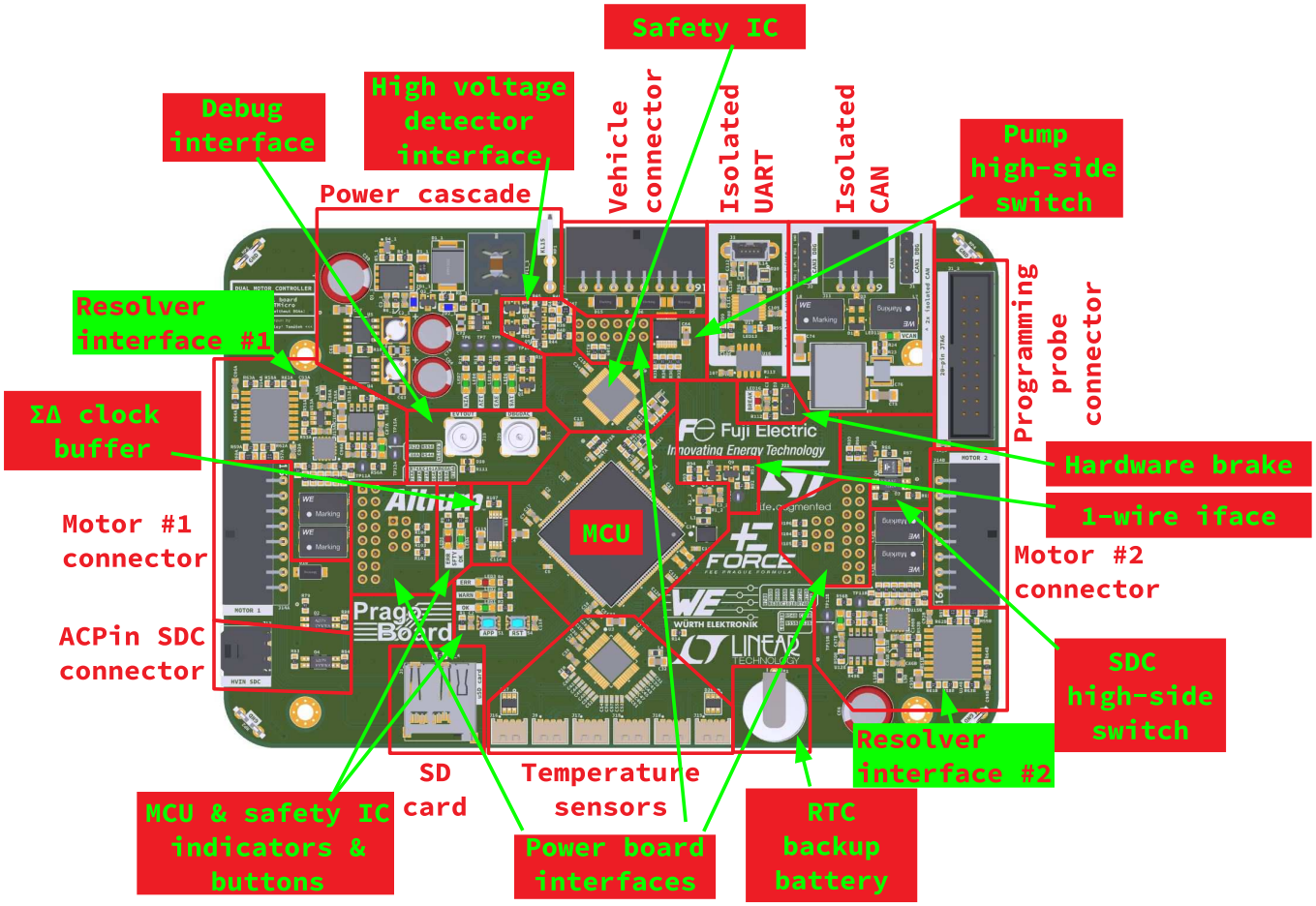


Figure 4.29: Control board with marked areas of every described hardware block.

Input vehicle connector is located on top edge of the board in the middle. The isolated CAN circuitry is located on the right side of this connector, next to the isolated USB interface.

Galvanically isolated interfaces' isolation gap is 2mm, providing isolation up to 900V according to the *IPC-2221B* standard. The rules do not explicitly define required isolation parameters for an external equipment isolation.

Power cascade of the motor controller is located on the top of the board close as possible to the input connector in order to reduce parasitic effects of long power leads. The switching-mode power supplies' design aimed to ensure the smallest possible current loops to eliminate electromagnetic emissions into both subsequent circuitry and into the vehicle.

Integrated circuits are placed horizontally on a center plane with 45° rotation to allow for two-sided access from both power board and motor connectors which are located on left and right sides of the board.

Connectors for the motor low-voltage harnesses, containing resolver, temperature, shutdown circuit and identification memory lines are located on the edges of the board. These are routed to their respective processing circuits, most prominent being the resolver processing circuitry.

The resolvers' circuitry possess a dedicated ground planes, separate from the digital ground plane, these are led under the signal traces all the way to the micro-controller and joined with the micro-controller's analog ground. Digital ground is poured in all other layers with a sufficient via stitching, therefore effect of the ground splitting should be negligible. Thanks to the resolvers' circuitry being identical to both motors, the feature of *room copying* was used again to eliminate need for unnecessary design duplication.

Chapter 5

Motor controller firmware

This chapter details development of the primary micro-controller's firmware in relation to the theory and hardware described in earlier chapters of the thesis.

The firmware implements a *direct field oriented control* described in the theory chapter.

The motor controller uses a *ST Microelectronics' ARM*-based 32-bit micro-controller equipped with a dedicated floating-point unit, plethora of peripherals and a peak core clock frequency of 100MHz with declared processing throughput of 125*DMIPS*.

A two firmware versions were developed simultaneously on both prototype unit and the newest vehicle unit. The prototype unit firmware uses a simpler programming model, based around native C language without any operating system. Its purpose is to act as a testbench and possible fallback for implementation of control into release firmware.

The release version of the firmware is being developed concurrently, using the C++ language alongside with the *FreeRTOS* operating system to allow for scalability and further extensibility of the codebase by the team.

Currently, only the C-based firmware has been fielded in a motor controller of the fourth generation vehicle and therefore will be discussed primarily.

The chapter will be split into following sections, each detailing major aspect of the firmware implementation. The sections will also gradually explain used peripherals of the micro-controller.

- Tools and libraries.
- Clock initialization.
- Power board handling.
- Pulse-width modulation generation with space vector modulation.
- Sigma-delta modulator processing.
- Resolver excitation & angle tracking observer.
- Field-oriented control implementation.
- Temperature sensors integrated circuit interaction.

- CAN bus communication.
- Debug USB to UART.
- SD card with *FAT* file system.
- Identification memory interface.

5.1 Tools and libraries

The base of the micro-controller's firmware is usually provided by the manufacturer. These libraries contain basic initialization code of the micro-controller's core functionality which can be used to *jump-start* the development. These libraries contain complete API with definitions of register addresses, control values and functions needed for interaction with micro-controller and its peripherals.

STMicroelectronics currently offer three sets libraries for their micro-controllers of the *STM32* family.

- **SPL** – *Standard Peripheral Libraries (StdPeriph)* – the oldest library and currently discontinued in further development. It is a low-level library, its functions are interacting directly with the micro-controller's registers.
- **HAL** – *Hardware Abstraction Layer library* – an intended successor to the SPL, used primarily by the *STM32CubeMX* code generator tool. Its implementation is more complex, with various abstraction layers in the library which allow the developers to reuse already developed code even when developed for different micro-controllers.
- **LL** – *Low Level library* – This library aims at providing replacement for the discontinued SPL. It will bring back the low-level approach, providing the developers with tighter control of the micro-controller. It is still in active development and therefore not available for all the micro-controller families and their respective peripherals.

For motor controller's firmware a *SPL* was chosen for its low-level approach, giving the most control over the hardware, while supporting every used peripheral in the controller at the expense of an occasional software bug.

Next decision is which software development tools to use. There are many options ranging from simple *Makefile* scripts with command line-based debugging interfaces to a fully-fledged integrated development environments with plethora of features. To ease the initial setup requirements an IDE were used for both firmware editions of the controller.

The C-based firmware was developed using the *Keil V5* IDE while C++ based firmware was developed with *Atollic Studio* based on the *Eclipse* IDE.

While *Keil* possesses an advanced compiler and solid debugging facilities, its user interface lacks some important features (GIT VCS integration, complex

project management) and work-flow found in the *Atollic Studio* which on the other hand use open-source GNU compilers (*gcc*, *g++*) and debugger (*gdb*), lacking performance of the ARM tools found in the commercial *Keil V5*.

Selection of the *FreeRTOS* as used operating system was motivated by good documentation and proven support for the STM's micro-controllers and author's experience with its usage.

5.2 Micro-controller initialization

The firmware's starting point is basic initialization of the micro-controller itself. After reset, the code initializes interrupt vector table and performs initialization of the FPU and internal clock within the `SystemInit` function. While the implementation of the `SystemInit` function is provided by the library, a custom implementation can be created.

After this initial setup the `main` function starts with execution.

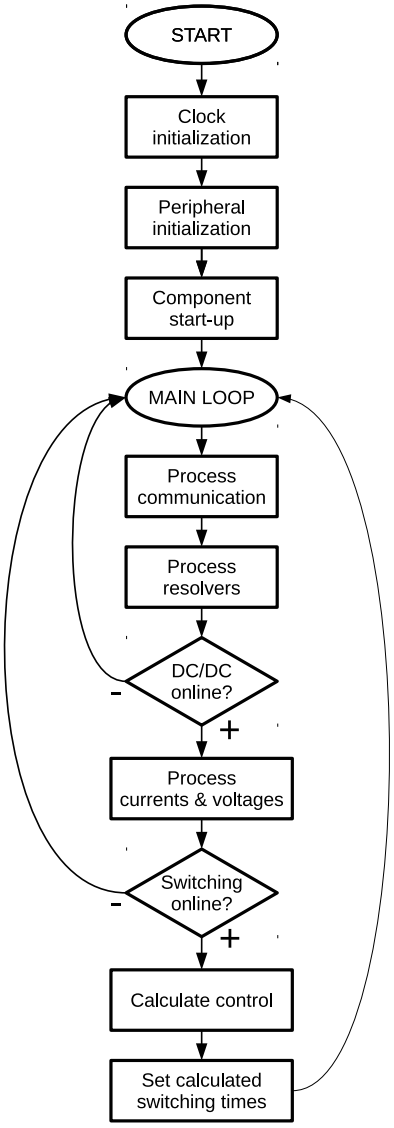


Figure 5.1: Flowchart of the designed motor controller program.

All the used peripherals are consecutively initialized to ready them for motor control operations. Control itself is performed in the infinite loop.

5.2.1 Clock initialization

Before any of the control peripheral initialization a system clocks should be initialized to utilize a precise external oscillator with maximum allowed clock frequency of the micro-controller, which is 100MHz.

At the start-up the device is initialized to use its internal clock source *HSI* with frequency of 16MHz.

The clock initialization routine sets flash memory access latency to 3 cycles in order to allow flash memory operations completion with a higher clock frequencies and enables flash memory prefetch to avoid a performance hit.

After increasing the latencies, the device's *PLL* is first ensured to be disabled, then the *HSE* clock is enabled and the code waits for assertion of the HSE's availability. Should the start fail, the device will assert a fault and will stop the code execution.

With *HSE* running, a *PLL* is ready to be configured. In order to select a proper *PLL* coefficients to obtain desired frequencies, the *STM32CubeMX* configuration tool has been used. This tool contains a clock configuration tool, loaded with all constraints of the clock system for a selected microcontroller, alleviating any misconfiguration concerns. A complete clock tree of the *STM32F423* can be found in the section 6.2., figure 13 of the device's reference manual.[60]

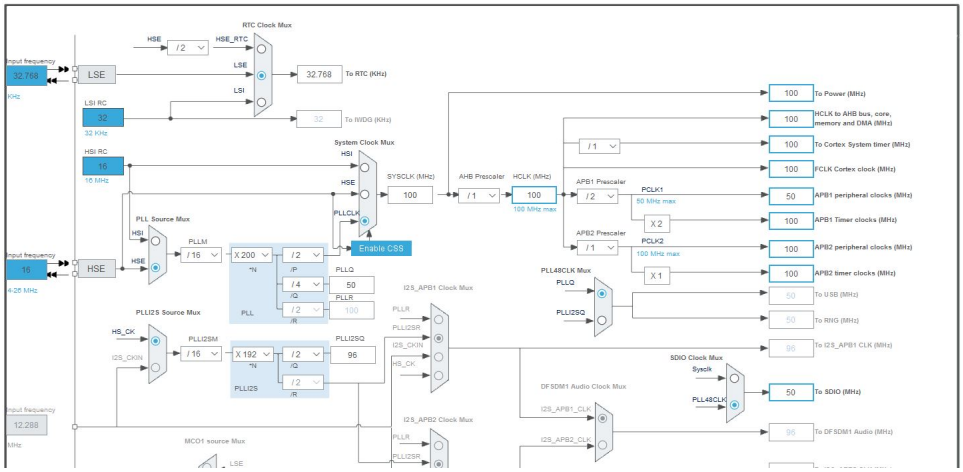


Figure 5.2: Part of a clock tree visualized in the *STM32CubeMX* clock tuning tool.

PLL is loaded with proper coefficients and is started with *HSE* selected as a clock source. The code waits for a *PLL* lock. After successful *PLL* initialization, a clock dividers for internal buses must be entered. The *STM32CubeMX* clock configuration tool can be used again to select proper divider ratios, while achieving maximum allowed clock frequencies.

Finally, the *PLL* clock is selected as a primary system clock and after a quick verification of proper clock setting, the clock configuration routine finishes.

Each peripheral has a clock domain control managed by the `RCC` component of the MCU. Clock domain must be enabled before any interaction with a required peripheral. It can be also disabled to turn off the peripheral, reducing power consumption of the controller.

5.3 Power board interfacing

The power board requires several control signals in order to allow for switching action of the integrated power modules.

5.3.1 Isolated DC/DC enable

First required signal is for enabling power to the isolated DC/DC converters. This signal is served directly from the basic GPIO peripheral.

To initialize a GPIO for output a clock for respective GPIO group must be first activated by means of the `RCC` peripheral, the GPIO are bound to the `AHB1` clock domain. After clock enabling, a configuration of the peripheral's registers specifying direction, output speed, pins and eventual pull-up/down resistors. Output state of individual pins can be controlled by writing into `ODR` or `BSSR` registers. To read pin state, individual bits from the `IDR` register can be polled.

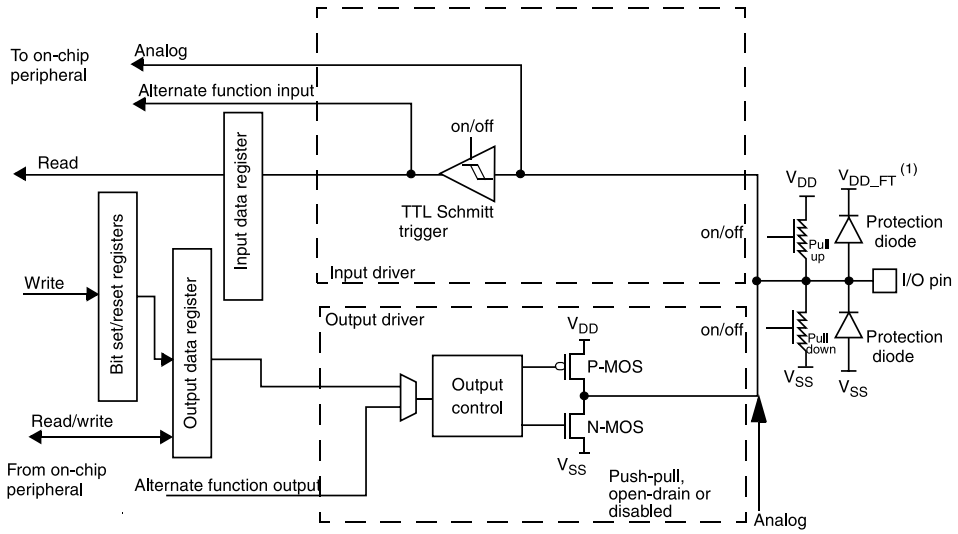


Figure 5.3: Basic structure of a five-volt tolerant I/O port bit.[60]

GPIO's configuration can be also locked by means of `LCKR` register, to prevent accidental or spurious configuration changes.

The power enable of the DC/DC converters is governed by the vehicle's state which is received via CAN bus message.

5.3.2 Switching pulses buffer enable

Second required signal is a switching pulses buffer enable. This signal is actually generated by the board's safety chip, based on a state of shutdown circuit, over-current protections or any previously latched error.

MCU also sends a signal confirming the vehicle's and motor controller's readiness for switching and possible driving.

5.4 Pulse-width modulation generation

A pulse width modulation is used in order to generate switching signals for the power modules, which will result in generation of a proper voltage vector

for 3-phase AC motor driving.

To generate a switching pulses, an advanced timer peripherals of the *STM32* are used. A single timer allows generating up to 3 complementary PWM pairs with automatic dead-time insertion. Used MCU posses two of these advanced timer peripherals, giving exact possibility to drive two 3-phase AC motors simultaneously.

Generally speaking, the timer works as a counter of pulses, given by a source clock and prescaler. Once it reaches specified value an action is usually asserted. Timers can be also bound to the micro-controller's pins to interact with other devices and are therefore used for precise action timing, pulse generation, PWM generation, pulse counting or a pulse time measurement.

5.4.1 Timer initialization

Routine for a PWM generator initialization use a following procedure for both advanced timers. First, all the used PWM GPIO pins are initialized into alternate-function mode in order to be utilizable by the timer's output.

Timer initialization in the SPL is split into base timer initialization and subsequent initialization of a specific requested features.

The base timer initialization needs to set a prescaler and an auto-reload values which will set the switching frequency. Counter alignment influences direction of the counting, the center-aligned counter mode sets the timer into configuration suitable for high-power polyphase inverter control.

The counter will first count up until reaching auto-reload value, afterwards it starts to count down until it reaches 0, restarting the whole process.

Repetition counter allows for choosing of the update event firing instant, as illustrated on the figure below.

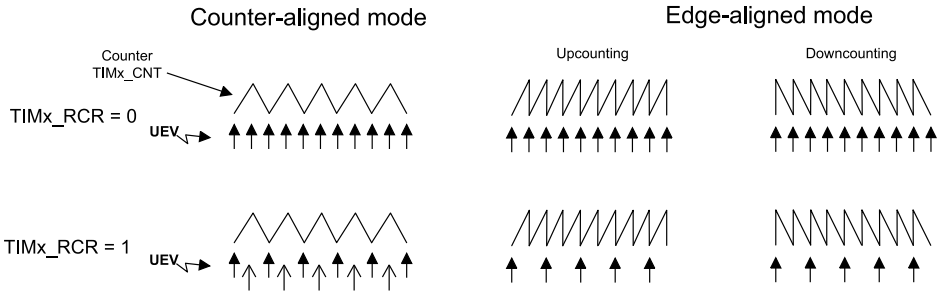


Figure 5.4: PWM edge aligned versus center aligned counting examples with various repetition counter setting.[60]

Center-aligned mode ensures that switching action of the individual phases do not always occur in a same time, but will be spread through an entire switching period.

Should an edge aligned mode be selected for the timer counting, a switch would occur at the same time with every switching period, causing excessive voltage drops on the DC-link capacitors with associated EMI emission.

With timer base initialized, an output compare block must be initialized to allow for a PWM output generation. The output compare specifies whether to generate complementary or a single ended PWM, polarity of the generated pulses and idle output state. The complementary outputs can be now enabled.

Advanced timer-specific initialization entails emergency break signal toggle and polarity with dead-time specification and peripheral locking, similar to already described GPIO lock. After advanced initialization the PWM output control can be enabled.

Both outputs are then synchronized by using master/slave mode capability of the advanced timers with output event generation based off the repetition counter value.

Finally, the update event interrupt is enabled in the `TIM1` and `NVIC` to allow for a motor control algorithm update scheduling based off these PWM-generating timers.

With initialization complete, the timers' actual operation is enabled after all other motor controller peripherals' initialization being done.

5.4.2 Space vector modulation

The space vector modulation is tasked with generating a proper voltage vector, based off a requested voltages in d, q reference frame provided by the control algorithm, alongside with an estimated rotor electrical angle by the angle tracking observer.

The actual generation is based off the *CMSIS* libraries, providing the Inverse Park transformation and implementation described in[61]. The described space vector modulator implementation rely on modified inverse Clarke transformation and a sector identification from sign of the transformed voltages in α, β coordinate system.

After sector identification a switching times t_a, t_b and t_c are calculated from a sector-specific equations. These switching times are fed into the PWM timers to modulate requested voltage vector. In order to prevent partial load into the timers' output capture registers an update must be disabled during register writing.

5.5 Sigma-delta modulator processing

The sigma-delta modulators emit a high-speed digital signal representing a measured analog value. This signal must be filtered in order to retrieve modulated signal. The `DFSDM` peripheral of the used MCU implements *sinc* filters to perform necessary filtering.

The `DFSDM` peripheral is split into channel and filter sub-modules. The used micro-controller has two `DFSDM` peripherals each with 2 and 4 filters and with 4 and 8 input channels. Each individual `DFSDM` peripheral is capable of generating a clock signal, used for a signal modulation by the converters. The clock signal rate can be modified by using a built-in prescaler.

The channel represents a physical pin of the MCU, receiving the modulated data stream. These channels can take care of the over-current protections thanks to each having their own dedicated low-order *sinc* filter for watchdog functionality and a 1/0 counter for a fast short-circuit detection. This over-current detection can be connected internally to the break input of the PWM-generating timers, allowing seamless interruption of PWM generation without any firmware intervention. Channel can also detect a missing input data by clock absence.

Filters are used to convert bound channels into original signals. The firmware implementation uses channels and filters in 1:1 relation, allowing continuous conversion of the data at the maximum allowed sampling rate for certain oversampling ratio. Sampling rate can be calculated by following equation.

$$f_s = \frac{f_{mod}}{OSR} \tag{5.1}$$

Where OSR represents selected oversampling ratio of the filter and f_{mod} is the modulation frequency generated by the `DFSDM` peripheral. It should be noted, that a filter order does not enter this equation thanks to using a continuous conversion.

5.5.1 Peripheral initialization

Initialization routine is split into two, where first sets up whole `DFSDM` peripheral for modulation clock generation and a second one for individual channel-filter couples.

The master routine first initializes GPIO in alternative mode for clock output, starts the `APB2`-associated clock for the peripheral, sets the *SysClock* as a clock source and provides prescaler value. Finally, the clock generation is started to allow for converters start-up.

The channels' initialization routine also starts the channel's input pin in alternative mode first, afterwards a DMA is set-up to allow for seamless sampling of the data without need for firmware intervention.

DMA requires a source and destination addresses, address increment mode, memory size in word fractions, buffer size, channel which to utilize for data transfer, transfer direction and whether to use normal, circular or double-buffered transfers. Detailed description of the DMA peripheral can be found in the application note.[60]

While the filter outputs data in a 24-bit width into a 32-bit register, the DMA takes only 16 upper bits of the register. Reason for this is the declared effective bit count of the used sigma-delta modulators. DMA also utilizes a circular transfer to keep the conversion running indefinitely since the control algorithm is only interested in the latest data from the filter.

Channel is initialized with used clock and data input sources, right bit shift and data offset calibration. Short circuit and clock absence detectors are left disabled due to DC/DC converters not yet being active. Turning on the

overcurrent detection at this moment would cause instantaneous signalization and subsequent lockout of the PWM drivers.

Filter initialization requires only selected oversampling ratio and a filter order required for conversions. After filter initialization, the channel is instantly bound to the filter, both fast continuous mode and DMA transfers are enabled.

Overcurrent protections are set up in the next step, where both thresholds are set for phase current reading and short circuit 1/0 counter threshold is set. Also, a break signal for both PWM timers is linked to these signals. DC-link measurement do not require any of these protections activated. It may be added in the future to protect against accumulator pack over-/undercharge.

After this initialization, the channel alongside with filter, DMA and conversion is started. The converted data will automatically fill the selected buffer to allow for control algorithm function once all the initializations are complete.

5.6 Resolver reading

The resolver reading is closely bound to the DAC and the ADC peripherals. The ADC is set to process the resolver's values in an *injected* sequence, allowing for auxiliary regular conversions to take place in spare time.

The DAC is set up with the DMA in a circular mode to generate sine-wave at 10kHz frequency with $1.5V_{pp}$ amplitude and 1.65V bias.

The ADC data readout is realized by using interrupt in which the injected channel data is added into a circular buffer. Reason for not using a DMA for automatic transfers is that injected conversions cannot be processed with using DMA. Injected conversions are triggered by `TIM2`, providing with a 20kHz sampling frequency.

5.6.1 Analog peripheral initialization

Both analog peripherals' GPIOs are configured as analog pins.

The DAC uses a single timer `TIM6` to trigger the conversion at 2Msps rate, which is a declared maximum throughput of the peripheral. This timer is used for both DAC channel triggering.

DAC requires setting of output trigger pulse of the `TIM6` binding and whether to use MCU-integrated analog buffer. Data width and alignment is declared by using a specific data-holding register to set the output data. Care must be taken to ensure that generated waveform won't be clipped when using integrated buffer due to not being a rail-to-rail amplifier!

Asociated DMA is configured in a circular mode with DAC holding register of 12-bit, right aligned data `DHR12Rx` where `x` represents output channel.

ADC's initialization must first set master clock frequency for the peripheral by specifying valid prescaler to satisfy condition $f_{adc} \leq 30MHz$. Next a `TIM2` is configured as a trigger for the injected channel sampling with binding to the

ADC peripheral to accept it as a trigger for injected conversion. An injected channel interrupt is also enabled to allow for saving of the measured data.

To convert auxiliary signals (input low-voltage power measurement, *MultiSense* of the high side switch controlling the pumps, etc.) a DMA is setup to automatically transfer converted data into the MCU's operating memory.

The individual injected channels are then setup for reach individual resolver, specifying channel and offset to acquire signed data value.

Additionally, an initialization contains a discrete PI regulator initialization for error to angular velocity processing.

5.6.2 Angle tracking observer

The measured sin/cos channels are processed with an *angle tracking observer*. Unlike from the *arctangent method*[1], it provides precise position readout with angular velocity as a side output. The angle tracking observer works by estimating the angular position and comparing the estimation with measured values from sensor, the resultant error is fed into a low-pass element to obtain an angular velocity.

By integrating velocity a new position estimation is acquired. By continuously performing the estimation, the error will become minimized and the angle tracking observer will acquire a lock on the actual position.

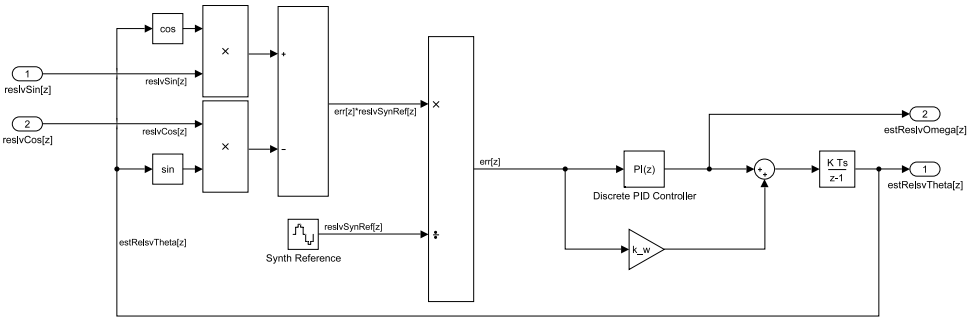


Figure 5.5: Block diagram of firmware-implemented angle tracking observer.

The signal error is calculated using a following trigonometric identity.

$$\sin(\varepsilon) \cdot \sin(\omega t + \varphi) = \left(\sin(\theta) \cdot \cos(\hat{\theta}) - \cos(\theta) \cdot \sin(\hat{\theta})\right) \cdot \sin(\omega t + \varphi) \quad (5.2)$$

For small values of ε the sine function can be discarded thanks to the sine function's linearity when close to zero. This is exploited with locked ATO to save processing performance.

After error calculation, the carrier signal must be demodulated. A phase offset φ must be considered in a real application for a proper demodulation.

Actual demodulation is achieved by dividing calculated error with value acquired from applying DAC's DMA current pointer to a pre-calculated lookup table.

[1] Method using `atan2` function to acquire angle – extremely susceptible to the noise on the signal lines, unstable in the function's interval extremes due to a division by zero

Demodulated error, saturated into approximately 10° range is then fed into a discrete PI controller to acquire angular velocity.

Velocity is then used alongside with the right-shifted demodulated error (division by 2^n) to estimate a position.

5.7 CAN bus communication

The motor controller is capable of utilizing two CAN buses simultaneously.

CAN peripheral's initialization's primary concern is to provide correct timing quanta with respect to the vehicle's selected signalling rate and CAN peripheral clock frequency, needed for bus state sampling instant definitions. These are defined in the CAN bus standard.[62]

A more intuitive approach can be used for time quanta allocation, by exploiting a special tools developed for this purpose. A used one for this firmware development can be found at `http://bittiming.can-wiki.info/`

Peripheral is also initialized with interrupts for completed transmission and received data.

The actual data processing is done by using *CANdb* library, created by the eForce which takes care for the individual messages' processing for both transmission and receive directions. The *CANdb* takes communication defined by a web tool and converts it into C-code which can be embedded into units' firmware.

Messages required from the other units are one describing current vehicle state, needed for the IGBT switching control. Second required message is torque request from the pedal unit, this message is considered system critical and should any timeout occur, the controller must enter safe state by stopping the switching.

5.8 Field-oriented control

Actual control is done in the code's main loop, after proper initialization of all required peripherals.

Implementation of control requires a two *PS* regulators for each motor, each controlling a single decoupled component of the motor's current.

The control is recalculated with every update event coming from the PWM timers. Timer recalculates instant is signalized by interrupt's flag setting, which is polled in the main loop.

The control first uses a windowed average to down-sample the measured phase currents and DC-link voltages. Measured phase currents are fed into modified Clarke transform, accepting first and third phase currents – i_1 and i_3. These currents in α, β stator reference frame alongside with estimated position are fed into the Park transform, acquiring currents in d, q rotor reference frame.

These decoupled currents are subtracted from reference values, where i_q^*

is provided by vehicle's pedal unit[2] after slew rate control in the control algorithm and i_d^* is currently set to zero. Current error values $\varepsilon(i_d)$ and $\varepsilon(i_q)$ are processed in their respective *PS* regulators to obtain required voltage vector u_d^* and u_q^*.

This voltage vector is scaled and saturated into valid range of the measured DC-link voltage. No dead-time or switching element drop compensation was implemented. This altered vector is finally applied to the SVM block to obtain switching times needed by PWM generators.

[2] In later vehicles supplied by the traction-control units.

Chapter 6

Testing & evaluation

To verify developed prototype a series of tests were undertaken. Each test was tasked with testing various functional blocks of the motor controller.

The testing data was acquired by a vendor provided *STMStduio* software tool. It utilizes a standard programming probe for data transfer. This sometimes cause an invalid data readout due to asynchronous nature of data retrieval and aliasing with a higher data rates reaching the throughput limit of the used probe.

6.1 Resolver angle tracking

A rotor's electrical angle is an absolutely crucial parameter, needed to properly decouple phase currents into direct and quadrature components and also to modulate a proper space vector.

While in development, the motor is spun by hand and a zero position is usually evaluated to match the ATO readout.

Alternatively applying a small voltage vector without positional feedback, which will excitate a motor phase aligned with electric zero angle (usually i_α) reading electric angle close to the zero can be used.

This test was undertaken by externally driving the motor from dynamo and reading direction, angle and angular velocity of provided by the implemented angle tracking observer. The angle is analyzed for its expected shape and ranges while angular speed is measured directly on the motor's shaft by using hand-held tachometer and compared to the reading.

Results (B.2) indicate valid readings of both angles, satisfying expected sawtooth shape, and an angular velocity being approximately equivalent to one measured by external tachometer.

6.2 Space vector modulator operation

With ATO operational, a space vector modulation can be tested. By connecting the electrical angle reading a generated switching times from the SVM block can be evaluated.

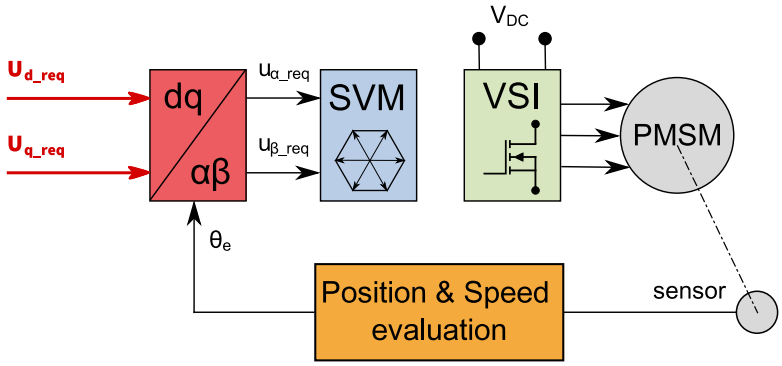


Figure 6.1: Block diagram of performed space vector modulation testing.[21]

The test is done by coupling the previously tested ATO into the SVM block without enabling the VSI's switching action in order to not possibly damage the power modules or motor in case of a possible incorrect function of the modulator.

Results (B.3) show that the modulator generates a proper switching times for a timer peripheral with an expected waveform shape with some occasional glitches, which may be caused by invalid data retrieval by the debugging probe.

6.3 Open-loop operation

By having a functional SVM generator block, a motor can be connected to the motor controller and can be run in open loop mode.

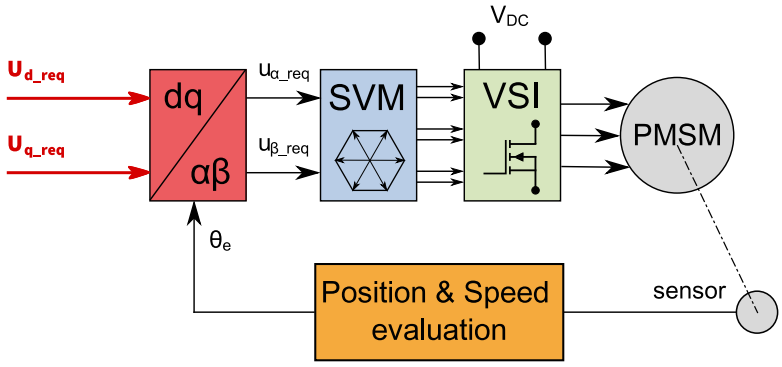


Figure 6.2: Block diagram of performed open-loop motor control.[21]

This control is performed by directly setting requests for the generated voltage vector components. This voltage vector is transformed by the inverse Park and Clarke transformations and applied to the SVM block. Angular position reading must be present in order to correctly orient the voltage vector in the inverse Park transformation.

Both phase current measurements, alongside with transformed currents

from the Clarke and Park transformations can be observed for expected values in this test and to evaluate control's ability to enter closed-loop operation.

Captured data (see B.4) shows that

6.4 Closed-loop operation

A closed-loop function of the motor control can be entered after all aforementioned blocks are working properly. Here, a control loop tuning takes place in order to optimize control's response to the requested torque-producing current, while aiming to maintain stability of the control.

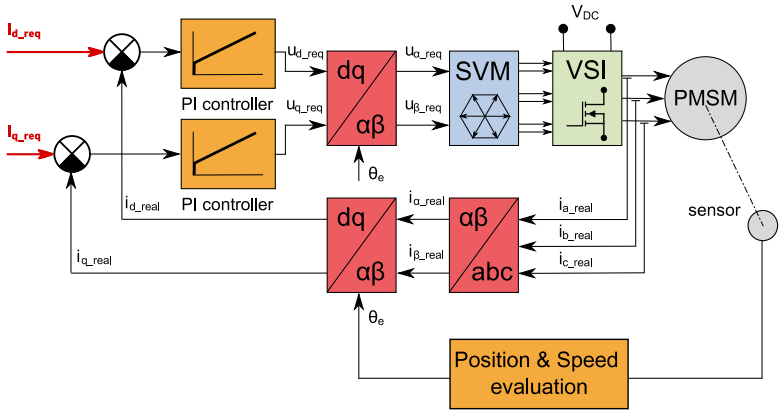


Figure 6.3: Block diagram of performed closed-loop motor control.[21]

Captured data (see B.5) from the testing show that control successfully performs a closed-loop vector control. The torque requests i_q^* are followed closely with some overshoots. Only when the induced voltage reaches the power source levels, the current begins to drop. This could be addressed by implementing the *field-weakening* to the control algorithm. Flux request is set to $i_d^* = 0\text{A}$, but the control is not capable of keeping the current at the set level. This can be caused by improperly tuned PI controllers.

6.5 Vehicle testing

The vehicle testing was not unfortunately possible to this date, due to unforeseen technical difficulties with both motor controller design and several problems in the FSE.04x's electric systems.

Chapter 7

Conclusions

The thesis had described a motor controller design and development in the context of current eForce FEE Prague Formula's vehicle construction.

Thesis had thoroughly described the design alongside with major theory, design decisions and performed work in creating several functional prototypes. It also shown that the implementation of a shunt-based phase current measurement is a viable strategy for a medium-power frequency inverter.

While the thesis failed to do a proper testing in a Formula Student-class vehicle due to a time constraints. It managed to do a good amount of prepwork and the testing so-far managed to verify significant portions of the described design.

The work will continue in order to fully implement designed motor controller into the team's vehicles and will continue with development of both hardware and firmware for upcoming generations...

Appendix A

Acronyms

A

ADC

Analog to digital converter. 83

AMS

Accumulator management system. 5

API

Application interface. 75

ATO

Angle tracking observer. 23, 24, 84, 87, 88

B

BLDC

Brush-less DC motor. 7

BMS

Battery management system. 5

D

DAC

Digital to analog converter. 53, 71, 83, 84

DMA

Direct memory access. 82–84

DTC

Direct torque control. 19, 20

E

EMF

Electromotive force. 7

EMI

Electromagnetic interference. 9, 12, 28, 30, 47, 55, 62, 63, 80

ENOB

Effective number of bits. 30

ESD

Electro-static discharge. viii, 31, 56, 61, 63, 64

ESL

Equivalent series inductance. 33

ESR

Equivalent series resistance. 28, 33, 48

F

FEE

Faculty of Electrical Rngineering (at the Czech Technical University in Prague). 3

FME

Faculty of Mechanical Engineering (at the Czech Technical University in Prague). 3

FOC

Field-oriented control. 20, 22

FPU

Floating point unit. 76

FSAE

Formula Student SAE. 3

G

GPIO

General-purpose input/output. 66, 79–83

I

IDE

Integrated development environment. 75

IGBT

Insulated-gate bipolar transistor. vii, 27–29, 31, 33, 37, 39, 40, 42, 43, 47, 85

L

LDO

Low-Dropout Regulator. 48

LVDS

Low voltage differential signalling. 30, 31

M

MCU

Micro-controller unit. 21, 78–84

P

PMSM

Permanent magnet synchronous motor. 7

PWM

Pulse width modulation. 21, 80–83, 85, 86

R

RTC

Real-time clock. 51

S

SAE

Society of Automotive Engineers. 2

SMT

Surface mount technology. 35

SPL

Standard peripheral library. 80

SVM

Space vector modulation. 86–88

V

VSI

Voltage source inverter. 8–12, 18, 21, 88

W

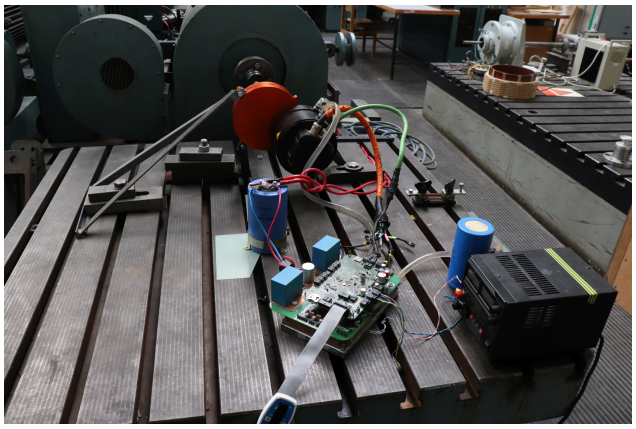
WRL

World ranking list of the FSAE competition. 2

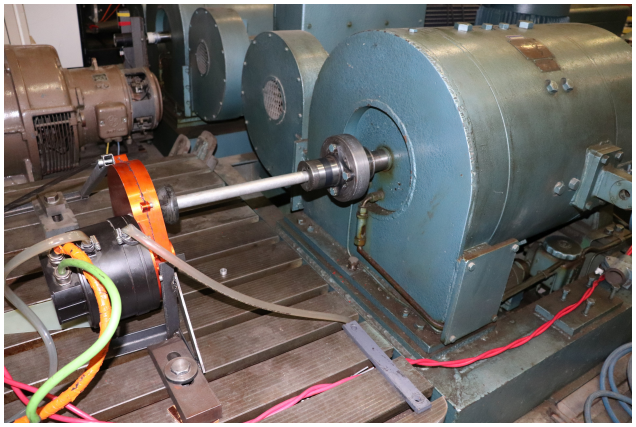
Appendix B

Measurements

The testing was performed on the prototype motor controller. Data were acquired by a vendor provided *STMStduio* software tool. It utilizes a programming probe for data transfer.



(a) : Motor controller with laboratory power supply and connection to the power supply dynamo.



(b) : Rear motor of the *FSE.04x* with gearbox, attached to the dynamometer.

Figure B.1: Prototype motor controller testing setup in laboratory *H26*.

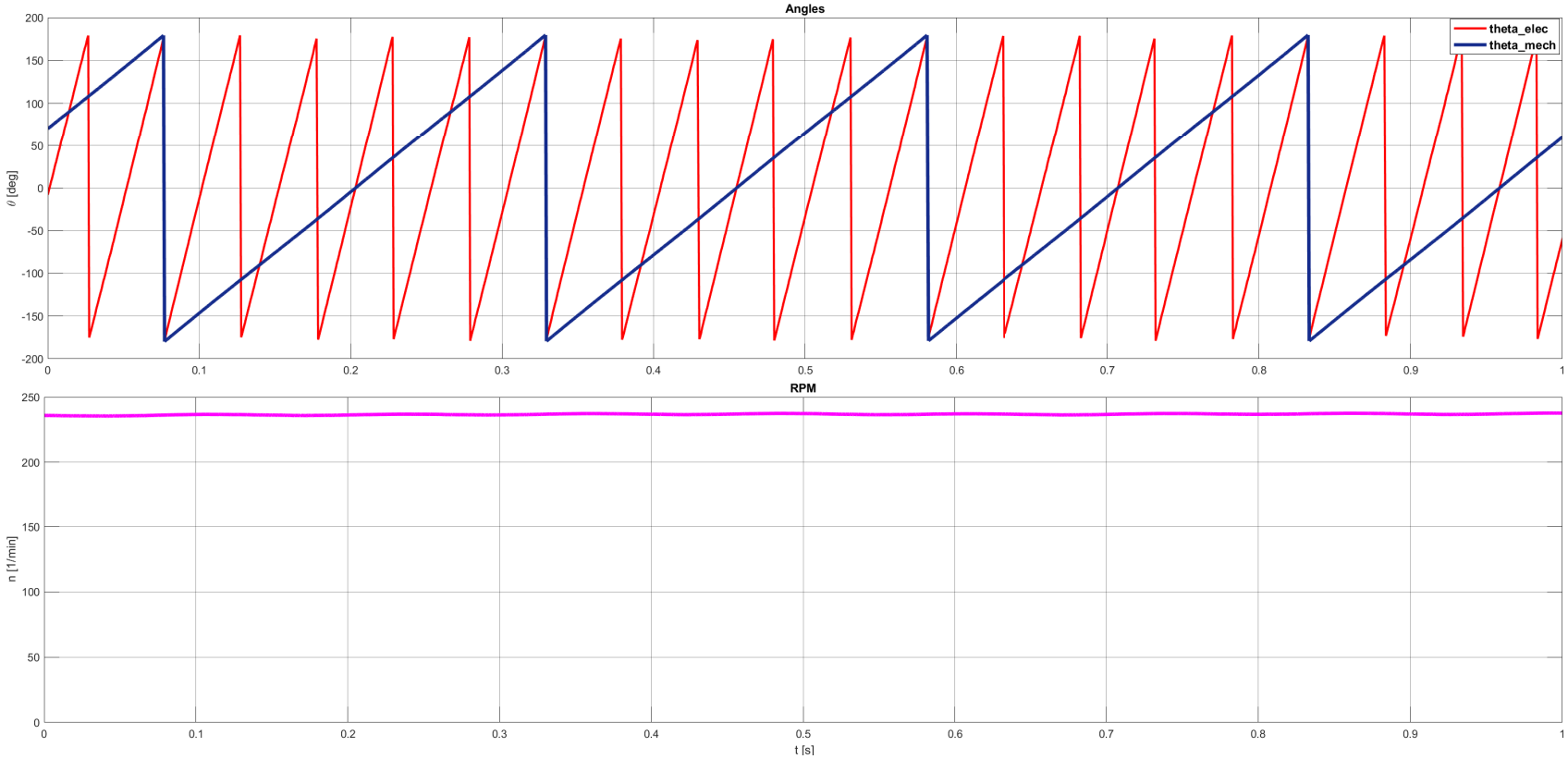


Figure B.2: Measured data of performed angle tracking observer testing.

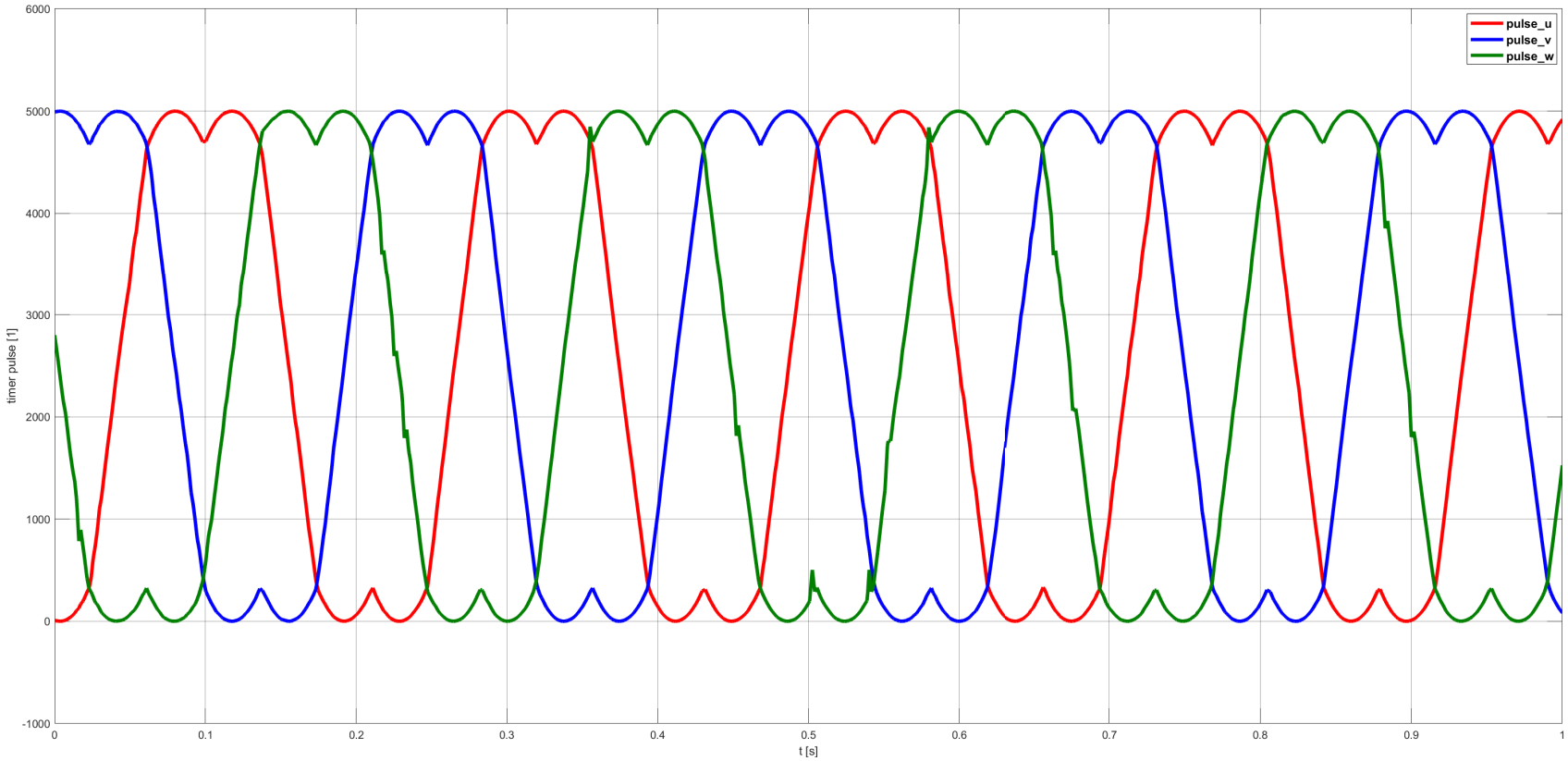


Figure B.3: Measured waveforms of performed space vector modulator testing.

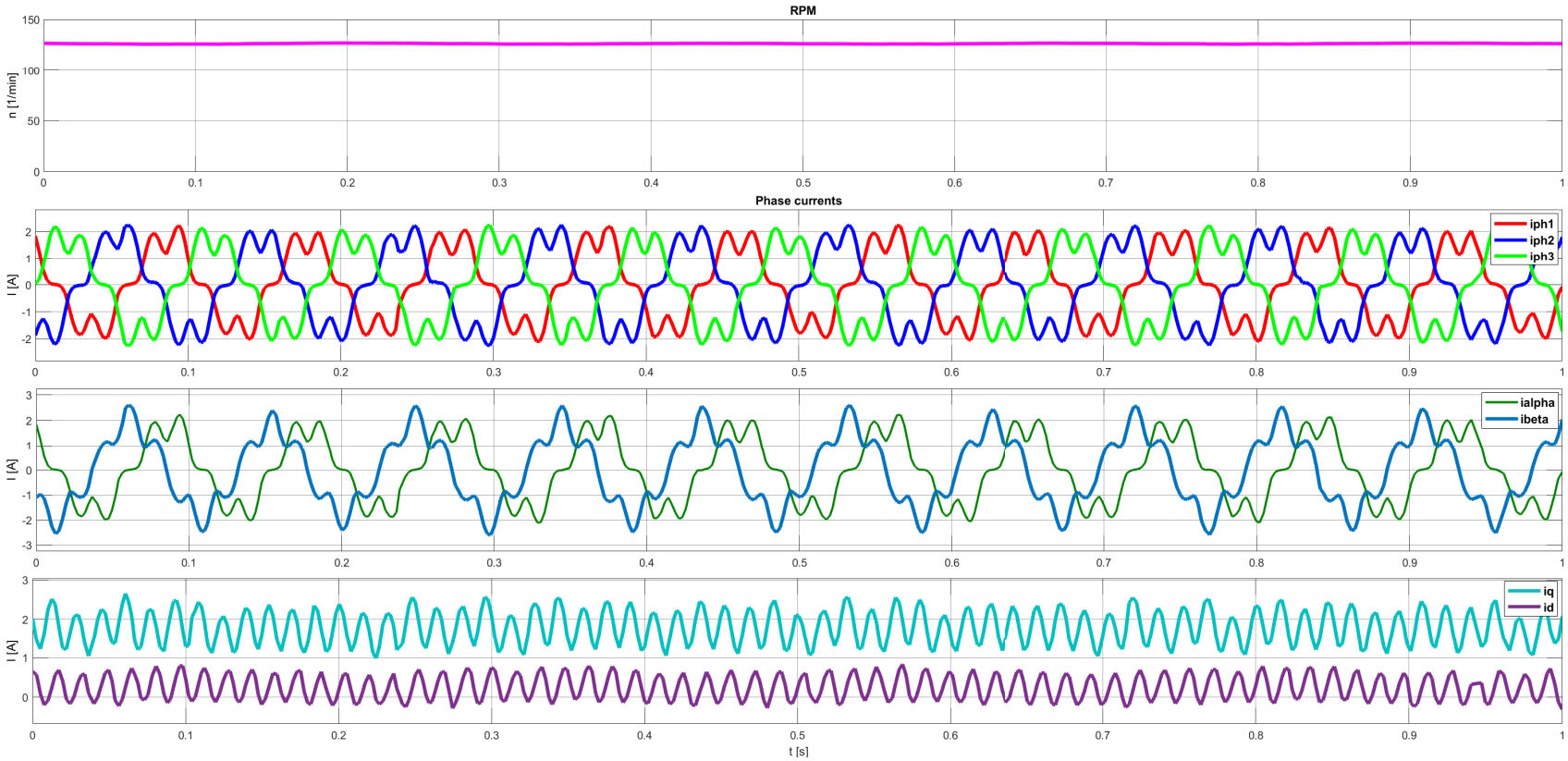


Figure B.4: Measured data of performed open-loop motor control testing.

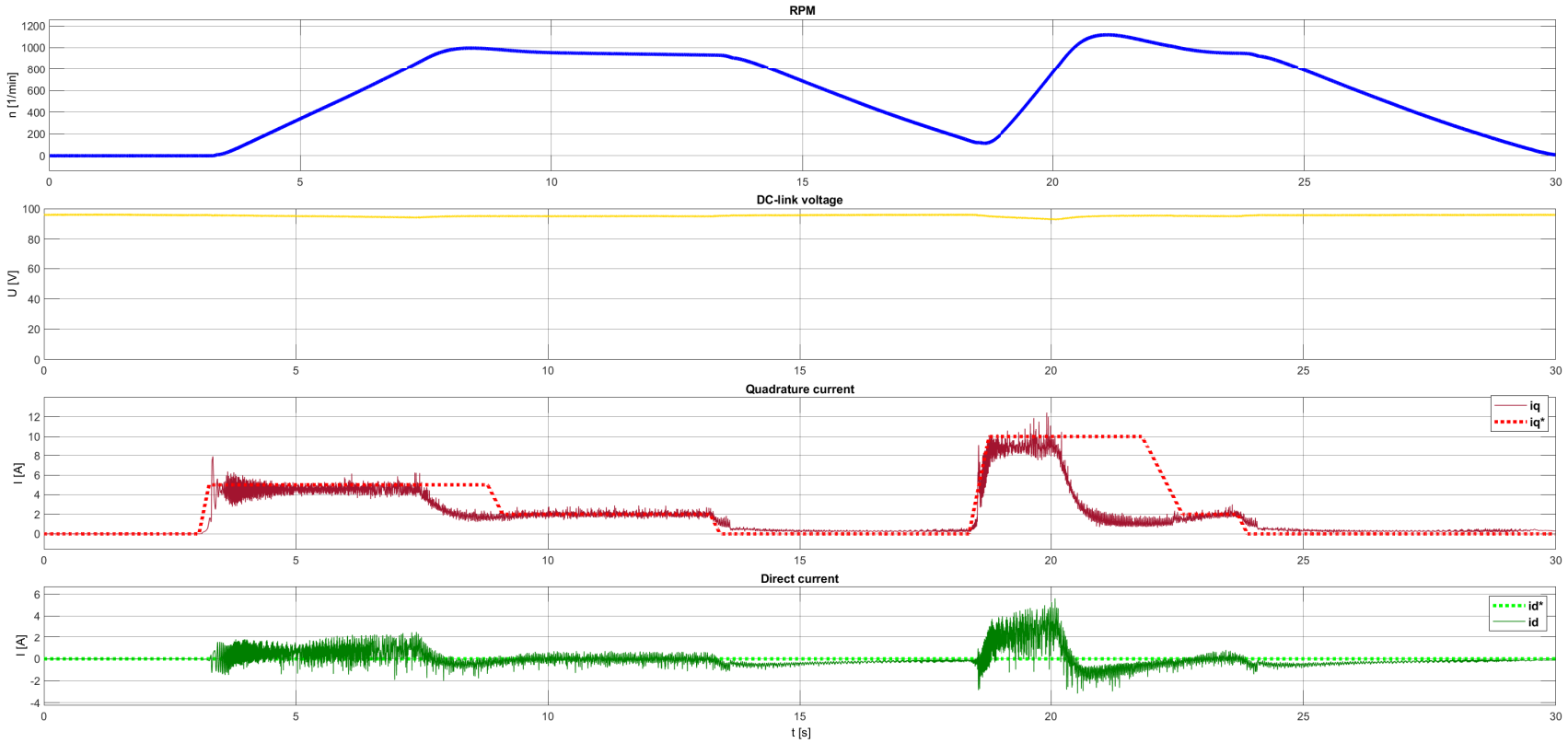


Figure B.5: Measured data of performed closed-loop motor control testing.

Appendix C

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