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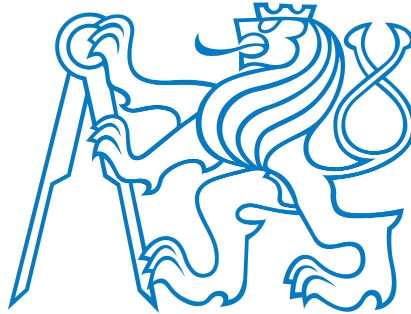
Department of Radioelectronics



Ph.D. Thesis

New Models of High Voltage Semiconductor Devices for Radio Frequencies

by

Ing. Stanislav Banáš

Supervisor: doc. Ing. Josef Dobeš, CSc.

Prague, 2019

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Declaration

I declare that my doctoral dissertation thesis was prepared personally and bibliography used duly cited. This thesis and the results presented were created without any violation of copyright of third parties.

The most of new ideas described in this thesis are at least 80% my own. My ratios of participation in the relevant publications are 30–50% depending on the topic. For details see conclusions in chapters 3–8.

Chapters 3–8 representing the new contribution of this thesis were presented either in impacted journals excerpted in Web of Science or in international conferences, as it is documented in Appendix A. I am the first author of all the mentioned publications [5, 4, 2, 6, 3, 7].

In Prague March 18th, 2019 . . . .

Abstract

This thesis is focused on the modeling of high-voltage components built from low doped layers and therefore containing effects not covered by standard compact SPICE models. The main result of this work is a model of high-voltage dual-gate JFET covering effects like voltage dependent pinch-off, impact ionization, reverse recovery, high frequency effects or bi-modal statistical distribution of simulated parameters.

This Verilog-A model has universal use for many types of components in various high-voltage technologies as stand-alone voltage dependent resistor, pinch resistor, drift area of HV FET or LDMOS, dual gate JFET, etc...

The first phase of this work was the development of basic large signal model containing basic tunable model parameters, e.g. concentration, diffusion depth, saturation current or gate capacitance. The next phase was focused on the modeling in frequency domain. Besides the precise modeling of the voltage dependent capacitance of both JFET gates and using RLC network for the precise modeling of the polysilicon gate resistance in GHz range, the main accent was put on the modeling of gate p-n junction reverse recovery. The developed comprehensive behavioral model is applicable also as a stand-alone diode to all standard SPICE simulators supporting Verilog-A language. The third phase was the development of the statistical model. In this case a tight cooperation with the production was necessary, because the input for the statistical model was a set or real statistical data from the production.

The model was developed using quite large set of measured data. Some of measured characteristics compared with the simulated results are presented in the thesis.

Keywords: FET, HV FET, JFET, SPICE, behavioral model, drift, quazisaturation, convergence, dual-gate JFET, pinch resistor, modeling, parameter extraction, high voltage, reverse recovery, RF, parasitic, RLC network.

Abstrakt

Tato dizertační práce je zaměřena na modelování vysokonapěťových součástek tvořených velmi nízko dotovanými vrstvami. Takovéto součástky se vyznačují vlastnostmi, které ve standardních kompaktních SPICE modelech nejsou obsaženy. Hlavní výsledek této práce je model vysokonapěťového dvouhradlového JFETu obsahujícího jevy jako napěťově závislý pinch-off, nárazová ionizace, zpětné zotavení, vysokofrekvenční jevy nebo bi-modální statistické rozdělení simulovaných parametrů.

Tento Verilog-A model má univerzální využití pro mnoho typů součástek v různých vysokonapěťových technologiích, jako jsou napěťově závislé resistory, pinch resistory, driftová oblast vysokonapěťového FETu nebo LDMOSu, dvouhradlový JFET, atd...

První fáze této práce bylo vytvořit základní velkosignálový model obsahující základní ladící modelové parametry jako jsou koncentrace, hloubka difúze, saturační proud nebo hradlová kapacita. Následující fáze byla zaměřena na modelování ve frekvenční doméně. Kromě přesného modelování napěťově závislé kapacity obou hradel JFETu a využití RLC sítě pro přesné modelování odporu polykřemíkového hradla v GHz oblasti, byl hlavní důraz kladen na modelování zpětného zotavení hradlového p-n přechodu. Výsledný univerzální behaviorální model je použitelný i jako samostatná dioda pro všecky standardní SPICE simulátory podporující jazyk Verilog-A. Třetí fáze byla vývoj statistického modelu. V tomto případě byla nezbytná úzká spolupráce s výrobou, protože vstupem pro statistický model bylo množství reálných statistických dat z produkce.

Pro vývoj modelu bylo zapotřebí velké množství měřených dat. Některé z měřených charakteristik porovnané se simulovanými výsledky jsou prezentovány v této práci.

Klíčová slova: FET, HV FET, JFET, SPICE, behavioral model, drift, quazisaturation, convergence, dual-gate JFET, pinch resistor, modeling, parameter extraction, high voltage, reverse recovery, RF, parasitic, RLC network.

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List of Symbols

α_{0G} — First parameter of impact ionization gate current [μmV^{-1}], see equation (3.19), page 48

α_{1G} — Length scale parameter of impact ionization gate current [V^{-1}], see equation (3.19), page 48

α_{l} — Lateral Pinching Factor [cmV$^{-0.5}$], see equation (3.8), page 34

α_{v} — Vertical Pinching Factor [cmV$^{-0.5}$], see equation (3.7), page 34

β — Transconductance Parameter [IV^{-2}], see equation (3.1), page 33

β_{0G} — Second parameter of impact ionization gate current [V^{-1}], see equation (3.19), page 48

$\delta a_{\Delta w_m}$ — Absolute shift of parameter ΔW - mean [μm], see equation (3.32), page 56

$\delta a_{\Delta w_s}$ — Absolute shift of parameter ΔW - sigma [μm], see equation (3.32), page 56

δr_{ISG_m} — Absolute shift of parameter I_{SG} - mean [%], see equation (3.33), page 56

δr_{ISG_s} — Absolute shift of parameter I_{SG} - sigma [-], see equation (3.33), page 56

δr_{Nbody_m} — Relative shift of parameter N_{body} - mean [%], see equation (3.30), page 54

δr_{Nbody_s} — Relative shift of parameter N_{body} - sigma [%], see equation (3.30), page 54

δr_{rho_m} — Relative shift of parameter r_{ho} - mean [%], see equation (3.31), page 54

δr_{rho_s} — Relative shift of parameter r_{ho} - sigma [%], see equation (3.31), page 54

$\Delta_{\rm L}$ Difference between effective and drawn length [m], see equation (3.2), page 33

$\Delta_{\rm W}$ Difference between effective and drawn width [m], see equation (3.2), page 33

ϵ_0 Vacuum Permitivity [$\rm Fm^{-1}$], see equation (3.7), page 34

$\epsilon_{\rm diel}$ Permitivity of dielectricum [-], see equation (2.8), page 25

$\epsilon_{\rm Si}$ Permitivity of silicon [-], see equation (2.8), page 25

ϵ_r Relative Permitivity of Silicon [-], see equation (3.7), page 34

λ Velocity Overshoot Coefficient [$\rm V^{-1}$], see equation (3.1), page 33

$\rm MULT_{mm}$ JFET model mismatch multiplication factor [-], see equation (3.34), page 57

$\rm rsub_{tc}$ Temperature coefficient of pinch-off voltage [$\rm K^{-1}$], see equation (3.27), page 51

$\rm xti_G$ Temperature exponent of gate OFF state current [-], see equation (3.29), page 51

μ Mean value [unit], page 54

ω Angular frequency [rad/sec], see equation (5.1), page 77

$\psi_{\rm l}$ Lateral built-in potential [V], see equation (3.6), page 34

$\psi_{\rm v}$ Vertical built-in potential [V], see equation (3.5), page 34

σ Standard deviation [unit], page 54

σ_{mm} JFET model mismatch standard deviation [m], see equation (3.34), page 57

τ Minority carrier lifetime [sec], see equation (6.14), page 86

$A_{\rm act}$ Active area [$\rm m^2$], page 16

$A_{\rm G}$ Gate area [$\rm \mu m^2$], page 46

C Capacitance [F], see equation (3.15), page 44

$C_{\rm inj}$ Injection capacitance [F], see equation (6.5), page 84

$C_{\rm j0}$ Zero-bias junction capacitance per unit area [F], see equation (3.15), page 44

C_{j}	Drift capacitance [F], see equation (6.6), page 84
C_{mult}	Multiplication factor for the JFET capacitance model equation [-], page 44
C_{SG}	Source-gate capacitance [F], see equation (3.18), page 46
C_{DG}	Drain-gate capacitance [F], see equation (3.17), page 46
C_{GD}	Gate-drain capacitance [F], page 1
C_{GS}	Gate-source capacitance [F], page 62
C_{SUBD}	Substrate drain capacitance [F], page 66
C_{SUBS}	Substrate source capacitance [F], page 66
d_{depl}	Depletion layer length [m], see equation (2.8), page 25
d_{epi}	Epitax layer depth [m], page 16
E_G	Band gap energy width [eV], see equation (4.3), page 63
E_{lat}	High electric field [Vm^{-1}], see equation (2.1), page 17
F_{n}	Normalization factor [V^{-1}], see equation (3.14), page 41
g_{1G}	First order voltage coefficient of gate current [V^2], see equation (3.22), page 49
g_{2G}	Second order voltage coefficient of gate current [V], see equation (3.22), page 49
G_{shapeG}	Gate current dependency on gate voltage [V^2], see equation (3.19), page 48
I_{D}	Drain current [A], page 21
I_{Gii}	Gate impact ionization current [A], see equation (3.19), page 48
I_{inj}	Injection current [A], see equation (6.11), page 85
I_{j}	Junction current [A], see equation (6.11), page 85
I_{leak}	Leakage current [A], see equation (3.23), page 49
I_{SG}	Gate saturation (OFF state) current [A], see equation (3.24), page 49
I_{SUB}	Substrate current [A], page 116

I_K	High-injection knee current [A], see equation (6.22), page 89
I_S	Saturation current [A], see equation (6.2), page 84
I_{pn}	Large signal diode current [A], see equation (6.1), page 84
I_{S}	Source current [A], page 41
j	Imaginary unit [-], see equation (5.1), page 77
k_{b}	Boltzmann constant [JK^{-1}], see equation (3.5), page 34
L	Length [m], see equation (3.2), page 33
L_{drift}	Drift length [m], page 16
L_{eff}	Effective JFET length [m], see equation (3.19), page 48
L_0	Distance between active structure and device edge [m], see equation (2.3), page 17
M_{j}	Grading coefficient [-], see equation (3.15), page 44
n_{i}	Intrinsic carrier concentration of silicon [cm^{-3}], see equation (3.5), page 34
n_e	Emission coefficient [-], see equation (3.23), page 49
N_{body}	JFET body (drift area) concentration [cm^{-3}], see equation (3.7), page 34
N_{epi}	Epitax layer concentration [cm^{-3}], page 16
N_{side}	Side concentration of JFET body [cm^{-3}], see equation (3.7), page 34
N_{tub}	JFET gate (substrate) concentration [cm^{-3}], see equation (3.7), page 34
q	Unit charge [C], see equation (3.5), page 34
Q_{e}	Charge of carriers injected to the p-n junction [C], see equation (6.12), page 86
Q_{inj}	Charge of injected carriers [C], see equation (6.1), page 84
Q_{j}	Fixed charge of ionized dopant atoms [C], see equation (6.1), page 84

Q_{m}	Charge of carriers injected away from the p-n junction [C], see equation (6.12), page 86
r_{sub}	Parameter for fine tuning of pinch-off voltage [-], page 35
r_{ho}	Linear resistance contribution [Ω], see equation (3.9), page 35
r_{sub0}	Independent tuning parameter for pinch-off voltage [-], see equation (3.13), page 39
r_{sub1}	1st order width dependency coefficient of r_{sub} [m^{-1}], see equation (3.13), page 39
r_{sub2}	2nd order width dependency coefficient of r_{sub} [m^{-2}], see equation (3.13), page 39
r_{sub3}	3rd order width dependency coefficient of r_{sub} [m^{-3}], see equation (3.13), page 39
r_{subb}	r_{sub} dependency on V_{SG2} [V^{-1}], see equation (3.14), page 41
r_{subd}	r_{sub} dependency on V_{DS} [-], see equation (3.14), page 41
R_S	Series resistance [Ω], see equation (6.22), page 89
R_{dson}	Series resistance in ON State [Ω], page 1
R_{SH}	Sheet Resistance [Ω/sq], see equation (2.2), page 16
S	Steepness of the JFET gate capacitance drop [V^2], see equation (4.4), page 70
T	Absolute Temperature [K], see equation (3.26), page 51
T_{M}	Diffusion transit time [sec], see equation (6.12), page 86
T_{nom}	Nominal Temperature [K] - 300K, see equation (3.26), page 51
T_T	Transit time [sec], see equation (6.4), page 84
T_{RS}	Temperature coefficient of series resistance R_S [K^{-1}], see equation (6.24), page 89
V	Voltage [V], see equation (3.15), page 44
V_{DSeff}	Effective Drain-Source Voltage [V], see equation (3.10), page 35
V_{SDeff}	Effective Source-Drain Voltage [V], see equation (3.11), page 36
V_{BR}	Drain-source Breakdown Voltage [V], page 14

V_{DD} Supply Voltage of Integrated Circuit [V], page 1

V_{DG2eff} Effective Drain-Gate2 Voltage [V], page 41

V_{DG} Drain-Gate Voltage [V], see equation (3.9), page 35

V_{DS} Drain-Source Voltage [V], page 3

V_{D} Drain Voltage [V], page 10

V_{G1S} Gate1 source voltage [V], page 52

V_{G1} Gate1 Voltage [V], page 39

V_{G2S} Gate2 source voltage [V], page 50

V_{G2} Gate2 Voltage [V], page 43

V_{GD} Gate-Drain voltage [V], page 47

V_{GS} Gate-Source Voltage [V], page 19

V_{j} Junction built-in potential [V], see equation (3.15), page 44

V_{poff} Critical pinch-off voltage for modeling of JFET capacitance [V], page 44

V_{SD} Source-Drain Voltage [V], page 39

V_{SG2eff} Effective Source-Gate2 Voltage [V], page 41

V_{SG2} Source-Gate2 Voltage [V], see equation (3.14), page 41

V_{SG} Source-Gate Voltage [V], see equation (3.9), page 35

V_{S} Source voltage [V], page 46

V_{t} Thermal voltage [V], see equation (3.23), page 49

V_{diff} Difference between drain-source voltage and effective drain-source voltage [V], see equation (3.19), page 48

V_{thinf} Threshold voltage for infinite wide resistor [V], see equation (3.4), page 33

V_{th} Threshold Voltage [V], see equation (3.1), page 33

V_{G} Gate voltage [V], page 63

V_{SUB} Substrate voltage [V], page 63

var	Master variable controlling JFET model statistical distribution [-], see equation (3.30), page 54
$\mathrm{var}_{\mathrm{mm}}$	JFET model mismatch master variable [-], see equation (3.34), page 57
W	Width [m], see equation (3.2), page 33
x_{j}	Resistor depth [m], see equation (3.4), page 33
x_{dn}	N layer depth [m], see equation (2.5), page 18
x_{dp}	P layer depth [m], see equation (2.5), page 18
X_{ti}	Intrinsic carrier concentration temperature exponent [-], see equation (4.3), page 63
CMOD	Capacitance model selector [-], see equation (3.16), page 44
GMIN	Minimal conductance of the model [S] , page 95
GMOD	Geometry Model Selector [-], page 35
IGMOD	Gate current model selector [-], see equation (3.25), page 50
texp	Temperature exponent of JFET resistance [-], see equation (3.26), page 51
xjtexp	Temperature exponent of JFET depth [-], see equation (3.28), page 51

List of Abbreviations

AC-DC	Alternating Current - Direct Current, page 1
ACMOS	Analog CMOS technology, page 10
BCD	Bipolar CMOS DMOS - Semiconductor technology integrating Bipolar, CMOS and DMOS technologies, page 10
BiCMOS	Semiconductor technology integrating Bipolar and CMOS technologies, page 91
BPV	Backward Propagation of Variances, page 4
CLAVER	Combined Lateral Vertical RESURF, page 24
CMOS	Complementary Metal-Oxide-Semiconductor, page 25
DAM	Data Management - ON Semiconductor internal measurement and data management system, page 10
Dieler	Dielectric Resurf, page 26
DMOS	Double Diffused MOS, page 41
DUT	Device Under Test, page 77
ESD	Electrostatic discharge, page 4
FET	Field-Effect Transistor, page 1
HDL	Hardware Description Language, page 5
HEMT	High-Electron Mobility Transistor, page 44
HV	High Voltage, page 1
HV FET	High Voltage Field Effect Transistor, page 18
IC-CAP	Integrated Circuit Characterization and Analysis Program, page 10
IGBT	Insulated Gate Bipolar Transistor, page 102

JFET	Junction Field-Effect Transistor, page 1
LCL	Lower Control Limit, page 55
LDMOS	Laterally Diffused MOS transistor, page 1
LED	Light-Emitting Diode, page 1
LSL	Lower Specification Limit, page 55
MESFET	Metal-Semiconductor Field-Effect Transistor, page 44
Monte Carlo	Algorithm for statistical simulation, page 54
N+	High N Doped Silicon, page 14
N-	Low N Doped Silicon, page 14
NBL	N Burried Layer, page 19
N_{drift}	N doped drift area, page 23
P+	High P Doped Silicon, page 14
P-	Low P Doped Silicon, page 14
PB	P Body, page 20
PCC	Process Characterization Chip, page 9
PCM	Process Control Monitoring, page 9
RESURF	Reduced Surface Field, page 1
RF	Radio Frequency, page 3
RLC	Resistor Inductor Capacitor, page 3
SOA	Safe Operation Area, page 18
SPICE	Simulation Program with Integrated Circuit Emphasis, page 1
STI	Shallow Trench Isolation, page 25
TLP	Transmission-Line Pulse, page 19
UCL	Upper Control Limit, page 55
USL	Upper Specification Limit, page 55
VHVNW	Very High Voltage Nwell layer, page 68

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CHAPTER 1

Introduction

The new technologies of integrated AC-DC converters, used for example in LED drivers, require high voltage components supplied from high voltage source in order of hundreds volts to transfer high voltage to the supply acceptable by the rest of the integrated circuit. Such devices are designed to withstand required high voltage and concurrently eliminate series resistance R_{dson} and output capacitance C_{GD} to the minimum. This is achieved by two main factors. First one is the lateral layout of the device. High voltage devices have typically circle or oval shape with the high voltage bonding pad in the center surrounded by the low doped layer. The electric field is dropping in this low doped layer with the distance from the center. Increasing this distance typically increases breakdown voltage but also series resistance. This low doped area is often called the drift area. The second factor is vertical concentration profile of the drift area. There exist several techniques, as for example RESURF [1], double RESURF [56], triple RESURF [54], super-junction [27], poly plates or metal plates to optimize breakdown voltage, series resistance and output capacitance. Due to specific construction, these HV components have also specific electrical characteristics. There are observed effects, as for example pinching or quasi-saturation, not covered by most silicon devices and hence not considered in standard compact models.

The following thesis is focused on the modeling of high voltage devices, operating in the area of tens to hundreds of volts. The first theoretical part describes the making of high voltage devices and the related challenges. The second part is focused on the modeling of described phenomena.

The result of the thesis is universal behavioral model applicable in SPICE simulators for the simulation of high voltage components containing pinch effect and related phenomena, e.g., HV LDMOS, start-up FET, dual gate JFET or pinch resistor. Unlike standard compact models focused typically on the submicron technologies operating in voltages $V_{\mathrm{DD}} << 100\ \mathrm{V}$, the

presented model is more accurate in HV applications and contains all phenomena typical for devices operating at hundred volts, including parasitic effects. This thesis presents the main idea of the behavioral model demonstrated on the example of high voltage dual gate JFET and high voltage pinch resistor, including the comparison of measured data vs simulation.

The model is precise in full operation area, converges very well, its simulation speed is comparable with conventional compact models and contains all phenomena observed in high voltage devices. Moreover, it has universal use for many types of devices such as stand-alone voltage dependent resistor, pinch resistor, drift area of power FETs, part of special high side driver components, start-up devices, dual gate JFET, etc.

1.1 Current Status of the Studied Topic (State of the Art)

Modeling work on JFETs has been mainly focused on three-terminal JFETs [59] [35]. This thesis introduces a comprehensive model enabling using two independent gates, one top-side, one bottom-side, and their mutual interaction. Most existing publications about (dual-gate) JFET model are focused on DC parameters [61, 57, 58]. Recently published dual-gate JFET [61] provides a more physical and less empirical solution and their DC model can be more accurate in many cases. However, in dual-gate JFET the top-side gate not necessarily covers the whole JFET channel, as demonstrated in Fig. 3.9. The ratio of covered and uncovered channel controls the dependency of pinch-off on V_{DS}. In this thesis this dependency is modeled by an empirical equation. Another merit of the presented model is the addition of impact ionization to the leakage current of both gates. In the presented model the capacitance parameters were implemented by using the structural model defined by instantiation of Verilog-A [16, 49] component with the implementation of additional voltage dependency. For the next model version it is planned to switch to the charge controlled model as recommended in [40].

The presented Verilog-A model is relatively complex, containing DC parameters, capacitance parameters, parasitic parameters for leakage current and impact ionization, temperature parameters and statistical parameters. It does not yet cover the self-heating and noise parameters [35].

In last two years, some very interesting publications of physically based dual-gate JFET from respected modeling experts [64, 63] appeared, quoting the key part of this thesis published in Solid-State Electronic journal [5]. The mentioned articles valuated especially the modeling of impact ionization which was missing in other articles.

One of the main requirements for the developed model was the precise simulation of RF applications, so one of key parts of this thesis was dedicated to the modeling of voltage dependent gate capacitance affected by the pinching effect. Although this effect was already published [12], the contribution and uniqueness of this thesis is the description of the modeling this effect with respect to the special dual-gate JFET layout containing two p-n junction gates affecting each other. The two variants of the dual-gate JFET layout with different capacitance models are presented.

The next part of this thesis is also focused on RF application, but from different point of view. In this case the published JFET model is a part of macromodel representing very large power MOSFET. Although one of the most advanced MOSFET models BSIM4 [62] was used for the modeling of intrinsic MOSFET channel, the development of advanced RLC network was

necessary to to simulate correctly singal in the range of GHz.

Another important part of the developed model is reverse recovery of p-n junction, where both the reverse current and the reverse voltage can be simultaneously large, which significantly affects the resulting power consumption. Unfortunately, standard compact SPICE models often neglect this effect, which can be crucial for some applications. The reverse recovery model can be used not only as a part of published JFET model, but in any model containing p-n junction. Most of components including MOSFET contain one or more p-n junctions, which need to be modeled precisely. The new technologies and new applications with the accent on the high speed and low power consumption require SPICE device models to be accurate in full operating range, including high speed in combination with high voltage.

Fundamental reverse recovery modeling researches used in this thesis have been published in [25, 29, 28]. Some of the recently published papers are focused on ultrafast diodes of various types, e.g., Si fast recovery diode, SiC Schottky barrier diode [23], or PIN diodes [14, 9]. There also exist several studies focused on measurement methods of the reverse recovery time [50, 47].

Recently the new compact diode models containing reverse recovery as for example hisim diode or diode cmc appeared in some SPICE simulators. These models appeared just before the publishing of our behavioral model in Solid-State Electronics journal and quote the same references, so a special chapter comparing these models and describing merit of our behavioral model was added to the article. This chapter is part of the thesis.

The published model contains equations and parameters enabling simulation of process distribution as well as mismatch distribution. It is based on the Backward Propagation of Variances (BPV) method [36, 38]. However, during the research it was necessary to improve the statistical model to be able to simulate bi-modal statistical distribution appearing in real production data, because any publication solving this challenge was not found.

All mentioned parts of the model are contained in this thesis and organized in well-arranged sections. The final section then contains the future challenges for the potential model improvement, that have not been published yet.

1.2 Organization of the Thesis

The thesis is organized as follows:

- **Chapter 1** gives a brief overview of the current situation of the studied topic and aims of the thesis.
- **Chapter 2** presents theoretical background relating to the JFET modeling, focused mainly on the principles of Reduced Surface (RESURF).
- **Chapter 3** deals with the basic concept of the introduced Verilog-A behavioral dual-gate JFET model. This chapter practically represents the core of the presented model. It contains all the model sections, which are DC model, capacitance model, parasitic DC model containing impact ionization as well as the leakage current, temperature model, statistical model. All the following chapters are then the extension of improvement of this core model. Final subsection contains the table of extracted model parameters for two chosen device examples: dual gate JFET and pinch resistor, where each one contains different challenges.
- **Chapter 4** extends the capacitance model presented in Chapter 3 and deals with the techniques of the measurement and modeling of the voltage dependent JFET gate capacitance affected by the JFET pinch-off voltage.
- **Chapter 5** presents the solution of the polysilicon gate resistance modeling applicable for high frequencies in order of GHz and higher. Although JFET model presented in Chapter 3 does not contain polysilicon gate, the model can be used (and in our case was used) as a part of high-voltage discrete MOSFET macromodel.
- **Chapter 6** describes the behavioral model of diode containing reverse recovery, which was used for the modeling of JFET gate characteristics. The model was used as a part of the core JFET model presented in Chapter3, but it can be used also as a stand-alone model for the modeling of diode or as a part of another complex macromodel. Chapter 6 as well as Chapter 3 were published in Solid-State-Electronics journal.
- **Chapter 7** extends the statistical model presented in Chapter 3 with the implementation of the method for the modeling of bi-modal statistical distribution.

- **Chapter 8** presents challenges for the potential future model improvement. The presented effects are not included in any of published dual-gate JFET model yet.

- **Chapter 9** contains conclusion and final remarks.

1.3 Aims of the Thesis

The aim of this thesis is development of the **comprehensive behavioral Verilog-A model of the dual-gate JFET** with following features:

- **Implementation of independent second gate.** Complex Dual-gate JFET model is not yet implemented in SPICE simulators (Eldo, Spectre, Hspice). Papers published before this work [61, 57, 58] are focused on DC parameters only and do not take into account many important effects published in this thesis.

- **Improved bias and geometry scalability of pinch-off voltage with consideration of 3-D effects.** There exist many layout variants affecting the pinch-off voltage and it's scalability.

- **Implementation of parasitic impact ionization current for both independent gates.** Even existing single-gate SPICE JFET model does not contain the impact ionization yet. Papers published before this work [61, 57, 58, 37] don not consider this effect.

- **Implementation of pinching factor in the gate capacitance for both independent gates.** Papers published before this work [61, 57, 58, 37] are focused on DC parameters only and do not mention this effect.

- **Implementation of reverse recovery effect for both independent gates.** The most of reverse recovery models published before this work are not usable for production design, mainly due to the insufficient convergence. This might be the reason why this important effect has not been implemented in SPICE models for so long time.

- **Improved temperature model by adding more temperature parameters.** Very important part of complex dual-gate JFET model development.

- **Implementation of statistical parameters for the simulation of process distribution.** Very important part of complex dual-gate JFET model development.

- **Applicability of the model or its segments for various types of components.** The model is intended to be used in various components as stand-alone pinch resistors, dual-gate/single-gate JFET, drift area of HV LDMOS, diode with reverse recovery, etc...

- **Implementation of the model to RF application and its verification in GHz+ frequencies.** One of intended model use is the

drift area of discrete high voltage MOSFET constructed for high frequency use.

The fundamental results (new scientific findings) of this thesis are described in Chapters 3-7. Each of these chapters was published either in an impacted journal excerpted in Web of Science or presented in an international conference. The references to these papers can be found in Appendix B.

1.4 Used Model Parameter Extraction Methodology

The following list of steps describes used model development flow:

- **Design of Process Characterization Chip (PCC)** – At first characterization test chip was designed in software Cadence Virtuoso Layout. Each of the characterized devices was placed there in different dimensions and configurations to enable to measure and precisely implement the device scalability to the model parameters. There were also created structures allowing various types of measurement (e.g. DC, AC, mismatch, etc.). PCC chip typically contains all the structures necessary for characterization of the process and making predictive SPICE models. Therefore it is typically very large chip covering full reticle.

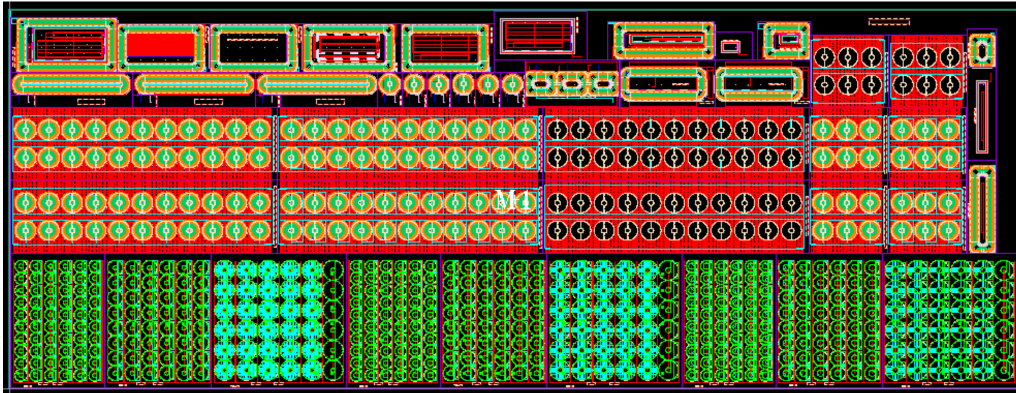

Figure 1.1: PCC - Process Characterization Chip.

- **Design of Process Control Monitoring (PCM) test chip** – PCM test chip was designed in software Cadence Virtuoso Layout and added into all following production masks (each fabricated standard production wafer then contains PCM test chip with required devices for statistical modeling). PCM has defined testplan measured in each wafer before testing production device. Measurement must pass the defined criteria. PCM is used for monitoring distribution of main process parameters and generation of statistical models.

Figure 1.2: PCM - Process Control Monitoring Chip.

- **PCC and PCM test chip manufacturing** – Test chips were manufactured for both technologies: 700V 1 μm ACMOS technology and 700V 0.25 μm BCD technology. The wafers best matching process means were selected for measurement.

- **PCC measurement methods definition followed by measurement** – The measurement methods were defined, tested and used for various device dimensions and configurations.

  - Various DC measurements at various temperatures −40, −20, 0, 27, 60, 90, 125, and 150°C ($I_\mathrm{D}V_\mathrm{D}$, $I_\mathrm{D}V_{\mathrm{G_n}}$, $V_\mathrm{S}I_\mathrm{S}$-load line, etc...)
  - Various CV measurement at various temperatures −40, −20, 0, 27, 60, 90, 125, and 150°C ($C_{\mathrm{G_1}}V_\mathrm{GD}$, $C_{\mathrm{G_1}}V_\mathrm{GS}$, $C_{\mathrm{G_2}}V_\mathrm{GD}$, $C_{\mathrm{G_2}}V_\mathrm{GS}$)
  - Various parasitic DC measurements at various temperatures −40, −20, 0, 27, 60, 90, 125, and 150°C ($I_{\mathrm{G_1}}V_\mathrm{D}$, $I_{\mathrm{G_2}}V_\mathrm{D}$, $I_{\mathrm{G_1}}V_{\mathrm{G_2}}$, $I_{\mathrm{G_n}}I_\mathrm{D}$, $I_{\mathrm{G_1}}I_\mathrm{S}$, $I_{\mathrm{G_2}}I_\mathrm{S}$, etc...)

- **PCM measurement methods definition followed by production measurement** – The measurement methods were defined, tested and used for selected device dimensions and configurations (e.g. 2 widths for pinch resistor, one dimension for dual-gate JFET). In PCM only a few basic single point tests at nominal temperature are measured. Statistical PCM results are used for the statistical model evaluation.

- **Export/import data from PCC testchip measurement** – PCC Measured data were exported from measurement Data Management (DAM) database (ON Semiconductor internal measurement and data management system, thesis author is employee) in .mdm file format and then imported into IC-CAP (Integrated Circuit Characterization and Analysis Program).

- **Measurement PCC data quality verification** – The quality of measured data was verified (e.g. comparing same bias points from different measurement methods, verifying measured data trends, physical data scaling, etc...)

- **Parameter extraction** – Parameters of all demonstrated models were extracted in IC-CAP using measured PCC data and various optimization methods [13]. For the statistical model the real production statistical PCM data were used as an input. For the implementation of measured statistical parameters to the model the Backward Propagation of Variances method [36] was used.

- **Model implementation** – The models were implemented into the commercial simulators HSpice (Synopsys), Eldo (Mentor) and Spectre (Cadence).
- **Simulated and measured data comparison** – All measured data were compared with simulated data and all discrepancies were eliminated by model or equation corrections.
- **Final model testing** – The developed models were verified in their defined operation areas at temperatures from -50 to 200 °C. The verification was provided with models applied to several device types. The important requirement was that the new developed models had smooth derivatives of simulated characteristics.

CHAPTER 2

Theoretical Background

2.1 Introduction

The key parameter of high voltage devices is naturally maximal output voltage, which is typically limited by the avalanche breakdown voltage. However, still growing demands for low power consumption and high speed requires also low ON state resistance as well as low capacitance. Unfortunately increasing breakdown voltage in traditional structure makes the ON state resistance higher and vice versa. The reason is that the simplest way of breakdown voltage increase is increase of the device output resistance. Higher resistance naturally withstands larger electrical field. So the easiest techniques to make a device suitable for higher voltage are:

a) Increase the device length, especially the layer, where the high voltage is applied (drift layer)

b) Decrease concentration of the layer, where the high voltage is applied (drift layer)

Both methods cause unwanted increase of resistance. Fortunately there exist several techniques how to increase breakdown voltage without significant increase of output resistance. One of the most common and most effective methods is technique called RESURF (Reduced Surface Field).

RESURF demonstrated in Fig. 2.1a is one of the most widely-used methods for the design of lateral high-voltage, low on-resistance devices. It enables realization of high breakdown voltage and low ON state resistance. The power device using RESURF has high breakdown voltage at reverse characteristics and simultaneously low resistance in ON state, which is important for switching operation.

The more effective is double RESURF demonstrated in Fig. 2.1b. The additional layer of opposite conductivity (p-top layer) is incorporated inside n drift region so that the total charge in the n drift region can be doubled

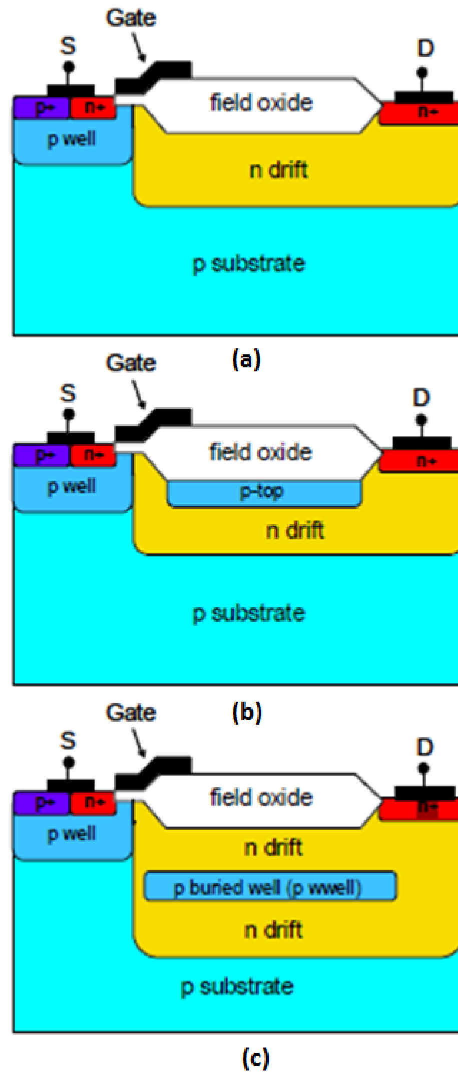

Figure 2.1: Cross-sections of LDMOS (a) Single RESURF structure, (b) Double RESURF structure, (c) Triple RESURF structure. Reprinted from "State-of-the-art Device in High Voltage Power ICs with Lowest ON State Resistance", by Su, R. et al., 2010, Electron Devices Meeting (IEDM), 2010 IEEE International, p.20.8.1. © 2010 by the IEEE. Reprinted with permission, see App. B.

compared to the single RESURF LDMOS to minimize the ON state resistance. However, the maximum doping is limited by the requirement that the drift region should be fully depleted before device avalanche breakdown. Another attractive structure with floating p buried well (pwell) inserted into n drift region to provide dual conduction path is triple RESURF demonstrated in Fig. 2.1c, which makes two conduction paths and the depleting

RESURF effect is doubled.

Following sub-chapters describe these principles and their variants more in details.

2.2 Single RESURF

The success of high voltage devices depends on the combination of high drain-source breakdown voltage V_{BR} and low on resistance R_{on}. The principle of RESURF was disclosed by J. A. Appels and H. M. J. Vaes from Philip Research Laboratories in 1979 [1].

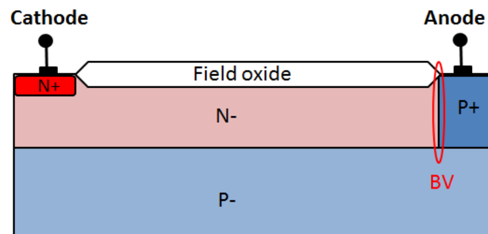

Figure 2.2: Cross-section of PN diode with deep N-.

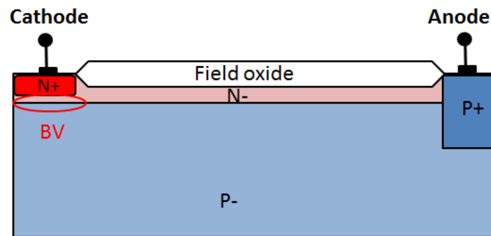

Figure 2.3: Cross-section of PN diode with shallow N-.

Here is the main idea: Let's have a P-N- diode, where N- is contacted by N+ diffusion and P- is contacted by P+ diffusion, as it is demonstrated in in Fig. 2.2. N+ is in the center of the device, so N- is laterally bounded by P+. The junction of N-P+ marked by red oval (Fig. 2.2a) is the critical point as concerns breakdown voltage due to high concentration of P+. The vertical P-N- junction has lower breakdown. There are two possibilities how to increase breakdown voltage, both of them are spreading the electric field away from the critical point:

1. Enlarge distance between N+ and P+ and hence increase the voltage drop on N- layer (Fig. 2.2)

2. Narrow N- layer, which causes that the depletion stretches along the surface over much longer distance.

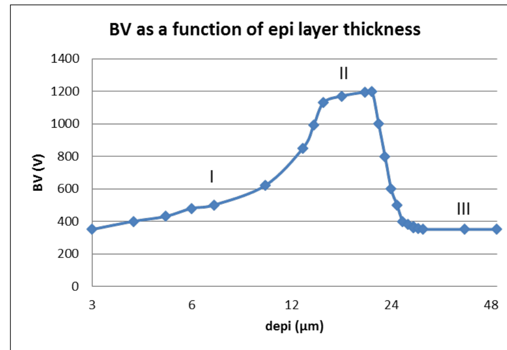

Figure 2.4: Breakdown voltage as a function of epitaxial layer thickness. Reprinted from "High voltage thin layer deivces (RESURF devices)", by Appels, J. and Vaes, H., 1979, Electron Devices Meeting (IEDM), 1979 IEEE International, vol. 25 p.239 © 1979 by the IEEE. Reprinted with permission, see App. B.

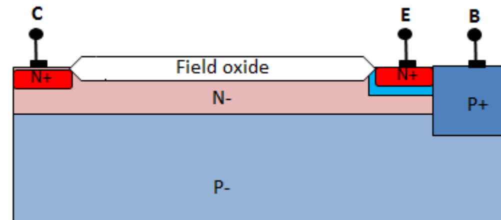

Figure 2.5: Cross-section of lateral bipolar transistor.

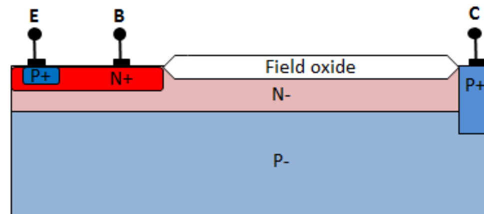

Figure 2.6: Cross-section of vertical bipolar transistor.

The first method does not require intervention to the technology, however enlarges device area and therefore also increases ON state resistance R_{on}. Therefore during the technology optimization cycle the second method is rather used. However, there are also limitations. Since the N- layer is fully depleted a new effect arises. Due to the curvature of the N+ contact the electric field will strongly increase. For very thin N- layers the effects is so strong, that the electric field at the edge of the N+ region is larger than

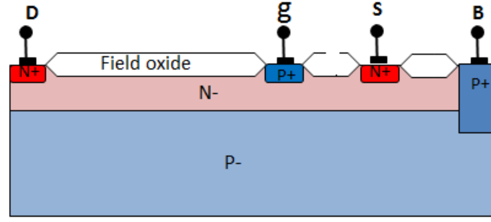

Figure 2.7: Cross-section of JFET.

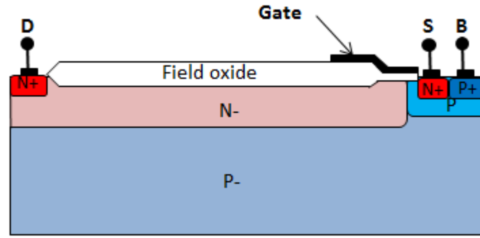

Figure 2.8: Cross-section of LDMOS.

the field in the bulk. The critical point moves to the N+ area and the breakdown drops down as demonstrated by red oval in in Fig. 2.3. Apparently there exists optimal width of N- layer for given doping concentration. In [1] it has been demonstrated, that there really exists an ideal combination of epitax (or well) doping concentration N_{epi} and epitax (or well) thickness d_{epi}, which is $N_{\mathrm{epi}}d_{\mathrm{epi}} = 10^{12}$ at/cm^2 as it is shown in Fig. 2.4.

In region II breakdown takes place at the horizontal junction. In region I and II breakdown takes place at the N+ or P+ regions, respectively. However, even optimal device must be optimized with respect to design rules. When the lateral distance (L_{drift}) between N+ contact and P+ isolation is decreased, device still exhibits lower V_{BR}. So the searching of optimal trade-off between normalized on resistance $R_{\mathrm{on}}A_{\mathrm{act}}$ and breakdown voltage V_{BR} is still one of main challenges of high voltage device development.

High Electric Field

$$E_{\mathrm{lat}} = \frac{V_{\mathrm{BR}}}{L_{\mathrm{drift}}} \tag{2.1}$$

is an important parameter for lateral power devices. Using this equation, the relation between drain-source breakdown voltage V_{BR} and effective resistance $R_{\mathrm{on}}A_{\mathrm{act}}$ can be derived [27]:

$$R_{\mathrm{on}} = R_{\mathrm{sh}}\frac{L_{\mathrm{drift}}}{W} \tag{2.2}$$

$$R_{\mathrm{on}}A_{\mathrm{act}} = R_{\mathrm{sh}}L_{\mathrm{drift}}\left(L_{\mathrm{drift}} + L_0\right) \tag{2.3}$$

$$R_{\mathrm{on}}A_{\mathrm{act}} \sim R_{\mathrm{sh}}\left(\frac{V_{\mathrm{BR}}}{E_{\mathrm{lat}}}\right)^2 \tag{2.4}$$

where W is device width, L_0 is the distance between active structure and device edge and R_{sh} is sheet resistance of drift area.

The implementation of the RESURF to various HV devices is demonstrated in Figs. 2.5, 2.6, 2.7 and 2.8.

Following sections will describe another improvement of RESURF technique.

2.3 Double RESURF

This section will demonstrate, how to shift above mentioned ideal combination $N_{\mathrm{epi}}d_{\mathrm{epi}} = 10^{12}\mathrm{at/cm}^2$ to much higher values of the current, whereas breakdown still occurs in the bulk. This is achieved by the improved doping profile as it is described in 2.9 and 2.10 in JFET example.

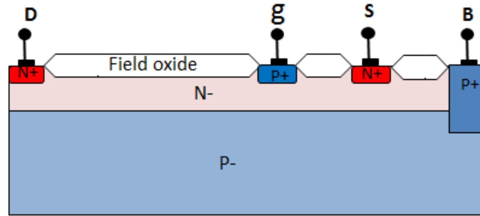

Figure 2.9: Cross-section of JFET with RESURF.

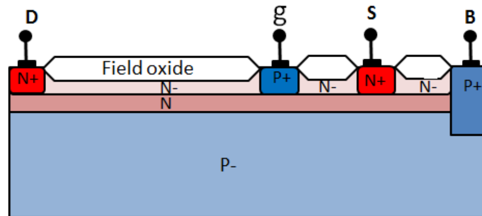

Figure 2.10: Cross-section of JFET with improved N- doping profile.

Now the doping concentration in the channel has been increased, however the total dope integral $N_{\mathrm{epi1}}d_{\mathrm{epi1}} + N_{\mathrm{epi2}}d_{\mathrm{epi2}}$ still fulfills the RESURF condition $\int N\mathrm{d}x = 10^{12}$ at/cm^2.

Thus the drain saturation current has increased, whereas breakdown still occurs in the bulk at the P-N junction. An even better current carrying capability can be obtained by implementing of P- surface concentration instead of N- as it is demonstrated in 2.11. This solution is called double RESURF.

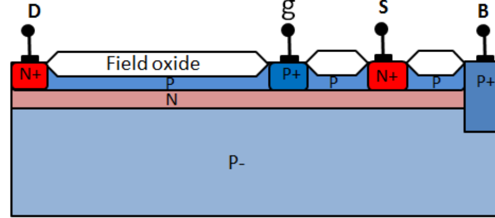

Figure 2.11: Cross-section of JFET with improved N- doping profile - double RESURF.

The n-layer is now depleted from two sides, so the total dope integral is expected to be

$$\int N\mathrm{d}x = N_{\mathrm{n}}x_{\mathrm{dn}} - N_{\mathrm{p}}x_{\mathrm{dp}} = 10^{12}\mathrm{at/cm}^2 \tag{2.5}$$

where x_{dn} is N layer depth and x_{dp} surface P layer depth.

However this is only the first-order approximation. The two dimensional numerical calculation got the ideal values for the bulk breakdown [56]

$$N_{\mathrm{p}}x_{\mathrm{dp}} = 0.5 \times 10^{12}\mathrm{at/cm}^2 \tag{2.6}$$

and

$$N_{\mathrm{n}}x_{\mathrm{dn}} = 1.8 \times 10^{12}\mathrm{at/cm}^2 \tag{2.7}$$

To compare the current carrying capabilities of the different types of RESURF JFET's, $I_{d_{ss}}$ is given as a function of the pinch-off voltage 2.12. It is apparent, that the double RESURF structure has the best performance [56]. The same double RESURF principle could be demonstrated in other structures, like bipolar transistors, LDMOS, etc. (Figs. 2.5-2.8).

However, double RESURF concept can be used not only for V_{BR} vs R_{on} optimization by depleting drift area, as it is shown in Fig. 2.10, but also for SOA improvement by depleting deeper layers, as for example body of LDMOS, as depicted in Fig. 2.13 [45]

The concept demonstrated in Fig. 2.13 was successfully used for the reduction of quazisaturation effect and hereby increasing of current at high V_{DS}. Quazisaturation in HV FETs means that the high voltage drop in drift area caused by high electric field E_{lat} is limiting the drain current. This effect

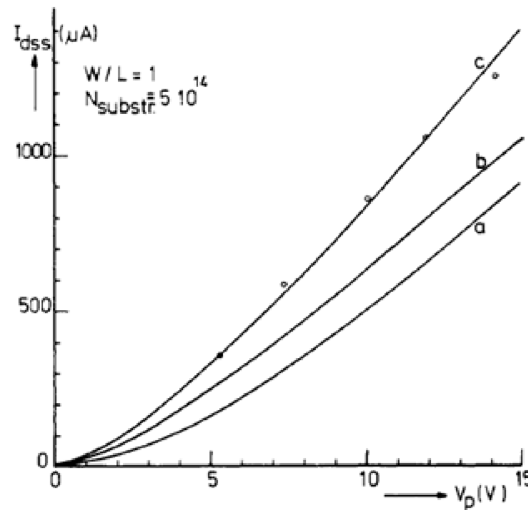

Figure 2.12: Drain saturation current as a function of pinch-off voltage a) RESURF JFET b) improved RESURF JFET c) Double RESURF JFET Reprinted from "High voltage, high current lateral devices", by Vaes, H. and Appels, J., 1980, Electron Devices Meeting (IEDM), 1980 IEEE International, vol. 26 p.89 © 1980 by the IEEE. Reprinted with permission, see App. B.

is observed typically in higher V_{DS}. In Fig. 2.14 and Fig. 2.15 200V LDMOS with very strong quazisaturation is demonstrated. This device operates as a MOSFET only very close to threshold voltage, which is V_{GS}=0.9V. At higher V_{GS} the electric field depletes the drift area and hereby strongly increases its resistivity. As described in Fig. 2.14, another increasing V_{GS} and opening the channel no more has an effect on the drain current, because the current is limited practically only by drift area. In output characteristics is quazisaturation visible as a current compression – see Fig. 2.15.
The self-heating sometimes shows the similar current compression, but it can be simply eliminated by pulse TLP measurement.

Using double RESURF in LDMOS body depicted in Fig. 2.13 causes the depletion of P layer and therefore minimizing of the unwanted quazisaturation effect. As was demonstrated in [45], structure b) from Fig. 2.13 has the current in saturation about two times higher than the structure a).

The principle question is, how to bias NBL. A plot of V_{BR} as a function of NBL voltage (Fig. 2.16) shows that even with a significant voltage difference between the NBL and drain, the V_{BR} is not compromised. Moreover, if the NBL is left floating, punch-through from drain to NBL causes the NBL

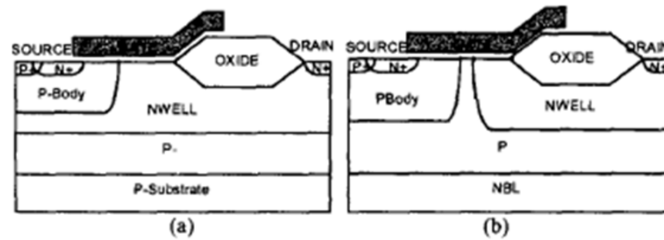

Figure 2.13: Schematic cross-section of the (a) conventional single RESURF structure with substrate grounded and (b) proposed double RESURF structure where heavily doped NBL is and independent terminal and can be externally tied to the drain terminal to achieve high breakdown voltage. Reprinted from "SOA improvement by a double RESURF LDMOS technique in power IC technology", by Parthasarathy, V. et al., 2000, Electron Devices Meeting (IEDM), 2000 Technical Digest. International, p.75 © 2000 by the IEEE. Reprinted with permission, see App. B.

voltage to float to approximately 25V below the drain resulting in almost optimal V_{BR} [45].

2.4 Multiple RESURF

2.4.1 Triple RESURF

Triple RESURF (Fig. 2.18) is a structure with floating P buried well inserted into N drift region to provide dual conduction path, which can provide a significant reduction in ON state resistance. The depletion of N doped drift area $\mathrm{N}_{\mathrm{drift}}$ is made from two sides, so the effect of RESURF is doubled.

2.4.2 Superjunction

The next RESURF extension is using multiple RESURF regions in charge balance as stacked horizontal layers or vertical regions [27]. This concept is called superjunction and it is using principle of multiple epitaxial layers (Fig. 2.19) or set of multiple deep trenches.

2.5 PB Extension RESURF

Structure called PB Extension RESURF is demonstrated in the Fig. 2.20. A P body layer was inserted into the n drift region from source terminal extended to drain side to set up transverse electric field to improve the

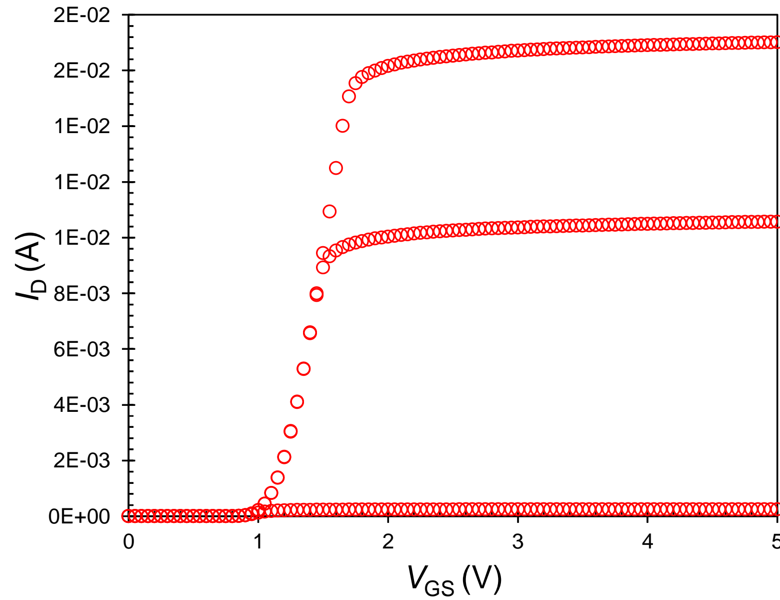

Figure 2.14: Example of $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristic of 200V LDMOS with very strong quazisaturation for $V_{\mathrm{DS}} = 0.1, 5, 10$ V. Early after threshold voltage the current is saturated.

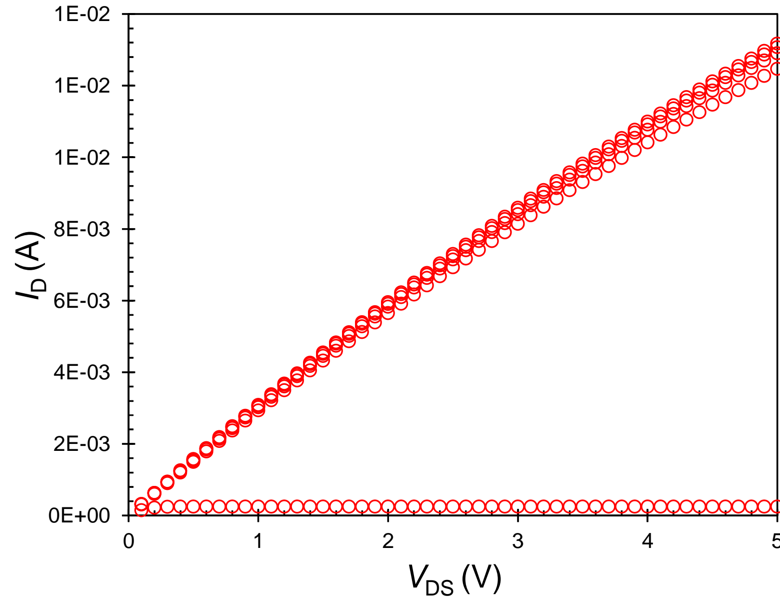

Figure 2.15: Example of $I_{\mathrm{D}}(V_{\mathrm{D}})$ characteristic of 200V LDMOS with very strong quazisaturation for $V_{\mathrm{GS}} = 1, 2, 3, 4, 5$ V. Current saturation from Fig. 2.14 is visible here as the current compression in $V_{\mathrm{GS}} > 1$ V.

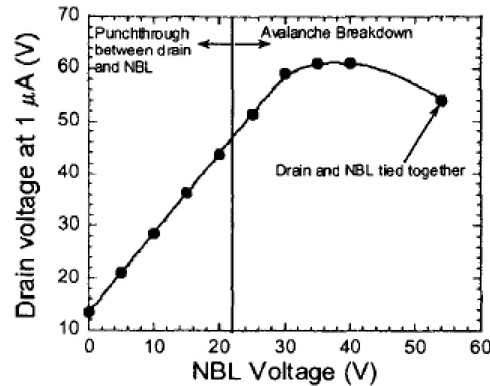

Figure 2.16: Measured breakdown voltage of the double RESURF device as a function of NBL bias. Reprinted from "SOA improvement by a double RESURF LDMOS technique in power IC technology", by Parthasarathy, V. et al., 2000, Electron Devices Meeting (IEDM), 2000 Technical Digest. International, p.77 © 2000 by the IEEE. Reprinted with permission, see App. B.

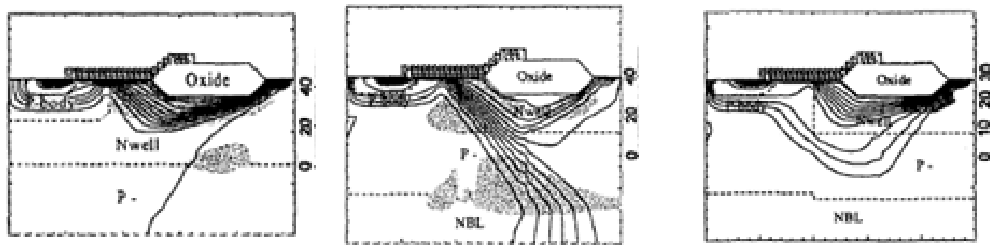

Figure 2.17: Simulation of current flowlines for single RESURF (a), double RESURF (b) and double RESURF with floating NBL (c). Shaded is impact ionization. Reprinted from "SOA improvement by a double RESURF LDMOS technique in power IC technology", by Parthasarathy, V. et al., 2000, Electron Devices Meeting (IEDM), 2000 Technical Digest. International, p.76, p.77, p.78 © 2000 by the IEEE. Reprinted with permission, see App. B.

distribution of electric field and thus increase the breakdown voltage. In fact it is a variation of the above described triple RESURF, however P buried layer is not floating, but is connected to the source.

This PB Extension layer is highly doped then n drift region and becomes fully depleted before device avalanche breakdown.

Fig. 2.21 shows the variation of breakdown voltage value as a function of PB Extension dose on this device. There exists an ideal dose of PB Exten-

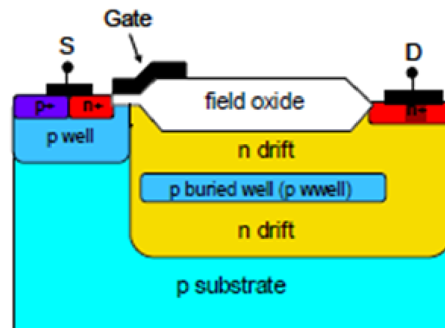

Figure 2.18: Cross-section of LDMOS with triple RESURF. Reprinted from "State-of-the-art Device in High Voltage Power ICs with Lowest ON State Resistance", by Su, R. et al., 2010, Electron Devices Meeting (IEDM), 2010 IEEE International, p.20.8.1. © 2010 by the IEEE. Reprinted with permission, see App. B.

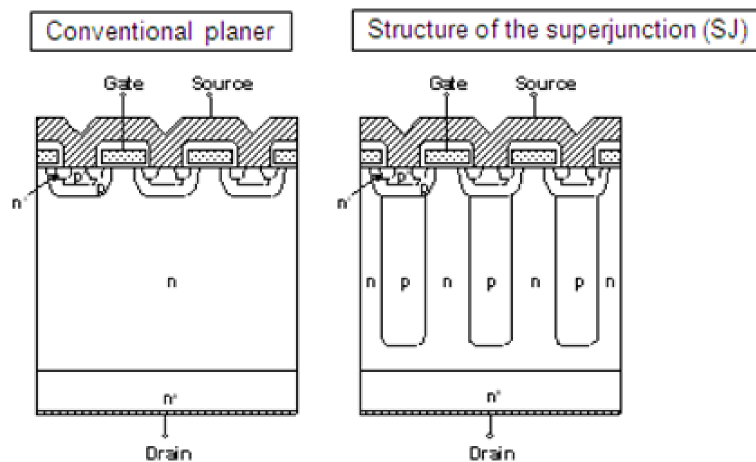

Figure 2.19: Comparison of conventional MOSFET and MOSFET using multiple RESURF structure.

sion for highest breakdown voltage as it is demonstrated in Fig. 2.21 [54]. Lower dose reduces the depletion of N_{drift}, higher dose reduces the depletion of PB Extension. Both layers, PB Extension and N_{drift} must be depleted before the avalanche breakdown is achieved. The [54] demonstrates, that the concept of PB Extension RESUFR has 40% improvement than Triple RESURF, 65% improvement then Double RESURF.

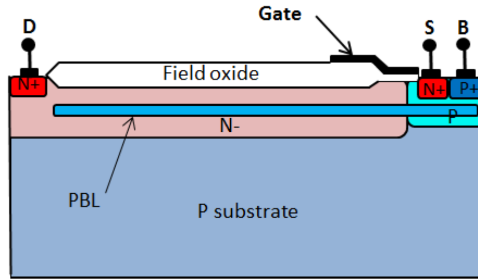

Figure 2.20: Cross-section of LDMOS with PB Extension RESURF.

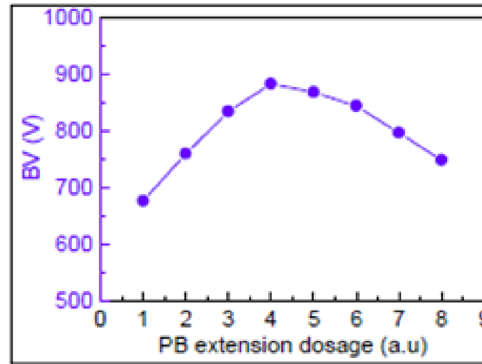

Figure 2.21: Breakdown voltage as a function of different PB Extension layers dosage. Reprinted from "State-of-the-art Device in High Voltage Power ICs with Lowest ON State Resistance", by Su, R. et al., 2010, Electron Devices Meeting (IEDM), 2010 IEEE International, p.20.8.3. © 2010 by the IEEE. Reprinted with permission, see App. B.

2.6 CLAVER LDMOS structure

Next principle of RESURF improvement is called Combined Lateral Vertical RESURF or shortly CLAVER. The proposed device cross-section is shown in the Fig. 2.22 (b). It shows the presence of a secondary Nwell used for the vertical junction termination. In the case of simple RESURF (Fig. 2.22 a), the drift region can support a maximum breakdown limited by the presence of the vertical junction. CLAVER structure exceeds this limitation by introducing a floating secondary drift region (Fig. 2.22 b). The device initially operates as a single RESURF LDMOS transitioning into double RESURF action after punch-through to bottom Nwell resulting in a graded double RESURF operation. Thus a combined lateral and vertical RESURF action shields the electrical field away from the bottom junction and results in an evenly-distributed potential across the primary drift region [24].

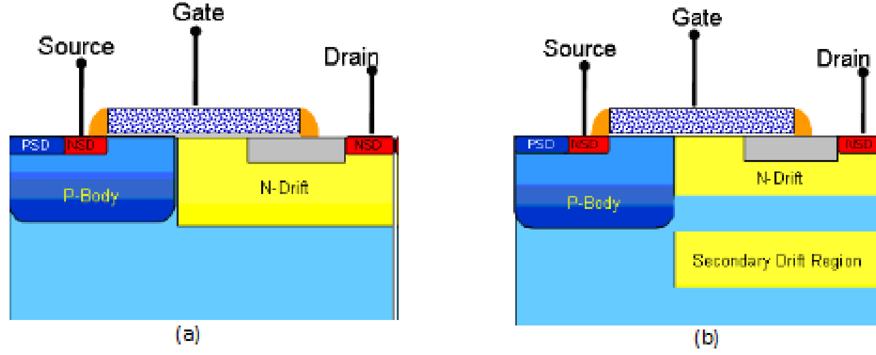

Figure 2.22: Cross-section of single RESURF LDMOS (a) and CLAVER RESURF LDMOS (b). Reprinted from "Combined Lateral Vertical RESURF (CLAVER) LDMOS structure", by Khan, T. et al., 2009, Power Semiconductor Devices IC's (IPSD), 2009 21st International Symposium, p.14. © 2010 by the IEEE. Reprinted with permission, see App. B.

2.7 Dielectric RESURF (Dieler)

The RESURF principle does not work only in silicon, but also in dielectrics. The method Dielectric RESURF (shortly DIELER) uses the principle, where the junctions or active region in CMOS are interleaved with dielectric region (STI) [53]. Let's demonstrate the technique on simple diode in Fig. 2.23 a). Simulated equipotential lines and depletion extension (dashed lines indicated with arrows at breakdown) are drawn. An identical diode with oxide along its edges inducing a wider depletion layer is depicted in Fig. 2.23 b) and Fig. 2.23 c). The fringing fields at the edge of the junction add to the junction capacitance, which is charged by extra depletion charge at the edge. This leads to a wider depletion layer and thus lower fields over the whole silicon width and therefore higher breakdown voltage. The effect s schematically indicated in Fig. 2.23 d).

The total capacitance consists of the junction (silicon) capacitance combined with the dielectric capacitance and can be expressed as:

$$C_{\text{total}} = \frac{\epsilon_{\text{Si}} W_{\text{Si}} + \epsilon_{\text{diel}} W_{\text{diel}}}{d_{\text{depl}}} \tag{2.8}$$

with d_{depl} being the depletion layer length. The charging of the extra dielectric capacitance has to originate in depletion layer and therefore the depletion layer will widen. Consequently at the same reverse bias the electrical field lowers and the breakdown voltage increases as it is described in Fig. 2.23. The silicon width has to be smaller than the depletion length d_{depl} to get a wider depletion over the whole silicon width [53].

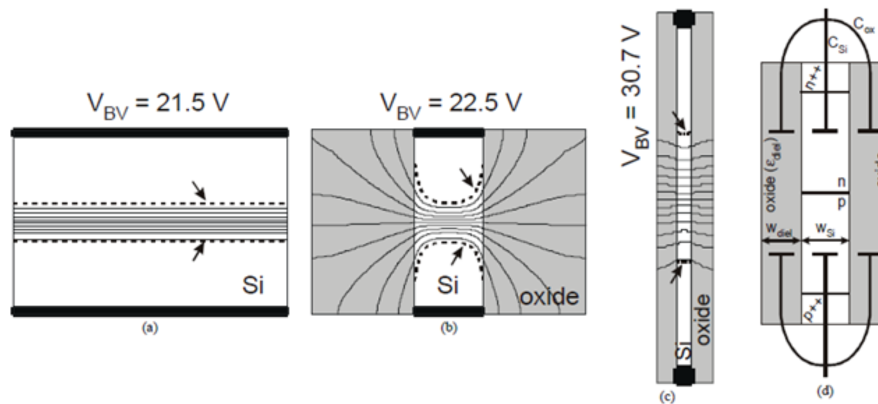

Figure 2.23: Schematics of (a) simple p-n diode, (b) wide and (c) narrow (2x magnified for clarity) p-n diode embedded with and oxide layer, and a double capacitor equivalent circuit model (d). Reprinted from "Dielectric resurf: breakdown voltage control by STI layout in standard CMOS", by Sonsky, J. and Heringa, A., 2005, Electron Device Meeting (IEDM), 2005 IEEE International, p.376. © 2005 by the IEEE. Reprinted with permission, see App. B.

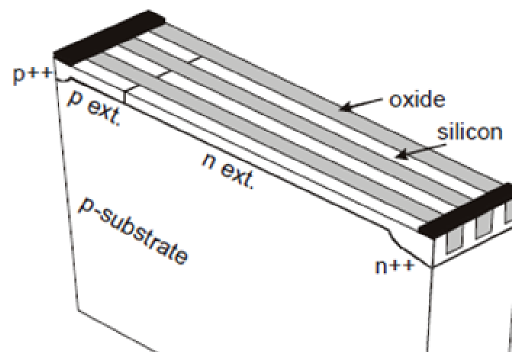

Figure 2.24: DIELER diode in standard CMOS technology. The dielectric RESURF is implemented by introducing shallow trench isolation (STI). Reprinted from "Dielectric resurf: breakdown voltage control by STI layout in standard CMOS", by Sonsky, J. and Heringa, A., 2005, Electron Device Meeting (IEDM), 2005 IEEE International, p.376. © 2005 by the IEEE. Reprinted with permission, see App. B.

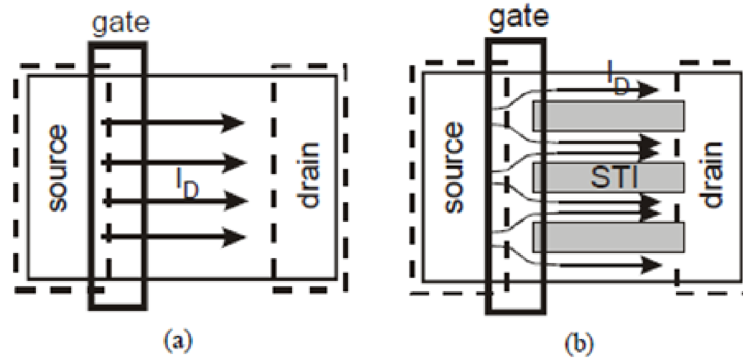

Figure 2.25: NMOS transistor layout (a) with a conventional extended drain region and (b) with DIELER structure in the extended drain region, used for measurement in Fig. 2.26. Reprinted from ”Dielectric resurf: breakdown voltage control by STI layout in standard CMOS”, by Sonsky, J. and Heringa, A., 2005, Electron Device Meeting (IEDM), 2005 IEEE International, p.376. © 2005 by the IEEE. Reprinted with permission, see App. B.

The application dielectrical RESURF by STI to the MOFETs is demonstrated in Fig. 2.25 and Fig. 2.26. It is clear, that the breakdown voltage was by DIELER increased $\sim 2\times$, while the specific drain current is almost equal for both transistors and the increase of the R_{on} is $\sim 2\times$ [53].

2.8 Interdigitated Source Structure

As was mentioned earlier, high voltage LDMOS requires high breakdown immunity and minimum size. For the improvement of breakdown immunity normal structure LDMOS (Fig. 2.27 b) needs P+ implant to form a low-resistance strip contacted with p-well in addition to conventional CMOS process. On the other hand, interdigitated source LDMOS (Fig. 2.27 a) can achieve high breakdown immunity without the additional process, because P+ well contacts are located near the gate. And it can reduce chip size and manufacturing cost, because P+ well contacts can be fabricated by conventional CMOS process.

Publication [55] is dealing with SPICE modeling of interdigitated source, because the conventional model does not contain this effect. The parasitic resistance near the source P+ region is not formulated in the conventional compact models. It does not calculate with the W_{n}/W (the ratio of the total width of the N+ source region by the whole width). Therefore, the new modeling concept is proposed.

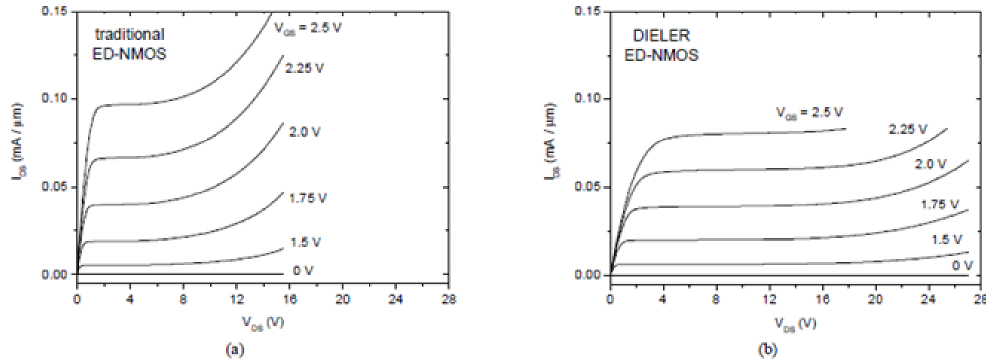

Figure 2.26: Measured ON state characteristics for an NMOS transistor with a conventional extended drain region (a) and with DIELER structure in the extended drain region (b). Reprinted from "Dielectric resurf: breakdown voltage control by STI layout in standard CMOS", by Sonsky, J. and Heringa, A., 2005, Electron Device Meeting (IEDM), 2005 IEEE International, p.376. © 2005 by the IEEE. Reprinted with permission, see App. B.

As it is demonstrated in Fig. 2.28, the non-inverted region near the source P+ does not have a large effect on the total charge amount when the device operates in the linear region, while it has a large effect in the saturation region. Figs. 2.29 and 2.30 show the proposed equivalent circuit and proposed macromodel.

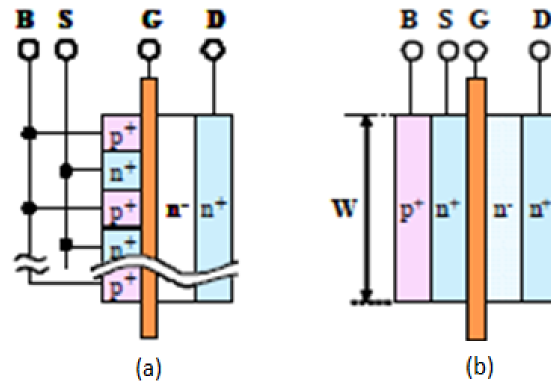

Figure 2.27: Mask layout of interdigitated source LDMOS (a) and normal structure LDMOS (b). Reprinted from ”Accurate Spice modeling of 80V power LDMOS with interdigitated source structure”, by Tamegaya, Y. et al, 2012, Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium, p.101. © 2012 by the IEEE. Reprinted with permission, see App. B.

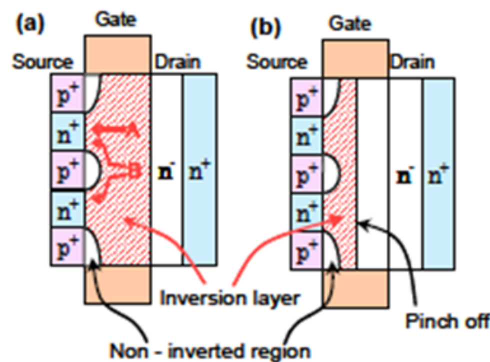

Figure 2.28: Shapes of Inversion layer spread. (a) Linear region, (b) Saturation region. Reprinted from ”Accurate Spice modeling of 80V power LDMOS with interdigitated source structure”, by Tamegaya, Y. et al, 2012, Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium, p.102. © 2012 by the IEEE. Reprinted with permission, see App. B.

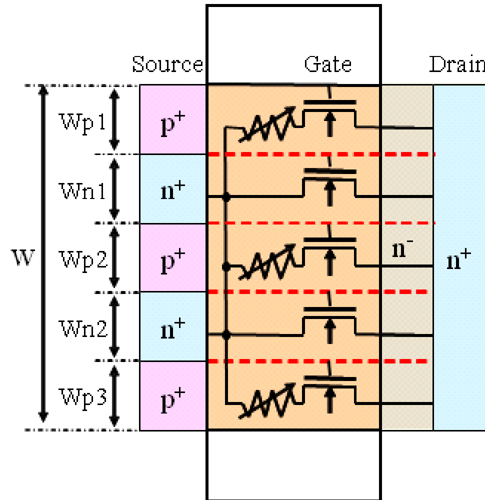

Figure 2.29: Equivalent circuit of interdigitated source LDMOS. Reprinted from "Accurate Spice modeling of 80V power LDMOS with interdigitated source structure", by Tamegaya, Y. et al, 2012, Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium, p.102. © 2012 by the IEEE. Reprinted with permission, see App. B.

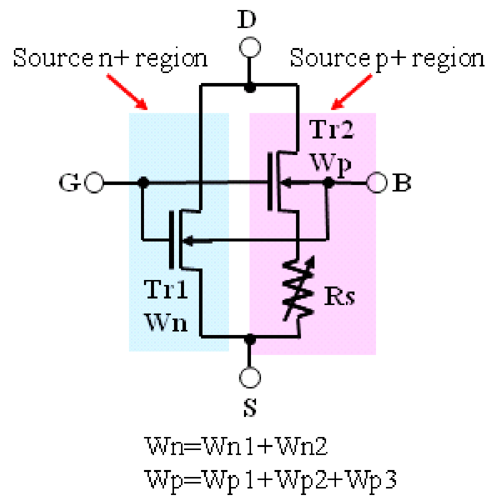

Figure 2.30: Proposed Macromodel of interdigitated source LDMOS. Reprinted from "Accurate Spice modeling of 80V power LDMOS with interdigitated source structure", by Tamegaya, Y. et al, 2012, Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium, p.102. © 2012 by the IEEE. Reprinted with permission, see App. B.

CHAPTER 3

Comprehensive Behavioral Model of Dual-Gate High Voltage JFET and Pinch Resistor

3.1 Introduction

This chapter published in [5] deals with the development of new behavioral Verilog-A model of JFET, containing all the parasitic phenomena required for the simulation and universally applicable for many macromodels.

The first prototype of the model based on SPICE arbitrary sources was developed in Motorola [59], but its accuracy was limited, the simulation time was too long, the versatility was not so universal and mainly the model didn't converge well.

It was necessary to solve several convergence issues. The model was linearized for very low voltages, where the pinching effects do not exist and the linearized equation was sewed with the main voltage dependent model without any impact on convergence. Existing voltage dependent equations were adjusted to be able to remove existing recursion. Both solutions significantly improved the simulation speed and the convergence.

There were introduced additional effects, e.g., pinch-off voltage width dependency, pinching effect in gate capacitance, impact ionization or statistical distribution.

The model was extended for the use in various applications, e.g., high voltage LDMOS drift area in combination with PSP [19], HiSIM [41], HiSIM HV [33, 34] or BSIM4 [26] compact MOSFET model.

Another application, where the model can be used, is pinch resistor, where using the conventional compact JFET model is very insufficient.

Finally, the model can also be used as a dual gate JFET (high voltage JFET with two independent gates). Dual gate JFET is a device, which is not supported with the compact SPICE models, although there exist several important applications [31].

The most of existing publications about (dual gate) JFET model are focused on DC parameters [61, 57, 58, 37]. The goal of this thesis is to present the complex universal model, containing all the required phenomena, including parasitic effects, anomalies and statistical properties.
The chapter is organized into several sections:

- Section DC Model demonstrates the evolution of the model and its application in various high voltage devices, namely high voltage pinch resistor and dual gate JFET, where each one requires a different concept. For example while for the pinch resistor lateral pinching is important and hence the width dependent pinch-off, for the oval shape high voltage JFET this effect is invisible. On the other side, as depicted in Fig. 3.9, below mentioned high voltage JFET has two independent gates (substrate from the bottom and P implant from the top), which requires to implement the interaction between these two gates in the model.

- Section Capacitance model describes the principle of the gate capacitance modeling, which especially in dual-gate JFET is not trivial. This topic is quite complex, so it is described in more details in **chapter 4.** The frequency model was also extended by the modeling of reverse recovery of both gates, which is not part of this chapter. The reverse recovery is the independent Verilog-A module applicable not only in JFET, so there is a special **chapter 6** describing this topic.

- Section Parasitic DC Model, Gate current deals with the modeling of leakage and impact ionization gate current of both gates. This part can be also used independently in whatever macromodel, not only in JFET.

- Section Temperature model describes the model temperature scalability.

- Section Statistical model describes the modeling of technology statistical distribution of the JFET using method Backward Propagation of Variances [36, 39]. A special case is the modeling of the bi-modal statistical distribution, which is described in **chapter 7**.

- Extracted Model Parameters contains table of model parameters extracted for two device representatives: dual gate JFET and pinch resistor.

It is apparent, that this chapter represents the core of the model and the following chapters represent following extension of the model.

3.2 DC Model

3.2.1 Customized compact JFET model

Let's start with the 3-terminal JFET modeled by Shichman-Hodges model for linear region ($0 < V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{th}})$). The current flowing from drain to source is defined as [60]

$$I_{\mathrm{DS}} = \beta V_{\mathrm{DS}}(1 + \lambda V_{\mathrm{DS}})\Big(2(V_{\mathrm{GS}} - V_{\mathrm{th}}) - V_{\mathrm{DS}}\Big) \tag{3.1}$$

where β is the transconductance parameter, λ is velocity overshoot coefficient, and V_{th} is threshold (pinch-off) voltage.

For the size dependency evaluation let's consider JFET in linear region, where V_{GS} and V_{DS} are very close to 0 volts. The resistance of JFET is then defined as

$$R = \frac{V_{\mathrm{DS}}}{I_{\mathrm{DS}}} = \frac{1}{-2\beta V_{\mathrm{th}}} = R_{\mathrm{SH}}\frac{L + \Delta_{\mathrm{L}}}{W + \Delta_{\mathrm{W}}} \tag{3.2}$$

where R_{SH} is the sheet resistance, Δ_{L} is length offset and Δ_{W} is width offset. The transconductance parameter can then be expressed as

$$\beta = -\frac{1}{2V_{\mathrm{th}}R} = -\frac{1}{2V_{\mathrm{th}}R_{\mathrm{SH}}\frac{L+\Delta_{\mathrm{L}}}{W+\Delta_{\mathrm{W}}}} \tag{3.3}$$

Substituing (3.3) in (3.1) the JFET model becomes scalable with the resistor length and width and suitable for modeling voltage-dependent resistors.

The next phenomenon which has to be taken into account is the impact of a lateral pinching and its width dependency. The voltage dependent resistor is typically pinched from 3 sides: bottom, right and left. For very wide shallow resistors, bottom pinching dominates, while narrow deep resistors are dominated by right and left pinching. This effect is modeled by the parametrization of JFET parameter V_{th} as described in the following equation

$$V_{\mathrm{th}} = \frac{V_{\mathrm{thinf}}}{1 + \frac{2x_{\mathrm{j}}}{W}} \tag{3.4}$$

where V_{thinf} is the threshold (pinch-off) voltage for infinitely wide resistor and x_j is resistor depth. The model is sufficient for most voltage dependent diffusion or implant resistors, but its use for the real pinch resistor, operating in the saturation region, is limited.

3.2.2 Behavioral JFET model - first prototype

Therefore a behavioral pinch resistor model was developed based on the following physical elements: vertical and lateral built-in potentials [59]

$$\psi_{\mathrm{v}} = \frac{k_{\mathrm{b}}T}{q} \ln \frac{N_{\mathrm{body}} N_{\mathrm{tub}}}{n_{\mathrm{i}}^2} \tag{3.5}$$

$$\psi_{\mathrm{l}} = \frac{k_{\mathrm{b}}T}{q} \ln \frac{N_{\mathrm{side}} N_{\mathrm{tub}}}{n_{\mathrm{i}}^2} \tag{3.6}$$

and vertical and lateral pinching factors [59]

$$\alpha_{\mathrm{v}} = \sqrt{2\epsilon_0\epsilon_r \frac{N_{\mathrm{tub}}}{qN_{\mathrm{body}}(N_{\mathrm{body}} + N_{\mathrm{tub}})}} \tag{3.7}$$

$$\alpha_{\mathrm{l}} = \sqrt{2\epsilon_0\epsilon_r \frac{N_{\mathrm{tub}}}{qN_{\mathrm{side}}(N_{\mathrm{side}} + N_{\mathrm{tub}})}} \tag{3.8}$$

where k_{b} is Boltzmann constant, T is absolute temperature, q is elementary charge, n_{i} is intrinsic carrier concentration of used material, ϵ_0 is vacuum permitivity, ϵ_r is permitivity of used material, and N_{body}, N_{side}, N_{tub} are tuning parameters described in Table 3.1.

The total current between drain and source derived from [59] is

Table 3.1: DC parameters of JFET.

Parameter name	**Parameter description**	**Unit**
N_{body}	JFET body (drift area) concentration	cm^{-3}
N_{side}	side concentration of JFET body	cm^{-3}
N_{tub}	gate (substrate) concentration	cm^{-3}
x_{j}	JFET depth	µm
λ	Velocity overshoot coefficient	V^{-1}
r_{ho}	Linear resistance concentration	$\Omega\mu\mathrm{m}^{-1}$
Δ_{L}	Length offset	µm
Δ_{W}	Width offset	µm

$$I_{\mathrm{res}} = \frac{V_{\mathrm{DG}} - V_{\mathrm{SG}}}{r_{\mathrm{ho}}\left(L + \Delta_{\mathrm{L}}\right)}\left(1 + \lambda V_{\mathrm{DS}}\right) \times \left(W - 2\alpha_{\mathrm{l}}\sqrt{\psi_{\mathrm{l}} + \frac{V_{\mathrm{DG}} + V_{\mathrm{SG}}}{2}} + \Delta_{\mathrm{W}}\right) \times \left(x_j - \alpha_{\mathrm{v}}\sqrt{\psi_{\mathrm{v}} + \frac{V_{\mathrm{DG}} + V_{\mathrm{SG}}}{2}}\right) \quad (3.9)$$

where r_{ho} is tuning parameter described in Table 3.1. The original equation of I_{res} in [59] contains additional effect of top pinching caused by metal plate above field oxide. However, this effect does not exist in devices described below and it is not considered here.

The saturation of current I_{res} is handled by setting the derivative of (3.9) with respect to V_{DG} equal to zero, which expresses saturation voltage V_{DGsat}. The applied V_{DG} and V_{DGsat} are then fed into a conventional saturation smoothing function, resulting in an effective bias V_{DGeff} [59], substituted for V_{DG} in (3.9). However, the solution could not be obtained explicitly, therefore it was iteratively solved by the simulator during simulation using a dedicated circuit containing arbitrary sources.

Although the smooth and continuous transition from the linear region into saturation region was ensured, the simulation time was relatively long and in some cases even convergence issues appeared. Therefore some improvements were introduced.

3.2.3 DC model of pinch resistor

First of all, the pinch resistor has no top pinching caused by the metal/poly flap, described in [59]. The top and bottom pinching have both the same physical basis, only the gate concentration is different. However, the top gate is shorted to the substrate, as illustrated in Fig. 3.1. We can thus consider only one pinching gate, which simplifies (3.9) and enables us to express the explicit solution of V_{DGeff} and V_{SGeff}. This significantly improves model convergence and simulation speed. Thus, no recursive function is required in the model any more.

The next step was linearization of the model close to V_{DS}=0V, where a too complicated calculation of the current caused the convergence issues. Therefore the model was divided into three operation areas.

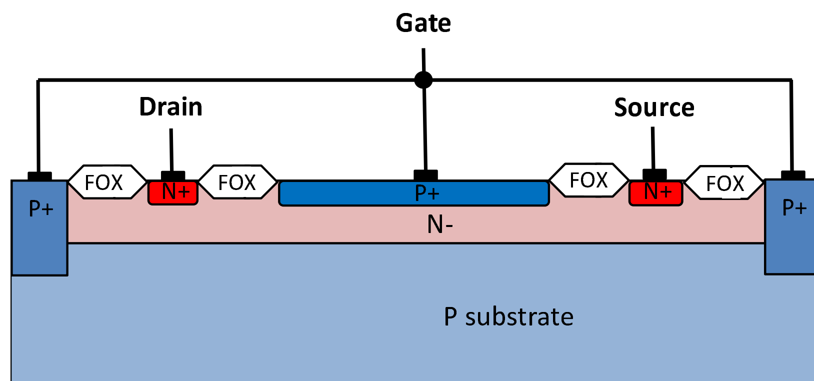

Figure 3.1: Cross-section of pinch resistor (simple JFET).

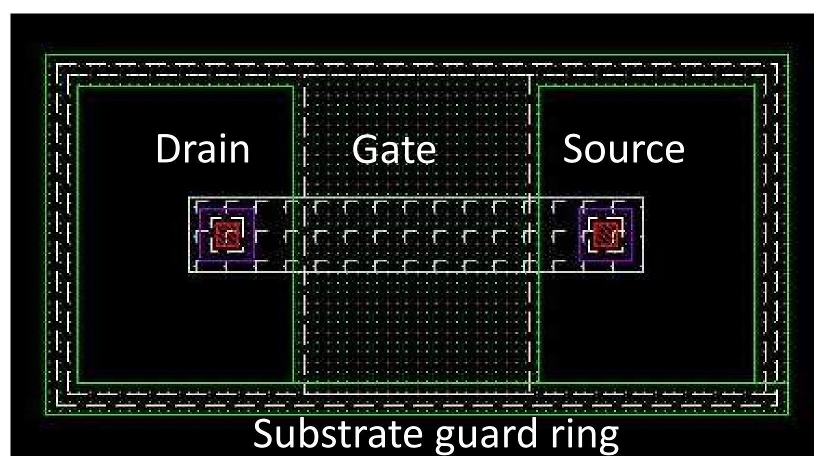

Figure 3.2: Layout of pinch resistor (simple JFET).

For $V_{\mathrm{DS}} > 1$ nV:

$$I_{\mathrm{res}} = \frac{V_{\mathrm{DSeff}}}{r_{\mathrm{ho}}\left(L + \Delta_{\mathrm{L}}\right)}\left(1 + \lambda V_{\mathrm{DS}}\right) \times \left(W + \Delta_{\mathrm{W}} - \mathrm{GMOD} \times 2\alpha_{\mathrm{l}}\sqrt{\psi_{\mathrm{l}} + \frac{V_{\mathrm{DSeff}} + r_{\mathrm{sub}}V_{\mathrm{SG}}}{2}}\right) \times \left(x_j - \alpha_{\mathrm{v}}\sqrt{\psi_{\mathrm{v}} + \frac{V_{\mathrm{DSeff}} + r_{\mathrm{sub}}V_{\mathrm{SG}}}{2}}\right) \quad (3.10)$$

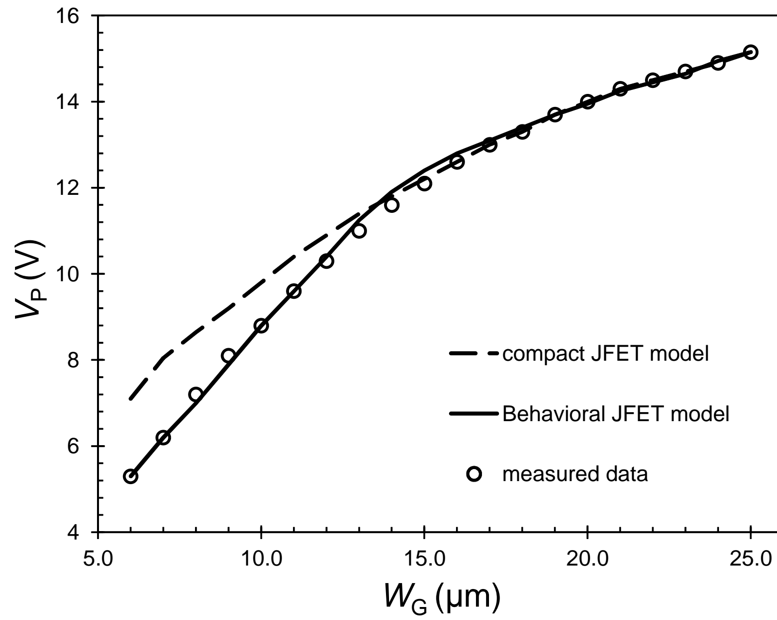

Figure 3.3: Width dependency of pinch-off voltage in pinch resistor.

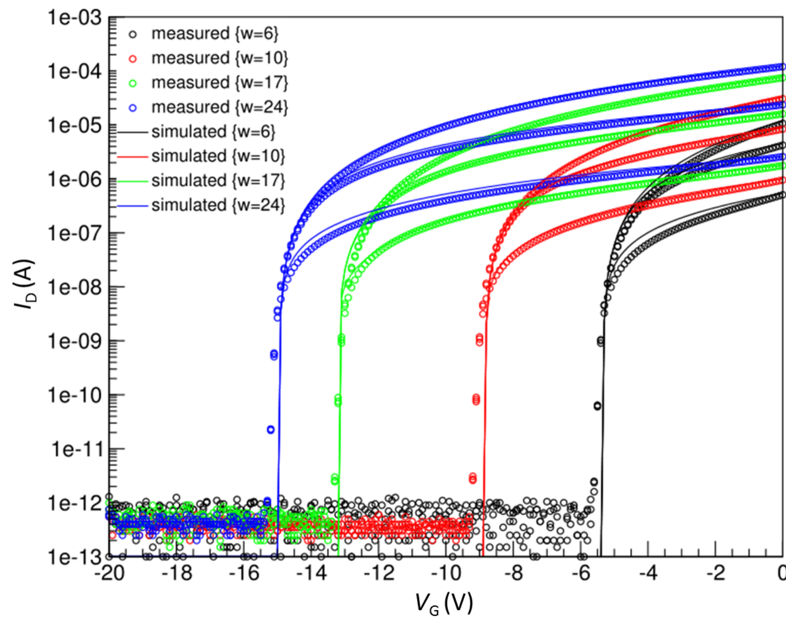

Figure 3.4: Pinch resistor I_D-V_G characteristics for L=100 µm and W=6, 10, 17, 24 µm. V_{DS}=0.1, 1, 10 V.

Table 3.2: Additional DC parameters for pinch resistor.

Param.	Description	Unit
GMOD	geometry model selector	-
r_{sub3}	3rd order width dependency coefficient of r_{sub}	m^{-3}
r_{sub2}	2nd order width dependency coefficient of r_{sub}	m^{-2}
r_{sub1}	1st order width dependency coefficient of r_{sub}	m^{-1}
r_{sub0}	independent tuning parameter for pinchoff voltage	-

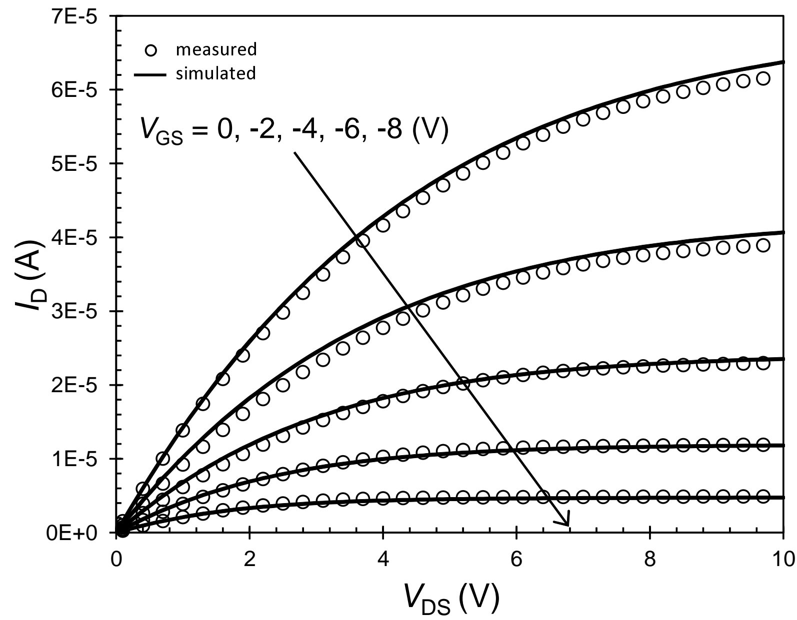

Figure 3.5: Pinch resistor I_{D}-V_{D} characteristic for W=15 µm and L=100 µm. V_{GS}=0, −2, −4, −6, −8 V.

For $V_{\mathrm{DS}} < -1$ nV:

$$I_{\mathrm{res}} = -\frac{V_{\mathrm{SDeff}}}{r_{\mathrm{ho}}\left(L+\Delta_{\mathrm{L}}\right)}\left(1+\lambda V_{\mathrm{SD}}\right)\times \left(W+\Delta_{\mathrm{W}}-\mathrm{GMOD}\times 2\alpha_{\mathrm{l}}\sqrt{\psi_{\mathrm{l}}+\frac{V_{\mathrm{SDeff}}+r_{\mathrm{sub}}V_{\mathrm{DG}}}{2}}\right)\times \left(x_j-\alpha_{\mathrm{v}}\sqrt{\psi_{\mathrm{v}}+\frac{V_{\mathrm{SDeff}}+r_{\mathrm{sub}}V_{\mathrm{DG}}}{2}}\right) \quad (3.11)$$

For $V_{\mathrm{DS}} \in \langle -1\ \mathrm{nV}, 1\ \mathrm{nV}\rangle$:

$$I_{\mathrm{res}} = \frac{V_{\mathrm{DSeff}}}{r_{\mathrm{ho}}(L+\Delta_{\mathrm{L}})}\left(W+\Delta_{\mathrm{W}}\right)x_j \quad (3.12)$$

where r_{sub} is the parameter for fine tuning of pinch-off voltage, and GMOD is geometry model selector for the optional disconnection of lateral pinching in the case of oval or circle device shape. V_{DSeff} in (3.10) and (3.12) represents $(V_{\mathrm{DGeff}} - V_{\mathrm{SGeff}})$ described in [59], where the substitution of V_{DGeff} and V_{SGeff} into (3.9) provides a smooth, continuous transition from the linear region into saturation. A similar definition holds for V_{SDeff} in (3.11). All three operation areas (3.10, 3.11, 3.12) are sewed, so there is no discontinuity between them. Both the function and its first derivative are continuous. A similar concept was used for capacitance equations in [11].

Velocity saturation, resulting from the longitudinal electric field, is negligible due to the increased pinching effect saturation dominance induced by the surface depletion [59]. As shown in Fig. 3.7, the model length scalability is sufficient even for relatively short dimensions. On the other hand Fig. 3.8 demonstrates that the pinch-off voltage is length independent.

The side pinching causes nonlinear width dependency of pinch-off voltage, as shown in Figs. 3.3 and 3.4. This dependency can be significantly improved by the use of second or third order polynomial of parameter r_{sub} on a limited interval of widths.

$$r_{\mathrm{sub}} = W^3 r_{\mathrm{sub3}} + W^2 r_{\mathrm{sub2}} + W r_{\mathrm{sub1}} + r_{\mathrm{sub0}} \quad (3.13)$$

where r_{sub3}, r_{sub2}, r_{sub1}, and r_{sub0} are tuning parameters described in Table 3.2. In the case of using the model for a stripe-shaped device with an unlimited width, the parameters r_{sub3}, r_{sub2} and r_{sub1} must be set to zero. This ensures that r_{sub} is constant.

The model was created in the Verilog-A language [16, 49] as a voltage-controlled current source with auxiliary voltage sources. The modifications described in this section significantly improved the model accuracy as well as the simulation speed, and solved all the reported convergence issues. The

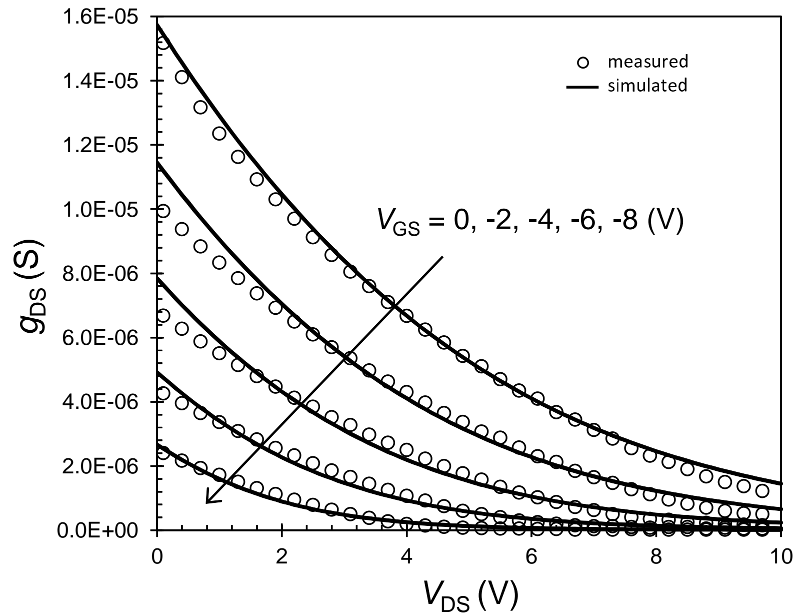

Figure 3.6: Pinch resistor transconductance characteristic for W=15 µm and L=100 µm. V_{GS}=0, −2, −4, −6, −8 V.

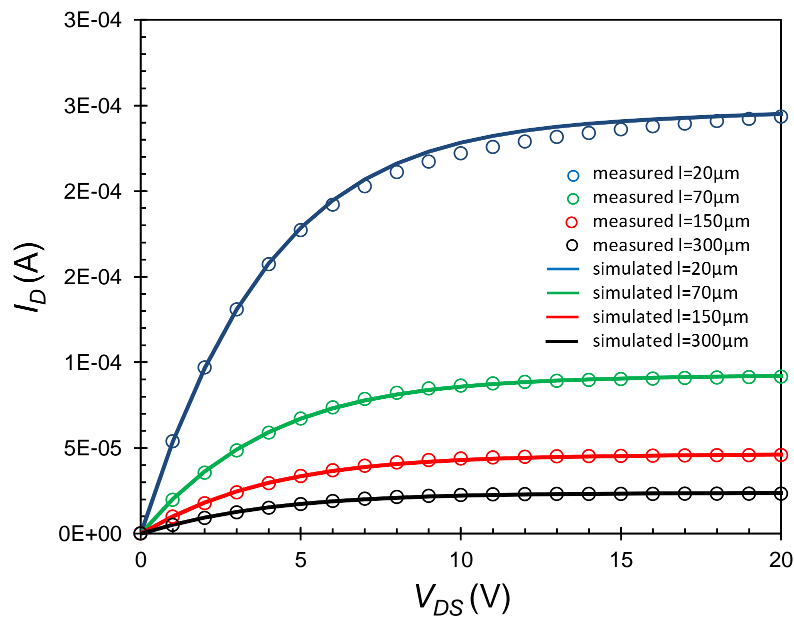

Figure 3.7: Pinch resistor I_D-V_D characteristic for W=15 µm and L=20, 70, 150, 300 µm. V_{GS}=0 V.

model is universal and applicable in various high voltage macromodels (e.g. DMOS).

So far, we dealt with a 3-terminal (1 gate) JFET. The following section is focused on oval shape dual-gate JFET, used mainly for high voltage applications (in our case 200V and 700V applications).

3.2.4 DC model of dual gate JFET

Examples of the dual-gate JFET applications can be found in [31]. Example described below has a circular or oval shape with the high voltage pad in the center, as illustrated in Fig. 3.9. This configuration ensures that the high voltage applied to the drain appears only in vertical direction in the center of the oval where the high voltage breakdown is ensured by low substrate concentration. Sufficient drift length or other techniques (e.g. double RESURF [27]) make sure that this high voltage does not appear in the device's perimeter and the device can operate at such high voltages.

However, due to the layout configuration there is no pinch-off voltage width dependency, described in previous section. On the other hand, it is important to implement the impact of two independent gates - the top gate (gate1) and the substrate (gate2). The device can be pinched either by the substrate or by the top gate or by both.

The first idea was to extend (3.10) and (3.11) by adding gate2 pinching - similarly as in (3.9). However, this solution would make the equation too complicated and would require to go back to the original calculation of V_{DG2eff} and V_{SG2eff} with the convergence issues. Therefore, it was decided to reuse the idea of the parameter r_{sub} from (3.10) and (3.11) to parametrize pinch-off. In this case it was not parametrized with the device width but with potential at gate2

$$r_{\mathrm{sub}} = r_{\mathrm{subb}} V_{\mathrm{SG2}} + r_{\mathrm{subd}} \ln\left(F_{\mathrm{n}} \sqrt{V_{\mathrm{DS}}^2 + K} \right) + r_{\mathrm{sub0}} \tag{3.14}$$

where r_{subb}, r_{subd}, and r_{sub0} are model parameters described in Table 3.3, F_{n}=1V^{-1} is a normalization factor, and K prevents the logarithm from becoming enormous and ensures a smooth dependency on V_{DS}.

Table 3.3: Additional DC parameters for dual-gate JFET.

Parameter	Description	Unit
r_{sub0}	independent tuning parameter for pinchoff voltage	-
r_{subb}	rsub dependency on V_{SG2}	V^{-1}
r_{subd}	rsub dependency on V_{DS}	-

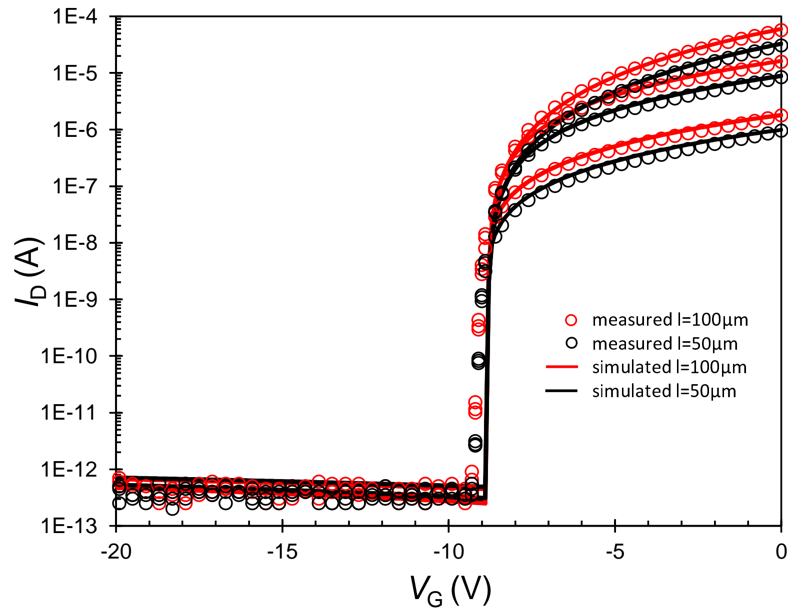

Figure 3.8: Pinch resistor I_D-V_G characteristic for W=10 µm and L=50, 100 µm. V_{DS}=0.1, 1, 10 V.

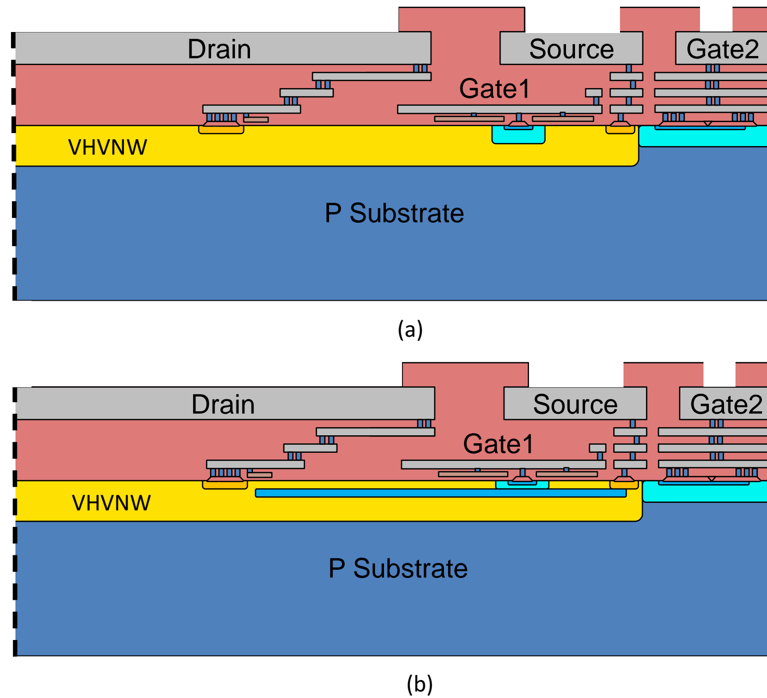

Figure 3.9: Cross-section of dual-gate JFET. (a) gate1 above part of the channel (b) gate1 above whole channel.

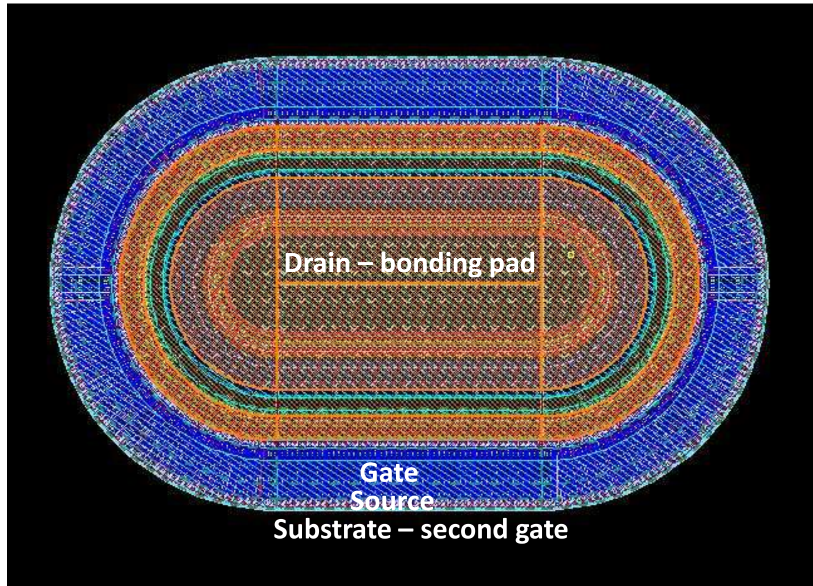

Figure 3.10: Layout of oval shape dual-gate JFET with effective gate width wg = 500µm. Drain bonding pad is in the center of the oval.

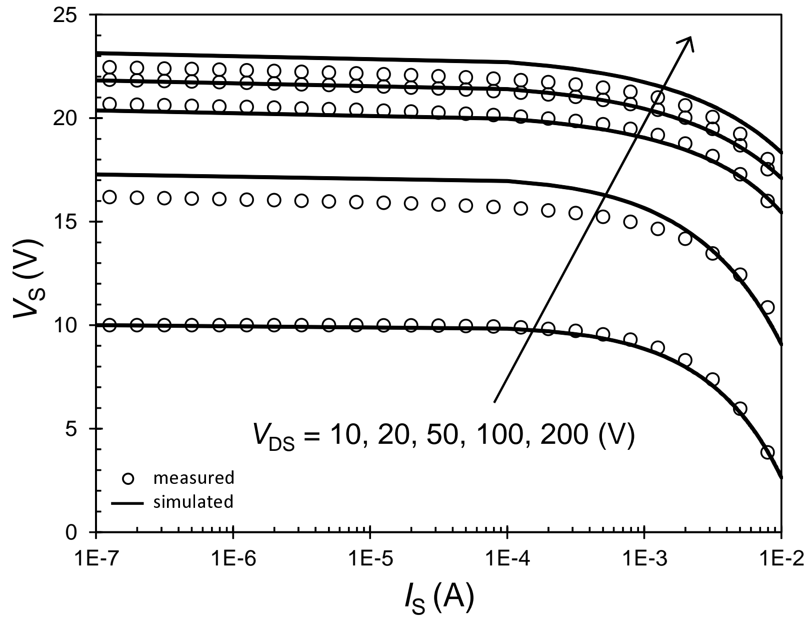

Figure 3.11: Dual-gate JFET load-line for $V_{G1} = V_{G2} = 0$ V and parametrized V_D.

This equation is valid only in the forward direction. For reverse direction, V_{SG2} is replaced with V_{DG2} and V_{DS} with V_{SD}.

The key characteristic of the high voltage dual-gate JFET is the load-line, describing the source voltage V_{S} vs source current I_{S} dependency, where the V_{S} value represents the pinch-off voltage. I_{S} is the JFET source current here. The saturation current described in following chapters is subscripted with gate and denoted with the symbol I_{SGn}. The load-line demonstrating pinch-off dependency on V_{D} is shown in Fig. 3.11, and the load-line demonstrating pinch-off dependency on V_{G1} is in Fig. 3.12.

3.3 Capacitance Model

The most significant capacitance in conventional compact JFET model is the capacitance of p-n junction between the JFET body and JFET gate. This capacitance is included in the model typically as two voltage dependent capacitors, one between drain and gate, and the second one between source and gate. Each one represents the capacitance of half of the p-n junction area.

In the conventional model it is described by C-V equation [32, 60]

$$C = \frac{C_{\text{j0}}}{\left(1 - \frac{V}{V_{\text{j}}}\right)^{M_{\text{j}}}} \times \text{AREA} \tag{3.15}$$

where C_{j0} is the zero-bias junction capacitance per unit area, V_{j} is junction built-in potential, M_{j} is grading coefficient, and AREA is the area of pn junction (representing the half of JFET gate area). In the case of dual-gate JFET there are two p-n junctions, so there are four voltage dependent capacitors in the model, as depicted in Fig. 3.13.

Moreover, the pinch-off voltage can be observed not only in DC curves but also in CV curves, as shown in Fig. 3.14. When the voltage across the p-n junction reaches the critical value V_{poff}, the JFET body becomes fully depleted, and the capacitance steeply drops down. The same effect was observed also in gate capacitances of MESFET/pHEMT or microwave varactors [12].

In this case it was implemented into (4.1) using a dimensionless multiplication factor C_{multGn}

$$C_{\text{multGn}} = \left(\sqrt{(V + V_{\text{poffGn}})^2 + S_{\text{Gn}}} + 0.5\text{V} - \sqrt{(V + V_{\text{poffGn}} - 0.5\text{V})^2 + S_{\text{Gn}}} \right) \times \text{CMOD} \tag{3.16}$$

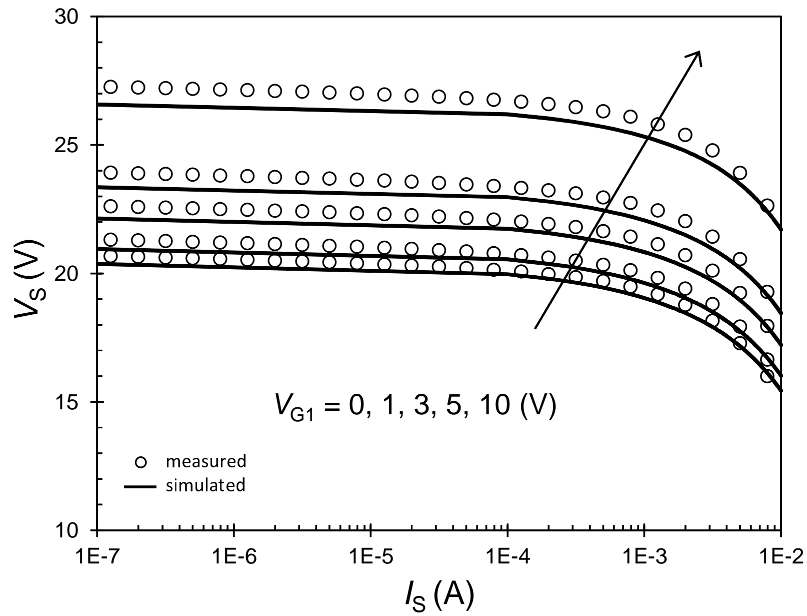

Figure 3.12: Dual-gate JFET Load-line for $V_{\mathrm{G2}} = 0$ V $V_{\mathrm{D}} = 50$ V and parametrized V_{G1}.

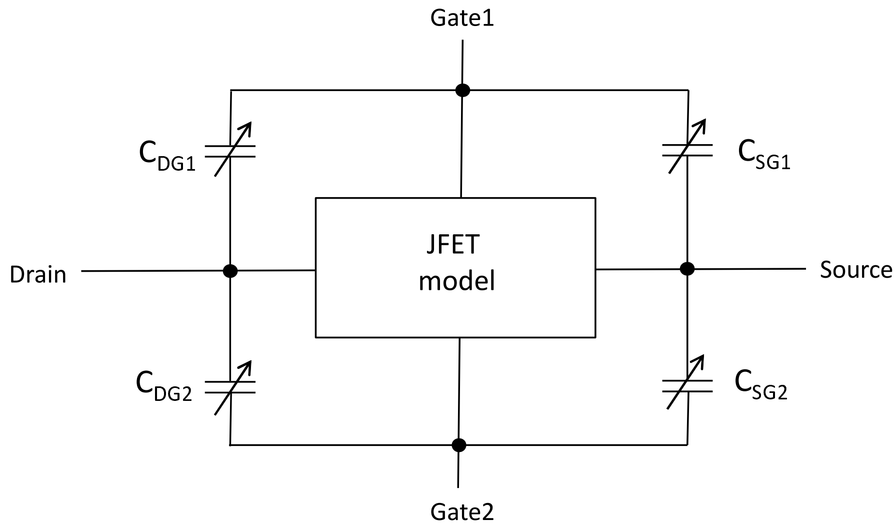

Figure 3.13: Simplified CV macromodel of dual-gate JFET.

Table 3.4: Capacitance parameters for JFET (pinch resistor).

Param.	Description	Unit
CMOD	capacitance model selector	V^{-1}
C_{j0G1}	gate1 capacitance per unit area at zero bias	$\mathrm{F\mu m}^{-2}$
V_{jG1}	gate1 built-in potential	V
M_{jG1}	gate1 grading coefficient	-
V_{poffG1}	gate1 capacitance pinching voltage	V
S_{G1}	steepness of gate1 capacitance drop	V^2
C_{j0G2}	gate2 capacitance per unit area at zero bias	$\mathrm{F\mu m}^{-2}$
V_{jG2}	gate2 built-in potential	V
M_{jG2}	gate2 grading coefficient	-
V_{poffG2}	gate2 capacitance pinching voltage	V
S_{G2}	steepness of gate2 capacitance drop	V^2

where n represents the index of gate (n=1 for gate1, n=2 for gate2), CMOD is a capacitance model selector for optional disconnection of the equation (3.16) from the rest of the model, and V_{poffGn}, S_{Gn} are tuning parameters as described in Table 3.4. The approximate behavior of (3.16) for CMOD=1 is

for $V \leq -V_{\mathrm{poff}}$: $C_{\mathrm{multGn}} = 0$

for $V \in (-V_{\mathrm{poff}}, -V_{\mathrm{poff}} + 0.5\mathrm{V})$: $C_{\mathrm{multGn}} \in (0, 1)$

for $V \geq -V_{\mathrm{poff}} + 0.5\mathrm{V}$: $C_{\mathrm{multGn}} = 1.$

The final voltage dependent capacitances are then defined as

$$C_{\mathrm{DGn}} = \frac{C_{\mathrm{j0Gn}}}{\left(1 - \frac{V_{\mathrm{DGn}}}{V_{\mathrm{jGn}}}\right)^{M_{\mathrm{jGn}}}} \times \frac{A_{\mathrm{Gn}}}{2} \times C_{\mathrm{multGn}} \tag{3.17}$$

$$C_{\mathrm{SGn}} = \frac{C_{\mathrm{j0Gn}}}{\left(1 - \frac{V_{\mathrm{SGn}}}{V_{\mathrm{jGn}}}\right)^{M_{\mathrm{jGn}}}} \times \frac{A_{\mathrm{Gn}}}{2} \times C_{\mathrm{multGn}} \tag{3.18}$$

where A_{Gn} represents area of gate with index n.

3.4 Parasitic DC Model, Gate Current

The next phenomenon implemented in behavioral JFET model is the gate current caused by the impact ionization. Due to the high electric field electron-hole pairs are generated in the drift area which causes parasitic gate current. Based on the MOSFET equation for impact ionization implemented in BSIM4 model [62], a similar equation was introduced for the

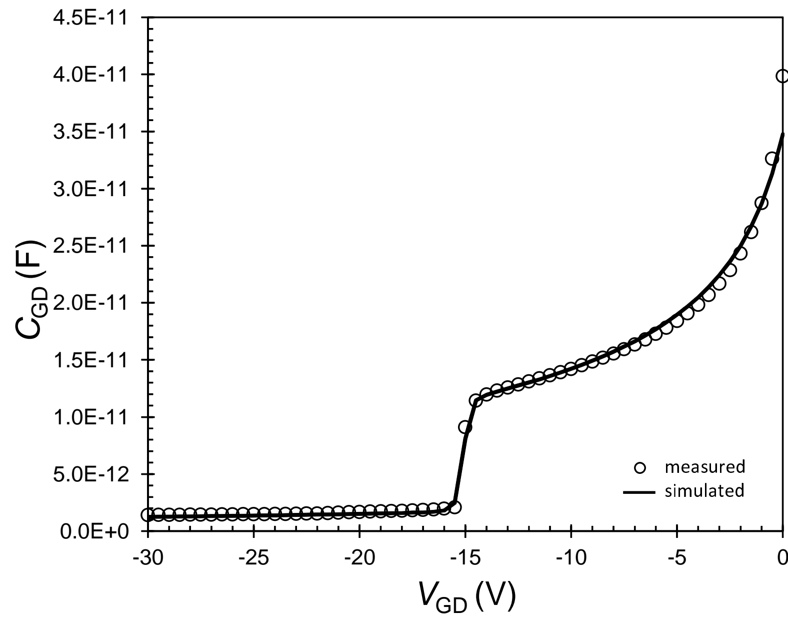

Figure 3.14: CV characteristic of JFET with full depletion at $V_{\mathrm{GD}} = -15$ V.

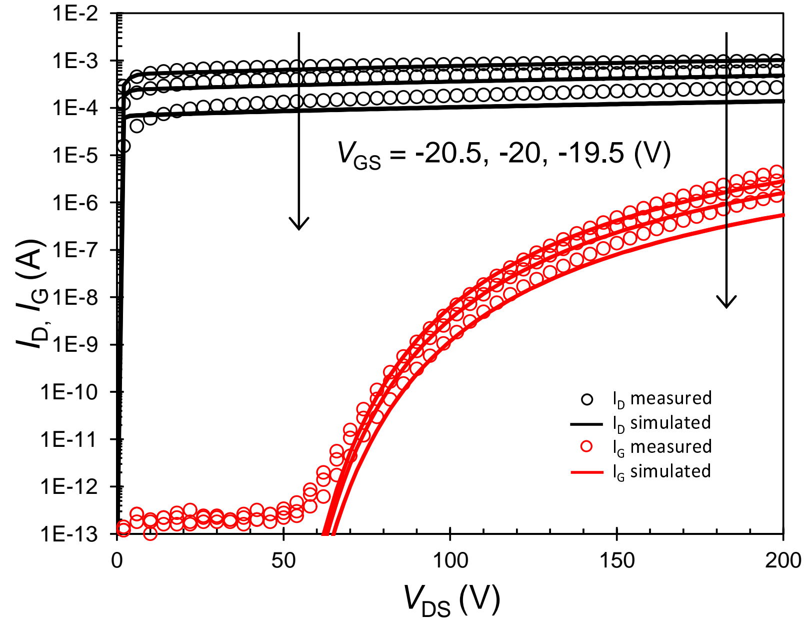

Figure 3.15: V_{D} dependency of gate1 current in dual-gate JFET for V_{G2}=V_{S}=0 V.

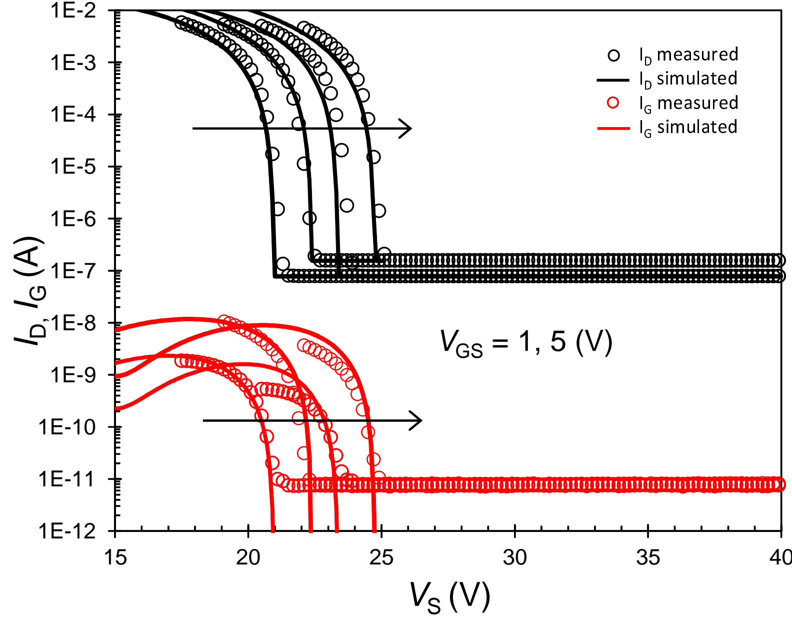

Figure 3.16: V_{S} dependency of gate1 current in dual-gate JFET for V_{D}=50 and 100 V, V_{G2}=0 V.

JFET and implemented as the gate current

$$I_{\mathrm{Gnii}} = \frac{\alpha_{\mathrm{0Gn}} + \alpha_{\mathrm{1Gn}} L_{\mathrm{eff}}}{L_{\mathrm{eff}}} V_{\mathrm{diffGn}} \cdot \exp\left(\frac{-\beta_{\mathrm{0Gn}}}{V_{\mathrm{diffGn}}}\right) I_{\mathrm{DS}} G_{\mathrm{shapeGn}} \tag{3.19}$$

where α_{0G}, α_{1G} and β_{0G} are tuning parameters described in Table 3.5, L_{eff} is effective JFET length, and I_{DS} is JFET current. Parameter V_{diff} represents the difference between drain-source voltage and effective drain-source voltage

$$V_{\mathrm{diffGn}} = V_{\mathrm{DS}} - V_{\mathrm{DSeffGn}} \tag{3.20}$$

where

$$V_{\mathrm{DSeffGn}} = (V_{\mathrm{pf0Gn}} - V_{\mathrm{DS}}) - 0.5\Big((V_{\mathrm{pf0Gn}} - V_{\mathrm{DS}}) + \sqrt{(V_{\mathrm{pf0Gn}} - V_{\mathrm{DS}})^2 + K}\Big) \tag{3.21}$$

V_{pf0Gn} is a tuning parameter representing the drain voltage where the impact ionization starts and coefficient K ensures a smooth course of the V_{DSeffG} dependency.

As can be derived from (3.21), the voltage V_{DSeffGn} approaches V_{DS} for $V_{\mathrm{DS}} < V_{\mathrm{pf0}}$ and V_{pf0Gn} for $V_{\mathrm{DS}} \geq V_{\mathrm{pf0Gn}}$. Hence, the parameter V_{diffGn} in (3.19) is roughly equal to zero for $V_{\mathrm{DS}} < V_{\mathrm{pf0Gn}}$ and the impact ionization

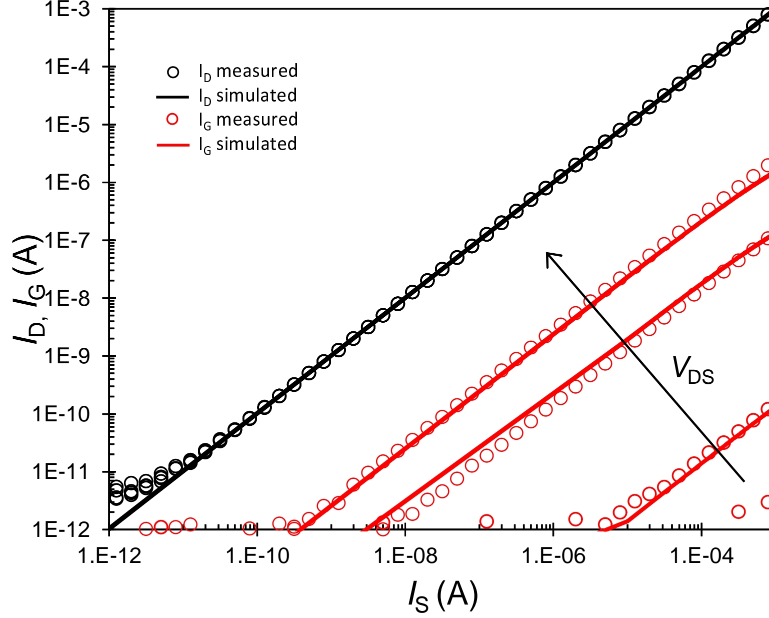

Figure 3.17: I_{S} dependency of gate1 current in dual-gate JFET for V_{D}=50, 100, 150 and 200 V, V_{G2}=0 V.

appears only for $V_{\mathrm{DS}} \geq V_{\mathrm{pf0Gn}}$. The impact of parameter V_{diffGn} is demonstrated in Fig. 3.15, which is $I_{\mathrm{D}}(V_{\mathrm{D}})$ characteristic measured/simulated up to the maximum voltage with gate current plotted.

The last parameter in (3.19) is G_{shapeGn}, representing the gate current dependency on gate voltage

$$G_{\mathrm{shapeGn}} = (V_{\mathrm{SGn}} - g_{\mathrm{2Gn}})^2 + g_{\mathrm{1Gn}} \tag{3.22}$$

where g_{1Gn} and g_{2Gn} are tuning parameters described in Table 3.5. The impact of gate voltage on gate current is demonstrated in Fig. 3.16. The scalability of impact ionization current is ensured in (3.19) by dependency on scalable drain-source current I_{DS}. The dependency of gate current on drain-source current in dual-gate JFET is demonstrated in Fig. 3.17.

For low V_{DS} where impact ionization is not active, the gate-drain and gate-source leakage currents are modeled by a standard diode equation [60]

$$I_{\mathrm{leakDGn}} = I_{\mathrm{SGn}} \left(\exp\left(\frac{V_{\mathrm{DGn}}}{n_e V_{\mathrm{t}}} \right) - 1 \right) \tag{3.23}$$

$$I_{\mathrm{leakSGn}} = I_{\mathrm{SGn}} \left(\exp\left(\frac{V_{\mathrm{SGn}}}{n_e V_{\mathrm{t}}} \right) - 1 \right) \tag{3.24}$$

where I_{SGn} is a tuning parameter described in Table 3.5, n_e is the emission coefficient and V_{t} is thermal voltage. Typically two diodes are used. The

Table 3.5: Impact ionization parameters for JFET (pinch resistor).

Parameter	Description	Unit
IGMOD	gate current model selector	-
α_{0G1}	First parameter of impact ionization gate1 current	μmV^{-1}
α_{1G1}	L-scale param. of impact ionization gate1 current	V^{-1}
β_{0G1}	Second parameter of impact ionization gate1 current	V^{-1}
V_{pf0G1}	V_{DS} offset of impact ionization gate1 current	V
I_{SG1}	Gate1 saturation (OFF state) current density	$A\mu m^{-2}$
g_{1G1}	First order voltage coef. of gate1 current	V^2
g_{2G1}	Second order voltage coef. of gate1 current	V
α_{0G2}	First parameter of impact ionization gate2 current	μmV^{-1}
α_{1G2}	L-scale param. of impact ionization gate2 current	V^{-1}
β_{0G2}	Second parameter of impact ionization gate2 current	V^{-1}
V_{pf0G2}	V_{DS} offset of impact ionization gate2 current	V
I_{SG2}	Gate2 saturation (OFF state) current density	$A\mu m^{-2}$
g_{1G2}	First order voltage coef. of gate2 current	V^2
g_{2G2}	Second order voltage coef. of gate2 current	V

first one between drain and gate, the second one between source and gate. Each of them represents the leakage current of one half of the p-n junction area. In the case of dual-gate JFET there are two p-n junctions, so there are four diodes used in the model. The total gate current is then defined as

$$I_{\mathrm{Gntot}} = \mathrm{IGMOD} \times I_{\mathrm{Gnii}} + (I_{\mathrm{leakDGn}} + I_{\mathrm{leakSGn}})A_{\mathrm{Gn}} \tag{3.25}$$

where A_{Gn} represents the area of p-n junction between JFET body and gate with index n, and IGMOD is gate current model selector for the optional disconnection of equation (3.19) from the model.

3.5 Temperature Model

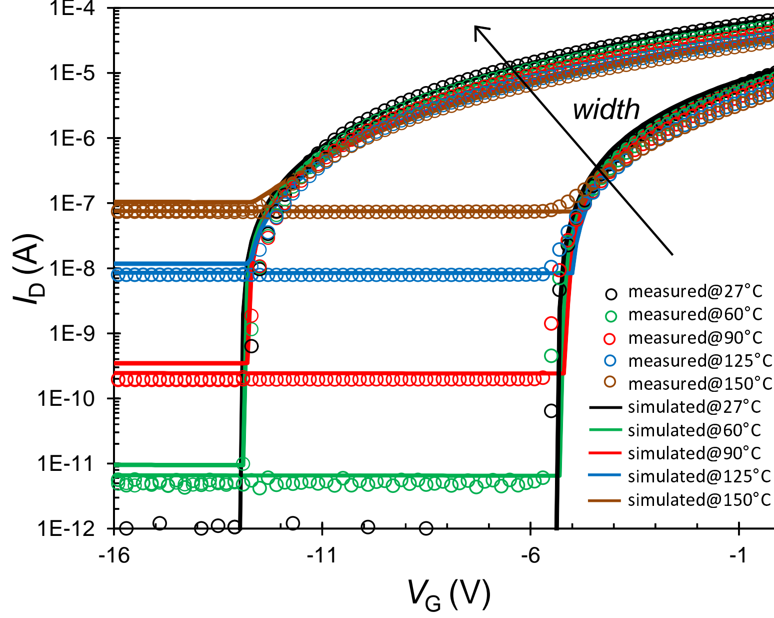

Figure 3.18: Pinch resistor I_D-V_G characteristics for $W=$ 6 and 16 μm at various temperatures.

Temperature dependency of the behavioral JFET model is more complex than in the case of compact JFET model. Three parameters controlling the temperature dependency of JFET were selected by the sensitivity analysis of temperature data: sheet resistance, pinch-off voltage and junction depth. Resulting temperature equations are

$$r_{\mathrm{ho}}(T) = r_{\mathrm{ho}} \left(\frac{T}{T_{\mathrm{nom}}} \right)^{\mathrm{texp}} \tag{3.26}$$

$$r_{\mathrm{sub}}(T) = r_{\mathrm{sub}} \left(1 + \mathrm{rsub}_{\mathrm{tc}} \left(T - T_{\mathrm{nom}}\right)\right) \tag{3.27}$$

$$x_j(T) = x_{\mathrm{j}} \left(\frac{T}{T_{\mathrm{nom}}} \right)^{\mathrm{xjtexp}} \tag{3.28}$$

where texp, $\mathrm{rsub}_{\mathrm{tc}}$ and xjtexp are tuning temperature parameters, described in Table 3.6.

Leakage current to gate is modeled by a standard equation [32, 60]

$$I_{\mathrm{SGn}}(T) = I_{\mathrm{SGn}} \left(\frac{T}{T_{\mathrm{nom}}} \right)^{\mathrm{xti}_{\mathrm{Gn}}} \tag{3.29}$$

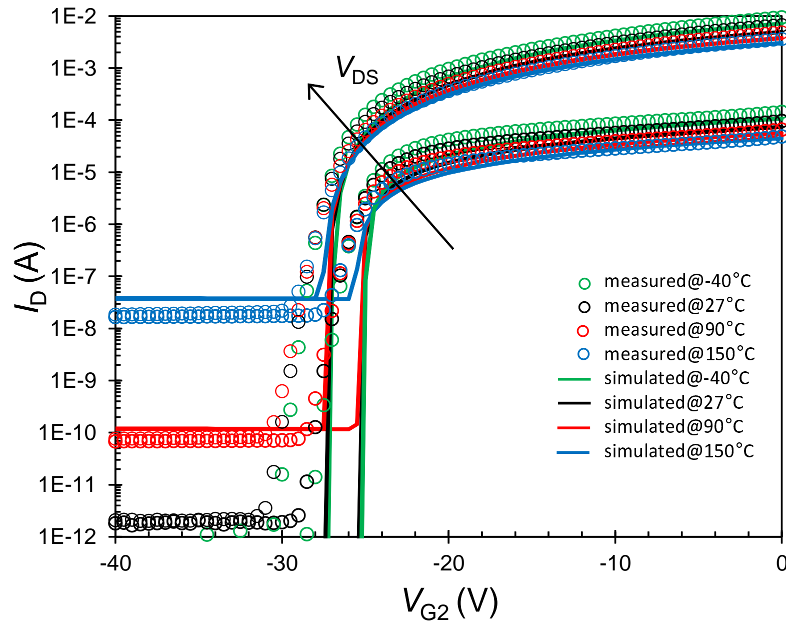

Figure 3.19: Dual-gate JFET I_D-V_{G2} characteristics for V_{G1S}=−22 V and V_{DS}=0.1 and 10 V at various temperatures.

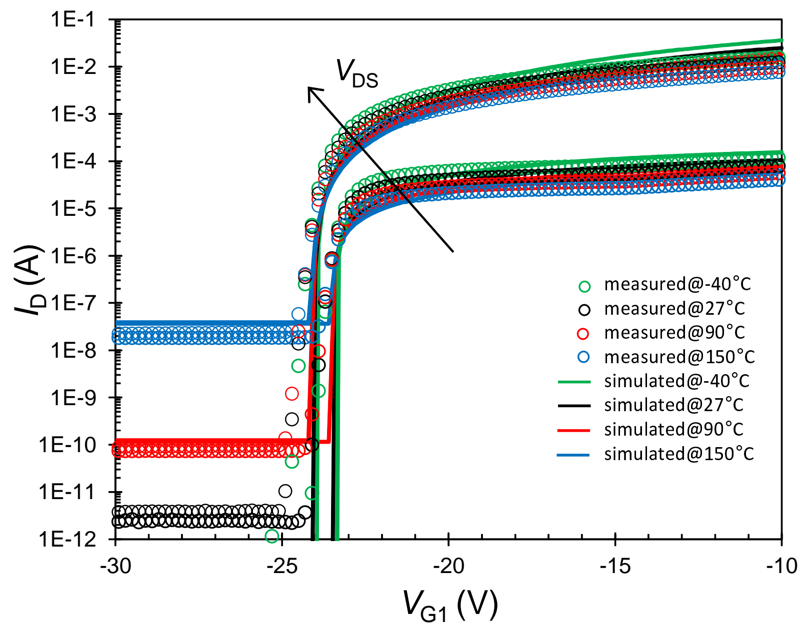

Figure 3.20: Dual-gate JFET I_D-V_{G1} characteristics for V_{G2S}=−20 V and V_{DS}=0.1 and 50 V at various temperatures.

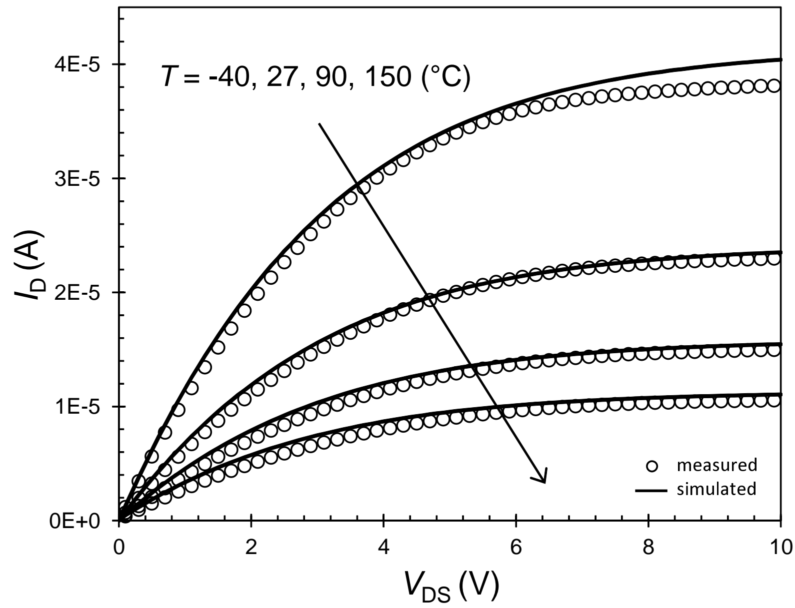

Figure 3.21: Pinch resistor I_D-V_D characteristic for V_{GS2}=−4 V at various temperatures.

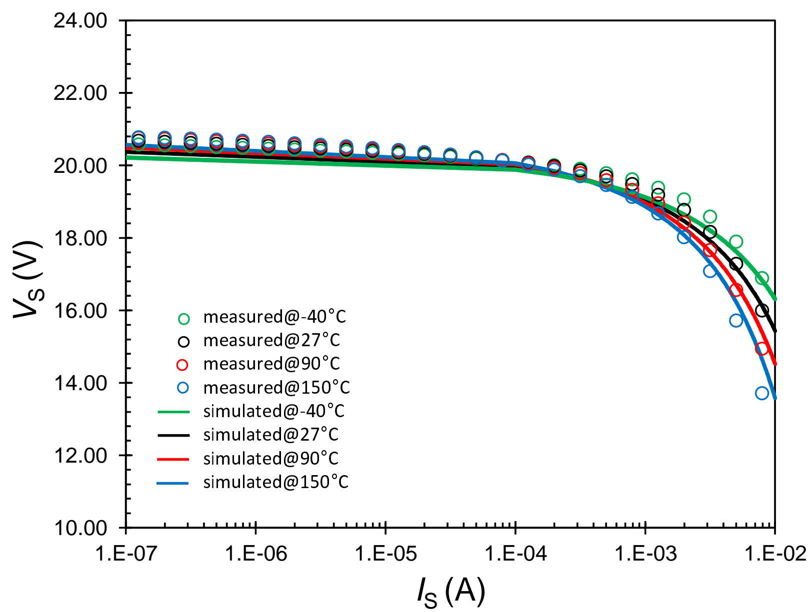

Figure 3.22: Dual-gate JFET load line V_{DS}=50 V at various temperatures. V_{G1}=V_{G2}=0 V.

Table 3.6: Temperature parameters for JFET (pinch resistor).

Param.	Description	Unit
texp	temperature exponent of JFET resistance	-
$\mathrm{rsub_{tc}}$	temperature coefficient of pinch-off voltage	K^{-1}
xjtexp	temp. exponent of JFET depth	-
$\mathrm{xti_{G1}}$	temp. exponent of gate1 OFF state current	-
$\mathrm{xti_{G2}}$	temp. exponent of gate2 OFF state current	-

where $\mathrm{xti_{Gn}}$ is tuning temperature parameter for gate with index n, described in Table 3.6. The temperature dependency of pinch-off and leakage current is demonstrated in Figs. 3.18 and 3.20. The temperature dependency of impact ionization current is covered by the temperature dependency of main JFET current I_{DS}, which plays an important role in the impact ionization equation (3.19).

3.6 Statistical Model

Each technology has some natural statistical distribution, which should be reflected in SPICE models. Several statistical tests, e.g., pinch-off voltage, R_{dson}, saturation current, etc., were defined and added to the PCM testplan to cover the electrical characteristics of the device. The tests were then measured in production lots and the final statistical data were used for the extraction of the statistical model. Four parameters controlling the process statistical distribution during Monte Carlo analysis were selected using sensitivity analysis of the measured statistical data: N_{body}, r_{ho}, ΔW, and I_{SGn}.

Parameters N_{body} and r_{ho} are distributed in the model with model parameter δr (relative shift) using following mapping equations [35]

$$N_{\mathrm{bodyFin}} = N_{\mathrm{body}}\Big(1 + \frac{\delta r_{\mathrm{Nbody_m}} + \mathrm{var}_1 \times \delta r_{\mathrm{Nbody_s}}}{100}\Big) \tag{3.30}$$

$$r_{\mathrm{hoFin}} = r_{\mathrm{ho}}\Big(1 + \frac{\delta r_{\mathrm{rho_m}} + \mathrm{var}_2 \times \delta r_{\mathrm{rho_s}}}{100}\Big) \tag{3.31}$$

where $\delta r_{\mathrm{Nbody_m}}$, $\delta r_{\mathrm{Nbody_s}}$, $\delta r_{\mathrm{rho_m}}$, and $\delta r_{\mathrm{rho_s}}$ are tuning parameters described in Table 3.7. The statistical distribution during Monte Carlo simulation is controlled by master variables var_1 and var_2 that vary randomly based on Gaussian distribution with $\mu = 0$ and $\sigma = 1$. This principle ensures that uncorrelated parameters vary independently, while correlated parameters vary simultaneously [36, 52].

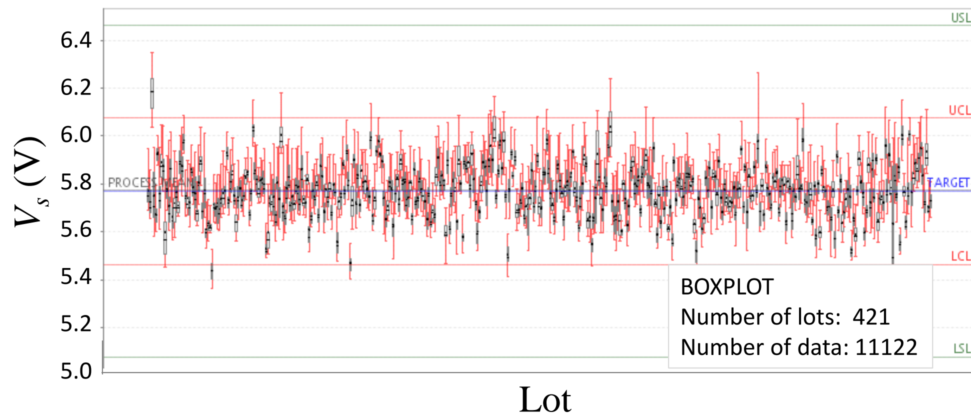

Figure 3.23: Boxplot of measured pinch-off voltage. Green lines define upper and lower specification limit (USL and LSL), red lines define upper and lower control limit (UCL and LCL).

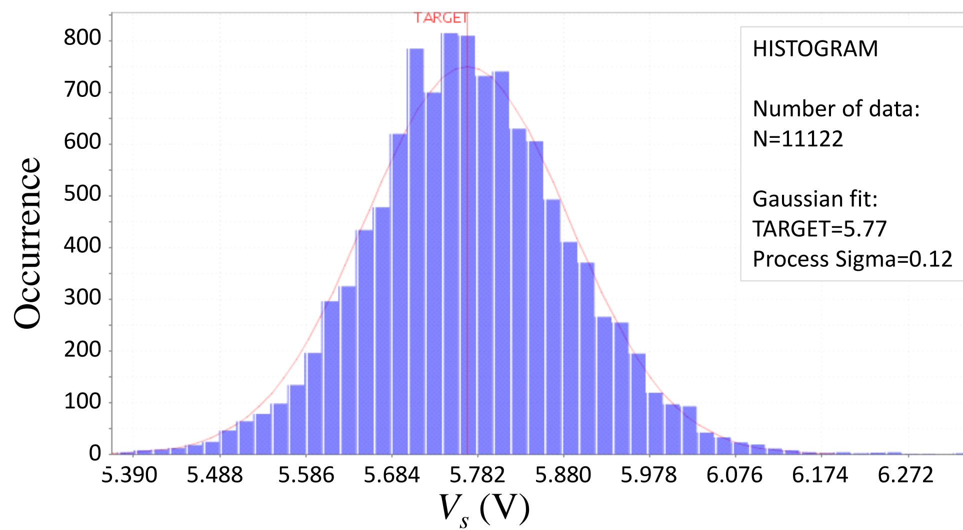

Figure 3.24: Histogram of measured and simulated pinch-off voltage. Red curve represents modeled Gaussian distribution.

Table 3.7: Statistical parameters for JFET (pinch resistor).

Parameter	Description	Unit
$\delta r_{\mathrm{Nbody_m}}$	Relative shift of parameter N_{body} - mean	%
$\delta r_{\mathrm{Nbody_s}}$	Relative shift of parameter N_{body} - sigma	%
$\delta r_{\mathrm{rho_m}}$	Relative shift of parameter r_{ho} - mean	%
$\delta r_{\mathrm{rho_s}}$	Relative shift of parameter r_{ho} - sigma	%
$\delta a_{\Delta \mathrm{w_m}}$	Absolute shift of parameter ΔW - mean	µm
$\delta a_{\Delta \mathrm{w_s}}$	Absolute shift of parameter ΔW - sigma	µm
$\delta r_{\mathrm{ISG1_m}}$	Relative shift of parameter I_{SG1} - mean	%
$\delta r_{\mathrm{ISG1_s}}$	Absolute shift of parameter I_{SG1} - sigma	-
$\delta r_{\mathrm{ISG2_m}}$	Relative shift of parameter I_{SG2} - mean	%
$\delta r_{\mathrm{ISG2_s}}$	Absolute shift of parameter $\log(I_{\mathrm{SG2}})$ - sigma	-

The parameter ΔW which can become positive or negative, is statistically modified by absolute shift δa as described in equation [35]

$$\Delta W_{\mathrm{Fin}} = \Delta W + (\delta a_{\Delta \mathrm{w_m}} + \mathrm{var}_3 \times \delta a_{\Delta \mathrm{w_s}}) \tag{3.32}$$

where $\delta a_{\Delta \mathrm{w_m}}$ and $\delta a_{\Delta \mathrm{w_s}}$ are tuning parameters described in Table 3.7. Monte Carlo simulation is in this case controlled by the parameter var_3.

The last statistically distributed model parameter is I_{SGn}. In this case the relative shift was applied again but using the log-normal distribution which is in agreement with measured statistical data:

$$I_{\mathrm{SGnFin}} = I_{\mathrm{SGn}} \left(1 + \frac{\delta r_{\mathrm{ISGn_m}}}{100}\right) \times 10^{\mathrm{var}_4 \times \delta r_{\mathrm{ISGn_s}}} \tag{3.33}$$

where $\delta r_{\mathrm{ISGn_m}}$ and $\delta r_{\mathrm{ISGn_s}}$ are tuning parameters described in Table 3.7. Monte Carlo simulation is here controled by the parameter var_4, and the exponential (3.33) performs conversion of Gaussian distribution of var_4 to log-normal distribution of I_{SGnFin}.

As an example, the histogram of measured and simulated pinch-off voltage (V_{S} at V_{D}=20 V and I_{S}=-1 nA) of pinch resistor W=7 and L=200 µm is depicted in Fig. 7.2. The boxplot in shown in Fig. 3.23. The number of

measured devices was 11122, the number of lots 421. The standard deviations of model parameters described in this section have been calculated from standard deviations of these measured electrical process parameters using Backward Propagation of Variances method (BPV) [36, 38].

Mismatch parameters have not been extracted yet. However, the model is open for the implementation of the mismatch parameters multiplicating (3.30) and (3.31) by multiplication factors [35]

$$\mathrm{MULT_{mm}} = \left(1 + \frac{\mathrm{var_{mm}} \times \sqrt{0.5} \times \frac{\sigma_{mm}}{\sqrt{WL}}}{100}\right) \tag{3.34}$$

where σ_{mm} is extracted mismatch standard deviation for given parameter and $\mathrm{var_{mm}}$ is master variable distributed by Monte Carlo simulation. The usage of master variable $\mathrm{var_{mm}}$ is the same as in the case of process distribution.

3.7 Extracted Model Parameters

The developed model was used for several real components, for example pinch resistors, high voltage JFETs or drift area of HV LDMOS. This chapter presents two of them: pinch resistor in 700V 1 μm analog CMOS technology and dual-gate 200V JFET in 700V 0.25 μm BCD technology.

Table 3.8: Extracted DC Parameters.

Parameter name	Parameter value Pinch resistor	Parameter value Dual-gate JFET	Unit
GMOD	1	0	-
N_{body}	1.38×10^{15}	1.20×10^{15}	$\mathrm{cm^{-3}}$
N_{side}	9.64×10^{14}	1.20×10^{15}	$\mathrm{cm^{-3}}$
N_{tub}	6.11×10^{14}	5.91×10^{14}	$\mathrm{cm^{-3}}$
x_{j}	1.03	0.53	μm
λ	2.00×10^{-3}	0	$\mathrm{V^{-1}}$
r_{ho}	3.00×10^{-1}	2.29×10^{-3}	$\Omega\mu\mathrm{m^{-2}}$
Δ_{L}	1.14	0	μm
Δ_{W}	-0.05	0	μm
r_{subb}	0	1.76×10^{-3}	$\mathrm{V^{-1}}$
r_{subd}	0	6.32×10^{-3}	-
r_{sub0}	2.53×10^{-1}	3.97×10^{-1}	-
r_{sub1}	3.19×10^{-2}	0	$\mathrm{m^{-1}}$
r_{sub2}	-1.66×10^{-3}	0	$\mathrm{m^{-2}}$
r_{sub3}	2.35×10^{-5}	0	$\mathrm{m^{-3}}$

Table 3.9: Extracted CV Parameters.

Parameter name	Parameter value Pinch resistor	Parameter value Dual-gate JFET	Unit
CMOD	0	1	V^{-1}
C_{j0G1}	2.14×10^{-17}	1.05×10^{-14}	$F\mu m^{-2}$
V_{jG1}	5.00	8.38	V
M_{jG1}	0.25	1.00	-
V_{poffG1}	30.0	15.6	V
S_{G1}	0.05	0.05	V^2
C_{j0G2}	0	1.50×10^{-17}	$F\mu m^{-2}$
V_{jG2}	0	0.06	V
M_{jG2}	0	0.25	-
V_{poffG2}	0	45.0	V
S_{G2}	0	0.05	V^2

Table 3.10: Extracted Parasitic Gate Current Parameters.

Parameter name	Parameter value Pinch resistor	Parameter value Dual-gate JFET	Unit
IGMOD	0	1	-
α_{0G1}	0	1.74×10^{-8}	μmV^{-1}
α_{1G1}	0	0	V^{-1}
β_{0G1}	0	582.3	V^{-1}
V_{pf0G1}	0	23	V
g_{1G1}	0	15	V^2
g_{2G1}	0	9	V
I_{SG1}	3.17×10^{-18}	2.50×10^{-16}	$A\mu m^{-2}$
α_{0G2}	0	1.74×10^{-8}	μmV^{-1}
α_{1G2}	0	0	V^{-1}
β_{0G2}	0	582.3	V^{-1}
V_{pf0G2}	0	23	V
g_{1G2}	0	15	V^2
g_{2G2}	0	9	V
I_{sG2}	0	1.50×10^{-17}	$A\mu m^{-2}$

The parameters of the models were extracted using standard modeling extraction flow. The measurement methods were defined, tested and used for various device dimensions and configurations. Various DC, CV and parasitic DC measurements were realized at temperatures from -40 to 150 °C. Parameters of both presented devices shown in Tables 3.8, 3.9, 3.10, 3.11, 3.12 were extracted using various optimization methods [13]. The models were implemented into the commercial simulators HSpice (Synopsys),

Table 3.11: Extracted Temperature Parameters.

Parameter name	Parameter value Pinch resistor	Parameter value Dual-gate JFET	Unit
texp	1.64	1.50	-
$rsub_{tc}$	0	0	K^{-1}
xjtexp	0	3.50×10^{-2}	-
xti_{G1}	1.84	3.0	-
xti_{G2}	0	3.0	-

Table 3.12: Extracted Statistical Parameters.

Parameter name	Parameter value Pinch resistor	Parameter value Dual-gate JFET	Unit
δr_{Nbody_m}	14.0	0.0	%
δr_{Nbody_s}	3.07	6.09	%
δr_{rho_m}	4.92	0.0	%
δr_{rho_s}	1.66	0.0	%
$\delta a_{\Delta w_m}$	0.037	0.0	µm
$\delta a_{\Delta w_s}$	0.149	0.0	µm
δr_{ISG1_m}	0.0	0.0	%
δr_{ISG1_s}	0.10	0.07	-
δr_{ISG2_m}	0.0	0.0	%
δr_{ISG2_s}	0.10	0.07	-

Eldo (Mentor) and Spectre (Cadence). Statistical model parameters were extracted based on evaluation of real production data using the Backward Propagation of Variances method (BPV) [36, 38].

3.8 Conclusion

This chapter represents the core of the developed new dual-gate JFET model, including genesis of the model development.

The developed behavioral Verilog-A model model is very complex, which is demonstrated by the simulated characteristics compared with measured data in various regimes of the device operation: DC currents, capacitance, parasitic gate currents, temperature sweep or statistical distribution.

The list of extracted model parameters for two representatives dual-gate high voltage JFET and pinch resistor have been presented.

Dual-gate JFET compact model does not exist in any commercial simulator yet. The presented model is therefore the only solution for the simulation of technology containing such device. Moreover, most JFET models published before the publication of this [61, 57, 58] [35] have been focused on DC parameters. The presented model proposes a more complete and universal solution covering most of required phenomena for real production designs.

The new ideas described in this chapter were approximately 85% author's own. The author's ratio of participation in the relevant publication [5] was about 40%.

The following chapters deal with the extension of this model.

CHAPTER 4

Techniques of HV JFET Gate Capacitance Modeling

4.1 Introduction

The Junction Field Effect Transistor (JFET) is a component used in many applications, as for example low-noise amplifier, high input impedance amplifier, constant current source, etc. [10]. It can be constructed as 3-terminal (3T) or 4-terminal (4T) component. The more complicated 4T JFET contains two independently controlling gates, which allow two input signals to be applied simultaneously, so it can be used in signal mixing applications [61].

Development of JFETs especially for high-voltage applications requires considering various aspects, as for example optimization of breakdown voltage with series resistance, ESD robustness, etc. Therefore, various JFET concepts can be found. Apart from that, the JFET can be found as a parasitic structure in other components as for example in high-voltage PMOS, which can be observed in measured characteristics and should be considered in macromodel.

This chapter published in [4] is focused on the modeling of JFET gate capacitance, which is seemingly only a simple p-n junction, but in reality the measured C-V characteristics can at first look quite surprising. Various JFET concepts and measured gate capacitances including explained physical interpretation of observed phenomena are presented. Modeling techniques (lumped model, behavioral model, etc.) are compared and plots with silicon data vs. simulated results are demonstrated.

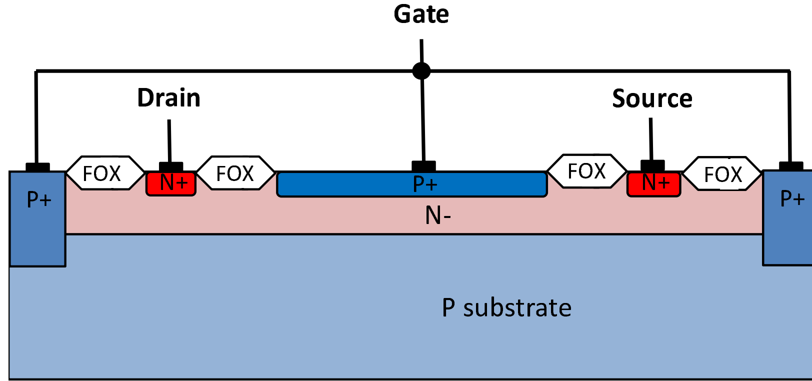

Figure 4.1: Cross-section of single-gate JFET (pinch resistor).

4.2 Single-gate (three-terminal) JFET

The example of single-gate JFET cross-section is shown in Fig. 4.1, the related layout is in Fig. 4.2 and the typical macromodel is in Fig. 4.3. Such component is often called the pinch resistor and it is often used as a constant current source.

Voltage dependent capacitances C_{GD} and C_{GS} are usually represented by the compact diode SPICE models with the voltage dependent p-n junction barrier capacitance described by the equation [32, 60]

$$C = \frac{C_{\mathrm{j0}}}{\left(1 - \frac{V}{V_{\mathrm{j}}}\right)^{M_{\mathrm{j}}}} \mathrm{AREA} \tag{4.1}$$

where C_{j0} is the zero-bias junction capacitance per unit area, V_{j} is junction built-in potential, M_{j} is grading coefficient, and AREA is the area of pn junction (representing the half of JFET gate area).

These compact diode SPICE models can be either part of customized lumped macromodel or integrated in the JFET model as for example in R3 model [35].

It is apparent, that low doped substrate and high doped P+ gate are connected in our three-terminal JFET, so the question is, how to measure and evaluate model parameters of C_{GD} and C_{GS} for the equation 4.1. The equation assumes a physical p-n junction with depletion area spreading with the applied p-n junction voltage, not two parallel p-n junctions affecting each other.

One of possible solutions is to measure the gate and substrate p-n junctions separately and implement two parallel diodes in the model instead of one. However, such solution does not correctly represent the real situation,

where the JFET channel can be pinched off by a few volts. The separate measurements in artificial structures do not cover this case.

It is more correct to measure the real situation of gate and substrate connected in a real JFET device. In such a case, however, the extracted parameters V_{j} and M_{j} can get quite far from their expected physical values, which especially occurs at low temperatures. In compact models the parameter V_{j} has the integrated temperature dependency [32]

$$V_J(T) = V_J(T_{\mathrm{nom}}) \left(\frac{T}{T_{\mathrm{nom}}} \right) + 2V_t \ln \left(\frac{n_i(T_{\mathrm{nom}})}{n_i(T)} \right) \tag{4.2}$$

where T is simulation temperature, T_{nom} is nominal reference temperature at which the values of basic model parameters were extracted, V_t is the thermal voltage and n_i is the intrinsic carrier concentration of used material, in our case silicon, with its own temperature dependency [32]

$$n_i(T) = n_i(T_{\mathrm{nom}}) \left(\frac{T}{T_{\mathrm{nom}}} \right)^{X_{\mathrm{ti}}} \exp \left(\frac{q}{2k} \left(\frac{\mathrm{E_G(T_{nom})}}{T_{\mathrm{nom}}} - \frac{\mathrm{E_G(T)}}{T} \right) \right) \tag{4.3}$$

where X_{ti} is intrinsic carrier concentration temperature exponent used in SPICE as a tunable temperature parameter, typically set to the value 1.5, and E_G is the gap width with its own temperature dependency described in [42].

Therefore, if the extracted V_{J} value gets too far from its expected physical value, it can become too low at very low temperatures, and making V/V_{j} too dominant, in extreme case even larger than 1, which could cause negative capacitance. The extracted parameters should thus be carefully verified in the full temperature range. If the verification fails and obtaining precise

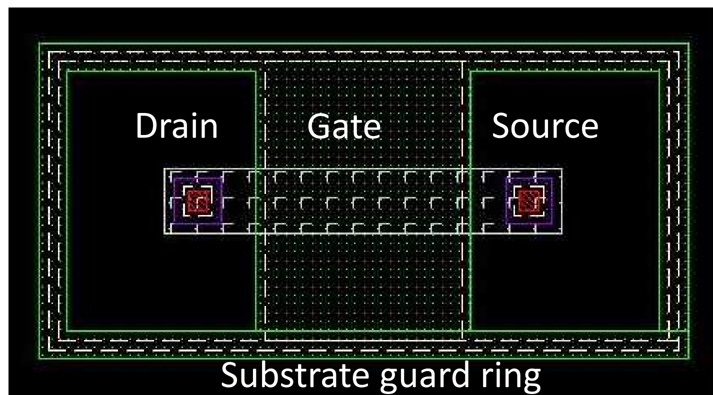

Figure 4.2: Layout of single-gate JFET (pinch resistor).

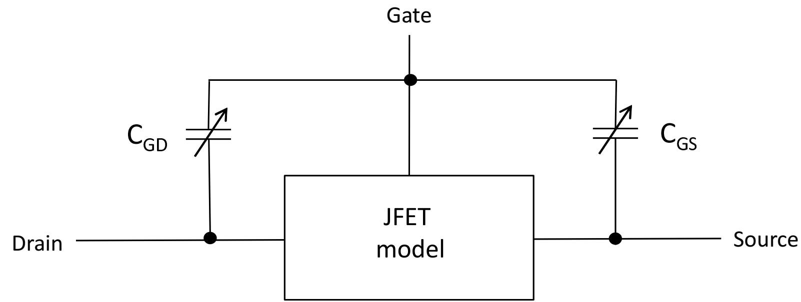

Figure 4.3: Simplified C-V macromodel of single-gate JFET (pinch resistor).

voltage dependent capacitance with the integrated model equation 4.1 becomes impossible, the alternative solution of behavioral voltage dependent capacitor model can be used.

In any case it is necessary to measure the gate capacitance in the real three-terminal structures containing drain, source and gate terminals, and not (as is often practised) in large two-terminal customized p-n junction structures. If the JFET is too small and gate capacitance value is under tester measurement limit (sometimes called measurement noise floor), more JFETs in parallel can be used instead. Correct measurement of gate-drain capacitance C_{GD} is with floating source, correct measurement of gate-source

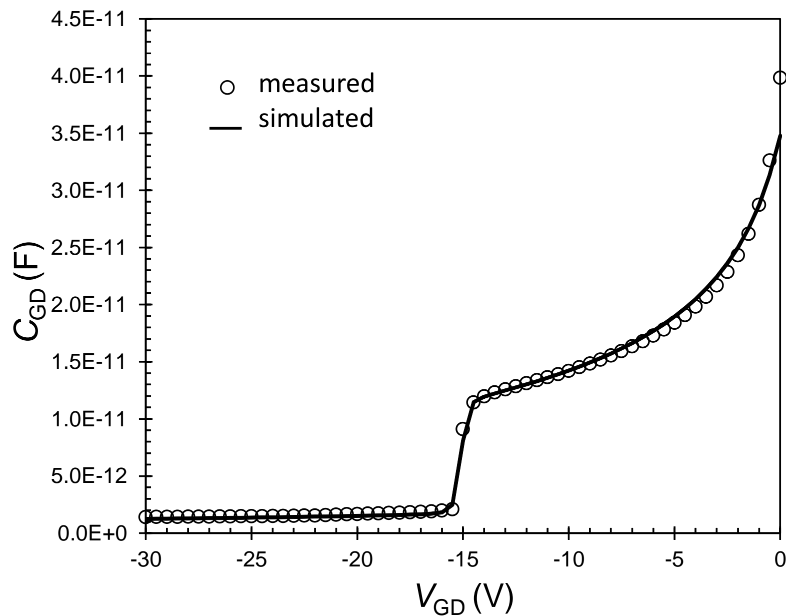

Figure 4.4: C_{GD}-V characteristic of single-gate JFET with full depletion at $V_{\mathrm{GD}} = -15$ V.

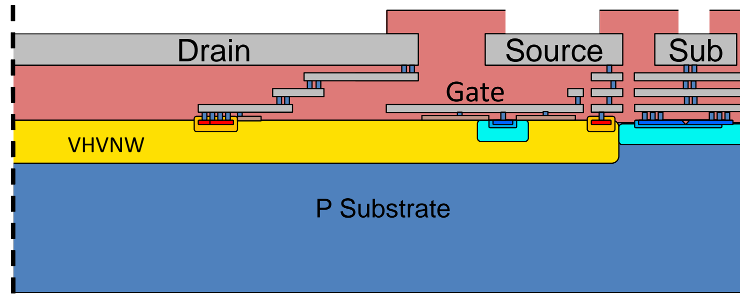

Figure 4.5: Cross-section of high-voltage dual-gate 4T JFET.

capacitance C_{GS} is with floating drain.

Let us for simplicity only talk about measurement of gate-drain capacitance C_{GD} in the following text. In such a case the measured gate-drain capacitance C_{GD} is equal to the sum of two parallel capacitances: gate-drain capacitance (direct p-n junction) and gate-source capacitance in series with the source-drain resistance, which is basically a JFET represented by its DC model. When the gate-drain voltage V_{GD} voltage across the p-n junction reaches the JFET pinch-off voltage, the JFET body becomes fully depleted, and the mentioned second parallel path containing gate-source capacitance C_{GS} is disconnected. This appears as a steep drop of capacitance in measured C-V characteristic, as demonstrated in Fig. 4.4. Measurement of the gate capacitance with shorted drain and source does not show this effect. The same effect was observed also in gate capacitances of MESFET/pHEMT or microwave varactors [12].

4.3 Dual-gate (four-terminal) JFET

An example of dual-gate JFET cross-section is shown in Fig. 4.5, the related layout is in Fig. 4.6 and the typical macromodel is in Fig. 4.7. This component is designed for high-voltage applications, therefore it has a circular or oval shape with the high voltage pad in the center, as illustrated in Fig. 4.6. This configuration ensures that the high voltage applied to the drain appears only in vertical direction in the center of the oval where the high breakdown voltage is ensured by low concentration of carriers in the substrate. Sufficient drift length or other techniques (e.g. double RESURF [27]) make sure that this high voltage does not appear in the device's perimeter and the device can operate at such high voltages [5]. Examples of the dual-gate JFET applications can be found in [31].

In the case of dual-gate JFET there are two effective gates (gate and substrate) represented by two p-n junctions, so there are four voltage de-

pendent capacitors in the macromodel, as depicted in Fig. 4.7. Therefore, four C-V tests must be measured: Gate-drain capacitance C_{GD} with floating source, substrate-drain capacitance C_{SUBD} with floating source, gate-source capacitance C_{GS} with floating drain and substrate-source capacitance C_{SUBS} with floating drain. The principle is analogous with that described in previous section for single gate JFET, but in this case the measurement of gate capacitances has substrate voltage as a parameter and the measurement of substrate capacitances has gate voltage as a parameter.

The measured characteristics as well as the simulated curves are presented in Fig. 4.8 and Fig. 4.9. Fig. 4.8 shows gate-drain capacitance C_{GD} measured for various substrate voltages. It is apparent, that the substrate voltage is affecting the pinch-off voltage V_{GD}, because the pinch-off voltage of dual-gate JFET is affected by depletion areas of both gates. The more dominant gate is the one with higher concentration of carriers, because the diffusion of minor carriers to the JFET body is higher in this case. This can be demonstrated by the comparison of Fig. 4.8 and Fig. 4.9, where the same step of second parameter has different impacts: the gate charge is apparently more concentrated and therefore the gate voltage V_G in Fig. 4.9 has a higher impact on the pinch-off voltage than the substrate voltage V_{SUB} does in Fig. 4.8. As mentioned in previous section, a well-fitting DC model (especially for pinch-off voltage) is a necessity for the correct precise low-signal capacitance model. For the dual-gate JFET it is even more challenging, because the pinch-off voltage is determined by a combination of both gate voltages V_G and V_{SUB} and each of them has a different impact. Various

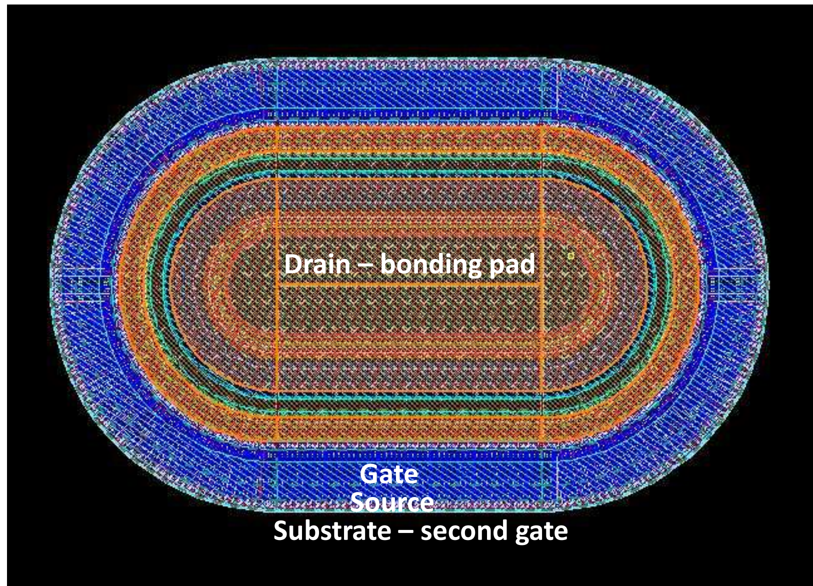

Figure 4.6: Layout of high-voltage dual-gate 4T JFET.

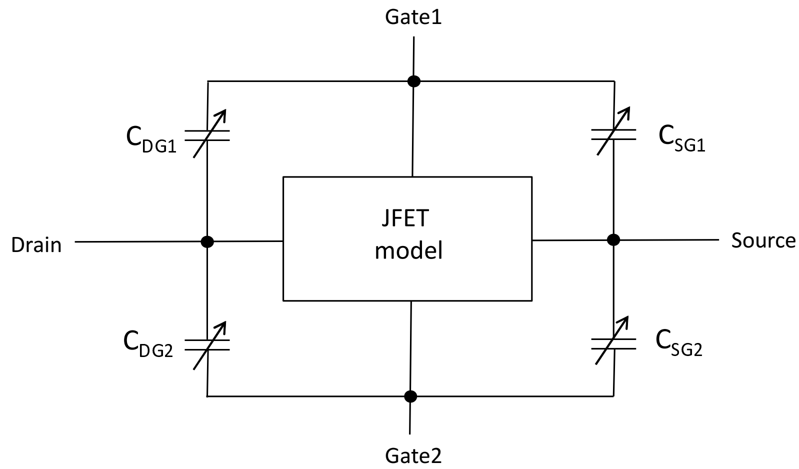

Figure 4.7: Simplified C-V macromodel of dual-gate 4T JFET.

behavioral DC models of dual-gate JFET are published for example in [61] or in [5].

The next challenge for the dual-gate JFET gate capacitance modeling is the device with a non-uniform JFET channel. Fig. 4.5 shows a JFET with gate covering only a smaller part of JFET channel. In such a case the

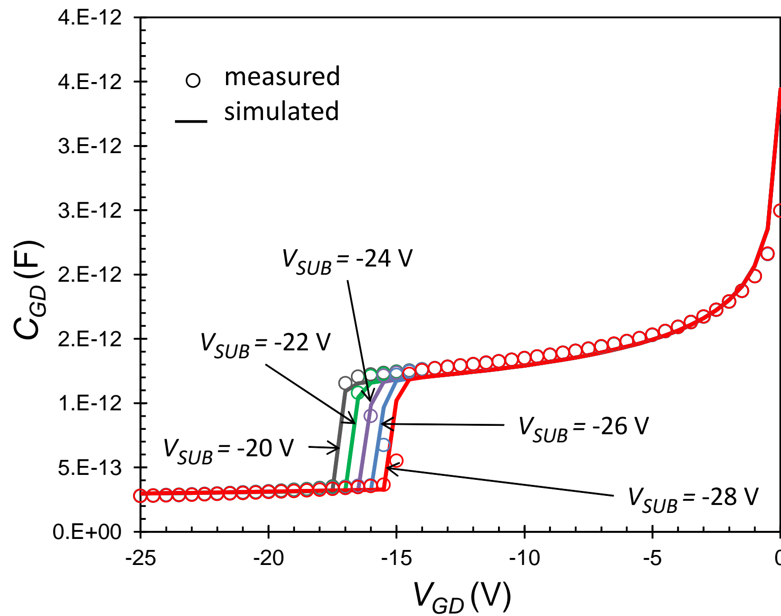

Figure 4.8: C_{GD}-V characteristic of high-voltage dual-gate JFET with parametrized $V_{\mathrm{SUB}} = -20, -22, -24, -26, -28$ V.

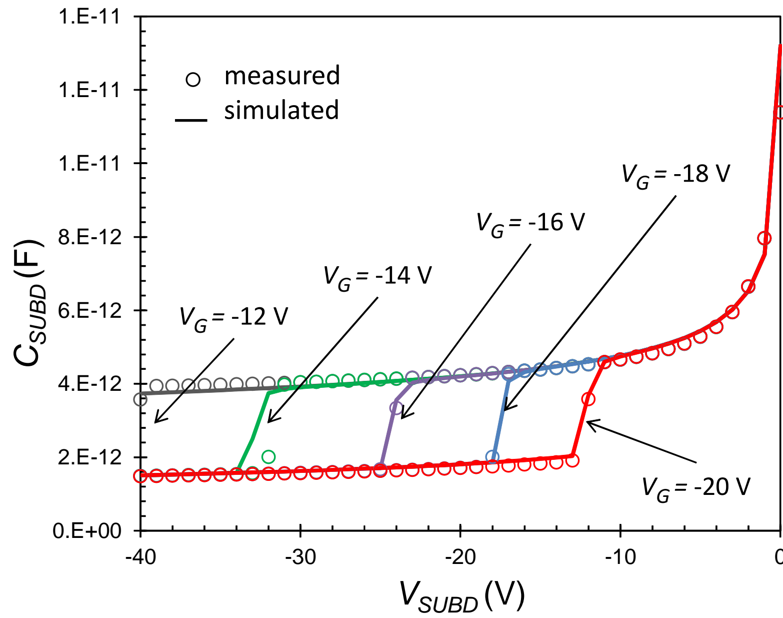

Figure 4.9: C_{SUBD} - V_{SUBD} characteristic of high-voltage dual-gate JFET with parametrized $V_{\mathrm{G}} = -12, -14, -16, -18, -20$ V.

gate-drain capacitance is in reality a p-n junction capacitance in series with a very-high-voltage Nwell (VHVNW) layer not covered by the gate. Ideal modeling solution would be the macromodel of dual-gate JFET in series with single gate JFET and the gate-drain capacitance would rather be the capacitance between gate and internal node between the two mentioned JFETs. Such a solution directly corresponds with the layout, but it is overly complicated and difficult for the parameter extraction mainly due to impossibility to measure these two segments separately. Moreover this solution is predisposed to convergence issues.

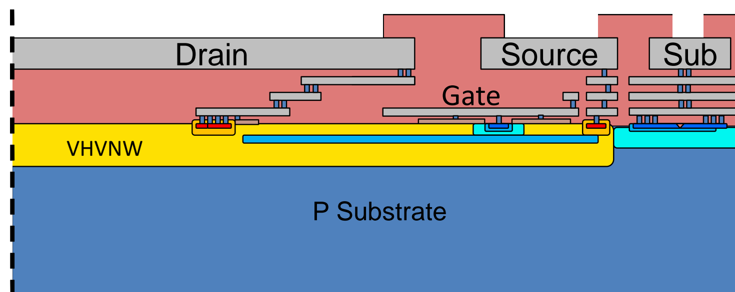

Figure 4.10: Cross-section of high-voltage dual-gate 4T JFET with parasitic surfact channel.

Another possible modeling solution is using the standard barrier capacitance of equation 4.1, but unfortunately with a high probability of the extracted parameters far from their physical values and thus the temperature model failing, as explained in section A. So the verification in full temperature range is again necessary.

The last proposed modeling solution is using the customized behavioral voltage dependent capacitance. It is preferred to model the capacitance with a charge controlled model as recommended in [40].

4.4 Dual-gate (four-terminal) JFET with parasitic surface channel

A high-voltage JFET does not necessarily have to have non-uniform channel. Fig. 4.10 demonstrates JFET described in the previous section, in this case with the additional buried-layer gate covering almost whole of the JFET channel. However, this construction has another challenge, consisting in the parasitic JFET channel between silicon surface and buried gate.

In such case the gate-drain capacitance is predominantly located in the parasitic JFET channel between the surface and buried layer, while the majority of current flows via the main channel under buried layer. Measurement of such gate-drain capacitance with substrate voltage as a parameter and floating source is shown in Fig. 4.11. Unlike in the previous tests, in this case the gate was grounded while the drain voltage being swept on. Therefore, $-V_{\mathrm{DG}}$ instead of V_{GD} is on X-axis. This information is important only for correct understanding of parameter V_{SUB}. Measured is the gate-drain capacitance C_{GD} like in previous tests.

At low gate-drain voltages the measured capacitance is composed of the surface gate-drain capacitance, the main channel gate-drain capacitance and the gate-source capacitance in series with JFET. At about $V_{\mathrm{GD}} = 15V$ the parasitic surface channel becomes depleted and the surface gate-drain capacitance becomes disconnected. Because it was the dominant one, the measured capacitance significantly drops down. In the range of gate-drain voltage between about 15V and 20V the main channel gate-drain capacitance and the gate-source capacitance in series with JFET are significant. And finally at $V_{\mathrm{GD}} > 20V$ the main JFET channel gets fully pinched, with the pinch-off voltage affected by the applied substrate voltage, as detailed Fig. 4.12. This effect was explained in previous section. In other words, the substrate voltage affects only the second capacitance drop at $V_{\mathrm{GD}} > 20V$, while the rest of the C-V curve is substrate-voltage independent.

The modeling of the second capacitance drop is covered naturally by the combination of precise DC model of dual-gate JFET [61, 5] and four related

voltage dependent capacitances (compact diode SPICE models). The modeling of the first dominant capacitance drop can be done by two possible methods.

The first one was demonstrated in [5]. The gate-drain surface channel capacitor is modeled by a behavioral voltage-dependent capacitor using equation 4.1 multiplied with the dimensionless multiplication factor C_{mult}

$$C_{\mathrm{mult}} = \left(\sqrt{(V_{\mathrm{GD}} + V_{\mathrm{poff}})^2 + S} + 0.5\mathrm{V} - \sqrt{(V_{\mathrm{GD}} + V_{\mathrm{poff}} - 0.5\mathrm{V})^2 + S} \right) \times \mathrm{CMOD} \quad (4.4)$$

where $V_{\mathrm{GD}} = -V_{\mathrm{DG}}$ is the gate-to-drain voltage, V_{poff} is the absolute value of gate capacitance pinch-off voltage and S controls the steepness of the gate capacitance drop and CMOD is a capacitance model selector for optional disconnection of the equation (4.4) from the rest of the model.
The approximate behavior of (4.4) for CMOD = 1 is

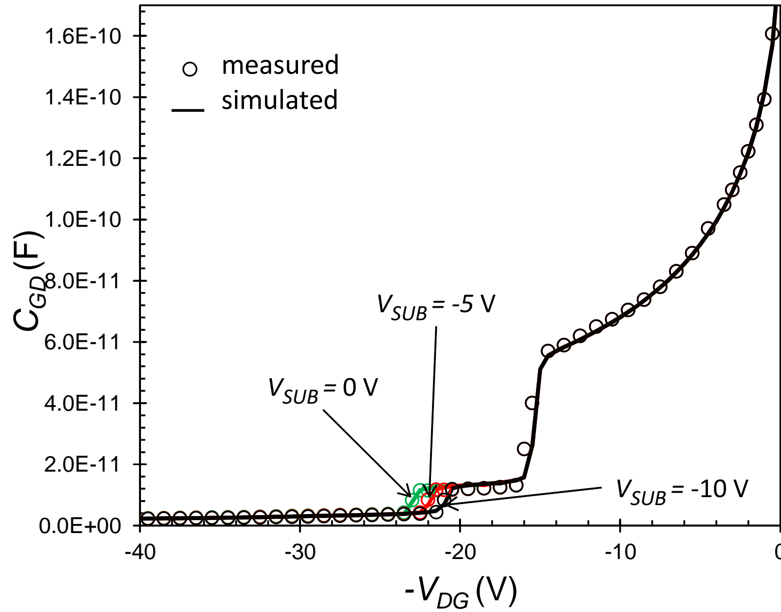

Figure 4.11: C_{GD}-V_{GD} characteristic of high-voltage dual-gate JFET with parasitic surface channel and parametrized $V_{\mathrm{SUB}} = 0, -5, -10$ V affecting the pinching of main JFET channel.

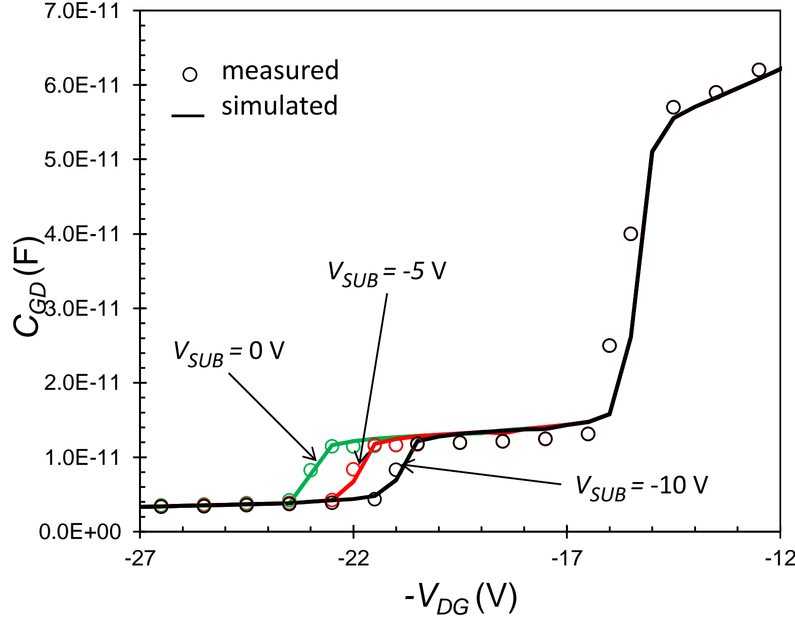

Figure 4.12: C_{GD}-V_{GD} characteristic of high-voltage dual-gate JFET with parasitic surface channel and parametrized $V_{\mathrm{SUB}} = 0$, -5, -10 V, focused on disconnection of ”source path” due to pinched main JFET channel.

for $V_{\mathrm{GD}} \leq -V_{\mathrm{poff}}$: $C_{\mathrm{mult}} = 0$
for $V_{\mathrm{GD}} \in (-V_{\mathrm{poff}}, -V_{\mathrm{poff}} + 0.5\mathrm{V})$: $C_{\mathrm{mult}} \in (0, 1)$
for $V_{\mathrm{GD}} \geq -V_{\mathrm{poff}} + 0.5\mathrm{V}$: $C_{\mathrm{mult}} = 1$.
The voltage-dependent gate-drain capacitance is then defined as

$$C_{\mathrm{GD}} = C_{\mathrm{mult}} \frac{C_{\mathrm{j0}}}{\left(1 - \frac{V_{\mathrm{GD}}}{V_{\mathrm{j}}}\right)^{M_{\mathrm{j}}}} AREA \tag{4.5}$$

This solution, however, brings a risk of convergence errors in transient analysis, as mentioned in [40], where the charge-controlled model is recommended. Another possible solution is to implement the surface parasitic JFET channel in the macromodel as a JFET DC model and put it in series with the substrate gate-drain capacitor. The disadvantage of this is the increase of model complexity. However, it is close to the actual layout, which is usually a good solution.

4.5 Parasitic JFET in other components

As mentioned earlier, the JFET device, especially for high side applications, can be structured in different ways which should be taken into account dur-

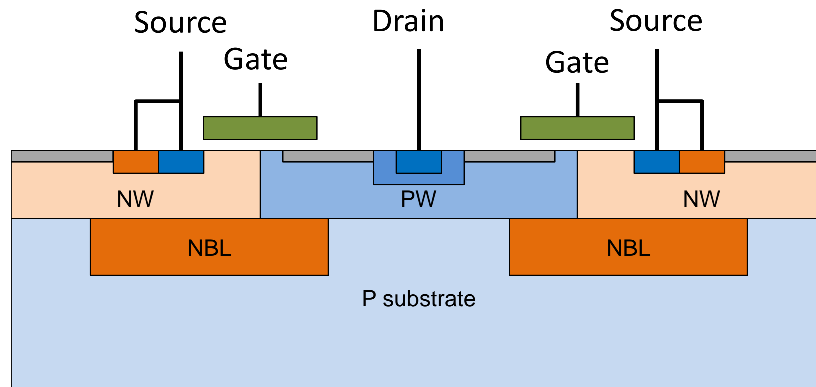

Figure 4.13: Cross-section of high-voltage PMOS with parasitic drain JFET (p-type). N-body shorted to P-source represents JFET gate (n-type).

ing model development. Previous sections demonstrated only some examples of possible JFET types.

In Fig. 4.13 the cross-section of another component, in this case high voltage PMOS, is shown, where the drain-source capacitance is affected by the parasitic JFET created by the P-substrate channel and two N buried layers (NBL) representing JFET gate. This PMOS has its bulk shorted with the source, so the measured output drain-source capacitance for negative V_{DS} might be expected to be the simple barrier capacitance with voltage dependency described by the equation 4.1. But the data shows a similar capacitance drop as in Fig. 4.4, which is caused by the pinching of the mentioned parasitic JFET. In this case the drain-source capacitance must be modeled, similarly as the surface parasitic channel described in previous section, either by behavioral voltage dependent capacitance or by the implementation of parasitic JFET in the lumped macromodel.

Similar parasitic JFETs can appear also in other component types, as for example bipolar transistors, diodes, etc. So a careful measurement using the right measurement setup and considering these phenomena in the final model are necessary to obtain an accurate model representing the real electrical behavior of the device.

4.6 Conclusion

JFET gate capacitance is often considered to be just a simple p-n junction. Its measurement and careful modeling is therefore often underestimated. This capacitance is however usually affected by the pinching JFET effect, which must be taken into account. It was demonstrated, that JFET can appear also as a parasitic component in other electrical components and

must be also considered in the macromodel. Various examples were presented and for each of them various techniques and principles of modeling gate capacitance were proposed. Some plots with measured silicon data and simulated models were demonstrated.

Such complex guide as presented in this chapter, taking into account various device variants, was not found in any other publication or SPICE manual.

The new ideas described in this chapter were approximately 90% author's own. The author's ratio of participation in the relevant publication [4] was about 50%.

CHAPTER 5

Lumped RF Model of MOSFET Gate Resistance for GHz+ Frequencies

5.1 Introduction

Nowadays the design of competitive integrated circuits requires short cycle time and first pass success in manufacturing. This is assured by precise SPICE models. The commercial simulators contain many compact models, e.g. BSIM [62], HiSIM [34] or PSP [19] for MOSFETs, Gummel-Poon [51] or VBIC [8] for bipolar transistors, containing set of tunable parameters. However, the high voltage and high frequency area is not yet fully covered by compact models. Therefore the macromodels built from the combination of compact model with the parasitic RLC network or behavioral HDL blocks must be created.

This chapter published in [2] is focused on the modeling of fast high voltage MOSFET used as an output stage, operating in frequencies in order of GHz and voltages up to V_{DS}=30V and V_{GS}=8V. Due to the very large gate width in the order of meters the MOSFET has very low ON state resistance R_{dson} and due to the construction it has very low output capacitance. The typical R_{dson} is in order of milliohms, gate-drain capacitance is in order of picofarads and gate source capacitance in order of nanofarads. Although the total gate width is very large, in order of meters, the device total area is relatively small, in order of square millimeters, due to the high integration (see layout in Fig. 5.1 and Fig. 5.1).

Such a device of course contains many parasitic phenomena not observed in standard MOSFETs. Namely the gate impedance including the imaginary part has to be considered. Especially the inductance part because the

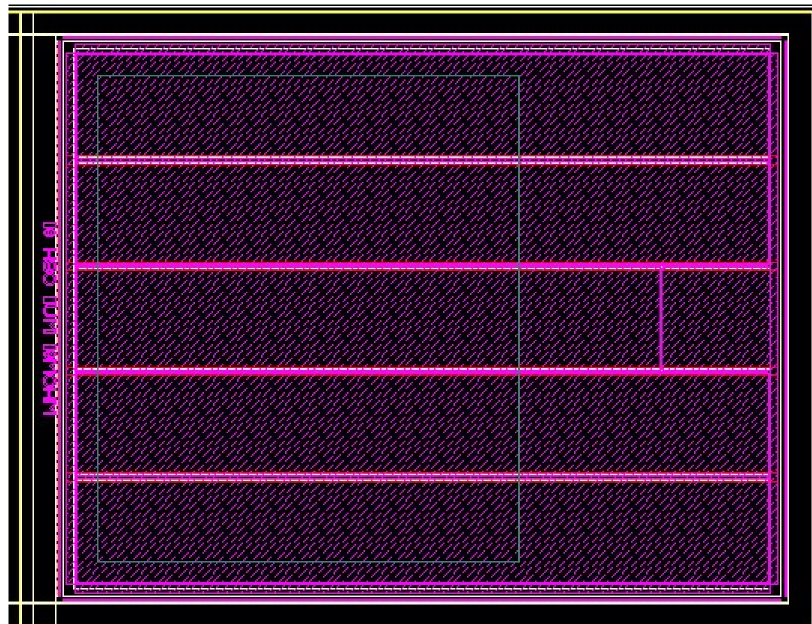

Figure 5.1: Layout of characterized high voltage MOSFET with area 3 mm^2.

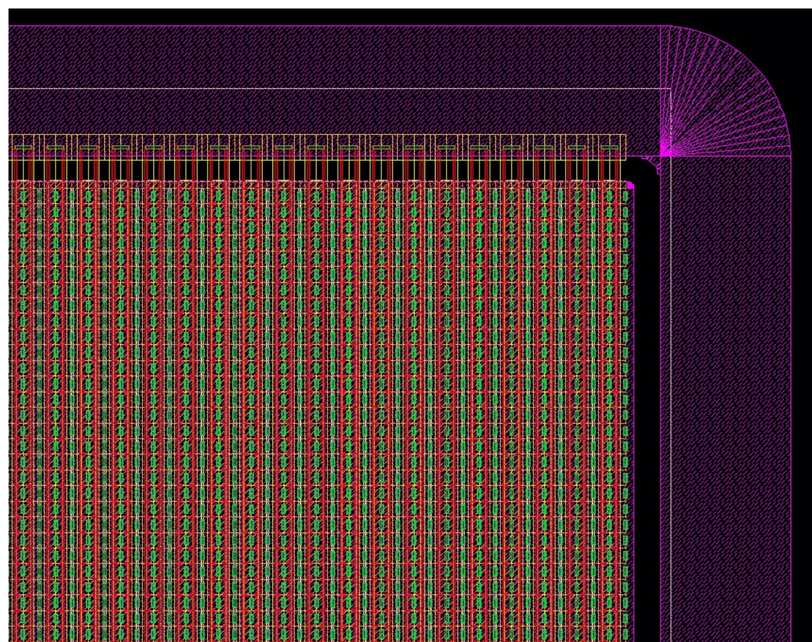

Figure 5.2: Layout of characterized high voltage MOSFET - detail 50×50 µm^2.

density of gate connections is in our case quite large as demonstrated in Fig. 5.1.

The compact BSIM4 [62] model was used for the modeling of basic MOSFET. Although this model contains gate resistance parameters, the measured data were too different from the expected characteristics. So it was decided to use RLC network instead.

5.2 Model development

The scalable model was created based on the standard SPICE modeling methodology [32, 21, 60]. The test-mask containing required device in several configurations, namely various gate width, number of rows, and number of columns was designed. The device was measured in full operation area up to maximal voltages and in full temperature range (from –40°C to +150°C). The test plan contained DC methods $I_{\mathrm{D}}(V_{\mathrm{D}})$ and $I_{\mathrm{D}}(V_{\mathrm{G}})$, capacitance methods $C_{\mathrm{GD}}(V_{\mathrm{GD}})$ and $C_{\mathrm{GS}}(V_{\mathrm{GS}})$, and Transmission Line Pulse (TLP) tests for the measurement of high currents to prevent self-heating. The measured data were then used for the extraction of BSIM4 MOSFET model parameters.

Finally, the frequency measurement of S-parameters using Ground-Signal structure demonstrated in Fig. 5.3 and network analyzer Agilent 8753 operating up to frequency 2 GHz was performed. As it can be seen in Fig. 5.3, the MOSFET has grounded drain and source, so the measured Z_{12} impedance corresponds to the MOSFET in series with gate resistance. The measured S-parameters were transformed to Z parameters using standard transfer functions.

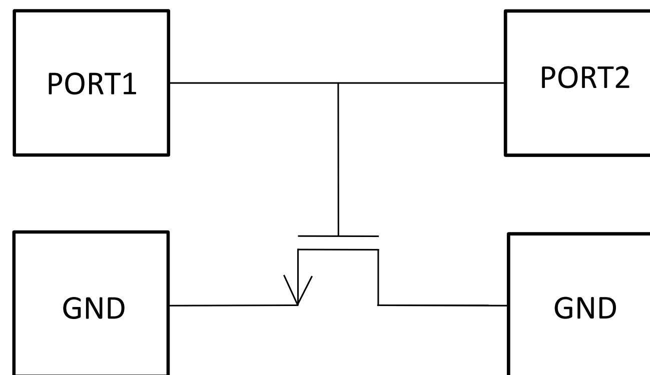

Figure 5.3: Ground-Signal two-port structure for S-parameters measurement.

The most of compact MOSFET models contain only parasitic capacitance and do not calculate with parasitic gate impedance. The measured DUT then can be simplified to the gate resistance in series with the parallel combination of gate-drain and gate source capacitances. Such a model is very simple and the Z_{12} impedance can be expressed by the simple equation

$$Z = R + \frac{1}{j\omega C} \tag{5.1}$$

where R corresponds to gate resistance and C corresponds to parallel combination of gate-drain and gate-source capacitances. Bulk is here shorted to the source, so the gate-bulk capacitance is here considered as a part of gate source capacitance. However, such a model was in our case insufficient, as demonstrated in Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7. Blue line represents the simulation with the standard compact MOSFET BSIM4 model, circles represent measured data.

The BSIM4 MOSFET model contains set of RF parameters for the gate resistance modeling [62] but they represent just parallel combination of gate resistance and capacitance. This is sufficient for standard CMOS but not for our power device with strong influence of parasitic inductance. Therefore the implementation of BSIM4 RF model made simulation results even worse, as it is depicted in Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7, plotted with green line.

Therefore it was decided to use the external RLC network demonstrated in Fig. 5.8. Except gate-drain and gate-source capacitors which are part of the compact BSIM4 model, all other components are modeled by separate resistor and inductor compact models. The parameters of external RLC networks were extracted from several dimensions of MOSFETs measured in Ground-Signal structure demonstrated in Fig. 5.3. The simulated results are demonstrated in Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7, purple line.

Although the agreement with measured results is in this case much more promising than in previous two cases, there are still discrepancies. Especially in frequency range of MHz the strong non-idealities visible mainly in real part of impedance can be observed. Peaks in about 200 MHz are probably caused by the resonance of RLC network created by high density of gate connectors that behave in high frequencies like inductors.

5.3 Final results

It was discussed that for the precise modeling of such complex characteristics the large device area and the signal delay should be considered. The signal comes faster to the periphery parts of the device than to the central parts which should be considered by the model. The idea of the model is demon-

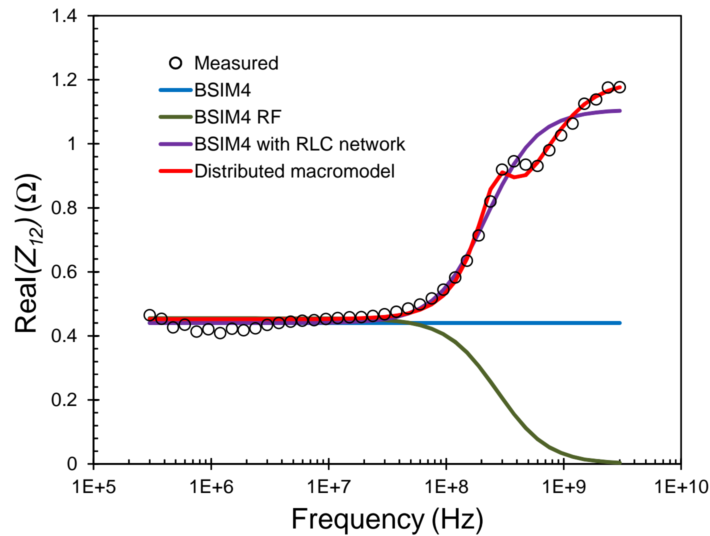

Figure 5.4: Real part of Z_{12} impedance, comparison of simulated results with measured data.

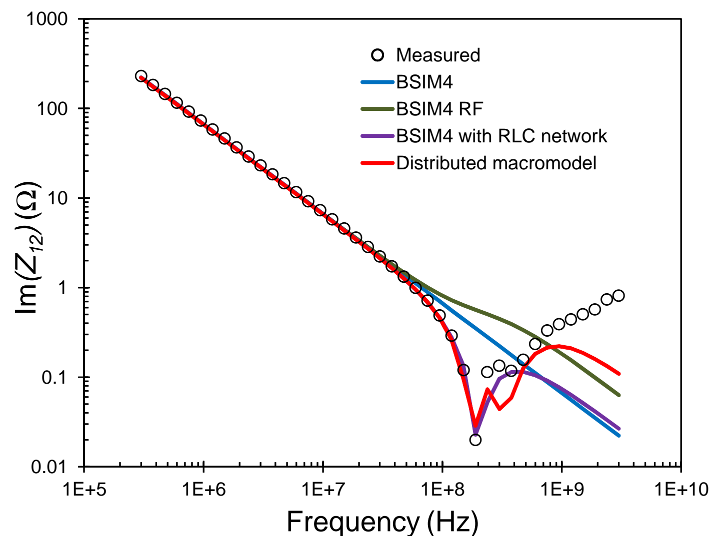

Figure 5.5: Imaginar part of Z_{12} impedance, comparison of simulated results with measured data.

strated in Fig. 5.9: to split the device to three parts, central area, middle area and peripheral area, where the signal comes to the central area longer than to the peripheral area. The RLC network representing the gate signal path to the central area must contain larger R, L and C values than the RLC network representing the gate signal path to the peripheral area. The final macromodel created by three parallel MOSFETs where each represents one

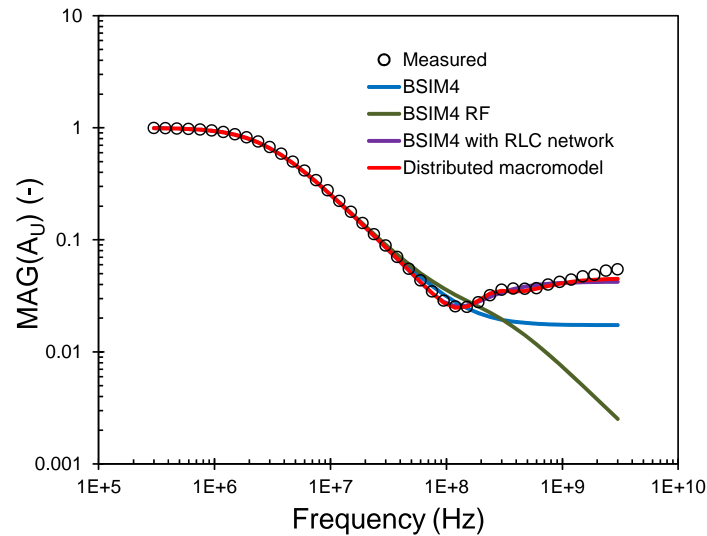

Figure 5.6: Magnitude of transfer function, comparison of simulated results with measured data.

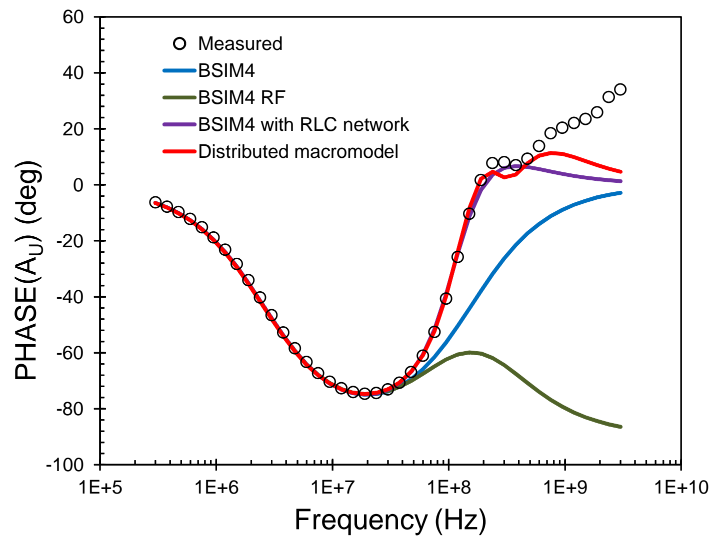

Figure 5.7: Phase of transfer function, comparison of simulated results with measured data.

third of gate width is depicted in Fig. 5.10. Three RLC networks are then connected in such a way, that the signal coming to the MOSFET representing central area goes through three RLC networks, the signal coming to the MOSFET representing the middle area goes through two RLC networks, and finally the signal coming to the MOSFET representing peripheral area goes through one RLC network. This distribution assures more realistic

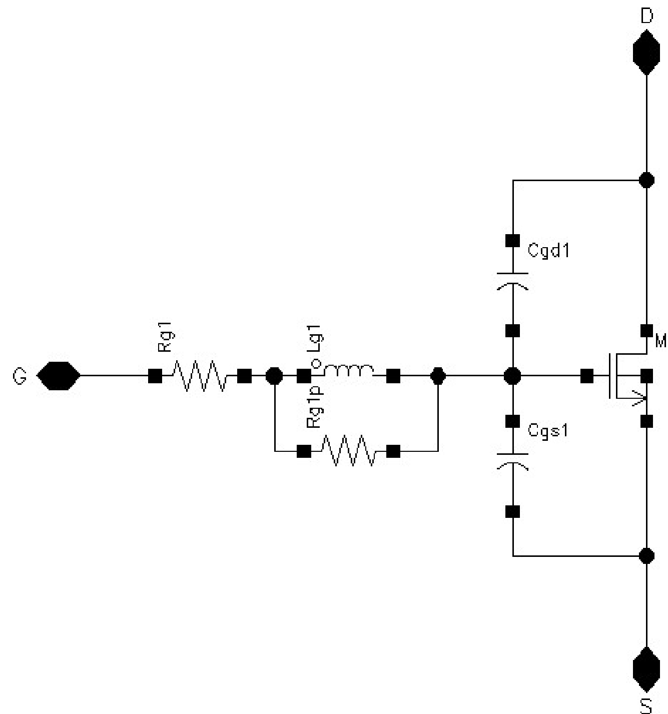

Figure 5.8: Macromodel – first prototype.

signal delay. And finally, the right extraction of RLC values of these three segments covers above mentioned resonance effect in MHz range.

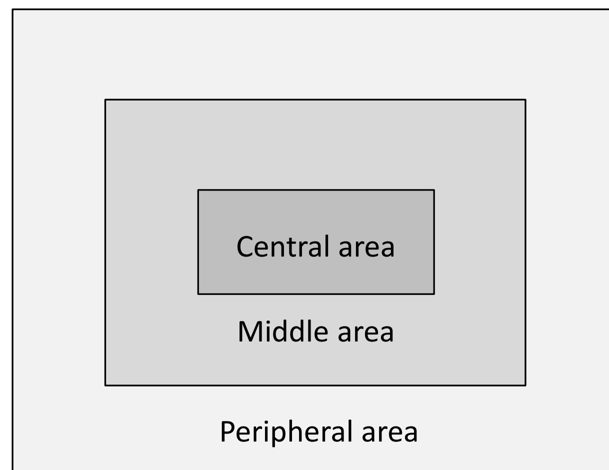

Figure 5.9: MOSFET Layout segmentation for the modeling of signal delay.

The various dimensions of the device were used for the RLC network parameter extraction to cover the scalability of the device, especially the

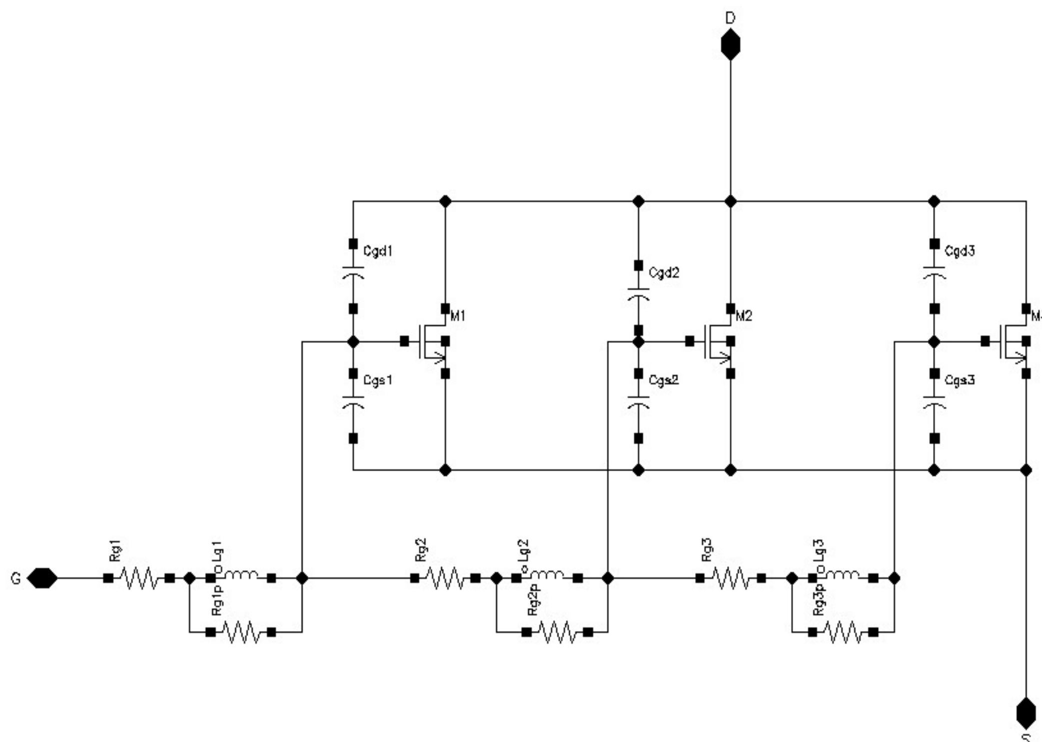

Figure 5.10: Macromodel – final solution.

dependency on the input parameters, which are gate width of the segment, number of segments in line, number of segments in columns - see Fig. 5.2. Moreover, the dependency on the gate pad position and editable width of metal gate was implemented. Final model vs data plots are demonstrated in Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7, red line vs circle data points. The agreement with measured data is in this case very good.

5.4 Conclusion

This chapter deals with the enhanced accurate RF model of high voltage power MOSFET for GHz frequency range. The modeling results were compared with measured data and with other concepts of models. The model was validated in full temperature range and operation range. It is fully scalable and valid even for very large dimensions. It was proved that the model has smooth derivatives of all simulated characteristics and therefore has very good convergence and simulation speed. The model can be used in standard commercial simulators, which was verified in Eldo, Spectre and HSpice.

The main contribution of this chapter is the implementation of parasitic RLC network to the polysilicon gate including the inductance segments. RF models of various SPICE MOSET compact models contain usually the RC network modeling parasitic polysicion gate resistance, the impact of parasitic inductance is however largely missed.

The new ideas described in this chapter were approximately 80% author's own. The author's ratio of participation in the relevant publication [2] was about 50%.

CHAPTER 6

Accurate Diode Behavioral Model with Reverse Recovery

6.1 Introduction

This chapter published in [6] demonstrates comprehensive behavioral model of p-n junction directly applicable to all common SPICE simulators supporting Verilog-A [16, 49]. The model can be used as a stand-alone model or as a part of more complicated macromodel, as for example dual-gate JFET presented in this thesis.

The chapter deals with the basic equations, used solutions and test methods for the parameter extraction in time and frequency domains and it is organized into several sections:

- Section Model development deals with the basic concept of the model. The reverse recovery principles [25] merged with the basic diode equations were implemented into Verilog-A language and the compact model functional in all SPICE simulators supporting Verilog-A was created.
- Section Model validation demonstrates comparison of the simulated results using the extracted behavioral model with the data measured in time and frequency domains.
- Section Model parameter extraction shows the extracted model parameters and compares the values with the standard SPICE compact model of the diode.
- Section Comparison with SPICE compact models containing reverse recovery effect compares the presented model with the recently published HiSIM model.

6.2 Model development

6.2.1 Basic equations of compact SPICE diode model

This section deals with the set of well known basic diode equations, used as a ground for the behavioral model development. The goal of this section is not to describe full set of compact diode SPICE model equations and parameters, which can be found in each SPICE manual.

The total diode current in standard SPICE compact diode model is described as [32, 60]

$$i = I_{\mathrm{pn}} + \frac{dQ_{\mathrm{inj}}}{dt} + \frac{dQ_{\mathrm{j}}}{dt} \tag{6.1}$$

where I_{pn} is the large signal current defined for $V > 0\mathrm{V}$ as [32, 60]

$$I_{\mathrm{pn}}(V) = I_S \left(\exp\left(\frac{V}{nV_{\mathrm{t}}} \right) - 1 \right) \tag{6.2}$$

and for $V < 0\mathrm{V}$ as [32, 60]

$$I_{\mathrm{pn}}(V) = I_S \tag{6.3}$$

where I_S is saturation current, n is emission coefficient and V_{t} is thermal voltage. Except the thermal voltage all these parameters are used as tunable compact SPICE model parameters.

Q_{inj} in (6.1) is charge of injected carriers, dominant mainly with positive voltage applied to p-n junction ($V > 0\mathrm{V}$), defined as [32, 60]

$$Q_{\mathrm{inj}}(V) = T_T I_{\mathrm{pn}}(V) \tag{6.4}$$

where T_T is transit time used as a tunable compact SPICE model parameter. Derivative of this charge with respect to applied voltage is often denoted as the injection capacitance

$$C_{\mathrm{inj}}(V) = \frac{dQ_{\mathrm{inj}}}{dV} \tag{6.5}$$

Q_{j} in (6.1) is fixed charge of ionized dopant atoms, dominant mainly with negative voltage applied to p-n junction. This charge is stored in voltage dependent barrier or drift capacitance [32, 60, 21]

$$C_{\mathrm{j}}(V) = \frac{dQ_{\mathrm{j}}}{dV} = \frac{\mathrm{C_{J0}}}{(1 - \frac{V}{\mathrm{V_J}})^{\mathrm{M_J}}} \tag{6.6}$$

where $\mathrm{C_{J0}}$ is the zero-bias junction capacitance, $\mathrm{V_J}$ is junction potential and $\mathrm{M_J}$ is a grading coefficient, all used as tunable compact SPICE model parameters.

In fact, (6.6) is actually not implemented in the SPICE programs. Instead of (6.6) a charge-controlled formulation of the junction capacitance is implemented, which can be obtained by an integration of $\mathrm{d}Q_\mathrm{j} = C_\mathrm{j}\mathrm{d}V$:

$$\int_0^{Q_\mathrm{j}} \mathrm{d}Q'_\mathrm{j} = \int_0^{V} \frac{C_\mathrm{J0}}{\left(1 - \frac{V'}{V_\mathrm{J}}\right)^{\mathrm{M_J}}} \mathrm{d}V'. \tag{6.7}$$

For evaluating this integral equation, let us make a substitution

$$1 - \frac{V'}{V_\mathrm{J}} = x \Rightarrow \mathrm{d}V' = -V_\mathrm{J}\mathrm{d}x, \tag{6.8}$$

which gives the integral

$$Q_\mathrm{j} = -V_\mathrm{J} \int_1^{1-\frac{V}{V_\mathrm{J}}} \frac{C_\mathrm{J0}}{x^m} \mathrm{d}x, \tag{6.9}$$

to be solved, after that a final formula for the junction charge is obtained:

$$Q_\mathrm{j} = \frac{C_\mathrm{J0} V_\mathrm{J}}{1 - \mathrm{M_J}} \left[1 - \left(1 - \frac{V}{V_\mathrm{J}}\right)^{1-\mathrm{M_J}}\right]. \tag{6.10}$$

The formula (6.10) is actually implemented, and a current created by the junction capacitance is calculated in the standard way as $\dot{Q}_\mathrm{j}$.

Although the full set of diode model parameters contains a parameter called transit time, the T_T in (6.4) is not a real transit time. The transit time normally means an amount of time needed for carriers to travel at a finite velocity the distance from the middle of the diode to the external terminals. But SPICE model does not include such a concept, as it is clearly seen in (6.4). The stored injected charge Q_inj is an instantaneous function of the applied voltage.

6.2.2 Principle of reverse recovery behavioral model

Therefore, we were looking for a way to model the reverse recovery correctly. Several published lumped and behavioral models of reverse recovery were tested [25, 29, 28, 15, 48, 46], but the simulation results of many of them were not satisfying. Either convergence or accuracy issues were observed during simulation. Finally the concept published in [25] was chosen.

The total diode current is there defined as

$$i = I_\mathrm{inj} + I_\mathrm{j} = \frac{dQ_\mathrm{inj}}{dt} + \frac{dQ_\mathrm{j}}{dt} \tag{6.11}$$

where I_inj is injection current defined as time derivative of the charge of injected carriers Q_inj and I_j is junction current defined as time derivative of the fixed charge of ionized dopant atoms Q_j.

Injection current I_{inj} is then in [25] expressed as

$$I_{\mathrm{inj}} = \frac{Q_{\mathrm{e}} - Q_{\mathrm{m}}}{T_{\mathrm{M}}} \tag{6.12}$$

where T_{M} is diffusion transit time used as a tunable model parameter, Q_{e} is the charge of carriers injected to the p-n junction and Q_{m} is the charge of carriers injected away from the p-n junction. Charges Q_{e} and Q_{m} are modeled by following equations [25]

$$Q_{\mathrm{e}} = \tau I_S \exp\left(\frac{V}{nV_{\mathrm{t}}} - 1\right) \tag{6.13}$$

$$Q_{\mathrm{m}} = \tau I_{\mathrm{inj}} - \frac{d(\tau Q_{\mathrm{m}})}{dt} \tag{6.14}$$

where τ representing minority carrier lifetime is used as a tunable model parameter.

The injection capacitance from equation (6.5) can then be expressed as [25]

$$C_{\mathrm{inj}} = \frac{d(Q_{\mathrm{e}} - Q_{\mathrm{m}})}{dV} \tag{6.15}$$

The description of fixed charge of ionized dopant atoms Q_{j} as well as the drift capacitance C_{j} provided by (6.6) remain unchanged in the modified model.

6.2.3 Realization of model development

The reverse recovery model published in [25] has been developed in language MAST for Saber simulator, not compatible with SPICE simulators used, like Eldo, Spectre or HSpice. So it was necessary to translate the model to more universal HDL language Verilog-A [16, 49] applicable to most of standard SPICE simulators. However, the quite complex dependence between (6.12) and (6.14) demonstrated in Fig. 6.1 was found very difficult for the simulation and convergence in Verilog-A.

The first approach of dealing with this challenge was to use current controlled voltage source as a calculator for the charge Q_{m}. The charge Q_{m} from (6.12) became an auxiliary voltage to enable Verilog-A to express result of (6.14) using arbitrary voltage source and then the result returns back as the charge to (6.14). The solution is graphically demonstrated in Fig. 6.2.

However, such solution is not recommended for robust models, as it can cause convergence issues [40]. This happens during model verification using latest versions of Eldo simulator. The convergence issue appeared during transient analysis. So although Spectre simulation, HSpice simulations as

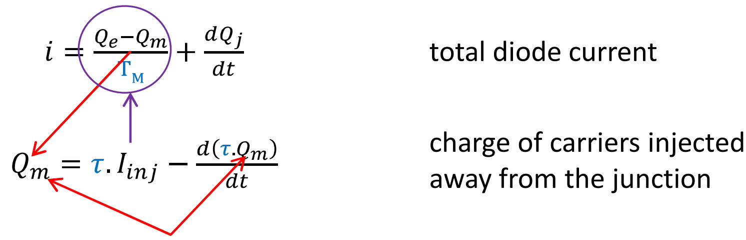

Figure 6.1: Interdependencies in diode reverse recovery formulas.

well as the simulation with older Eldo versions passed well, we had to look for an alternative solution.

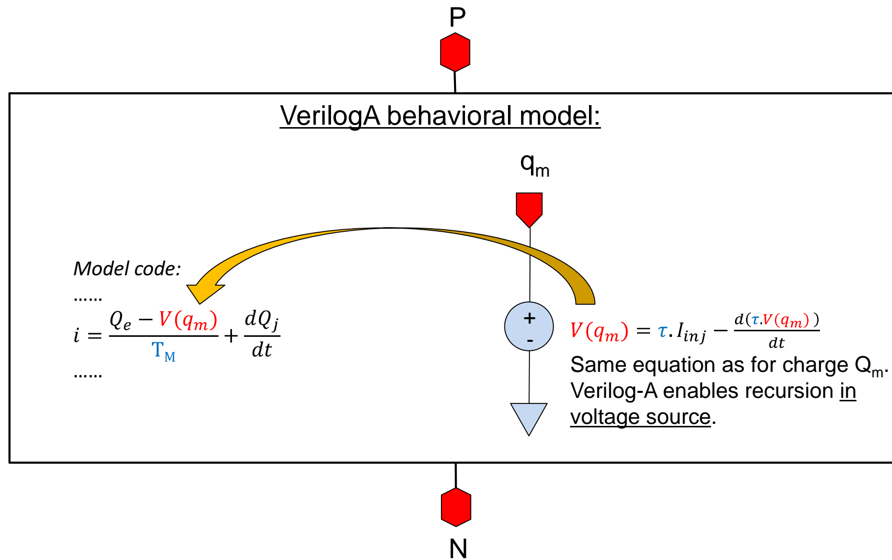

Figure 6.2: Solving the recursive calculation of reverse recovery charge.

Based on recommendations in [40], the equation (6.11) represented in Verilog-A by the current source was divided into two parallel equations represented in Verilog-A by two parallel current sources flowing through two separate branches as depicted in Fig. 6.3. The first branch represents the junction current

$$I_{\mathrm{j}} = \frac{dQ_{\mathrm{j}}}{dt} \tag{6.16}$$

the second branch represents the injection current I_{inj}, specified by (6.12).

The recursion then appears only in the branch with injection current $I_{\rm inj}$. Substitution of (6.14) into (6.12) gives

$$I_{\rm inj} = \frac{Q_{\rm e} - (\tau I_{\rm inj} - \frac{d(\tau Q_{\rm m})}{dt})}{T_{\rm M}} \tag{6.17}$$

Minority carrier lifetime τ is a tuning parameter, so it can be as a constant factored out of the time derivative. Equation (6.17) can then be expressed as

$$I_{\rm inj} = \frac{Q_{\rm e} - \tau I_{\rm inj}}{T_{\rm M}} + \frac{\tau \frac{dQ_{\rm m}}{dt}}{T_{\rm M}} \tag{6.18}$$

where $Q_{\rm m}$ is from (6.12) obtained as

$$Q_{\rm m} = Q_{\rm e} - T_{\rm M} I_{\rm inj} \tag{6.19}$$

The total diode current in the model is then composed of two parallel currents defined by equations (6.18) and (6.16). Equations (6.18) and (6.19) still contain recursion, but much simpler than in the original approach, so Verilog-A simply solves it. Another advantage of using the (6.18) form is its clear separation between real and imaginary parts, which helps in AC analysis described later.

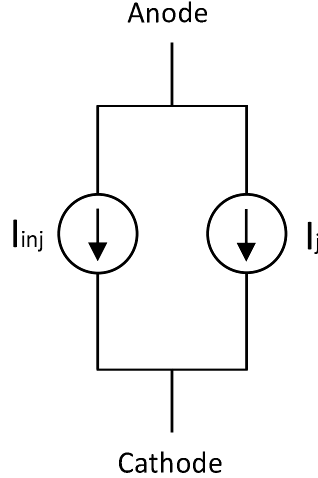

Figure 6.3: Example of using two parallel branches for modeling of injection and junction currents independently.

The next goal was to add temperature scalability to the model, using the standard temperature dependency equations. The most dominant for the

diode is temperature dependency of saturation current, defined by equation [32, 60]

$$I_S(T) = I_S(T_{\text{nom}}) \left(\frac{T}{T_{\text{nom}}}\right)^{\text{X}_{\text{ti}}} \exp\left(\frac{qE_G}{k_{\text{b}}T}(\frac{T}{T_{\text{nom}}} - 1)\right) \tag{6.20}$$

where T is absolute temperature, T_{nom} is nominal temperature, for which the parameters of the device are defined (typically $T_{\text{nom}} = 300K$), X_{ti} is saturation current temperature exponent used as a SPICE parameter for the tuning of temperature model, q is elementary charge, k_{b} is Boltzmann constant and E_G is the band-gap energy.

The temperature dependency of silicon band-gap energy is defined as [42]

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{6.21}$$

where experimentally obtained constants for silicon are $E_G(0) = 1.16\text{eV}$, $\alpha = 7.02 \times 10^{-4}\text{eV/K}$ and $\beta = 1108\text{K}$.

The nominal temperature saturation current $I_S(T_{\text{nom}})$ in (6.20) was extended with the high-injection parameters by adding the factor

$$K_{\text{fwd}} = \frac{1}{1 + \sqrt{\frac{I_S(T)\exp\left(\frac{V - R_S I_{\text{pn}}}{nV_{\text{t}}} - 1\right)}{I_K}}} \tag{6.22}$$

where I_K is high-injection knee current and R_S is series resistance. Both parameters are used as model tunable parameters. The final $I_S(T_{\text{nom}})$ is then calculated as

$$I_S(T_{\text{nom}}) = I_S K_{\text{fwd}} \tag{6.23}$$

The temperature dependency was also added to the series resistance parameter, using following equation [21]

$$R_S(T) = R_S(T_{\text{nom}})(1 + T_{RS}(T - T_{\text{nom}})) \tag{6.24}$$

where T_{RS} is temperature coefficient of series resistance used as a tunable model parameter. The impact of series resistance was added also to (6.13) modified to form

$$Q_{\text{e}} = \tau I_S(T)\exp\left(\frac{V - R_S(T)I_{\text{pn}}}{nV_{\text{t}}} - 1\right) \tag{6.25}$$

where $V - R_S I_{\text{pn}}$ represents voltage in p-n junction reduced by voltage drop across series resistance.

The temperature dependency was also added to the calculation of barrier drift capacitance, especially to the parameter V_J, using following equation [32, 60]

$$V_J(T) = V_J(T_{\text{nom}}) \left(\frac{T}{T_{\text{nom}}} \right) + 2V_{\text{t}} \ln \left(\frac{n_{\text{i}}(T_{\text{nom}})}{n_{\text{i}}(T)} \right) \tag{6.26}$$

where n_{i} is intrinsic concentration of used material, in our case silicon, with its own temperature dependency [42]

$$n_i(T) = n_i(T_{\text{nom}}) \left(\frac{T}{T_{\text{nom}}} \right)^{X_{\text{ti}}} \exp \left(\frac{q}{2k} \left(\frac{E_G(T_{\text{nom}})}{T_{\text{nom}}} - \frac{E_G(T)}{T} \right) \right) \tag{6.27}$$

where X_{ti} is intrinsic concentration temperature exponent, typically set to a value of 1.5.

The scalability of the model with dimension of the p-n junction was created by adding of area factor *area*, which multiplies current parameters I_S or I_K and capacitance parameter C_{J0} and divides series resistance parameter R_S. More sophisticated scaling can be implemented by replacement of these model parameters with customized scaling equations dependent on length, width, perimeter, number of fingers, etc.

The model convergence was assured by adding parallel conductance controlled by the general SPICE parameter GMIN, representing minimal conductance of the model for the case, that the simulated current is too low. SPICE simulators clamp the maximum resistance to 1/GMIN, which defaults to 10^{12} Ω and can be set as an option parameter [60].

The original model prototype contained also avalanche breakdown parameters. But after testing of model convergence using transient simulation, AC and DC simulations or temperature simulations, the avalanche effect was found to cause convergence issues. Therefore it was decided to omit this capability and prioritize the model stability and perfect convergence. Breakdown voltage can be modeled externally using compact diode SPICE model connected in parallel to this behavioral model. Similar practice is commonly used in bipolar transistor model, diffusion/implanted resistor model or some other models containing p-n junction.

Also flicker noise parameters were omitted, however in this case their implementation should not cause any convergence troubles.

6.3 Model validation

The best validation of the final behavioral model is its application to real device and use for the simulation of real design. In our case the model parameters of two different components were measured and extracted: Zener

diode manufactured in integrated 0.25 μm BiCMOS technology and drain-bulk diode of power LDMOS transistor manufactured in fast discrete 0.25 μm technology developed for fast GHz applications.

6.3.1 Validation in time domain

Time domain measurement was provided using pulse generator Agilent 81104A and oscilloscope Tektronix DPO 7104C with current probe Tektronix CT1. The simulation netlist must reflect the reality including all the parasitic effects. The signal simulated by the ideal SPICE pulse source does not reflect the real signal at the end of cable coming from real pulse source. Therefore it is necessary to add all the parasitic phenomena to the netlist, as it is depicted in Fig. 6.4. The measurement was provided on wafer to eliminate the impact of the package, which on the other hand made taking the voltage and current probes close to DUT (Device Under Test) very difficult or even impossible. To see the current flowing directly through DUT without impact of parasitic cable between current probe and DUT, it was necessary to add the parasitic RLC circuit to the netlist. The highest impact comes from the parasitic capacitance, which has to be considered in the calculated deembedded measured current used instead of current coming from oscilloscope - see Fig. 6.4.

The circuit depicted in Fig. 6.4 is used directly for the simulation and tuning model based on measured data. The first step is to measure the "open" circuit (connected probes, connected cables, needle up) and tuning the netlist RLC parameters to fit the "open" simulation with "open" measured data. The second step is to connect DUT and measure. The final DUT current is then calculated as the current measured in current probe minus simulated current at the capacitor $C_{\text{parasitic}}$.

Measured pulse characteristics compared with simulated results are shown in Fig. 6.5 and Fig. 6.6. It is apparent, that the parasitic drain-bulk diode

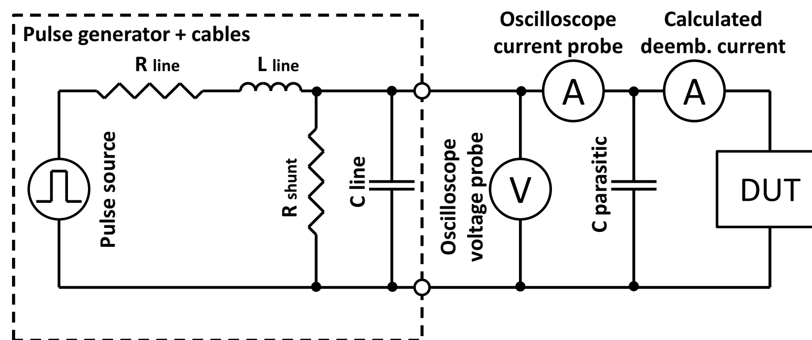

Figure 6.4: Setup for pulse measurement of diode reverse recovery.

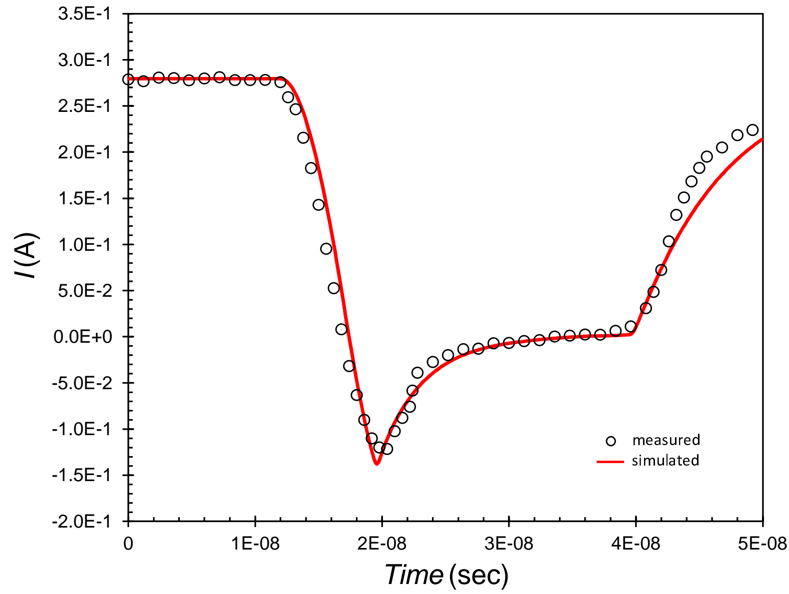

Figure 6.5: Current forward-to-reverse transient of Zener diode with area=0.01 mm^2.

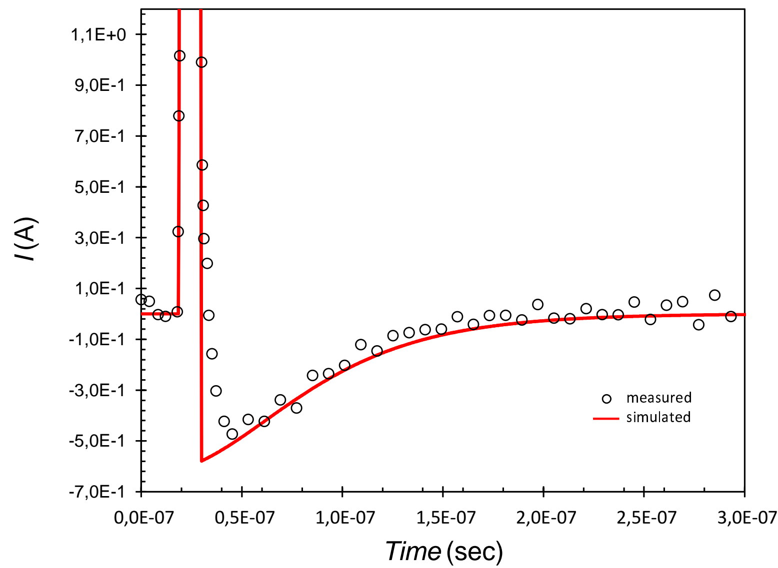

Figure 6.6: Current forward-to-reverse transient of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is about 2.5 m.

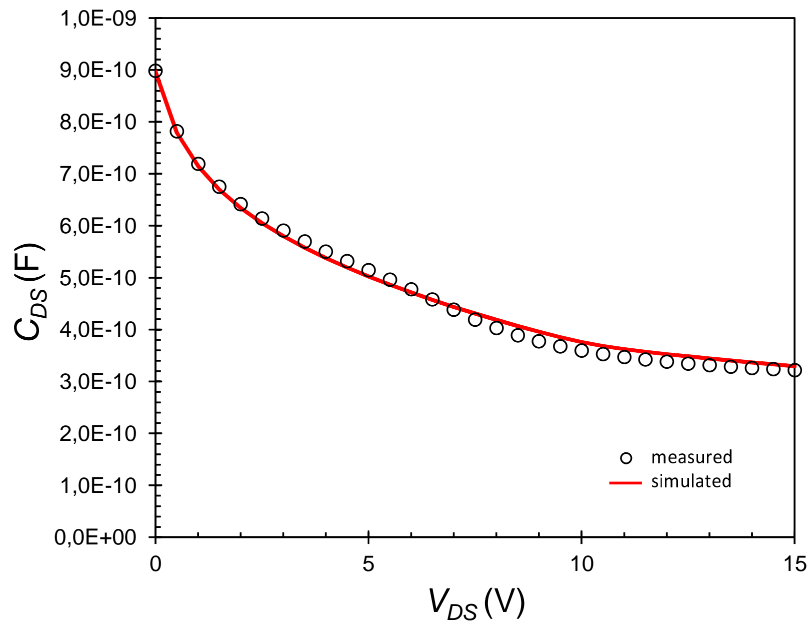

Figure 6.7: C-V characteristic of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m.

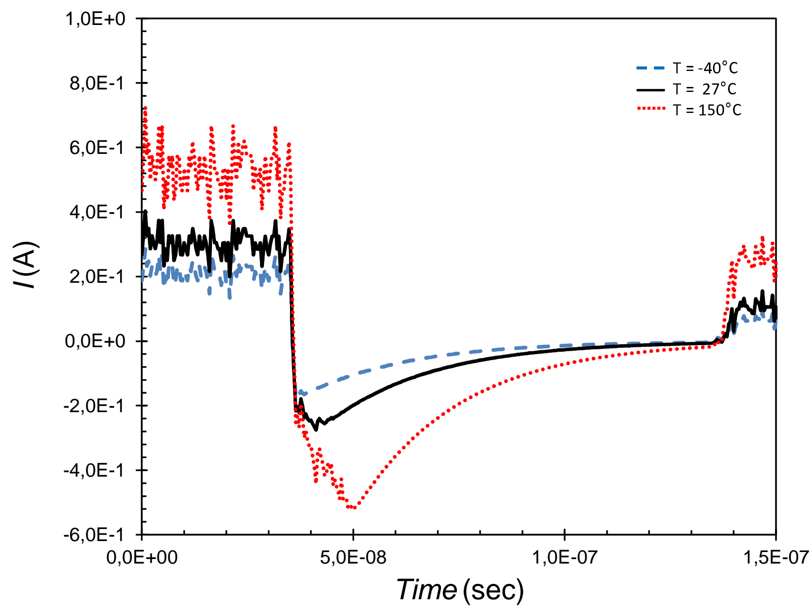

Figure 6.8: Verification of the model temperature dependency - simulation of current response forward-to-reverse transient.

of discrete power LDMOS with gate width 2.5 m containing several narrow fingers of p-n junction with relatively large area and perimeter has significantly larger reverse recovery time than the integrated Zener diode. The model is able to cover large portfolio of various device types. The first step prior to the reverse recovery extraction must be of course the accurate DC model and mainly accurate model of reverse bias barrier capacitance. The example of the measured vs. simulated barrier capacitance of power LDMOS drain-bulk diode is in Fig. 6.7.

The temperature dependency was verified by the comparison with standard SPICE diode model. The I-V and C-V curves scale exactly same as in standard SPICE diode model. Simulated reverse recovery temperature dependency is demonstrated in Fig. 6.8.

The scalability of the model was verified by the comparison with standard SPICE diode model. The I-V and C-V curves scale exactly same as in standard SPICE diode model. Current response transient characteristics unlike standard SPICE model contain the reverse recovery effect with the scaling correlated to the DC scaling - see Fig. 6.9. Larger device simulates larger current also in reverse recovery. Voltage response transient characteristics on the other hand follows CV scaling. Larger device with larger capacitance simulates larger delay of dV/dt - see Fig. 6.10. The smallest device with the negligible simulated reverse recovery depicted as dotted line in Fig. 6.9 has simulated voltage response similar to the simulated standard SPICE diode model without implemented reverse recovery, as it is demonstrated in Fig. 6.10.

6.3.2 Validation in frequency domain

As a verification of physical correctness the reverse recovery model, it was decided to measure the admittance of discrete power LDMOS drain-source diode manufactured in fast GHz discrete 0.25 μm technology and compare measured data with simulated results of standard SPICE diode model and simulated results of new Verilog-A diode behavioral model. For the measurement the network analyzer Agilent 8753 and DUT designed as two-gate in ground-signal-ground layout were used. The schematic of test method is presented in Fig. 6.11.

The applied DC forward voltage at p-n junction was set to range 0.7V–0.8V. For a voltage below 0.7V the measured current is lower than network analyzer noise floor, for a voltages above 0.8V the measured data are affected by series resistance. The device was measured at frequencies from 300 kHz to 3 GHz.

Measured scattering S-parameters were converted to admittance Y-parameters using conversion equations [18] implemented in IC-CAP model extraction tool and plotted as a real and imaginary parts vs. frequency.

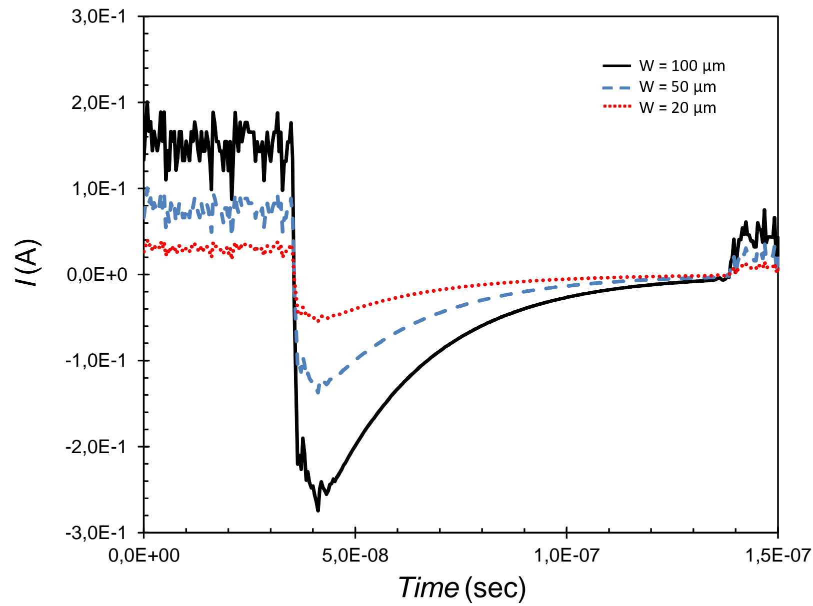

Figure 6.9: Verification of the model scalability - simulation of current response forward-to-reverse transient.

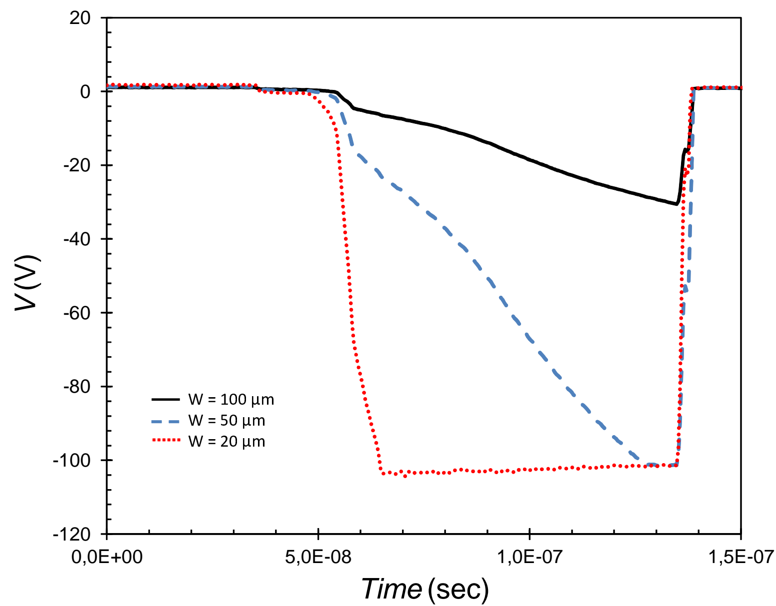

Figure 6.10: Verification of the model scalability - simulation of voltage response forward-to-reverse transient.

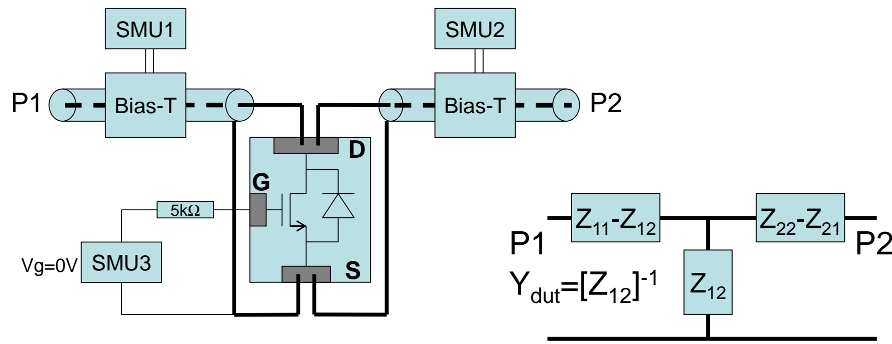

Figure 6.11: Setup for MOSFET drain-source diode S-parameter measurement.

Fig. 6.12 demonstrates the real part of LDMOS parasitic drain-bulk diode admittance using standard SPICE diode model. Dotted line demonstrates the impact of standard diode parameters. Fig. 6.13 shows the same measured data compared with simulated results of behavioral diode model containing the reverse recovery effect. It is apparent, that although the model fit is not ideal, the new Verilog-A model has much better trends than the original SPICE model. This improvement is even more visible in imaginary part of admittance, where the Fig. 6.14 shows the measured data vs simulations of standard SPICE diode model, while the Fig. 6.15 demonstrates the same data vs simulation of new Verilog-A model.

As it was already mentioned, the model accuracy in Fig. 6.13 and Fig. 6.15 is still unsatisfactory especially at high frequencies. But it is still much more accurate than in the case of standard SPICE model demonstrated in Fig. 6.12 and Fig. 6.14. The main reason of publishing these plots is to demonstrate, that the implementation of reverse recovery naturally improves the model even in the forward area.

In the case of very large fast power devices, or in the cases, where measured p-n junction is part of some more complex device and the quality of p-n junction is controlled by more terminals (e.g. drain-source diode in LDMOS controlled by the gate voltage), it can be very difficult to measure transient of diode switching from on to OFF state. In such a case the measurement of S-parameters of two-port using the network analyzer can be used as an alternative.

The disadvantages of this method are current and voltage limitation of the network analyzer, the need for a of special ground-signal or ground-signal-ground test structures and a more difficult parameter extraction, especially difficult differentiation between parameters τ and T_{M}. The advantages are less noisy measured data in some cases and an easy separation of measurements in various bias points and their potential customization and

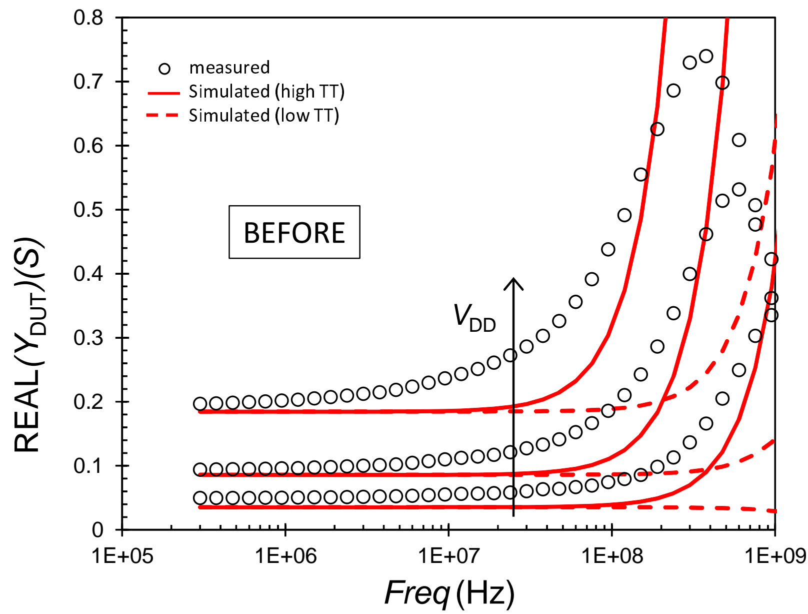

Figure 6.12: Measured data vs. simulation BEFORE implementation of new behavioral model: Real part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5m, the applied V_{DD} is 0.7V, 0.75V and 0.8V.

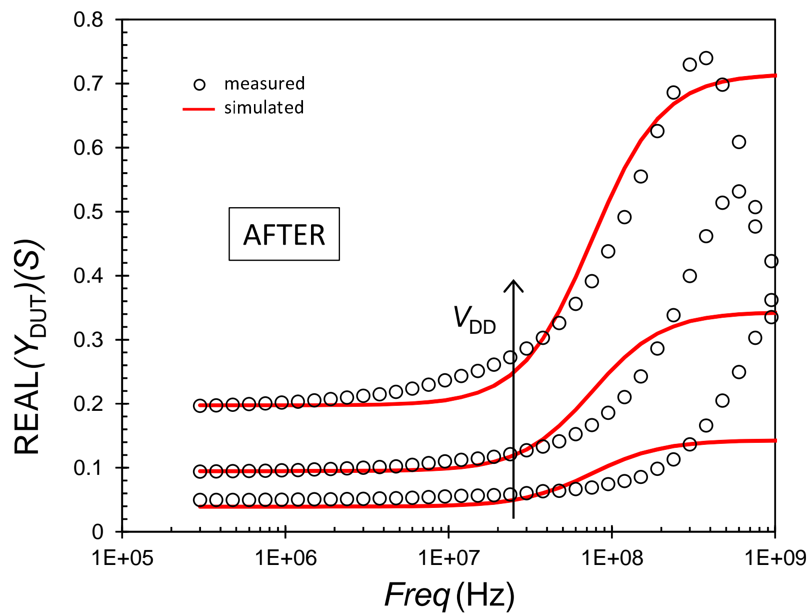

Figure 6.13: Measured data vs. simulation AFTER implementation of new behavioral model.

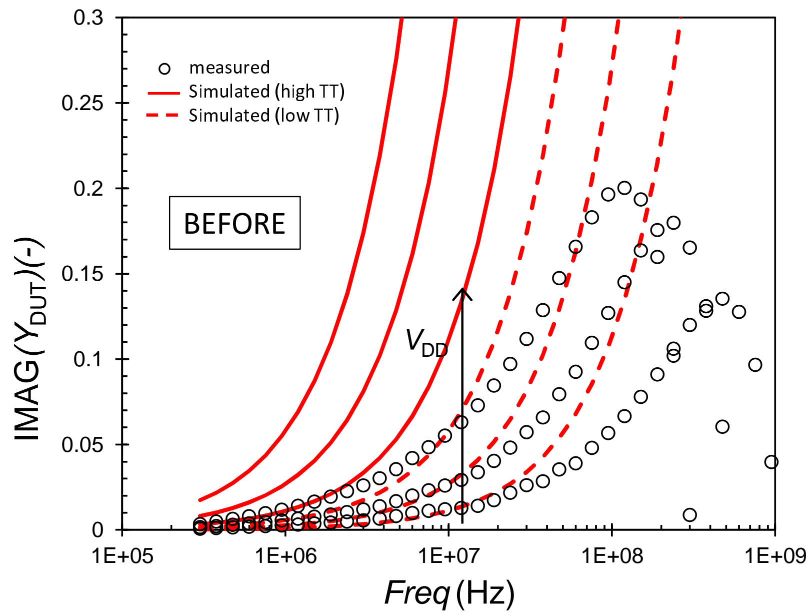

Figure 6.14: Measured data vs. simulation BEFORE implementation of new behavioral model: Imaginary part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5m, the applied V_{DD} is 0.7V, 0.75V and 0.8V.

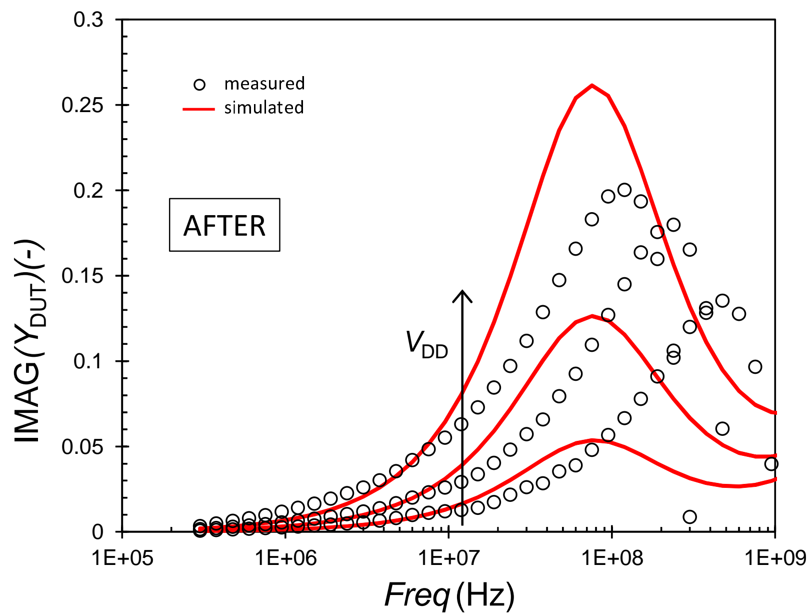

Figure 6.15: Measured data vs. simulation AFTER implementation of new behavioral model.

parametrization in the model.

6.4 Model parameter extraction

The final model is compatible with the standard SPICE diode [60] implemented in common SPICE simulator as *level* 1. Table 6.1 demonstrates the key model parameters of published model having the same meaning like in *level* 1 model. Therefore also the model parameter extraction is the same.

The main difference of the model parameter set in Table 6.1 comparing to model parameter set in [60] is, that the *level* 1 SPICE parameter transit time T_T has been replaced by two new parameters diffusion transit time T_{M} and minority carrier lifetime τ.

The transfer of *level* 1 to the published behavioral model containing the reverse recovery effect is therefore very simple. The two new parameters T_{M} and τ can be simply extracted from the measured transient characteristics containing reverse recovery effect demonstrated in Fig. 6.5 or Fig. 6.6.

Due to the simplicity, this publication does not focus on the model details contained in *level* 1 as for example area vs perimeter vs length/width scaling or modeling of parasitic metal capacitor. Therefore the Table (6.1) contains only the key model parameters, related to the published reverse recovery effect.

Table 6.1: Set of basic tunable model parameters.

Parameter	Description	Unit	Default
$AREA$	Area factor	-	1
I_S	Saturation current	A	10^{-14}
n	Emission coefficient	-	1
C_{j}	Zero-bias junction capacitance	F	0
M_{j}	Grading coefficient	-	0.5
V_{j}	Junction potential	V	1
T_{M}	Diffusion transit time	sec	10^{-12}
τ	Minority carrier lifetime	sec	10^{-12}
R_S	Series resistance	Ω	0
I_K	High-injection knee current	A	1
T_{nom}	Nominal model temperature	K	300
T	Absolute model temperature	K	300
X_{ti}	Saturation current temperature exponent	-	3
E_G	Band-gap energy	eV	1.11
T_{RS}	Temperature coefficient of series resistance	K^{-1}	0

6.5 Comparison with SPICE compact models containing reverse recovery effect

The main reason of developing our Verilog-A diode model was the lack of diode SPICE compact model containing reverse recovery. The first prototype of the model was developed in cooperation with prof. Lauritzen from the University of Washington [25] and the Verilog-A code was placed in the University of Washington web pages.

However, during the time the new compact diode models containing reverse recovery as for example hisim_diode or diode_cmc appeared in some SPICE simulators. Our concept was to make the diode model compatible with the original SPICE diode model [60] to allow the simple transfer of the standard diode SPICE model to the new model only by adding the reverse recovery effect using two simple model parameters. Diode_cmc has completely different set of model parameters, so our interest for the below described model-to-model comparison was focused on the comparison of our Verilog-A diode model with HiSIM diode model, in Spectre simulator called hisim_diode.

Although the Spectre simulator has declared the HiSIM reverse recovery model, actual simulations still ignore the parameters for the reverse recovery. So in this case for the model comparison only the simuator Eldo was used.

Both our Verilog-A and compact HiSIM models are based on similar source [25], so the same or very similar simulation results were expected. As it is demonstrated in Fig. 6.16, the simulated current pulses of HiSIM model and published Verilog-A model are comparable, while the simulated current pulse of standard compact SPICE model does not contain reverse recovery effect.

However, as it is demonstrated in Fig. 6.17, in the area of high injection the HiSIM diode model differs from next two models due to missing parameter knee current I_K. This area is calculated differently in HiSIM model, while the published Verilog-A model uses the same equations like standard SPICE diode model [60] in this area.

So, although published Verilog-A model and HiSIM model have comparable simulated results for low current, for high forward current the published Verilog-A model follows the original standard SPICE diode model and can be used for simple adding reverse recovery effect to already existing extracted SPICE model. Moreover, it should be pointed out that only the models based on I_K (as our Verilog-A one) define the diode high-current area correctly (in principle).

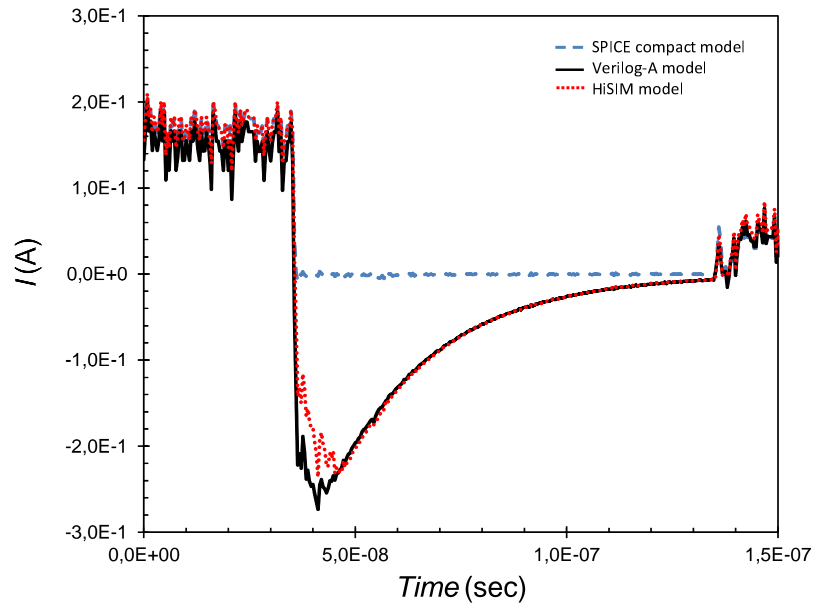

Figure 6.16: Comparison with HiSIM and standard level1 SPICE model - simulation of current response forward-to-reverse transient.

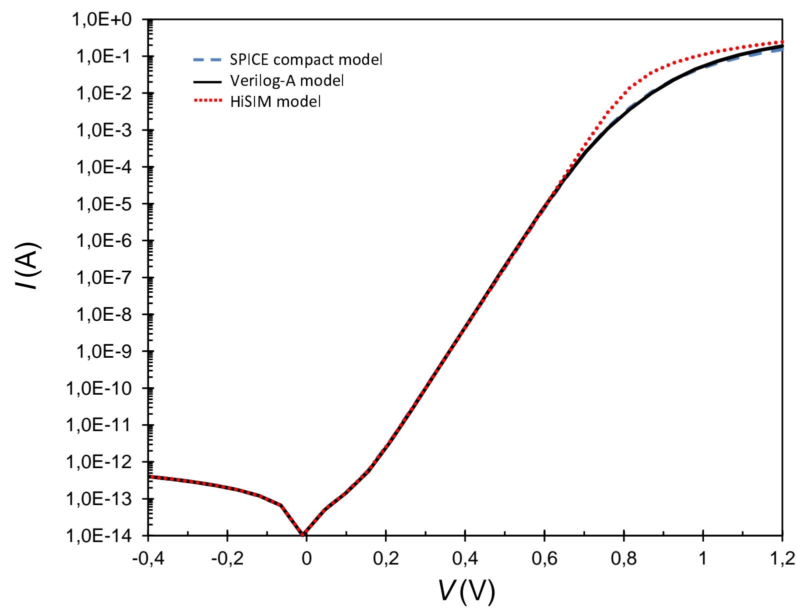

Figure 6.17: Comparison with HiSIM and standard level1 SPICE model - simulation of DC I-V characteristic.

6.6 Conclusion

This chapter describes the complex robust temperature and area scalable Verilog-A model of diode containing reverse recovery effect.

The model can be used as stand-alone 2-terminal diode or as a parasitic p-n junction of more complex lumped macromodel, e.g. MOSFET, JFET, bipolar transistor or IGBT. Due to the implemented reverse recovery effect the model is useful especially for high-speed or high-voltage power devices.

Two methods of model parameter extraction or model validation have been demonstrated – time domain pulse method and frequency domain S-parameter method.

The comparison with HiSIM model demonstrated differences in high injection area, where the published Verilog-A model uses the same concept as the basic diode model [60]. It was also presented, that the Verilog-A model is applicable even in the simulators where the HiSIM compact model is not implemented yet.

Although there exist many publications about reverse recovery modeling, the most of published models are not usable for production design, mainly due to the insufficient convergence. The model presented in this chapter fills this gap – the model has been already used in several production designs. However during work on the model the new version of Eldo simulator presented diode reverse recovery model very similar as the presented one. The contribution of presented model is the implementation of high injection current parameters and mainly its usability in all simulators supporting Verilog-A.

The new ideas described in this chapter were approximately 85% author's own. The author's ratio of participation in the relevant publication [6] was about 30%.

CHAPTER 7

Implementation of Bi-modal Statistical Distribution into SPICE Models

7.1 Introduction

The requirements on the accuracy of SPICE models [32, 60] are being continuously increased and the implementation of process statistical distribution nowadays is the standard. Designers can run Monte Carlo simulation [22], sensitivity analysis or various predefined or customized generic cases, so the SPICE models are required to represent the real process distribution containing targets, process sigmas, including correlations and various types of statistical distributions.

Still more often it happens, that one technology is produced in two or more plants, where each plant has slightly different parameters. Such situation should be implemented in SPICE models too, which is often done by simple widening of process sigma, so the simulation covers all the plants. However, in the extreme case it can happen, that the difference of given measured parameter between two plants is larger than its process distribution. The result is then the bi-modal distribution.

This chapter published in [3] demonstrates, how such bi-modal distribution can be implemented into SPICE model including weight factor between two simulated cases. The first section presents several reasons of bi-modal distributions, including mentioned example with two plants. The next section deals with the implementation of bi-modal distribution in the model, including detailed model equations. Simulated results of Monte Carlo simulations are presented in demonstrative plots.

7.2 Examples of Bi-modal Process Distributions

Bi-modal statistical distribution of measured electrical parameter is not as infrequent as it could seem. There can be several reasons of bi-modal distribution, but only some of them should be simulated.

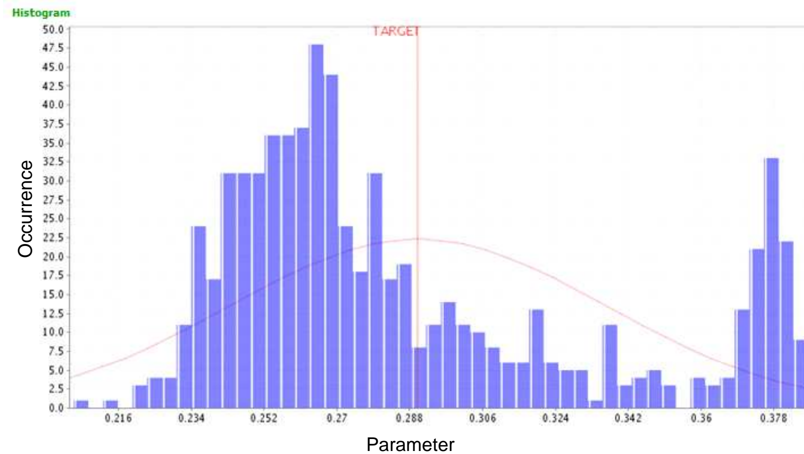

Figure 7.1: Example of bi-modal distribution modeled by normal distribution with wider sigma. Typical case simulation (peak of red curve) in such case does not represent the real typical case(s).

7.2.1 One Product Manufactured in Two Wafer Lines

The mass production of integrated circuits is often manufactured in two or even more plants. The reason is the backup for the case of unexpected failure in one plant and better flexibility for the controlling of the production. Two different plants naturally produce slightly different electrical parameters and in some extreme cases can appear even the bi-modal statistical distribution. Such case should be considered also in the model. The simple widening of sigma and covering both distributions with the wider Gaussian curve can be sufficient as concerns the parameter distribution, but in the typical case simulation it can happen, that the designer simulates the case with very low probability of occurrence instead of the typical case, as it is demonstrated in Fig. 7.1. This chapter represents the tool to simulate both plants together with controlling the ratio between productions, so in extreme cases only one of them depending on the simulation inputs can be simulated.

7.2.2 Technology Related Causes

Some electrical components can have some technology related issue causing the bi-modal distribution of one or more electrical parameters. The example can be Schottky diode using titan silicide instead of much more expensive platinum silicide. This cheaper solution makes narrower Schottky junction, which causes in some cases metal diffusion through the titan silicide and makes Schottky junction metal-silicon instead of metal-silicide. Finally, the forward current flowing through such Schottky junction can be even two orders lower. But this happens only in some cases. In the other cases the metal does not diffuse. This effect makes then the clear bi-modal distribution, because the distance between peaks is larger than the process sigma of two mentioned cases.

7.2.3 Combination of Various Measurement Setups in One Factory

In the case of mass production can happen, that the statistical measurement is provided by two or more testers or measurement lines. Although all the testers used in the production should be calibrated, sometimes especially in the case of very sensitive parameters it can happen, that different measurement lines give slightly different statistical results. In the extreme case such data can result as a bi-modal distribution. In this case the bi-modality does not exist in real process, it reflects only the measurement setup differences. Therefore the results of lines should be normalized using the offset, annulling the measurement differences.

7.3 Simulation of Bi-modal Statistical Distribution

Both targets representing two peaks have to be specified for the simulation of the device with bi-modal statistical distribution. The two nominal case models are supported instead of one nominal case model representing the peak of standard uni-modal distribution. The device macromodel therefore contains a control parameter $\mathrm{switch}_{\mathrm{BM}}$ for the switching between two separate models. If $\mathrm{switch}_{\mathrm{BM}}=0$, the model for first peak is active, if $\mathrm{switch}_{\mathrm{BM}}=1$, the model for second peak is active. The switching between two peaks can be done by switching between two independent models e.g via AREA factors

$$\mathrm{AREA1}_{\mathrm{BM}} = \mathrm{switch}_{\mathrm{BM}}\mathrm{AREA1} \qquad (7.1)$$

$$\mathrm{AREA2_{BM}} = (1 - \mathrm{switch_{BM}})\mathrm{AREA2} \tag{7.2}$$

where AREA1 is area factor of the model representing the first peak and AREA2 is area factor of the model representing the second peak. The suffix BM means, that the parameter is controlled by bi-modal switch $\mathrm{switch_{BM}}$ and reflects the bi-modality.

The alternative and more flexible method is the switching of various model SPICE parameters affected by the bi-modality, e.g.

$$P_{\mathrm{BM}} = \mathrm{switch_{BM}} P1 + (1 - \mathrm{switch_{BM}})P2 \tag{7.3}$$

Where P_{BM} is SPICE model parameter containing bi-modality, P1 is parameter value for the first peak simulation, P2 is parameter value for the second peak simulation.

This however covers only simulation of two nominal cases representing two peaks of bi-modality. The simulation of bi-modal statistical distribution is explained in following sections. The first subsection explains how the statistical models are implemented, the second subsection demonstrates the implementation of bi-modality.

7.3.1 Implementation of Normal and Log-Normal Statistical Distributions in SPICE Models

For the statistical model and the translation of electrical parameter statistical distribution into SPICE model parameter distribution the Backward Propagation of Variances (BPV) [36, 39] is used. In the case, where the measured statistical electrical parameter is SPICE model parameter (e.g. sheet resistance or gate oxide thickness) the Forward Propagation of Variances (FPV) is used [36]. In both cases the SPICE parameters being statistically distributed are replaced with the mapping equations, containing shift of the parameter to the target, process sigma and master variable ensuring the link between correlated parameters.

The most common is mapping equation using relative shift δr [36, 52]

$$P_{\mathrm{Fin}} = P\Big(1 + \frac{\delta r_{\mathrm{P_m}} + \mathrm{var_i} \times \delta r_{\mathrm{P_s}}}{100}\Big) \tag{7.4}$$

where P_{Fin} is final statistically distributed SPICE parameter, P is the parameter value before implementation of statistical distribution, $\delta r_{\mathrm{P_m}}$ and $\delta r_{\mathrm{P_s}}$ are tuning parameters, where $\delta r_{\mathrm{P_m}}$ represents the relative shift of the parameter P to the target and $\delta r_{\mathrm{P_s}}$ represents the relative standard deviation σ of the parameter P.

The statistical distribution is controlled during Monte Carlo simulation by the set of independent master variables $\mathrm{var_i}$, where each master variable is

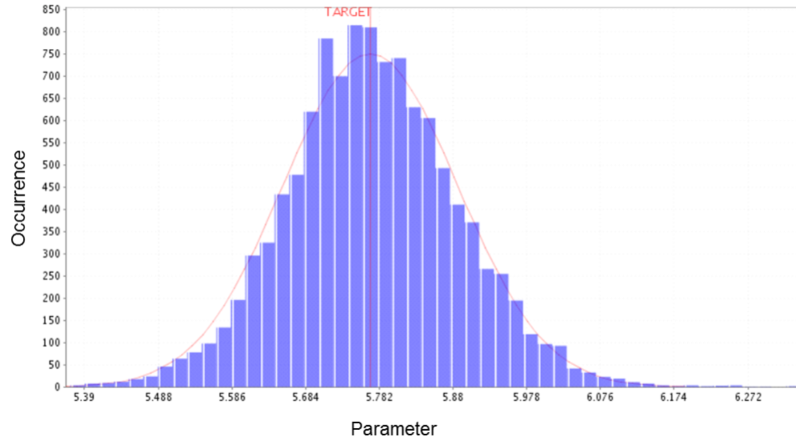

Figure 7.2: Example of measured and simulated normal distribution.

common for all correlated parameters in the model file. Each master variable varies randomly based on Gaussian distribution with $\mu = 0$ and $\sigma = 1$. This principle ensures that uncorrelated parameters vary independently, while correlated parameters vary simultaneously [36, 52].

The parameter P which can become positive or negative, is statistically modified by absolute shift δa as described in equation [36, 52].

$$P_{\mathrm{Fin}} = P + (\delta a_{\mathrm{P_m}} + \mathrm{var_i} \times \delta a_{\mathrm{P_s}}) \tag{7.5}$$

where $\delta a_{\mathrm{P_m}}$ and $\delta a_{\mathrm{P_s}}$ are tuning parameters representing in this case absolute shift of the parameter P to the target and absolute standard deviation σ of the parameter P. Monte Carlo simulation is in this case again controlled by the parameter $\mathrm{var_i}$.

In the case of log-normal distribution (e.g. in the case of leakage current) the following mapping equation is used:

$$P_{\mathrm{Fin}} = P\left(1 + \frac{\delta r_{\mathrm{P_m}}}{100}\right) \times 10^{\mathrm{var_i} \times \delta r_{\mathrm{P_s}}} \tag{7.6}$$

where $\delta r_{\mathrm{P_m}}$ and $\delta r_{\mathrm{P_s}}$ are tuning parameters representing relative shift and relative standard deviation σ of the logarithmic parameter P. Monte Carlo simulation is here again controlled by the parameter $\mathrm{var_i}$, and the exponential (7.6) performs conversion of Gaussian distribution of $\mathrm{var_i}$ to log-normal distribution of P_{Fin}.

All the demonstrated implementations expect the uni-modal distribution.

The following section presents the implementation bi-modality to statistical Monte Carlo simulation.

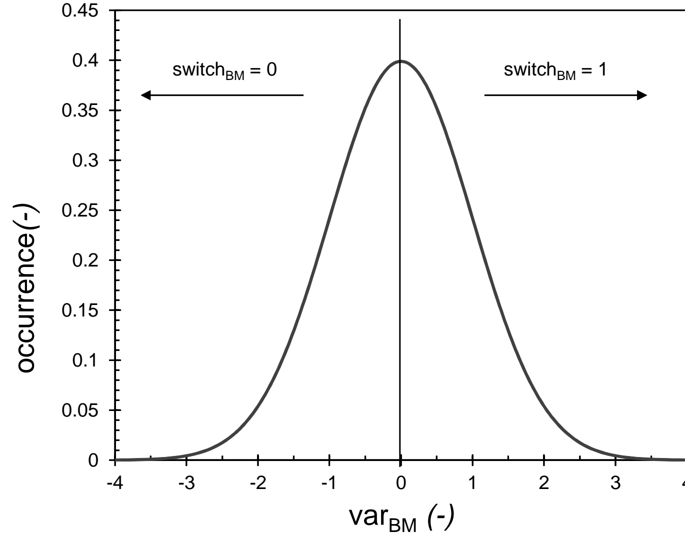

Figure 7.3: Simulated distribution of statistical master variable $\mathrm{var}_{\mathrm{BM}}$ with the coefficient $\mathrm{weight}_{\mathrm{BM}} = 0$. Simulated values of $\mathrm{var}_{\mathrm{BM}} < \mathrm{weight}_{\mathrm{BM}}$ set $\mathrm{switch}_{\mathrm{BM}} = 0$, simulated values of $\mathrm{var}_{\mathrm{BM}} >= \mathrm{weight}_{\mathrm{BM}}$ set $\mathrm{switch}_{\mathrm{BM}} = 1$. Zero value of $\mathrm{weight}_{\mathrm{BM}}$ makes the bi-modal peaks with comparable height.

7.3.2 Implementation of Bi-modal Statistical Distribution into SPICE Models

The substitution of statistically distributed SPICE parameter P_{Fin} from (7.4) or (7.5) or (7.6) to (7.3) gives the formula

$$P_{\mathrm{BMFin}} = \mathrm{switch}_{\mathrm{BM}} P_{\mathrm{Fin1}} + (1 - \mathrm{switch}_{\mathrm{BM}}) P_{\mathrm{Fin2}} \tag{7.7}$$

The switching between P_{Fin1} and P_{Fin2} during Monte Carlo simulation is controlled by setting either $\mathrm{switch}_{\mathrm{BM}} = 0$ or $\mathrm{switch}_{\mathrm{BM}} = 1$, which is done using statistically distributed master variable $\mathrm{var}_{\mathrm{BM}}$ varying randomly based on Gaussian distribution with $\mu = 0$ and $\sigma = 1$. The implementation of master variable $\mathrm{var}_{\mathrm{BM}}$ for the calculation $\mathrm{switch}_{\mathrm{BM}}$ is defined as

$$\mathrm{switch}_{\mathrm{BM}} = \mathrm{sgn}(\mathrm{sgn}(\mathrm{var}_{\mathrm{BM}}) + 1) \tag{7.8}$$

The calculated result of $\mathrm{switch}_{\mathrm{BM}}$ from (7.8) is:

for $\mathrm{var}_{\mathrm{BM}} < 0$: $\mathrm{switch}_{\mathrm{BM}} = 0$

for $\mathrm{var}_{\mathrm{BM}} \geq 0$: $\mathrm{switch}_{\mathrm{BM}} = 1$.

as is also demonstrated in Fig. 7.3.

Such model, however, represents only the case with the same probability of occurrence for both peaks. The example of the simulated bi-modal distribution with the same probability of both peaks and different standard

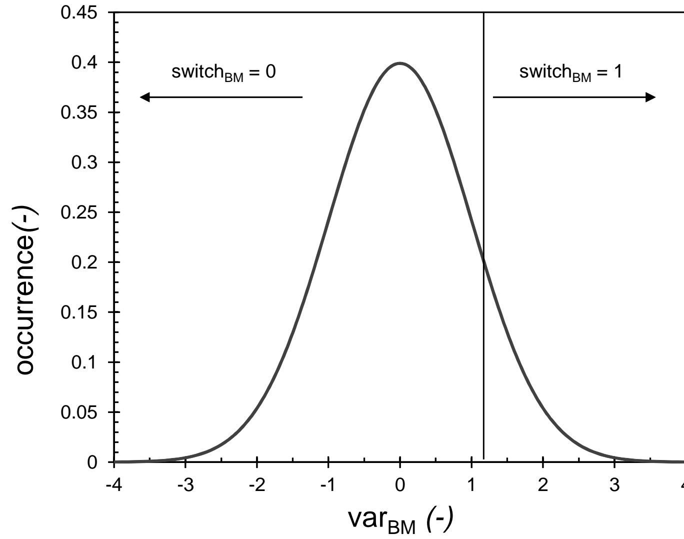

Figure 7.4: Simulated distribution of statistical master variable var_{BM} with the non-zero coefficient $\text{weight}_{\text{BM}}$. Simulated values of $\text{var}_{\text{BM}} < \text{weight}_{\text{BM}}$ set $\text{switch}_{\text{BM}} = 0$, simulated values of $\text{var}_{\text{BM}} >= \text{weight}_{\text{BM}}$ set $\text{switch}_{\text{BM}} = 1$. Non-zero value of $\text{weight}_{\text{BM}}$ makes asymmetrical bi-modal peaks.

deviation is demonstrated in Fig. 7.5. In this case the left distribution with higher σ is valid for $\text{switch}_{\text{BM}} = 0$, while the right distribution with lower σ is valid for $\text{switch}_{\text{BM}} = 1$. But the same probability of occurrence might not be always true. More typical is the bi-modal distribution, where one occurrence of one peak is dominant.

Therefore (7.8) has been extended to

$$\text{switch}_{\text{BM}} = \text{sgn}(\text{sgn}(\text{var}_{\text{BM}} - \text{weight}_{\text{BM}}) + 1) \tag{7.9}$$

where $\text{weight}_{\text{BM}}$ controls the ratio between probability of peak one and peak two occurrence.

The calculated result of $\text{switch}_{\text{BM}}$ from (7.9) is:

for $\text{var}_{\text{BM}} < \text{weight}_{\text{BM}}$: $\text{switch}_{\text{BM}} = 0$

for $\text{var}_{\text{BM}} \geq \text{weight}_{\text{BM}}$: $\text{switch}_{\text{BM}} = 1$.

The simulation of Fig. 7.5 adjusted for higher probability of right peak is demonstrated in Fig. 7.6, the simulation adjusted for higher probability of left peak is demonstrated in Fig. 7.7. Increasing parameter $\text{weight}_{\text{BM}}$ to positive or negative direction makes the effect stronger and finally for very large $\text{weight}_{\text{BM}}$ one of peak disappears and the distribution becomes uni-modal.

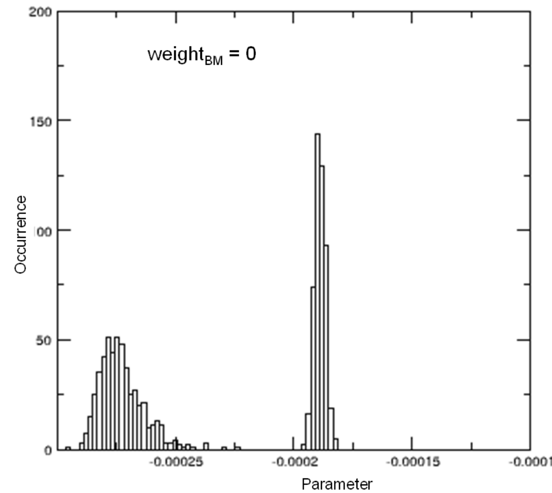

Figure 7.5: Simulated bi-modal distribution of a final model electrical parameter, where the left peak represents distribution with larger sigma. The probability of both peaks is in this case equal, which is represented by the same areas of simulated Gaussian distributions.

7.4 Conclusion

This chapter demonstrates principles of the modeling and simulation of bi-modal statistical distribution using SPICE simulators. Several examples from the production were used to demonstrate the usefulness of this this SPICE model extension. The principle is universal and applicable in all commercial SPICE simulators, and in all SPICE models. The model was verified with the real production data using SPICE simulators Spectre, Eldo and HSpice. The examples of simulated results are demonstrated.

The presented concept is very original and authors did not find any other publication describing this topic.

The new ideas described in this chapter were approximately 65% author's own. The author's ratio of participation in the relevant publication [3] was about 35%.

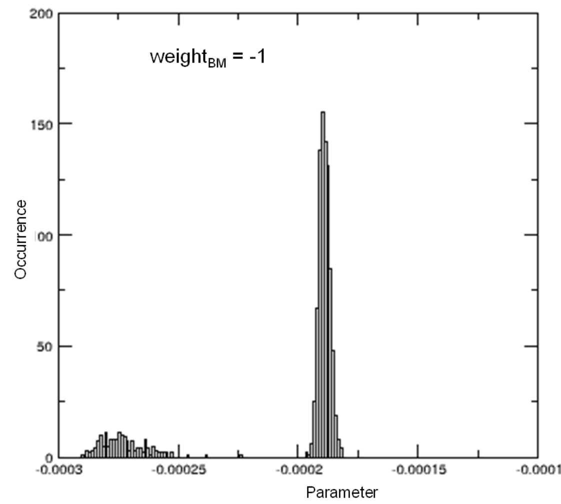

Figure 7.6: Simulated bi-modal distribution of a final model electrical parameter, where the left peak represents distribution with larger sigma. The probability of right peak is in this case higher, which is controlled by the negative value of parameter $\text{weight}_{\text{BM}} = 1$.

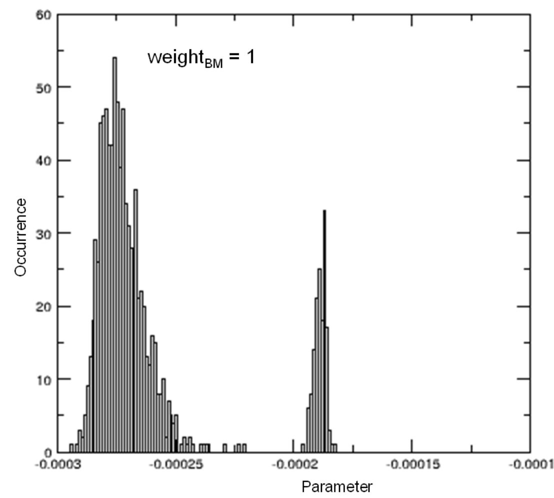

Figure 7.7: Simulated bi-modal distribution of a final model electrical parameter, where the left peak represents distribution with larger sigma. The probability of left peak is in this case higher, which is controlled by the positive value of parameter $\text{weight}_{\text{BM}} = 1$.

CHAPTER 8

New Challenges - Anomalous Phenomena in HV JFET Channel Pinching

8.1 Introduction

Power devices, such as startups or half-bridges usually include a very low doped layer as a drift area to be able to withstand high voltages in the order of hundreds of volts. This drift area is often pinched from top, bottom or both sides by a reversely doped layer [27].

Although previous chapters presented quite complex model of high voltage JFET containing a lot of new phenomena, the challenges for the future research still exist. Lot of effects solved neither by conventional compact models nor by recently published models including this thesis still can be observed and wait for implementation to SPICE simulators.

This chapter published in [7] demonstrates an interesting phenomenon, that could be added in the future as a new attribute to the existing dual-gate JFET models [5, 64].

8.2 Device Description

The discussed high voltage JFET is a relatively large device of circular or oval shape. The drain containing the bonding pad is located in the middle of the oval, to sustain applied high voltage. The source is at the device perimeter and the top gate is then forming a device annulus. As demonstrated in Figs. 8.1–8.3, the top gate represented by High Voltage PWell layer (HVPW) covers only a small part of the JFET drift area. However,

this small part represents the most important part of the device, as the JFET channel can be fully pinched by the HVPW layer. The rest of the drift area is represented by a very low doped Very High Voltage Nwell layer (VHVNW). The breakdown voltage of this high-voltage component is controlled by the distance between a drain contact and edge of the top gate. The longer the distance, the larger the breakdown voltage. In our case the high-voltage JFET is designed for 700 V, so its gate-to-drain distance is more than 100 μm while the top gate length is only a few μm. This structure causes interesting effects described below. The interaction between the top HVPW gate and the substrate representing the second bottom gate plays the key role in the presented effects.

8.3 Redistribution of Currents in High-Voltage Dual-Gate JFET

The dual gate JFET contains four terminals: drain, source, top gate and bottom gate represented by the substrate. The current flows through all four terminals so for our demonstration all four currents are considered.

Fig. 8.1 demonstrates the situation with a partly pinched JFET channel. The channel is partly depleted, which is marked by dotted green line. The device in this situation is operating in ON state and the current is flowing from drain to source due to the positive drain-source voltage. In other words, electrons flow from the source to the drain, which is demonstrated by a green arrow.

Increasing the negative gate voltage makes the channel more and more depleted and finally the depletion fully pinches the channel, as it is depicted in Fig. 8.2. The device in this situation is operating in OFF state and the drain to source current in this case is ideally equal to zero. However, the combination of fully depleted channel and relatively large gate-substrate voltage causes that the current starts to flow from the top gate to the substrate through the depleted VHVNW channel (vertical punch-through effect), which is again marked by the green arrow using the same convention of current direction as in Fig. 8.1 (the measured current has opposite direction than the green arrow). A part of this vertical current flows to the drain and another part flows to the source, resulting in at first sight unexpected the same direction of drain and source currents.

This effect can be eliminated by increasing the drain-source voltage. As soon as the drain-source voltage crosses a critical value, the electrical field makes the current flow across the depleted area (lateral punch-through). This effect is demonstrated in Fig. 8.3 including the impact ionization current flowing to the top and bottom gates.

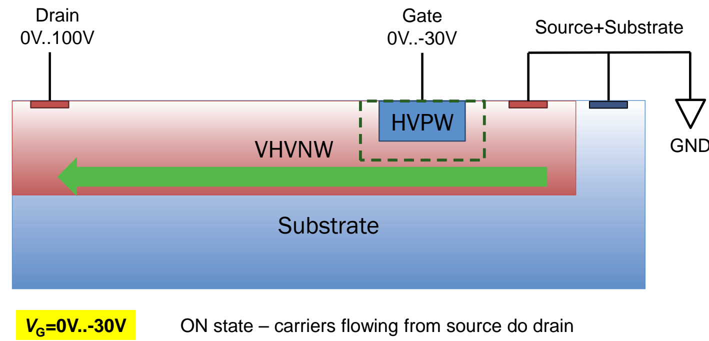

Figure 8.1: Current distribution of HV JFET in ON state (V_{G} < pinch-off voltage).

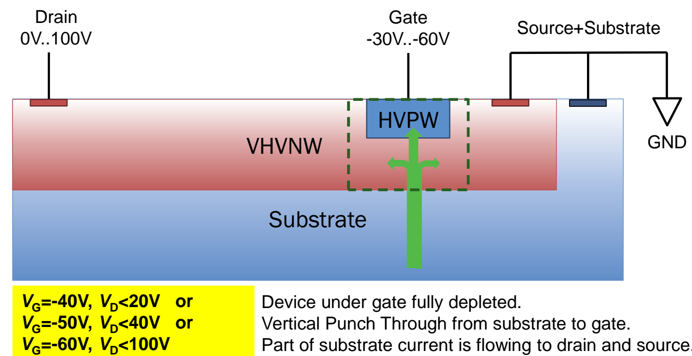

Figure 8.2: Current distribution of HV JFET in OFF state (V_{G} > pinch-off voltage) and low V_{D}.

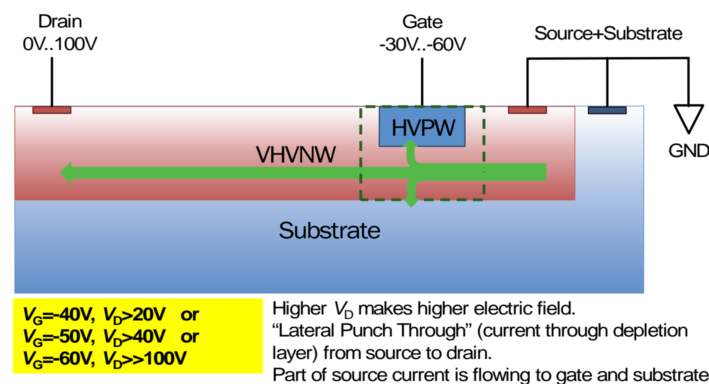

Figure 8.3: Current distribution of HV JFET in OFF state (V_{G} > pinch-off voltage) and high V_{D}.

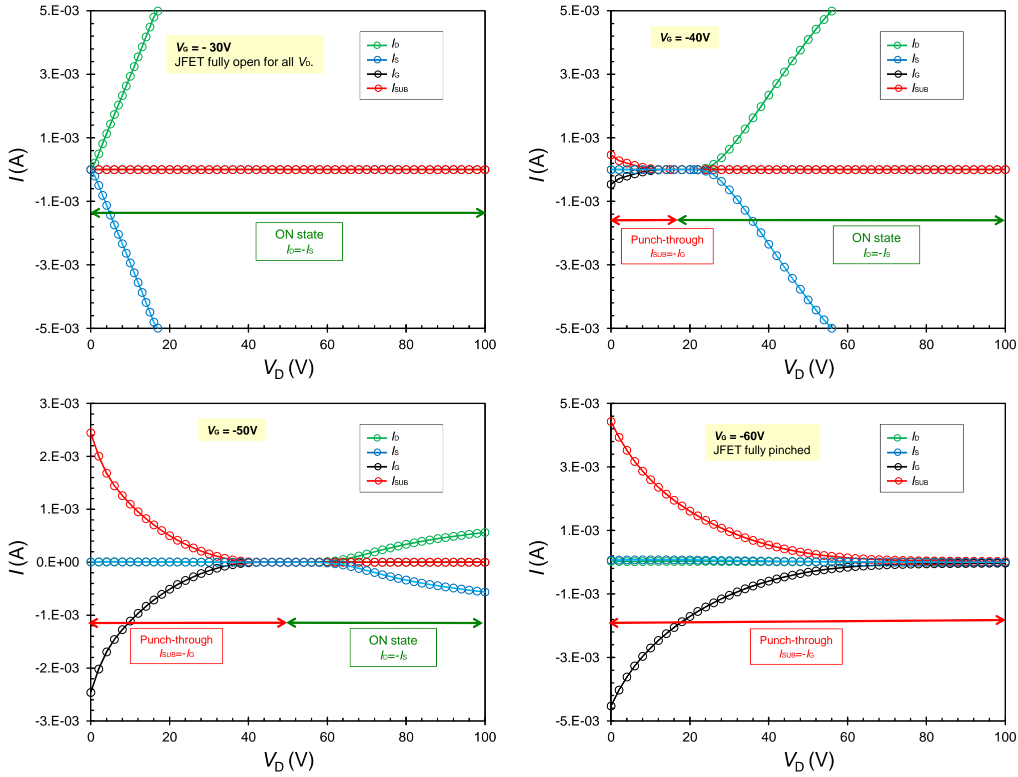

Figure 8.4: $I_{\mathrm{D}}(V_{\mathrm{D}})$ characteristics of high-voltage dual-gate JFET measured for various V_{G}.

It is apparent, that the combination of top gate and drain voltages significantly affects the pinch-off voltage of this type of high-voltage JFET and the difference between measured pinch-off voltages for various bias conditions can be relatively large. The modeling of such voltage dependent pinch-off voltage is demonstrated in [5, 4].

8.4 Experimental Results

Let us look at the experimentally measured currents of 700 V high-voltage dual-gate JFET. Figs. 8.4 and Fig. 8.5 show $I(V)$ curves of JFET measured with grounded source and grounded substrate. The primary dependent variable (X-axis) is the drain voltage.

Fig. 8.4 shows the full plots, and Fig. 8.5 shows the same plot zoomed to the lower currents. The Y-axis is in linear scale, because logarithmic scale does not show the current direction, which is crucial in our demonstration.

Plots in Fig. 8.4a and Fig. 8.5a demonstrate JFET operating in ON state. The top gate voltage is $V_{\mathrm{G}} = -30\,\mathrm{V}$, which is bellow the pinch-off

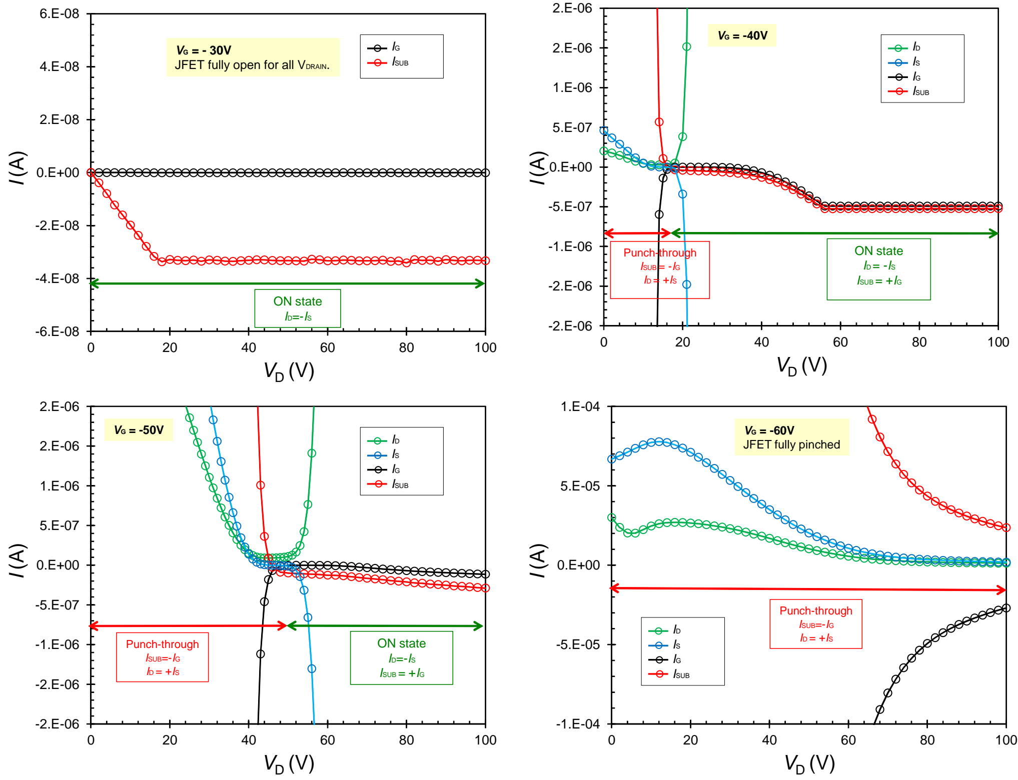

Figure 8.5: $I_D(V_D)$ characteristics of high-voltage dual-gate JFET measured for various V_G – zoom to lower currents.

voltage and the channel is not yet pinched. This situation was described in previous section, Fig. 8.1. The current flows from drain to source and therefore they have opposite directions: $I_D = -I_S$ as it is demonstrated in Fig. 8.4a. The top gate current is equal to zero, $I_G = 0\,\text{A}$, the substrate current I_{SUB} is equal to leakage of wafer substrate to the chuck.

Plots in Fig. 8.4b and Fig. 8.5b with top gate voltage $V_G = -40\,\text{V}$ up to drain voltage around $V_D = 20\,\text{V}$ demonstrate JFET operating in OFF state (see Fig. 8.2). In this area the vertical punch-through appears and the current flows from the top gate to the substrate ($I_G = -I_{SUB}$), while the drain and source currents have the same direction – see Fig. 8.5b. This is in agreement with Fig. 8.2 in previous section.

Plots in Fig. 8.4b and Fig. 8.5b for larger drain voltage demonstrates the lateral punch-through (Fig. 8.3), which behaves like the operation in ON state: current flows mainly from drain to source, and much smaller gate and substrate currents then represent the impact ionization. This “ON state” however appears only for drain voltages larger than the critical voltage – in this case around $V_D = 20\,\text{V}$, where the lateral field breaks the pinched channel.

Increasing top gate voltage increases vertical electrical field, so a larger critical drain voltage is then required to create the lateral punch-through and make the JFET behave like in ON state.

Plots in Fig. 8.4c and Fig. 8.5c demonstrate situation with top gate voltage $V_G = -50\,V$, where the critical drain voltage around $V_D = 50\,V$ is required to make the JFET behave like in ON state.

And finally plots in Fig. 8.4d and Fig. 8.5d demonstrate situation with top gate voltage $V_G = -60\,V$, where the critical drain voltage of more than 100 V is required to make the JFET behave like in ON state.

JFET pinch-off voltage is typically expected to be a constant, however in this particular case (dual-gate JFET with the top gate covering only a small part of JFET body – see Figs. 8.1–8.3) the pinch-off voltage is dependent on the potential of all four JFET terminals. Therefore the modeling of such device is very challenging [5, 4]. Even so, the pinch-off voltage is stable for the defined operating conditions, so it can be used as a parameter for required design. On the other hand, the process distribution of this parameter is relatively high [5].

8.5 Conclusions

This chapter shares experimentally measured data of a high-voltage dual-gate JFET. Due to its special layout this device has a specific behavior, which was measured, described and explained. Demonstrative cross-sections and plots with all measured terminal currents were used to clarify the seemingly anomalous observed phenomena.

As the high-voltage dual-gate JFET serves as a key part of contemporary power supply equipment for hundreds of millions RF circuits, such as mobile phones, tablets, etc., fully understanding its various operating modes is very important.

The main contribution of this chapter is the opening new fields, where the dual-gate JFET model development can continue.

The new ideas described in this chapter were approximately 95% author's own.

CHAPTER 9

Conclusion

The highest scientific contribution of this thesis indisputably consists in the introduction of a very complex dual-gate JFET model, which was and still is the missing component in common SPICE simulators. Although some new publications presenting alternative solutions appeared recently, the model published in journal Solid-State Electronics [5] and described mainly in Chapter 3 of this thesis sets in many ways the direction of future development, which is proved by frequent citations [63, 64, 17, 30].

The developed behavioral model can be used either as a stand-alone model of dual-gate/single-gate JFET or as a part of a complex macromodel, for example, as a drift area of high voltage FET in combination with PSP [20], HiSIM [34] or BSIM4 [62] compact MOSFET models.

Another very valuable scientific contribution of this thesis is made by the introduction of a reverse recovery diode model created in cooperation with University of Washington, published also in Solid-State Electronics journal [6] and described in Chapter 6. The reverse recovery module can be used either as a stand-alone diode model or as a part of complex macromodel, for example in BJT, MOSFET or mentioned dual-gate JFET model.

The following points provide a comparison of presented models with similar published models:

- The dual-gate JFET compact model does not exist in any commercial simulator yet. The presented model is therefore the only solution for the simulation of technology containing such device.
- Most JFET models published before the publication of this work [61, 57, 58, 35] have been focused on DC parameters only. The presented model proposes a more complete and universal solution covering most of required phenomena for real production designs. The core of the

model is described in the chapter Comprehensive Behavioral Model of Dual-Gate High Voltage JFET and Pinch Resistor, where the modeling results are divided into the following sections:

- DC model: Implementation of second gate, improving bias and geometry scaling of pinch-off voltage for both JFET gates considering various layout of the device.
- Capacitance Model: Implementation of pinching factor in the gate capacitance for both independent gates considering various layout of the device.
- Parasitic DC model, Gate Current: Implementation of parasitic leakage and impact ionization currents for both independent gates.
- Temperature Model: Improved temperature model by adding more temperature parameters considering all the new effects added to the model.
- Statistical Model: Implementation of statistical parameters for the simulation of process distribution. The model development and the parameter extraction have been based on real production statistical data.

The reverse recovery effect is described in another chapter, because it was researched and published separately.

- The chapter Techniques of HV JFET Gate Capacitance Modeling contains a complex guide taking into account various device variants. Such complex manual was not found in any other publication or SPICE manual.
- RF models of various SPICE MOSET compact models contain the RC network modeling parasitic polysicion gate resistance, the impact of parasitic inductance is however missing. The chapter Lumped RF Model of MOSFET Gate Resistance for GHz+ Frequencies gives an example of modeling this effect.
- Although there exist many publications about reverse recovery modeling, the most of published models are not usable for production design, mainly due to the insufficient convergence. The model presented in the chapter Accurate Diode Behavioral Model with Reverse Recovery fills this gap – the model has already been used in several production designs. However, during the work on the model, the new version of Eldo simulator presented diode reverse recovery model very similar to the presented one. The contribution of the presented model is the implementation of high injection current parameters and mainly its usability in all simulators supporting Verilog-A.

- The chapter Implementation of Bi-modal Statistical Distribution into SPICE Models presents the original concept how to implement bi-modal statistical distribution to the model. Author did not find any publication describing this topic.

- The chapter New Challenges – Anomalous Phenomena in HV JFET Channel Pinching opens new fields, where the dual-gate JFET model development can continue.

The contribution of the thesis is proved by the number of citations of published articles, especially the main article Comprehensive Behavioral Model of Dual Gate High Voltage JFET and Pinch Resistor cited 4× in last two years. The total number of authors citations is 10 – see the chapter List of candidate's work.

The model was implemented into main commercial simulators supporting Verilog-A (Eldo, Spectre, HSpice) and can be used in circuits from various areas of electrical design, such as analog, digital, signal processing or RF circuits.

The model verification was realized in several real designs, for example a DC-DC converter [43] or Secondary Side Synchronous Rectification Driver [44]. The large set of data measured in various components in various configurations was used for the verification. Some examples of the comparison between measured characteristics and simulated data are presented in this thesis. The model has very good convergence and simulation speed. During the verification and real application no convergence issue was observed. The model has continuous first derivative of simulated characteristics which is generally important in computer-aided design.

The most of new ideas described in this thesis are at least 80% author's own. Author's ratios of participation in the relevant publications are 30–50% depending on the topic. For details about the author's participation in this work see conclusions in chapters 3–8.

Chapters 3–8 were presented either in impacted journals excerpted in Web of Science or in international conferences. Author of this thesis is the first author of all these publications.

Author moreover participated in some other publications in impacted journals not published in this thesis as it is demonstrated in Appendix A.

The participation in impacted journals excerpted in Web of Science and not published in this thesis is 35% for [A4], 18% for [A3] and 10% for [A0].

The participation in papers excerpted in Web of Science and not published in this thesis is 35% for [B3], and and 10% for [B2].

The participation in papers in reviewed journals and not published in this thesis is 50% for [C3].

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Appendix A: List of Candidate's Works

List of Candidate's Works Relating to the Doctoral Thesis

Papers in Impacted Journals Excerpted in Web of Science

[A0] D.Černý, J.Dobeš, S.Banáš. Efficient Procedure Improving Precision of High Conditioned Matrices in Electronic Circuits Analysis. *Radioengineering, vol. 27, no. 4, p. 1100-1111, December 2018.*

[A1] S.Banáš, J.Divín, J.Dobeš, V.Paňko. Accurate Diode Behavioral Model with Reverse Recovery. In *Solid-State Electronics, vol. 139, pp. 31-38, 2018.* [http://www.sciencedirect.com/science/article/pii/S0038110117304872]

[A2] S.Banáš, V.Paňko, J.Dobeš, P.Hanyš, J. Divín. Comprehensive Behavioral Model of Dual Gate High Voltage JFET and Pinch Resistor. In *Solid-State Electronics, vol. 123, pp. 133-142, 2016.* [http://www.sciencedirect.com/science/article/pii/S0038110116300326]

[A3] V.Paňko, S.Banáš, R.Burton, K.Ptáček, J.Divín, J. Dobeš. Enhanced Model of Nonlinear Spiral High Voltage Divider, *Radioengineering*. 2015, vol. 24, no. 1, p. 130-136. ISSN 1210-2512. [http://www.radioeng.cz/fulltexts/2015/15_01_0130_0136.pdf]

[A4] V.Paňko, S.Banáš, D.Prejda, J.Dobeš. MOSFET Gate Dimension Dependent Drain and Source Leakage Modeling by Standard SPICE Models. In *Solid-State Electronics*, Volume 81, March 2013, Pages 144–150 [http://www.sciencedirect.com/science/article/pii/S0038110113000075]

Papers Excerpted in Web of Science

[B1] S.Banáš, M.Brzobohatý, J.Dobeš. Implementation of Bi-modal Statistical Distribution into SPICE Models. In: 2017 Progress in Electromagnetics Research Symposium - Fall (PIERS - FALL)*, Singapore, 2017, pp. 2914-2919.* [http://ieeexplore.ieee.org/document/8293630/]

[B2] J.Dobeš, V.Paňko, S.Banáš, D.Černý. An Improved Model of High-Voltage Power LDMOSFET and Its Usage in Multi-Objective Optimization of Radio-Frequency Amplifiers. In *Proceedings of the 14th IEEE WORKSHOP ON CONTROL AND MODELING FOR POWER ELECTRONICS (COMPEL)*, Salt Lake City, USA, 2013 [http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6467635&contentType=Conference+Publications] [http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6626472&isnumber=6626389]

[B3] V.Paňko, S.Banáš, K.Ptáček, R.Burton, J.Dobeš. An Accurate DC and RF Modeling of Nonlinear Spiral Polysilicon Voltage Divider in High Voltage MOSFET Transistor. In *Proceedings of the 11th IEEE International Conference on Solid-State and Integrated Circuit Technology, Xian, 2012* [http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6467635&contentType=Conference+Publications]

[B4] J.Slezák, A.Litschmann, S.Banáš, R.Mlčoušek, M.Kejhar. On the correlations between model process parameters in statistical modeling. In *2004 NSTI Nanotechnology Conference and Trade Show.* Boston, 2004. ISBN 0972842284. [http://nsti.org/publications/Nanotech/2004/pdf/B2-33.pdf]

Papers in Reviewed Journals

[C1] M.Skalský, S.Banáš, V.Paňko. A resistance model of integrated octagonal-shaped Hall sensor using JFET compact model. Proceedings of the 2017 IEEE International Conference on IC Design and Technology, ICICDT 2017. art. no. 7993510. [http://ieeexplore.ieee.org/abstract/document/7993510/]

[C2] S.Banáš, J.Dobeš, V.Paňko. Techniques of JFET Gate Capacitance Modeling. Proceedings of the World Congress on Engineering and Computer Science 2016 Vol II, WCECS 2016. [http://www.iaeng.org/publication/WCECS2016/WCECS2016_pp771-775.pdf]

[C3] S.Banáš, V.Paňko, V.Stejskal, J.Slezák, J.Dobeš. Universal behavioral model for accurate modeling of high voltage devices. WIT Transactions on Information and Communication Technologies. 2014, vol. 60, p. 545-551. ISSN 1743-3517. [http://www.witpress.com/elibrary/wit-transactions-on-information-and-communication-technologies/60/31841]

Other Publications

[D1] S.Banáš, C.Hoggatt, V.Paňko, J.Dobeš, J.Divín. Lumped RF Model of MOSFET Gate Resistance for GHz+ Frequencies. In *Proceedings of the IPCT2015 Information Processing and Communication Technology*, Roma, 2015 [http://www.ipct.theired.org]

[D2] S.Banáš, J.Dobeš, V.Paňko. Anomalous Phenomena in Ultra High Voltage JFET Channel Pinching. In *28th International Conference Radioelektronika.* Prague, 2018, pp. 1-4. [https://ieeexplore.ieee.org/document/8376349].

[D3] S.Banáš, D.Prejda. Modeling of gate length dependent leakage in MOSFETs. In *MOS-AK/GSA Workshop.* Rome, 2010. [http://ebookbrowse.com/p07-banas-mos-ak-rome-pdf-d77162700] Poster.

[D4] S.Banáš, V.Stejskal, J.Slezák. Modeling of very low doped and pinched resistors. In *MOS-AK/ESSDERC/ESSCIRC Workshop.* Montreaux, 2006. [http://www.mos-ak.org/montreux/posters/12_Banas_MOS-AK06.pdf] Poster.

[D5] J.Slezák, P.Kahánek, S.Banáš, M.Kejhar. Statistical modeling: role and position in semiconductor industry. In *MOS-AK/ESSDERC/ESSCIRC Workshop.* Montreaux, 2006. [http://www.mos-ak.org/montreux/posters/13_Slezak_MOS-AK06.pdf] Poster.

List of Other Candidate's Works

Papers Excerpted in Web of Science

[E0] J. Dobeš, J. Michal, S. Banáš. Accurate Semisymbolic Analysis with Usage of 128-bit Arithmetics. In: *2018 IEEE Radio and Antenna Days of the Indian Ocean (RADIO).* IEEE, 2018. p. 1-2.

Other Publications

[F1] D.Prejda, J.Slezák, S.Banáš. Modeling of parasitic phenomena in trench technology. In *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), 2011.* Gliwice, 2011. s. 95 - 98, ISBN 978-1-4577-0304-1. [http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6016043&contentType=Conference+Publications&sortType%3Dasc_p_Sequence%26filter%3DAND%28p_IS_Number%3A6015915%29%26rowsPerPage%3D50]

[F2] J.Fulton, W.Fagale, S.Banáš, M.Imam. Measurement of mobility in power trench FET technology using the conductance and transconductance methods. In *22nd International Conference on Microelectronics, 2000.* Nis, 2000. s. 649 - 652, vol.2. ISBN 0-7803-5235-1. [http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=838774&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D838774]

[F3] V.Marek, S.Banáš, P.Horvath, J.Slezák. Challenges in modeling a power lateral PNP device. In *MOS-AK/GSA Workshop.* Dresden, 2012. [http://www.mos-ak.org/Dresden] Poster.

[F4] M.Skalský, D.Prejda, J.Slezák, S.Banáš. Vertical PNP transistor TCAD simulation. In *MOS-AK/ESSDERC/ESSCIRC Workshop.* Edinburgh, 2008. [http://www.mos-ak.org/edinburgh/posters/P06_Skalsky_MOS-AK_08.pdf] Poster.

Responses and Reviews

Citations

Paper [A2]

Comprehensive behavioral model of dual-gate high voltage JFET and pinch resistor
By: Banas, Stanislav; Panko, Vaclav; Dobes, Josef; et al.
SOLID-STATE ELECTRONICS Volume: 123 Pages: 133-142 Published: SEP 2016

IS CITED IN

JFETIDG: A Compact Model for Independent Dual-Gate JFETs With Junction or MOS Gates
By: Xia, Kejun; McAndrew, Colin C.
IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 65 Issue: 2 Pages:
747-755 Published: FEB 2018

AND IS ALSO CITED IN

JFETIDG: A Compact Model for Independent Dual-Gate JFETs
By: Xia, Kejun; McAndrew, Colin C.; Sheng, Hanyu
Conference: IEEE Electron Devices Technology and Manufacturing Conference (EDTM) Location:
Toyama, JAPAN Date: FEB 28-MAR 02, 2017
Sponsor(s): IEEE; IEEE Elect Devices Soc
2017 IEEE ELECTRON DEVICES TECHNOLOGY AND MANUFACTURING CONFERENCE
(EDTM) Pages: 124-125 Published: 2017

AND IS ALSO CITED IN

CMOS-Integrated Low-Noise Junction Field-Effect Transistors for Bioelectronic Applications
By: Fleischer, D. A., Shekar, S., Dai, S., Field, R. M., Lary, J., Rosenstein, J. K., & Shepard, K. L.
IEEE Electron Device Letters, 2018.

AND IS ALSO CITED IN

A Compact Model for Static and Dynamic Operation of Symmetric Double-Gate Junction FETs
By: Nikolaos Makris, Matthias Bucher, Farzan Jazaeri, Jean-Michel Sallese
48th European Solid-State Device Research Conference (ESSDERC). IEEE, 2018. p. 238-241.

Paper [A4]

MOSFET gate dimension dependent drain and source leakage modeling by
standard SPICE models
By: Panko, Vaclav; Banas, Stanislav; Prejda, Dusan; et al.
SOLID-STATE ELECTRONICS Volume: 81 Pages: 144-150 Published: MAR 2013

IS CITED IN

Analysis and modeling of zero-threshold voltage native devices with
industry standard BSIM6 model
By: Gupta, Chetan; Agarwal, Harshit; Lin, Y. K.; et al.
JAPANESE JOURNAL OF APPLIED PHYSICS Volume: 56 Issue: 4 Special Issue:
SI Article Number: 04CD09 Published: APR 2017

AND IS ALSO CITED IN

Modeling and analysis of sub-surface leakage current in nano-MOSFET

under cutoff regime
By: Swami, Yashu; Rai, Sanjeev
SUPERLATTICES AND MICROSTRUCTURES Volume: 102 Pages: 259-272
Published: FEB 2017

AND IS ALSO CITED IN

Modeling of Subsurface Leakage Current in Low V-TH Short Channel MOSFET at Accumulation Bias
By: Lin, Yen-Kai; Khandelwal, Sourabh; Medury, Aditya Sankar; et al.
IEEE TRANSACTIONS ON ELECTRON DEVICES Volume: 63 Issue: 5 Pages: 1840-1845 Published: MAY 2016

Paper [B4]

On the correlations between model process parameters in statistical modeling.
By Slezak, J., Litschmann, A., Banas, S., Mlcousek, R., Kejhar, M.
Conference: *2004 NSTI Nanotechnology Conference and Trade Show.*
Location: Boston Massachusetts, USA, 2004. ISBN 0972842284.

IS CITED IN

Circuit statistical modeling for partially correlated model parameters
By: Bittner, C. J., Grundon, S. A., Lee, Y., Lu, N., Watts, J. S. US patent 7640143 B2, 2009.
[http://www.google.cz/patents?hl=cs&lr=&vid=USPAT7640143&id=lDTLAAAAEBAJ&oi=fnd&printsec=abstract#v=onepage&q&f=false]

Paper [C1]

A resistance model of integrated octagonal-shaped Hall sensor using JFET compact model
By: Skalsky, M.; Banas, S.; Panko, V.
Conference: 2017 IEEE International Conference on IC Design and Technology (ICICDT)
Location: Austin, Texas, USA Date: May, 2017
2017 IEEE INT C IC D Pages: 1-4 Published: 2017

IS CITED IN

A One-Dimensional Magnetic Chip with a Hybrid Magnetosensor and a Readout Circuit
By: Sung, Guo-Ming; Wang, Hsin-Kwang; Gunnam, Leenendra Chowdary JOURNAL OF SENSORS
Article Number: 6436481 Published: 2018

Paper [C2]

Techniques of JFET Gate Capacitance Modeling.
By: S. Banáš, J. Dobeš, V.Paňko.
Conference: 2016 World Congress on Engineering and Computer Science (WCECS).
Location: San Francisco, California, USA Date: October, 2016

IS CITED IN

Charge-Based Modeling of Long-Channel Symmetric Double-Gate Junction FETs—Part II: Total Charges and Transcapacitances
By: Makris, N., Jazaeri, F., Sallese, J. M., & Bucher, M.
IEEE Transactions on Electron Devices 65.7 (2018): 2751-2756

Appendix B: Used Equipment and Software

Equipment Used for the Measurement

DC/CV Measurement Equipment - autoprober:

- Electroglas EG4090A Automatic Prober
- Thermochuck (-40C to 150C)
- Temptronic 315A temperature controller
- Test System Agilent 4072
- RLC meter Agilent 4284A
- Multimeter Agilent 3458A (DVM)
- 4x Middle-power SMU, 1x High-power SMU, 1x High-voltage SMU
- Switching matrix

DC/CV Measurement Equipment - manual prober:

- Manual prober Karl Suss PM8
- Thermochuck (-40C to 200C)
- Temptronic 315A temperature controller
- Semiconductor Parameter Analyzer Agilent 4156B
- RLC meter Agilent 4284
- Modular DC Source up to 1000V Agilent 4142

AC Measurement Equipment - manual prober:

- Manual prober Cascade Microtech SUmmit 9000

- Thermochuck (-40C to 150C)
- Temptronic 315A temperature controller
- Vector Network Analyzer Agilent 8753E

Transient Measurement Equipment - manual prober:

- Pulse generator Agilent 81104A
- Oscilloscope Tektronix DPO 7104C
- Current probe Tektronix CT1

Used Software

- Cadence Virtuoso Layout
- Cadence Schematic Editor
- Mentor Graphics Layout
- Mentor Graphics Schematic Editor
- Model parameter extraction tool Agilent IC-CAP
- SPICE simulator Eldo
- SPICE simulator Spectre
- SPICE simulator HSpice
- Programming language Pearl
- Modeling language Verilog-A
- Matlab
- MS Office
- LaTex

Appendix D: Candidate's Short Curriculum Vitae

Personal Information:

Name	Stanislav
Surname	Banáš
Email	stanislav.banas@onsemi.com

Education:

2012-Present	**PhD Student in Microelectronics** Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radioelectronics
1989-1994	**Master's degree in Microectronics** Technical University in Brno, Faculty of Electrical Engineering, Departmentof Microelectronics. Thesis: Study of the optoelectronic properties of hydrogenated amorphous silicon layers (see Internship)

Experience:

1996-Present	**Senior Principal Modeling and Characterization Engineer**, ON Semiconductor, SCG Czech Design Center, s.r.o., Rožnov pod Radhoštěm.

Internship:

1994	Scholarship in CNRS institute in Grenoble, France. Thesis: Study of the optoelectronic properties of hydrogenated amorphous silicon layers. The thesis defended for international committee.

Languages:

English	Fluent
Russian	Fluent

Certifications:

2018	Real Modeling with Verilog AMS (Cadence)
2014	Eldo Simulation (Mentor Graphics)

2013	IC Design with Pyxis (Mentor Graphics)
2013	TCAD Synopsis (ON Semiconductor)
2010	Analog Modeling and Simulation with Spice (Cadence Design Systems)
2010	Visual Basic (ON Semiconductor VPS)
2010	MOS-AK/GSA (Sapienza Universita di Roma)
2009	Prezentační dovednosti (Wojtovič Adam-ESCHOLA)
2007	Advanced Analog CMOS IC Design (Swiss Federal Institute of Technology in Lausanne, Switzerland)
2007	Behavioral Modeling with Verilog (Cadence Design Systems)
2005	Six Sigma - Green Belts (ON Semiconductor VPS)
2005	Jump (ON Semiconductor VPS)
2004	Virtuoso XL Layout Editor (Cadence Design Systems)
2004	Device Simulations Using ISE (Vobecký, Voves, ČVUT Praha)
2004	Verilog-A (Deinshop C.)
2004	SPICE training (Vladimirescu, A.)
2000	RF measurement and parameter extraction (Agilent)
1999	EG Commander software (Electroglas)
1999	Effective presentation (Inventura Manager Prog)

Skills:

Prog.Languages	Perl, LaTeX, Turbo Pascal
Sim. Languages	Spice, HSpice, Eldo, Spectre, ADMS, Verilog-A
Design Tools	Cadence, Mentor, Calibre
Other Tools	TCAD (Synopsys), Matlab, IC-CAP

Appendix C: Permission Grants

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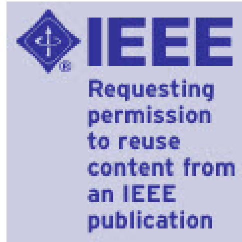

Title: High voltage thin layer devices (RESURF devices)

Conference Proceedings: Electron Devices Meeting, 1979 Internationa

Author: Appels, J.A.; Vaes, H.M.J.

Publisher: IEEE

Date: 1979

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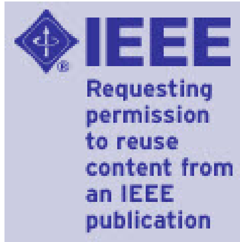

Title: Combined Lateral Vertical RESURF (CLAVER) LDMOS structure

Conference Proceedings: Power Semiconductor Devices & IC's, 2009. ISPSD 2009. 21st International Symposium on

Author: Khan, T.; Khemka, V.; Ronghua Zhu; Weixiao Huang; Xu Cheng; Hui, P.; Muh-ling Ger; Grote, B.; Rodriquez, P.

Publisher: IEEE

Date: 14-18 June 2009

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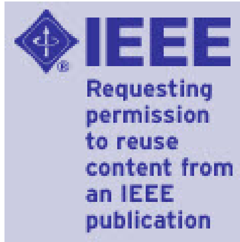

Title: SOA improvement by a double RESURF LDMOS technique in a power IC technology

Conference Proceedings: Electron Devices Meeting, 2000. IEDM '00. Technical Digest. International

Author: Parthasarathy, V.; Khemka, V.; Zhu, R.; Bose, A.

Publisher: IEEE

Date: 10-13 Dec. 2000

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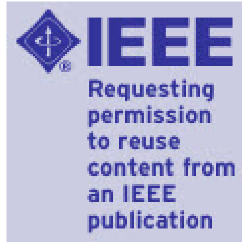

Title: Dielectric resurf: breakdown voltage control by STI layout in standard CMOS

Conference Proceedings: Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International

Author: Sonsky, J.; Heringa, A.

Publisher: IEEE

Date: 5-5 Dec. 2005

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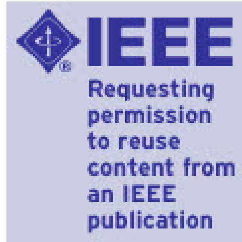

Title: State-of-the-art device in high voltage power ICs with lowest on-state resistance

Conference Proceedings: Electron Devices Meeting (IEDM), 2010 IEEE International

Author: Su, R.Y.; Yang, F.J.; Tsay, J.L.; Cheng, C.C.; Liou, R.S.; Tuan, H.C.

Publisher: IEEE

Date: 6-8 Dec. 2010

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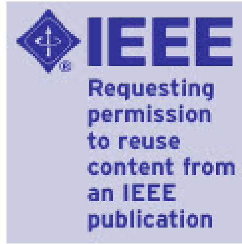

Title: Accurate spice modeling of 80V power LDMOS with interdigitated source structure

Conference Proceedings: Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on

Author: Tamegaya, Y.; Koh, R.; Hatanaka, Y.; Iizuka, T.

Publisher: IEEE

Date: 3-7 June 2012

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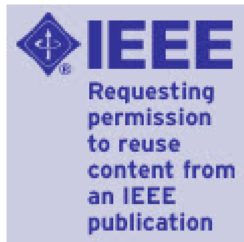

Title: High voltage, high current lateral devices

Conference Proceedings: Electron Devices Meeting, 1980 International

Author: Vaes, H.M.J.; Appels, J.A.

Publisher: IEEE

Date: 1980

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