ZATPG: SAT-based ATPG for Zero-Aliasing Compaction

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Abstract

One of long-standing problems in digital circuit testing is a fault aliasing in the response compaction. Fault aliasing is an important source of coverage loss, especially if we strive to achieve high compaction ratio. Existing methods to lower or eliminate aliasing mostly require changes to the compactor design. This can lead to a higher compactor complexity, bigger area overhead, longer propagation paths, etc.

We propose a method to eliminate aliasing without the need to modify the compactor design. The basic idea is to constrain the test pattern generation itself to produce a test with zero aliasing. This is in contrast to previous methods, where a test is computed independently and anti-aliasing algorithm does not modify test further [1, 2]. Some anti-aliasing algorithms exert a partial control over a test sequence, by reordering (already existing) test [3–5].

Note that we are only considering aliasing in a temporal compactor. Preventing aliasing in a spatial compactor is much easier problem, for both pre-existing and new test set. In our paper, we assume a spatial compactor that does not introduce new redundant faults.

1.1 Constraining the ATPG

Our method, ZATPG (zero-aliasing test patterns generator), is based on a SAT-based (Boolean satisfiability) ATPG (automated test patterns generator) [6]. Conventional SAT-ATPG works by modelling a fault as a replica of the CUT, transforming the miter to a CNF (conjunctive normal form), and solving the resulting CNF-SAT problem with a SAT solver [7].

We then expand the miter by introducing anti-aliasing constraints in following way. First, we construct miter as usual, consisting of the fault-free circuit and circuit with a tested fault f_i and find a test pattern p_i to detect f_i. Additionally, we insert selected faults $f_{s,1}$–$f_{s,m}$, modelled in their own replicas of the CUT. (Figure 1)

Aliasing happens only *after* the application of test pattern that causes it. It is therefore necessary to know the future state of compactor during the generation of test pattern p_i. This is achieved by unrolling combinational part of the compactor (block *MISR* in the Figure 1). Previous state of the compactor also needs to be supplied ($S_f f$,S_1–S_m) and output (next state, partial signature) is constrained to differ from the state for the fault-free circuit.

1.2 Results

For experiments, we have used slight simplification possible for linear compactors (for details see [8]). The experiment were performed on benchmark circuits from the ISCAS'85 and selected ITC'99 bench-

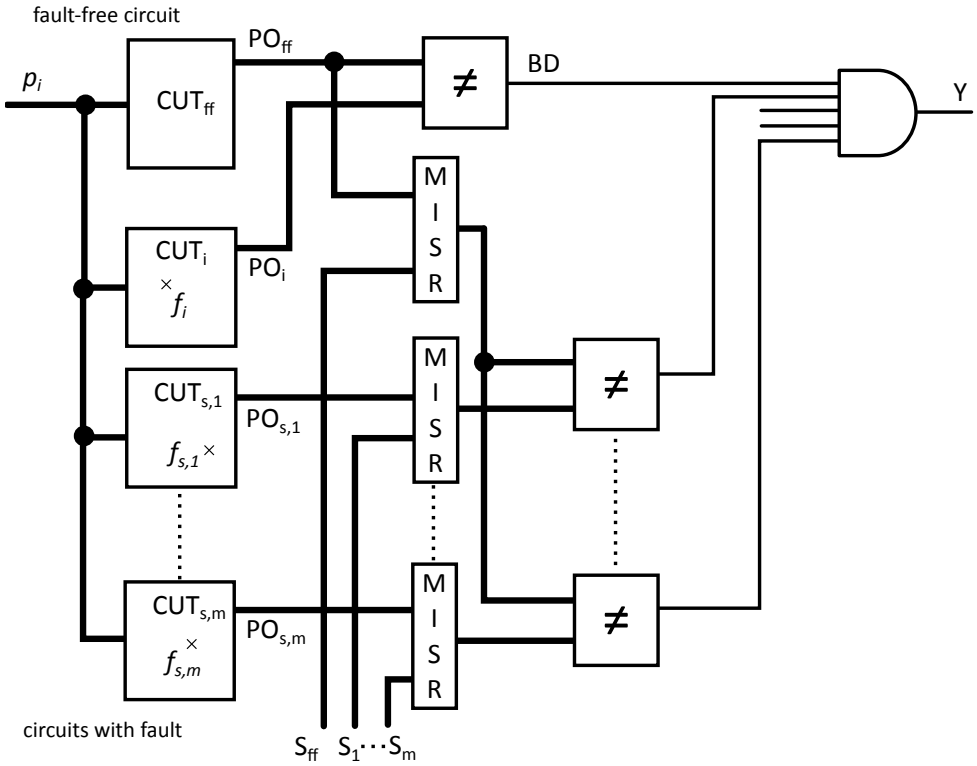

Figure 1: Extended miter for zero-aliasing in compaction

marks.

For all tested circuits, we have achieved zero aliasing (full coverage) with ZATPG for smaller compactors of same design (LFSR) than with normal ATPG. The observed gain was between 2 and 5 bits of LFSR saved. With the exception of the circuit c7552, where the achieved LFSR size was same as with ATPG.

Paper origin

This paper has been accepted and presented at the conference Euromicro DSD/SEAA 2017, Vienna, Austria [8].

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