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OPTIMIZATION OF POWER MOSFET DEVICES SUITABLE FOR INTEGRATED CIRCUITS

Doctoral Thesis

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Declaration

I declare I have completed my expert study on my own with the contribution of my supervisor and consultants. I used only materials (literature, projects, articles) specified in the attached list.

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In Prague, 25th January 2019 Patrik Vacula

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Abstract

This doctoral thesis deals with the design of lateral power transistor with lower specific on-resistance for integration into IC.

The new model of MOSFET with waffle gate pattern is there described. For first, time the conformal transformation the Schwarz-Christoffel mapping has been used for the description of nonhomogeneous current distribution in the channel area of MOSFET with waffle gate pattern. In addition base on the figure of merit definition Area Increment (AI) the topological theoretical limit of MOSFET with waffle gate pattern has been a first time defined.

The more precise model with bulk-segmented power MOSFET with waffle gate patterns is described this doctoral thesis. A new model of MOSFET with waffle gate pattern and with orthogonal source and drain interconnections and with considering edge element due to bulk-segmentation has been the first time describe. Moreover, there has been defined conditions, where bulk-segmented power MOSFETs structures with waffle gates occupy smaller area compared to standard MOSFETs without increasing channel resistance.

To improve the channel resistance of HV power GaN HEMT the new topologies have been proposed and are described. In addition, the production cost of GaN HEMT can be reduced by decreasing chip area and by it yield improvement. The standard waffle gate pattern and proposed two new gate patterns the dissimilar square waffle and octagon waffle pattern can apply for any lateral normally-On or normal-Off GaN HEMT processes. New proposals are lateral structures and due to this are perspectives for integration into power management integrated circuits on GaN substrates.

New methodologies to reduce physical design development time and cost for smart power IC is present. To optimized analog layout implementation flow for smart power IC, the several improvements have been developed and are used at STMicroelectronics. The new automatic pre-placement phase of flow has been a first time defined, to simplify and speed up analog and mixed-signal (AMS) layout. The new and more time effective way of objects modification in the layout database has been defined. In addition, the new and more time effective searching flow in layout and schematic database have been developed and is presented.

Keywords: power MOSFET, GaN HEMT, waffle pattern, integrated circuit, physical design of analog and mixed-signal circuits

Abstrakt

Táto doktorská práca sa zaoberá návrhom laterálnych výkonových tranzistorov s nízkym špecifickým odporom pri zapnutom stave, vhodných pre integráciu do Integrovaných Obvodov.

Je tu popísaný nový model MOSFET tranzistora s mriežkovou hradlovou elektródou. Prvý krát bola použitá konformná Schwarz-Christoffelova transformácia pre popis nehomogénne rozloženého prúdu v oblasti kanála MOSFET tranzistora s hradlovou elektródou mriežkového vzoru. Navyše na základe kvalitatívneho parametra Prírastok Plochy (AI), bol prvýkrát zadefinovaný teoretický, topologický limit pre MOSFET tranzistor s hradlovou elektródou mriežkového vzoru.

V tejto práci je popísaný presnejší model pre MOSFET tranzistor s hradlovou elektródou mriežkového vzoru, ktorý je delený kontaktovaním substrátu. Prvýkrát bol popísaný nový model pre MOSFET tranzistor s hradlovou elektródou mriežkového vzoru s ortogonálnym prepojením source a drain elektród s uvažovaním okrajových elementov delených kontaktovaním substrátu. Boli zadefinované podmienky, kedy substrátom predelené výkonové MOSFET štruktúry s mriežkovým hradlom zaberajú menšiu plochu v porovnaní so štandardnými MOSFET tranzistormi, bez navýšenia odporu.

Na zlepšenie odporu kanála vysokonapäťových výkonových GaN HEMT tranzistorov, boli navrhnuté a zadefinované nove topológie. Okrem toho výrobná cena GaN HEMT môže byť redukovaná zmenšením plochy čipu, ktorá zároveň zlepší i výťažnosť. Štandardný mriežkový hradlový vzor a dve nové hradlové vzory, mriežkový s rôznymi štvorcami a oktagonálny mriežkový hradlový vzor, môžu byť použité pre ľubovoľný výrobný proces normálne zapnutého alebo normálne vypnutého GaN HEMT tranzistora. Nové navrhnuté tvary sú laterálne, a preto sú vhodné pre integráciu do výkonových GaN integovaných obvodov.

Na optimalizáciu analógového fyzického návrhu v moderných výkonových Integrovaných Obvodov bolo vyvinutých viacero vylepšení, ktoré sú používané vo firme STMicroelectronics. Nový automatický postup na triedenie súčiastok, rovnako ako i nový, a viac efektívny spôsob modifikácie objektov databáze fyzického návrhu, a zároveň i nový a efektívnejší spôsob vyhľadávania v databázach pomáhajú zjednodušovať a zefektívňovať fyzický návrh.

Kľúčové slová: výkonový MOSFET, GaN HEMT, mriežkový vzor, integrovaný obvod, fyzický návrh analógových a zmiešaných obvodov

“Imagination is more important than knowledge.”

Albert Einstein

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List of Acronyms

A	– Homogenous channel element
B	– Non homogenous cross channel element
BCD	– Bipolar CMOS DMOS process
BGCT	– Bi-mode Gate Commutated Thyristor
BV	– Breakdown Voltage
CMOS	– Complementary (PMOS, NMOS) MOS process
CoolMOS^{TM}	– Super Junction MOSFET transistor developed by Infinion
D	– Drain terminal of transistor
DMOS	– Double diffusion MOS transistor
DIE	– IC area (Chip)
Fin-FET	– Fin channel Field Effect Transistor
G	– Gate terminal of transistor
GAA FET	– Gate All Around Field Effect Transistor
HCI	– Hot Carrier Injection
HEMT	– High Electron Mobility Transistor
HexFET	– Hexagonal gate pattern Field Effect Transistor
HV	– High Voltage
IC	– Integrated Circuit
IGBT	– Isolated Gate Bipolar Transistor
LDD	– Low Doped Drain
LDMOS	– Lateral Double diffusion MOS transistor
LV	– Low Voltage
MOS	– Metal Oxide Semiconductor transistor
MOSFET	– Metal Oxide Semiconductor Field Effect Transistor
NMOS	– N (negative) type channel Metal Oxide Semiconductor transistor
N-well	– N (negative) type well doping
PMOS	– P (positive) type channel Metal Oxide Semiconductor transistor
P-well	– P (positive) type well doping
RESURF	– REduced SURface Field effect on silicon/oxide interface
S	– Source terminal of transistor
Salicide	– Self-aligned silicide (metal to semiconductor formation process)
SAS	– Slovak Academy of Science
SCR	– Silicon Controlled Rectifier (Thyristor)
SJ-MOSFET	– Super Junction MOSFET
STI	– Shallow Trench Isolation
TCAD	– Technology computer aided design
UMOSFET	– U-grooved MOSFET Transistor (Trench gate Transistor)
VDMOS	– Vertical Double diffusion MOS transistor
XtreMOS^{TM}	– Specific hexagonal gate pattern MOS Field Effect Transistor
2DEG	– Two Dimensional Electron Gas effect
2DHG	– Two Dimensional Hole Gas effect

List of Symbols

a	– Acceleration [m/s^2]
A	– Area [m^2]
AI	– Area Increment [-]
AI_C	– Area Increment based on core area [-]
A_P	– Area of regular polygon [μm^2]
BV	– Breakdown Voltage [V]
C_D	– Contact dimensions [μm]
C_S	– Contact spacing [μm]
E	– Electrical field [V/m]
E_C	– Critical electrical field [V/m]
F	– Force [N]
L	– Length of the channel [μm]
L_{POLY}	– Y axis dimension of polysilicon gate [μm]
n	– Number of sides of regular polygon [-]
N_A	– Acceptors doping concentration [1/cm^3]
N_D	– Donors doping concentration [1/cm^3]
N_X	– Number of gates fingers in X-axis [-]
N_Y	– Number of gates fingers in Y-axis [-]
P_P	– Perimeter of regular polygon [μm]
P_{POLY}	– Total perimeter of polysilicon gate [μm]
Ron	– Resistance of transistor in ON (conductive) state [Ω]
sRon	– Specific resistance of transistor in ON state on area [mΩ cm^2]
S_{POLY}	– Gate polysilicon space [μm]
q	– Electron elementary charge 1.602 10^{-19}[C]
X_{POLY}	– X axis dimension of polysilicon gate [μm]
W	– Width of channel [μm]
ε	– Semiconductor permittivity [F/m]
ρ	– Space charge density [C/m^3]
ρ_S	– Semiconductor resistivity [Ω cm]
μ	– Permeability [H/m]
μ_n	– Electron mobility [cm^2/(V·s)]
μ_p	– Hole mobility [cm^2/(V·s)]
Φ	– Potential [V]

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1. Introduction

Due to new power management applications in fields like consumer electronics, telecommunication, transportation, and energetic there is a continuous need for more efficient power management. We stand today on the edge of new frontiers like are wearable electronics, mobile applications, wireless electric power transfer, electric cars, commercial space project, and renewable wind and solar energy. The progress in each of those fields are driven or are a link with power management improvements.

To explore future applications of microelectronics, we can use an analogy from the different technological field, as is engine development. The steam engine, which at the beginning drives the industrial revolution, was later, replace by gasoline engine technology. Mainly due to a much lighter and smaller gasoline engine, it was possible to build the first airplane. Without significant progress in the engine scaling and efficiency improvement compared to the steam engine the aircraft industry and aviation revolution would not begin. Similarly, in the microelectronics industry, the transistor scaling is described and driven by Moore's law. Smaller transistor dimensions bring new applications not possible by previous generations. For example, we can look how transistor scaling is changing the music industry and humans behavior in more than half century.

In the 1960s, started mass-produce pocket transistor radio and listeners get mobile device more compact compared to the bulky stationary home radio or heavy radio in the cars. In the late 1970s, Sony made Walkman, the portable, pocket-sized device to play custom music from cassette tapes. In the late 1980s, it was replaced with Discman, to play music from digitally recorded Compact Discs (CD). In the late 1990s, mp3-players was popular because had a more compact shape and store more songs due to the use of solid-state memories, and higher compression ratios respectively. In 2001, Apple introduced the iPod that allows storing more than 1000 CD-quality songs. Later mobile phones become the most common music player. Now streaming of music from clouded services with a mobile phone is the most common way to listen to music. It allows accessing all available songs on demand. In future still, addition miniaturization of smartphones hardware is required to allow its replacement with even more general

Augmented Reality (AR) smart glasses, capable of using Artificial Intelligence and Machine Learning, with processing from the devices rather than from cloud. That type of general-purpose human skills extension devices can allow for example professional custom music compositions for each user, offering not just content consumption but content creation also.

As was mentioned earlier in some examples, miniaturization brings not only price reduction but also allows more circuit functions per IC or application. There is continuous need to use smaller and smaller power MOSFET structures or to decrease the power MOSFET resistance without enlarging its area. There is a need to enlarge the voltage capabilities of power MOSFET structures in blockage state while minimalizing it influence on resistance in conductance state. There is also a need to improve the reliability over wider voltage, current, and temperature range or higher radiation. All of those needs are possible to reach by optimizing the power MOSFET layout, improving the process and using relevant materials.

On the field of power MOSFET components, the wide energy bandgap semiconductors are becoming more and more popular. Because there is continuous improvement of silicon-based devices, the silicon remains most common material for power MOSFETs currently. Advantages of silicon are very good process control (low density of crystal defects) and price per wafer (is cost-effective) allowing manufacturing of wafer size high power devices like IGCT or BGCT with thyristor-like conduction. Because the cost of wafer and process control is better for silicon than for SiC, GaN or Diamond even more complex and more costly architecture like XtreMOS [1] are feasible.

The increasing demand for high-power and high-temperature and high-frequencies operation of the power conversion and modulation systems brings traditional silicon semiconductor ever closer to its fundamental material limits [2]. Due to the rapid improvement of GaN material defects, the HEMT GaN power electronics is attracting interest due to wide bandgap (3.4 eV), which leads to a large critical electric field (3 MV/cm), reasonably high electron mobility good thermal conductivity (comparable to Si). To reach lower specific on-resistance of conventional HEMT GaN power transistors with multi fingers planar gate, it is proposed to use the waffle pattern planar gate. To sustain high voltage, two new waffle structures are proposed. Using Waffle planer gate pattern approach we can reach up to 40% lower specific on-resistance than by using a conventional gate with fingers pattern.

The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of all GaN power ICs. Next-generation monolithic integration (e.g. advanced I/O features, over-current and over-temperature protection) will enable even higher levels of efficiency, power density and reduced system cost. The power revolution of the late 1970s [3] will finally repeat today, 40 years later [4].

The dimension scaling of power transistors in smart power IC is very beneficial due to efficiency improvement of power IC or due to production costs reduction by decreasing chip area and by it yield improvement. To fulfill those expectation several lateral LV and HV waffle transistors are proposed, describe and model in this work.

1.1. Goals of This Thesis

The development of lateral power transistor with lower specific on-resistance is an actual topic. The main goals of this thesis are the following:

- Development of lateral power MOSFET transistor with lower specific on-resistance compares to standard finger gate MOSFET structure, for integration into current and future power management Integrated Circuits on Si substrates.
- Research of lateral power HEMT transistor with lower specific on-resistance compares to standard finger gate power HEMT topology, with perspectives for integration into future power management Integrated Circuits on GaN substrates.
- Research & Development of new methodologies to speed up processes of physical design in modern power IC, compare to standard physical design flows.

1.2. Organization of This Thesis

This thesis is organized as follows. The topic of this work together with descriptions of the author's contributions and state of the art are introduced in chapter 1 followed by a summary of power MOSFET fundamentals in chapter 2.

Analysis and comparison of different waffle MOSFET structures with standard MOSFET are presented in chapter 3. More advance models of waffle structures

considering edge element due to bulk-segmentation are shown and discussed in chapter 4.

New waffle structures dedicated to GaN HEMT are described in chapter 5. Additional transistor structures proposals are presented in chapter 6. The principles how to reduce physical design development time and cost for smart power IC is described in chapter 7. Finally, the work is concluded in chapter 8.

1.3. Author Scientific Contribution

The goals of this work are development, description, and improvement of power MOSFET or HEMT transistors with lower specific On-resistance with perspectives for integration into current and future power management Integrated Circuits on Si or GaN substrates.

More specifically, this work brings the following contributions:

- **The defined theoretical limit of waffle MOSFET and its new model by using Schwarz-Christoffel transformation**

  The new model of MOSFET with waffle gate pattern is described in chapter 3. For first, time the conformal transformation the Schwarz-Christoffel mapping has been used for the description of nonhomogeneous current distribution in the channel area of MOSFET with waffle gate pattern. In addition base on the figure of merit definition Area Increment (*AI*) the topological theoretical limit of MOSFET with waffle gate pattern has been a first time defined. This new model has been published in the reviewed journal ElectroScope [5] and waffle MOSFET theoretical limit has been published in the reviewed journal ElectroScope [6] and presented at international conferences [7], [8].

- **New waffle and finger structures models considering edge elements**

  The more precise model with bulk-segmented power MOSFET with waffle gate patterns is described in chapter 4. A new model of MOSFET with waffle gate pattern and with orthogonal source and drain interconnections and with considering edge elements due to bulk-segmented has been the first time describe. Moreover, there has been defined conditions, where bulk-segmented power MOSFETs structures with waffle gates occupy smaller area compared to standard MOSFETs without increasing channel resistance. All those models have been published in the impacted journal Radioengineering [9] (currently is in the review)

- **Defined new power GaN HEMT topologies**

  To improve the channel resistance of HV power GaN HEMT the new topologies have been proposed and are described in chapter.5. In addition production cost of GaN HEMT can be reduced by decreasing chip area and by it yield improvement. Those new architectures have been publish in the patents [10], [11].

- **New power trench MOSFET proposals**

  The two new concepts of HV power trench MOSFET are described in chapter 6. The new trench MOS with a source with waffle pattern and new trench MOS with triangle gate pattern has been compared with conventional trench MOSFET. All new concepts have been presented at an international conference [12].

- **Power IC layout flow improvements**

  How to reduce physical design development time and cost for smart power IC is described in chapter 7. To optimized analog layout implementation flow for smart power IC, the several improvements has been developed and are used in STMicroelectronics. The new automatic pre-placement phase of flow was a first time defined, to simplify and speed up analog and mixed-signal (AMS) layout and has been published in the impacted journal Integration, the VLSI Journal [13]. The new and more time effective way of objects modification in layout database have been defined and published in the reviewed journal named Advances in Science, Technology and Engineering Systems Journal [14] and have been also presented at international conferences [15], [16]. In addition, the new and more time effective searching flow in layout and schematic database have been developed and presented at an international conference [17].

1.4. State of the Art

Silicon is currently the most commonly used semiconductor material in Power electronics. The first generation of power MOSFET devices used Double diffused MOSFET (DMOS) architecture. The second generation used trench-gate power MOSFETs and third used super-junction power MOSFETs architecture.

Tab. 1.1. Specific On-Resistance and BV for Power MOSFETs on Si

BV [V]	Ron A [mΩ cm^2]	Topology	Gate type	Gate pattern	Reference
752.4	48.5	SJ-LDMOS	Planar	Fingers	[18]
880	90	IGBT	Planar	Fingers	[19]
130	1.95	LDMOS	Planar	Fingers	[20]
23	0.3	LDMOS	Planar	Fingers	[21]
47	0.218	LDMOS	Planar	Fingers	[22]
54	0.32	LDMOS	Planar	Fingers	[23]
36	0.145	LDMOS	Planar	Fingers	[24]
55	2.17	LDMOS	Planar	Fingers	[25]
55	1.1	LDMOS	Trench	Fingers	[25]
22	0.4	LDMOS	Planar	Fingers	[26]
165	1.59	LDMOS	Planar	Fingers	[27]
6.05	0.01	LDMOS	Planar	Fingers	[28]
98.6	1.01	SJ-LDMOS	Planar	Fingers	[29]
25	0.2	LDMOS	Trench	Fingers	[30]
25	0.07	Bi-LDMOS	Trench	Fingers	[30]
68	0.18	SJ-FINFET	Planar	Fingers	[31]
55	3.05	LDMOS	Trench	Fingers	[32]
800	72	IGBT	Planar	Fingers	[19]
94	0.3	XtreMOS	Trench	Hexagonal	[1]
72.3	1.01	SJ-LDMOS	Planar	Fingers	[33]
275	7	LDMOS	Planar	Fingers	[34]
55	0.8	VDMOS	Trench	Waffle	[35]
11.5	0.095	MOS	Planar	Fingers	[36]
21	0.17	MOSFET	Trench	Fingers	[37]
660	600	MOSFET	Planar	Fingers	[38]
34.1	0.084	MOSFET	Trench	Fingers	[39]
11.2	0.077	MOSFET	Planar	Fingers	[40]
15.5	0.057	LDMOS	Planar	Fingers	[40]
15.5	0.061	LDMOS	Planar	Fingers	[40]
165	1.65	SJ-LDMOS	Planar	Fingers	[41]
750	200	LDMOS	Planar	Fingers	[42]
73	0.72	MOSFET	Trench	Fingers	[43]
7	0.0068	MOSFET	Planar	Waffle	[44]
71.5	0.56	LDMOS	Planar	Fingers	[45]

Additional advantages of Silicon is very good process control (low density of crystal defects) and price per wafer (is cost-effective) which allow development of wafer size high power devices like IGCT or BGCT with thyristor-like conduction [46], [47].

Overview of experimental Power MOSFETs made on Silicon with their Specific On-Resistance, and breakdown voltage is present in Tab. 1.1. The Power MOSFETs made on Silicon Carbide are present in Tab. 1.2

Tab. 1.2. Specific On-Resistance and BV for Power MOSFETs on SiC

BV [V]	**Ron*A [mΩ cm^2]**	**Topology**	**Gate type**	**Gate pattern**	**Reference**
1760	7.06	DMOS	Planar	Fingers	[48]
1650	3.7	DMOS	Planar	Fingers	[49]
1540	5	MOSFET	Planar	Fingers	[50]
12000	127	MOSFET	Planar	Fingers	[51]
12000	14.3	IGBT	Planar	Fingers	[51]
1550	54	MOSFET	Planar	Fingers	[52]
2420	10.3	DMOS	Planar	Fingers	[53]
11000	290	IGBT	Trench	Fingers	[54]
1760	27	MOSFET	Planar	Fingers	[55]

Since the first report of high density two-dimensional (2D) electron gas in 1991 [56] and high electron mobility transistors in 1993 [57], GaN has gained traction and now discrete GaN transistors are emerging as commercial products [58].

The Power MOSFETs made on Gallium Nitride with their Specific On-Resistance and breakdown voltage are present in Tab. 1.3.

Tab. 1.3. Specific On-Resistance and BV for Power MOSFETs on GaN

BV [V]	**Ron*A [mΩ cm^2]**	**Topology**	**Gate type**	**Gate pattern**	**Reference**
330	1.2	FinFET	Tri Gate	Fingers	[59]
650	3.4	HEMT	Planar	Fingers	[60]
770	3	HEMT	Planar	Fingers	[61]
86	1.86	HEMT	Planar	Fingers	[62]
1320	20	HEMT	Planar	Fingers	[63]
665.5	87	MOS	Planar	Fingers	[64]

Visualization of Specific On-Resistance as the function of BV for devices from Tab. 1.1, Tab. 1.2 and Tab. 1.3 with the Specific On-Resistance limits of drift region for unipolar devices is on figure Fig. 1.1.

Currently, best State of the Art MOSFET architecture on Silicon is XtreMOS with trench gate with hexagonal shape [36]. The XtreMOS have specific On-Resistance equal to 0.3 mΩ*cm^2 for breakdown voltage 94 V. On SiC substrate State of the Art MOSFET [51] have BV equal to 12000 V and have specific On-Resistance equal to 127 mΩ cm^2. On GaN substrate State of the Art MOSFET [61] have BV equal to 770 V and have specific On-Resistance equal to 3 mΩ cm^2.

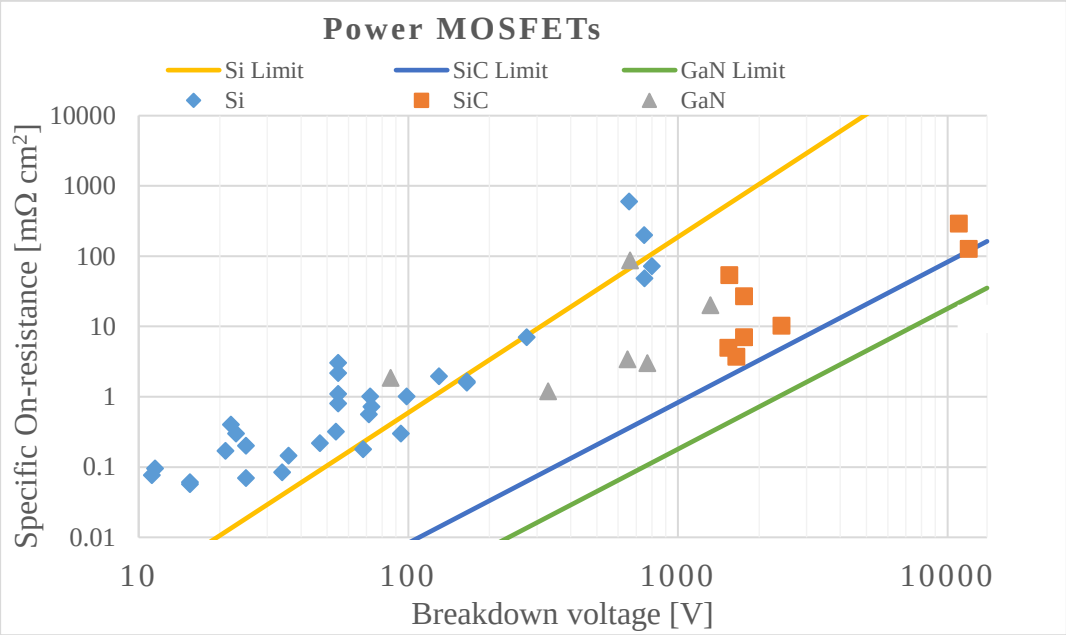


Fig. 1.1. Specific on-state resistance vs. avalanche breakdown voltage for experimental devices with material limits of drift region for unipolar devices

Devices with width band-gap materials are the main competitors to the silicon-based power devices. The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of all GaN power ICs. Next-generation monolithic integration (e.g., advanced I/O features, over-current, and over-temperature protection) will enable even higher levels of efficiency, power density and reduced system cost [4].

Miniaturization in the semiconductor industry is a well-known practice. It is driven not only by price per area optimization, but it also allows to realize new types of applications. These applications are not easily reachable by previous generations of technologies. Actual trends and intensive developments are currently focused on

mobile electronics, wearable electronics, and Internets of Things (IoT) applications that are limited by miniaturization possibilities. Applications such as smart watches, electronics pills, wireless head speakers, or Augmented Reality (AR) glasses represent a small part of new types of applications that come from progress in miniaturization. To solve high requirements on system dimensions, there the highest process nodes are being used as well as whole system integration by using System in Package (SIP), System on Chip (SOC) approach, Wafer Level Chip Scale Package (WLCSP, CSP), Package on Package (PoP) or more advance Through Silicon Via (TSV). The last TSV is used for 3D chips Integrated Circuits (IC) with more optimal interconnections and more compact chips stacking. An additional advantage of smaller chip area is yield improvement [65].

In the past and also nowadays, a big portion of IC chips is occupied by power management. In order to save area in SIP packages, we could use the more compact vertical power devices. Hence in more compact SOC, only lateral power devices can be used. For additional effective scaling of lateral low voltage, power devices the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) with waffle gate patterns can be used [66].

For effective scaling of lateral low voltage, power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices the waffle gate patterns can be used [66]. Another publication deals with RF measurement of the waffle MOSFET without defining an analytic model of channel conductance [67]. Vemuru has described models for square shape waffle MOSFET in [68]. However, these models do not allow describing non-square shapes. Madhyastha [69] has described waffle MOSFET with orthogonal source and drain interconnection but it metallization is more complex and has a weak electro-migration limit.

1.5. Solution Methods of the Work

To reach the goal the multiple analysis was realized. For very precise 2D modeling of the channel, area and current paths for simple polygons the MATLAB [70] with Schwarz–Christoffel Toolbox [71] was used. The complex medium size 2D polygons and 3D polygons have been analyzing with 2D and 3D FEM simulator TCAD from SILVACO [72]. The more complex and large size 2D polygons have been simulated with 2D FEM solver Agros2D [73]. The mathematical modeling and optimization have

been realize with Wolfram Mathematica [74] and function fitting has been calculating with the MATLAB [70].

The physical implementation of IC has been created in Cadence Virtuoso Layout Editors [75], [76] and new flow improvement features have been realizes in the Cadence SKILL programming language [77] and the Cadence SKILL IDE environment [78].

For physical design verification of Si IC the whole standard verification flow was used. The IC verification and Signoff Calibre DRC and LVS [79] tools have been used to check the layout database with design rule manual (DRM) respectively with schematic diagrams. The Post Layout Extraction (PLS) has been realizes with Synopsys Star-RCXT [80].

The physical design verification of GaN IC has been realizes with Calibre DRC [79] with a custom run set of DRM rules.

A fabricated test chips has been characterized and validated by standard laboratory equipment such as precise voltage and current sources, oscilloscopes, etc.

2. Power MOSFETs Fundaments

In following sections, are described fundamental properties of the MOSFET devices. Problematic is divided into section related to device characteristics and the section related to material and topology fundaments

2.1. Ideal and Typical Power MOSFET Device Characteristics

The volt-ampere characteristics of an ideal power switch are illustrated in Fig. 2.1. The ideal transistor conducts current in the on-state with zero voltage drop and blocks voltage in the off-state with zero leakage current. Also, the ideal device can operate with a high current and voltage in the active region, with the saturated forward current in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor indicating a gain that is independent of the forward current and voltage [81].

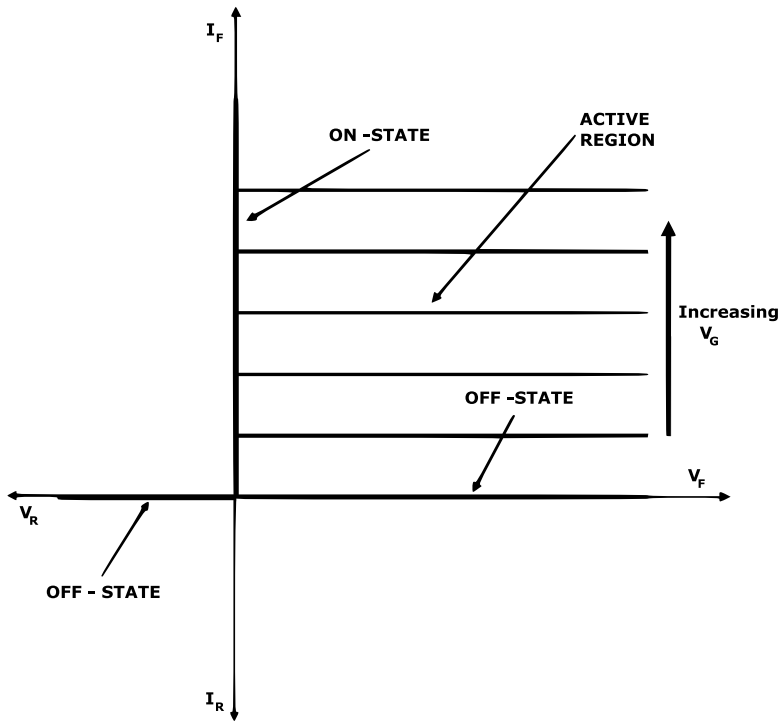


Fig. 2.1. Characteristics of an ideal transistor [81].

In the reverse blocking mode the third quadrant off operation in the figure, it should be able to hold of any value of voltage with zero leakage current. Further, the ideal rectifier should be able to switch between the on-state and the off-state, with zero switching time [81].

The volt-ampere characteristics of a typical power switch are illustrated in Fig. 2.2. This device exhibits a finite resistance when carrying current in the on-state as well as a finite leakage current while operating in the off-state (not shown in the figure because its value is much lower than the on-state current levels). The breakdown voltage of a typical transistor is also finite as indicated in the figure with “BV”. The typical transistor can operate with a high current and voltage in the active region. The spacing between the characteristics in the active region is nonuniform for a typical transistor with a square-law behavior for devices operating with channel pinch-off in the current saturation mode [81].

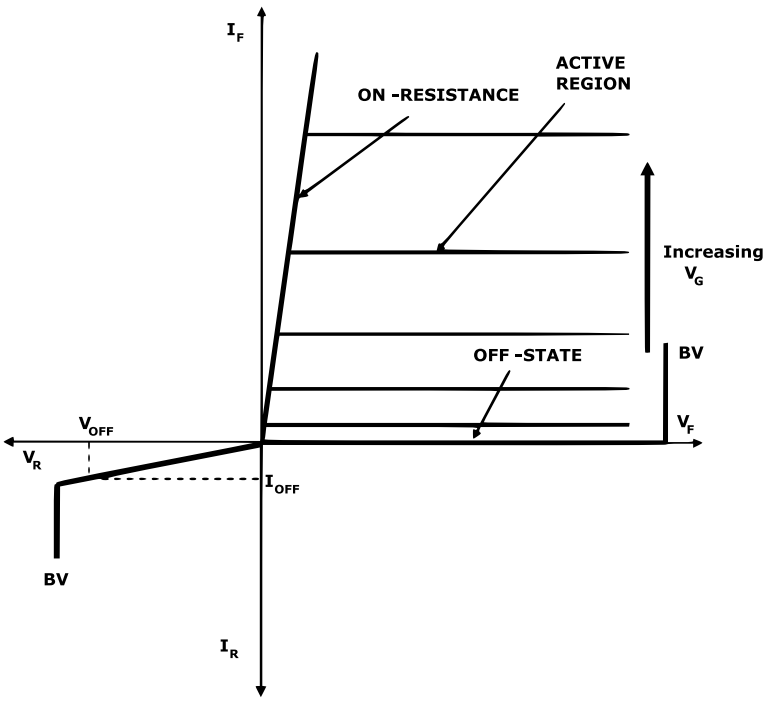


Fig. 2.2. Characteristics of a typical transistor [81].

They also have a finite leakage current (I_{OFF}) when blocking voltage in the off-state, creating off-state power loss. Also, the doping concentration and thickness of the drift region of the silicon device must be carefully chosen with a design target for the breakdown voltage (BV). Moreover, the power dissipation in power devices increases

when their voltage rating is increased because of an increase in the on-state voltage drop [81].

Following chapters 2.1.1 until 2.1.9 are based on [82], [83].

2.1.1. Mobility

Force interaction F on an electron is equivalent to it mass m_e and it accelerations a

$$\vec{F} = m_e\,\vec{a}. \tag{2.1}$$

The velocity v of the electron is at time t is

$$\vec{v} = \vec{a}\,t. \tag{2.2}$$

The electrical intensity E is defined as a normalized force for election charge q as

$$\vec{E} = \frac{\vec{F}}{\pm q}. \tag{2.3}$$

Inserting (2.1) and (2.3) into (2.2) we get how carriers accelerate in the direction of field E between collisions

$$\vec{v} = \frac{\pm q\,\vec{E}}{m_{\mathrm{e,h}}}\,t. \tag{2.4}$$

The average net velocity in the direction of field E is randomized over mean free time between collisions τ_c

$$v_{\mathrm{dn}} = -\frac{q\,E}{2\,m_{\mathrm{e}}}\,\tau_{\mathrm{c}} = -\frac{q\,\tau_{\mathrm{c}}}{2\,m_{\mathrm{e}}}\,E = -\mu_n\,E. \tag{2.5}$$

The average drift velocity of the hole is

$$v_{\mathrm{dp}} = +\frac{q\,E}{2\,m_{\mathrm{h}}}\,\tau_c = +\frac{q\,\tau_{\mathrm{c}}}{2\,m_{\mathrm{h}}}\,E = +\mu_{\mathrm{p}}\,E. \tag{2.6}$$

Where μ_n is an electron mobility

$$\mu_{\mathrm{n}} = \frac{q\,\tau_c}{2\,m_{\mathrm{e}}}. \tag{2.7}$$

The holes mobility μ_p is defined as follows

$$\mu_{\mathrm{p}} = \frac{q\,\tau_{\mathrm{c}}}{2\,m_{\mathrm{h}}}. \tag{2.8}$$

2.1.2. Drift current density

Drift electron current J_n^{drift} is equivalent to the number of electrons n with charge q and its drift velocity v_{nd}

$$J_{\mathrm{n}}^{\mathrm{drift}} = -q\ n\ v_{\mathrm{dn}} = q\ n\ \mu_{\mathrm{n}}\ E. \tag{2.9}$$

Drift holes current $J_{\mathrm{p}}^{\mathrm{drift}}$ is

$$J_{\mathrm{p}}^{\mathrm{drift}} = q\ n\ v_{\mathrm{dp}} = q\ n\ \mu_{\mathrm{p}}\ E. \tag{2.10}$$

Where the number of holes is p. Total drift current J^{drift} is

$$J^{\mathrm{drift}} = J_{\mathrm{n}}^{\mathrm{drift}} + J_{\mathrm{p}}^{\mathrm{drift}} = q\ (n\ \mu_{\mathrm{n}} + p\ \mu_{\mathrm{p}})\ E. \tag{2.11}$$

Ohm law

$$J = \delta\ E = \frac{E}{\rho_s}. \tag{2.12}$$

Where resistivity ρ_s and conductivity δ is defined as follows

$$\rho_s = \frac{1}{\delta_s} = \frac{1}{q\ (n\ \mu_{\mathrm{n}} + p\ \mu_{\mathrm{p}})}. \tag{2.13}$$

In N-type semiconductor the resistivity ρ_{n} is

$$\rho_{\mathrm{n}} \cong \frac{1}{q\ N_{\mathrm{D}}\ \mu_{\mathrm{n}}} \tag{2.14}$$

In P-type semiconductor the resistivity ρ_{p} is

$$\rho_{\mathrm{p}} \cong \frac{1}{q\ N_{\mathrm{A}}\ \mu_{\mathrm{p}}} \tag{2.15}$$

2.1.3. Diffusion current density

The concentration gradient is defined by Diffusion flux and is causing that particles diffused from high to low concentration, due to this is always negative. This behavior is described by Frick low. Diffusion flux F_{n} represents the number of particles crossing a unit area per unit time and for electrons with a gradient in the x-axis is

$$F_{\mathrm{n}} = -D_{\mathrm{n}}\ \frac{dn}{dx} \tag{2.16}$$

Moreover, for holes flux is F_{p}

$$F_{\mathrm{p}} = -D_{\mathrm{p}}\ \frac{dn}{dx} \tag{2.17}$$

Diffusion current density $J_{\mathrm{n}}^{\mathrm{diff}}$ for lattice and electron with the same temperature is

$$J_{\mathrm{n}}^{\mathrm{diff}} = -q\ F_{\mathrm{n}} = q\ D_{\mathrm{n}}\ \frac{dn}{dx} \tag{2.18}$$

Diffusion current density for holes $J_{\mathrm{p}}^{\mathrm{diff}}$ is

$$J_{\mathrm{p}}^{\mathrm{diff}} = q\ F_{\mathrm{p}} = -q\ D_{\mathrm{p}}\ \frac{dn}{dx} \tag{2.19}$$

2.1.4. Einstein relation

Because collision between particles and lattice have the same physics for diffusion and drift carrier, there is a relation among them defined by Einstein relation

$$\frac{D_{\mathrm{n}}}{\mu_{\mathrm{n}}} = \frac{D_{\mathrm{p}}}{\mu_{\mathrm{p}}} = \frac{k\,T}{q} \tag{2.20}$$

where k is Boltzmann constant, and T is a temperature

2.1.5. Total current density

In general, the total current is the composition of drift and diffusion current. The current for electrons J_{n} is

$$J_{\mathrm{n}} = J_{\mathrm{n}}^{\mathrm{drift}} + J_{\mathrm{n}}^{\mathrm{diff}} = q\,n\,\mu_{\mathrm{n}}\,E + q\,D_{\mathrm{n}}\,\frac{dn}{dx} \tag{2.21}$$

The current for holes J_{p} is

$$J_{\mathrm{p}} = J_{\mathrm{p}}^{\mathrm{drift}} + J_{\mathrm{p}}^{\mathrm{diff}} = q\,n\,\mu_{\mathrm{p}}\,E - q\,D_{\mathrm{p}}\,\frac{dn}{dx} \tag{2.22}$$

The total current J_{total} is the composition of electron and holes currents

$$J_{\mathrm{total}} = J_{\mathrm{n}} + J_{\mathrm{p}} \tag{2.23}$$

2.1.6. Non-uniform doped semiconductor

First Maxwell equation

$$\nabla \cdot D = \rho \tag{2.24}$$

where ρ is space charge density and D is electric displacement field. Second Maxwell equation is

$$\nabla \cdot B = 0 \tag{2.25}$$

where B is a magnetic field. Third Maxwell equation

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{2.26}$$

Where t is time. Forth Maxwell equation is

$$\nabla \times H = J + \frac{\partial D}{\partial t} \tag{2.27}$$

Where H is magnetic field strength, and J is a current density

$$D = E\,\varepsilon \tag{2.28}$$

The is permittivity ε and electric intensity E

$$H = B / \mu \tag{2.29}$$

Where μ is permeability. From Maxwell equation (2.24) we get

$$\nabla \cdot E\, \varepsilon = \rho \tag{2.30}$$

Poisson equation (Gauss' low) for electric field E in X-axis is

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon} \tag{2.31}$$

Where ρ is space charge density and ε is electrostatic permittivity. Electrostatic potential Φ *is*

$$\frac{d\Phi}{dx} = -E \tag{2.32}$$

The non-uniform doped semiconductor in thermal equilibrium

$$J_{\mathrm{n}} = q\, n\, \mu_{\mathrm{n}}\, E + q\, D_{\mathrm{n}}\, \frac{dn}{dx} = 0 \tag{2.33}$$

Inserting (2.31) and (2.32) into (2.33) we can get

$$-q\, n\, \mu_{\mathrm{n}}\, \frac{d\Phi}{dx} + q\, D_{\mathrm{n}}\, \frac{dn}{dx} = 0 \tag{2.34}$$

Rewriting (2.34) we can get

$$\frac{\mu_{\mathrm{n}}}{D_{\mathrm{n}}}\, \frac{d\Phi}{dx} = \frac{1}{n}\, \frac{dn}{dx} \tag{2.35}$$

By inserting (2.20) into (2.35), we get

$$\frac{k\, T}{q}\, \frac{d\Phi}{dx} = \frac{1}{n}\, \frac{dn}{dx} \tag{2.36}$$

After integration

$$\frac{k\, T}{q} \int_{\Phi}^{\Phi_{\mathrm{ref}}} d\Phi = \int_{n_0}^{n_{\mathrm{ref}}} \frac{1}{n}\, dn \tag{2.37}$$

After integration

$$\frac{k\, T}{q}\, (\Phi - \Phi_{\mathrm{ref}}) = \ln n_0 - \ln n_{\mathrm{ref}} = \ln \frac{n_0}{n_{\mathrm{ref}}} \tag{2.38}$$

After reduction n_0

$$n_0 = n_{\mathrm{ref}}\, e^{\frac{q}{k\, T}(\Phi - \Phi_{\mathrm{ref}})} \tag{2.39}$$

Reference potential Φ_{ref} =0 and $n_{\mathrm{ref}} = n_{\mathrm{i}}$ then we get Boltzmann relations

$$n_0 = n_{\mathrm{i}}\, e^{\frac{q\, \Phi}{k\, T}} \tag{2.40}$$

Because of $n_0 \,.\, p_0 = n_{\mathrm{i}}^2$ then Boltzmann relations for holes is

$$p_0 = n_{\mathrm{i}}\, e^{-\frac{q\, \Phi}{k\, T}} \tag{2.41}$$

The potential Φ in n region is

$$\Phi = \frac{k\,T}{q}\ \ln\frac{n_0}{n_i} \tag{2.42}$$

The potential in p region is

$$\Phi = -\frac{k\,T}{q}\ \ln\frac{p_0}{n_\mathrm{i}} \tag{2.43}$$

Rewriting natural logarithm to the logarithm to the base 10 of at

$$\Phi = \frac{k\,T}{q}\ \ln\frac{n_0}{n_\mathrm{i}} = \frac{k\,T}{q}\ \ln(10)\ \log\frac{n_0}{n_\mathrm{i}} \tag{2.44}$$

For silicon at temperature 300 K

$$\Phi = (25\mathrm{mV})\ \ln(10)\ \log\frac{n_0}{n_\mathrm{i}} \tag{2.45}$$

Silicon at temperature 300 K have concentration n_i= 10^{10}, we get “60 mV Rule”

$$\Phi \cong (60\ \mathrm{mV})\ \log\frac{n_0}{10^{10}} \tag{2.46}$$

For every decade of increase in doping n_0 the potential Φ increase by 60 mV at temperature 300 K

2.1.7. Depletion of a p-n junction in thermal equilibrium

Consider p-n junction in thermal equilibrium without external supply voltage Fig. 2.3. In p-region, there is doping of acceptor $N_\mathrm{A,}$ and in n-region, there is doping of donors N_D.

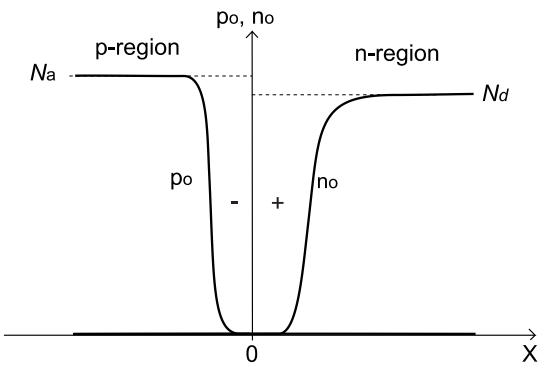


Fig. 2.3. Doping distribution of p-n junction in thermal equilibrium [82].

In the junction area of the p-region and n-region, there is a significant charge disbalance. Due to charge neutrality, the free charges are reallocated, and it creates a depletion region also called a space charge region. In thermal equilibrium positive

charge is described by p_0 and negative charge by n_0 as can be seen in Fig. 2.3. The Space charge density of p-n junction is in Fig. 2.4.

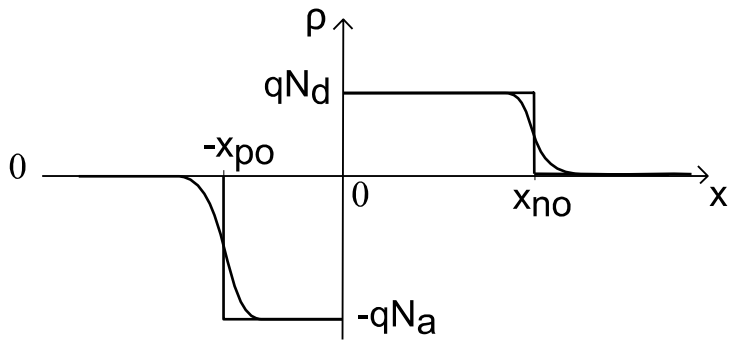


Fig. 2.4. Space charge density of p-n junction in equilibrium [82].

The electrical intensity in a p-n junction in equilibrium is in Fig. 2.5.

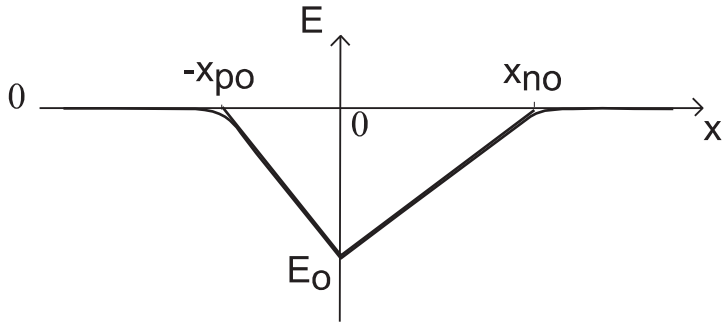


Fig. 2.5. The electrical intensity of a p-n junction in equilibrium [82].

Electrical intensity based on Gauss equation for $x < -x_{p0}$ is

$$E(x) = 0. \tag{2.47}$$

Electrical intensity for $-x_{p0} < x < 0$ is

$$E(x) - 0 = -\frac{1}{\varepsilon_s}\int_{-x_{p0}}^{x} \frac{q\,N_A}{\varepsilon_s}\,\mathrm{dx} = \frac{-q\,N_A}{\varepsilon_s}\,[x]_{-x_{p0}}^{x} \tag{2.48}$$

$$= -\frac{q\,N_A}{\varepsilon_s}\,(x + x_{p0}).$$

Electrical intensity for $0 < x < x_{n0}$ is

$$E(x) = \frac{q\,N_D}{\varepsilon_s}\,(x - x_{n0}). \tag{2.49}$$

Electrical intensity for $x_{n0} < x$ is

$$E(x) = 0. \tag{2.50}$$

The potential gradient in the p-n junction in equilibrium is present in Fig. 2.6.

Build in potential in the p-n junction is defined as the difference between (2.42) and (2.43) with p_0=N_A and n_0=N_D

$$\Phi_B = \Phi_n - \Phi_p = \frac{k\,T}{q}\ \ln\frac{N_A\,N_D}{{n_i}^2} \tag{2.51}$$

Potential for $x < -x_{p0}$ is

$$\Phi(x) = \Phi_p. \tag{2.52}$$

Potential for $-x_{p0} < x < 0$

$$\Phi(x) - \Phi_p = -\int_{-x_{p0}}^{x} -\frac{q\,N_A}{\varepsilon_s}\left(x + x_{p0}\right)\mathrm{dx} = \tag{2.53}$$

$$\frac{q\,N_A}{2\,\varepsilon_s}(x + x_{p0})^2$$

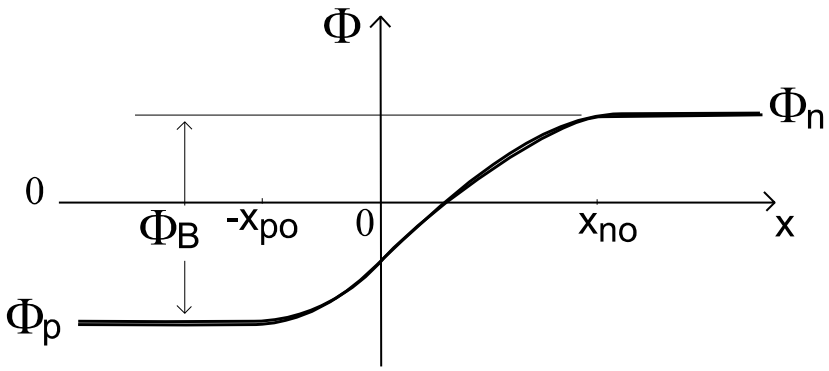


Fig. 2.6. The potential of a p-n junction in equilibrium [82].

From (2.53) can be derived potential

$$\Phi(x) = \Phi_p + \frac{q\cdot N_A}{2\cdot\varepsilon_s}\ (x + x_{p0})^2 \tag{2.54}$$

Potential for $0 < x < x_{n0}$

$$\Phi(x) = \Phi_n - \frac{q\cdot N_D}{2\cdot\varepsilon_s}\ (x - x_{n0})^2 \tag{2.55}$$

Potential for $x_{n0} < x$

$$\Phi(x) = \Phi_n \tag{2.56}$$

Due to the overall charge neutrality

$$q\ N_A\ x_{p0} = q\ N_D\ x_{n0} \tag{2.57}$$

Potential is continuous at x=0, and from (2.54) and (2.55) we can get

$$\Phi_p + \frac{q\cdot N_A}{2\cdot\varepsilon_s}\ \left(x_{p0}\right)^2 = \Phi_n - \frac{q\cdot N_D}{2\cdot\varepsilon_s}\ (x_{n0})^2 \tag{2.58}$$

From equations, (2.57) and (2.58) can be defined quadratic equations with unknown variable x_{n0}

$$\frac{q\,N_A}{2\,\varepsilon_s}\left(\frac{N_D}{N_A}\,x_{n0}\right)^2 = \frac{q\,N_D^2\,x_{n0}^2}{2\,\varepsilon_s\,N_A} = -\frac{q\,N_D}{2\,\varepsilon_s}\ (x_{n0})^2 + \Phi_B \tag{2.59}$$

From quadratic equations (2.59) can be solved unknown variable x_{n0}

$$x_{n0} = \sqrt{\frac{2\,\varepsilon_S\,\Phi_B\,N_A}{q\,(N_A+N_D)\,N_D}} \tag{2.60}$$

Similarly from (2.57) and (2.58) can be solved depletion width x_{p0} in the p-type semiconductor

$$x_{p0} = \sqrt{\frac{2\,\varepsilon_S\,\Phi_B\,N_D}{q\,(N_A+N_D)\,N_A}} \tag{2.61}$$

The overall width of the depletion region is

$$x_{d0} = x_{n0} + x_{p0} = \sqrt{\frac{2\,\varepsilon_S\,\Phi_B\,(N_A+N_D)}{q\,N_A\,N_D}} \tag{2.62}$$

Maximum Electrical intensity of p-n junction is at x=0 and can be calculated from (2.49) at x=0 and (2.60)

$$|E_0| = \left|\frac{q\,N_D}{\varepsilon}\left(-\sqrt{\frac{2\,\varepsilon\,\Phi_B\,N_A}{q\,(N_A+N_D)\,N_D}}\right)\right| = \sqrt{\frac{2\,q\,\Phi_B\,N_A\,N_D}{\varepsilon\,(N_A+N_D)}} \tag{2.63}$$

For strongly asymmetric junction N_A>>N_D the width of the depletion region is

$$x_{p0} \ll x_{n0} \cong x_{d0} \cong \sqrt{\frac{2\,\varepsilon_S\,\Phi_B}{q\,N_D}} \propto \frac{1}{\sqrt{N_D}} \tag{2.64}$$

Maximum Electrical intensity of p-n asymmetric junction N_A>>N_D from (2.63) is

$$|E_0| \cong \sqrt{\frac{2\,q\,\Phi_B\,N_D}{\varepsilon_S}} \propto \sqrt{N_D} \tag{2.65}$$

For symmetric junction N_A=N_D the width of depletion region x_{p0} and x_{n0} is

$$x_{n0} = x_{p0} = \sqrt{\frac{\varepsilon_S\,\Phi_B}{q\,N_A}} = \sqrt{\frac{\varepsilon_S\,\Phi_B}{q\,N_D}} \tag{2.66}$$

From (2.62) for symmetric junction N_A=N_D the width of the depletion region is

$$x_{d0} = x_{n0} + x_{p0} = \sqrt{\frac{4\,\varepsilon_S\,\Phi_B}{q\,N_A}} = \sqrt{\frac{4\,\varepsilon_S\,\Phi_B}{q\,N_D}} \tag{2.67}$$

Maximum Electrical intensity of p-n symmetric junction N_A=N_D is

$$|E_0| = \sqrt{\frac{q\,\Phi_B\,N_A}{\varepsilon_S}} = \sqrt{\frac{q\,\Phi_B\,N_D}{\varepsilon_S}} \tag{2.68}$$

2.1.8. P-N junction under the bias

For P-N junction under bias condition following substitution for (2.60) to (2.68) is required

$$\Phi_B \rightarrow \Phi_B - V \tag{2.69}$$

Depletion width x_n in the n-type semiconductor under bias V is

$$x_{\mathrm{n}}(\mathrm{V}) = \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{A}}}{q\,(N_{\mathrm{A}}+N_{\mathrm{D}})\,N_{\mathrm{D}}}} = x_{\mathrm{n0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}} \tag{2.70}$$

Depletion width x_{p} in the p-type semiconductor under bias V is

$$x_{\mathrm{p}}(\mathrm{V}) = \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{D}}}{q\,(N_{\mathrm{A}}+N_{\mathrm{D}})\,N_{\mathrm{A}}}} = x_{\mathrm{p0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}} \tag{2.71}$$

The overall width of the depletion region under bias V is

$$x_{\mathrm{d}}(\mathrm{V}) = \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)\,(N_{\mathrm{A}}+N_{\mathrm{D}})}{q\,N_{\mathrm{A}}\,N_{\mathrm{D}}}} = x_{\mathrm{d0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}} \tag{2.72}$$

The overall width of depletion region under bias V for strongly asymmetric junction $N_A >> N_D$ is

$$x_{\mathrm{p}}(\mathrm{V}) \ll x_{\mathrm{n}}(\mathrm{V}) \cong x_{\mathrm{d}}(\mathrm{V}) \cong \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)}{q\,N_{\mathrm{D}}}} = \tag{2.73}$$

$$= x_{\mathrm{d0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}}$$

From (2.66) for symmetric junction $N_A=N_D$ the width of depletion region x_{p0} and x_{n0} is

$$x_{\mathrm{n}}(\mathrm{V}) = x_{\mathrm{p}}(\mathrm{V}) = \sqrt{\frac{\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)}{q\,N_{\mathrm{A}}}} = \sqrt{\frac{\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)}{q\cdot N_{\mathrm{D}}}} = \tag{2.74}$$

$$= x_{\mathrm{n0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}}$$

The overall width of depletion region under bias V for symmetric junction $N_A=N_D$ is

$$x_{\mathrm{d}}(\mathrm{V}) = \sqrt{\frac{4\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)}{q\,N_{\mathrm{D}}}} = \sqrt{\frac{4\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}}-V)}{q\,N_{\mathrm{A}}}} = x_{\mathrm{d0}}\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}} \tag{2.75}$$

Maximum Electrical intensity of p-n junction under bias V is

$$|E(\mathrm{V})| = \sqrt{\frac{2\,q\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{A}}\,N_{\mathrm{D}}}{\varepsilon_{\mathrm{s}}\,(N_{\mathrm{A}}+N_{\mathrm{D}})}} = |E_0|\sqrt{1-\frac{V}{\Phi_{\mathrm{B}}}} \tag{2.76}$$

Maximum Electrical intensity of p-n junction under bias V for strongly asymmetric junction $N_A >> N_D$ is

$$|E(\mathrm{V})| \cong \sqrt{\frac{2\,q\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{D}}}{\varepsilon_{\mathrm{s}}}} \tag{2.77}$$

Maximum Electrical intensity of p-n junction under bias V for symmetric junction $N_A=N_D$ is

$$|E(\mathrm{V})| = \sqrt{\frac{q\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{A}}}{\varepsilon_{\mathrm{s}}}} = \sqrt{\frac{q\,(\Phi_{\mathrm{B}}-V)\,N_{\mathrm{D}}}{\varepsilon_{\mathrm{s}}}} \tag{2.78}$$

The depleted capacitance of depletion region per unit area under bias V is

$$C_{\mathrm{j}}(\mathrm{V}) = \frac{\varepsilon_{\mathrm{s}}}{x_{\mathrm{d}}(\mathrm{V})} = \sqrt{\frac{\varepsilon_{\mathrm{s}}\, q\, N_{\mathrm{A}}\, N_{\mathrm{D}}}{2\,(\Phi_{\mathrm{B}} - V)\,(N_{\mathrm{A}} + N_{\mathrm{D}})}} = \frac{C_{\mathrm{j0}}}{\sqrt{1 - \frac{V}{\Phi_{\mathrm{B}}}}} \tag{2.79}$$

For asymmetric junction $N_A >> N_D$ depleted capacitance of depletion region per unit area under bias V is

$$C_{\mathrm{j}}(\mathrm{V}) = \sqrt{\frac{\varepsilon_{\mathrm{s}}\, q\, N_{\mathrm{D}}}{2\,(\Phi_{\mathrm{B}} - V)}} \tag{2.80}$$

For symmetric junction, $N_A = N_D$ depleted capacitance of depletion region per unit area under bias V is

$$C_{\mathrm{j}}(\mathrm{V}) = \sqrt{\frac{\varepsilon_{\mathrm{s}}\, q\, N_{\mathrm{A}}}{4\,(\Phi_{\mathrm{B}} - V)}} = \sqrt{\frac{\varepsilon_{\mathrm{s}}\, q\, N_{\mathrm{D}}}{4\,(\Phi_{\mathrm{B}} - V)}} \tag{2.81}$$

The charge of the depletion region under bias V is

$$Q_{\mathrm{j}}(\mathrm{V}) = q\, N_{\mathrm{A}}\, x_{\mathrm{p}} = \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\, q\, N_{\mathrm{A}}\, N_{\mathrm{D}}\,(\Phi_{\mathrm{B}} - V)}{(N_{\mathrm{A}} + N_{\mathrm{D}})}} = \tag{2.82}$$

$$= Q_{\mathrm{j0}} \sqrt{1 - \frac{V}{\Phi_{\mathrm{B}}}}$$

For strongly asymmetric junction $N_A >> N_D$ the doping concentration in the drift region (2.77) at breakdown voltage BV require to obtain potential $V = -BV$ for $BV >> \phi_B$ at critical intensity E_c is given by

$$N_{\mathrm{D}} \cong \frac{\varepsilon_{\mathrm{s}}\, {E_c}^2}{2\, q\, BV} \tag{2.83}$$

By inserting (2.83) into (2.73)(2.64) for $BV >> \phi_B$ we get the width of the depletion region at breakdown voltage condition W_{D_BV} for asymmetric junction $N_A >> N_D$ is

$$\mathrm{W}_{\mathrm{D_BV}} \cong \sqrt{\frac{2\,\varepsilon_{\mathrm{s}}\,(\Phi_{\mathrm{B}} - VB)}{q\, N_{\mathrm{D}}}} \cong \frac{2\, BV}{E_{\mathrm{c}}} \tag{2.84}$$

For symmetric junction $N_A = N_D$ the doping concentration in the drift region (2.78) at breakdown voltage BV require to obtain potential $V = -BV$ for $BV >> \phi_B$ at critical intensity E_c is given by

$$N_{\mathrm{D}} = N_{\mathrm{A}} \cong \frac{\varepsilon_{\mathrm{s}}\, {E_c}^2}{q\, BV} \tag{2.85}$$

By inserting (2.85) into (2.74) for $BV >> \phi_B$ we get the width of the depletion region at breakdown voltage condition W_{D_BV} for symmetric junction $N_A = N_D$ is

$$W_{D_BV} = \sqrt{\frac{\varepsilon_s\,(\Phi_B - VB)}{q\,N_D}} \cong \frac{BV}{E_c} \tag{2.86}$$

2.1.9. MOSFET V I characteristic

Description of the channel current of MOSFET is present in Fig. 2.7

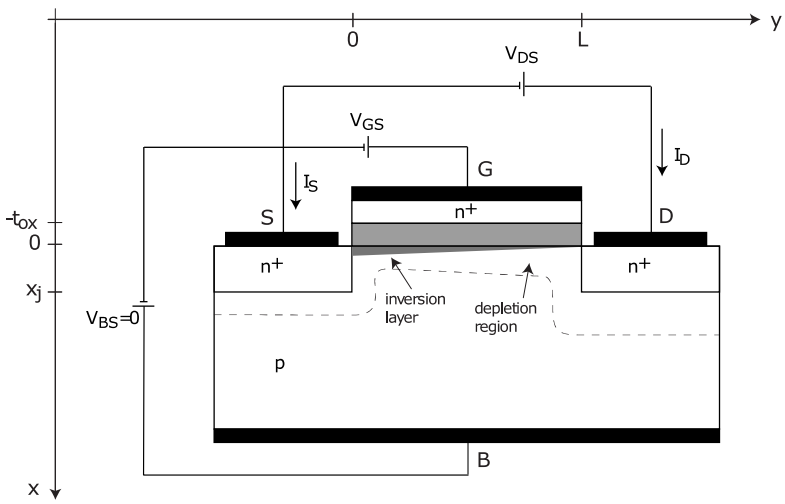


Fig. 2.7. Description of the channel current of MOSFET transistor [82].

The drain current flowing in the channel in the y-direction is

$$I_D = -\,W\,Q_n(y)\,v_{dn}(y) \tag{2.87}$$

Average drift velocity

$$v_{dn}(y) = -\mu_n\,E(y) = \mu_n\,\frac{dV_{channel}(y)}{dy} \tag{2.88}$$

Charge in an inversion layer in channel area is

$$Q_n(y) = -C_{ox}\,(V_{GS} - V_{channel}(y) - V_T) \tag{2.89}$$

By inserting (2.88) and (2.89) into (2.87), we get the current drain I_D

$$I_D = W\,\mu_n\,C_{ox}\,(V_{GS} - V_{channel}(y) - V_T)\,\frac{dV_{channel}(y)}{dy} \tag{2.90}$$

After some routine manipulation

$$I_D\,dy = W\,\mu_n\,C_{ox}\,(V_{GS} - V_{channel} - V_T)\,dV_{channel} \tag{2.91}$$

By applying integral

$$I_{\mathrm{D}} \int_0^L dy = \tag{2.92}$$

$$= W\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}} \int_0^{V_{\mathrm{DS}}} (V_{\mathrm{GS}} - V_{\mathrm{channel}} - V_{\mathrm{T}})\, dV_{\mathrm{channel}}$$

After some integration

$$I_{\mathrm{D}} = \frac{W}{L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, {}^{V_{\mathrm{DS}}}{}_{0}[(V_{\mathrm{GS}} - V_{\mathrm{T}})\, V_{\mathrm{channel}} - \frac{V_{\mathrm{channel}}{}^{2}}{2}] \tag{2.93}$$

Traitor is in the linear region if

$$V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{T}}) \tag{2.94}$$

The drain current in the linear region is

$$I_{\mathrm{D}} = \frac{W}{L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, (V_{\mathrm{GS}} - \frac{V_{\mathrm{DS}}}{2} - V_{\mathrm{T}})\, V_{\mathrm{DS}} \tag{2.95}$$

For small V_{DS}

$$I_{\mathrm{D}} \cong \frac{W}{L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, (V_{\mathrm{GS}} - V_{\mathrm{T}})\, V_{\mathrm{DS}} \tag{2.96}$$

On Resistance between drain and source in the linear region for small V_{DS} voltage is

$$R_{\mathrm{DS-ON}} = \frac{V_{\mathrm{DS}}}{I_{\mathrm{D}}} \cong \frac{1}{\frac{W}{L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, (V_{\mathrm{GS}} - V_{\mathrm{T}})} \tag{2.97}$$

The condition for drain current in the saturation region is

$$V_{\mathrm{DS}} = V_{\mathrm{GS}} - V_{\mathrm{T}} \tag{2.98}$$

The drain current in the saturation region is for $V_{\mathrm{DS}} \geq V_{\mathrm{GS}}$-$V_{\mathrm{T}}$

$$I_{\mathrm{Dsat}} = \frac{W}{2\,L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, (V_{\mathrm{GS}} - \mathrm{V_T})^2 \tag{2.99}$$

Due to channel length modulation

$$I_{\mathrm{Dsat}} = \frac{W}{2\,L}\, \mu_{\mathrm{n}}\, C_{\mathrm{ox}}\, (V_{\mathrm{GS}} - V_{\mathrm{T}})^2\, (1 + \lambda\, V_{\mathrm{DS}}) \tag{2.100}$$

where λ is channel length modulation parameter.

2.1.10. Power Devices. Specific resistance

The specific resistance (resistance per unit area) of the ideal drift region is given from (2.14) by [81]

$$R_{\mathrm{on_sp}} = R_{\mathrm{on}}\, Area = \rho\, L = \frac{L}{q\, \mu_{\mathrm{n}}\, N_{\mathrm{D}}} \tag{2.101}$$

The depletion width under breakdown conditions for asymmetric junction $N_A >> N_D$ is given by (2.84) [81]

$$L_{D_BV} = \frac{2\,BV}{E_c} \tag{2.102}$$

The doping concentration in the drift region required to obtain this breakdown voltage BV is given by (2.83) [81]

$$N_D = \frac{\varepsilon_s\, E_c^{\,2}}{2\,q\,BV} \tag{2.103}$$

Combining relationships (2.101), (2.102), and (2.103) the specific resistance of the ideal drift region is [81], and [84]

$$R_{on_sp} = \frac{4\,BV^{\,2}}{\varepsilon_s\,\mu_n\,E_c^3} \tag{2.104}$$

The denominator of this equation ($\varepsilon_s.\mu_n.E_C^3$) is commonly referred to as Baliga's figure of merit for power devices.

For lateral devices, specific on-resistance is [85]

$$R_{on_sp} = \frac{BV^{\,2}}{q\,\mu_n\,n_s\,E_c^2} \tag{2.105}$$

where n_s is the sheet electron density in the channel. For lateral GaN HEMT with drain to source distance L_{DS} specific on-resistance is [86]

$$R_{on_sp} = \frac{L_{DS}^{\,2}}{q\,\mu_n\,n_s} = \frac{BV^{\,2}}{q\,\mu_n\,n_s\,(E_c^2 - E_P^2)} \tag{2.106}$$

where E_P is the polarization induced field in AlGaN/GaN heterostructure.

2.1.11. Power Super Junction Power Devices. Specific resistance

The drift region of a Super Junction (SJ) transistor is present in Fig. 2.8.

The specific resistance (resistance per unit area) of the ideal drift region of super-junction structure SJ (charge-coupled structure) is given from (2.14) by [81]

$$R_{on_sp} = R_{on}\,Area = \rho\,\frac{t_{SJ}}{AreaCh}\,Area \tag{2.107}$$

The specific resistance (resistance per unit area) of the ideal drift region is given from (2.14) by [81]

$$R_{on_sp} = \rho\,\frac{p}{W_N}\,t_{SJ} = \frac{t_{SJ}\,p_{SJ}}{q\,\mu_n\,N_D\,W_N} \tag{2.108}$$

where p_{SJ} is element dimension, and t_{SJ} is the thickness of the charge coupling region. The depletion width under breakdown conditions for symmetric junction N_A=N_D is given by (2.86), (2.84)

$$t = \frac{BV}{E_c} \tag{2.109}$$

It was found that the highest *BV* occurs when the charge in these regions is given by [81]:

$$Q_{\mathrm{opt}} = 2\, q\, N_{\mathrm{D}}\, W_{\mathrm{N}} = \varepsilon_{\mathrm{s}}\, E_{\mathrm{c}} \tag{2.110}$$

Combining these relationships, the specific resistance of the ideal super-junction region is obtaine [81]

$$R_{\mathrm{on_sp}} = \frac{2\, BV\, p_{SJ}}{\varepsilon_{\mathrm{s}}\, \mu_{\mathrm{n}}\, E_c^2} \tag{2.111}$$

It is visible that specific on-resistance of SJ transistor depend linearly on breakdown voltage BV and is proportionally inverse to quadrat of critical electric field E_c

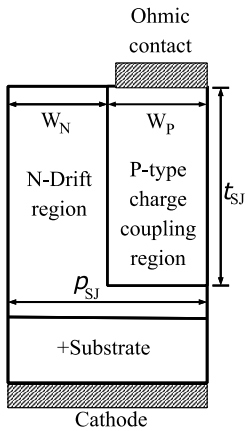


Fig. 2.8. A drift region of a Super Junction transistor [81].

2.2. Power MOSFETs Material & Topology Fundaments

For more than two decades, wide energy bandgap semiconductors, especially silicon carbide (SiC) and gallium nitride (GaN), have been touted as preferred semiconductors for developing compact, high-power, and high-temperature electronics systems because of their superior electrical and thermal characteristics compared to the semiconductor silicon. Although there has been significant investment and research in the past two decades, progress in developing low-cost and reliable SiC and GaN power devices has been slow. Unlike silicon, both SiC and GaN materials

contain a high density of crystal defects in the drift region of a power semiconductor switch; these defects are primarily caused by defects in the substrate material [87].

Devices based on the width band-gap materials suffer from a common drawback, namely the high resistivity of P-doped layers in SiC and also in some GaN normally-off designs, resulting in values of internal gate resistances higher than the ones found in Si devices. These two referred facts lead to a specific limitation on possible switching speed [88].

Gallium nitride is suitable for high-voltage, high temperature and high frequencies devices due to its remarkable material properties like wide bandgap (3.4 eV), which leads to a large critical electric field (3 MV/cm), reasonably high electron mobility with 2DEG (comparable to Si) and good thermal conductivity [63] Tab. 2.4 .

Tab. 2.4. Physical properties of Si, GaAs, GaN and SiC [87], and Diamond [89], (*) for 2DEG.

Property	**Si**	**GaAs**	**GaN**	**3C-SiC**	**6H-SiC**	**4H-SiC**	**Diamond**
Bandgap, E_g [eV at 300K]	1.12	1.43	3.4	2.4	3	3.2	5.45
Critical electric field, E_c [V/cm]	2.510^5	3.10^5	3.10^6	2.10^6	$2.5.10^6$	$2.2.10^6$	1.10^7
Thermal conductivity, λ [W/cmK at 300K]	1.5	0.5	1.3	3-4	3-4	3-4	22
Saturated electron drift velocity, v_{sat} [cm/s]	1.10^7	1.10^7	$2.5.10^7$	$2.5.10^7$	2.10^7	2.10^7	$2.7.10^7$
Electron Mobility, μ_n [cm^2/V•s]	1350	8500	1000 1500(*)	1000	500	950	2200
Hole Mobility, μ_p [cm^2/V•s]	480	400	30	40	80	120	850
Dielectric constant, ε_r [-]	11.9	13	9.5	9.7	10	10	5.5

The higher critical electric field of GaN allow to place source, drain and gate terminal closer together to reach smaller $R_{DS\text{-}ON}$ compare to Si, SiC o GaAs.

In addition, GaN is highly piezoelectric material and forms spontaneous polarization charges, and the orientation of the layer that is between two dissimilar materials, AlGaN and GaN in these devices causes a buildup of electrons at the AlGaN/GaN interface forming a thin sheet of electrons known as the two-dimensional electron gas (2DEG [90]). The GaN high electron mobility transistors (HEMT) with 2DEG are more widely used compare to GaN bulk devices because of almost 2-time better electron mobility.

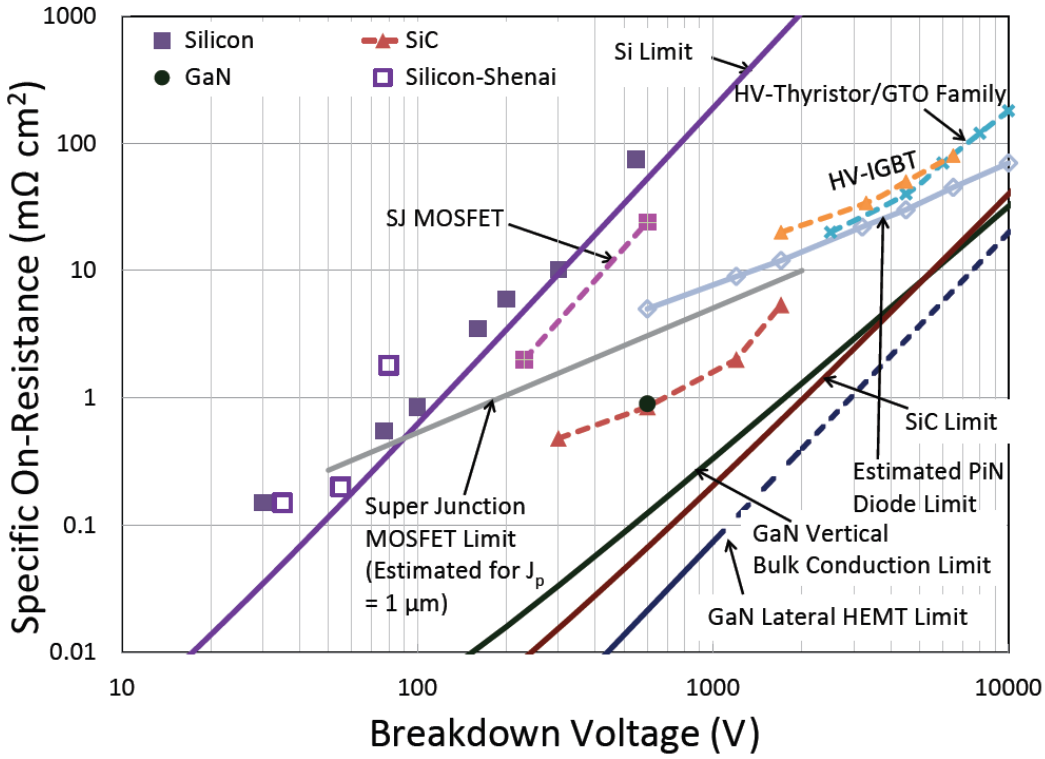


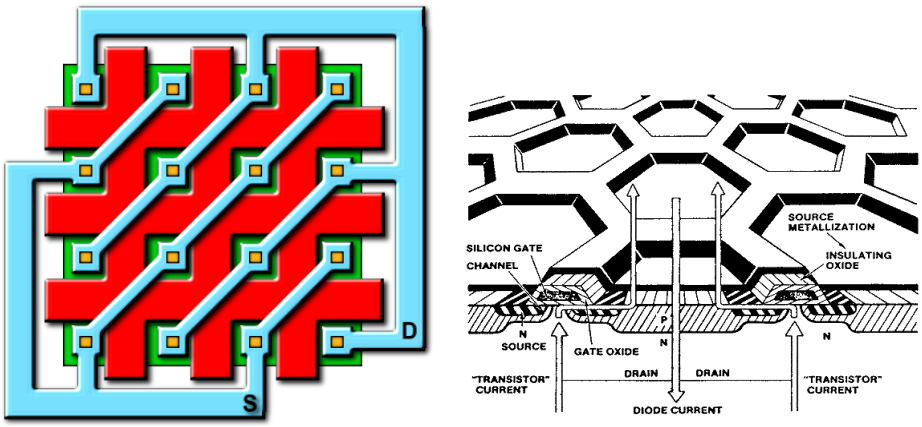
Fig. 2.9. Specific on-state resistance vs. avalanche breakdown voltage for commercial devices with material limits [91].

The specific on-resistance *Ron•Area* of the drift region for unipolar devices for different materials in mΩ.cm^2 is given by (2.104) [84] and its comparison is visible on Fig. 2.9.

2.2.1. Planar MOSFET

For LV power MOSFETs where source and drain have the same architecture, it is possible to use a gate with Waffle pattern (Fig. 2.10 a) to decrease specific on-resistance.

Silicon double diffused MOSFET (DMOS) structure with a hexagonal cell layout—known as “HexFET” Fig. 2.10 b) is widely used for power conversion below 1 kV and 100 A as it offers the highest cell packing density with improved ruggedness [91].

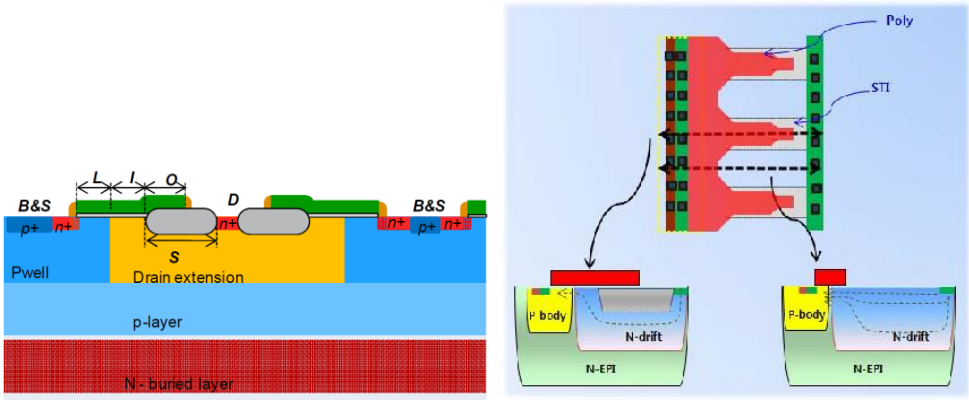


a) **b)**

Fig. 2.10. Planar MOSFETs a) The planar Gate with Waffle pattern for LV MOSFET, b) Cross section of DMOS HexFET [92].

Drift MOS transistors (Fig. 2.11 a) is widely used to realize high voltage NMOS in advanced BCD technology since they are both cost-effective, sharing the body implant/mask with the available CMOS one, and flexible, being the channel length a parameter that can be tuned for performance optimization [93].

One of the most advanced architecture based on Drift MOS is Interdigitated LDMOS (Fig. 2.11 b) where due to the specific gate and active pattern lower specific on-resistance was reached [94].

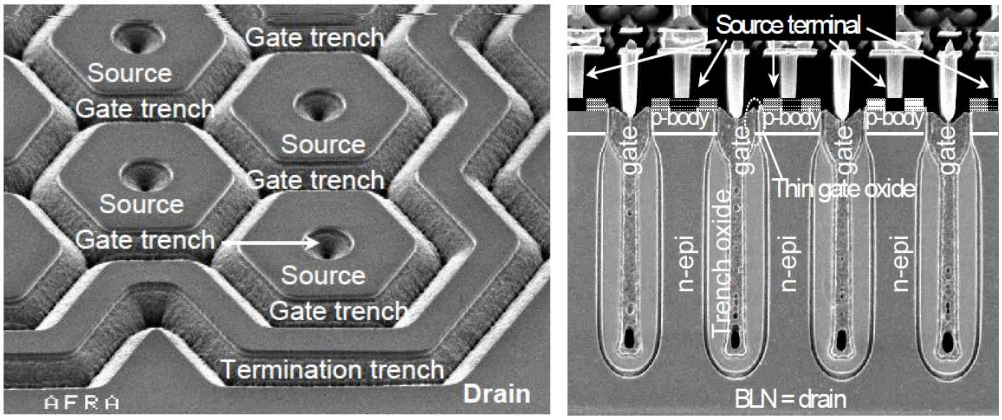


a) **b)**

Fig. 2.11. MOSFETs (a) Drift MOS with locos [93], (b) Proposed Interdigitated LDMOS. STI is partially removed, and the gate field plate is in the form of fingers. The current path is thus increased while depletion is maintained through a lateral field plate effect [94].

2.2.2. Trench MOSFET

The Trench MOSFET is currently a widely used architecture as a second generation of power MOSFETs overcoming the first generation based on DMOS architecture. The MOSFETs using the trench gate allow to reach lower specific on-resistance hence vertical structure to enhance the channel density. To improve the specific on-resistance of the Trench MOSFET architecture, the different trench gate pattern like Waffle [35] or hexagon in XtreMOS [95], [96] (Fig. 2.12) is used.



a) **b)**

Fig. 2.12. XtreMOS (a) Top-view of a hexagonal layout of the transistor, (b) Cross-section of the device, the BLN serves as the drain, contacted from the top the pbody layer serves as the vertical channel [95], [96].

2.2.3. Drain with RESURF

A higher breakdown voltage in vertical devices usually requires a thicker and lower doped epitaxial layer. However, in experimental IC samples with lateral isolation diffusion, a much higher breakdown voltage is obtained on a thinner layer: here the surface field at the isolation junction is decreased by 2-D depletion. This technology is called the REduced SURface Field (RESURF) effect and is one of the most widely-used methods for the design of lateral high-voltage and low on-resistance devices [97].

During the last 30 years was developed multiple of different RESURF structures [97] but for simplicity, we can describe just three different types of them. The single-RESURF, double-RESURF and triple-RESURF structures of lateral power MOSFETs are present in Fig. 2.13 [98].

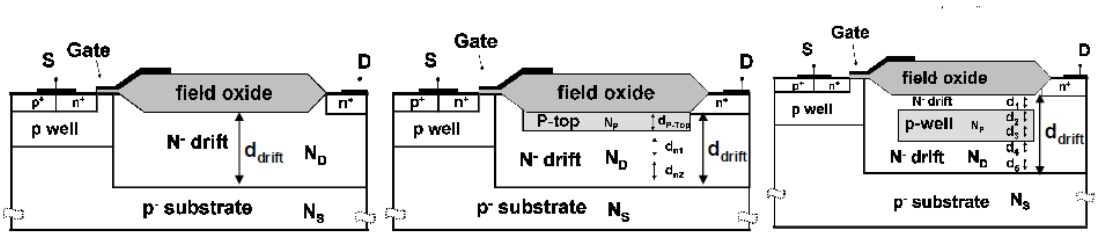


Fig. 2.13. Schematic structures of (a) single-RESURF, (b) double-RESURF, (c) triple-RESURF LDMOSFETs [98].

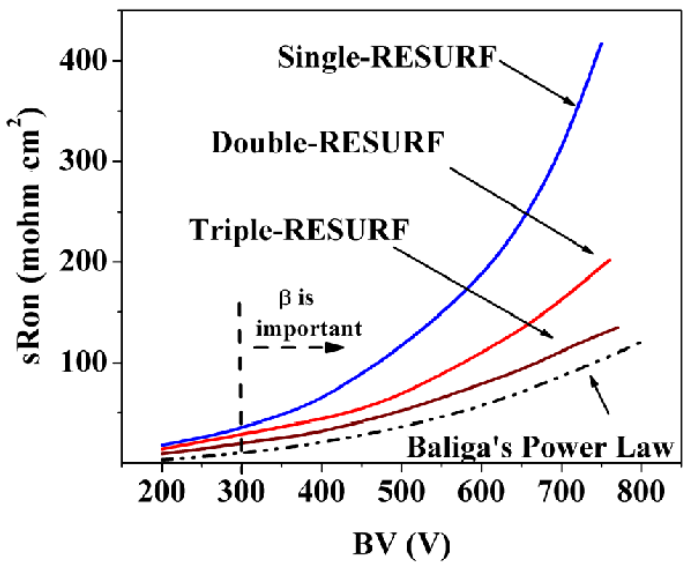


Fig. 2.14. Simulated RDSON-BV relationship comparison for RESURF technologies at 27°C (drift length vary from 10μm to 80μm) [98].

The *Ron•Area* -BV Power Law of a single-RESURF device at 27 °C is given by [98]:

$$R_{\text{on_sp}} = R_{\text{on}}\, Area = \ 5.93\ 10^{-9}\ 3.7\ (BV)^{2.5} \qquad (2.112)$$

The *Ron•Area* -BV Power Law of a double-RESURF device at 27 °C is given by [98]:

$$R_{\text{on_sp}} = R_{\text{on}}\, Area = \ 5.93\ 10^{-9}\ 5.8\ (BV)^{2.33} \qquad (2.113)$$

The *Ron•Area* -BV Power Law of a triple-RESURF device at 27 °C is given by [98]:

$$R_{\text{on_sp}} = R_{\text{on}}\, Area = \ 5.93\ 10^{-9}\ 32\ (BV)^{2} \qquad (2.114)$$

Comparison of all Power Law with different RESURF types is present in Fig. 2.14. The power law of triple-RESURF is better optimized because is closest to Baliga's Power Law.

2.2.4. Super Junction MOSFET

In Super Junction (SJ) -MOS, the drift region of the conventional DMOS is replaced by a set of alternating and highly doped N- and P-type semiconductor layers (pillars) as shown in Fig. 2.15, Fig. 2.16. In theory, the SJ structure results in high BV due to charge compensation in the pillars and low R_{ON} is achieved by highly doping in the pillars [99], [100]. The "ideal specific on-resistance" of the Super-junction MOSFET is equal to [101], [99]:

$$R_{\text{on_sp}} = R_{\text{on}}\, Area = \ 1.98\ 10^{-1}\, d^{5/4}\, (BV) \qquad (2.115)$$

where Ron•Area is in Ω.cm2 and BV in Volt and "*d*" is the P and N-layer width of Super-Junction MOSFET.

The Super-Junction devices are superior for very high voltage application (> 1000 V) because of the linear relation between the specific on-resistance and the breakdown voltage [101].

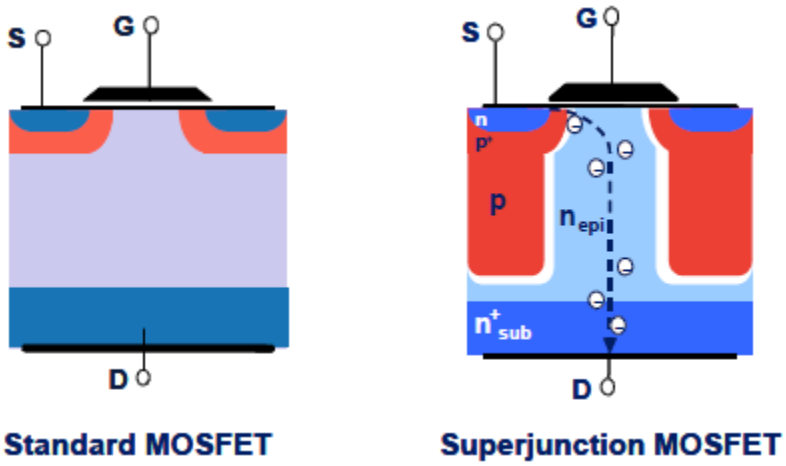
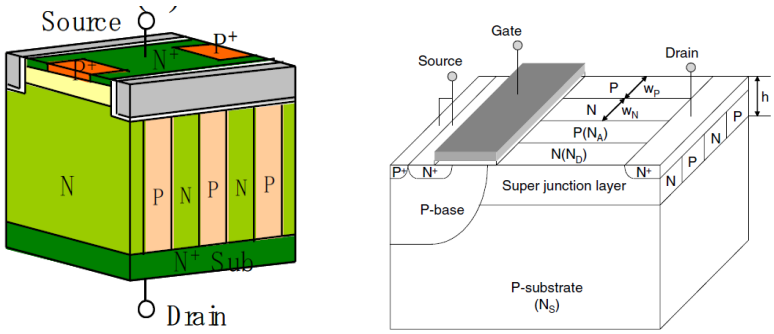


Fig. 2.15. Schematic Cross-Section of a Standard Power MOSFET versus a Superjunction MOSFET (CoolMOS™)

All CoolMOS™ series are based on the Superjunction principle, which is a revolutionary technology for high voltage power MOSFETs [99]. (Infineon Technologies has been the first company worldwide to commercialize this idea into the market [102]) The basic idea is simple: instead of having electrons flowing through

a relatively high resistive (high voltage blocking) n-area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, which go all the way straight through the device close to the back side n+ contact [103].

The breakdown voltage, specific on-resistance, and gate-to-drain charge of 736 V, 16.4 mΩ.cm^2, and 6 nC, respectively, have been achieved for the fabricated SJ-MOSFET [104].



a) **b)**

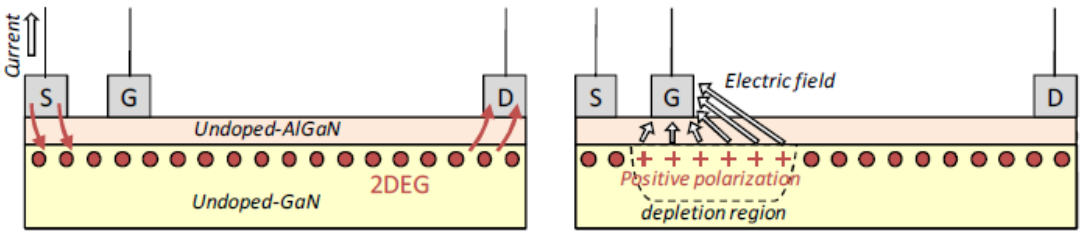
Fig. 2.16. Schematic 3D view of the designed SJ-LDMOSFET (a) vertical [105], (b) lateral [100]

In theory, the SJ structure results in high BV due to charge compensation in the pillars and low R_{ON} is achieved by highly doping in the pillars [99], [100].

2.2.5. GaN HEMT (Normally On)

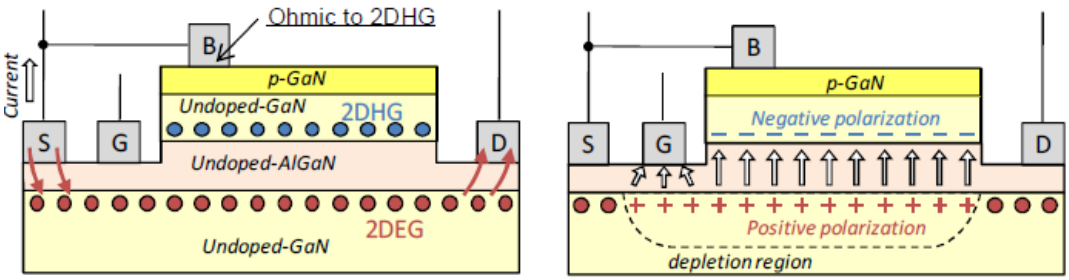
A two-dimensional electron gas with AlGaN/GaN heterojunction gives very high mobility in the channel and drain drift region, so resistance is much reduced compared to both Si and SiC [78].

The first generation of GaN High Electron Mobility Transistors (HEMT) was normally On and its schematic is in Fig. 2.17.



a) **b)**

Fig. 2.17. Schematic of a conventional HFET in a) the ON-state and b) the OFF-state. There are three electrodes which are the source (S), gate (G) and drain (D) [106].



a) **b)**

Fig. 2.18. Schematic of a Super HFET in a) the ON-state, b) the OFF state and There are four electrodes which are source (S), gate (G), drain (D) and base (B) [106].

The GaN Super Heterojunction Field Effect Transistors (Super HFETs) based on the polarization junction (PJ) concept are demonstrated on Sapphire substrates.

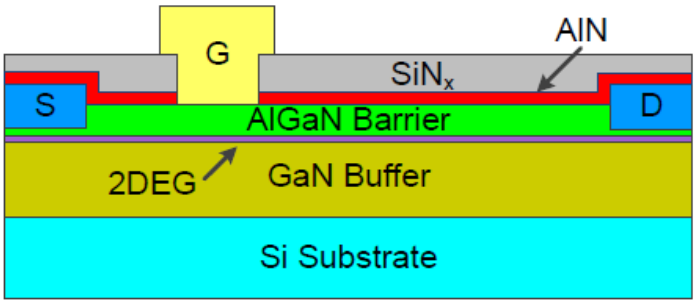


Fig. 2.19. Device cross-sectional schematic diagram of an AlGaN/GaNHEMT with a 4-nm AlN/50-nm SiNx stack as the passivation structure. The epi-structure includes a 3.8-µm GaN buffer layer and a 21-nm Al0.25Ga0.75N barrier layer. The T-gate structure features 1-µm gate footprint and 0.5-µm extension to both sides on top of SiNx. [107].

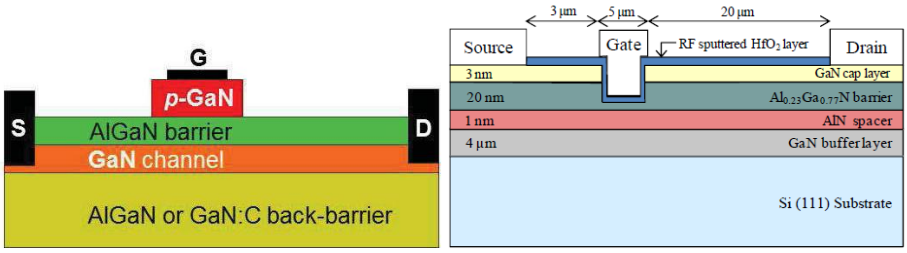
These Super HFETs were fabricated from a GaN/Al0.23Ga 0.77N/GaN heterostructure with a 2D hole and electron gas densities of 1.1×10^{13} and 9.7×10^{12}

cm^{-2} at the respective hetero-interfaces Fig. 2.18. The Super HFETs show breakdown voltage above 700 V with specific on-resistances of 3.3 mΩ·cm^2 [106].

The specific on-resistance of 1.3 mΩ.cm^2 for AlGaN/GaN HEMT transistor with 600V BV was achieved Fig. 2.19 [107].

2.2.6. GaN HEMT (Normally Off)

To fabricate normally-off AlGaN/GaN HEMTs, various methods such as fluorine-treated HFETs, p-type GaN gate [108], tunnel junction structure, and recessed gate structure [109] have reported. Fig. 2.20.



a) **b)**

Fig. 2.20. Schematic cross-section of GaN normally-off transistor using (a) p-GaN gate technology [108], (b) gate-recessed AlGaN/GaN MOS HEMTs [109].

2.2.7. Vertical GaN HEMT structures

Currently, both lateral and vertical structures are considered for GaN power devices. Vertical GaN power devices have attracted significant attention recently, due to the capability of achieving high breakdown voltage (BV) and current levels without enlarging the chip size, the superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management than lateral devices [110], [111].

Several structures have been proposed for vertical GaN transistors, with the highest BV close to 2 kV. Current aperture vertical electron transistor (CAVET) combines the high conductivity of a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction and the improved field distribution of a vertical structure [112] (Fig. 2.21 (a)). The CAVET is intrinsically normally-on, but a trench semi-polar gate could allow for normally-off operation [113] (Fig. 2.21 (b)). Vertical GaN trench MOSFETs have no 2DEG channels, but do not need the regrowth of AlGaN/GaN structures and are intrinsically normally-off [114] (Fig. 2.21 (c)). Recently, vertical fin

MOSFETs have been demonstrated to achieve normally-off operation without the need for p-type GaN materials or epitaxial regrowth [115] (Fig. 2.21 (d)) [111].

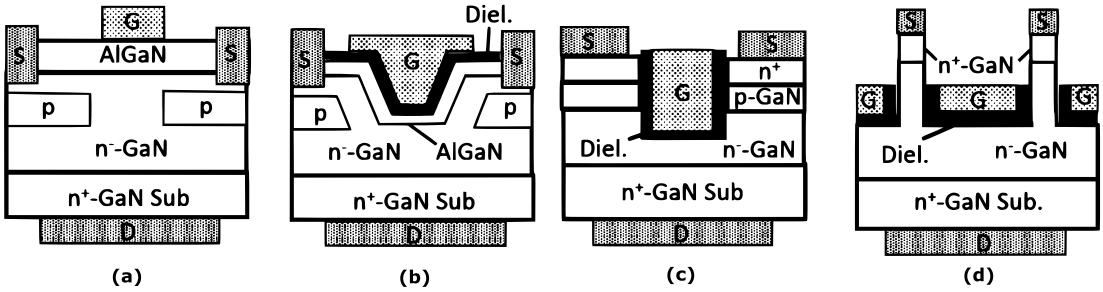
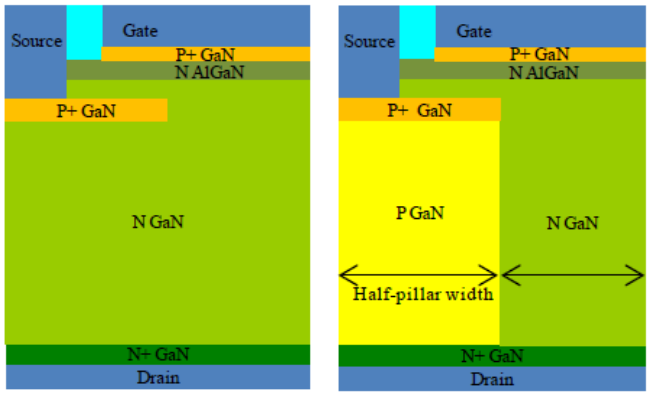


Fig. 2.21. Schematic of representative vertical GaN transistors: (a) CAVET, (b) trench CAVET, (c) trench MOSFET and (d) vertical fin MOSFET. In this figure, 'Diel.' stands for dielectrics, and 'Sub.' for substrates [111].

The GaN HEMT is possible to realize vertically as it is shown in Fig. 2.22. The breakdown voltage of 12.4 kV and specific on-resistance of 55.1 mΩ cm^2 for vertical GaN HEMT and of 4.2 mΩ·cm^2 for vertical superjunction AlGaN/GaN HEMT was simulated [116].



a) **b)**

Fig. 2.22. Schematic cross-section view of (a) GaN vertical HEMT, and (b) GaN vertical SJ HEMT [116].

2.2.8. GaN HEMT ICs

The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of AllGaN power ICs [4].

For GaN monolithic integration IC the lateral structures of HEMT are required.

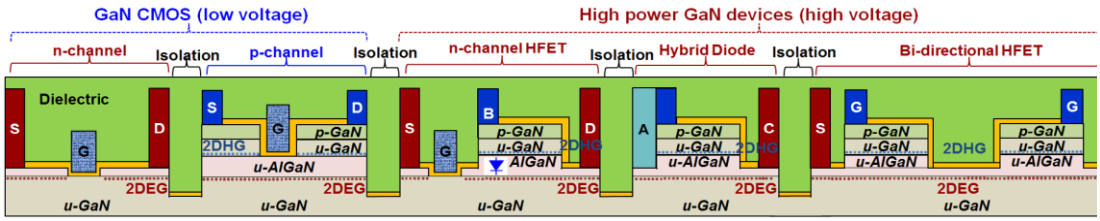


Fig. 2.23. Proposed PSJ platform for monolithic power integrated circuits the substrate is not specified, however, thin sapphire is the most cost-effective option because to serve for both low as well as high voltage devices and provide full electrical isolation (a critical requirement for monolithic integration) [58].

Early GaN power IC technology was published from university research [117]. The ability to integrate multiple power switches on a single chip is a big advantage for GaN power ICs. Isolating substrates began with sapphire and silicon carbide, though it was clear that an ability to grow GaN onto Si substrates enabled a cost structure and an ability to use existing large-diameter wafer fabs that would be a big cost and capacity advantage. Since Si is conductive, this introduces an additional challenge, of handling the substrate potential, and the way that it interacts with the power device. [4]

GaN has gained traction, and now discrete GaN transistors are emerging as commercial products [58]. Their performance is however limited to about 1/5 of their potential capability by slower external silicon gate driver circuits required to control them. Si circuits have a limited operating temperature range, and inherently efficient GaN devices are forced to slow down, leading to failure and severe derating of efficiency. The dual (Si & GaN) technology approach impacts cost deleteriously. By monolithically integrating control circuits with power devices on a single GaN technology platform Fig. 2.23 the efficiency can be greatly increased, and cost reduced [58].

2.2.9. GaN FinFET

The FinFET gate or 3D gate transistor approach was originally developed for pure digital CMOS process due to better channel control of nano-scale gate geometries. Original low voltage and low power determination were transformed to high voltage after replacing silicon channel with GaN. The concept of the junctionless transistor is very promising and suitable for the requirement of a new semiconductor device [59] Fig. 2.24.

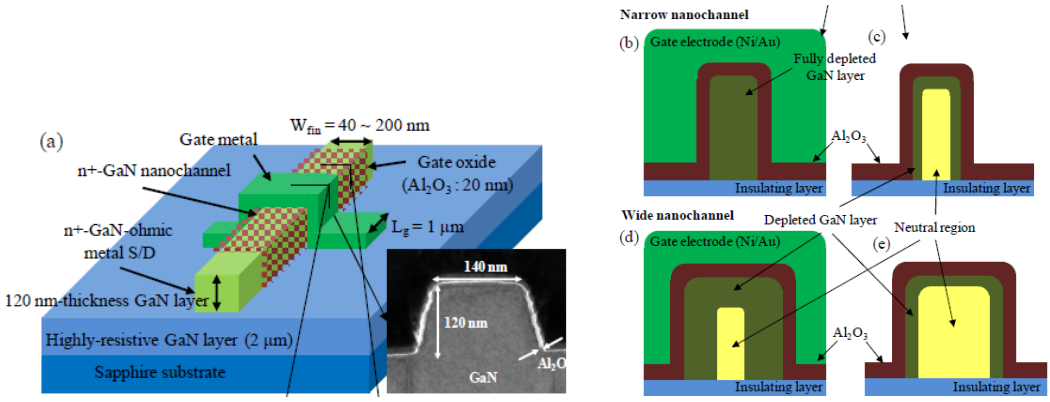


Fig. 2.24. FinFET (a) Three-dimensional schematic view of the proposed GaN nanochannel FinFET including epitaxial layers and device dimensions. (b-c) Narrow fin: The depletion region (dark green) extends in the whole body (full depletion) in off-state and gradually reduces with increasing gate bias. (d-e) Wide fin: the body cannot be fully depleted [59].

2.3. IC Yield Fundaments

Whether the circuit is made on bulk wafer material or epitaxial layers, the starting material always contains defects and, as the processing continues, other defects will be introduced by heat or chemical interaction. Some of these defects, associated with crystal imperfections, inclusions or precipitates (for instance, Cu on a stacking fault), or doping variations, may be serious enough to ruin the circuit performance. A single defect may give trouble, but sometimes the deterioration is more gradual and depends on the density or magnitude of the typical defect. The greater the chip area, the lower the yield. If the defects are uniformly distributed over the wafer, the yield Y for area A is given by [65]

$$Y = (Y_0)^{A/A_0} \tag{2.116}$$

Where Y_0 is the yield for area A_0. For instance, the probabilities of no defects in area 2 A_0 must be the product of the probabilities of defects in two areas A_0, namely $Y = Y_0^2$. If A_0 is chosen so that $Y_0 = 1/e$ then we have [65]

$$Y = e^{-A/A_0} \tag{2.117}$$

and the logarithm of yield is inversely proportional to chip area. The observed yield decrease is however usually at less than an exponential rate as suggested by Fig. 2.25 (a). This comes about because the defects tend to be clustered on the wafer instead of uniformly distributed [65].

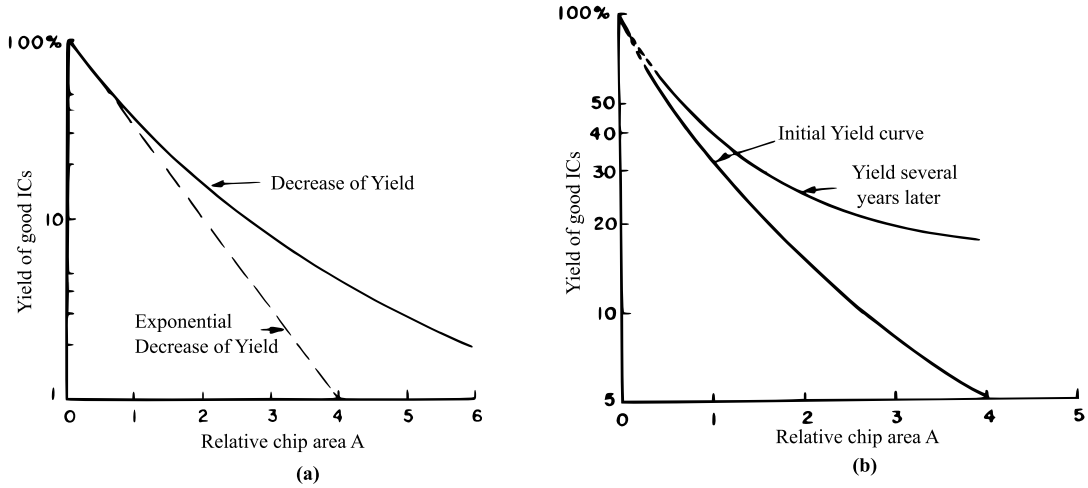


Fig. 2.25. Typical yield curves for ICs: (a) Yield of ICs decreases rapidly with the increase of chip area but usually at less than an exponential rate; and (b) Illustration of how IC yield may increase with time [65].

Based on the second law of thermodynamics the total entropy of an isolated system with time increase. This phenomena also influencing ICs yield and make it time dependence.

Under constant design rule conditions, larger area chips allow more circuit functions per IC, but the chance of including a defect increases by Fig. 2.25 (b) [65].

The conclusion is that smaller chip area improves the IC yield. Due to this power MOSFET area reduction in power ICs can be very beneficial for power IC yield improvement.

3. Analysis of MOSFET with Waffle Gate Patterns

The dimension scaling of LV power MOSFET in smart power IC is very beneficial due to efficiency improvement of power IC and due to production costs reduction by decreasing chip area and by it yield improvement. To fulfill that expectation several lateral LV waffle MOSFET are described and model.

Parts of this chapter has been published by the author of this thesis in [5], [6]. Author of this thesis contributes to this chapter by 90%.

3.1. Comparison Method

Related to MOS geometry the process design rules have to be defined. Often λ-based design rules are used. Then the relationship between scale factor λ and the feature sizes are as shown in Tab. 3.1 [66].

Tab. 3.1. Designed rules for MOS layout

Minimum Dimension Rules	***Name***	***Size***
Poly width	d_1	λ
Contact opening	d_2	$\lambda \times \lambda$
Contact-poly spacing	d_3	λ
Contact-contact spacing	d_4	λ
Poly-contact-poly spacing	$d_5=d_2+2.d_3$	3λ

For a quantitative comparison of different MOSFET structures, it is necessary to define a qualitative parameter for evaluation of benefits coming from more complex layout structures.

Drain current I_D in linear region of the MOSFET transistor with nonrectangular channel area is defined as (2.95)

$$I_D = \left(\frac{W}{L}\right)_{EF} \mu\, C_{ox}\, (V_{GS} - \frac{V_{DS}}{2} - V_T)\, V_{DS} \tag{3.1}$$

where V_{GS} is gate to source voltage, V_T is threshold voltage and V_{DS} is voltage between drain terminal to source terminal of the MOSFET, μ is charge-carrier effective mobility, C_{OX} is gate oxide capacitance per unit area and $(W/L)_{EF}$ is an effective width to length ratio of the channel.

For small V_{DS} where $V_{DS} << 2\ (V_{GS} - V_T)$, the drain current is linear function of V_{DS} described by

$$I_D \cong \left(\frac{W}{L}\right)_{EF} \mu\, C_{ox}\, (V_{GS} - V_T)\, V_{DS}. \tag{3.2}$$

From known drain current I_D, it is possible to define the resistance of path from the drain to the source marked as $R_{DS\text{-}ON}$ with neglecting contacts and diffusion resistance [66] marked as

$$R_{DS-ON} = \frac{V_{DS}}{I_D} \cong \frac{1}{\left(\frac{W}{L}\right)_{EF} \mu\, C_{ox}\, (V_{GS} - V_T)}. \tag{3.3}$$

For regular finger shape of the MOSFET channel, the on-resistance is proportional to the channel length L, inversely proportional to the channel width W, and inversely proportional to the width to length ratio of the channel $(W/L)_{fin}$

$$R_{fin} \cong \frac{1}{\left(\frac{W}{L}\right)_{fin} \mu\, C_{ox}\, (V_{GS} - V_T)}. \tag{3.4}$$

For MOSFETs with non-regular channel area such as waffle gate, the resistance R_{waf} is inversely proportional to the effective width to length ratio of the channel $(W/L)_{waf}$

$$R_{waf} \cong \frac{1}{\left(\frac{W}{L}\right)_{waf} \mu\, C_{ox}\, (V_{GS} - V_T)}. \tag{3.5}$$

In practice, the power MOSFET devices are described by a figure of merit parameter known as specific on-resistance and defined as resistance on device area. In our case the specific on-resistance of MOSFET with waffle gate sR_{waf} is

$$sR_{waf} = R_{waf}\, A_{waf} \tag{3.6}$$

where R_{waf} and A_{waff} is resistance respectively area of the MOSFET with waffle gate topology. The specific on-resistance can be used not only to compare power MOSFETs devices but also to calculate area for required resistance. The area of MOSFET devices with the same resistance for waffle gate topology and finger MOSFET $(A_{waf})_{Rfin}$ is described by following expression

$$(A_{\mathrm{waf}})_{\mathrm{R_{fin}}} = \frac{\mathrm{s}R_{\mathrm{waf}}}{R_{\mathrm{fin}}} = \frac{R_{\mathrm{waf}}\,A_{\mathrm{waf}}}{R_{\mathrm{fin}}} = \frac{\left(\frac{W}{L}\right)_{\mathrm{fin}} A_{\mathrm{waf}}}{\left(\frac{W}{L}\right)_{\mathrm{waf}}}. \tag{3.7}$$

The Area Increment *AI* of waffle MOSFET compared to finger MOSFET is

$$AI = \frac{(A_{\mathrm{waf}})_{\mathrm{R_{fin}}} - A_{\mathrm{fin}}}{A_{\mathrm{fin}}} = \frac{(A_{\mathrm{waf}})_{\mathrm{R_{fin}}}}{A_{\mathrm{fin}}} - 1 \tag{3.8}$$

where after insertion of (3.7) into (3.8) the Area Increment *AI* is

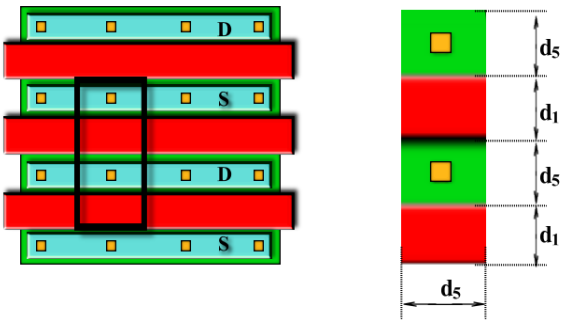
$$AI = \frac{A_{waf}\,R_{\mathrm{waf}}}{A_{fin}\;R_{\mathrm{fin}}} - 1 = \frac{A_{\mathrm{waf}}\left(\frac{W}{L}\right)_{\mathrm{fin}}}{A_{fin}\left(\frac{W}{L}\right)_{waf}} - 1. \tag{3.9}$$

The figure of merit parameter *AI* quantitatively defines how much the waffle structure area is required to achieve the same resistance as the standard MOSFET with finger gate topology has.

The same equation (3.9) can be derive by considering drain current in the saturation region (2.100) instead of (3.2).

3.2. Classical MOS with Gate's Fingers

One of the most used topology for low voltage MOS is the classical fingers MOS structures with all transistors in one common active area Fig. 3.1.



(a) **(b)**

Fig. 3.1. (a) Classical fingers MOS structure (b) Reference element.

The effective width to length ratio $(W/L)_{FING}$ of the elementary cell for classical fingers MOS structure is defined as follows

$$\left(\frac{W}{L}\right)_{\mathrm{FING}} = 2\left(\frac{d_5}{d_1}\right) \tag{3.10}$$

where d_1 is process parameter describing minimum polysilicon width and d_5 is minimum poly to poly spacing with considering contact between them.

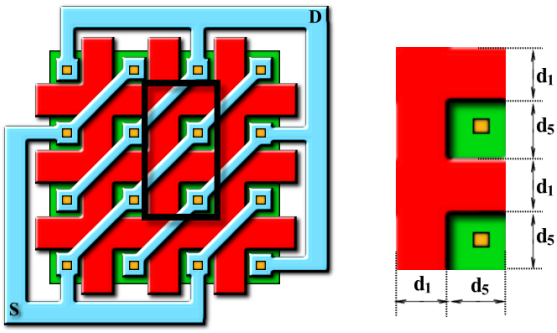
The elementary cell area A_{FING} is defined by minimum distance process parameters as follows

$$A_{\mathrm{FING}} = 2\,(d_1 + d_5)\,d_5 \tag{3.11}$$

3.3. MOS with Waffle Gate

The second topology to be considered is Waffle MOS structure. One of the specifics of Waffle MOS is polysilicon gate (waffle like) pattern and specific stagger Source (S) and Drain (D) terminal arrangement. To reconnect all Source and Drain staggered terminals usually diagonal metal interconnection routed at 45-degree angle is required.

The sub-element *B* of Waffle MOS (Fig. 3.4 b) has an effective width to length ratio with highly nonhomogeneous current distribution. As it was described in a previous publication [5] the value of this nonhomogeneous sub-element is not trivial, and conformal Schwarz-Christoffel Transformation mapping for calculation was used. The result of the calculation is as follows.



(a) **(b)**

Fig. 3.2. (a) Waffle MOS structure (b) Reference element.

The effective width to length ratio $(W/L)_{WAFF}$ for Waffle MOS elementary cell is defined as follows.

$$\left(\frac{W}{L}\right)_{\mathrm{WAFF}} = 4\left(\frac{d_5}{d_1}\right) + 2\left(\frac{W}{L}\right)_{\mathrm{B}} \tag{3.12}$$

Where coefficient $(W/L)_B$ represents width to length ratio of nonlinear element *B* defines in Fig. 3.4.b. The area occupied by Waffle MOS element is defined base on minimum process dimensions

$$A_{\mathrm{WAFF}} = 2\,(d_1 + d_5)^{\,2} \tag{3.13}$$

3.4. Schwarz-Christoffel Transformation

The one way how to perform effective channel *W/L* ratio calculation is to constructing a conformal mapping onto a new domain where the problem is trivial. In our case, that new domain should be a rectangle [118]. Base on Riemann mapping theorem we know that for any polygon exist mapping to open unit disk. The mapping from unit disk to any polygon is called Schwarz-Christoffel transformations [119]. The mapping h from W_1 plane to W_2 plane should be done as the composition of two independent SC mapping as shown in Fig. 3.3. First is inverse SC mapping f^{-1} from element polygon E to the unit disk P. And second mapping is SC mapping g from unit disk P to rectangular polygon Q [118]

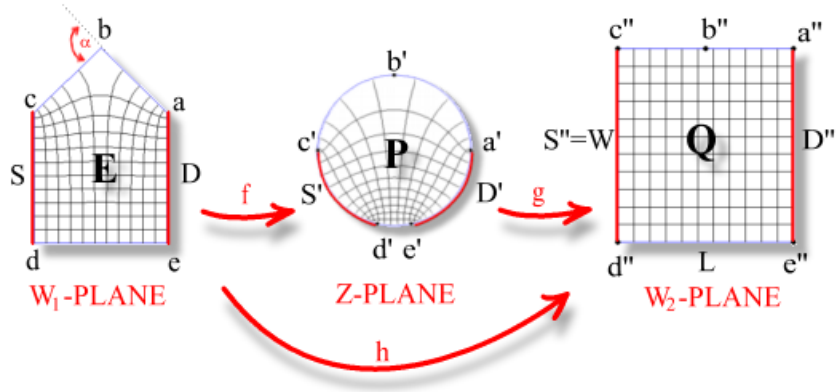


Fig. 3.3. Conformal map of an elementary polygon onto an equivalent rectangle [5].

$$\mathrm{f}^{-1}(z) = K + C \int_0^z \prod_{k=1}^{5} (1 - w/z_k)^{-\beta_k}\, dw \tag{3.14}$$

where K, C, and z_k are unknown complex constants and $|z_k|=1$. The exponents β_k are associated with angles at k-th corners points in plane W_1 and

$$\beta_k = 1 - \frac{\alpha_k}{\pi} \tag{3.15}$$

where α_k are exterior angels for points $z_k = \{a, b, c, d, e\}$ in plane W_1 and where $\beta_1=\beta_3=3/4$, $\beta_2=\beta_4=\beta_5=1/2$. The mapping g from unit disk P to rectangular polygon Q is

$$g(z) = \int_0^z [t(w)]^{-1/2}\, dw \tag{3.16}$$

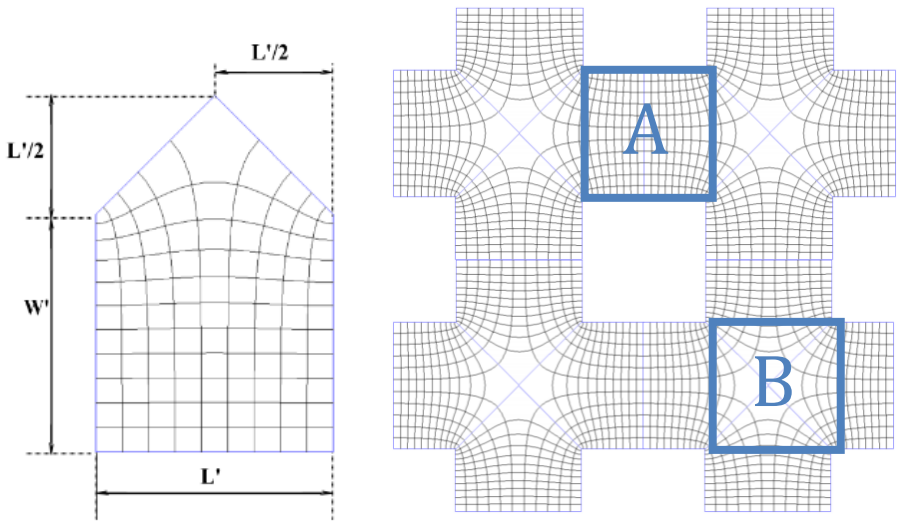
where

$$t(w) = (w - a')(w - c')(w - d')(w - e') \tag{3.17}$$

The constant *K*, *C* in equation (3.14) was skipped there because they have only influence on position and scale of the polygon and *W/L* ratio is invariant for them. Because *W/L* ratio of polygon *E* is equivalent to polygon *Q* to get the effective *W/L* ratio of *E*, it needs to calculate just three points of polygon *Q*

$$\left(\frac{W}{L}\right)_{\mathrm{E}} = \frac{|g(e') - (a')|}{|g(c') - (a')|} = 1.13967 \pm 10^5 \tag{3.18}$$

After the composition of four elements *E* we should get macro-element as shown in Fig. 3.4.b. This macro-element contains four times area *A* type on the periphery and one area *B* type located in the center.



(a) **(b)**

Fig. 3.4. (a) Proposed element E with defined dimensions and containing conformal mapping mash (b) Macro element with orthogonal mesh after SC transformation with area type A and B.

To get effective *W/L* ratio of element *B*, it is needed to have an effective ratio for region *A* first. In Fig. 3.4 (b) is seen that element *A* is not precisely homogeneous and contain some small no homogeneity close to the common boundary with element *B* type. To do not lose the high precision of *W/L* ratio reached for element *E*, all no homogeneity of region *A* are shifted and calculated in already nonhomogeneous

element *B* type. It means that we consider element *A* type as entirely homogenous. In our case where width dimension *W'* is equal to length dimension *L'* effective ratio is

$$\left(\frac{W}{L}\right)_{\mathrm{A}} = \frac{W'}{L'} = \frac{|a-e|}{|e-d|} = \frac{L'}{L'} = 1 \tag{3.19}$$

The effective *W/L* ratio of element *B* is composition of *W/L* ratio of four elements *E* and subtraction of *W/L* ratio of four elements *A*

$$\left(\frac{W}{L}\right)_{\mathrm{B}} = 4\left(\left(\frac{W}{L}\right)_{\mathrm{E}} - \left(\frac{W}{L}\right)_{\mathrm{A}}\right) \tag{3.20}$$

Numerical value is follows [5]

$$\left(\frac{W}{L}\right)_{\mathrm{B}} = 0.55871 \pm 10^5 \tag{3.21}$$

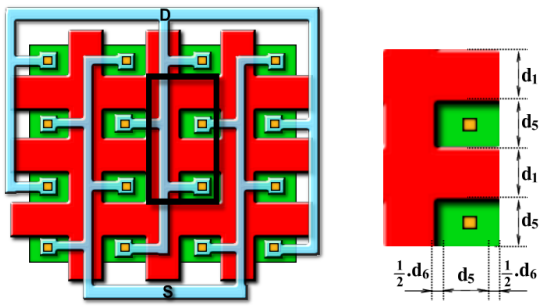
For whole MOSFET with waffle gate the total width to length ratio is [5]

$$\left(\frac{W}{L}\right)_{\mathrm{waf}} = M_A \frac{W'}{L'} + M_B\, 0.55871 \pm 10^5 \tag{3.22}$$

Where M_{A} is total number of homogenous element A and with geometrical dimension width *W*' and length *L*' and M_{B} is total number of nonhomogeneous element B.

3.5. MOS with Asymmetric Waffle Gate

One disadvantage of Waffle MOS structure is that due to diagonal metal interconnection routed at 45-degree angle in same processes we should violate design rules. In such cases, alternative orthogonal routing should be applied [69] (Fig. 3.5). Advantages coming from orthogonal routing are not for free because due to more complex metallic interconnection the larger contact spacing is required and determine.



(a) (b)

Fig. 3.5. (a) Asymmetric Waffle MOS structure (b) Reference element.

The effective width to length ratio $(W/L)_{A\text{-}WAFF}$ of Asymmetric Waffle MOS elementary cell is defined as follows

$$\left(\frac{W}{L}\right)_{\mathrm{A-WAFF}} = 2\left(\frac{d_5}{d_1} + \frac{d_5 + d_6}{d_1} + \left(\frac{W}{L}\right)_{\mathrm{B}}\right) \tag{3.23}$$

where d_6 dimension represent an enlargement of contact to poly spacing compare to minimum dimension due to more complex interconnection. The area occupied by Asymmetric Waffle MOS element is defined as follows

$$A_{\mathrm{A-WAFF}} = 2\,(d_1 + d_5)\,(d_1 + d_5 + d_6) \tag{3.24}$$

3.6. Comparison

As was mention earlier the equation (3.9) describing increment of the area is used in this work to describe the area saving and to compare between two different Waffle MOS topologies.

Let's define the area increment for Waffle MOS structure $AI_{WAFF,\ FING}$. The reference element area A_{REF} is represented by element area of classical fingers MOS structure A_{FING}. Moreover, required area A_{REQ} is represented by element area of Waffle MOS structure A_{WAFF}. After insertion of (3.10), (3.11), (3.12), (3.13) to equation (3.9) we obtain the following formula

$$AI_{\mathrm{WAFF,FING}} = \frac{A_{\mathrm{WAFF}} - A_{\mathrm{FIN}}}{A_{\mathrm{FIN}}} = \frac{A_{\mathrm{WAFF}}\left(\frac{W}{L}\right)_{\mathrm{FIN}}}{A_{\mathrm{FIN}}\left(\frac{W}{L}\right)_{\mathrm{WAFF}}} - 1 = \\ = \frac{d_1 - \left(\frac{W}{L}\right)_{\mathrm{B}} d_1 - d_5}{\left(\frac{W}{L}\right)_{\mathrm{B}} d_1 + 2\,d_5} \tag{3.25}$$

The area increment for Asymmetric Waffle MOS

$$AI_{\mathrm{A-WAFF,FING}} = \frac{A_{\mathrm{A-WAFF}} - A_{\mathrm{FIN}}}{A_{\mathrm{FIN}}} = \frac{A_{\mathrm{A-WAFF}}\left(\frac{W}{L}\right)_{\mathrm{FIN}}}{A_{\mathrm{FIN}}\left(\frac{W}{L}\right)_{\mathrm{A-WAFF}}} - 1 = \\ = \frac{d_1 - \left(\frac{W}{L}\right)_{\mathrm{B}} d_1 - d_5}{\left(\frac{W}{L}\right)_{\mathrm{B}} d_1 + 2\,d_5 + d_6} \tag{3.26}$$

structure $AI_{A\text{-}WAFF,\ FING}$ is calculated similar way by insertion (3.10), (3.11), (3.23), (3.24) to equation (3.9).

If we expect that Asymmetric Waffle MOS has dimension d_6 always greater than zero, from (3.25), (3.26), we can get

$$\frac{d_1 - \left(\frac{W}{L}\right)_{\mathrm{B}} d_1 - d_5}{\left(\frac{W}{L}\right)_{\mathrm{B}} d_1 + 2\,d_5 + d_6} < \frac{d_1 - \left(\frac{W}{L}\right)_{\mathrm{B}} d_1 - d_5}{\left(\frac{W}{L}\right)_{\mathrm{B}} d_1 + 2\,d_5} \tag{3.27}$$

From (3.25), (3.26), (3.27) we can get the relation between area efficiency of Waffle MOS and Asymmetric Waffle MOS

$$AI_{\mathrm{A-WAFF,FING}} < inc_{\mathrm{WAFF,FING}} \tag{3.28}$$

Process parameters to be used for calculation are considered minimum process dimensions. Just for Dual oxide process the two times longer channel length d_1 is considered as it is seen in Tab. 3.2.

Tab. 3.2. Designed rules for different processes

	Standard process	***Dual oxide process***
d_1	λ	2λ
d_5	3λ	3λ
d_6	λ	-

Because in Dual oxide process the channel length d_1 is considered two times larger, this space is large enough also for more complex orthogonal metal routing of Asymmetric Waffle MOS. Due to this, there is no need to reserved additional space for Asymmetric Waffle MOS, and d_6 is equal to zero. So Waffle MOS with orthogonal metal routing shouldn't be asymmetrical in Dual oxide process.

The final results comparing different Waffle MOS topologies and different dimensions by using Table 5.2 and equations (3.25), (3.26) are present in Tab. 3.3.

Tab. 3.3. Comparison of area increment for different layout structures

	Standard process	***Dual oxide process***
Waffle MOS	-39.0%	-29.7%
Asymmetric Waffle MOS	-33.8%	-

As it is describe in Tab. 3.3.the area improvement of Waffle MOS compare to Classical fingers MOS structure is -39.01%. This value is slightly more precise than

value -38.9% described by Saqib [66]. The improvement was reached due to using the more precise coefficient of element B= 0.55871 instead of 0.55.

3.7. Topological Waffle MOS Limit

As was mention previously change of geometry has a significant influence on resistance per area. Due to this, we can investigate maximum allowed Waffle gate geometry where MOS topology became ineffective compared to standard finger gate pattern. To find this threshold shape we have to simplify equation (3.25). To do so let's define the aspect ratio (*AR*) parameter as follows.

$$AR = \frac{d_1}{d_5} \tag{3.29}$$

Where d_1 is polysilicon width, and d_5 is minimum polysilicon to polysilicon spacing with a contact in the middle. After insertion of equation (3.29) into equation (3.25) we can get more straightforward description of area increment of Waffle MOS.

$$AI_{\mathrm{WAFF,FING}} = \frac{1 + \mathrm{AR}}{2 + AR\left(\frac{W}{L}\right)_{\mathrm{B}}} - 1 \tag{3.30}$$

As it is visible, the area increment of Waffle MOS patter is now dependent only on one variable parameter *AR*. Because of this, we can visualize area increment of Waffle MOS in 2D graph Fig. 3.6

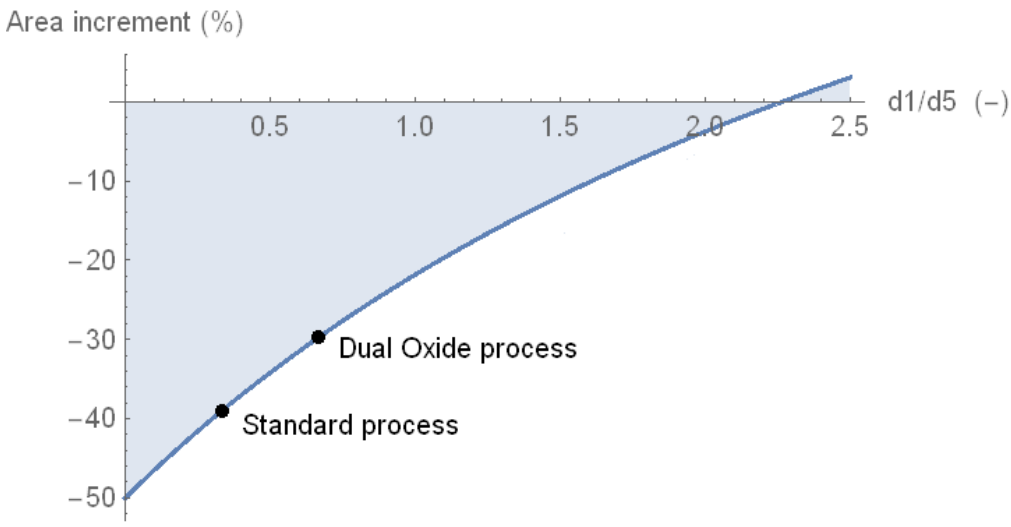


Fig. 3.6. Area Increment dependence on geometry (d_1/d_5) of Waffle MOS structure [6].

On the graph, it is possible to see not just standard process area increment and dual oxide process area increment but also point where area increment of Waffle MOS become zero. After that threshold point, the area increment of Waffle MOS is positive, and Waffle gate pattern become no more useful for area saving.

To quantify the boundary of Waffle MOS use case we have to set equation (3.30) equal to zero. It corresponds to point where area increment of Waffle MOS becomes zero.

$$AI_{\mathrm{WAFF,FING}} = 0 \tag{3.31}$$

Under that condition we get from equation (3.31) specific Aspect Ratio *AR* value as follows:

$$AR = 2.26 \tag{3.32}$$

After that ratio (3.32) the Waffle gate pattern become useless in term of area saving. It means that if polysilicon width d_1 is 2.26 times larger than the spacing between polysilicon d_5 than Waffle gate pattern (compare to standard gate pattern with fingers) is worst in term of resistance per area.

Finally, we can define dimensions constrains for Waffle gate pattern where resistance per area is better than with Standard fingers gate pattern. It is useful to use Waffle gate pattern only when, gate length d_1 is smaller than 2.26 times the spacing between polysilicon gates d_5 [6]

$$d_1 < 2.26\, d_5. \tag{3.33}$$

3.8. Alternative Calculation of Cross Element in the Channel of Waffle MOS

This chapter describes the alternative calculation of width to length ratio of a cross element based on a known analytic model for trapezoid.

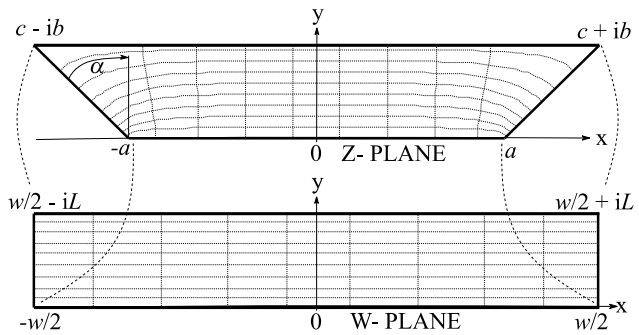


Fig. 3.7. Conformal map of trapezoid elementary polygon onto an equivalent rectangle by use Schwarz-Christoffel transformation.

The analytic model of trapezoid *W/L* ratio by use Schwarz-Christoffel transformation is [120]

$$\left(\frac{W}{L}\right)_t = \frac{2\,a}{b} - 7\;10^{-5}\,\alpha^2 + 1.57\;10^{-2}\alpha - 2\;10^{-3} \tag{3.34}$$

where α is in degrees, and there is 1 percent accuracy for

$$\frac{2\,a}{b} > 1.4 \tag{3.35}$$

The trapezoid *W/L* ratio for α=45° is

$$\left(\frac{W}{L}\right)_{\text{trap45}} = \frac{2\,a}{b} + 0.56275 \tag{3.36}$$

For half trapezoid the *W/L* ratio is

$$\left(\frac{W}{L}\right)_{\text{trap_half}} = \frac{1}{2}\;\left(\frac{W}{L}\right)_{\text{trap45}} \tag{3.37}$$

For two half trapezoid connected in series, the *W/L* ratio $(W/L)_{\text{H}}$ is

$$\left(\frac{W}{L}\right)_{\text{H}} = \frac{1}{2}\;\left(\frac{W}{L}\right)_{\text{trap_half}} = \frac{1}{4}\;\left(\frac{W}{L}\right)_{\text{trap45}} \tag{3.38}$$

The waffle element contains four half trapezoid connected in series and the *W/L* ratio $(W/L)_{\text{waf}}$ is

$$\left(\frac{W}{L}\right)_{\text{waf}} = 4\,\left(\frac{W}{L}\right)_{\text{H}} = \left(\frac{W}{L}\right)_{\text{trap45}} = \frac{2\,a}{b} + 0.56275 \tag{3.39}$$

By replacing $a=d_5/2$ and $b=d_1/2$ the waffle element *W/L* ratio is

$$\left(\frac{W}{L}\right)_{\text{waf}} = \frac{2\,W'}{L'} + 0.56275. \tag{3.40}$$

Equation (3.40) can reach accuracy less than 1 % for following inputs

$$\frac{L'}{W'} = \frac{d_1}{d_5} < 1.4. \tag{3.41}$$

While having the same resistance. This calculated

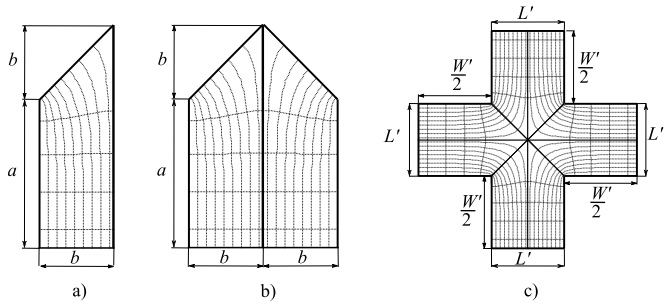


Fig. 3.8. Composition of cross element: a) half of trapezoid; b) two of half trapezoid connected in series; c)

The width to length ratio of element B calculated from trapezoid analytic formula is as follow

$$\left(\frac{W}{L}\right)_{\mathrm{B}} = \left(\frac{W}{L}\right)_{\mathrm{waf}} - \frac{2\,W'}{L'} = 0.56275. \tag{3.42}$$

The effective W/L channel ratio of the element A is directly aspect ratio of rectangle A. The effective W/L channel ratio of cross element type B in Waffle MOS is 0.55871 with tolerance 10^{-5}. It is much precise value than 0.55 described by Saqib [66].

If polysilicon width d_1 is 2.26 times larger than spacing between polysilicon d_5, than waffle gate pattern in term of resistance per area is always worse than standard gate pattern with fingers. It is useful to use waffle gate pattern only when, gate length d_1 is smaller than 2.26 times the spacing between polysilicon gates d_5

3.9. Conclusion for Waffle Topologies

The effective W/L channel ratio of the homogenous elements A is directly aspect ratio of rectangle A. The effective *W/L* channel ratio of cross element B in Waffle MOS is 0.55871 with tolerance 10^{-5}. It is much precise value than 0.55 described by Saqib [66]. It is useful to use waffle gate pattern in case, when the gate length d_1 is smaller than 2.26 times a spacing between polysilicon gates d_5. In opposite case, when polysilicon width d_1 is 2.26 times larger than the spacing between polysilicon d_5 then waffle gate pattern in term of resistance per area is worse than standard gate pattern with fingers.

4. Model Considering Edge Elements

Parts of this chapter has been published (currently is in the review) by the author of this thesis in [9]. Author of this thesis contributes to this chapter by 85%.

4.1. Waffle and Finger Structure Model Considering Edge Elements

The advantage is that waffle gate topology patterns does not require any further adjustment of the process. This study introduces a new model allowing description and comparison of two waffle gate patterns. The former one is a MOSFET with waffle gate topology and with orthogonal source and drain interconnection (Fig. 4.13). This metal interconnection is more robust in term of serial resistance and electro-migration than Madhyastha used [69]. The latter one is MOSFET with waffle gate topology and diagonal source and drain interconnections (Fig. 4.11). Both of them are compared with a standard MOSFET with finger gate topology (Fig. 4.9).

Tab. 4.1. General designed rules for MOS layout [66].

Minimum Dimensions	**Name**	**Size** [-]
Poly width	d_1	λ
Contact-opening	d_2	λ x λ
Contact-poly spacing	d_3	λ
Contact-contact spacing	d_4	λ
Poly -poly spacing with contact	$d_5 = d_2 + 2\ d_3$	$3\ \lambda$
Poly-poly spacing with diagonal contact	$d_{d5} = \sqrt{2}\ d_2 + 2\ d_3$	$(\sqrt{2} + 2)\ \lambda$

The IC fabrication process follows every process design rules that are collected in a design rule manual (DRM). Related to MOSFET geometry, the process design rule is often based on the scale process factor λ [66], [68]. Then the relationship between scale factor λ and the feature sizes is as shown in Tab. 4.1 [66]. Dimension d_5 defines a minimum spacing between polysilicon gates with a contact to diffusion in between

(see Fig. 4.10). Dimension d_{d5} defines a spacing between gates with the contact to diffusion in between but contact is rotated about 45° (see Fig. 4.14).

To support devices of higher voltage range from dual oxides processes, the gates length is also considered larger than minimum. In other words in this article, the gate length d_1 can acquire a larger dimension than the minimum value defined in Tab. 4.1.

Standard MOSFET Structure with Finger Gates

The basic MOSFET structures have finger gate topology where each finger has rectangular shape of channel region as can be seen in Fig. 4.9. For correct and robust well polarization, the bulk connections are created on each side of the MOSFET.

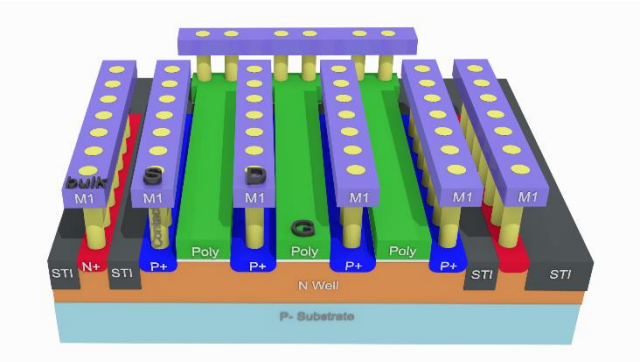


Fig. 4.9. Standard P-channel MOSFET with finger gate (G) and orthogonal source (S) and drain (D) terminals with bulk connection on each sides [9].

From a layout point of view, the bulk connection divides the whole power MOSFET into smaller segments. These parts are repeated over all structure. An example of segment of standard MOSFET topology with two finger gates without bulk connection is described in Fig. 4.10. The Y dimension of this standard MOSFET and its width in general are defined as a real number. In this publication it is considered as a discrete value due to alignment with waffle MOSFET dimensions and to simplify analytic model. Due to this Y dimension of the standard MOSFET, it is possible to scale by an equivalent number of gate fingers N_{yF} in Y-axis.

For full analytical description it is important to define not just dimensions of whole structure but also its subparts called core area. The core area A_{FC} of the standard MOSFET with finger gate and without considering peripheral area outside the core area is

$$A_{FC} = (d_1 + d_5)^2 N_{xF} N_{yF} \tag{4.1}$$

where N_{xF} is a number of gate fingers in X-axis direction. Since the core area does not always contain whole contacts inside the boundary but also their fractions (Fig.

4.10). It is important to define area enlargement to allow fit of whole contacts into the boundary. In this publication, we consider enlargement of the core area about $d_5/2$ on each side in X and Y-axis. After that, the total area of the standard MOSFET with finger gates A_F is

$$A_F = (d_5 + (d_1 + d_5)\, N_{xF})\, (d_5 + (d_1 + d_5)\, N_{yF}). \qquad (4.2)$$

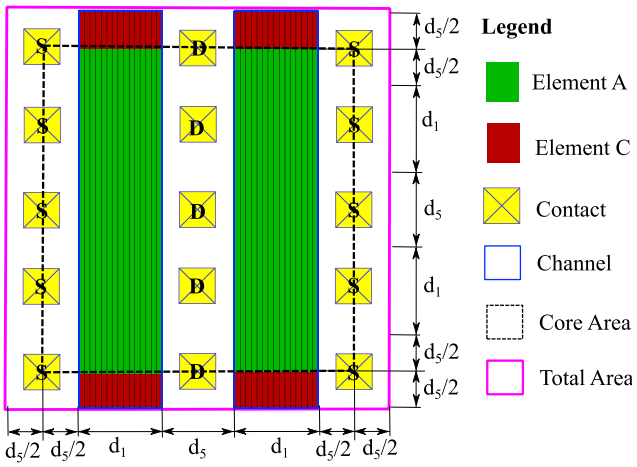


Fig. 4.10. Dimensions and portioning of channel area in the segment of Standard MOSFET with finger gate and with orthogonal source (S) and drain (D) terminals to element A and peripheral element C, the whole and core structure dimension is N_{xF}=2, N_{yF}=2 [9].

The width to length channel ratio in the core area for the standard MOSFET with finger gates WL_{FC} is

$$WL_{FC} = \frac{(d_1 + d_5)\, N_{xF}\, N_{yF}}{d_1} \qquad (4.3)$$

and the width to length channel ratio for the standard MOSFET with finger gates on total area WL_F is

$$WL_F = \frac{N_{xF}\, (d_5 + (d_1 + d_5)\, N_{yF})}{d_1}. \qquad (4.4)$$

4.2. Waffle MOSFET Structure with Diagonal Source and Drain

The MOSFETs with waffle gate topology have diagonal interconnections of source and drain terminals comparing to the standard MOSFET with finger gate topology (Fig. 4.11). The presented structure is compatible with all processes where diagonal

interconnection is allowed and where the waffle shape polysilicon gates do not violate the process design rules. No additional process steps are required. The portioning of the channel area of the waffle MOSFET segment is on Fig. 4.12.

Core area A_{WdC} of the MOSFET with waffle gates and diagonal source and drain interconnections without considering peripheral area outside the core area is

$$A_{\mathrm{WdC}} = (d_1 + d_5)^2 \, N_{\mathrm{xWd}} \, N_{\mathrm{yWd}} \tag{4.5}$$

where N_{xWd} is a number of gate fingers in X-axis direction and N_{yWd} is a number of gate fingers in Y-axis direction. The total area of the MOSFET with waffle gates and diagonal source and drain interconnections A_{Wd} is

$$A_{\mathrm{Wd}} = \\ = (d_5 + (d_1 + d_5)\, N_{\mathrm{xWd}})\,(d_5 + (d_1 + d_5)\, N_{\mathrm{yWd}}). \tag{4.6}$$

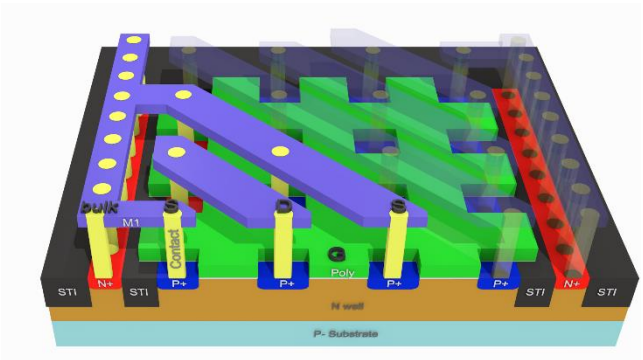


Fig. 4.11. P-channel MOSFET with waffle gate (G) and diagonal source (S) and drain (D) interconnections with bulk connection on each sides [9].

The width to length channel ratio in core area WL_{WdC} for the MOSFET with waffle gates and diagonal source and drain interconnections is

$$WL_{\mathrm{WdC}} = N_{\mathrm{xWd}} \, N_{\mathrm{yWd}} \left(\frac{2\, d_5}{d_1} + WL_{\mathrm{B}}\right). \tag{4.7}$$

The width to length channel ratio WL_{Wd} of the MOSFET with waffle gates and diagonal source and drain interconnections on total area is

$$WL_{\mathrm{Wd}} = \frac{d_5 (N_{\mathrm{xWd}} + N_{\mathrm{yWd}} + 2\, N_{\mathrm{xWd}} \, N_{\mathrm{yWd}})}{d_1} + \\ + N_{\mathrm{xWd}} \, N_{\mathrm{yWd}} \, WL_{\mathrm{B}}. \tag{4.8}$$

As we can see, the equation (4.8) describing the width to length channel ratio of the MOSFET with waffle gates and diagonal source and drain interconnections is a sum of width to length ratios of homogenous elements A, central elements B, and cross edge element E (see Fig. 4.14).

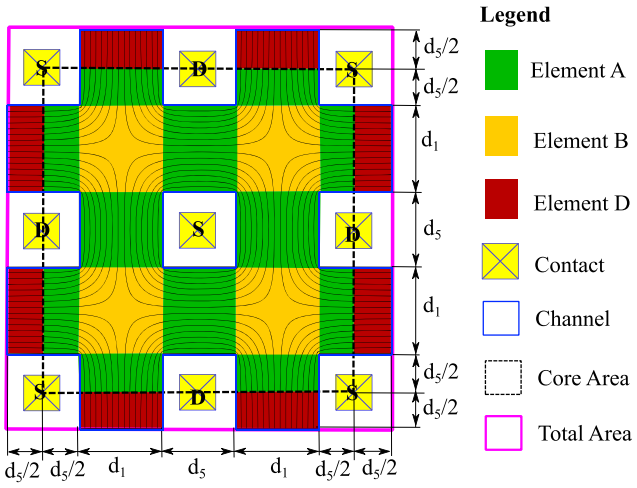


Fig. 4.12. Dimensions and portioning of channel area in the segment of Waffle MOSFET with orthogonal source (S) and drain (D) terminals to element A and cross element B and peripheral elements D, the whole and core structure dimension is N_{xWd}=2, N_{yWd}=2 [9].

4.3. Waffle MOSFET Structure with Orthogonal Source and Drain

Additional waffle structure is the MOSFET with waffle gates in orthogonal interconnections of the source and drain terminals (Fig. 4.13). Because source and drain contacts in the layout are not rotated, the layout of the structure (Fig. 4.14) is compatible in general with all processes where diagonal polysilicon gate does not violate the process design rules. No additional process steps are required. The bulk connection makes segmentation of the compact whole power MOSFET

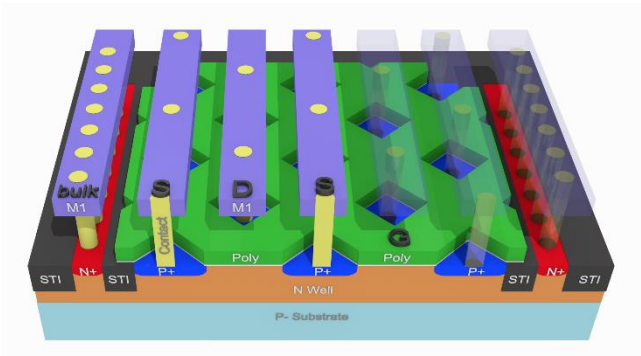


Fig. 4.13. Waffle P-channel MOSFET with waffle gate (G) and orthogonal source (S) and drain (D) interconnections with bulk connection on each sides.

into segments repeated over structure. To prevent process modification or design rule violations the contacts are not rotated about 45°. Due to this reason the spacing

between two polysilicon gates d_{d5} is larger than d_5 for waffle MOSFETs with diagonal source and drain interconnection as can be seen in Tab. 4.1. The core area of the MOSFET with waffle gates and orthogonal source and drain interconnections A_{WoC} without considering peripheral area outside the core area is

$$A_{WoC} = \frac{(d_1 + d_{d5})^2}{2} N_{xWo} N_{yWo} \tag{4.9}$$

where N_{XWo} is a number of gate in X-axis direction and N_{yWo} is a number of gate in Y-axis direction.

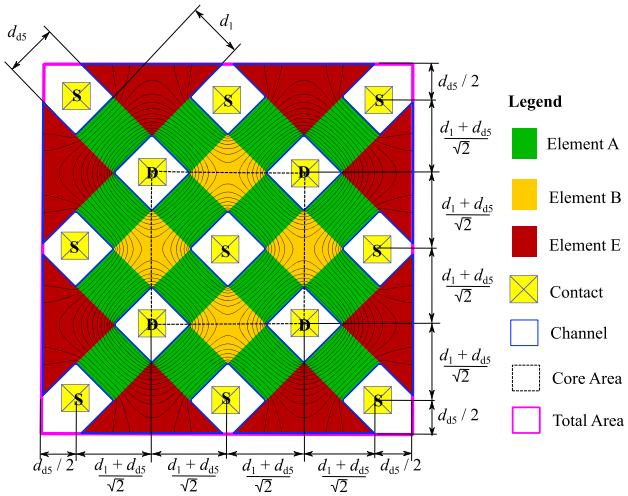


Fig. 4.14. Dimensions and portioning of channel area in the segment of Waffle MOSFET with orthogonal source (S) and drain (D) terminals to element A and cross element B and peripheral element E, core dimension is N_{xWo}=2, N_{yWo}=2 and whole structure dimension is N_{xWo}=4, N_{yWo}=4 [9].

The total area of the MOSFETs with waffle gates and orthogonal source and drain interconnections A_{Wo} is

$$A_{Wo} = {d_{d5}}^2 + d_{d5}\,(d_1 + d_{d5}) \left(\frac{N_{xWo}}{\sqrt{2}} + \frac{N_{yWo}}{\sqrt{2}}\right) + \frac{(d_1 + d_{d5})^2}{2} N_{xWo}\, N_{yWo}. \tag{4.10}$$

The width to length channel ratio WL_{WoC} in core area for the MOSFET with waffle gates and orthogonal source and drain interconnections is

$$WL_{WoC} = N_{xWo}\, N_{yWo} \left(\frac{d_{d5}}{d_1} + \frac{WL_B}{2}\right). \tag{4.11}$$

The width to length channel ratio WL_{Wo} for the MOSFET with waffle gates and diagonal source and drain interconnections on total area is

$$WL_{\mathrm{Wo}} = N_{\mathrm{xWo}}\, N_{\mathrm{yWo}} \left(\frac{d_{\mathrm{d5}}}{d_1} + \frac{WL_{\mathrm{B}}}{2}\right) + (N_{\mathrm{xWo}} + \\ + N_{\mathrm{yWo}}) \left(WL_{\mathrm{E}} - \frac{WL_{\mathrm{B}}}{2}\right). \tag{4.12}$$

As can be seen in equation (4.12), the width to length channel ratio for MOSFET with waffle gate and diagonal source and drain interconnections is a sum of width to length ratios of homogenous elements A, central elements B and cross edge elements E.

4.4. Width to Length Ratio Calculation for Waffle MOSFET Elements

For calculation of width to length channel ratio of the element B and element E, 2D Finite Element Method (FEM) solver from TCAD SILVACO was used [72]. Test structure of element B is shown in Fig. 4.15.

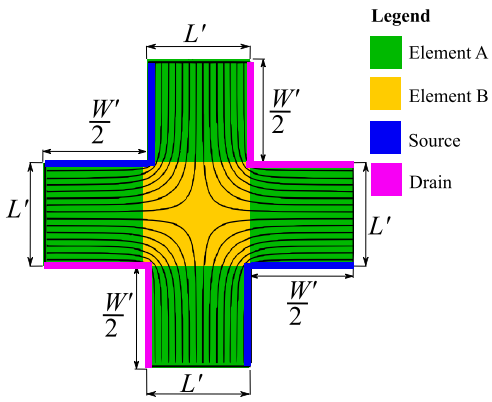


Fig. 4.15. The 2D cross structure used in TCAD simulation for determination of width to length channel ratio of cross element B for different dimensions *W'* and *L'* [9].

The effective width to length channel ratio of the cross test structure $(W/L)_{\mathrm{cross}}$ is calculated based on the simulated 2D resistance $R_{2\mathrm{D}}$ and its resistivity ρ as follows

$$\left(\frac{W}{L}\right)_{cross} = \frac{\rho}{R_{2D}} = \rho \frac{I_D}{V_{DS}}. \tag{4.13}$$

To consider only the width to length channel ratio of element B it is required to subtract the width to length channel ratio of four elements A. By considering homogenous current distribution in area of elements A and its subtraction from cross

element, all nonhomogeneous current distributions will be pressed only into area of element B.

For homogenous current distribution in elements A, the effective width to length ratio is equal to its geometry aspect ratio

$$\left(\frac{W}{L}\right)_{\mathrm{B}} = \left(\frac{W}{L}\right)_{\mathrm{cross}} - 4\left(\frac{W}{L}\right)_{A} = \left(\frac{W}{L}\right)_{\mathrm{cross}} - 4\frac{W'}{2L'} \qquad (4.14)$$

The result of the calculation as a function of its dimension is in Fig. 4.16.

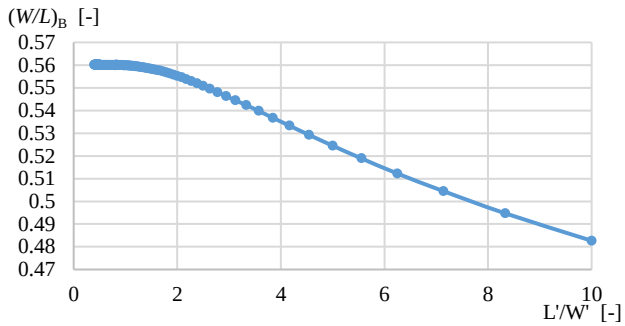


Fig. 4.16. The width to length channel ratio of cross element B $(W/L)_{\mathrm{B}}$ for different dimensions *W'* and *L'* [9].

For dimensions with ratio *L'*/*W'*<10 we can approximate data from TCAD simulation by following fitting function

$$WL_{\mathrm{B}}\left(\frac{L'}{W'}\right) = \frac{5.44 - 1.146\frac{L'}{W'} + 0.56\left(\frac{L'}{W'}\right)^2 - 7\ 10^{-4}\left(\frac{L'}{W'}\right)^3}{9.719\ -\ 2.071\ \frac{L'}{W'} + \left(\frac{L'}{W'}\right)^2}. \qquad (4.15)$$

Another element E (Fig. 4.17) describing channel on the periphery can be calculated in a similar way. From known 2D resistance $R_{2\mathrm{D}}$ (TCAD simulation) and its resistivity ρ it is possible to calculate effective width to length channel ratio of cross test structure $(W/L)_{\mathrm{cross2}}$ as

$$\left(\frac{W}{L}\right)_{cros2} = \frac{\rho}{R_{2D}} = \rho\frac{I_D}{V_{DS}}. \qquad (4.16)$$

To consider only width to length channel ratio of element E, it is required to subtract the width to length channel ratio of two elements A. By considering homogenous current distribution in area of elements A and its subtraction from edge cross element, all nonhomogeneous current distribution will be pressed only into area of element E.

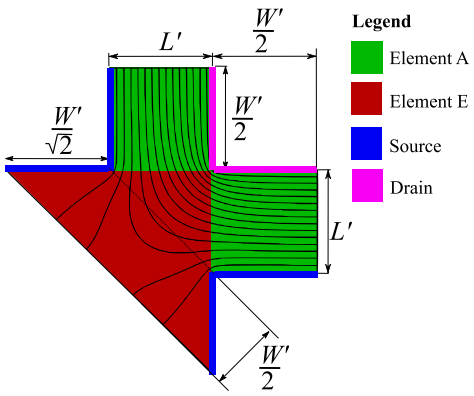


Fig. 4.17. The 2D structure used in TCAD simulation for determination of width to length channel ratio of peripheral element E for different dimensions *W'* and *L'* [9].

For homogenous current distribution in elements A the effective width to length ratio is equal to its geometry aspect ratio

$$\left(\frac{W}{L}\right)_E = \left(\frac{W}{L}\right)_{\text{cros2}} - 2\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_{\text{cros2}} - 2\frac{W'}{2\,L'} \qquad (4.17)$$

Calculation results of effective width to length channel ratio of element E is shown in the following graph (Fig. 4.18)

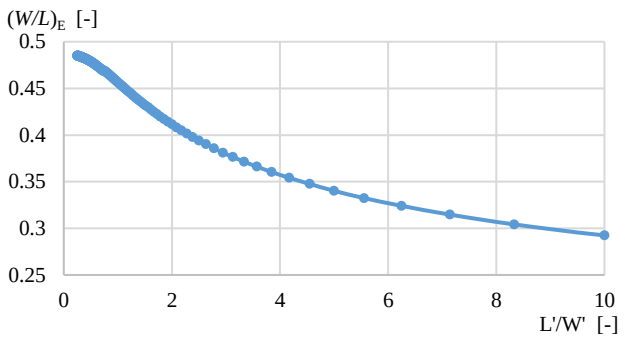


Fig. 4.18. The width to length channel ratio of cross element E $(W/L)_E$ for different dimensions *W'* and *L'* [9].

For *L'*/*W'* value smaller than 10 we can approximate data from TCAD simulation by following fitting function

$$WL_{\text{E}}\left(\frac{L'}{W'}\right) = \frac{0.72 + 1.44\frac{L'}{W'} + 0.23\left(\frac{L'}{W'}\right)^2 - 8.2\;10^{-4}\left(\frac{L'}{W'}\right)^3}{1.514 \;+\; 2.724\;\frac{L'}{W'} + \left(\frac{L'}{W'}\right)^2}. \qquad (4.18)$$

4.5. Core Structures Comparison

For core structures comparison, the figure of merit *AI* is used. In this section, no edge elements C, D and E will be taken into account.

In addition, the analytic model has been verified by 3D TCAD simulation from SILVACO [72] for different dimensions. The first simulated structure is the MOSFET with finger gates (Fig. 4.19) and the second is the NMOSFET with waffle gates (Fig. 4.20). The simulated NMOSFET transistors have been in linear region where V_{GATE} is equal to 2.0 V, V_{DS} is equal to 0.2 V and gate threshold voltage V_{TH} is equal to 1.18 V.

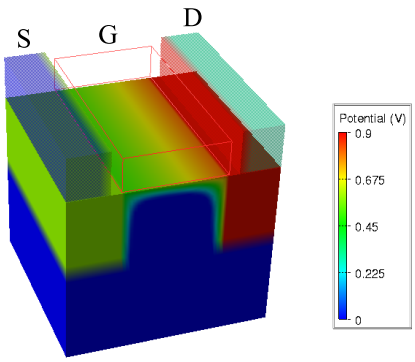


Fig. 4.19. Potential gradient from TCAD simulation in Standard NMOSFET with finger gate (G), source (S), drain (D) terminal and with dimensions N_X=1, N_Y=1 without considering edge elements [9].

The resistance $R_{DS\text{-}ON}$ has been calculated from simulated drain current I_D. The Area Increment *AI* is calculated from $R_{DS\text{-}ON}$ resistance of waffle and finger structures and from their areas by applying equation (3.9) (Fig. 4.21).

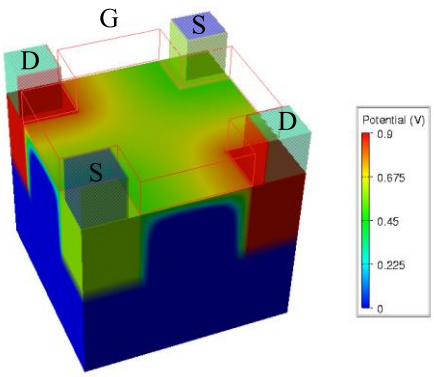


Fig. 4.20. Potential gradient from TCAD simulation in Waffle gate (G) NMOSFET with orthogonal and diagonal source (S) and drain (D) terminals with dimensions N_X=1, N_Y=1 without considering edge elements [9].

To simplify the analytic model of Area Increment we can define aspect ratio of gate dimension d_1 and dimension of source or drain area d_5 as follows

$$AR_{15} = \frac{d_1}{d_5}. \tag{4.19}$$

Putting expression (4.1), (4.3), (4.5), (4.7) and (4.15) into (3.9) and by applying (4.19), we have got core Area Increment AI_{WDC} of waffle MOSFETs with diagonal source and drain terminals on core area as

$$AI_{\mathrm{WDC}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}(AR_{15})} = \frac{1 + AR_{15}}{2 + AR_{15} WL_{\mathrm{B}}} - 1. \tag{4.20}$$

It is apparent from equation (4.20) [6], the Area Increment AI_{WDC} is independent on area dimensions of core elements N_{xF}, N_{yF}, N_{xWd}, N_{yWd}

To simplify analytic model of the waffle MOSFETs with orthogonal source and drain terminal, we can define aspect ratio of gate dimension d_1 and dimension of source or drain area with diagonal contact d_{d5} as follows

$$AR_{1\mathrm{d5}} = \frac{d_1}{d_{\mathrm{d5}}}. \tag{4.21}$$

Putting expression (4.1), (4.3), (4.9), (4.11) and (4.15) into (3.9) and by applying (4.21), we have got core Area Increment AI_{WOC} of waffle MOSFET with orthogonal source and drain terminals on core area as

$$AI_{\mathrm{WOC}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}(AR_{1\mathrm{d5}})} = \\ = \frac{AR_{15}(1 + AR_{1\mathrm{d5}})^2}{(1 + AR_{15})\, AR_{1\mathrm{d5}}(2 + AR_{1\mathrm{d5}}\, WL_{\mathrm{B}})} - 1. \tag{4.22}$$

As can be seen from equation (4.22), the Area Increment AI_{WOC} is also independent on area dimensions of core elements N_{xF}, N_{yF}, N_{xWo}, N_{yWo}.

Since equation (4.22) is a function of two aspect ratios AR_{15} and $AR_{1\mathrm{d5}}$, it will be useful to simplify it. The first step is to define relation between d_5 and d_{d5} by using scaling parameter λ from Tab. 4.1. Thus

$$d_{\mathrm{d5}} \cong \frac{\sqrt{2} + 2}{3} d_5. \tag{4.23}$$

By inserting equation (4.23) into (4.21), we have got

$$AR_{1\mathrm{d5}} = \frac{d_1}{d_{\mathrm{d5}}} \cong \frac{3}{\sqrt{2} + 2}\, AR_{15}. \tag{4.24}$$

By inserting equation (4.24) into (4.22) we have got a simplified core Area Increment AI_{WOC} which depends only on one aspect ratio AR_{15}

$$AI_{\mathrm{WOC}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}\left(\frac{3}{\sqrt{2}+2} AR_{15}\right)} \cong$$

$$= \frac{\left(\frac{\sqrt{2}+2}{3}\right)^2 + AR_{15}\left(2\frac{\sqrt{2}+2}{3} + AR_{15}\right)}{(1 + AR_{15})\left(2\frac{\sqrt{2}+2}{3} + AR_{15}\, WL_{\mathrm{B}}\right)} - 1. \tag{4.25}$$

As mentioned earlier, the figure of merit parameter Area Increment *AI* quantitatively defines amount of needed areas to have the equal resistance of waffle structures and the standard MOSFETs with finger gates. When qualitative parameter Area Increment of waffle structure has negative value, it means that waffle structure requires less area. Due to this, for real application it is very useful to know the dimensions of waffle structures where *AI* is negative.

The Area Increment AI_{WDC} equation (4.20) is negative only if

$$0 < AR_{15} < 2.239. \tag{4.26}$$

The Area Increment from equation (4.25) is $AI_{\mathrm{WOC}} < 0$ only if

$$0 < AR_{15} < 2.237. \tag{4.27}$$

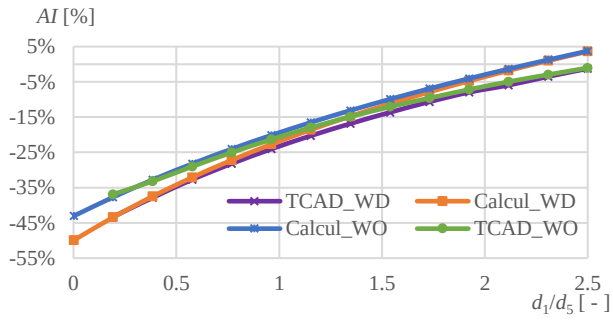


Fig. 4.21. Dependence of Area Increment (AI) on core structures dimensions d_1/d_5 for analytic model of waffle with diagonal source and drain Calcul_WD and from 3D TCAD simulation TCAD_WD, the analytic model of waffle with orthogonal source and drain Calcul_WO and from 3D TCAD simulation TCAD_WO [9].

The equations (4.26) and (4.27) can be used for analytic definition of conditions when the area of core waffle structure occupies smaller area than core finger structure with having the same resistance.

4.6. Structures Comparison Considering Edge Elements

For more precise comparison of two topologies, with considering edge elements, it is useful to have same or similar area of each test structures. Same area of segments of the MOSFETs with finger or waffle gate topology and with diagonal source and drain terminals is guaranteed when N_x=N_{xF}=N_{xWd} and N_y=N_{yF}=N_{yWd}. After putting expressions (4.2), (4.4), (4.6), (4.8) and (4.15) into equation (3.9) we have got Area Increment AI_{WD} of the waffle MOSFET with diagonal source and drain terminals on segment total area

$$AI_{\mathrm{WD}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}(AR_{1\mathrm{d}5})} = \\ = \frac{N_{\mathrm{x}}(1 + N_{\mathrm{y}} + AR_{15}\, N_{\mathrm{y}})}{N_{\mathrm{x}} + N_{\mathrm{y}} + 2\, N_{\mathrm{x}}\, N_{\mathrm{y}} + AR_{15}\, N_{\mathrm{x}}\, N_{\mathrm{y}}\, WL_{\mathrm{B}}} - 1. \tag{4.28}$$

To have similar area of the finger MOSFET as the waffle MOSFET with orthogonal source and drain terminals it is required to set correctly the number of fingers N_{xF} and N_{yF} in the standard MOSFET. Number of gate fingers in X axis is

$$N_{\mathrm{xF}} = \frac{AR_{15}\,(1 + (\frac{1}{\sqrt{2}} + \frac{AR_{1\mathrm{d}5}}{\sqrt{2}})\, N_{\mathrm{xWO}}) - AR_{1\mathrm{d}5}}{(1 + AR_{15})\; AR_{1\mathrm{d}5}} \tag{4.29}$$

and for Y axis is

$$N_{\mathrm{yF}} = \frac{AR_{15}\,(1 + (\frac{1}{\sqrt{2}} + \frac{AR_{1\mathrm{d}5}}{\sqrt{2}})\, N_{\mathrm{yWO}}) - AR_{1\mathrm{d}5}}{(1 + AR_{15})\; AR_{1\mathrm{d}5}} \tag{4.30}$$

After putting expressions (4.2), (4.4), (4.10), (4.12), (4.15), (4.18), (4.29) and (4.30) into equation (3.9) and by applying (4.21) we have got Area Increment AI_{WO} of the waffle MOSFET with orthogonal source and drain terminals on segment total area

$$\begin{aligned} AI_{\mathrm{WO}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}(AR_{1\mathrm{d}5})\,\&\,WL_{\mathrm{E}} \to WL_{\mathrm{E}}(AR_{1\mathrm{d}5})} = \\ = -1 + (\,(-\sqrt{2}\; AR_{1\mathrm{d}5} + AR_{15}\,(\sqrt{2} + (1 + \\ + AR_{1\mathrm{d}5})\, N_{\mathrm{xWo}}))\,(\sqrt{2} + (1 + \\ + AR_{1\mathrm{d}5})\, N_{\mathrm{yWo}}))/((1 + \\ + AR_{15})\; AR_{1\mathrm{d}5}\,(\, AR_{1\mathrm{d}5}\, N_{\mathrm{yWo}}\,(- WL_{\mathrm{B}} + \\ +2\, WL_{\mathrm{E}}) + N_{\mathrm{xWo}}\,(- AR_{1\mathrm{d}5}\, WL_{\mathrm{B}} + \\ +N_{\mathrm{yWo}}\,(2 + AR_{1\mathrm{d}5}\, WL_{\mathrm{B}}) + 2\; AR_{1\mathrm{d}5}\, WL_{\mathrm{E}}))). \end{aligned} \tag{4.31}$$

By inserting equation (4.24) into (4.31), the simplified Area Increment AI_{WO} as function of one aspect ratio AR_{15} only and thus it can be defined as

$$
\begin{aligned}
& AI_{\mathrm{WO}} \mid_{WL_{\mathrm{B}} \to WL_{\mathrm{B}}\left(\frac{3}{\sqrt{2}+2} AR_{15}\right) \& WL_{\mathrm{E}} \to WL_{\mathrm{E}}\left(\frac{3}{\sqrt{2}+2} AR_{15}\right)} \cong \\
& \cong -1 + ((0.195 \ + ((\sqrt{2}+2)/3 \ + \\
& + AR_{15})\, N_{\mathrm{xWo}})\, ((2\sqrt{2}+2)/3 + ((\sqrt{2}+2)/3 \ + \\
& + AR_{15})\, N_{\mathrm{yWo}}))/((1 + \\
& + AR_{15})\, (\, AR_{15}\, N_{\mathrm{yWo}}\, (2\, WL_{\mathrm{E}} - WL_{\mathrm{B}}) + \\
& + N_{\mathrm{xWo}}\, (N_{\mathrm{yWo}}\, ((2\sqrt{2}+2)/3 \ + \\
& + AR_{15}\, WL_{\mathrm{B}}) + 2\, AR_{15}\, WL_{\mathrm{E}} - \ AR_{15}\, WL_{\mathrm{B}}))).
\end{aligned}
\tag{4.32}
$$

4.7. Definition of Waffle Use Cases Considering Edge Elements

In general qualitative parameter Area Increment AI has negative value for all use cases. Because only then area of waffle structure occupies smaller area than finger structure with same resistance. The Area increment from (4.28) AI_{WD} is negative only if

$$0 < \ AR_{15} \leq 2.24 \ \& \ N_{\mathrm{x}} \geq 1 \ \& \ N_{\mathrm{y}} \geq 1 \tag{4.33}$$

and for additional interval

$$2.24 < \ AR_{15} < 4.27 \ \& \ 1 \leq N_{\mathrm{x}} < N_{x1} \ \& \ N_{\mathrm{y}} \geq 1. \tag{4.34}$$

Where N_{x1} can be approximated by function

$$
\begin{aligned}
& N_{x1} \ = (242975 \ - \ 51775 \ AR_{15} + \\
& +2.5\ 10^{4} \ AR_{15}{}^{2})/(-242975 \ + \\
& + 1.589\ 10^{5} \ AR_{15} - \ 48125 \ AR_{15}{}^{2} \ + \\
& + 11085 \ AR_{15}{}^{3} \ + \ 169 \ AR_{15}{}^{4}).
\end{aligned}
\tag{4.35}
$$

The $AR_{1\mathrm{d5}}$ can be transformed into AR_{15} by using following equations derivated from (4.24)

$$AR_{15} = \frac{d_1}{d_5} \cong \frac{\sqrt{2}+2}{3}\ AR_{1\mathrm{d5}}. \tag{4.36}$$

Then for negative Area Increment AI_{WO} equation (4.32) can be calculated following conditions

$$0 < \ AR_{15} \leq 2.24 \ \& \ N_{\mathrm{x}} \geq 1 \ \& \ N_{\mathrm{y}} > N_{y2} \tag{4.37}$$

and for additional interval

$$2.24 < AR_{15} < 3.35 \;\&\; 1 \leq N_x < N_{x2} \;\&\; N_y > N_{y2} \tag{4.38}$$

where N_{X2} can be approximated by following function

$$\begin{aligned} N_{x2} = (&-0.201 - 0.057\ AR_{15} + 1.318\ {AR_{15}}^2 + \\ &+0.044\ {AR_{15}}^3)/(-3.637 + 0.595\ AR_{15} - \\ &-1.776\ {AR_{15}}^2 + {AR_{15}}^3) \end{aligned} \tag{4.39}$$

and coefficient N_{Y2} can be approximated by function

$$\begin{aligned} N_{y2} = 524.4/(&249.8 + 48.53\ AR_{15} - \\ &-57.5\, {AR_{15}}^2 + 1.949\ {AR_{15}}^3 - 1.394\, N_x - \\ &- 6.168\ AR_{15}\, N_x + 0.2578\ {AR_{15}}^2\, N_x + \\ &+ 0.4615\, {N_x}^2 + 0.1638\ AR_{15}\, {N_x}^2 - 0.017\, {N_x}^3). \end{aligned} \tag{4.40}$$

The equations (4.33), (4.34), (4.37) and (4.38) can be used for analytic definition of condition when area of waffle structures occupies smaller area than finger structure with the same resistance.

4.8. Comparison of Models with FEM Results

To analyze proposed models, more complex test structures in certain process have to be simulated in 2D FEM solver Agros2D [73] and the results are presented in modified to be more robust (Tab. 4.2).

Tab. 4.2. General designed rules for MOS layout based on standard TSMC 0.35μm process and for modified process.

Name	**TSMC 0.35μm**	**Modified**
d_1 [μm]	1.7	1.7
d_2 [μm]	2.1	2.1
d_3 [μm]	1.7	2.1
d_5 [μm]	5.5	6.3
d_{d5} [μm]	6.37	7.17

Example of potential gradient for three different gate patterns simulated in Agros2D can be seen in Fig. 4.22. Considering these three examples, it can be seen that they occupy similar areas (Tab. 4.3; Tab. 4.4). The standard MOSFET with finger gates

length d_1 = 1.7 μm, d_5 = 6.3 μm and dimension N_x = 5, N_y = 5 has area A_F = 2144 μm^2 and width to length channel ratio calculated by analytic model is WL_F = 136.17.

The waffle MOSFETs with diagonal source and drain terminals and dimension N_x = 5, N_y = 5 has identical area A_{Wd} = 2144 μm^2 as fingers MOSFET and have width to length channel ratio calculated by analytic model WL_{Wd} = 236.35 which is about 0.66 % higher value than calculated by FEM WL_{Wd} = 234.8. From these analytic values by using equation (3.9), the Area Increment AI = -42.38 % can be calculated.

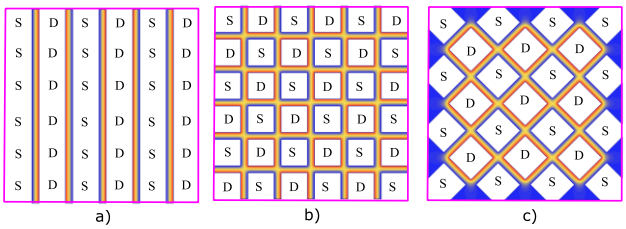


Fig. 4.22. The 2D simulation of channel area by Agros2D tool, illustrations of potential gradient for a) Standard MOSFET with finger gate dimension Nx = 5, Ny = 5, b) Waffle MOSFET with diagonal source (S) and drain (D) terminals dimension Nx = 5, Ny = 5, c) Waffle MOSFET with orthogonal source (S) and drain (D) terminals dimension Nx = 6, Ny = 6 [9].

Based on this figure or merit parameter, it can be concluded that the waffle MOSFET with diagonal source and drain terminals with same resistance as the standard MOSFET with finger gates will occupy about 42.38% less area than finger structure, or equivalently for same area it have about 42.38 % less resistance. And on top of that the analytic definition of requirements for AI_{Wd}<0 based on equation (4.33), (4.34) ($0<d_1/d_5\leq 2.24$& $N_X \geq 1$ & $N_Y \geq 1$) is consistent with observation where d_1/d_5 = 0.27. For additional structure with these parameters d_1 = 18 μm, d_5 = 6.3 μm, d_1/d_{d5} = 2.857, N_x = 4, N_y = 2, the Area Increment AI_{Wd} = +1 % has positive value because it exceeds predicted requirements ($2.24< d_1/d_5 <4.27$& $1\leq N_X <3.41$ & $N_Y \geq 1$).

Tab. 4.3. Comparison of Core Area Increment AIC and Area Increment AI different for different layout structures where Nx is dimesion in X axis, Ny is dimension inY axis, Ac is area of core structure, A is area of the whole structure, (W/L)c is effective width to length channel ratio of core element, (W/L) is effective width to length channel ratio of whole element, $(W/L)_{FEM}$ is effective width to length channel ratio of the whole element calculated with FEM by using Agros2D tool, $(W/L)_{ERR}$ is relative error between (W/L) and $(W/L)_{FEM}$. The F is Standard MOSFET with finger gate, the Wd is MOSFET with waffle gate having diagonal interconnections of source and drain terminals and.

MOS	N_X [-]	N_Y [-]	d_1 [μm]	d_5 [μm]	d_1/d_5 [-]	A_c [μm^2]	A [μm^2]	$(W/L)_c$ [-]	(W/L) [-]	$(W/L)_{FEM}$ [-]	$(W/L)_{ERR}$ [%]	AI_C [%]	AI [%]	**Analytic Definition of Requirements for $AI < 0$**
F	2	2	1.7	6.3	0.270	256	497	18.82	26.23					$0 < d_1/d_5 \leq 2.24$ &
Wd	2	2	1.7	6.3	0.270	256	497	31.88	46.71	46.45	0.56	-39.76	-42.99	$N_X \geq 1$ & $N_Y \geq 1$
F	4	4	1.7	6.3	0.270	1024	1467	75.29	90.11					$0 < d_1/d_5 \leq 2.24$&
Wd	4	4	1.7	6.3	0.270	1024	1467	127.54	157.19	156.1	0.70	-40.97	-42.67	$N_X \geq 1$ & $N_Y \geq 1$
F	5	5	1.7	6.3	0.270	1600	2144	117.65	136.17					$0< d_1/d_5 \leq 2.24$&
Wd	5	5	1.7	6.3	0.270	1600	2144	199.29	236.35	234.8	0.66	-40.97	-42.38	$N_X \geq 1$ & $N_Y \geq 1$
F	2	2	18	6.3	2.857	2362	3014	5.4	6.1					$2.24< d_1/d_5 <4.27$ &
Wd	2	2	18	6.3	2.857	2362	3014	4.98	6.38	6.274	1.84	8.23	-4.53	$1 \leq N_X < 3.41$ & $N_Y \geq 1$
F	4	2	18	6.3	2.857	4724	5682	10.8	12.2					$2.24< d_1/d_5 <4.27$&
Wd	4	2	18	6.3	2.857	4724	5682	9.98	12.07	11.85	1.93	8.23	1.00	$1\leq N_X <3.41$ & $N_Y \geq 1$

Tab. 4.4. Comparison of Core Area Increment AIC and Area Increment AI different for different layout structures where Nx is dimesion in X axis, Ny is dimension inY axis, Ac is area of core structure, A is area of the whole structure, (W/L)c is effective width to length channel ratio of core element, (W/L) is effective width to length channel ratio of whole element, $(W/L)_{FEM}$ is effective width to length channel ratio of the whole element calculated with FEM by using Agros2D tool, $(W/L)_{ERR}$ is relative error between (W/L) and $(W/L)_{FEM}$, (* value for dimension dd5, # value for ratio d1/ dd5). The F is Standard MOSFET with finger gate and Wo is MOSFET with waffle gate having orthogonal interconnections of source and drain terminals.

MOS	N_X [-]	N_Y [-]	d_1 [μm]	d_5 [μm]	d_1/d_5 [-]	A_c [μm²]	A [μm²]	$(W/L)_c$ [-]	(W/L) [-]	$(W/L)_{FEM}$ [-]	$(W/L)_{ERR}$ [%]	AI_C [%]	AI [%]	**Analytic Definition of Requirements for $AI < 0$**
F	2	3	1.7	6.3	0.270	384	676	28.24	35.65					$0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 2.06$
Wo	2	4	1.7	6.3; 7.169*	0.270; 0.237#	315	636	35.97	37.20	36.87	0.92	-35.69	-9.84	
F	3	3	1.7	6.3	0.270	576	918	42.35	53.47					$0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 2.06$
Wo	4	4	1.7	6.3; 7.169*	0.270; 0.237#	629	1040	71.95	73.59	72.98	0.85	-35.69	-17.66	
F	5	5	1.7	6.3	0.270	1600	2144	117.65	136.18					$0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 2.24$
Wo	6	6	1.7	6.3; 7.169*	0.270; 0.237#	1416	2007	161.90	164.36	163.0	0.84	-35.69	-22.43	
F	3	2	10	6.3	1.587	1594	2147	9.78	11.67					$0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 3.32$
Wo	4	2	10	6.3; 7.169*	1.587; 1.395#	1179	1753	7.97	8.91	8.787	1.50	-9.24	6.82	
F	2	5	10	6.3	1.587	2657	3415	16.3	17.56					$0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 3.06$
Wo	2	6	10	6.3; 7.169*	1.587; 1.395#	1769	2517	11.96	13.22	13.02	1.54	-9.24	-2.13	

Similar comparison can be performed for the waffle MOSFET with orthogonal terminals. This test structure with gate d_1 = 1.7 μm, d_5 = 6.3 μm and dimensions N_x = 6, N_y = 6 has area A_{Wo} = 2007 μm^2 which is about 6.3 % smaller area than for finger MOSFET with calculated dimension N_x = 5, N_y = 5 from equations (4.29) and (4.30). The width to length channel ratio calculated by analytic model WL_{Wo} = 164.36, which is about 0.84% higher value than calculated by FEM WL_{Wo} = 163.00.

The Area Increment for analytic values is AI = -22.43 %. In addition, the analytic definition of requirements for $AI_{Wo}<0$ based on equation (4.37), (4.38) ($0 < d_1/d_5 \leq 2.24$ & $N_X \geq 1$ & $N_Y > 2.24$) is consistent with observation where d_1/d_5 = 0.27 is recalculated based on (4.36) from d_1/d_{d5} = 0.237.

From the results it is also apparent that Area Increment calculated for core area AI_C presented by [66] is independent on segment dimensions and depends on aspect ratio of d_1/d_5 or d_1/d_{d5} only. Because it does not consider peripheral elements it cannot be used for precise description of power MOSFETs with segmentation.

4.9. Discussion

In this work, the gates length d_1 is considered in wider range. Due to this the aspect ratio AR_{15} defined by (4.19) can be larger than minimum ratio 1/3 used in [68] and [67] defined based on the λ scale process factor. Reason for larger gate length variability is to cover dimensions of low voltage MOSFETs with higher voltage range used by processes with dual oxide. In this processes the gate with thicker oxide have also larger length to sustain there the higher voltage but minimum contact to polysilicon spacing d_3 is robust so it can remain the same. Hence, the dimension d_5 can remain unchanged also. Additional used cases for longer gate is in analog design where different W/L ratios are required.

In general, width to length channel ratios of non-homogenous elements B and E with non-homogenous current distribution are fixed values and do not have to variate with different element geometry. In opposite, width to length channel ratios of homogenous elements A, C and D with $d_5 >> d_1$ have mostly homogenous current distribution and have to variate with ratio of element geometry. For $d_5 \leq d_1$, the elements C and D mostly have non-homogenous current distribution mostly. In publications [66], [67], [68] and [69], only homogenous currents are considered for these partially homogenous elements. In this work, all non-homogenous current distributions are

considered to reach higher precision of width to length channel ratio calculation in range $d_5 \leq d_1$. This error correction is presented in the value of width to length channel ratio of non-homogenous elements B and E. This is the reason why width to length channel ratios of non-homogenous elements B and E are not fixed values and have to variate with different element geometry (4.15) and (4.17). Due to this reason, the precision less than 2 % can be reached even for larger d_1 (see Tab. 4.4 test structure: d_1 = 18 μm, d_5 = 6.3 μm, d_1/d_{d5} = 2.857, N_x = 4, N_y = 2 the WL_{ERR} = 1.93 %).

More precise *AI* equations (4.28) and (4.31) are function of multiple variables such as channel geometry AR_{15}, AR_{1d5}, WL_B, WL_E and segment dimensions N_x, N_y. Therefore, the conditions for negative *AI* are not simple to recognize. To overcome these drawbacks, conditions (4.33), (4.34), (4.37) and (4.38) has been calculated where the MOSFETs structures with waffle gates occupy less area than the standard MOSFETs with finger gates with same channel resistance.

4.10. Waffle Implementation in Power IC

Advantage of waffle MOS structures is that even without additional process steps or process modification of mature process it allows to improve power MOSFET specific resistance. To reach same $R_{DS\text{-}ON}$ the smaller power MOS area structure is required with the waffle MOS topology.

To use the waffle MOS concept in application, the test chip has been created and has been fabricated. In power management product from STMicroelectronics, made in 160nm BCD8sp process the main LV (5V) power MOSFET Fig. 4.23 a) has been replaced with equivalent waffle power 5V MOSFET with orthogonal source and drain interconnections Fig. 4.23 b). Because waffle MOS have same orthogonal source and drain interconnection as original finger MOS the replacement was simplified.

Proposed new IC with smaller power part pass all standard product validation tests. Measured resistance of original power MOSFETs was 397.53 mΩ and measured resistance of waffle MOSFETs was 397.92 mΩ. Even we can consider same resistance for both power MOSFET structures, the area of waffle MOSFET is about 19% smaller compare to finger MOSFET structure. Due to smaller power MOS area but same control part area the total chip area is reduce about 6%.

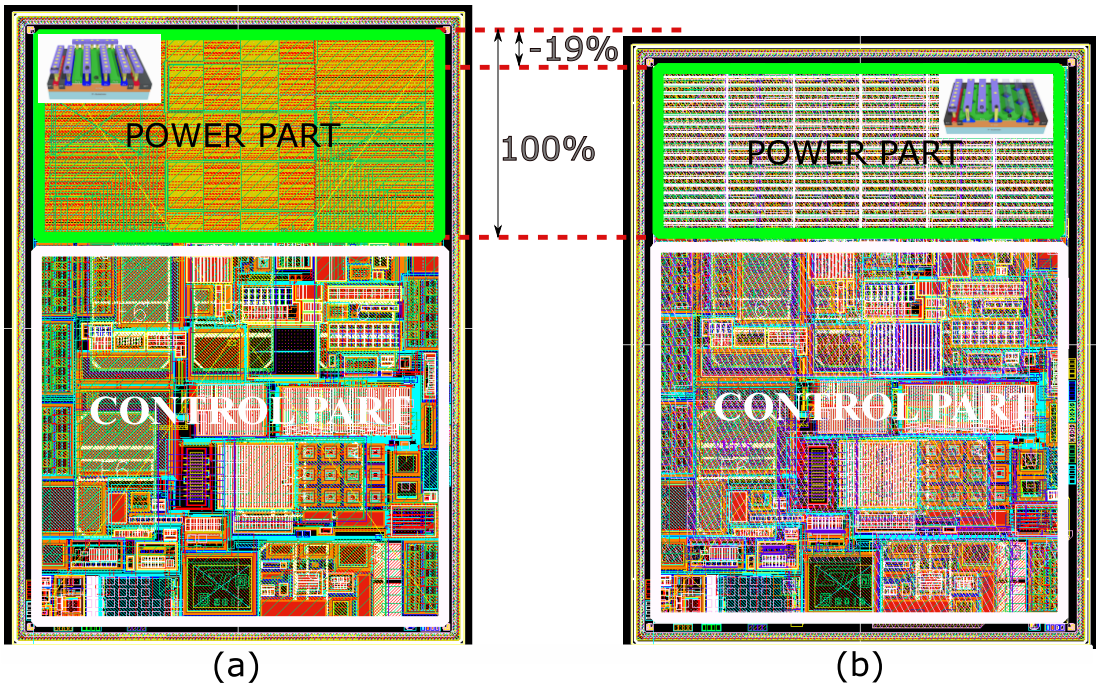


Fig. 4.23. Improvement of power management ICs in 160nm BCD8sp process (a) Original IC with standard finger power 5V MOSFET, (b) Reduced power MOSFET area about 19% by using waffle power 5V MOSFET with orthogonal source and drain interconnections

4.11. Waffle MOSFET Conclusion

To achieve a high reliability of power MOSFETs transistors the bulk connection have to be robustly connected. This lead to power MOSFETs segmentation and it influenced the specific on-resistance parameter. In this work two MOSFET topologies with waffle gate with a diagonal and orthogonal source and drain interconnections has been described for the first time. Moreover, its new analytic models have been describe. It also allows to descibre non-square shapes of power MOSFETs compare to Vemuru [68].

The MOSFET structure with waffle gates with orthogonal source and drain interconnections has been described, and its analytic model of channel area has been the first time proposed. In addition, orthogonal source and drain interconnections are much more simple in comparison to orthogonal topology proposed by Madhyastha [69] Fig. 3.5, where an orthogonal source and drain interconnection have metallization more complex and has a weak electro-migration limit.

In additional, the analytic models of effective width to length channel ratio have been compared by numerical 2D FEM simulation. Here, the good match has been

observed between analytical and numerical models with differences less than 2 % for both waffle structures.

Moreover, this thesis confirms that models considering core area elements only [66] are not sufficient precise for the exact description of power MOSFETs with segmentation, and therefore in this work the new more precise models are presented.

There has been compared the example of MOSFET topology with waffle gate pattern with diagonal source and drain interconnections and the standard MOSFET with finger gates with the condition of the same on-resistance. The result of it is that the waffle gate pattern with diagonal source and drain interconnections occupies 42.38 % less area than the standard one.

Similarly, the second example of MOSFET topology with waffle gate with an orthogonal source and drain interconnections occupies 22.43 % less area compared to the standard MOSFET with finger gates with the condition of the same on-resistance.

Moreover, there has been defined conditions where the segmented power MOSFETs structures with waffle gates occupy less area than the standard MOSFETs with finger gates with same channel resistance.

In power IC, it has been presented 19 % area saving of power 5V MOSFET in 160nm BCD8sp process by using waffle power MOSFET with orthogonal source and drain interconnections.

4.12. Possible Future Development of Waffle MOSFET Topologies

It has been described advantage of waffle MOSFET for RF application [67] due to better gate resistance. By using MOSFET with orthogonal source and drain (Fig. 4.14), where source and drain contacts are rotated 45° to gate pattern the lower capacitance in-between is expected. The RF model of waffle MOSFET with orthogonal source and drain interconnection is promising for future development.

5. New Power GaN HEMT

The dimension scaling of HV power GaN HEMT in discrete devices or smart power GaN IC is very beneficial due to the possibility to improve the channel resistance or efficiency of power discrete or IC devices or due to the reduction of production cost by decreasing chip area and by it yield improvement. To fulfill those expectation several lateral HV waffle GaN HEMT structures are described and modeled in the following chapter.

Parts of this chapter has been published by the author of this thesis in the patents [10], and [11]. Author of this thesis contributes to this chapter by 90%.

5.1. Waffle GaN HEMT

The Waffle patterns with planar gate are well known from Silicon-based power MOSFETs. The main advantage of this gate pattern is that allows to reach lower specific On-Resistance without additional process steps or change.

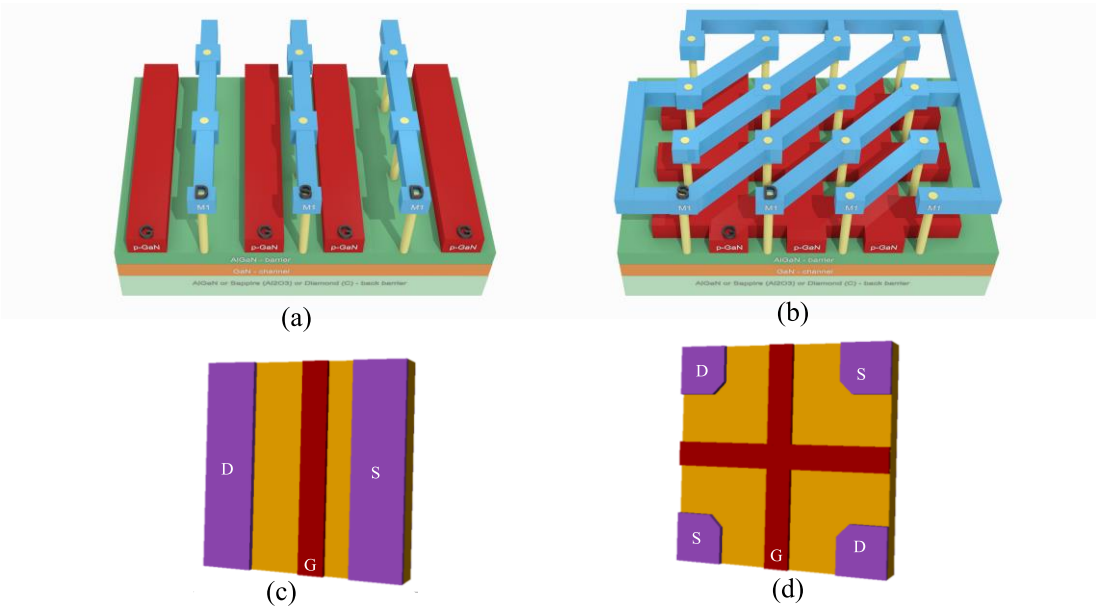


Fig. 5.1. HV GaN HEMT transistor with different gate patterns: (a) with standard finger gate, (b) proposal of new transistor with Waffle gate pattern with GaN normally-off transistor (using p-GaN gate technology), (c) element of finger gate transistor, (d) element of new transistor with Waffle, where S is source contact, D is drain contact and G is gate.

Because there is no need for extra cost due to the additional process steps, we can implement Waffle MOS structure in almost all MOSFET processes and also in GaN HEMT.

One of the main advantages of wide energy bandgap semiconductors is that sustain significantly higher nominal voltage compare to silicon. The critical electric field of GaN is 12-times higher than for silicon and about 30% higher than for SiC. Due to better HV capability, the GaN-based HV power devices do not need to have such a complex drain architecture, and it is possible to have the same dimensions and topology for drain and source electrode Fig. 5.1 a). The symmetrical architecture of source and HV drain electrodes is compatible with a planar waffle gate pattern Fig. 5.1 b). Due to the symmetry of waffle pattern also source contact S have to have the same distance to the gate electrode as drain contact D Fig. 5.3 b). For HV transistors, usually only drain electrode should sustain HV and other electrodes like gate G and source S are LV. Because gate and source electrodes are LV, but the proximity between them is overdesign to sustain HV, there is room for area optimization that could be addressed.

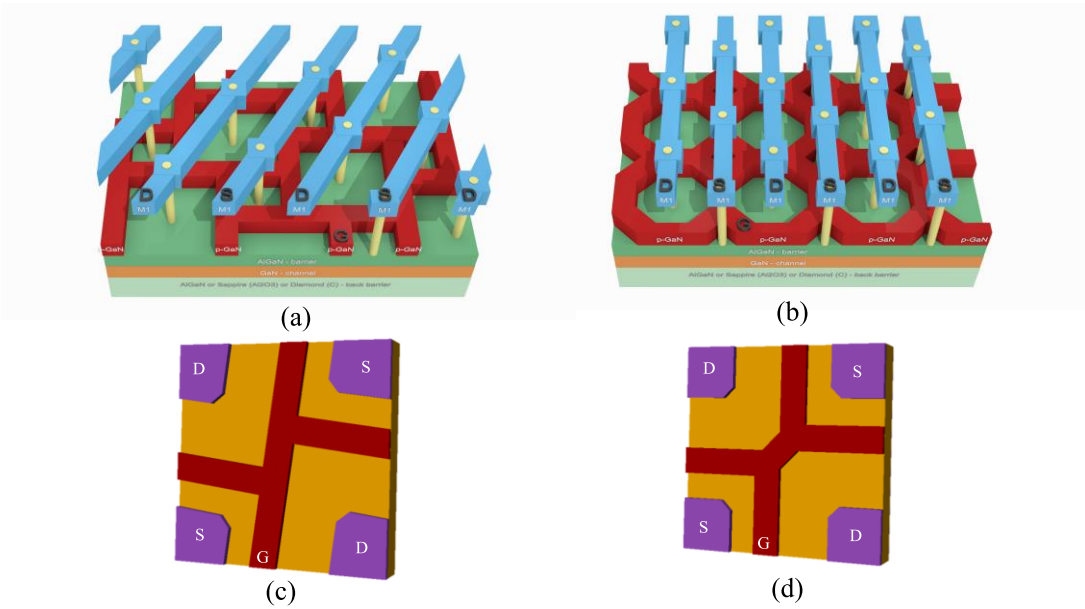


Fig. 5.2. Proposal gate patterns for HV GaN HEMT new transistor patents: (a) with dissimilar square waffle pattern [11], (b) with octagon waffle pattern [10], (c) element with new dissimilar square waffle gate pattern, (d) element with new octagon waffle pattern, where S is source contact, D is drain contact and G is gate

To find suitable solutions the classification of periodic tilings composed from regular and semiregular polygons [121] was used. A “tiling” or “tessellation” of a flat

surface is a decomposition into a pattern tiles to cover the whole surface with no overlaps and no gaps.

Two solutions have been found to fulfill the optimization task. The dissimilar square waffle gate pattern [11] shown in Fig. 5.2 a) c), and octagon waffle gate pattern [10] shown in Fig. 5.2 b),d).

Both proposed topologies, the dissimilar square waffle gate pattern [11] and octagon waffle gate pattern [10] can change independently spacing between the gate and drain contacts and spacing between gate and source contacts. Also, both described elements can be, as regular tiles, compose to whatever area without overlaps and gaps what is suitable for large power transistor structures. The gate channel length can also be customized.

5.2. Geometrical Properties of Proposals

The main dimensions of conventional GaN HEMT transistors and all new proposals are present in Fig. 5.3

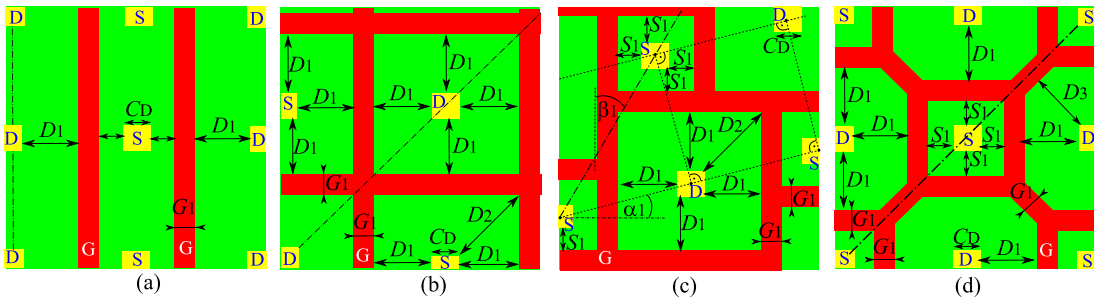


Fig. 5.3. Main dimensions of different GaN HEMT patterns: (a) finger gate transistor, (b) new transistor with waffle gate, (c) new transistor with dissimilar square waffle gate pattern, (d) new transistor with octagon waffle pattern, where S is source contact, D is drain contact and G is gate terminal.

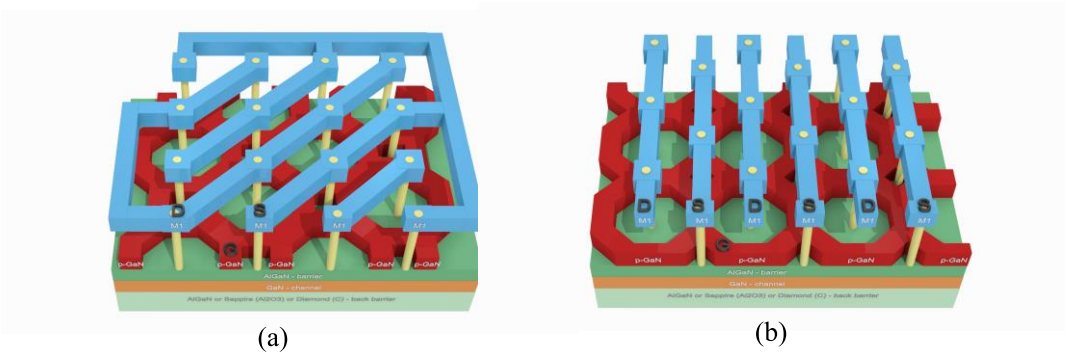
For finger structure Fig. 5.3 a) the gate G have orthogonal orientation and metallization to interconnection all source contact S and all drain contacts D is also orthogonal. The waffle structure Fig. 5.3 b) have orthogonal gate G orientation and metallization to interconnection all source contact S and all drain contacts D is also orthogonal. However, similar as for silicon waffle if the gate is rotated diagonally then source S and drain D interconnection can be orthogonal. The dissimilar square waffle

gate pattern Fig. 5.3 c) can have orthogonal gate G orientation and source S and drain D interconnections are oriented under the slope β_1 equal to

$$\beta_1 = arctan\left(\frac{S_1 + G_1}{D_1 + G_1}\right) \tag{5.1}$$

Where S_1 is spacing between source contact and gate, D_1 is spacing between drain contact and gate, and G_1 is the dimension of the gate electrode. Another possibility is to rotate gate pattern of dissimilar square waffle about angle β_1 and then source S and drain D interconnections are orthogonally oriented.

The octagon waffle gate pattern Fig. 5.3d) have orthogonal and diagonal gate G orientation and source S and drain D interconnections can be oriented diagonally Fig. 5.4 a) or orthogonally Fig. 5.4 b).



(a) (b)

Fig. 5.4. Proposal of octagon waffle gate pattern [10] for HV GaN HEMT (a) with diagonal source S and drain D interconnections (b) with orthogonal source S and drain D interconnections, where G is a gate

The dissimilar square waffle gate pattern Fig. 5.3 c) have it element Fig. 5.2 c) rotated about angle α_1 equal to

$$\alpha_1 = arctan\left(\frac{D_1 - S_1}{D_1 + S_1 + G_1 + C_D}\right) \tag{5.2}$$

The diagonal spacing between drain and gate, dimension D_2, from Fig. 5.3 b), c) for waffle gate and a dissimilar square waffle gate pattern is always larger than its orthogonal spacing D_1 and can be calculated as follows

$$D_2 = \sqrt{2}\ D_1 \tag{5.3}$$

For a transistor with octagon waffle pattern Fig. 5.3 d) the diagonal spacing between drain and gate, dimension D_3, is more variable and dependent also on the source to gate spacing S_1, gate dimension G_1 and can be described as

$$D_3 = \frac{\sqrt{2}\,(S_1 + D_1 + G_1) - G_1}{2} = \frac{S_1 + D_1 + G_1\left(1 - \frac{1}{\sqrt{2}}\right)}{\sqrt{2}} \qquad (5.4)$$

Because D_3 can be smaller than D_1 in HV applications, it is suitable to avoid it and to have $D_3 \geq D_1$ or in another case to use drain contacts with a chamfer to compensate smaller proximity.

5.3. Electrical Properties of Proposals

For additional calculation of resistance improvement in waffle structures, the Area Increment *AI* figure of merit is used. Let's consider Normally-On GaN HEMT where the conductive 2DEG layer is present in the channel area and source and drain area. After that condition for calculation of $R_{DS\text{-}ON}$ resistance between the source and drain contacts for fully open transistor the gate electrode can be removed, as it is described in Fig. 5.5.

(a) (b)

Fig. 5.5. Element for modeling Area Increment *AI* from $R_{DS\text{-}ON}$ resistance for Normally-On Waffle GaN HEMT: (a) element of finger gate transistor, (b) element of new transistor with Waffle, where S is source and D is drain contact

The 2D resistance between contacts depend on width to length effective ratio as follows

$$R_{2D} = \rho_{2DEG}\left(\frac{L}{W}\right)_{eff} = \rho_{2DEG} / \left(\frac{W}{L}\right)_{eff} \qquad (5.5)$$

where ρ_{2DEG} is resistivity of 2DEG layer. After insertion of (5.5) into (3.4) and into (3.5) we can get same equation (3.9) for Area Increment *AI* GaN HEMT as it is for Silicon.

5.3.1. Rectangular contacts of finger

For Area Increment *AI* calculation of proposed waffle structures, the reference finger structure has to be defined. The area of finger element is chosen to be equal to waffle to simplify *AI* calculation Fig. 5.6 where C_D is contact dimension and C_S is contacts space.

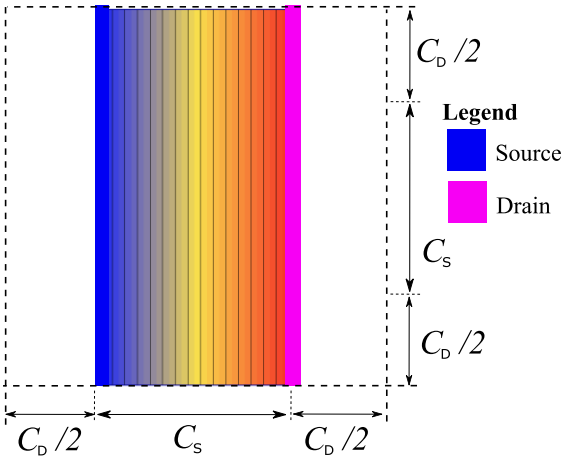


Fig. 5.6. Dimensions and terminals of the element with rectangle shape contacts and simulated potential gradient solved with Agros2D; where C_D is contact dimension and C_S is contacts space.

5.3.2. Square contacts of waffle

Following fatter can be used to describe resistance of fully open HEMT with waffle gate pattern and octagonal pattern.

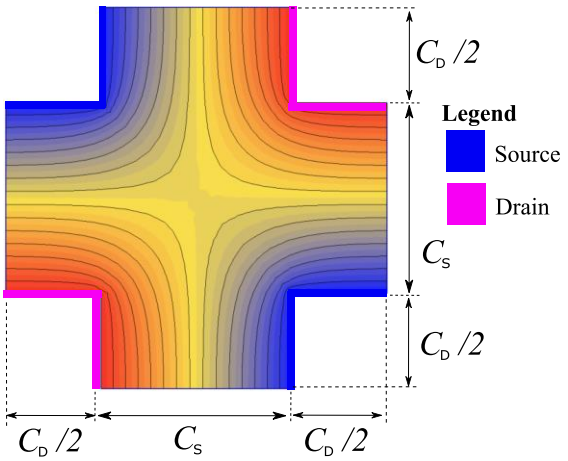


Fig. 5.7. Dimensions and terminals of the element with square shape contacts and simulated potential gradient solved with Agros2D.

The Area Increment calculated from width to length ratio between square shape contacts Fig. 5.7 for various dimensions simulated in 2D FEM solver Agros2D [73] are present in Tab. 5.1.

Tab. 5.1. The Area Increment calculated from width to length ratio between square shape contacts for various dimensions.

Potential										
C_S/C_D [-]	0.1	0.2	0.3	0.5	0.7	1.0	1.5	2.0	2.26	2.5
$(W/L)_{waff}$ [-]	20.52	10.54	7.20	4.53	3.38	2.54	1.87	1.55	1.43	1.34
$(W/L)_{fing}$ [-]	11.00	6.00	4.33	3.00	2.43	2.00	1.67	1.50	1.44	1.40
AI [%]	-46.4	-43.1	-39.8	-33.7	-28.2	-21.1	-10.9	-3.0	0.7	4.6

The Area Increment for 2DEG between square shape contacts can be seen in Fig. 5.8

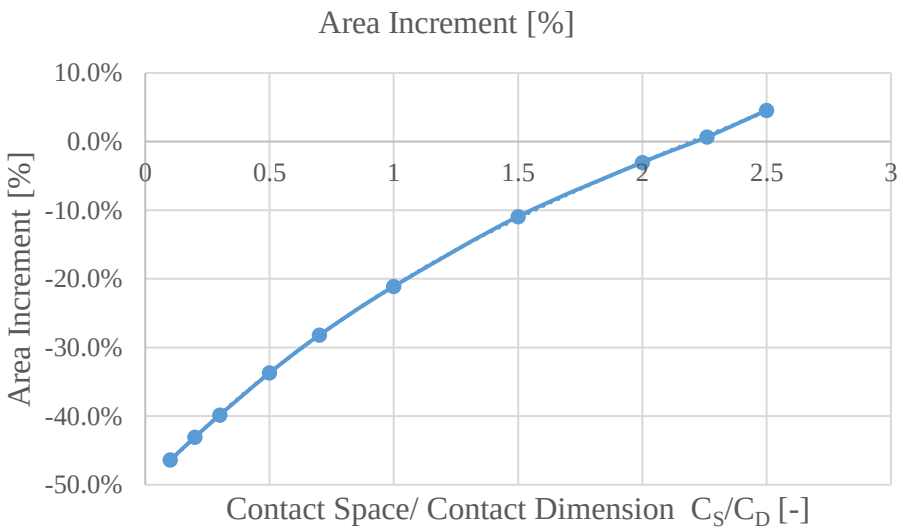


Fig. 5.8. Area Increment for square shape contacts.

The following function can approximate the Area Increment for 2DEG between square shape contacts.

$$AI_{\mathrm{ConSq}} = 0.0136\left(\frac{C_S}{C_D}\right)^3 - 0.096x\left(\frac{C_S}{C_D}\right)^2 + 0.3735\frac{C_S}{C_D} - \\ - 0.5014 \tag{5.6}$$

In general, qualitative parameter Area Increment *AI* has a negative value for all use cases. Because only then the area of waffle structure occupies a smaller area than finger structure with the same resistance. The condition, when Area Increment is negative, is as follows

$$C_S < C_D\ 2.26. \tag{5.7}$$

5.3.3. Square contacts with 30% chamfer

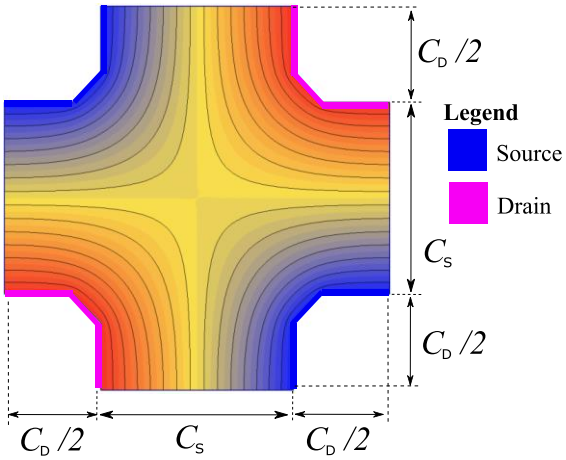


Fig. 5.9. Dimensions and terminals of the element with square shape contacts with 30% chamfer and simulated potential gradient solved with Agros2D.

The Area Increment calculated from width to length ratio between octagon contacts with 30% chamfer Fig. 5.9 for various dimensions simulated in 2D FEM solver Agros2D [73] are present in Tab. 5.2.

Tab. 5.2. The Area Increment calculated from width to length ratio between octagon contacts with 30% chamfer for various dimensions.

Potential										
C_S/C_D [-]	0.1	0.2	0.3	0.5	0.7	1.0	1.5	2.0	2.26	2.5
$(W/L)_{waff}$ [-]	17.00	9.10	6.36	4.12	3.13	2.38	1.79	1.48	1.38	1.30
$(W/L)_{fing}$ [-]	11.00	6.00	4.33	3.00	2.43	2.00	1.67	1.50	1.44	1.40
AI [%]	-35.3	-34.0	-31.8	-27.1	-22.4	-16.1	-6.7	1.1	4.8	8.0

The Area Increment for 2DEG between square shape contacts with 30% chamfer can be seen in Fig. 5.10.

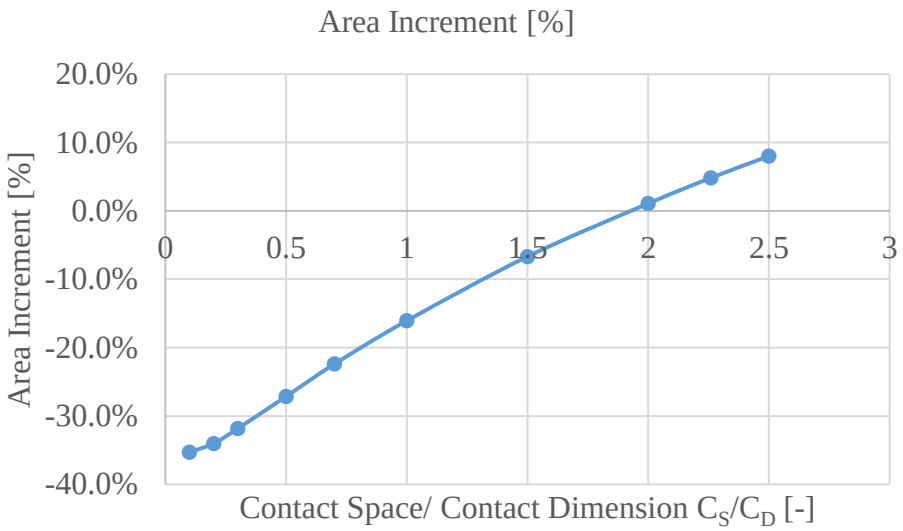


Fig. 5.10. Area Increment for octagon contacts with 30% chamfer.

The following function can approximate the Area Increment for 2DEG between octagon contacts with 30% chamfer.

$$AI_{\mathrm{ConO30}} = -0.0041\left(\frac{C_S}{C_D}\right)^3 - 0.0086\left(\frac{C_S}{C_D}\right)^2 + 0.2317\frac{C_S}{C_D} - 0.3825 \tag{5.8}$$

The condition, when Area Increment is negative, is as follows

$$C_S < C_D\ 1.9. \tag{5.9}$$

5.3.4. Square contacts with 58% chamfer

The Area Increment calculated from width to length ratio between octagon contacts with 58% chamfer Fig. 5.11 for various dimensions simulated in 2D FEM solver Agros2D [73] are present in Tab. 5.3Tab. 5.2.

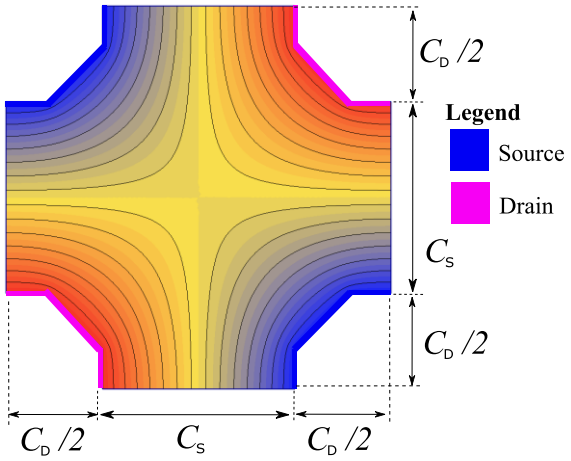


Fig. 5.11. Dimensions and terminals of the element with square shape contacts with 58% chamfer and simulated potential gradient solved with Agros2D.

Tab. 5.3. The Area Increment calculated from width to length ratio between octagon contacts with 58% chamfer for various dimensions.

Potential										
C_S/C_D [-]	0.1	0.2	0.3	0.5	0.7	1.0	1.5	2.0	2.26	2.5
$(W/L)_{waff}$ [-]	12.54	7.16	5.19	3.51	2.75	2.13	1.64	1.38	1.29	1.21
$(W/L)_{fing}$ [-]	11.00	6.00	4.33	3.00	2.43	2.00	1.67	1.50	1.44	1.40
AI [%]	-12.3	-16.2	-16.6	-14.5	-11.6	-6.1	1.5	8.9	12.3	15.6

The Area Increment for 2DEG between square shape contacts with 58% chamfer can be seen in Fig. 5.12.

The following function can approximate the Area Increment for 2DEG between octagon contacts with 58% chamfer.

$$AI_{\mathrm{ConSq}} = -0.0402\left(\frac{C_S}{C_D}\right)^3 + 0.1746\left(\frac{C_S}{C_D}\right)^2 - 0.0691\frac{C_S}{C_D} - \\ - 0.1419 \tag{5.10}$$

The condition, when Area Increment is negative, is as follows

$$C_S < C_D\ 1.4. \tag{5.11}$$

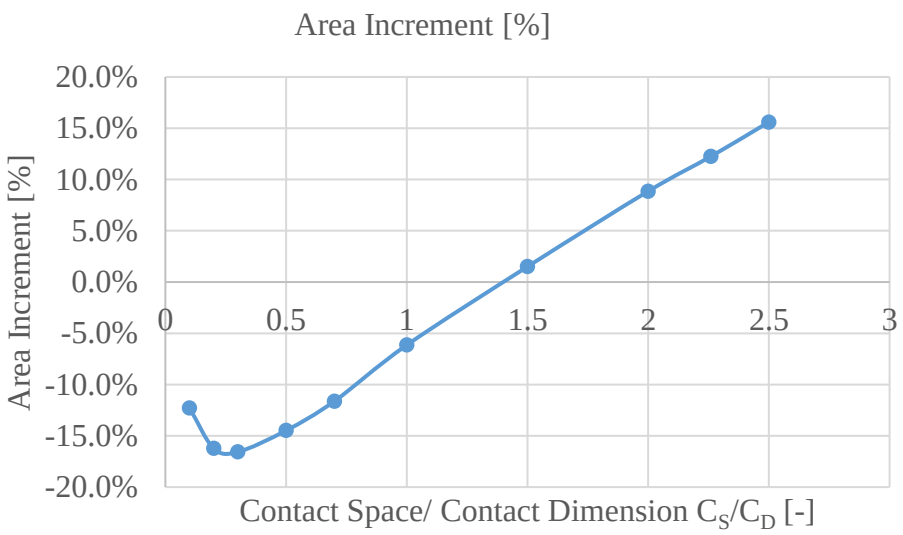


Fig. 5.12. Area Increment for octagon contacts with 58% chamfer.

5.3.5. Square and circle contacts

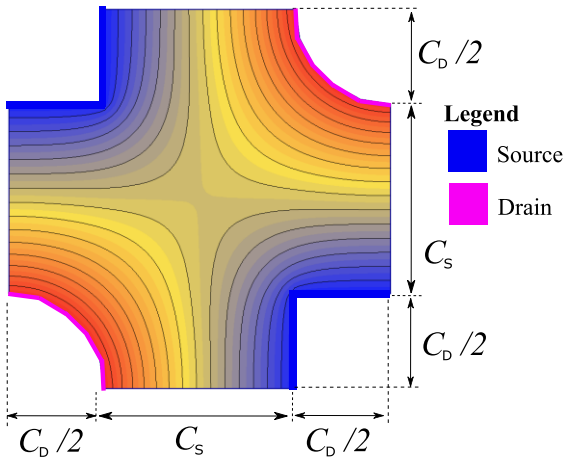


Fig. 5.13. Dimensions and terminals of the element with square and circle shape chamfer and simulated potential gradient solved with Agros2D.

The Area Increment calculated from width to length ratio between square and circle shaped contacts Fig. 5.13 for various dimensions simulated in 2D FEM solver Agros2D [73] are present in Tab. 5.4.

Tab. 5.4. The Area Increment calculated from width to length ratio between square and circle shaped contacts for various dimensions.

Potential										
C_S/C_D [-]	0.1	0.2	0.3	0.5	0.7	1.0	1.5	2.0	2.26	2.5
$(W/L)_{waff}$ [-]	12.05	7.40	5.48	3.73	2.89	2.23	1.71	1.42	1.34	1.24
$(W/L)_{fing}$ [-]	11.00	6.00	4.33	3.00	2.43	2.00	1.67	1.50	1.44	1.40
AI [%]	-8.7	-19.0	-21.0	-19.5	-16.1	-10.3	-2.2	5.9	7.5	12.8

The Area Increment for 2DEG between square and circle shaped contacts can be seen in Fig. 5.14.

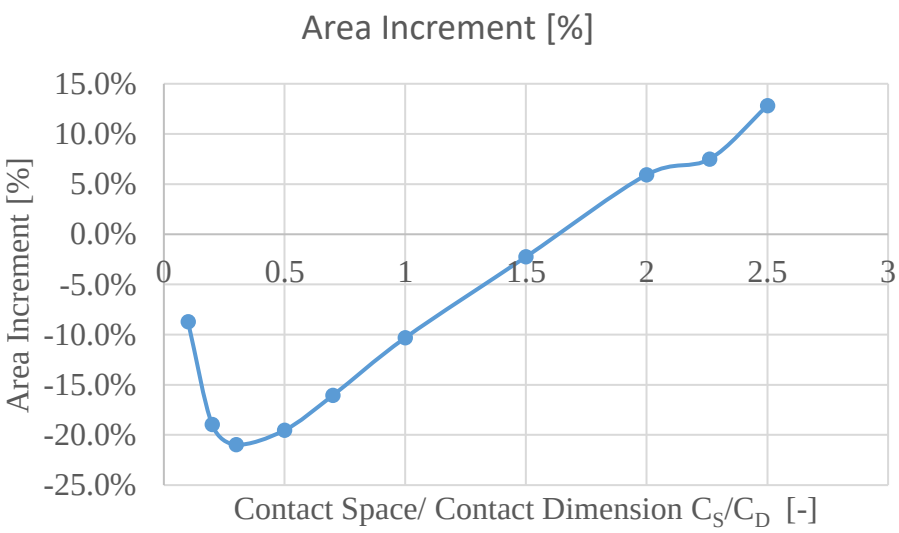


Fig. 5.14. Area Increment for square and circle shaped contacts

The Area Increment for 2DEG between square and circle shaped contacts can be approximated by the following function

$$AI_{\mathrm{ConSq}} = 0.1786\left(\frac{C_S}{C_D}\right)^6 - 1.4667\left(\frac{C_S}{C_D}\right)^5 + 4.7133\left(\frac{C_S}{C_D}\right)^4 - \\ - 7.5154\left(\frac{C_S}{C_D}\right)^3 + 6.1902\left(\frac{C_S}{C_D}\right)^2 - -2.2858\frac{C_S}{C_D} + 0.0827. \tag{5.12}$$

The condition, when Area Increment is negative, is as follows

$$C_S < C_D\ 1.65. \tag{5.13}$$

5.3.6. Circle contacts of waffle

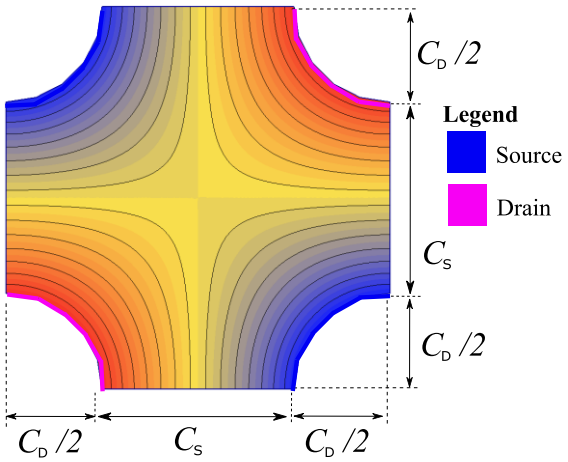


Fig. 5.15. Dimensions and terminals of the element with circle shape simulated potential gradient solved with Agros2D.

The Area Increment calculated from width to length ratio between circle shaped contacts for various dimensions simulated in 2D FEM solver Agros2D [73] are present in Tab. 5.5.

Tab. 5.5. The Area Increment calculated from width to length ratio between circle shaped contacts for various dimensions.

Potential										
C_S/C_D [-]	0.1	0.2	0.3	0.5	0.7	1.0	1.5	2.0	2.26	2.5
$(W/L)_{waff}$ [-]	9.46	6.04	4.58	3.22	2.56	2.02	1.57	1.33	1.24	1.18
$(W/L)_{fing}$ [-]	11.00	6.00	4.33	3.00	2.43	2.00	1.67	1.50	1.44	1.40
AI [%]	16.2	-0.7	-5.4	-6.9	-5.2	-1.2	6.0	12.9	16.1	19.0

The Area Increment for 2DEG between circle shaped contacts can be seen in Fig. 5.16.

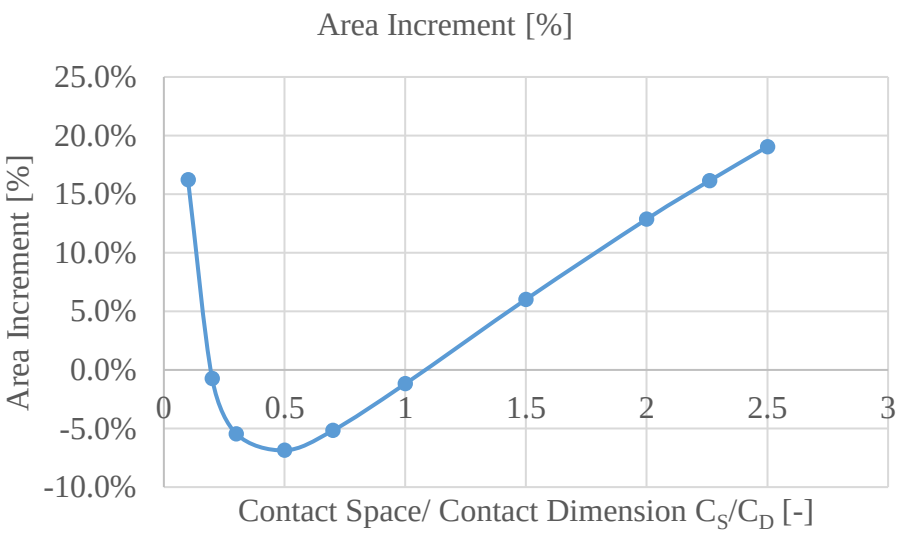


Fig. 5.16. Area Increment for square and circle-shaped contacts.

The Area Increment for 2DEG between circle shaped contacts can be approximated by the following function

$$AI_{\mathrm{ConSq}} = 0.1863\left(\frac{C_S}{C_D}\right)^6 - 1.5955\left(\frac{C_S}{C_D}\right)^5 + 5.3711\left(\frac{C_S}{C_D}\right)^4 - 9.0155\left(\frac{C_S}{C_D}\right)^3 + 7.8823\left(\frac{C_S}{C_D}\right)^2 - 3.2412\frac{C_S}{C_D} + 0.4077. \quad (5.14)$$

The condition, when Area Increment is negative, is as follows

$$C_S < C_D\ 1.1. \quad (5.15)$$

5.3.7. Contacts pattern comparison

Shape and pattern of contact (rectangle, square, square with chamfer or circle) in GaN HEMT influence $R_{\mathrm{DS\text{-}ON}}$. The square shape contacts placed in the waffle pattern can reach the best *AI* performance improvement up to compared to other contact shape and patterns. In opposite, the circle shape of contacts placed in the waffle pattern can reach worst *AI* performance improvement compare to another contact shape. The higher chamfer on square contacts leads to a decrease of *AI* performance. Pattern with square and circle contacts have better *AI* performance improvement compare to square contacts with 58% chamfer.

For higher BV of the drain to gate, the square shape drain contact with higher chamfer or circle shape is more suitable.

Proposed new patterns can be applied to all lateral normally-On or normally-Off GaN HEMT processes. New proposals are lateral structures and due to this have perspectives for integration into power management Integrated Circuits on GaN substrates. It is more suitable to use waffle gate pattern or new dissimilar square waffle gate pattern or octagon waffle gate pattern when contacts dimensions are 1.1 times larger than contact spacing.

5.4. BV of GaN HEMT

This TCAD simulation demonstrates the influence of the gate to drain distance L_{dg} and buffer layer thickness T(buffer) on the breakdown voltage and is based on the following references [122], and [123] Fig. 5.17.

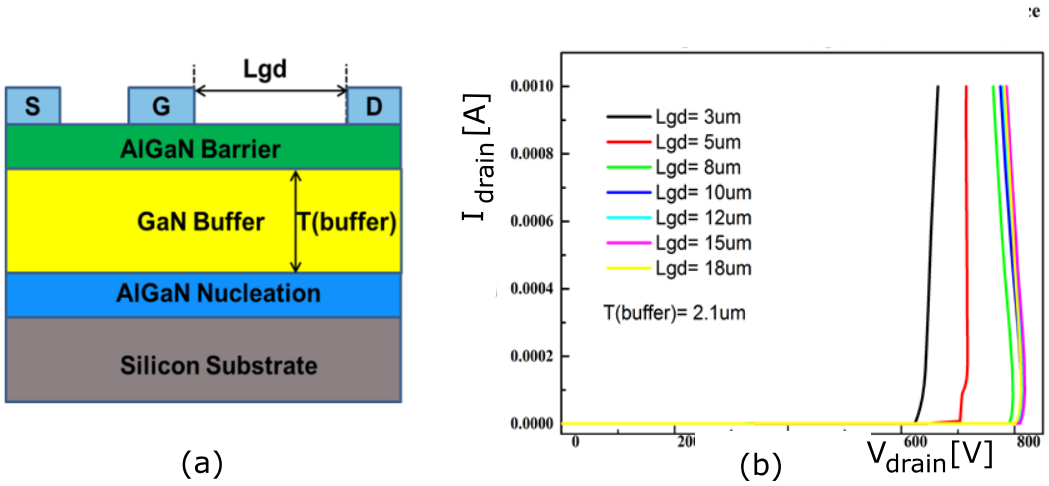


Fig. 5.17. GaN HEMT a) definition of GaN HEMT normally-on transistor, with parametric gate to drain spacing L_{gd}, b) the BV characteristic curves with varying gate to drain spacing L_{gd} from 3 μm to 18 μm were simulated when T(buffer) is 2.1 μm [123].

I have been demonstrated [122] that BV is defined by an avalanche phenomenon between the gate and the substrate due to charge accumulation at the GaN/Silicon interface.

The BV of GaN HEMT also depends on the thickness of GaN buffer T(buffer) and for thicker buffer higher BV can be reached [123]. The BV can also be improved by adding field plate connected to the gate [124], and our proposals are compatible with it. Additionally, known phenomena are BV dependence on surface passivation

material [125]. Finally, BV of GaN HEMT depends on the gate to drain distance L_{dg}. For the larger gate to drain distance, the higher BV can be reached as it is described in [122], and [123] Fig. 5.17.b).

As it is, describe in Fig. 5.3 both proposed GaN HEMT topologies, the dissimilar square waffle gate pattern [11] and octagon waffle gate pattern [10] can change independently spacing between the gate and drain contacts and spacing between gate and source contacts. Because larger gate to drain distance L_{dg} lead to higher BV by increasing D_1 distance and D_3 distance the higher BV can be reached by having more compact shape compare to finger shape gate pattern.

5.5. Waffle GaN HEMT Fabrication

Fabrication of proposed GaN HEMT with waffle gate patterns is realized with the cooperation of Slovak Academy of Science (SAS). To simplify the manufacturing process, the Normally-On HEMT based on AlGaN/GaN heterostructure was chosen. To prove the proposed concepts, the two different substrates are used, the less expensive Si substrate and more expensive SiC substrate but with better lattice matching to GaN. Because SiC has approximately two times better thermal conductivity than Silicon (Tab. 2.4) by using SiC substrate for GaN HEMT much better heat dissipation of power devices can be reached.

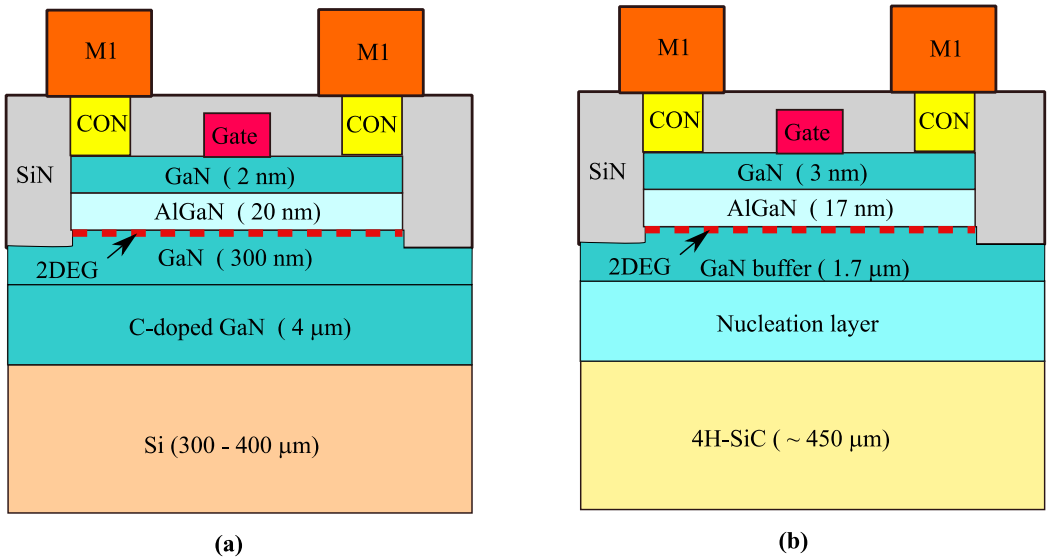


Fig. 5.18. SAS process: (a) AlGaN/GaN/Si HEMT structure; (b) AlGaN/GaN/SiC HEMT structure, where Gate is Schottky gate metal, CON is Ohmic contact metallization, and M1 is metallization for PAD and interconnections.

The source AlGaN/GaN HEMT structures grown on Si and SiC substrates are described in Fig. 5.18 a) and b), respectively. The proposed heterostructure layers with an induced 2-dimensional electron gas (2DEG) are commercially grown by metal organic chemical vapor deposition (MO CVD) method using an optimized growth process.

The SiC AlGaN/GaN wafer is from CREE and is<475 μm in thickness, the substrate is 4H-SiC, with 100.00 mm in diameter, the resistivity is greater than 1.0×10^5 Ω cm, both sides are polished. The AlGaN barrier layer in both types of heterostructures contains 29.5% of Al.

The simplified GaN HEMT process flow from SAS is as follows:

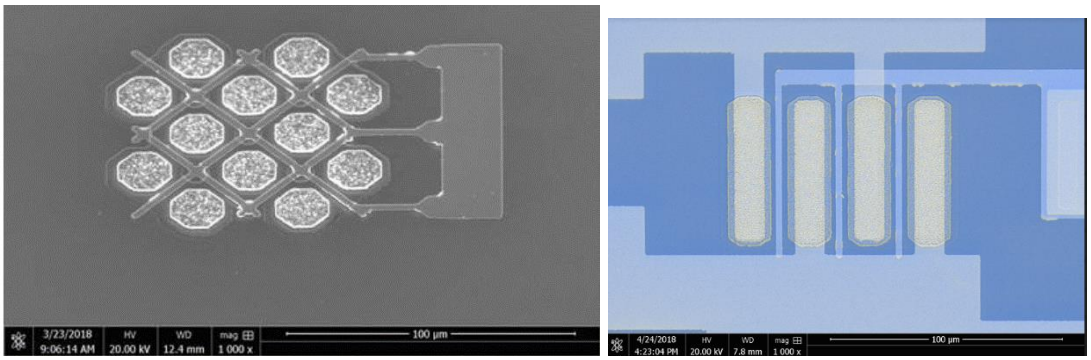
1) DIE cut of AlGaN/GaN/Si or AlGaN/GaN/SiC wafer
2) Contact
   - Ohmic Contact deposition
   - Contact patterning by „lift-off“
   - Contact annealing
3) Active region
   - Active area patterning
   - Active area MESA dry etching
4) Gate
   - Gate Schottky metal deposition
   - Gate patterning by „lift-off“
5) Passivation
   - Passivation layer (SiN) deposition
   - Passivation patterning by dry etching
6) PAD metallization M1
   - M1 deposition
   - M1 Patterning by „lift-off“

The MESA etching is applied outside the defined active area to break the 2DEG region and to allow separation/isolation of transistors (from each other) placed nearby on the same substrate.

The Ohmic Contact comprises of an Nb (20 nm) / Ti (20 nm) / Al (120 nm) / Ni (40 nm) / Au (70 nm) stack. In comparison to the conventional Ti/Al/Ni/Au metallization scheme, a thin Nb layer is added to enhance the surface morphology and specific contact resistivity [126]. Ni is used to prevent the forming of Au-Al intermetallics and unwanted in-diffusion to the sample interface.

Two different Schottky gate metallization were proposed for possible comparison of the HEMTs performance at elevated temperatures in the future. In our experiments, a stack of Ir (40 nm) / Au (80 nm) or Ni (40 nm) / Au (80 nm) was used.

The PAD metallization M1 consists of Ti (15 nm) / Au (100 nm). It is designed to improve metallic interconnections and device bonding. The thin Ti layer is deposited prior to Au to strengthen the adhesion.



a) **b)**

Fig. 5.19. Fabricated GaN HEMT normally-on transistor a) waffle gate after MESA etching, Schottky gate and ohmic contact fabrication (before SiN passivation and PAD metallization process); b) finger gate HEMT after all process steps.

Sample fabrication has been divided into two phases:

- in the first phase, the samples have been used for process tuning and preliminary evaluation
- in second phase samples has been used for qualifications

The sample from the first phase is present in Fig. 5.19 a) where GaN HEMT normally-on transistor with waffle gate is stopped before SiN passivation and PAD metallization process. Finally, fully finished GaN HEMT normally-on transistor with finger gates is in Fig. 5.19 b). All samples of GaN HEMT with waffle gate from the first phase has been facing two types of problems. The waffle gate GaN HEMT with smaller gate and source spacing than 1µm has been shorted Fig. 5.20 (a). This type of errors has been caused by week resolution of used lithography and has been fixed by

using larger gate-source spacing than 1μm. For waffle gate, GaN HEMT with larger than1μm gate and source spacing those shorts has not been observed. The second type of the issue has been observed on crossing area of waffle gates. There was a short between gate and source interconnections in metal above Fig. 5.20 (b). The issue has been caused due to unconformity of the gate electrode at crossing area and due to thin SiN passivation. The problem can be solved by using a thicker passivation layer.

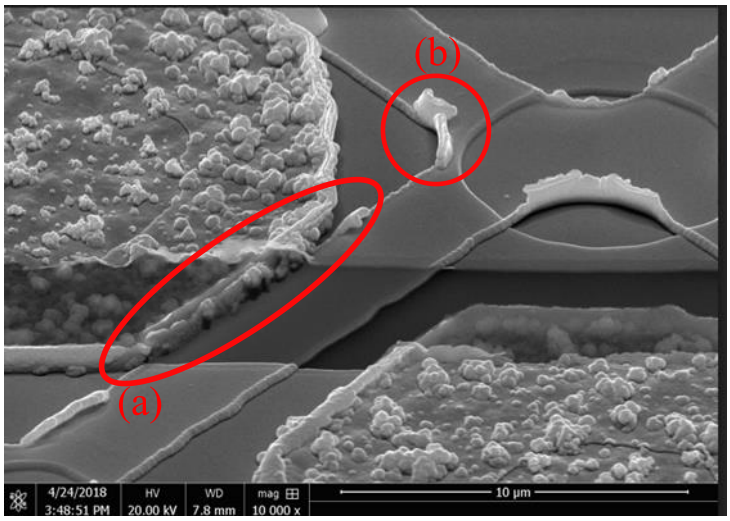


Fig. 5.20. Defects of Waffle GaN HEMT transistor: a) short of gate and source contact due to lithography issue for small 1μm proximity; b) short of the gate and source interconnection with metal above, due to unconformity of the gate at crossing area and due to thin SiN passivation

After all, issues have been analyzed and solved the second phase of fabrication should begin. The samples from the second phase are now in the fabrication process.

The physical design verification of GaN IC has realized with Calibre DRC [79] with a custom run set of DRM rules.

5.6. Measurement

For measurement of GaN HEMT transistors has been used Semiconductor Device Parameter Analyzer/Semiconductor Characterization System Mainframe B1500A from Agilent Technologies.

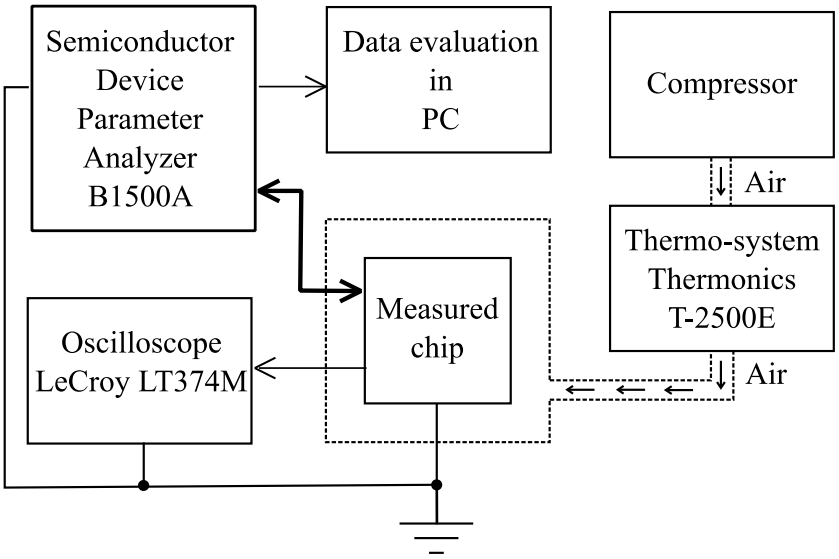


Fig. 5.21. Measurement scheme for GaN HEMT transistors

For verification reason oscilloscope, LeCroy LT374M has been used. To set precise temperature conditions, the thermos-system Thermonics T-250E has been used.

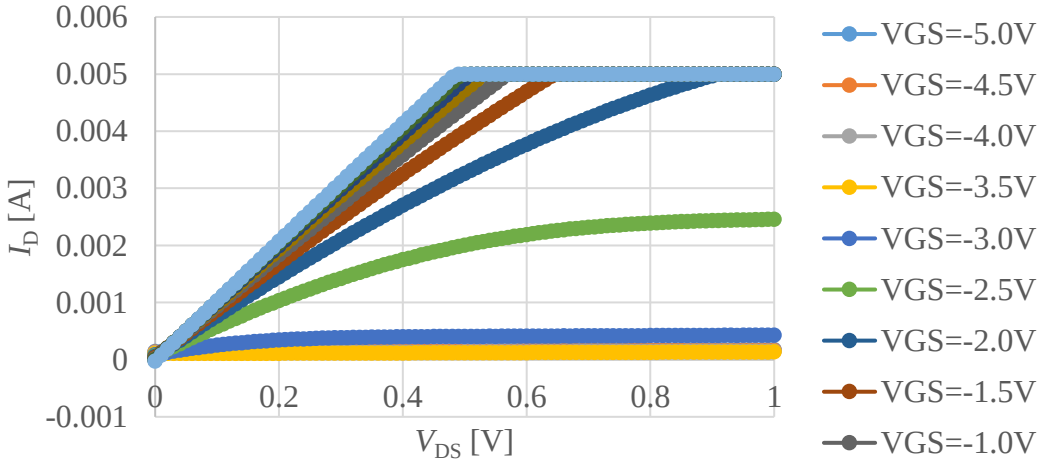


Fig. 5.22. The measured output characteristic of AlGaN/GaN/Si HEMT normally-On, with finger gate structure for different gate voltages at 25°C, current limit for measurement is 5 mA

The drain-source resistance measurement has been realizing by four terminals method where based on sensed drain-source voltage V_{DS} the drain current I_D is forced.

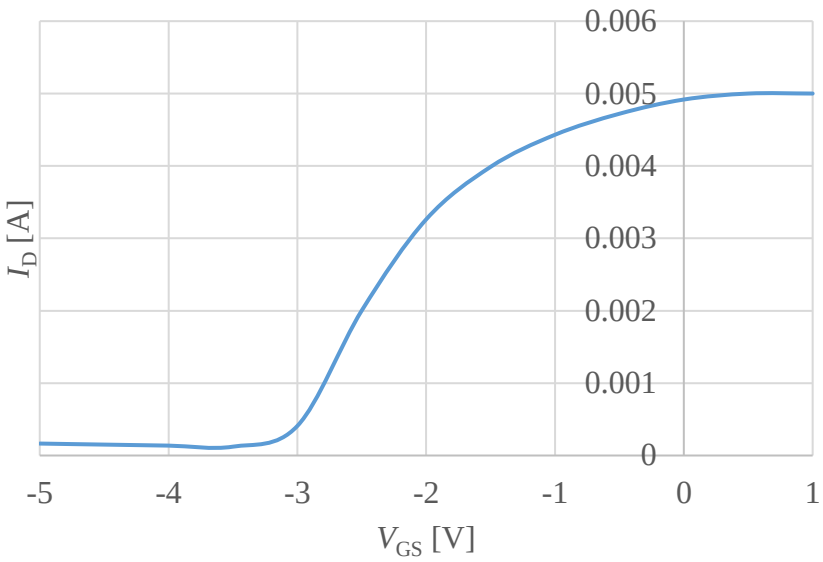


Fig. 5.23. The measured transfer characteristic of AlGaN/GaN/Si HEMT normally-On, with finger gate structure at 25°C,

Measurement of drain current versus drain-to-source voltage output characteristic, of AlGaN/GaN/Si HEMT with finger gate structure for different gate voltages at 25°C is in Fig. 5.22.

The transfer characteristic of AlGaN/GaN/Si HEMT with finger gate structure is in the Fig. 5.23. The transfer and output characteristic for AlGaN/GaN/Si HEMT with waffle gate pattern, octagon, and dissimilar square waffle gate pattern will be measured on second phase samples where the issue with short is fixed.

5.7. Conclusion for Waffle GaN Topologies

To improve the channel resistance of HV power GaN HEMT the new topologies have been proposed and described. The specific on-resistance can be reduced by using proposed new power GaN HEMT topologies with dissimilar square waffle pattern [11] and with octagon waffle pattern [10]. The area saving compared to standard finger gate pattern is up to 40 % depending on contact shape and pattern. In addition production cost of GaN HEMT can be reduced by decreasing chip area and by it yield improvement. The standard waffle gate pattern and proposed two new gate patterns the dissimilar square waffle and octagon waffle pattern can apply for any lateral normally-On or normally-Off GaN HEMT processes. New proposals are lateral

structures and due to this are perspectives for integration into power management integrated circuits on GaN substrates. Shape and pattern of contacts (rectangle, square, square with chamfer or circle) influence on-resistance of new GaN HEMT. The square shape of contacts placed in the waffle pattern can reach more than 40 % area reduction for $C_S/C_D < 0.3$ and 16.1 % reduction for contacts spacing C_S same as contact dimension C_D what is the best Area Increment *AI* performance improvement compared to other contact shapes in waffle patterns. In opposite, the circle shape of contacts placed in the waffle pattern can reach up to 6.9 % area reduction for $C_S/C_D < 0.5$ and 1.2 % area reduction for $C_S/C_D = 1$ compare to finger topology what is lowest *AI* performance improvement compare to another contact shape. The higher chamfer on square contacts leads to a decrease of *AI* performance. Pattern with square and circle contacts reach up to 21% area reduction for $C_S/C_D < 0.3$ and 10.3 % area reduction for $C_S/C_D = 1$ compare to finger topology what is better *AI* compare to square contacts with 58% chamfer where has been reach up to 16.6 % area reduction for $C_S/C_D < 0.3$ and 6.1 % area reduction for $C_S/C_D = 1$.

For the higher drain to gate BV of GaN HEMT, the square shape drain contact with higher chamfer or circle shape is more suitable. In general, for the same on-resistance the area can be reduced for: waffle gate pattern, new dissimilar square waffle gate pattern or octagon waffle gate pattern if contacts dimension C_D is 1.1 times larger than contacts spacing C_S.

5.8. Possible Future Development of Waffle GaN Topologies

The main advantage of proposed AlGaN/GaN/Si HEMT with waffle gate pattern, octagon waffle and dissimilar square waffle gate patterns is that is compatible with different processes, not just for power conversion but also for high-frequencies modulation system where the specific resistance is reduced. Therefore, the development of RF AlGaN/GaN/Si HEMT with waffle gate pattern, octagon waffle, and dissimilar square waffle gate patterns are promising for future GaN IC.

6. Additional Structure Proposals

The dimension scaling of HV power Trench MOSFET in smart power IC is very beneficial due to efficiency improvement of power discreet and due to production costs reduction by decreasing chip area and by it yield improvement in SiC. To fulfill those expectation several lateral HV Trench MOSFET are described and modeled.

Parts of this chapter has been presented by the author of this thesis in [12] Author of this thesis contributes to this chapter by 80%.

6.1. New Trench MOS Proposals

The Trench MOSFET is shown in Fig. 6.1 is currently a widely used architecture as overcoming the Drift MOSFET architecture, and Double diffused MOSFET (DMOS) architecture regarding specific On resistance.

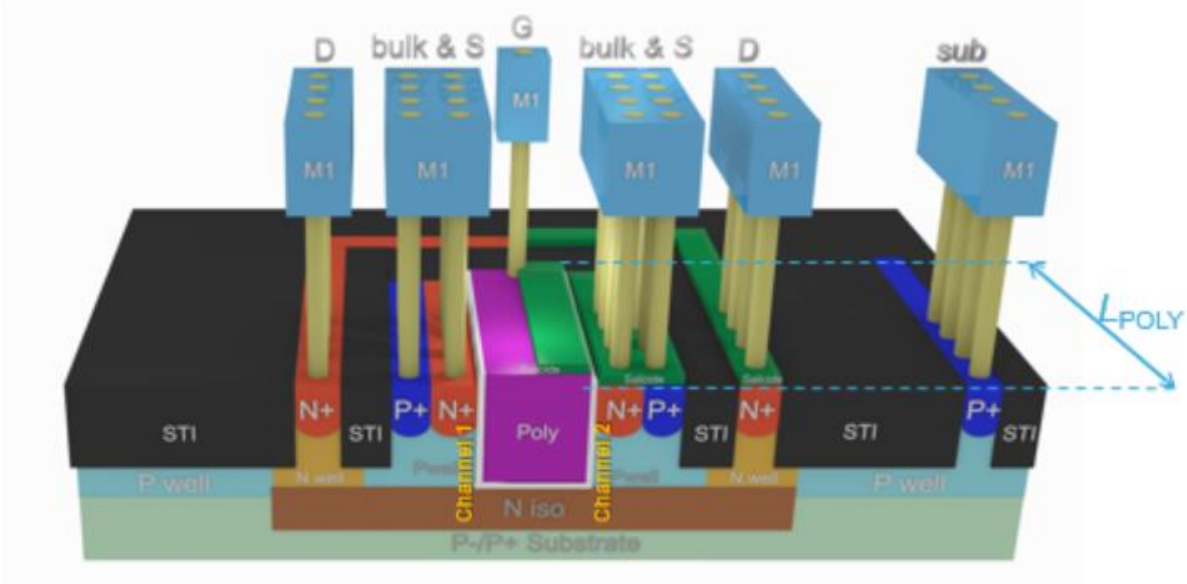


Fig. 6.1. Vertical channel orientation of Trench MOSFET [12]

The MOSFETs using the trench gate allow to reach lower specific on-resistance hence vertical structure to enhance the channel density. To improve the specific On-Resistance of the Trench MOSFET architecture, the different trench gate pattern like Waffle [34] or hexagon in XtreMOS [1] is used.

6.1.1. Trench MOS with source with waffle pattern

Due to the improvement of specific On-Resistance, the new architecture of Trench MOSFET with Source with Waffle pattern is proposed Fig. 6.2. New Trench MOSFET is a vertical structure with the lateral connection of all terminals.

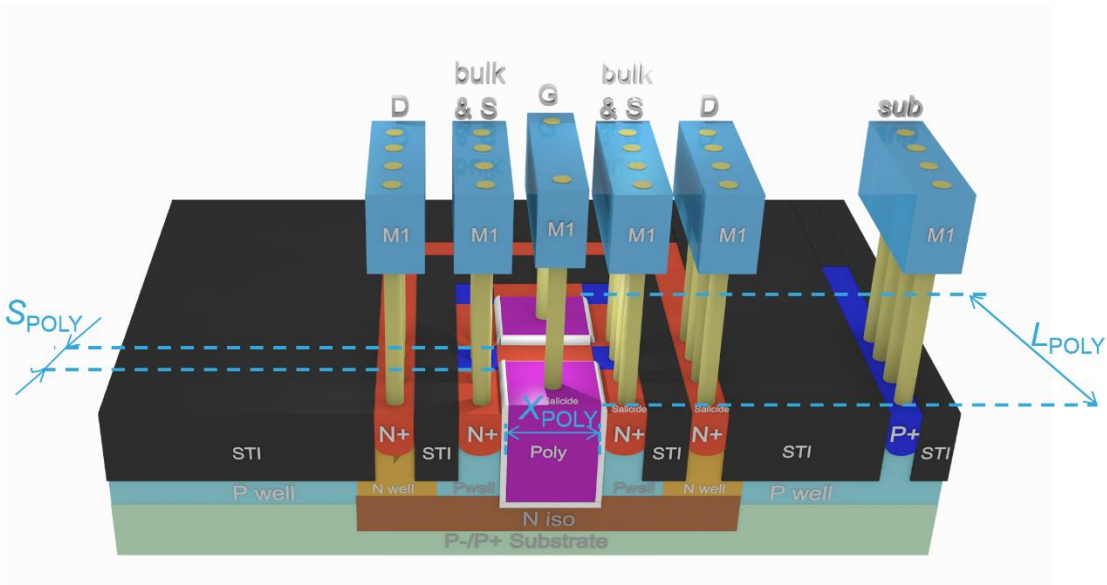


Fig. 6.2. Proposal of new Trench MOS with Source with Waffle pattern [12]

A gate is a vertical trench, source and Bulk are on top and Drain is at the bottom and is laterally connected. A Bulk implant is located between Gates and is on surface connected via Salicide with Source.

When the spacing between polysilicon Gates S_{POLY} is smaller than the dimension of polysilicon Gate $X_{POLY,}$ then the sum of gates perimeters which is equivalent to channel width is larger than for conventional Trench MOSFET.

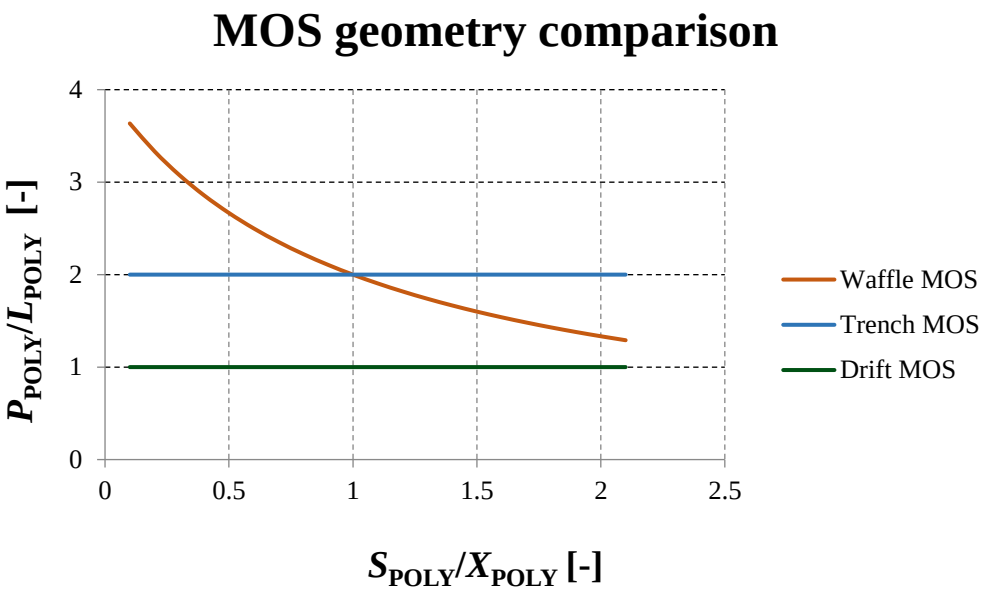


Fig. 6.3. : Comparison of new Trench MOS with Source with Waffle pattern (Waffle MOS) with conventional Drift MOS and Trench MOS base on normalized gates perimeter (equivalent to channel width) [12]

If the spacing between gates segments S_{POLY} is smaller than the dimension of gate segment X_{POLY} then the sum of gates perimeters, (which is equivalent to channel width) is larger than for conventional Trench MOSFET (6.4).

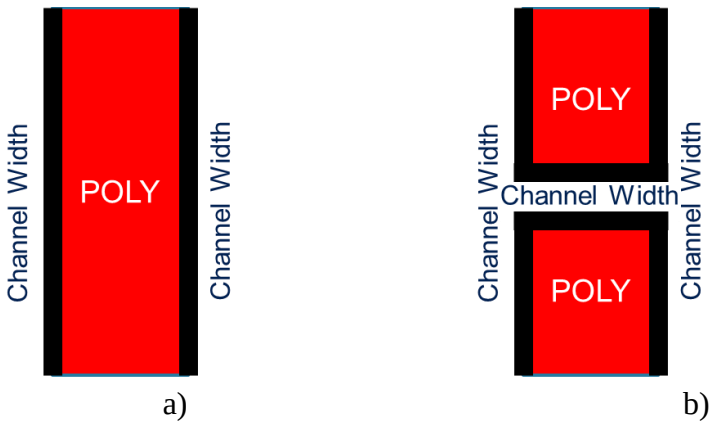


Fig. 6.4. Top view on channel width for: a) Trench MOSFET b) improved channel width of Trench MOSFET with Source with Waffle pattern [12]

Trench MOS with Source with Waffle pattern by using multi-square trench gate has a larger gate perimeter (equivalent to channel width) than conventional Trench MOS Fig. 6.3 and so we can expect lower specific On-Resistance.

6.1.2. Trench MOS with triangle gate pattern

The Trench MOS with Source with Waffle pattern overcome conventional Trench MOS structures because by using multi-square trench gate we can fit more gate perimeter per area. To find even better topology we have to find 2D polygon with even larger perimeter P_P per area first.

Let's consider basic formulas for calculation of perimeter P_P and

$$P_P = n\,s \tag{6.1}$$

area of regular polygon A_P with n sides and with the length of side s

$$A_P = \frac{1}{2}\,ap\;\;n\;\;s = \frac{1}{2}\,ap\;\;P_P \tag{6.2}$$

Where ap is apothem and define the shortest distance from the side of a polygon to the center and can be calculated as follows

$$ap = \frac{s}{2\tan\left(\frac{\pi}{n}\right)} \tag{6.3}$$

From equations (6.2) and (6.3) we can get the formula for side length of regular polygon s as follows

$$s = 2\sqrt{\frac{A_P\tan\left(\frac{\pi}{n}\right)}{n}} \tag{6.4}$$

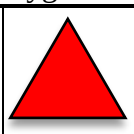
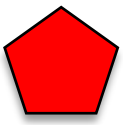
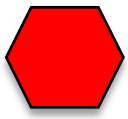
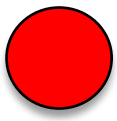
By insertion (6.4) to equation (6.1) we can get a direct relation between perimeter P_P of a regular polygon on some sides n and on its area A_P as follows:

$$P_P = 2\,n\sqrt{\frac{A_P\tan\left(\frac{\pi}{n}\right)}{n}} \tag{6.5}$$

For comparison of polygon let's consider unit polygon area equal to one. Then we get the following Tab. 6.1.

From Tab. 6.1we can see that square is not an optimal polygon regarding the perimeter. The largest perimeter for a unit area is for a polygon with a triangle shape. Another conclusion is that when the number of polygon sides increases the perimeter is decreased.

Tab. 6.1. Dependence of Perimeter of a regular polygon on some polygon sides *n* for polygons with the unit area (A_P=1) [12].

					
Polygon	triangle	square	pentagon	hexagon	circle
Sides *n*	3	4	5	6	infinite
Perimeter $P_P(A_P=1)$	4.56	4.00	3.81	3.72	3.54

To get Trench MOSFET with lower specific On-Resistance, we have to choose a trench gate with triangle pattern Fig. 6.5. The higher perimeter means higher channel width, and its lower resistance.

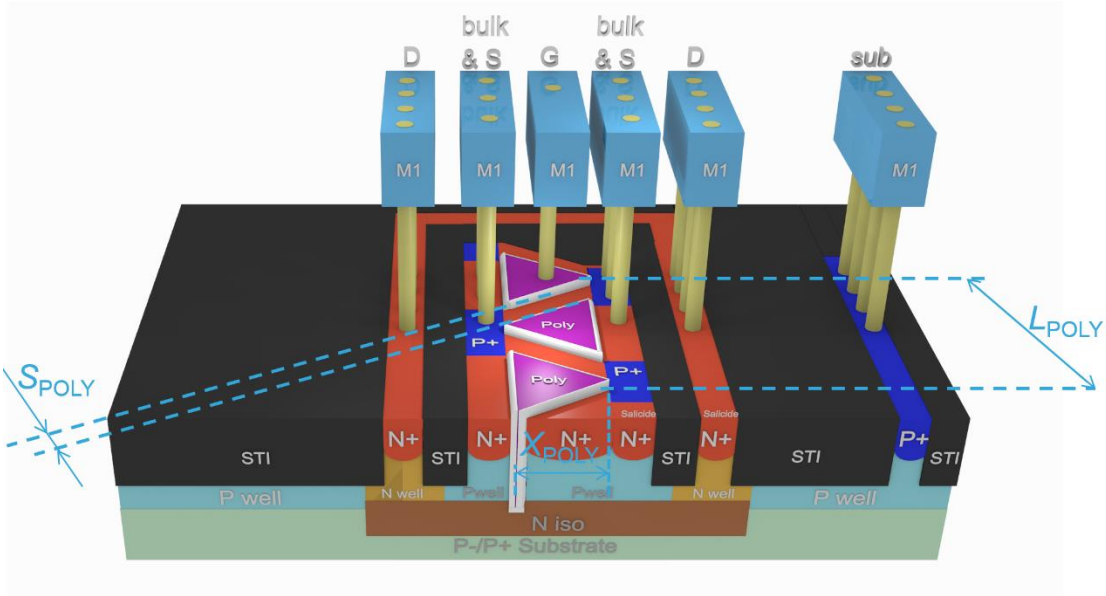


Fig. 6.5. Proposal of new Trench MOS with Triangle gate pattern (Triangle MOS) [12].

When the spacing between polysilicon Gates S_{POLY} is smaller than the dimension of polysilicon Gate X_{POLY}, then the sum of gates perimeters which is equivalent to channel width is larger than for Trench MOS with Source with Waffle pattern or for conventional Trench MOSFET Fig. 6.6.

The trench MOS with Triangle gate should have lower specific On-Resistance than Trench MOS with Source with Waffle pattern or conventional Trench MOS hence Trench MOS with Triangle gate have larger gate perimeter (equivalent to channel width) per area.

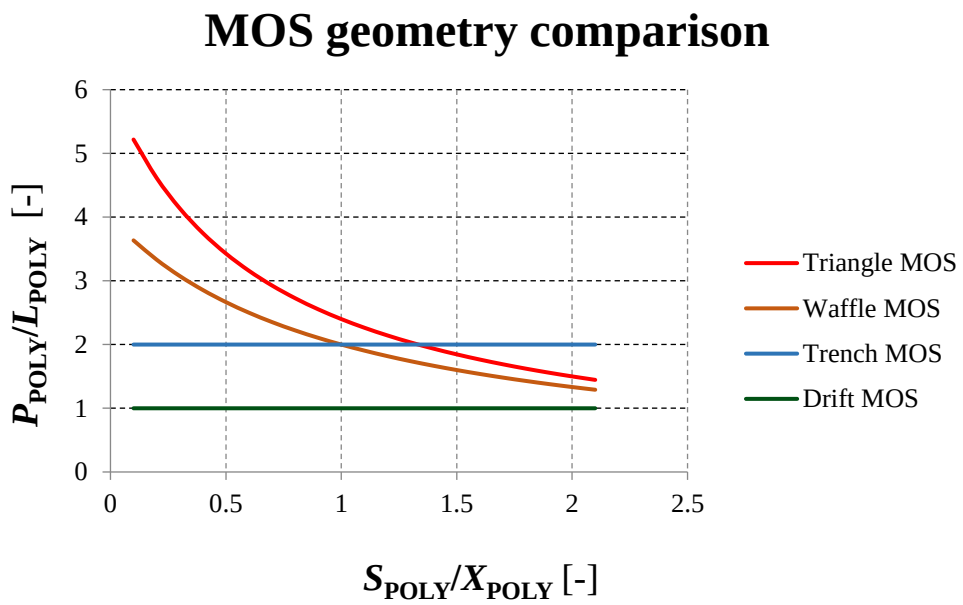


Fig. 6.6. Comparison of new Trench MOS with Triangle gate pattern (Triangle MOS) with conventional Drift MOS and Trench MOS and with Trench MOS with Source with Waffle pattern (Waffle MOS) base on normalized gate perimeter (equivalent to channel width) [12].

6.1.3. Conclusion for trench MOS

In was described two new Trench MOSFET structures with optimized specific On resistance parameter. The first structure is Trench MOSFET with Source with Waffle pattern and the second structure is Trench MOSFET with Triangle gate pattern. If gates segments spacing is smaller than segment dimensions, then both new structures have better specific On resistance than Drift MOSFET or Trench MOSFET. Smallest specific On resistance is reach for Trench MOSFET with Triangle gate pattern.

Due to sharp edges of the gate segment, the lower break down voltage is expected for Triangle gate pattern. Trench MOSFET with Source with Waffle pattern should be a good compromise due to lower specific On resistance and higher breakdown voltage.

For different trench MOSFET structures comparison, the normalized gate segment perimeter was used as an alternative figure of merit to specific On resistance.

6.2. GaN Nano-channel GAA

Nanowire-based field-effect transistors are among the most promising means of overcoming the limits of today's planar silicon electronic devices, in part because of

their suitability for gate-all-around architectures (GAA) Fig. 6.1., which provide perfect electrostatic control and facilitate further reductions in “ultimate” transistor size while maintaining low leakage currents [127].

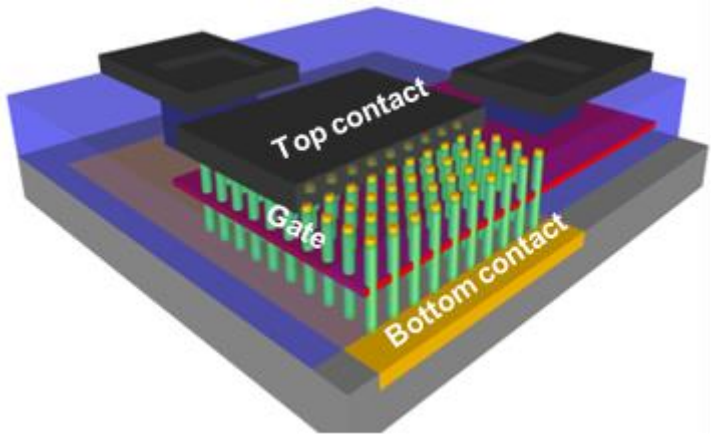


Fig. 6.1. Nanowire-based field-effect transistors (GAA FET) [127]

The GAA FET concept is currently considering for low power and low voltage applications only. However, base on analogy with FinFET architecture which was implemented in HV segment we can expect that GAA FET concept can be also applied in the high voltage power application.

To ensure that GAA structure provides for the highest capacitive coupling between the gate and the channel the cross-section of the channel must be small enough so that the gate can deplete the heavily doped channel entirely (OFF state). The concept of the junctionless transistor is very promising and suitable for the requirement of a new semiconductor device. The doping concentration is constant and uniform throughout the device.

7. Power IC Layout Implementation Flow Improvements

It is well-known practice in the semiconductor industry that by optimizing implementation flows can be reduced the development time, and it cost.

The smart power IC contain not only power devices but also analog and digital control parts. All modern CAD environments (from Cadence and Synopsys) allow doing only manual analog layout implementation. Only for digital designs (due to standard cells dimensions) is possible to realize automatic placement and automatic outing.

To optimize analog layout implementation flow for smart power IC, the several improvements were developed and are using in STMicroelectronics.

Parts of this chapter has been presented and published by the author of this thesis in [13], [14], [15]; [16], and [17]. Author of this thesis contributes to this chapter by 85%.

7.1. Incremental Control

During the creation of analog layout in Cadence, CAD environment layout engineers spend a lot of time by modifying objects in a database. By applying new control concept and targeting modern control approaches our solution unifies and simplifies control of any layout object to speed-up work. Discussed new control techniques are compatible with Cadence CAD environment and both current control devices as keyboard/mouse and new gesture tracking devices [15].

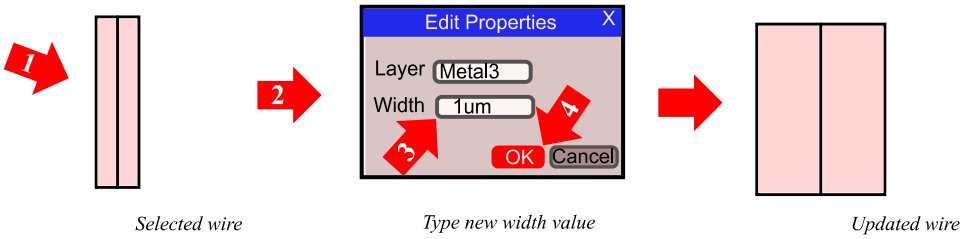


Fig. 7.1. The example of standard four steps modification flow for wire width change in the Virtuoso Layout Suite [14]

Virtuoso Layout Suite is very universal and user-friendly environment for physical implementation of integrated circuits [75]. Common concept for modification of selected layout objects is through the Edit Properties window and consist from four steps. For example, a width of a selected wire can be changed by using the bindkey "Q" to call the Edit Properties window, then type a new value for the wire width and press the OK button to apply Fig. 7.1.

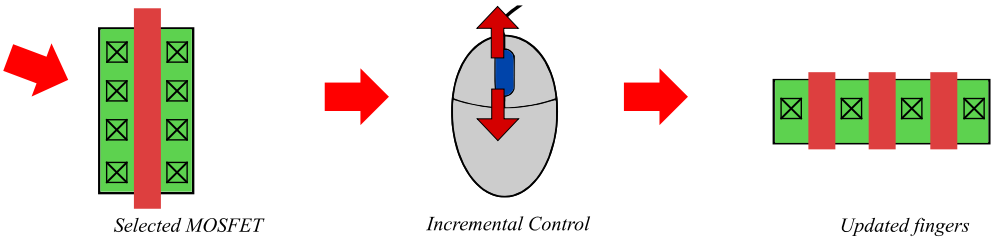


Fig. 7.2. The example of a number of gate finger modification of MOSFET by using Incremental Control [14].

The Incremental Control Fig. 7.2 brings an intuitive common control concept which reduces the number of actions needed to reach the optimal result.

The principles of the new control concept for layout object modifications are described by Fig. 7.3 and is described in [14].

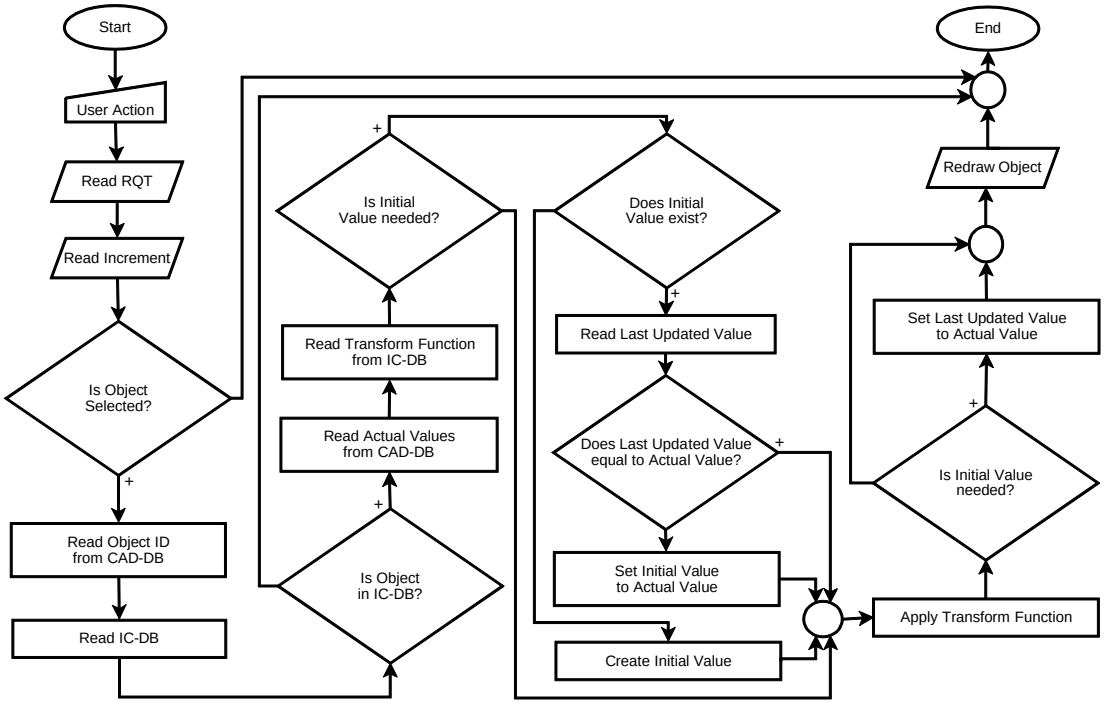


Fig. 7.3. The flow chart of Incremental Control [14].

To quantify layout productivity gain, the average time of standard control modification t_{SC} and the average time of Incremental Control modification t_{IC} to reach the target value of layout objects with random initial value are introduced. Relative difference of t_{IC} and t_{SC} has been used for calculation of average layout productivity gain for each layout object type. Based on measurement which is noted in Tab. 7.1, time-saving is in the range of 23% to 66%. In Tab. 7.1 there is evidence that higher efficiency is reached when different objects are modified simultaneously.

Tab. 7.1. Layout productivity measurement results [15]

Layout object	t_{SC} **[s]**	t_{IC} **[s]**	$(t_{IC} - t_{SC}) / t_{SC}$ **[%]**	**Layout object**	t_{SC} **[s]**	t_{IC} **[s]**	$(t_{IC} - t_{SC}) / t_{SC}$ **[%]**
via	5.6	2.0	-64.7	pin + label	15.1	5.0	-66.7
wire	4.6	3.5	-23.4	rectangle	5.2	3.2	-38.5
pin	7.0	4.5	-36.1	transistor	5.6	3.7	-33.6
label	5.8	3.5	-39.9	capacitor	5.4	3.5	-35.2

Discussed new control technique is compatible with the Cadence CAD environment and with current control devices such as a keyboard, mouse. In addition to it is also compatible with new gesture tracking systems. The Incremental Control is usually mapped to mouse wheel but has been experimentally mapped to gesture recognition camera Creative Senz3D using Fig. 7.4 [128].

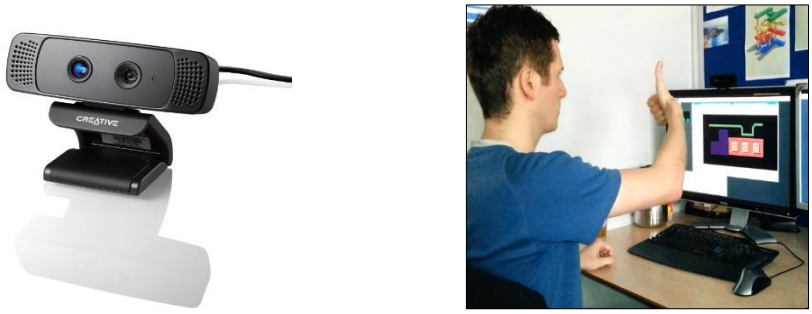


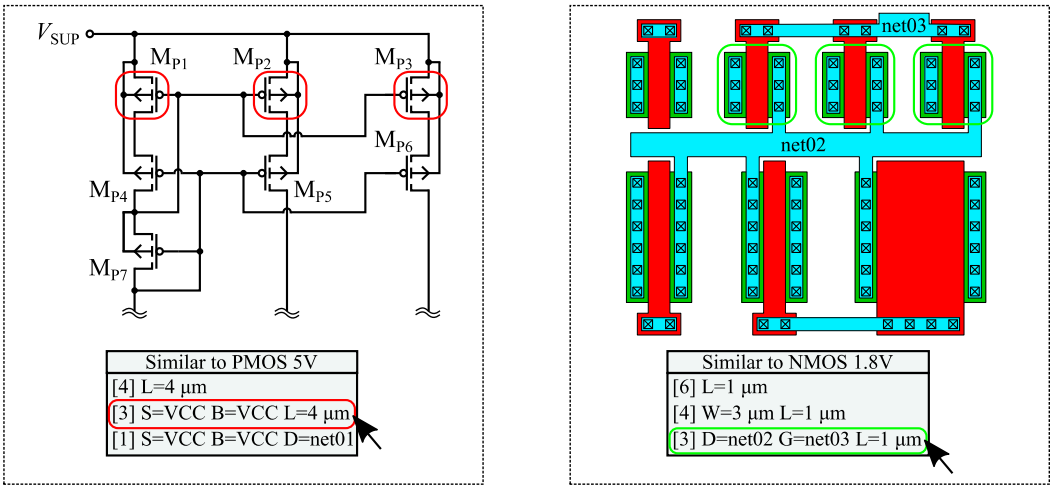
Fig. 7.4. Gesture control mapped to the incremental interface tested with the 3D tracking camera [16].

The Incremental Control is a new control concept which is very intuitive and simplifies interaction with the IC CAD environment. The Incremental Control is implemented in Cadence Virtuoso to be used for modification of layout objects such as wires, pins, labels, vias, rectangles, MOSFETs and capacitors. Main applied ideas are typing removal and incremental approach. Using the Incremental Control, the

productivity of analog layout creation has been improved in the range of 23% to 66%. Moreover, this type of interaction seems to be more native to all backend designers who use it. By using gesture control camera mapped to Incremental Control bindkeys, layout objects have been changed. Based on our experience, the gesture tracking device needs an additional improvement of precision [15].

7.2. Similar Search

During the creation of analog layout in Cadence Virtuoso environment, layout engineers spend a lot of time by selecting objects in a database. By applying new "Similar Search" concept for search and select control and targeting modern control approaches, the Similar search solution Fig. 7.5 unifies and simplifies search control of any CAD object to speed-up the work.



(a) (b)

Fig. 7.5. Similar search control in Cadence Virtuoso environment (a) in the schematic editor, (b) in layout editor [129].

Discussed new control technique is compatible with Cadence Virtuoso environment, both schematic and layout editor.

This innovative control concept offers a form-less interface for faster search and removes the need to type. Layout engineers experienced with the new control concept prefer this new flow to the classic one as object search, and select procedure has been simplified. Time needed to select relevant instances is measured for different designs is in Tab. 7.2

Tab. 7.2. Layout productivity measurement results [17]

Design	**Num. of instances [-]**	t_{man} **[s]**	t_{script} **[s]**	t_{man} / t_{script} **[-]**	(t_{script} - t_{man}) / t_{man} **[%]**
Cascoded mirror (schematic)	17	49.6	7.0	7.1	-85.9%
Cascoded mirror (layout)	73	76.0	6.1	12.5	-92.0%
Digital decoder (schematic)	14	20.3	4.9	4.1	-75.9%
Digital decoder (layout)	18	22.4	5.2	4.3	-76.8%

Where t_{man} is a time of manual selection and t_{script} is a time of selection with similar search script. The control concept is very intuitive and improves the productivity of analog layout search and select technique. Time saving is in the range of 76 % to 92 %. The highest level of efficiency is mainly achieved in very complex circuits. [17]

7.3. Smart Placement & Sorting

Addition innovation is an evolution of previously mention the invention of Similar Search where there have been replacing, time consuming, need of a selection of different type of reference devices in the database and now tool can do sorting base on electrical or geometrical properties on whole or patronal database at once.

A new pre-placement phase of integrated circuits (IC) analog-mixed-signal (AMS) physical design flow, automatically sorts electrical devices used in planar IC technologies according to their topological, structural and electrical properties. The presented design phase replaces human labor and allows to save design time and prevent human mistakes. A flow chart describing the pre-placement implementation is shown in Fig. 7.6 and is described in [13].

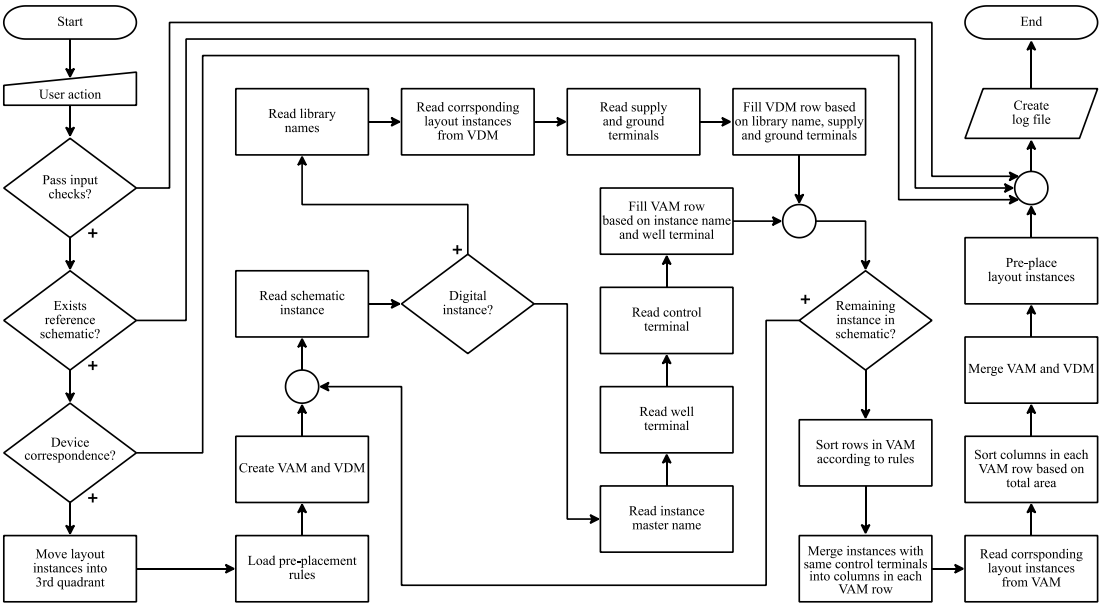


Fig. 7.6. Flow chart of the automatized pre-placement phase [13].

A software implementation of the proposed method works with virtual objects of layout instances which are moved only once at the end of the script when creating the final pre-placement matrix. Algorithm complexity is decreased by a new way of virtual objects matrix indexing. The automatic pre-placement phase has been used during the design of AMS circuits in 160 nm BCD8sP and SOIBCD8s technologies from STMicroelectronics and has been faster in the range of 3 000to 20 000 times compared to manual sorting as it is present in Tab. 7.3. Where the number of layout instances is N_{LI}, the number of rows is N_{ROW}, number of non-empty elements N_{NE}. For quantification of layout productivity increase, time of manual standard sorting t_{MS} and time of automatic preplacement phase t_{PP} to reach the final sorted matrix are introduced. The time saving between manual sorting and automatic pre-placement is described as a relative ratio ρ, estimated relative ratio ρ_{E}, relative difference of ρ and ρ_{E} is d_{R}

The estimation of the ratio between manual sorting time and automatic pre-placement time shows a growing time saving with increasing circuit complexity compared to standard layout flow. The introduced enhanced layout flow is able to prevent creation of hardly detectable errors occurring at the beginning of AMS physical design, especially the wrong bulk connection errors of semiconductor devices.

Tab. 7.3. Layout productivity measurement results [13].

Type of circuit	N_{LI} [-]	N_{ROW} [-]	N_{NE} [-]	t_{MS} [s]	t_{PP} [s]	ρ [-]	ρ_E [-]	d_R [%]
Comparator	29	4	11	110	0.028	3929	3471	-11.66
Comparator with hysteresis	32	6	13	155	0.038	4079	4288	5.13
Signal clamper	40	9	17	246	0.032	7688	5754	-25.15
Operational amplifier	52	7	16	249	0.065	3831	4330	13.03
Supply selector	66	6	17	167	0.047	3553	4060	14.26
Over voltage protection	78	8	15	174	0.055	3164	2930	-7.4
Rail-to-rail input comparator	94	4	23	431	0.106	4066	5266	29.52
Zero crossing detector	99	6	20	362	0.068	5324	4019	-24.52
Error amplifier	112	9	19	299	0.092	3250	3384	4.12
Trimm Operational amplifier-	112	8	26	572	0.117	4889	5724	17.08
Low drop out regulator	122	40	57	2280	0.089	25618	20099	-21.54
Soft start	129	7	25	390	0.098	3980	4858	22.05
Over current protection	197	13	32	746	0.143	5217	5470	4.85
Programmable comparator	213	15	33	742	0.173	4289	5455	27.18
Fast comparator	324	9	28	677	0.196	3454	3092	-10.48
Current reference	358	44	79	3420	0.199	17186	16407	-4.53

The automatic pre-placement phase saves hours of reworks and speeds up the entire design process [13].

7.4. Conclusion for Development of Design Methodology

During the creation of analog layout in power IC in Cadence, CAD environment layout engineers spend a lot of time by modifying objects in a database. By applying new control concept and targeting modern control approaches proposed solution unifies and simplifies control of any layout object to speed-up work. The control concept is very intuitive and time saving is in the range of 23% to 66%. There is evident that higher efficiency is reached when different objects are modified simultaneously.

In the process of creation of analog layout in power IC in CAD environment, the layout engineers spend a lot of time by selecting objects in a database. By applying new “Similar Search” concept for search and select control and targeting modern control approaches, the Similar search solution unifies and simplifies search control of any CAD object to speed-up the work. The control concept is very intuitive and improves the productivity of analog layout search and select technique. Time saving

is in the range of 76 % to 92 %. The highest level of efficiency is mainly achieved in very complex circuits.

A new pre-placement phase of integrated circuits analog-mixed-signal (AMS) physical design flow, automatically sorts electrical devices used in power IC technologies according to their topological, structural and electrical properties. The presented design phase replaces human labor and allows to save design time and prevent human mistakes. The automatic pre-placement phase has been used during the design of AMS circuits in 160 nm BCD8sP and SOIBCD8s STMicroelectronics processes and it has been faster in the range of 3 000 to 20 000 times compared to manual sorting.

7.5. Possible Future Development of Design Methodology

The partial or full automatization of AMS physical implementation flow is actual but also challenging topic for each semiconductor CAD vendors and their users.

Seems to be by promising to apply proposed automatic pre-placement phase [13] into constraints for automatic placers. Where main advantage is coming from the reduction of device count, substituted by pocket count. It will significantly reduce the number of combination and simplify to find optimal floorplan.

For additional improvement of AMS physical implementation flow will need to overcome the limitations of the current algorithm and use of Machine Learning (ML) is most promising.

8. Conclusion

The most important parameter of power MOSFETs devices is specific on- resistance, which plays a critical role in both trends of modern electronics: miniaturization and efficiency improvement, respectively. The main qualitative parameter used for optimization of power MOSFETs is Area Increment *AI*. It is a relative difference of specific on-resistances between compared topologies.

The effective *W/L* channel ratio of cross element in Waffle MOS is 0.55871 with tolerance 10^{-5}. It is much precise value than 0.55 described by Saqib [66]. It is useful to use waffle gate pattern in case, when the gate length d_1 is smaller than 2.26 times a spacing between polysilicon gates d_5. In opposite case, when polysilicon width d_1 is 2.26 times larger than the spacing between polysilicon d_5 then waffle gate pattern in term of resistance per area is worse than standard gate pattern with fingers.

To achieve a high reliability of power MOSFETs transistors the bulk connection have to be robustly connected. This lead to power MOSFETs segmentation and it influenced the specific on-resistance parameter. In this work two MOSFET topologies with waffle gate with a diagonal and orthogonal source and drain interconnections has been described for the first time. Moreover, its new analytic models have been describe. It also allows to descibre non-square shapes of power MOSFETs compare to Vemuru [68].

The MOSFET structure with waffle gates with orthogonal source and drain interconnections has been described, and its analytic model of channel area has been the first time proposed. In addition, orthogonal source and drain interconnections are much more simple in comparison to orthogonal topology proposed by Madhyastha [69], where an orthogonal source and drain interconnection have metallization more complex and has a weak electro-migration limit.

In additional, the analytic models of effective width to length channel ratio have been compared by numerical 2D FEM simulation. Here, the good match has been observed between analytical and numerical models with differences less than 2 % for both waffle structures.

Moreover, this thesis confirms that models considering core area elements only [66] are not sufficient precise for the exact description of power MOSFETs with segmentation, and therefore in this work the new more precise models are presented.

There has been compared the example of MOSFET topology with waffle gate pattern with diagonal source and drain interconnections and the standard MOSFET with finger gates with the condition of the same on-resistance. The result of it is that the waffle gate pattern with diagonal source and drain interconnections occupies 42.38 % less area than the standard one.

Similarly, the second example of MOSFET topology with waffle gate with an orthogonal source and drain interconnections occupies 22.43 % less area compared to the standard MOSFET with finger gates with the condition of the same on-resistance.

Moreover, there has been defined conditions where the segmented power MOSFETs structures with waffle gates occupy less area than the standard MOSFETs with finger gates with same channel resistance.

In power IC, it has been presented 19 % area saving of power 5V MOSFET in 160nm BCD8sp process by using waffle power MOSFET with orthogonal source and drain interconnections.

To improve the channel resistance of HV power GaN HEMT the new topologies have been proposed and described. The specific on-resistance can be reduced by using proposed new power GaN HEMT topologies with dissimilar square waffle pattern [11] and with octagon waffle pattern [10]. The area saving compared to standard finger gate pattern is up to 40 % depending on contact shape and pattern. In addition production cost of GaN HEMT can be reduced by decreasing chip area and by it yield improvement. The standard waffle gate pattern and proposed two new gate patterns the dissimilar square waffle and octagon waffle pattern can apply for any lateral normally-On or normally-Off GaN HEMT processes. New proposals are lateral structures and due to this are perspectives for integration into power management integrated circuits on GaN substrates. Shape and pattern of contacts (rectangle, square, square with chamfer or circle) influence on-resistance of new GaN HEMT. The square shape of contacts placed in the waffle pattern can reach more than 40 % area reduction for $C_S/C_D < 0.3$ and 16.1 % reduction for contacts spacing C_S same as contact dimension C_D what is the best Area Increment *AI* performance improvement compared to other contact shapes in waffle patterns. In opposite, the circle shape of contacts placed in the waffle pattern can reach up to 6.9 % area reduction for $C_S/C_D < 0.5$ and

1.2 % area reduction for $C_S/C_D = 1$ compare to finger topology what is lowest *AI* performance improvement compare to another contact shape. The higher chamfer on square contacts leads to a decrease of *AI* performance. Pattern with square and circle contacts reach up to 21% area reduction for $C_S/C_D < 0.3$ and 10.3 % area reduction for $C_S/C_D = 1$ compare to finger topology what is better *AI* compare to square contacts with 58% chamfer where has been reach up to 16.6 % area reduction for $C_S/C_D < 0.3$ and 6.1 % area reduction for $C_S/C_D = 1$.

For the higher drain to gate BV of GaN HEMT, the square shape drain contact with higher chamfer or circle shape is more suitable. In general, for the same on-resistance the area can be reduced for: waffle gate pattern, new dissimilar square waffle gate pattern or octagon waffle gate pattern if contacts dimension C_D is 1.1 times larger than contacts spacing C_S.

During the creation of analog layout in power IC in Cadence, CAD environment layout engineers spend a lot of time by modifying objects in a database. By applying new control concept and targeting modern control approaches proposed solution unifies and simplifies control of any layout object to speed-up work. The control concept is very intuitive and time saving is in the range of 23% to 66%. There is evident that higher efficiency is reached when different objects are modified simultaneously.

In the process of creation of analog layout in power IC in CAD environment, the layout engineers spend a lot of time by selecting objects in a database. By applying new “Similar Search” concept for search and select control and targeting modern control approaches, the Similar search solution unifies and simplifies search control of any CAD object to speed-up the work. The control concept is very intuitive and improves the productivity of analog layout search and select technique. Time saving is in the range of 76 % to 92 %. The highest level of efficiency is mainly achieved in very complex circuits.

A new pre-placement phase of integrated circuits analog-mixed-signal (AMS) physical design flow, automatically sorts electrical devices used in power IC technologies according to their topological, structural and electrical properties. The presented design phase replaces human labor and allows to save design time and prevent human mistakes. The automatic pre-placement phase has been used during the design of AMS circuits in 160 nm BCD8sP and SOIBCD8s STMicroelectronics

processes and it has been faster in the range of 3 000 to 20 000 times compared to manual sorting.

The results of this doctoral thesis are summarized in section 1.3 and come from the development, which has been supported by the Grant Agency of the Czech Technical University in Prague, grant No. SGS17/188/OHK3/3T/13 (Mikro a nanostruktury a součástky), grant No. SGS14/195/OHK3/3T/13 (MiNa), grant No. SGS11/156/OHK3 /3T/13, the GACR project No. 02/09/160, and Ministry of the Interior grant No. VG20102015015. Parts of this thesis have been developed in cooperation with companies ST-Ericsson and STMicroelectronics. Fabrication of proposed GaN HEMT has been realized with the cooperation of Slovak Academy of Science (SAS).

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Appendix A: List of Author's Publications

A.1 Publications Related to the Topic of This Work

A.1.1 Publications in Impacted Journals

P. Vacula, V. Kotě, D. Barri, M. Vacula, M. Husák, and J. Jakovenko, "Comparison of MOSFET Gate Waffle Patterns Based on Specific On-Resistance.", Radioengineering, 2019. (In the Review Process). Co-authorship: 55 %

V. Kotě, A. Kubačák, P. Vacula, J. Jakovenko, and M. Husák, "Automated pre-placement phase as a part of robust analog-mixed signal physical design flow," Integration, the VLSI Journal, 2018, vol 63. Co-authorship: 30 %

D.Barri, P. Vacula, V. Kotě, J. Jakovenko, and J. Voves, "Improvements in the Electrical Performance of IC MOSFET Components by Using Diamond Layout Style vs. Traditional Rectangular Layout Style Calculated by Conformal Mapping", Microelectronic Engineering 2019, (In the Review Process) Co-authorship: 20 %

A.1.2 Patents

P. Vacula, M. Vacula, V. Kotě, A. Kubačák, and M. Lzicar, "Transistors with dissimilar square waffle gate patterns", US20180342594, 2018, Co-authorship: 50 %

P. Vacula, M. Vacula, and M. Husák, "Transistors with octagon waffle gate patterns", US20180342504, 2018, Co-authorship: 33 %

A.1.3 Publications in Reviewed Journals

P. Vacula, and M. Husák, "Comparison of Waffle and standard gate pattern base on specific on-resistance.", ElectroScope [online]. 2014, vol. 2014, no. VIII, ISSN 1802-4564. , Co-authorship: 95 %

P. Vacula, and M. Husák, "Waffle MOS channel aspect ratio calculation with Schwarz-Christoffel transformation.", ElectroScope [online]. 2013, vol. 2013, no. VII, ISSN 1802-4564, Co-authorship: 95 %

P. Vacula, V. Kotě, A. Kubačák, M. Lzicar, R. Zeleny, M. Husák, and J. Jakovenko, “Incremental control techniques for layout modification of integrated circuits,” Advances in Science, Technology and Engineering Systems Journal, vol. 2, no. 3, pp. 1196–1201, 2017. Co-authorship: 40 %

A.1.4 Publications Excerpted by WoS

P. Vacula, V. Kotě, A. Kubačák, M. Lzicar, R. Zeleny, M. Husák, and J. Jakovenko,. “Incremental control techniques for layout modification in 11th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM), Smolenice, Slovakia, 2016, pp. 239–242.. ISBN 978-1-5090-3081-1. , Co-authorship: 40 %

A.1.5 Other Publications

P. Vacula, V. Kotě, and D. Barri, “Trench MOS Having Source with Waffle Patterns,” in Proceedings of the International Student Scientific Conference Poster 22/2018, Prague, Czech Republic, 2018, pp. 1–5, Co-authorship: 60 %

P. Vacula, “Simple DC electrical model of Asymmetric Waffle MOS.” In Proceedings of the 18th International Scientific Student Conference Poster 2014. Prague, Czech Republic, 2014, vol. 1, section EI – Paper Nr. EI55. ISBN 978-80-01-05499-4. , Co-authorship: 100 %

P. Vacula, M. Husák, “Comparison of different Waffle MOS topologies base on dimensions and channel resistance.” In Proceedings of Electronic Devices and Systems EDS 2014. Brno, Czech Republic, 2014, vol. 1, p. 25-31. ISBN 978-80-214-4985-5, Co-authorship: 95 %

P. Vacula, V. Michal, T. Matthieu, M. Husák, “Waffle MOS channel W/L calculation with Schwarz-Christoffel transformation.” In Proceedings of Electronic Devices and Systems EDS 2013. Brno, Czech Republic, 2013, vol. 1, p. 172-177. ISBN 978-80-214-4754-7, Co-authorship: 80 %

P. Vacula, V. Kotě, A. Kubačák, S. Cliquennois, M. Lzicar, M. Husák, and J. Jakovenko, “Modern search techniques for layout creation in CDNLive Cadence User Conference EMEA 2017, Munich, Germany 2017, Co-authorship: 43 %

P. Vančura, V. Kotě, P. Vacula, A. Kubačák, and J. Jakovenko, “Matched Structures Classification” in CDNLive Cadence User Conference EMEA 2017, Munich, Germany, 2017, Co-authorship:17 %

P. Vacula, V. Kotě, A. Kubačák, M. Lzicar, R. Zeleny, M. Husák, and J. Jakovenko,. “Modern Control Techniques for Layout Creation” in CDNLive Cadence User Conference EMEA 2016, Munich, Germany, 2016 , Co-authorship: 40 %

A.2 Publications Not Related to the Topic of This Work

A.2.1 Publications in Impacted Journals

V. Kotě, P. Vacula, V. Molata, O. Veselý, O. Tláskal, D. Barri, J. Jakovenko, and M. Husák, "A true random number generator with time multiplexed sources of randomness," Radioengineering, 2018, vol. 27, no. 3. Co-authorship: 15 %

A.2.2 Patents

P. Vacula, M.Vacula, and M. Lzicar, "Flexible layout for integrated mask-programmable logic.", EP 2996248 A3,2007, Co-authorship: 70%

P. Vacula, M. Vacula, and M. Lzicar, "Integrated mask-programmable logic devices with multiple", US 8134187 B2, 2012, Co-authorship: 70 %

A.2.3 Other Publications

V. Kotě, V. Molata, and P. Vacula, "Behavioral models of true random number generators," in Proceedings of the International Student Scientific Conference Poster – 22/2018, Prague, Czech Republic, 2018, pp. 1–6, Co-authorship: 20 %

T. Matthieu, P. Vacula, J. Jakovenko, "Design and validation of an SMPS distribution network.", In Proceedings of Electronic Devices and Systems EDS 2012. Brno: VUT Brno, FEKT, Czech Republic, 2012, vol. 1, p. 60-65. ISBN 978-80-214-4539-0, Co-authorship: 10 %

Appendix B: Recognition

Best Ph.D Oral Presentation Award, for the work “Waffle MOS channel W/L calculation with Schwarz-Christoffel transformation.”, IMAPS Electronic Devices and Systems International Conference 2013,. Brno, Czech Republic, 2013

Certificate of Participation for the contribution “Modern Search Techniques for Layout Creation.” CDNLive Cadence User Conference EMEA 2017. Munich, Germany, May 15–17, 2017