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Doctoral Thesis

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RADIATION TOLERANT POWER ELECTRONICS FOR SPACE APPLICATIONS

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Supervisor-Specialist: ***Dr. Pavel M. Trávníček***

Declaration

Hereby, I declare, that this Doctoral Thesis is based at all my own work and I have cited all sources I have used in the bibliography.

In Prague, November 25th, 2018

Prohlašuji, že jsem předloženou disertační práci vypracoval samostatně a že jsem uvedl veškerou použitou literaturu.

V Praze, 25. 11. 2018

……....……..

Jaroslav Laifr

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Abstract:

The aim of this thesis is to summarize the state-of-the-art satellite electronics design, find its bottlenecks and propose a novel, scientific-based approaches on the space power systems development addressing rapidly evolving so-called *"NewSpace"* ecosystem.

The modern consumer-driven electronics with rising computational power and miniaturization demands similar to the *Moore's Law* for computers brings new technological challenges and problems. The *NewSpace community* needs to understand them to successfully conduct its presence in space, both aboard earth-orbiting and interplanetary missions. It is the satellite (manned and unmanned) and aerospace industry, private or government-led institutions which need to follow the technological and scientific progress by faster steps if want to utilize the full potential of the scientific and technological progress in commercially available markets and technological breakthroughs.

Initial studies are the follow-up of the author's Master thesis: *Fluxgate Magnetometer for Satellite Attitude Control*, carried on within the multi-faculty *CubeSat project CzechTechSat* led by the author as the Principal Investigator. Students were implementing authors' hypotheses within their bachelor and master thesis terms and supported their research and validation.

Key findings were implemented as an practical example of the thesis utilization within the *Low Voltage Power Supply* unit for the *Radio and Plasma Waves Investigation* instrument selected to be flown aboard the *European Space Agency L-Class* mission called *JUICE* (*Jupiter Icy Moon Explorer*) into the Jovian system in 2023. Also in the project *CRREAT* by the realization of the ultra low power dosimeter for small satellites.

The thesis is also a base of the spacecraft electronics design E-Book called "*NewSpace Economically"* prepared to be released to the small satellite community in 2019.

Keywords: *ESA, RPWI, JUICE, CubeSat, NewSpace, Radiation, Power Supply, Satellite*

Abstrakt:

Cílem výzkumu v předložené disertační práci je shrnout dosud používané návrhy elektroniky vesmírných družic, poukázat na kritické body a rizika s tím spojená a navrhnout postupy založené na vědeckém bázi, beroucí do úvahy konzervativnost spojenou s neochotou ke změnám v uvažování nad návrhem kosmických systémů výkonové elektroniky. Nedílnou součástí nového přístupu je i snížení celkových nákladů (energetických i materiálních) s přihlédnutím k modernímu, tzv. "*NewSpace*" ekosystému.

Rychle se vyvíjející trh se spotřební elektronikou se svými rostoucími nároky na výkon a miniaturizaci, podobně jako *Moorův zákon* ve vývoji výkonu počítačů, přináší nové poznatky a problémy, které *NewSpace* komunita musí plně pochopit, pokud chce bezpečně působit ve vesmírném prostoru, a to jak na oběžné dráze Země, tak při meziplanetárních misích. Je to převážně kosmický (pilotovaný i nepilotovaný) a letecký průmysl, soukromé i vládní agentury, kteří musí vyvinout veliké úsilí, aby udržely krok s technologickým vývojem a průlomovými výsledky v komerční sféře a využily tak její plný potenciál.

Úvodní studium problematiky vychází z autorovy diplomové práce na téma *Magnetometr pro řízení polohy satelitu*, následované multifakultním projektem nanosatelitu *CzechTechSat* jehož je hlavním řešitelem. Studenti pod vedením autora práce implementovali navrhované hypotézy v rámci svých bakalářských a diplomových prací a pomáhali tak k jejich realizaci a ověření.

Klíčové prvky práce byly poté implementovány jako praktická ukázka využitelnosti v rámci projektu *ESA-Lunar Lander/L-DEPP/LPM* a nízkonapěťového napájecího zdroje přístrojového balíku pro studium radiových a plazmových vln *(RPWI)*, vybraného pro let na misi evropské kosmické agentury *ES*A s názvem *JUICE*. V rámci něj byl také vyvinut speciální systém potlačování rozběhových proudů pro vesmírné aplikace. Plánované vypuštění sondy do vesmíru je stanoveno na rok 2023. Dále v projektu *CRREAT* realizací nízkopříkonového širokospektrálního dozimetru pro malé satelity.

Práce je rovněž základem pro připravovanou elektronickou publikaci (*E-Book*) pro vývojáře elektronických systémů malých družic s názvem *"NewSpace ekonomicky"*, připravovaná k distribuci v roce 2019.

Klíčová slova: *ESA, RPWI, JUICE, CubeSat, NewSpace, radiace, napájecí zdroj, kosmická sonda*

Table of Contents

Acronym	Definition
ADC	Analog-to-Digital Converter
CBK PAN	Centrum Badań Kosmicznych Polskiej Akademii Nauk
CRC	Cyclic Redundancy Check
CRREAT	Research Center of Cosmic Rays and Radiation Events in the Atmosphere
DPU	Data Processing Unit
EBOX	Electrical Box
ESA	European Space Agency
FPGA	Field Programmable Gate Array
HDR	High Dose Rate
HF	High Frequency receiver
HK	Housekeeping
JUICE	Jupiter Icy Moon Explorer
LCL	Latching Current Limiter
LDR	Low Dose Rate
LF	Low Frequency receiver
LP/MIME	Langmuir Probe / Mutual Impedance Measurement Equipment
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
LVPS	Low Voltage Power Supply
MSB	Most Significant Bit
OCP	Overcurrent (Protection)
OVP	Overvoltage (Protection)
PDU	Power Distribution Unit
PoL	Point of Load
RPW	Radio and Plasma Waves instrument, LESIA, Meudon, Paris, France
RPWI	Radio and Plasma Waves Investigation instrument, Institute for Space Physics, Uppsala, Sweden
SCM	Search Coil Magnetometer
SCR	Silicon Controlled Rectifier (Thyristor)
SEB	Singe Event Burnout
SEE	Single Event Effect
SEL	Single Event Latchup
SPF-Free	Single Point of Failure Free Design
TC	Telecommand
TID	Total Ionizing Dose
TM	Telemetry
TM/TC	Telemetry/Telecommand
UART	Universal Asynchronous Receiver/Transmitter
UVLO	Undervoltage Lockout
XNOR	Negative Exclusive OR

1. Introduction

In the past decade a dramatic rise of small satellites, *CubeSats*, *PocketQubes* and microsatellites shown that the conservative approach of building space electronics is no longer in line with the technological progress in commercial electronics. Moreover, it turned out, that even commercially available parts are able to withstand the environment of space (vacuum, radiation, thermal cycling) for at least long enough time to fulfill short mission needs, if properly used. The new era of space exploration, such as first CubeSats for deep space flight to Mars (*MarCO-A, MarCO-B*, [R-23]) is known as the "*NewSpace*". To maximize the yield of the NewSpace age, this Thesis shall help the designers, mission owners and operators and scientific community to implement techniques to prolong the operational lifetime.

The semiconductor die layout, physical chip properties, materials, mechanical housing, shielding, adhesives or coating are the facts which could determine the electronic system failure rate, reliability and lifetime. The Thesis summarizes ideas, principles and already performed research of circuit design, component selection, software features, data protection, system concepts considerations, practical realization and test results.

Proposed approaches were applied in two *Czech Ministry of Education, Youth, and Sports* grant supported scientific instruments under the *ESA PRODEX* programme and two university and public-funded projects. Namely the *ESA / JUpiter ICy moon Explorer (JUICE)* / Radio and Plasma Waves Investigation (*RPWI*) / Low Voltage Power Supply (*LVPS*), the ESA / Lunar Lander / Lunar Dusty Environment and Plasma Package (*L-DEPP*) – Definition Study / Lunar Plasma Monitor (*LPM*), the *CzechTechSat – The Experimental University Picosatellite Platform* and *CRREAT*. Electrical system topologies and concepts are all focused to be able to withstand the operations within the harsh and condition-critical environments following the initial work developed during the Master Thesis, *Fluxgate Magnetometer for Satellite Attitude Control.*

1.1.Ionizing Radiation Impact on Semiconductors

The behavior of discrete semiconductors influenced by the different radiation sources such as particle or photonic irradiation causing ionizing damage, non-ionizing changes or single event effects during the biased operations were studied and summarized in [PP-3]. The paper gives an overview of the key parameters showing most significant changes with respect to accumulated radiation dose in PN junction, *BJT, JFET/MESFET, MOSFET, CMOS, IGBT, HEMT and SiC* components.

The space radiation influence on electronic systems depends strongly on the orbital altitude and inclination. It is therefore a different task to design a satellite system in the case of the deep space flight.

There are several, scientific community-accepted, software platforms to perform the expected radiation estimations such as the *CREME96 [R-1], SPENVIS [R-2] or SPIS [R-3]*. For the simulation of shielding properties the *GEANT4 [R-4]* or *SHIELDOSE* (part of the *SPENVIS*) tools are often used. To study the particle interaction with matter on semiconductor level, the *SRIM* [R-5] software can be employed. However, in the case of space mission the calculation is often done by payload study team, launch provider or a mission specialist and announced at the project kick-off as a one of the most important design drivers. The ESA convention is to apply a margin of hundred percents on finally identified dose. In the case of *JUICE/LVPS* the targeted Total Ionizing Dose (TID) has been determined to be *50 krads(Si)*, Therefore whole design shall withstand at least *100 krad(Si)*.

2. State of the Art Space-Grade Power Electronics

2.1. Components for Space-Grade Power Supplies

The radiation hardened portfolio of components intended for current or voltage mode space-grade power supplies and power electronics such as motor controllers or H-bridges is quite broad on the international market, mostly with vendors located in USA, EU, UK and Japan. The offer includes complete discrete components portfolio such as bipolar transistors, *BJT arrays, MOSFET transistors, JFETs, rectifiers, Schottky diodes, Zener diodes or voltage references*. Integrated circuits such as *PWM controllers, voltage references and TTL or CMOS logic families* are available as well, however with much variable total ionizing dose (TID) tolerance with respect to discrete parts, due to the high integration complexity.

The following breakdown list of basic electronic parts represents DISCUSSION ***(D:)*** of typical EEE part categories and their sensitivity to harsh environment of space with author's RECOMMENDATION ***(R:)*** about its key parameters to observe and pay attention to during the system design phase based on seven years long research period at the CTU FEE.

2.1.1. Resistors

D: Surface mounted, through hole or screw "wing" mounted shunt resistors are naturally insensitive to radiation in space. Variations and parametric drifts may be observable at extremely high doses (more than hundreds of MRads) due to physical destruction of the resistive material structure. However, such high doses could be omitted from robustness improvement consideration, as the accompanied semiconductors are typically already fully out of the operational range and shows no functionality.

Conventional ceramic resistor package disintegration or microscopic cracking may arise due to excessive thermal cycling and different thermal expansion coefficients with respect to the PCB. Typical unit temperature cycling during the dusk and dawn cycle when orbiting the Earth, other planet or self tumbling could be expected with reasonably low dT/dt, due to the hardware thermal capacity. Resistor package is then tempered well in line with the temperature of the target system via solder joints and thermal transfer from the PCB or unit frame, in case of wing mounted resistors.

R: Mounting the SMD rectangular package with elevated height above the PCB using so-called tin standoff (0.2 - 1 mm) increases the amount of metallic material in series with resistor body to spread the total thermal expansion stress.

Special case is the electronic system immersed directly into space, such as antenna or sensor preamplifier. The active thermal control heating elements in combination with encapsulation under the coverage of the *Multi Layer Insulation (MLI)* are then necessary to consider to stabilize the temperature range and average-out excessive thermal loading range.

Fig. 1 Multilayer Insulation example as a protective layer for spacecraft sensor (left), the composition of temperature insulating layers of the MLI (right), [I-1].

D: Much dangerous operational condition from thermal stress and mechanical rupture point of view occurs when the power to dissipate is changing as a step load. Over-dimensioning of the total power loss allowed in package shall be considered at least 200% or more of nominal power. The goal is to maximize the thermal conductivity according to 2.1.1 below

$$\frac{1}{R_\theta} = \frac{Q \cdot l_{path}}{A_{surface}(T_{element} - T_{ambient})}, \tag{2.1.1}$$

where R_θ is thermal resistivity of the conductive surface Q is the amount of heat per unit time, l_{path} represents the length of the heat transfer path, $A_{surface}$ is the heat transfer cross-section and T represents temperatures of the heating element and ambient environment respectively. When considering the real environment, a total sum of at least three components have to be taken into account: 1) the thermal resistivity of the resistive element body dissipating heat, 2) thermal resistivity of pins, legs or conductive strap or wire of the component, the mounting material such as tin/lead compound and finally 3) the thermal properties of the PCB itself.

R: Where possible, in case of SMD type of component, reverse packaging size with longer pads and shorter sides for better thermal conductivity is recommended to maximize the natural thermal transfer area, thus increasing the thermal conductivity.

Fig. 2 Example of the improved heat dissipation performance using reversed package, [I-2].

Flat thermal filler such as *Mica* or *CHO-THERM®* [R-6] would be used for wing-mounted packages and high power shunts. A droplet of thermally conductive epoxy glue would be utilized for THT/axially leaded resistors to fix them in position and to support the thermal runaway with good galvanic insulation.

Overvoltage stress condition could be encountered in high voltage circuits with excessive voltage peaks, such as in inductive load cases (relays, motors, filter inductor dampers, etc.). It is then necessary to check the voltage strength of the conformal coating to prevent coronal short-circuits. In the place where high voltage, high power resistor is assumed to be placed, the reverse packaging is wise to re-consider to increase the distance between electrodes, or to employ two or more resistors in series with adequately less resistance with respect to their amount to split the power dissipation and voltage stress over bigger/longer area/distance, respectively.

Except the coronal arcing short-circuits, resistors often results in open-circuit state due to fast excessive surge current applied such as from the inductive load. Where necessary such as in case of the feedback loop of the *PID* error amplifier, the ladder of four resistors of the same value would be used in configuration 2-in-parallel in series with 2-in-parallel. Then, when single resistor is opened by failure, the total resistance of the ladder increases by factor of 50 %. In case of short of one of resistors, the total resistance fall by a factor of 50%, which could still maintain the circuit in operational range with no fatal change of behavior as it would result in single component case (opened, or short).

2.1.2. Capacitors

D: There are several types of capacitors used in space electronics, with exception of commercial electrolytic and non-hermetic capacitors known mostly from PC power supplies and general electrical appliances for home and office use. The commercial production of *low ESR* capacitors with electrolytic filling has been mastered to deliver components with high surge current capability and very high capacity in limited volume. However, under conditions of vacuum, such components evaporate their dielectrics into open space quickly through their rubber feedthroughs and are unable to work without any hermetization. It is clear, that for the square wave filtering in space-grade rectifiers, the commercial electrolytic capacitor portfolio is not available and have to be replaced by different technology. From reliability point of view, the use of electrolytic capacitor encapsulated in hybrid package is still very risky to use.

The radiation damage again could be omitted from consideration due to the natural radiation insensitivity up to extremely high radiation dose levels destructing the physical properties of the capacitor material.

Mostly multilayer capacitors (*MLCC*) in SMD packages are used for low and medium range of capacitance (pF to μF). Highly stable capacitors known as the *Type-I* could be found in the range of picofarads up to several tens of nanofarads. They are mostly used for timing circuits or very high frequency operations due to their dielectrics thermal and applied voltage stability similar to *NP0* (*negative positive zero*). Multilayer capacitors, mostly known as the *Type-II* with high permittivity dielectrics such as X5R or X7R contains much bigger area of capacitor plates and due to the requirement to fit the same volume of the package as *Type-I*, might be considered as more susceptible to short-circuit failure.

R: The ladder configuration would be utilized to compensate one component failure, similarly as in case of resistors. The probability of short circuit failure of ceramic capacitors is generally higher than the probability of open-circuit failure of resistors due to higher amount of parallel layers in the same passive chip package volume. Soldering temperature and stress increases the failure probability, when the package is hand-soldered rather than reflow processed, bent or mechanically stressed. With machine soldering, the temperature profile is better equalized over the whole SMD capacitor body and expands its dimensions homogenously.

When high capacity storage is needed in order of tens to thousands of microfarads, mostly tantalum capacitors are utilized. Due to the physical principle of the tantalum component, the dielectric voltage strength is naturally lower than with respect to ceramic capacitors of the same size. Thus, ladder configuration of four capacitors is often employed when the target voltage is above ~20 V, which is a typical case for 28 V bus. Tantalum capacitors are also typical for their internal discharging leakage current in order of tens to hundreds of microAmps, dispersion of parameters is typical even within the manufactured batch. Thus the compensating resistor divider connected in parallel with capacitor ladder, splitting the leakage current in order of at least similar or one magnitude higher (around 1 mA, typ. across the tantalum capacitor) is recommended, to prevent overvoltage conditions.

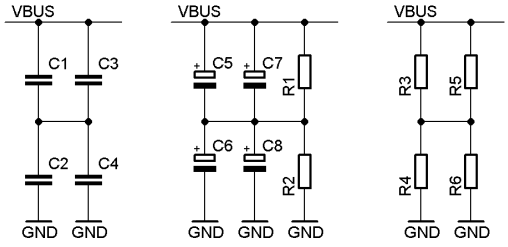


Fig. 3 Fully capacitive (left), Tantalum-Resistor and Resistor-Resistor (right) ladder schematics.

In Fig. 3 the typical configuration of three basic ladders is depicted. The fully capacitive ladder of capacitors of the same capacity *C1-C4* and rated to bus voltage is used to prevent short circuit failure in case of ceramic capacitors. Tantalum capacitor bank *C5-C8* shall be accompanied with resistive divider *R1, R2* to split equally the different leakage current causing voltage imbalance between low and high side of the capacitive chain. With no equalization, the applied voltage per capacitor may easily exceed rated limit. The *4C+2R* ladder is recommended also to prevent short circuit failure immunity, at a cost of large footprint area occupied, instead of conventionally utilized single capacitor. The total amount of tantalum capacitors is thus the design trade-off between the available footprint area and risk management.

Maximum power dissipation caused by ripple current and applied *AC* voltage have to be considered as the internal *ESR* component (mΩ up to Ω) is responsible for the thermal dissipation and may lead to overheating or thermal damage of the tantalum structure. Formula 2.1.2a describes maximum allowable *RMS* current applied to tantalum capacitors taking into account maximum power dissipation specified by manufacturer and *ESR* at given working/switching frequency. Similar approach would be studied for applied *RMS* voltage, where in 2.1.2b the Z_f is the impedance of the capacitor at given working/switching frequency.

$$I_{RMSMax} = \sqrt{\frac{P_{Max}}{ESR_f}}, \qquad V_{RMSMax} = Z_f \sqrt{\frac{P_{Max}}{ESR_f}}, \qquad \text{(2.1.2a), (2.1.2b)}$$

Furthermore, the frequency dependence of tantalum capacitor limits the target use in most of switch mode power supplies or power converter applications. It shall not be used for frequencies above approximately 100 kHz [R-7]. According to the manufacturer, as an example of the capacitors from the *AVX*, the *TAJ* family becomes inductive, when the operating frequency exceeds the resonance point (Fig.4 0.5 - 5 MHz range). Most probably because the granular conductive structure of the electrodes represents the inductive elements, which dominates over the capacitive part in mentioned tens to hundreds kHz frequency range.

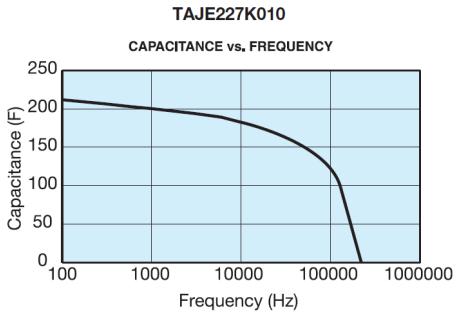


Fig. 4 An example of the capacitive drop with respect to high frequency ranges typical for DC-DC converters, [R-7].

Therefore, it is necessary to design the high frequency blocking and filtering power circuits around high capacitance ceramics with paralleling to achieve the desired capacitance or utilize damping resistors or power inductors as low pass filters in series with tantalums. The worst case requirement in terms of the circuit design is the combination of high voltage - high capacity such as input bus filters. The designer have to expect the need for high footprint area on the target PCB, which would be covered by single electrolytic capacitor in commercial electronics design.

2.1.3. Magnetics

D: Inductive components utilized in space-grade power electronics (except special scientific sensors) could be divided into: power inductors, low power pulse transformers, medium and high power transformers and RF coils/RF transformers. Whilst the RF coils are mostly custom-made in terms of size, inductance, material composition and could not be easily categorized, the key parameter is the quality of the wire enamel to prevent evaporation under the vacuum conditions or high power dissipation leading to overheating and/or enamel evaporation. Short circuit of internal turns caused by inappropriate filling chemistry may be a result of the overstressing the component by excessive current ripple or high frequency components of the current, acting as high frequency inductive heating caused by eddy currents. The correct calculation of total inductor power losses is a complex task exceeding the scope of this thesis, when taking into account core material properties such as shape, air gap, etc. However, sufficient order of magnitude precision approach would be found by equations 2.1.3a and 2.1.3b

$$P_{ConductorRMS} = I_{RMS}^2 \cdot R_{Conductor(f)}, \tag{2.1.3a}$$

where I_{RMS} represents the passing-through current, $R_{Conductor(f)}$ represents ohmic resistance of the conductor at given frequency taking into account the skin effect, and approximate estimation of the core losses

$$P_{Core} \propto k \cdot f^x \cdot \Delta B^y \cdot V_e, \tag{2.1.3b}$$

where k is the constant for core material, f^x is the frequency at frequency exponent, B is the magnetic flux with magnetic flux exponent y and V_e is the effective core volume.

R: During the selection of power inductors, a special care shall be taken on the rated frequency, as manufacturers mostly defines the operating conditions over single frequency only. Then the comparison between the conductor losses $P_{ConductorRMS}$ and inductive losses in ferrite P_{Core} have to be calculated and equalized. If the power loss due to high frequency current ripple is bigger than conductor losses, the Curie temperature of the ferrite material limits the component use and bigger package shall be selected.

The equilibrium shall be achieved between both power loss components to define the correct package, as the bigger inductor bobbin requires higher length of the copper wire and vice versa. High volume package also decreases the self resonant frequency, which could be an important design limit in case of low frequency input/output power filters by Tab.: 1.

Tab.: 1 Power magnetics optimization decision flow.

Calculation Result	Action
$P_{ConductorRMS} > P_{Core}$	Choose component rated for higher current, with wider conductor diameter or amount of conductors, to wind parallel windings in transformers.
$P_{ConductorRMS} \sim P_{Core}$	Less than a magnitude difference ~ design is optimized.
$P_{ConductorRMS} < P_{Core}$	Choose component with bigger ferrite/core material/volume.

In case of the dimensional constraints, the designer would consider to utilize the temperature heat sinking from the ferrite. Thermal filler shall be used to connect the ferrite and the PCB, if the ferrite is reachable and mounting is possible, in case the physical dimensions limits the designer to pickup bigger inductor body. When the maximum temperature is defined for the inductor, in most cases it represents the core temperature concentrated in the ferrite, not the copper wiring temperature. It is mandatory to understand, that the only efficient way of cooling the standard power inductor ferrite is through the enamel of the copper wire, to the copper wire and finally to mounting pads. The rest of thermal bridging is done via the inductor bobbin (plastic) and via thermal radiation, where both are acting as a thermal heatsink in minority. Such a small thermal bridge is difficult to identify as a potential source of overheating during the breadboarding phase of the development in laboratory, under standard atmospheric pressure acting as cooling medium.

Whilst inductors and power inductors are compact and lightweight devices in low and medium power systems, pulse transformers or power conversion transformers are wound on the bobbin with ferrite or other high permeability material in order of grams up to several tens of grams in most cases. Such highly concentrated mass mounted to the target PCB via through hole pins or SMD pads is critical with respect to rupture or destruction during the vibration and shock tests. Whilst sinusoidal or random vibrations represents the shaking of the satellite launcher, the payload fairing explosive screws represents short-term loads known as shocks. To prevent the damage by the elimination of remaining dilatation between the transformer and the target PCB, the ferrite material is recommended to epoxy glue to the PCB after soldering the wire leads, fix with low outgassing, vacuum-proof string, or fix in combination of both. Except for the wire with vacuum-proof enamel, the use of standard commercial bobbins and ferrite cores is not limited in most cases. Packages such as the EFD are used for their compact height and amount of available pins for wire leads on bobbins.

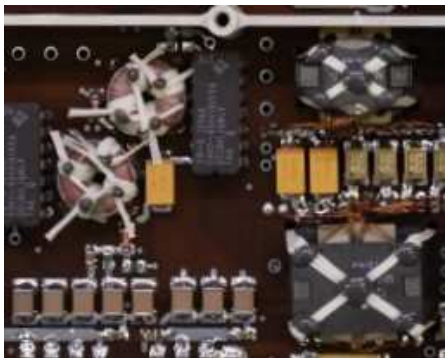


Fig. 5 An example of the ferrite-based transformer fixture using string and epoxy glue. Credits: ESA SOLAR ORBITER project, Czech Space Research Centre, ASU AVCR.

2.1.4. Rectifiers

The basic semiconductor used in power electronics is *PN* or metal-semiconductor diode, known as rectifier or Schottky diode, respectively. Whilst, standard Si-based diodes are broadly characterized in terms of mass production and use in space for many decades, Silicon-Carbide or Gallium-Nitride diodes offer new spectra of voltage, current and power ratings just recently.

D: As mentioned in [PP-3], the post-irradiation behavior of the diode is observed as increase in the forward voltage V_F and lower reverse breakdown voltage V_{BRR}. Induced impurities in the crystalline structure also prolongs the recovery time of the switching diode and increases the leakage current. A proper thermal heat sink is required to keep the rectifying diode reverse leakage current at low levels (below miliAmps). High power Schottky diodes

may show up to several tens of miliamps of the reverse leakage current after irradiation and at elevated temperature, close to operational limit of 125°C. The stabilizing effect of the forward voltage drop inversely proportional to junction temperature could be utilized, during the selection of the rectifier in the target application.

The avalanche effect resulting into permanent short circuit might occur and is known as the Single Event Burn-out [R-8]. When the low-voltage rated Schottky diode is reverse biased and hit by highly energetic particle, its depleted region is ionized and may initiate the avalanche current. Whilst, in low power switching operations such as diode logic, or low power digital signaling, the high capacity bank in rectifier represents sufficient amount of electric charge to thermally destruct the semiconductor during the surge current discharge via transformer winding, limited only by the DC resistance of the Capacitor-Diode-Transformer/Inductor current loop. The 50% or more voltage de-rating is recommended for power rectification / Schottky power diodes.

Following paragraphs are the auto citation of the part of the author's paper [PP-3], describing origins of the particle and photonic radiation damage in PN junction. It shall be considered as the baseline for understanding the radiation damage effects in more complex semiconductor structures (such as *BJTs, MOSFETs*, etc.):

"**Linear Energy Transfer (LET):**

The accelerated particles incident to the matter with atomic number $Z_{Particle}$ and transmits its kinetic energy through the Coulomb interactions to the charged particles. By this process the particle transfers its momentum to the matter and looses its velocity *v*. Amount of transmitted energy is proportional to the charge of the incident particle and to the time of interaction with atoms in the matter and is therefore inversely proportional to its speed (the slower, the more momentum can be transferred to the matter). The Bethe-Bloch formula given in (2.1.4.1) describes in detail the energy loss (linear energy transfer) of charged particles $(\alpha, \beta^{+}, p^{+})$ with respect to the penetrating depth *x*

$$LET = -\frac{dE}{dx} = nZ_{Target}\frac{4\pi e^4 Z_{Particle}^2}{m_0 v^2}B, \qquad [\text{MeV}/\mu\text{m}] \qquad (2.1.4.1)$$

where: *n* is the number of particles with atomic number Z_{Target}, *e* is a charge of the electron, m_0 is the rest mass of the electron and *B* is the "stopping number" - factor based on the atomic number of the absorber and the parameters of the incident particles (especially speed). For electrons the Bethe-Bloch formula is changed to given in (2.1.4.2)

$$LET = -\frac{dE}{dx} = nZ_{Target}\frac{4\pi e^4}{m_0 v^2}B, \qquad [\text{MeV}/\mu\text{m}] \qquad (2.1.4.2)$$

From (2.1.4.1), (2.1.4.2) follows the LET of the incident particle is not mass-dependent. Energy transfer is proportional to the square of the incident particle charge and inversely proportional to the square of velocity in the material. The result is that the particle passes its energy slowly at first and then reaches its peak with almost quadratic increase (decreased by a factor of factor velocity squared).

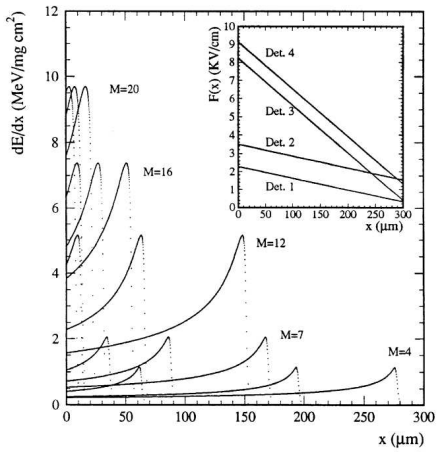


Fig. 6 Bragg curves of the LET of carbon ions passing through the silicon target [2], the parameter is the mass of the incident particle.

Once the energy transfer is finished the particle is stopped and the charge neutralized. The LET is then equal to zero. The energy loss plot given in Fig. 6 is so-called Bragg curve with a typical quadratic maximum at the end of the particle path.

When passing through the material the particle dissipate its energy by two most significant processes called electronic and nuclear stopping. The total transferred energy is then given by the sum of both processes given by (2.1.4.3)

$$LET_{Total} = \left(\frac{dE}{dx}\right)_{cores} + \left(\frac{dE}{dx}\right)_{electrons}, \quad [\text{MeV}/\mu\text{m}] \tag{2.1.4.3}$$

The electronic stopping process dominates at high incident energies (velocities). It is inelastic collision of ion with electron cloud connected with excitation or ionization (electron-hole pair generation) of the atoms of the matter. Thus the electrostatic interactions dominate. On the contrary the nuclear stopping dominates at a low energies, ie. low incident velocities or the end of the particle path in the matter. It is an elastic collision of ions with atoms and can be described by the classical kinematics – here the mechanical interactions dominate. Both processes [3] are illustrated .

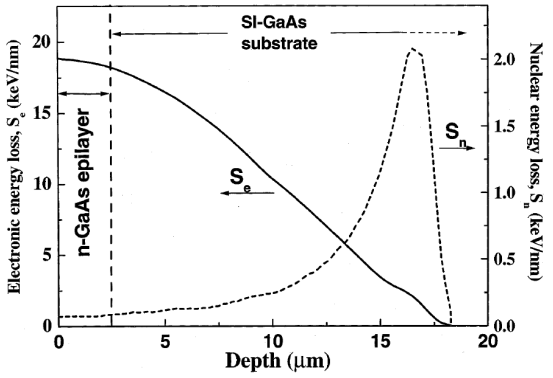


Fig. 7 Electronic (Se) and Nuclear (Sn) Stopping processes illustration [3] of 200 MeV $^{107}Ag^{14+}$ ion with respect to depth inside n-GaAs/SI-GaAs epitaxial layer.

By the energy transfer the incident particle can easily dislocate atoms of the semiconductor crystal lattice. As an example the approximate estimation of the number of dislocated nuclei after impact of the proton of energy E_{p+} into the silicon (covalent bonds of four e^-) with elastic collision can be determined from equation (4)

$$N_{Dislocated} = \frac{E_{p+}}{2E_{Dislocating(Si)}}, \qquad [-] \qquad (2.1.4.4)$$

where $2E_{Dislocating(Si)}$ is determined as an energy needed to dislocate one atom in the Si lattice (~ 15 eV). For illustrating from (4) follows that single p^+ with energy of 10 MeV (typical energy inside of the nuclear reactor) impacting the silicon matter can dislocate approximately $3{,}3 \cdot 10^5$ atoms. It is necessary to point out that during atomic dislocation primary defects occurs. They are interstitials, vacances or combination so-called Frenkel pairs. Lattice periodicity is then strongly affected. Secondary damage arise by interaction of primary defects with a crystal and with dopants in lattice, ie. V-O-H (vacancy-oxygen-hydrogen) complex or V-P (vacancy-phosphor) pair. Then previously neutral impurities become electrically active. Formation of V-O-H complex by impact of hydrogen ion is illustrated schematically in Fig. 3.

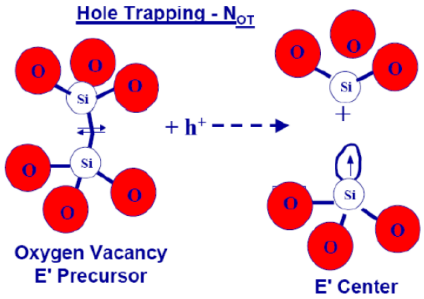


Fig. 8 Illustration of oxygen-vacancy complex formation [4].

Interaction between Electromagnetic Radiation and Matter:

At low energies the Compton scattering process dominates to energy dissipation. Photon colliding with atom transfers its energy to the increase of the kinetic energy of the particle and change also self trajectory. Scattered photon radiates energy quanta at longer wavelength by the equation (5) given below:

$$\Delta\lambda = \lambda' - \lambda = \frac{h}{m_e \cdot c}(1 - \cos\varphi), \qquad (2.1.4.5)$$

where h is Planck constant, m_e electron mass, c is speed of light and φ is an angle between previous and new velocity vector as is depicted in Fig. 9.

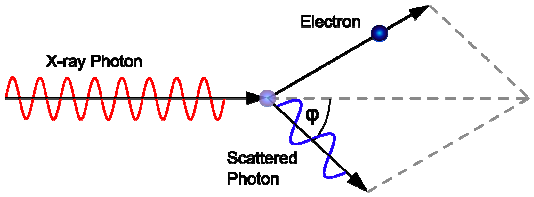


Fig. 9 Compton scattering illustration [5].

With increased energy of photon quanta the effects becomes more complex - from simple e^- excitation over the photoelectron generation up to electron-hole pair generation at (and higher than) so-called threshold level. Energy needed to produce this pair in Silicon can be determined by the equation (2.1.4.6):

$$E = \frac{2m_e \cdot c^2}{e} = \frac{2 \cdot 9{,}1 \cdot 10^{-31} \cdot c^2}{1{,}602 \cdot 10^{-19}} \doteq 1{,}022 MeV\ , \qquad (2.1.4.6)$$

As an example the photon energy absorption processes with respect to the photon energy dissipated in iron is depicted in Fig. 10.

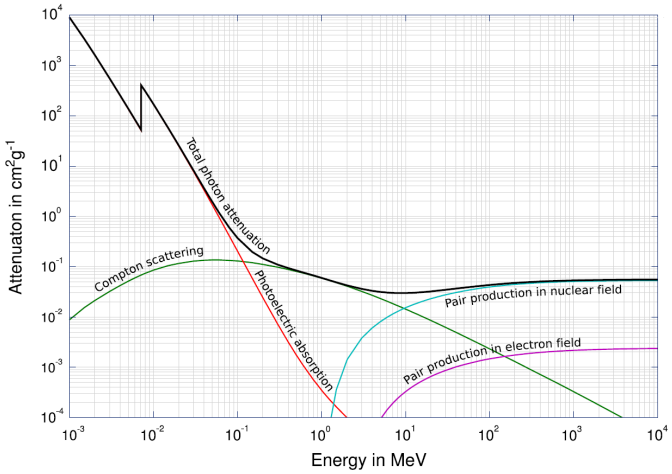


Fig. 10 Processes of proton energy absorption in iron with respect to the photon quanta [1].

Radiation Effects in PN-type Diodes

In general, the behavior of semiconductors exposed to ionizing radiation depends strongly on dopants, order of doping, particle energy, flux, fluence, type of radiation and electric current or applied voltage. But one common sensitive factor is degradation of carrier lifetime τ because of changes in concentration. They are generated or recombined with previously charge-inactive impurities as was mentioned or by ion implantation in case of ion bombardment. These, mainly point defects lying in bandgap, decrease a lifetime of abundant carriers with respect to defects capture cross-section.

During the irradiation of the N-type silicon semiconductor mainly acceptor levels at E_C - *0.16 eV* are created from typical atmospheric impurities. Similarly as phosphor they can form *E-centers* (donor-vacancy complexes) at level of E_C - *~0.45 eV*. Typical impurities in P-type material can create donor levels at E_V + *0,28 eV* and E_V + *0,05 eV*.

Free electrons and holes then recombine over these centers in forward or are generated in reverse bias. In [6], there are mentioned three types of PN junction diodes with different observed behavior and changes in V/I characteristics with respect to different neutron fluence. First type increase the forward voltage drop V_F proportionally to fluence. Second type reacts on low fluence by inversely proportional – by decrease of V_F forward voltage drop and on higher fluence then by the proportional increase of V_F. Third type of diodes decreases the V_F proportionally to fluence. Built-in voltage potential is given by (2.1.4.7)

$$V_0 = V_T \ln\left(\frac{N_A \cdot N_D}{n_i^{\,2}}\right), \text{ [V]} \qquad (2.1.4.7)$$

where,

$$V_T = \frac{kT}{q} = 26mV \text{ , at 300 K}$$

N_A is the concentration of acceptors, N_D concentration of donors, n_i is intrinsic concentration, k is Boltzmann constant, T temperature and q represents electron charge. Thus the concentration parameters are responsible for V/I characteristics changes in the term of ion implantation and lattice changes caused by radiation. From mentioned follows that with more intense radiation the carrier mobility is decreased, so the resistivity increase and the V/I characteristics 'lay' down as is mentioned in Fig. 11 (right). Creation of new conductive levels also leads to increase of leakage current in order of ten to hundred times more Fig. 11 (left).

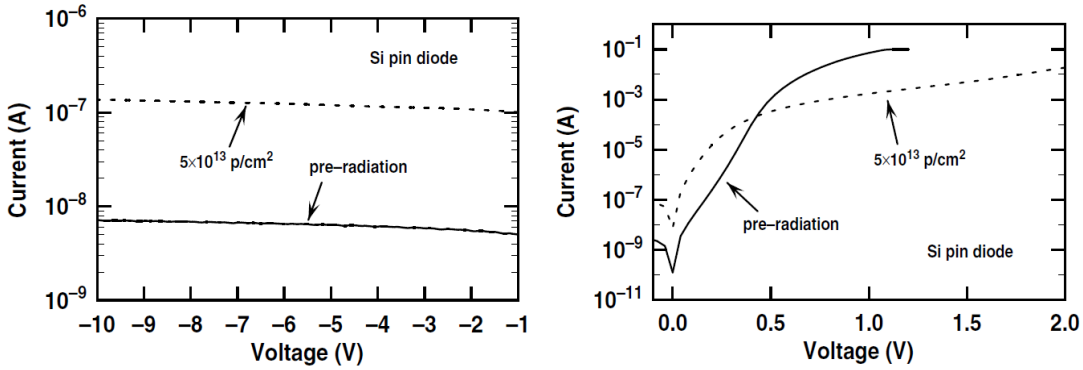


Fig. 11 Illustrative comparison of Si PN-junction V/I characteristics before and after irradiation [6]; reverse bias (left), forward bias (right).

Defects implantation during irradiation shortens the mean free path of carriers. Thus the switching time increases as well as the diode noise. For example at a fluence in order of $>10^{11}$ cm^2 protons with energy of 1 MeV the τ of low power conventional Silicon diode is so high that it loses its semi conductive behavior. Irradiation of the semiconductor by the photon radiation (γ, X, UV, ..) generates primarily the electron-hole pairs. They are distributed in the volume of the junction by applied voltage or according to the concentration of impurities. Photons are thus not the primary source of degradation processes as opposed to corpuscular radiation."

Annealing - Self healing mechanism to recovery the PN junction after irradiation

D: The thermal annealing is the effect taking into account the fact that all matter with temperature above 0 K is characterized by the movement of its atoms within the crystalline structure. When the mutual movement is stimulated by the heat, the vacancies and impurities tends to release their abnormal positions due to abnormal mechanical stress and thus recover the original structure and shape of the crystal.

R: Elevated temperature and excessive power dissipation bias point are thus one of the key ways to improve the radiation tolerance in Silicon based semiconductors as an alternative to radiation hardening process in case the low cost system is desired to be delivered to space.

2.1.5. Power Switches

D: From the switch-mode power supplies (SMPS) topology point of view there are two possibilities for choosing the semiconductor switches. One could select between current-driven bipolar or voltage controlled field effect transistors. Bipolar junction transistors (BJT) exhibit with current gain degradation which is decreased in order of tens from a nominal value. However, it is still possible to use it for switching purposes within the same circuit also

at the *End-of-Life (EOL)*. A drawback of BJTs is the high voltage drop between collector and emitter in switch-on state. Thus, from the efficiency point of view, BJTs are well suitable for high voltage power supplies. Whereas the field effect transistors with metal oxide silicon gates suffers from threshold voltage change which can lead to an uncontrollably opened channel and circuit overloading. The biggest advantage is often the extremely low switch-on resistance. The IGBT combine both drawbacks, despite its high power conversion factor. Relatively high V_{CE} voltage drop and insulated gate region controlling the collector emitter current makes this component suitable mainly for high power solar cell regulators rated to voltages in order of thousand Volts and tens of Amperes of switched currents.

R: The *Junction FETs* does not contain the insulated gate – the region where the charge deposition change doping level and accelerate recombination, decrease the carrier lifetime and make the channel current control impossible. Moreover, the JFET channel doping level is typically in order of 10^{15} to 10^{18} n·cm^{-3} [PP-3], leading to radiation displacement tolerance in order of Mrads(Si) and more. Similar components to JFETs, i.e. without insulated gate, are the *High Electron Mobility Transistors (HEMT) and MESFETs*, but suitable only for extra low voltages in order of Volts.

Industry first manufactured *SiC Normally-Off JFET* devices were introduced by US Silicon Carbide pioneering company *SemiSouth*. In [R9], two different transistors, namely *SJDP120R085 and the SJEP120R100* (R_{DSon} = 85 and 100 mΩ) were irradiated and tested to high energy gamma radiation. They were both found survived after 7 Mrad TID as a maximum of testing total dose. Unfortunately, the SemiSouth manufacturer announced closure in late 2012 and made these very promising products no longer available. The topic is discussed more in detail in [PP-3].

2.1.6. Voltage References

D: One of the key analog element in DC/DC converter is the voltage reference integrated circuit as a the thermally-stable precision voltage source. Due to the MOS transistors susceptibility to radiation damage, parametric drifts and ageing faster than in case of the bipolar technology, it is recommended to choose the bipolar junction transistors based chips as for example *LT1009* or its clones in radiation hardened version. The example of the schematic diagram of the *LT1009* is given in Fig. 12 [I-3].

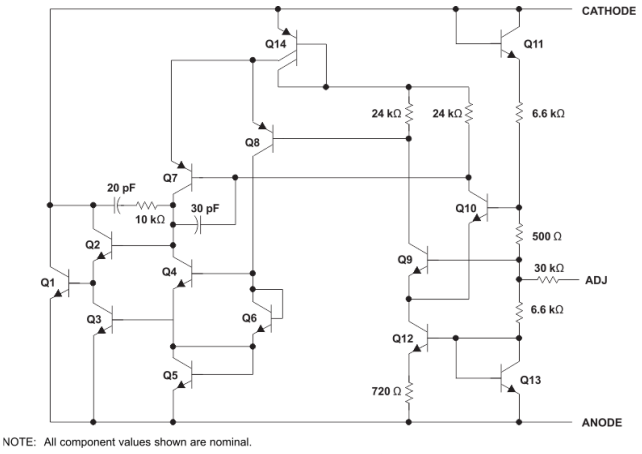


Fig. 12 LT1009 Voltage Reference Schematic Diagram, [I-3].

It is mandatory to highlight, that the high energetic particle hitting the silicon chip is penetrating the structure in various locations, inducing various voltage or charge conditions.

Such behavior is depicted in Fig. 13 [I-4]. The output voltage from steady state 2.5 V drops down by factor of several hundreds of milivolts, with the pulse duration in order of up to 3-7 μs.

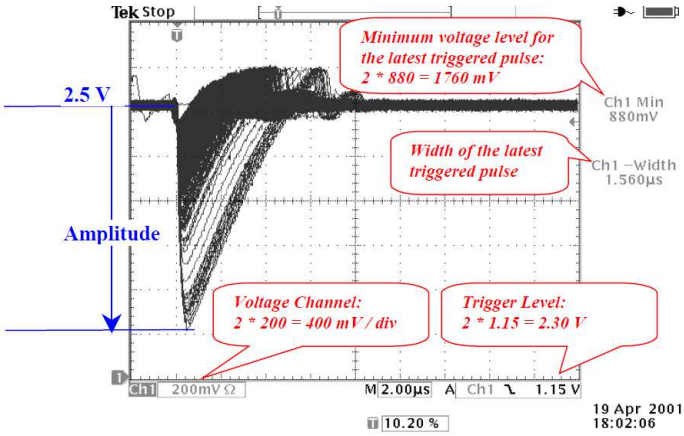


Fig. 13 The Single Event Effects on LT1009 output captured under heavy ion bombardment, [I-4].

R: The post filtering RC link to suppress and minimize the drop shall be applied such as in Fig. 14. The time constant $\tau = RC$ is in order of 10 μs for most cases and bipolar-based voltage references. As the RC product in fact commutative, the key aspect is the driving current necessary to feed the following stage. In Fig. 14 the example of operational amplifier feeding is represented. The input leakage current shall be then at least two magnitudes lower in the system end-of-life (after irradiation). Thus lower impedance of *R2* (and *R1*) is preferred. Ceramic capacitors in the order of microfarads are good candidates with respect to their miniature size (and the probability of failure of high capacity / small size *MLCCs* due to its internal high density of electrodes).

Similar *SEE* behavior is extremely important to fix in circuits such as *Undervoltage Lockouts*, *feedback error amplifiers or overload sensing circuits*, where the artificial voltage drop caused by the particle radiation could cause a temporary malfunction or the unit turn-off.

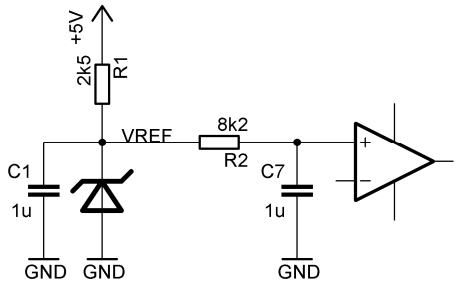


Fig. 14 Proper SEE voltage filtering schematics.

2.1.7. Opto and Photo Elements

D: The displacement damage is the root cause of the optical and photo elements degradation such as *LEDs, LASERs*, photo transistors or photodiodes. Photo sensors reacts by increased leakage (also known as dark) current which would destabilize the DC operation point of the biased sensor, photoelement preamplifier or the *DC offset* of the pulse shaping circuits. Where possible, the zero bias circuit shall be used to eliminate this phenomena.

Photon emitters, such as *LEDs and LASER* diodes degradation is indicated by the decreased output power and transition frequency, mandatory for digital optical buses. In

combined circuits such as the *OptoFETs* or *optocouplers*, both effects accumulates and lead to the *Current Transfer Ratio (CTR)* degradation.

R: There are various manufacturers of radiation hardened optocouplers with their portfolio of ruggedized and hermetic ceramic package encapsulated components, but with only limited radiation tests results available. From the metal CANs to Ceramic Leadless Chip Carrier (CLCC) packages, the example is given in Fig. 15 [I-5]. Due to the natural displacement damage degradation, the designer is either recommended to utilize highest available CTR parameter component, choose higher current driving or avoid the use of optocouplers in general.

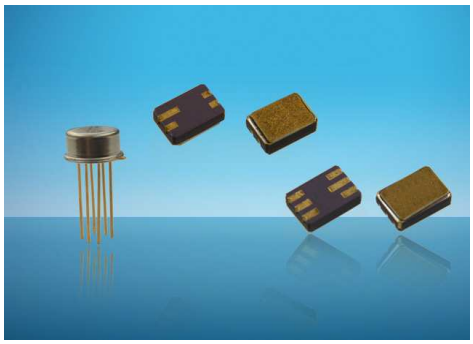


Fig. 15 Example of various packages of radiation hardened optocouplers by TT Electronics [I-5].

The advantage of the high voltage transient immunity in order of up to kV/µs, galvanic insulation and linear region of current transfer are benefits which are hardly achieved by any other type of galvanic insulation methods, such as transformer based, in given footprint. Above mentioned facts may lead to decision, that the optocoupler is still mandatory to be used. Then the spot-shielding or other physical barrier against the incident radiation (position of the system inside of the satellite body) is crucial to implement and pay attention to.

By addressing the Objective C of the Thesis, the opto-coupler feedback free insulated DC/DC converter with multiple outputs is proposed, designed and tested.

2.1.8. Electromechanical Elements and SSR

D: Monostable or latching (bistable) relays are often necessary for low power loss routing with limited amount of expected status change cycles such as high current switching, deployment initiators or battery charging/discharging controllers. There are available in various packages, with hermetically sealed cans or boxes, depending on the current, voltage or frequency rating. It is important to assure that no critical elements such as pyros or propulsion is under the control of mechanical contacts, to prevent unexpected reaction due to the launcher vibrations or shocks. To prevent unwanted reed status change, miniature permanent magnets are implemented to keep the mechanical part in stable position. The magnetic dipole is then required to be encountered in case of onboard sensors measuring the magnetic field.

R: An example of the latching relay is given in Fig. 16 [I-6]. It is the TO-5 CAN package with magnetic latching and *Double Pole, Double Throw (DPDT)* contact configuration, rated up to 1 A_{DC} and frequencies up to 1 GHz signals.

Fig. 16 Teledyne Latching Relay type HR422 in TO-5 CAN package, [I-6].

The electromechanical element is driven by the magnetic force induced by the relay coil, often supported with the force of permanent magnets to assure the shock and vibration tolerance. The driving current in monostable relays would be in order of 20 mA per coil with voltage rating between 5 to 24 Volts, implicating long-term medium power consumption and thermal power dissipation.

In a contrary, the bistable (latching) relay would be driven from the capacitor bank associated to driving elements such as bipolar transistors. The necessary energy is then stored in capacitors for status change events, which are charged via high ohmic charging resistor, assuring low power consumption since the first power up, over the whole mission lifetime and protect the spacecraft power budget in case of the permanent coil short circuit.

The hermetic package assure great radiation tolerance, which is in principle limited only by the disintegration of glass feedthroughs and the radiation susceptibility of the coil wire enamel. The amount of cycles guarantied by the manufacturer is in order of 100 000, per mechanical element.

The *Solid State Relays* based on *opto-FETs* and *LEDs* combines the disadvantages of silicon structures such as blinding of the optical receiver, dimming of the LED brightness, degradation of the CTR, similarly as in case of optocouplers. Their use shall be considered only if no other solution is not found more advantageous or spot shielding is not allowed.

2.1.9. Integrated Circuits - Analogue

D: A combination of BJT and JFET technology, with absence of MOS transistors with robust chip/transistor size is a great precursor for long-lasting linear analog circuits such as comparators in Fig. 17 [I-7] or operational amplifiers. Again, similarly as in case of the Voltage references, the circuit mounted on a chip, hit by the high energetic particle will generate the fast SEE voltage output change observable as a fast spike or drop. The accumulative TID damage is expected to create parametric drifts, mostly increased input leakage currents, quiescent currents or change the saturation voltage of output transistor stage. They might change by several magnitudes before the loss of function is encountered.

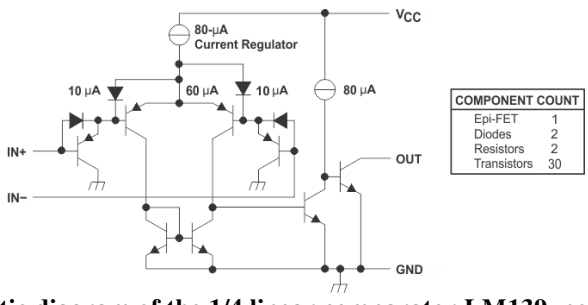


Fig. 17 Simplified schematic diagram of the 1/4 linear comparator LM139, note the bipolar technology used in critical input, signal processing and output circuits, [I-7].

R: The output of the comparator shall be R-C filtered where possible with respect to the time constraints, especially when it is used to trigger latching circuits such as electronic circuit breaker or critical events such as deployment. On the other hand, in fast signals processing chains, single missing pulse or false signal in very rapidly changing pulse trains such as sigma-delta samplers, may not cause a dramatic malfunction.

In case the analog integrated circuit to be used does not contain complementary MOS pairs, it is also understood as *Single Event Latchup Free by design*. Where the designer is not sure about the internal circuit realization or used technology, it shall assume it as SEL sensitive.

2.1.10. Integrated Circuits - Digital

D: With advancing the semiconductor development and technology, digital integrated circuits are available mostly based on CMOS transistor pairs, with advantage such as minimal input current required, very low quiescent current and power consumption, high output driving capability or fast frequency response. However, CMOS pairs in standard commercial electronics are one of the most sensitive components, when considered to be implemented in the satellite system. Single Event Latchups may be triggered easily by particles with *LET* as low as 10 $MeV \cdot mg^{-1} \cdot cm^2$, whilst practical limits for radiation hardened parts starts at around 40 $MeV \cdot mg^{-1} \cdot cm^2$ and more.

R: The designer shall utilize CMOS-based digital chips working at low voltages (3.3 V and less), to minimize the probability of avalanche-triggering the SEL, utilize power line protection against the hard (long lasting) short-circuit and integrated circuit burn-out due to excessive current and consider radiation spot shielding or possibility to replace the CMOS commercial chip with radiation hardened or even discrete-based, where feasible by the required complexity. Increased input leakage current, quiescent current, decreased driving capability and frequency response have to be kept in mind during planning the circuit behavior in the system EoL. A practical factor of 100-1000 shall be used as derating correction of working parameters during the BoL with respect to behavior under the EoL.

2.1.11. PWM Controllers

D: Commercial chips used in consumer electronics were a subject of radiation hardness investigation and improvements like single or double output drive (Flyback or Push-Pull) PWM Voltage-mode controllers *x1527* through *x1527* or Current-mode *x1840, x1841, x1843 or x1845* from several vendors (*ST Microelectronics, Texas Instruments, Microsemi, Intersil*). The most radiation hardened power supply driver on the space component market is currently the PWM5032 [R-10], double output PWM controller from the *Aeroflex/Cobham* as a product of the commercial and scientific cooperation between private company and *NASA / Mars Technology Program*. The chip with quiescent current of 7.1 mA, encapsulated in 24 pin Flat Pack ceramic package can withstand up to 1 Mrad(Si) at a dose rate between 30 – 200 rad/s. It is Single Event Latchup and Single Event Upset immune up to 100 and 20 $MeV \cdot cm^2 \cdot mg^{-1}$, respectively.

Integrated standalone primary side PWM drivers have several drawbacks. At first, the galvanically insulated feedback regulation needs to be included, such as optocouplers or magnetic isolators. Unfortunately, neither Rad Hard nor Space-qualified magnetic feedback integrated circuits were currently available on the market. In April 2013, the Intersil company announced its High Rel / Rad Hard Space Product Roadmap, where introduces the *ISL71901SEH* chip as an upgraded version of the *UC1901* Isolated Feedback Generator. It

was announced as an intended concept of radiation hardened development with beginning in 2014. TI offers this product in Hi Rel / Space category; however it is not the ESA-qualified product.

As the next category of DC/DC converters, the Point-of-Load (PoL), single chip regulators are available for local high current voltage supply, such as digital core voltage power source for ADCs, FPGAs or microprocessors. The example of high current capability PoL is for example the *ISL70003ASEH* by Intersil. It incorporates full step-down regulator requiring only external LC filter and several timing and power decoupling passive components. It delivers up to 9A, with maximum input voltage of 13.2 V and TID tolerance of up to 100 kRad(Si) with both LDR and HDR.

R: Where possible, use discrete-based solution of the PWM/power stage circuitry, to be able to choose the sensitivity of the system to radiation environment.

2.1.12. Accumulator Cells and Batteries

D: Conservatively used and preferred battery cells in aerospace industry, such as commercial airliners are the *Nickel-Cadmium (NiCd) or Nickel-Metal Hydride (NiMH)* cell assemblies with exceptionally long flight heritage, good temperature stability and power density, together with great safety during the operations.

In modern aerospace and space industry the *NiCd/NiMH* cells are often replaced with Lithium-based technology, such as *Li-Ion, Li-Poly, or* $LiFePO_4$ with the highest available power density. As mentioned in [R-11]: "The power density is 80 W/kg for the NiMH cell and lies between 330 and 3100 W/kg for the lithium-ion cells". As the fire safety is not absolute critical on unmanned spacecraft such as on the passenger carrying aircraft, the satellite power system may be designed to contain cold-redundant / multiple set of batteries, because of the unprecedented Li-cell power density.

R: From performance point of view, the amount of charging/discharging cycles with respect to cell capacity loss may not be necessarily understood as the key chemistry selection driver, as the typical time of the darkness within the orbital period (pure battery discharging) per LEO is generally not be long enough to discharge the cell/battery fully. In such case, the power budget and discharging scenarios shall be reconsidered and over-dimensioned to prevent advance mission loss due to power cycling failure. The most critical parameter to observe is the temperature dependence and discharging current, both limiting the charge accumulation capability. In case of the *Li-Ion* battery, the critical is charging and discharging below the freezing point [R-12]. The $LiFePO_4$ cells shows exceptionally good behavior also below the freezing point up to -20°C. The designer shall implement the heating elements to stabilize the temperature of the given chemistry, locate the battery pack in close vicinity to the thermally-dissipative part of the spacecraft or include the potential voltage or battery charge state into the mission power budget according to thermal characterization of the given cell.

2.1.13. Solar Cells

D: From solar orbits such as recent mission to the sun, the *NASA Parker Solar Probe*, european-japanese mission *BepiColombo* or European mission *Solar Orbiter*, up to the region of Jupiter, solar cells are the most common sources of electricity aboard spacecrafts.

Following Tab.: 2 summarizes the typical incident solar power densities at distant planets in the Solar system.

Tab.: 2 Solar Constants at given planets of the Solar System.

Planet	Distance from the Sun (AU)	Solar Power Density ($W \cdot m^{-2}$)
Mercury	57	9228
Venus	108	2586
Earth	150	1353
Mars	227	586
Jupiter	778	50
Saturn	1426	15
Uranus	2868	4
Neptune	4497	2
Pluto	5806	1

A paradox of the insufficient amount of power available at orbits closer to the Sun, than on LEO is caused by the need for excessive cooling of the solar cell array, as the efficiency of the photovoltaic effect in the semiconductor is inverse-proportional to the cell temperature.

The state-of-the-art mass production triple junction solar cells shows 30% efficiency with Air Mass 0, power density *1367 Wm^{-2} and 28°C* conditions, with maximum power point tracking (MPPT) load [R-13]. The manufacturer claims the drop in the efficiency down to 26.5% at the same optical conditions, when the cell is irradiated by 1 MeV electrons with fluence of $10^{15} e \cdot cm^{-2}$.

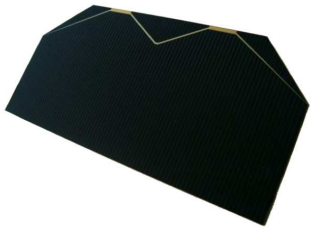


Fig. 18 Triple junction solar cell by Azur Space, [R-13].

R: According to [R-14], the highest practical solar array string voltage shall not be higher than 160 V to prevent short duration arcing between the solar panel conductive substrate and the cell. Thin glue or tape layer necessary to mount the cell into the panel is required to establish the thermal bridge and cool down the cell exposed to the sunlight. The schematic diagram in depicts the string and the situation of the voltage potential on large array.

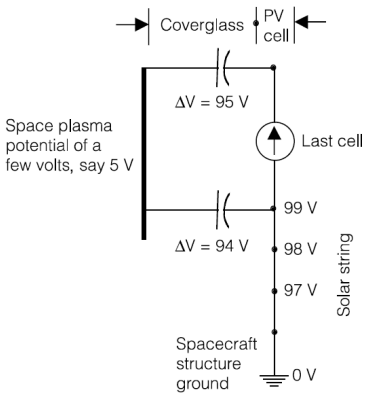


Fig. 19 High voltage solar cell string diagram with space plasma surroundings, [R-14].

2.1.14. Alternative Power Sources

D: There are plans to develop and produce more secure isotope-based types of power sources such as *Radioisotope Thermoelectric Generators (RTGs)*, mostly containing pellets of primarily alpha-decaying *Plutonium Oxide* $^{238}PuO_2$, *or* $^{90}Stroncium$ producing heat which is then converted using thermoelectric elements based on Seebeck effect into electricity. Such highly radioactive element aboard the launcher represents significant environmental risk, if the vehicle disintegration during the launch phase below the orbital velocity occurs above the populated territory.

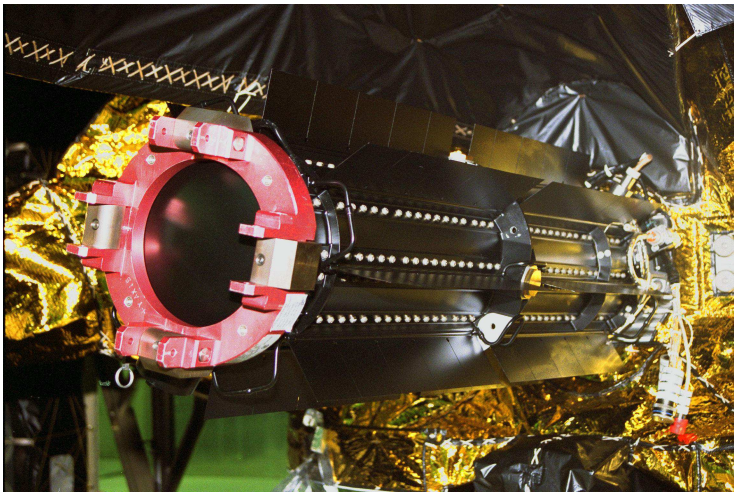


Fig. 20 Radioisotope Thermoelectric Generator power source of the Cassini spacecraft, [I-8].

Despite the thermocouple-based electricity generating principle, one of the promising technological breakthrough is the Betavoltaic battery. It represents a new way of long-lasting power generation assemblies development for deep space missions with not available sun-generated power. Several studies were done recently with working examples, using *tritium* ^{3}H, $^{14}Carbon$ *or* $^{63}Nickel$ as beta-radiator isotopes and P-N based charge colleting electrodes. Scientific studies such as [R-15] and [R-16] claims the power yield achieved so far in order of μW, power density of *3.3* $kWh \cdot kg^{-1}$, with operational lifetime expected to be between 25 to 100 years.

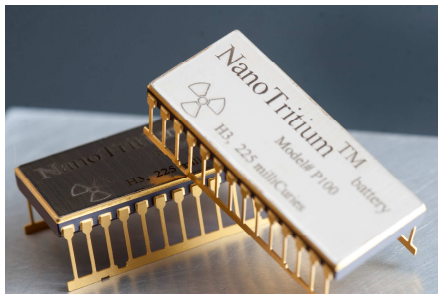


Fig. 21 Tritium-based beta decay battery cell by Citi Labs, [R-16].

R: All above listed isotopes decay as pure beta radiators and thus does not convert to the penetrating gamma ray isotopes over time, such as in case of the ^{238}Pu*-based RTGs*. They are suitable to be embedded close to the target electronics, whilst RTGs have to be mounted on external booms to protect the spacecraft itself during the operational lifetime.

2.1.15. Chemistry for Assembly and Finish

D: To prevent the disposal and minimize the amount of the lead in the environment by human activity, several countries have agreed and implemented into national legislation a rule proposed by the European Parliament in 2011, known as directive RoHS 2011/65/EU. Since that time, it was adopted by the majority of countries with the dominant market influence, such as USA, China, Switzerland and South Korea. The directive defines the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment. In consumer electronics with two year warranty cycle, the quality of solder joints using pure tin or the alloy of 99.5% tin with 0.5 % of silver is sufficient and does not block the production or reduce the customer comfort. In general, a vast majority of electronic parts manufacturers does not offer their portfolio in other than so-called RoHS-free or lead-free pad finish. Whilst, components for military and aerospace markets are still available with gold or solder pad finish assuming the tin/lead compound.

R: Although, the growth of tin whiskers, a crystalline structures similar to cat whisker, growing from the tinned part is not a new phenomenon (first observed in early 1940-1950), there are several spacecraft malfunctions in space considered to have a tin whisker growth as a cause. According to the *NASA NEPP program* [R-17], there are also other metals broadly used in space electronics sensitive to whisker growth, if the metal is present as pure. According to [R-17] such metals are: zinc, cadmium, indium, antimony or silver. In the electronic assembly, zinc finish could be easily met on some commercially available screw/board standoffs, silver then on connectors.

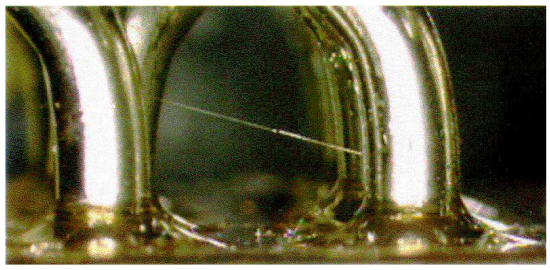


Fig. 22 The example of formed tin whisker, [R-17].

As the growth is dominant under the vacuum and was not clearly understood so far, the recommendation is to use the tin/lead 60% / 40% or 63% / 37% compound for soldering, pre-tinning for general electronic parts and even re-balling of BGA packages (if no other package is available for the chip).

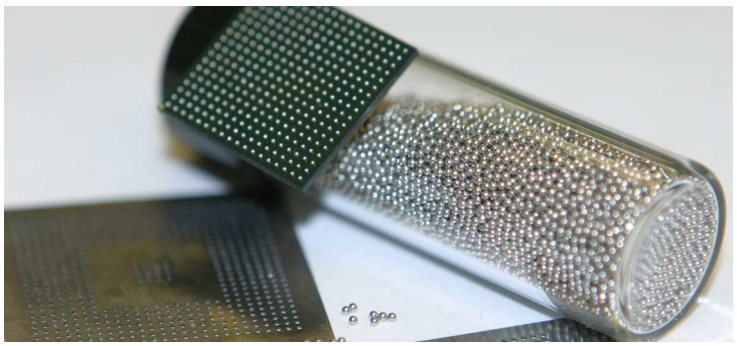


Fig. 23 The BGA chip, stainless steel stencil and tube with Tin/Lead balls ready for re-balling process of the commercial grade chip made to comply with RoHS. Image Credits: https://www.deskdecode.com/reballing

Similar pre-manufacturing treatment shall be valid for PCB traces. Conformal coating would help to stop or slow down the crystalline growth process, but also the penetration of the thin surface layer was observed [R-18]. The PCB coating thus could not be understood as fully sufficient solution for commercial-grade assemblies with high density chips such as industrial computers, primarily intended for terrestrial use.

As the tin whisker is physically a thin element, the possible short circuit caused inside of the power connector or close to the power bus with power source is naturally eliminated by self-burnout. The worst case remaining is small signal routing and high density pin or pad equipped integrated circuits.

D: Among the prohibition of lead in the solder compound, in Europe, the directive also prohibits the presence and use of the *Chromium-6*, broadly included in the aluminum conserving process chemicals called Alodine-1200, with its typical golden color. So far, within the European Union, no direct replacement was introduced or recommended, whilst in other countries it is still in use for aerospace industry. The black hard anodized surface provides similar aluminum anticorrosive treatment, but the thermal properties of such black body cools the unit down in vacuum environment, due to the infrared radiation. Golden color emissivity of the finalized unit surface is up to the magnitude less than the black one. In Tab.: 3 the comparison between two different coatings of the same aluminum material with a layer in order of several micrometers is summarized.

According to the Kirchhoff's law, the emissivity and absorptivity of a given material (color, paint, metal, ceramic, plastic, etc.) is the same at a given wavelength (monochromatic equality). Taking into account the spectra of the sunlight in space, the given absorptivity of the material is different than the emissivity of the infrared radiation (thermal dissipation for example). Such difference is a base for the design of the cooler or heater element on spacecraft body or components. There are also active means of temperature control such as mechanically steerable louvers or thermal switches for cases where the positive and negative balance is required to be changed during the mission.

Tab.: 3 A comparison between different Aluminum Surface Treatments, [R-19].

Aluminum Surface Treatment	α_{Sun} - Absorptance	ε_{IR} - Emissivity
Alodine 1200	0.39	0.068
Black Anodizing	0.68	0.88

R: Whilst onboard accumulator and battery assemblies are required to keep their internal temperature above the 0°C during the operations (almost all lithium-ion based batteries) it is desirable to finish their surface with the Alodine-1200 or similar treatment. Power supply units or highly power dissipation electronics would require the black anodizing finish to naturally dissipate the power into the space or spacecraft body by the radiation.

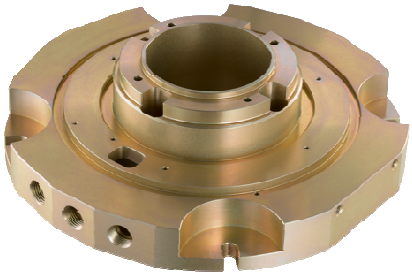


Fig. 24 Alodine-1200 Chroming applied on aluminum example.

Fig. 25 The example of the Black Hard Anodized aluminum.

The Stefan-Boltzmann law in 2.1.15.1 applied to the space environment shows that the body with given emissivity radiates the energy per unit time by

$$Q_{Radiated} = \varepsilon_{Infrared} \cdot \sigma \cdot A_{Element} \cdot (T_{Element} - 4)^4, \tag{2.1.15.1}$$

where ε is the emissivity of the surface, σ is the Stephan-Boltzmann constant, $A_{Element}$ is the surface area and T is the absolute temperature, where the ambient space relict radiation temperature $T = 4\ K$ is subtracted. Then the received energy per unit time from solar radiation incident at given angle is in 2.1.15.2

$$Q_{\mathrm{Re}\,ceived} = \alpha_{Sun} \cdot A_{Element} \cdot P_{SolarFlux} \cdot \cos\varphi, \tag{2.1.15.2}$$

where α_{Sun} is the absorptivity of the material surface at a given peak of the incident solar spectra, $A_{Element}$ is the surface area, P is the solar flux power per square meter at given distance from the sun (~1367 Wm^{-2} on *LEO*), and ϕ is the incident angle between the solar flux and material surface. If the $Q_{SelfGenerated}$ is the power of the self heating of the element, then the thermal equilibrium could be found by solving the 2.1.15.3 and resulting in stead state temperature TElement in vacuum environment in 2.1.15.4

$$Q_{\mathrm{Re}\,ceived} + Q_{SelfGenerated} = Q_{Radiated}, \tag{2.1.15.3}$$

$$(\alpha_{Sun} \cdot A_{Element} \cdot P_{SolarFlux} \cdot \cos\varphi) + Q_{SelfGenerated} = \varepsilon_{Infrared} \cdot \sigma \cdot A_{Element} \cdot (T_{Element} - 4)^4,$$

$$\frac{(\alpha_{Sun} \cdot A_{Element} \cdot P_{SolarFlux} \cdot \cos\varphi) + Q_{SelfGenerated}}{\varepsilon_{Infrared} \cdot \sigma \cdot A_{Element}} = (T_{Element} - 4)^4,$$

$$\sqrt[4]{\frac{(\alpha_{Sun} \cdot A_{Element} \cdot P_{SolarFlux} \cdot \cos\varphi) + Q_{SelfGenerated}}{\varepsilon_{Infrared} \cdot \sigma \cdot A_{Element}}} - 4 = T_{Element},$$

$$T_{Element} = \sqrt[4]{\frac{(\alpha_{Sun} \cdot P_{SolarFlux} \cdot \cos\varphi) + Q_{SelfGenerated}}{\varepsilon_{Infrared} \cdot \sigma}} - 4 \tag{2.1.15.4}$$

By solving the equation 2.1.15.4 with parameters given in Tab.: 3 the steady state temperature $T_{Element}$ for the insulated sun-facing surface is approximately 92°C and 332°C for *Black Anodizing* and *Alodine 1200* respectively, regardless the size of the element (when considering the sun power flux equally distributed). Although, the steady state temperatures might looks way too high with respect to commonly known temperatures of spacecraft bodies, it is necessary to point out the conditions considered during the calculation: the Sun Synchronnous Orbit and steadily constant incident angle of the satellite surface with no tumbling at all. With averaging and the thermal capacity taken into account the overall steady state temperature for above mentioned aluminum surface treatments varies approximately between -20°C for *Black Anodizing* and +40°C for *Alodine 1200*.

It is immediately clear how important the surface treatment/color finish is for the thermal control of any spacecraft system. In case of small satellites with self generated power in order of units of Watts, the self generated heat could be omitted from calculations. It means also that it is not worth to install active (electrical) thermal control system to such small satellites (CubeSats, etc.), in contrary to the passive means of thermal control using solar radiation. Such thermal balance system is barely possible or efficient due to not enough energy onboard to dissipate.

D: At the launch pad the electronics is stowed inside of the payload fairing in clean area. However, the electronic boards, assemblies and connectors may absorb the air humidity and possibly start to corrode, especially, when the payload fairing is not air-tight and the rocket is held at sea side cosmodrome. With assembly, integration and verification premises surrounded by the salty air and humidity which could be very aggressive to metallic parts, the uncoated electronic boards may start to degrade over the period of the long launch window.

R: For this reason, a chemical conserving layer of conformal coating shall be applied. There are several coatings such as two-part *Mapsil 213B* or single-part *Nusil CV-1152* or Parylene. Conventional conformal coatings and casting varnishes known from automotive industry or transformers encapsulation may suffer by high outgassing under the vacuum conditions and could evaporate from the surface by sublimation. During the in-orbit flight, the microgravity or weightlessness conditions cause that the evaporated particles will form a cloud which could then fly together with the satellite and may be attracted to sensitive surfaces such as optical elements by electrostatic forces, spacecraft charging or space plasma environment. It is therefore necessary to check the selected conformal coating with respect to its volatility.

D: Special part of the assembly and finish is the soldering and manufacturing process, which is a complex task, out of the scope of this thesis. This work is focused on design phase, where components are selected and being implemented into final system.

R: The manufacturing work is expected to be done properly, with significant influence on the final system reliability. In the european space industry, one of the key standard to follow during the manufacturing would be for example the standard *ECSS-Q-ST-70-38C*.

2.2. Hybrid Space-grade Power Supplies Overview

D: Encapsulated ready-to-use solutions exist to cover radiation hardened space-grade power conversion needs. For example, the International Rectifier or *VPT Inc.* vendors offer hermetically sealed hybrid solutions, both qualified to 100 kRad(Si). Internal block diagrams and physical form are given in Fig. 26 in and Fig. 27. It benefits from small dimension (glued and directly bonded chip dies) and no optocouplers. Proprietary solution (isolation amplifier) is realized as the magnetic feedback insulation. Both reaches efficiency around 80 % at full load (15 W) and voltages from 5 to 12 Volts. Low voltage ranges (1.5 V, 3.3 V) suffers from ratio between diode voltage drop and output voltage level, thus the efficiency falls to approximately 65% and 72%, respectively.

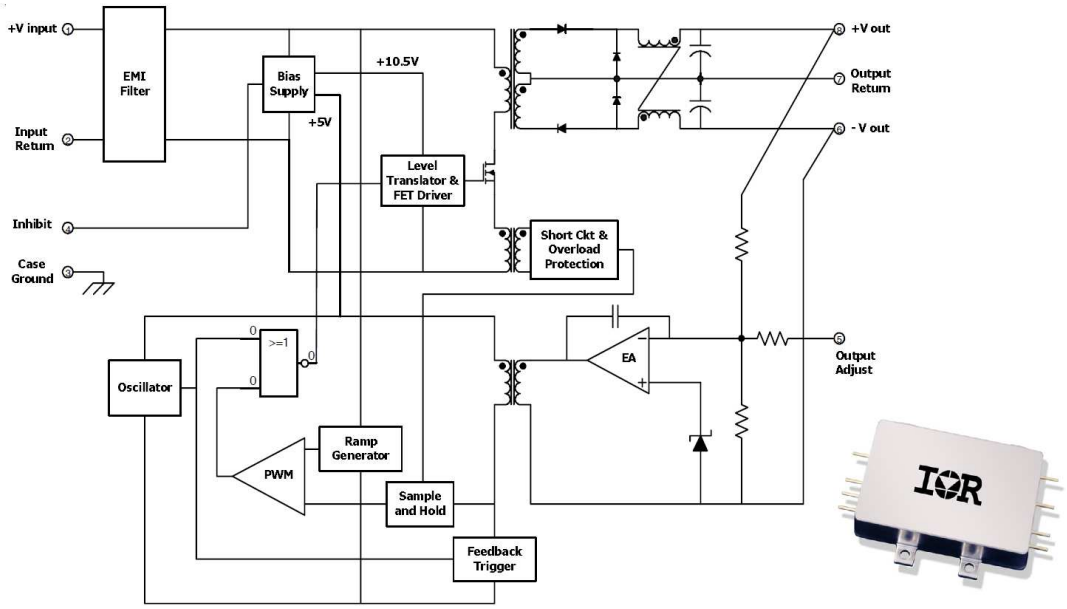


Fig. 26: International Rectifier LS-Series Hybrid DC/DC Module topology Schematic Diagram, Double Symmetrical Output displayed, 500 kHz fixed Switching Frequency; Image Credits: IR.

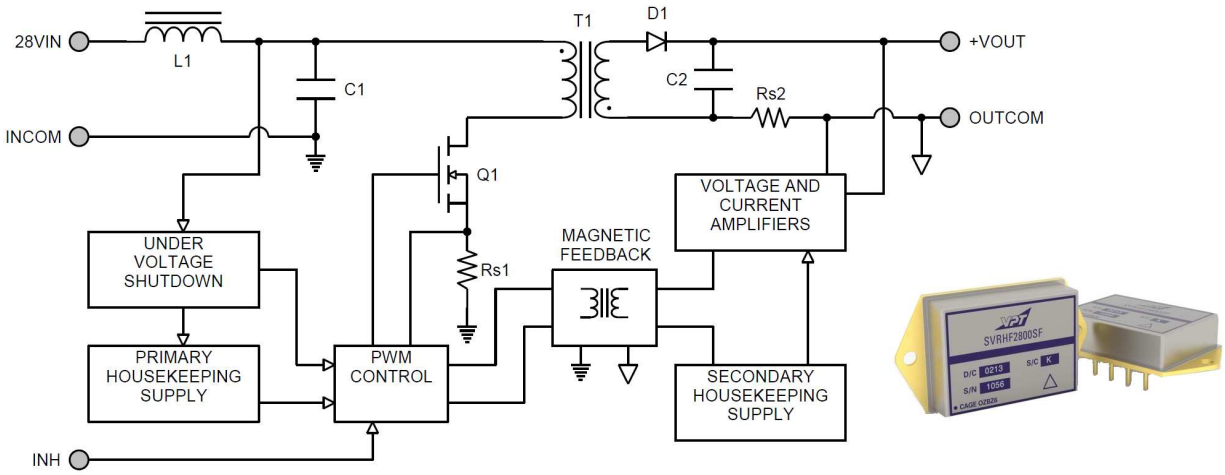


Fig. 27: VPT's SVRHF2800SF Hybrid DC/DC Module topology Schematic Diagram, Single Output, 15 W, 450 kHy fixed Switching Frequency; Image Credits: VPT, Inc.

R: The integrated/hybrid solution is therefore beneficial when single or double output is required with no additional need for housekeeping measurement or power distribution matrix and could not be always utilized as drop-in solution of all spacecraft power systems.

3. Objectives of the Thesis

The core of the Thesis is to propose and implement novel approaches in construction of space power electronic systems in category *"Reliable by Design"*, where conservative approaches used so far in aerospace industry and rad-hard / space-qualified markets does not provide with ready-made solutions to low cost *NewSpace* community.

The Thesis shall implement the developed knowledge base into the real application in the frame of the international scientific space plasma measurement package project called Radio and Plasma Waves Investigation instrument or *RPWI*, under the flag of *European Space Agency's* mission *JUICE* (Jupiter Icy Moon Explorer), Langmuir Probe and Magnetometer experiment as a part of the *L-DEPP* (Lunar Dusty Environment and Plasma Package) consortia, the CzechTechSat Czech Technical University in Prague University Picosatellite Platform and *CRREAT* (Research Center of Cosmic Rays and Radiation Events in the Atmosphere) projects. The work to be done is addressed by four following tasks:

A. To analyze the state-of-the-art space grade power supply converters and power electronics with a focus on utilization onboard resource-constrained missions.

B. To identify bottlenecks of electrical components and propose novel power electronics concepts with aim for deep space and interplanetary missions, and find its applications within the *CzechTechSat* and *L-DEPP* projects.

C. To implement the application of proposed methods for very low noise, cold-redundant low voltage power supply unit for deep space scientific instrument use-case as an alternative approach to integrated circuit solutions intended for *LEO* markets under the frame of the *LVPS/RPWI*.

D. To develop the miniature, low power solid-state dosimeter for small satellites with aim to cover wide energy spectra of gamma rays. To perform the high-altitude balloon test flight to validate the system functionality in the frame of the project *CRREAT*.

4. Hypotheses

To support each of the Thesis goals following hypotheses were further studied by the scientific work performed during each project term. Their list is given in Tab.: 4 below.

Tab.: 4 The summary of hypotheses further studied in the frame of the Thesis.

CzechTechSat Project					
No. of Hypothesis:	**Hypothesis Description**	**State-of-the-art**	**Implemented**	**Validated**	**Applicability to the NewSpace Community**
1	All BJTs which parametrically fits the manufacturer's datasheet parameters such as S21, VCEsat, etc. could be utilized.	It is believed that only costly screened BJT transistors shall be utilized in spacecraft systems.	Yes. (28V to 5 V DC/DC converter, Fluxgate Magnetometer payload - sensor excitation, deployment circuit for the boom), CubeSat EPS.	Yes, by radiation testing (Co60, 363 kRad(Si)).	Immediate.
2	BJTs operated at elevated power dissipation conditions may self-heal during irradiation due to the continual annealing.	It is believed that costly screened BJTs are subject to parametric degradation up to the End-of-Life with no way of self-healing.	Yes. (28V to 5 V DC/DC converter, Fluxgate Magnetometer payload - sensor excitation, deployment circuit for the boom), CubeSat EPS within CzechTechSat project.	Yes, by radiation testing (Co60, 363 kRad(Si)).	Immediate.
3	Elevated temperature of the spacecraft system, excluding batteries in order of 50-70°C would increase the operational lifetime.	Elevated temperature is not considered as a safety measure to prevent satellite systems from the radiation defects or system performance degradation, mostly for conservative reasons.	Yes. Design of the CzechTechSat Thermal Control System	Partially, confirmed only on part by part basis.	Partially, further study needed, mainly with respect to spacecraft batteries sharing the same thermal environment of the satellite
4	Ferroelectric cells RAM memories are less vulnerable to radiation and thus could be utilized in space as a direct replacement for SRAMs, FLASH memories or similar. Memory chips still contains CMOS readout circuits. However the amount of CMOS pairs is magnitudes lower than in case of pure SRAM or FLASH based memories.	Naturally, Ferroelectric principle of bit memory storage is understood as based on non-silicon technology and thus less vulnerable to radiation. Accompanied CMOS readout chips might block the operations and thus the usability of FRAM in space.	Yes. (Fluxgate Magnetometer payload - sensor excitation driving signal memory map circuit, CubeSat Onboard Computer within CzechTechSat project).	Feasibility and functionality of the system validated, not validated under radiation conditions.	Partially, further study needed under radiation conditions.

5	Parallel Triple Module Redundancy would be realized using multiple ports or pins of the microcontroller with distributed power and data bus.	No commercial triple module redundancy chips are available, only the radiation hardened versions with additional rad-hard voters. Parallel TMR using COTS solution not understood as reliable.	Yes. (Cold Redundant CubeSat Onboard Computer within CzechTechSat project).	Feasibility and functionality of the system validated during the High Altitude Balloon test flight up to the altitude of 33000 meters. With no detectable bit flips in data stored.	Immediate.
6	Distributed Serial Bus similar to RS-485 would be supported by the differential amplifiers improving the noise immunity by derivation of the input signal even with heavy loaded input leakage currents of particular receiver hooked on the bus.	Only dedicated bus drivers conforming RS-4xx standards are used.	Yes. (Cold Redundant CubeSat Onboard Computer, ADCS within CzechTechSat project).	Yes, artificially loaded LVCMOS bus was restored from LVCMOS signaling amplitudes down to 1Vpp at 9600 bps.	Immediate. Parametric improvements and scalability possible.
7	Junction FET transistors with no insulated gate, regardless of the type or vendor shall be utilized in space power switching circuits, according to their commercial usage given in the manufacturer's datasheet. It is due to the absence of the problematic charge capture insulated region controlling the conductivity after irradiation.	No COTS JFETs used in high power switching so far. SiC MOSFETs under review for rad-hard industry.	Yes. (Cold Redundant CubeSat Onboard Computer, ADCS within CzechTechSat project).	Yes, by radiation testing (Co60, ~60 kRad(Si)).	Immediate.

8	Low VCEsat or BISS transistors with overdopped silicon semiconductors regardless of the type or vendor shall be utilized in space power switching circuits, according to their commercial usage given in the manufacturer's datasheet. It is due to the magnitudes higher doping with respect to doping induced by radiation.	Currently overdopped BJT transistors are used mostly only in automotive industry as a replacement for medium current switching relay mechanisms.	Yes. (Fluxgate Magnetometer deployment initiators power switching within the CzechTechSat project).	Feasibility and functionality of the system validated, not validated under radiation conditions.	Partially, further study needed under radiation conditions.
LPM/L-DEPP Project					
No. of Hypothesis:	**Hypothesis Description**	**State-of-the-art**	**Implemented**	**Validated**	**Applicability to the NewSpace Community**
9	The pulse modulation with saturated switching shall be utilized to suppress the analog parameters degradation such as total gain, input leakage current, etc. especially in floating ground circuits. The analog to digital level domain using saturation of output switching stages would postpone the radiation effect on system performance	Rad-hard analog circuits with derating are used.	Yes. Engineering model of the LPM/L-DEPP	Feasibility and functionality of the system validated, not validated under radiation conditions.	Immediate. Scalability and performance to be optimized for particular solution.
10	BJT based output high voltage stage would work as a replacement of diode-based multipliers with extremely high sensitivity to temperature variations and radiation degradation. Opamp with the feedback is a good candidate to control the output voltage with respect to reference threshold.	Villard Cascade diode multiplier used so far for scientific purposes where high voltage sweep generator as low current power source controlled by low power digital circuits is used. With no direct feedback, the circuit is extremely sensitive to thermal variations and radiation degradation.	Yes. Engineering model of the LPM/L-DEPP	Feasibility and functionality of the system validated, not validated under radiation conditions.	Immediate. Scalability and performance to be optimized for particular solution.

ESA JUICE LVPS/RPWI Project					
No. of Hypothesis:	**Hypothesis Description**	**State-of-the-art**	**Implemented**	**Validated**	**Applicability to the NewSpace Community**
11	Discrete based design of the PWM regulator would significantly improve the radiation tolerance, when the circuit is build around part-by-part selected and properly biased parts.	Integrated PWM controllers exist only with 50kRad(Si) TID tolerance, with maximum of 1MRad (under ITAR restriction).	Yes. Engineering model of the LVPS.	Feasibility and functionality of the system validated, not validated under radiation conditions.	Immediate. Scalability and performance to be optimized for particular solution.
12	Inrush current limiting would be preformed by pulse train driving to chop the inrush current during the startup.	Gate-Source capacitive time constant introduced and commonly used.	Yes. Engineering model of the LVPS.	Feasibility and functionality of the system validated, not validated under radiation conditions.	Immediate. Scalability and performance to be optimized for particular solution.
13	Optocoupler-free feedback DC/DC converter is feasible with output impedance of 100mOhm or better.	Optocouplers commonly used in feedback.	Yes. Engineering model of the LVPS.	Feasibility and functionality of the system validated, not validated under radiation conditions.	Immediate. Scalability and performance to be optimized for particular solution.
CRREAT					
No. of Hypothesis:	**Hypothesis Description**	**State-of-the-art**	**Implemented**	**Validated**	**Applicability to the NewSpace Community**
14	Low power high energy gamma sensitive radiation meter would be based on scintillator-equipped Si PIN photodiode instead of high voltage biased Geiger-Müller tube.	Geiger-Müller tubes are used for high energy gamma radiation detection.	Yes. Engineering model of the LPM/L-DEPP	Feasibility and functionality of the system validated during the High Altitude Balloon test flight up to the altitude of 34500 meters.	Immediate.

5. Results

Results of the scientific period of the PhD. studies at the Czech Technical University, Faculty of Electrical Engineering, Department of Measurement at laboratories *SpaceLab, MagLab and NavLis* in parallel with the workplace at the *Astronomical Institute of the Czech Academy of Sciences, the Solar Department* are summarized in following chapters according to the list of objectives defined in Chapter 3.

5.1. Objective A)

Most of the research work done to achieve goals in the Objective A were obtained during the initial study phase between 2011 - 2013. This period addresses the summary given in the Chapter 2 and published more detailed in papers [PP-1], [PP-3] with a focus on individual types of components and their typical behavior under the radiation environment.

5.2. Objective B)

By the work on project CzechTechSat in the period between 2011 up to 2015, a total of six Functional Samples [FS-1 to FS-6] were developed at the CTU FEE with a co-development with bachelor and master students on various subsystems or ground support equipment for the subsystem testing, the emulation of space magnetic field and one degree of freedom in rotation (quasi-weightlessness). All work was performed thanks to the financial support from the Student Grant Competition of the Czech Technical University in Prague.

5.2.1. The CzechTechSat Project

Several concepts regarding reliable data storage, autonomous power arbitration, communication bus drivers and fluxgate magnetometer design including FRAM chip have been implemented in the low cost commercial-off-the-shelf based CzechTechSat (CTS) CubeSat-class picosatellite project depicted with deployed magnetometer sensor in Fig. 28.

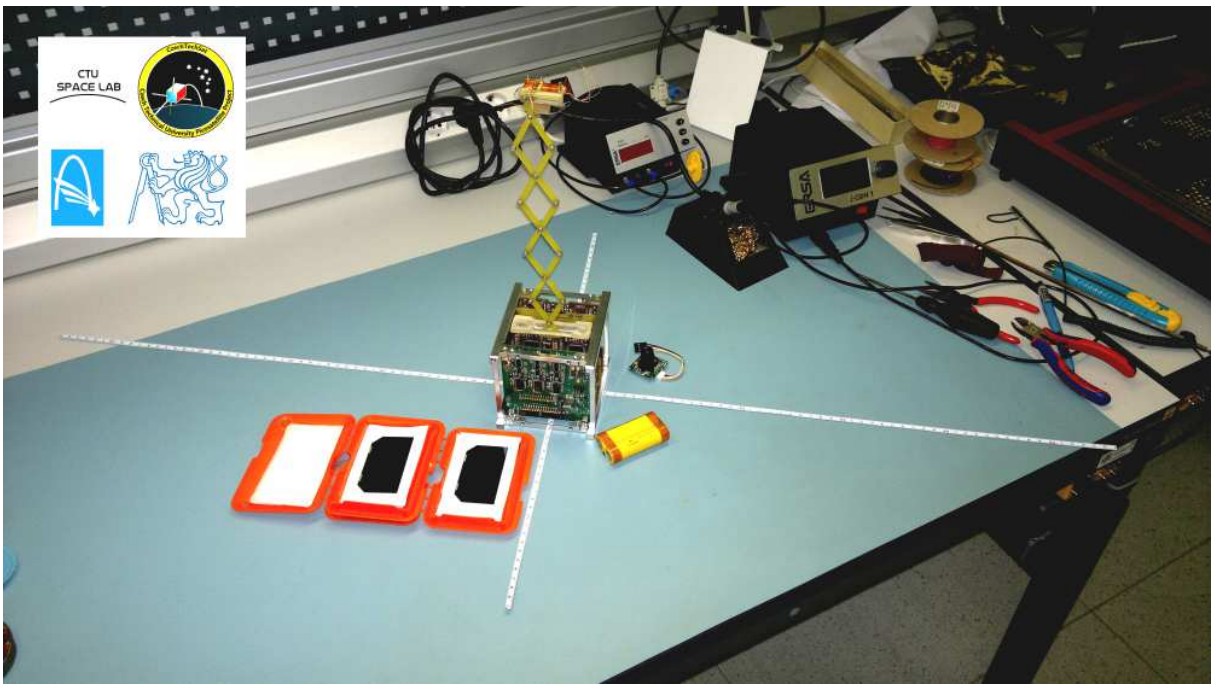


Fig. 28 The CzechTechSat Picosatellite, Engineering Model.

Thanks to the CTU financial support the CTS project could have been presented on the *10th Annual CubeSat Developers' Workshop at Cal Poly, CA, USA*, where the CubeSat standard was established in 2003. After the presentation, surprising response from US scientific and commercial community was received regarding the radiation impacts mitigation on semiconductors within the CTS as the first CubeSat Rad-Tolerant platform. The multi-disciplinary project connecting together students and academic staff from the *Faculty of Electrical Engineering and Faculty of Mechanical Engineering, Czech Technical University in Prague*, is a basis of a total of six Master Theses [MT-1 to 6].

One of the subsystem studied and developed is the Fault Tolerant On-Board Computer for CubeSat-class Satellite, with conceptual design published in [PP-6], and further block diagram description in Fig. 29. At the time of publication, it was the first up-to-date On-Board Computer for space applications and intended for low-cost CubeSat missions, utilizing Triple Module Redundancy realized using three identical Ferroelectric RAM memory-based storage chips and fully autonomous over-current driven power arbiter. It was based on scientific study by [R-20], assuming that in cold-redundant systems, the radiation damage would be lower in not-biased circuits. Thus, it is necessary to switch between the Main and Redundant power systems and not to run both simultaneously in hot-redundancy. Three memory chips were used to implement the TMR and software-based majority-out-of-three voter for valid data processing.

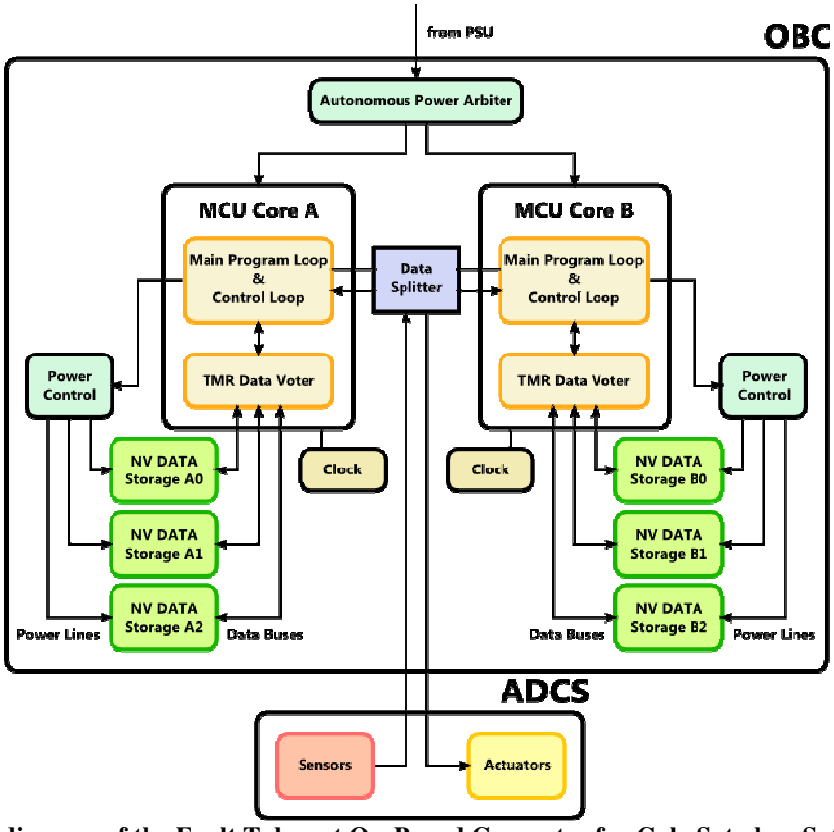


Fig. 29 Block diagram of the Fault Tolerant On-Board Computer for CubeSat-class Satellite, [PP-6].

The proposed Autonomous Power Arbiter is working as the one-time controlled bistable power switch, driven by the overcurrent detection method depicted in Fig. 30 (left) and its practical implementation example (right). The principle is based on sensing the voltage drop on current-sensing resistors *R**, expected to be set to trigger the bistable switches according to V_{GSth} of respective *P-MOSFETs*. The accumulated TID radiation damage is

mostly characterized by increased total power consumption. The proposed Arbiter is flipping from feeding the power to the Subsystem A to Subsystem B, when the current consumption exceeds predefined values. The *C1* capacitor is dimensioned to suppress the *Subsystem A* inrush current influence on initial (main +5 V) power-up event.

Practical implementation was successfully tested and further accommodated in the frame of the Master Thesis [MT-1], physical system realization is depicted in Fig. 31.

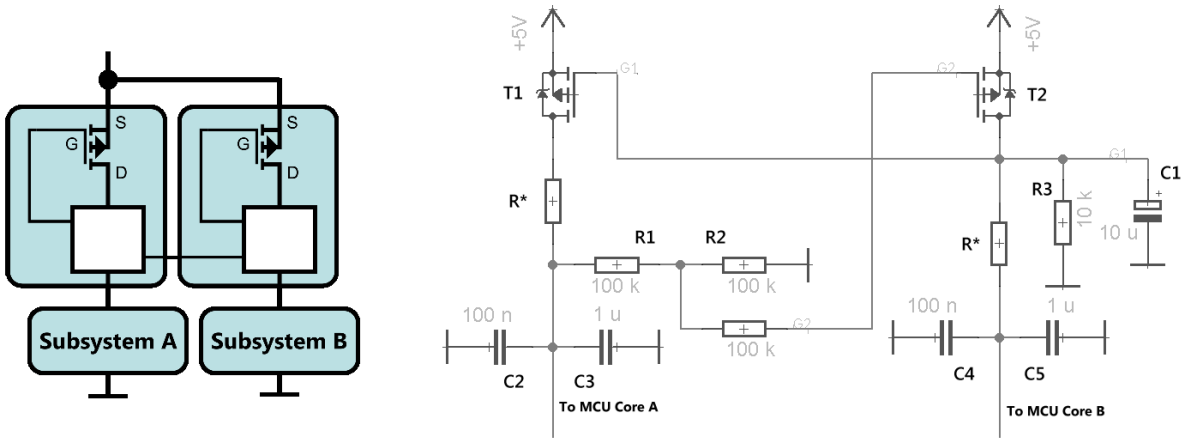


Fig. 30 One-time controlled bistable power switch concept and schematics.

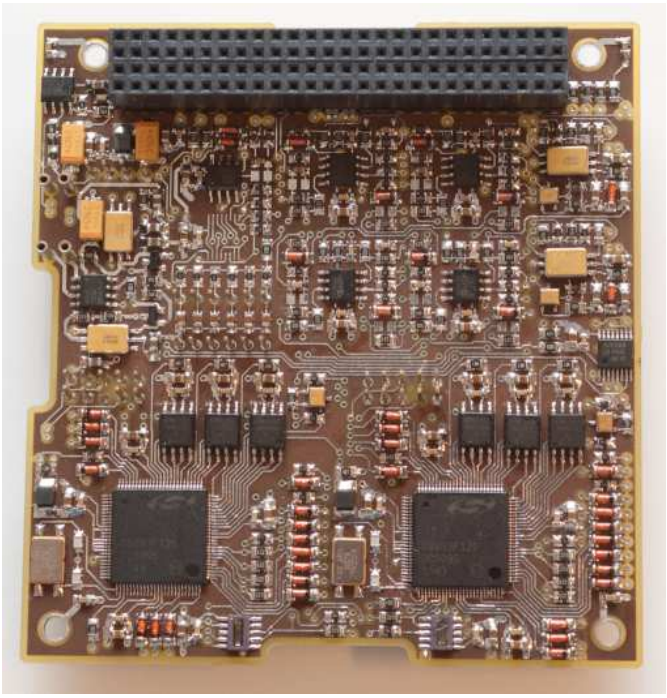


Fig. 31 The Cold-Redundant CzechTechSat On-Board Computer unit with TMR FRAM storage and autonomous power arbiter.

The next system based around the non-volatile Ferroelectric RAM for the predefined quasi-sine wave storage is implemented successfully in the frame of the *Fluxgate Magnetometer Payload* [MT-4]. The triplet of *Fluxgate Sensors* is driven using the BJT-based H-bridge and the synchronous detection with variable PWM-based signals reconfigurable during the flight. With *CTU FEE, Maglab* developed sensors and the scissor type boom, the payload is belonging to the one of the state-of-the-art and the most compact boom-including magnetic field measurement equipment concept in the CubeSat community.

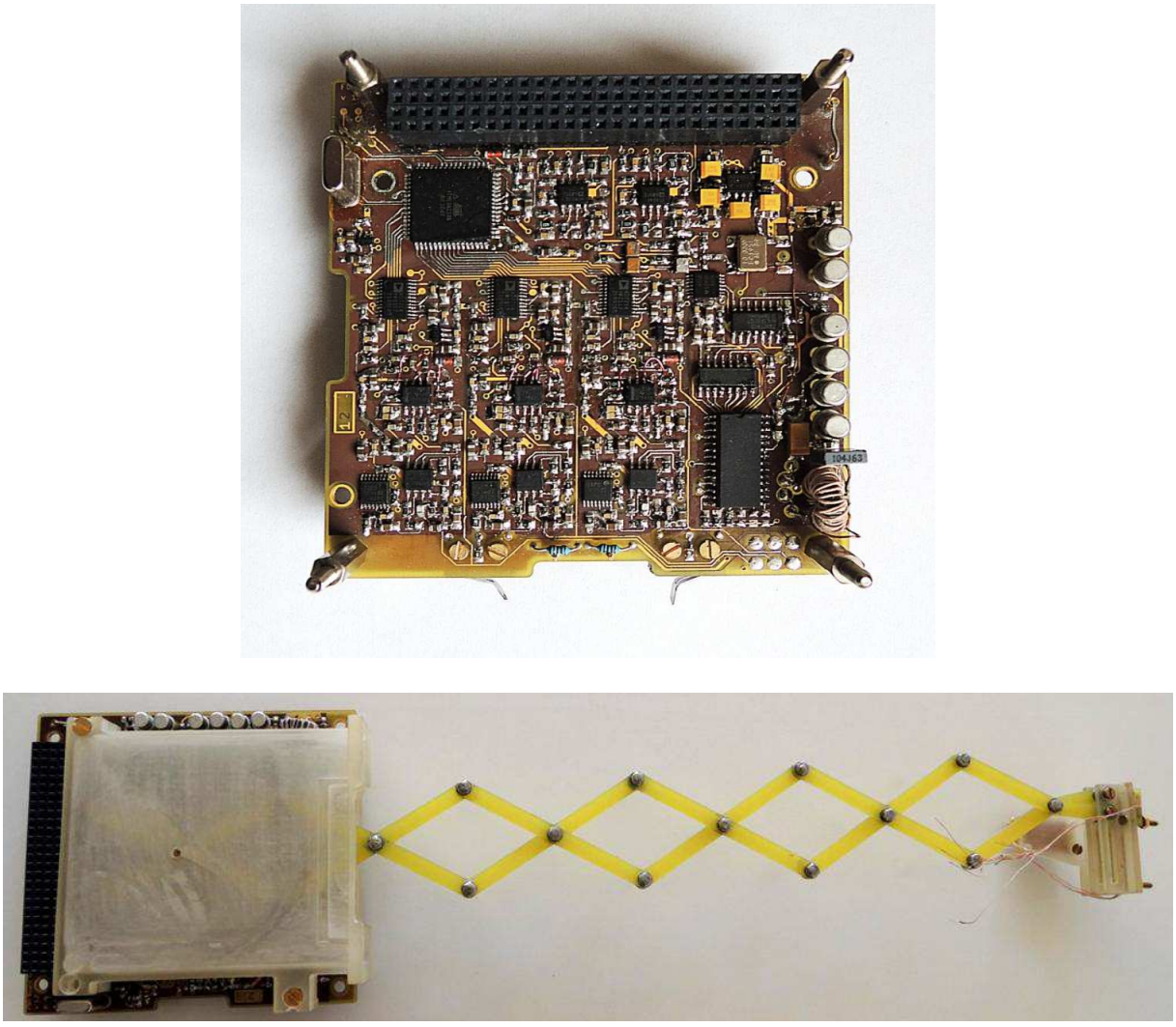


Fig. 32 Tri-axis Fluxgate Magnetometer electronics with FRAM based in-flight reconfigurable detection signal storage and BJT based H-bridge (Top), the scissor mechanism with the sensor head deployed (Bottom), Credits [MT-4].

5.2.2. *ESA / Lunar Lander / L-DEPP Project, LPM PoC*

A sensitive and ultra low leakage current-to-voltage converters as well as voltage sensing preamplifiers topologies have been adopted from already *TRL-9* design heritage to *PROBA-2/DSLP* and *ISL/DEMETER*. However, the current and voltage ranges were adjusted to cover wider span, since the Lunar plasma properties has not been investigated as detailed as for example in the case of the plasma environment close to the Earth. The project was conducted as a scientific study with a proof of concept deliverable for the *ESA Lunar Lander* mission (2011-2013).

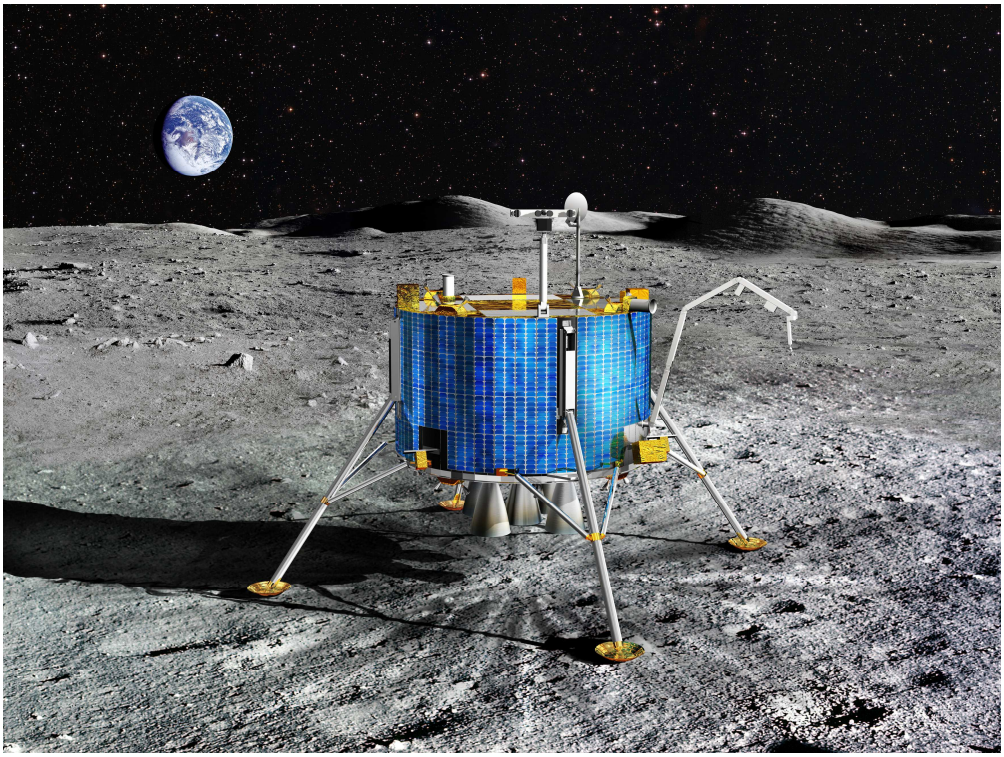


Fig. 33 The ESA Lunar Lander Mission conceptual study, [I-9].

The design of the *Langmuir Probe and Magnetometer* instrument - Proof of Concept (*LPM PoC*) was freed from the Magnetometer part, because of the need to test only the Langmuir Probe extended floating voltage potential concept. Thus, it implements off-the-shelf DC/DC converters as an alternative to the space-grade ones to power whole experiment from 18-36 V. The high-voltage DC/DC forward push-pull step-up converter with digitally (12-bit) controlled Bias Unit, microcontroller as a replacement for the control FPGA, two I/V converters and sweep circuitry driven by PWM-based signal isolators were designed. The *LPM PoC* also implements a housekeeping measurement such as internal temperature, reference voltage readout and main voltage measurement. Communication with PC, replacing the *L-DEPP Data Processing and Power Distribution Unit* is established via the USB-to-Serial cable and PC Control Software. Functional block diagram in Fig. 35 shows interconnection of above mentioned parts and gives overall concept summary.

5.2.2.1. *LPM PoC Electrical Design*

The measurement principle is the same as on *PROBA-2/Dual Segmented Langmuir Probe*. However, marginal changes have been done in the topology of the signal path and data acquisition chain. Previous design uses 16-bit ADC as an analog digitizer. This topology

cannot be used in the floating ground concept, since the preamplifiers and their outputs are not referenced to such ADC ground as is depicted in Fig. 34.

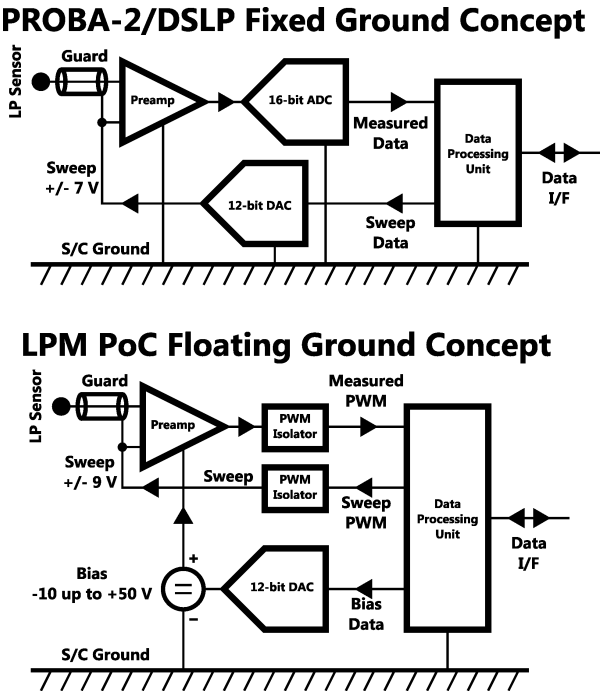


Fig. 34 Comparison of two different data acquisition chain concepts; Top: PROBA-2/DSLP fixed ground concept with a total sweeping range of ±7V, Bottom: LPM PoC Floating ground concept with an extended total sweeping range of -19 up to +59 V.

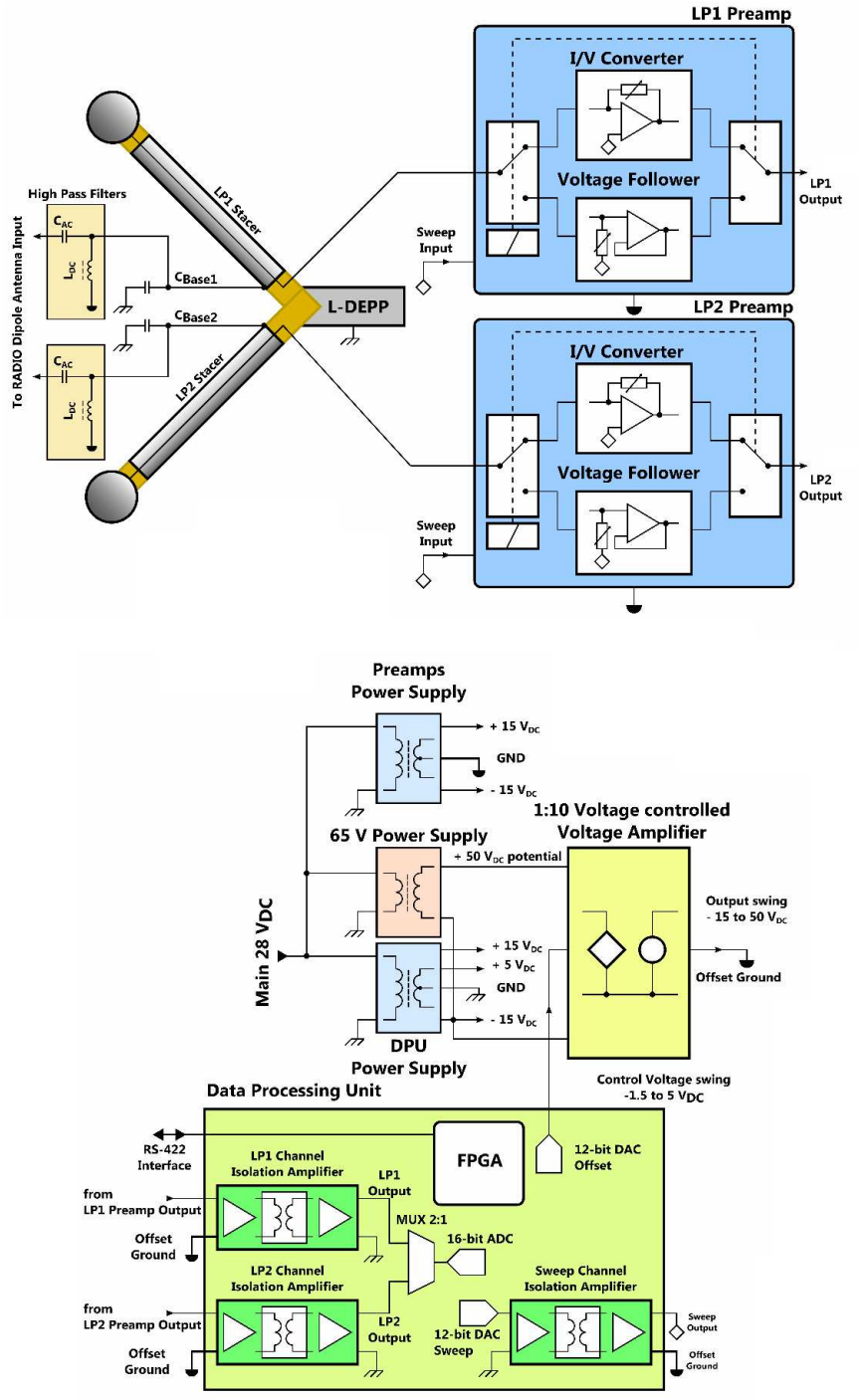


Fig. 35 LPM PoC Functional Block Diagram.

Following captures of schematic diagram show in detail the final status of the LPM PoC electronics. Critical circuits such as the Bias Unit was simulated to tune parameters of passive components before PCB assembly.

5.2.2.2. LPM PoC Low Voltage Power Supply

Three power supplies shown in Fig. 36 are separated from main power input by common and differential filters, in-rush current limiter, voltage sensing circuit and three DC/DC converters to produce main +5 V for digital parts and analog ±15 V for op-amps with

respect to main ground and second galvanically isolated ±15 V for floating potential circuits (floating I/V converters and V followers).

To minimize the noise at any integrated circuit in the design, the RC network is Hybrid DC/DC COTS converters are used as a substitution to space-grade converters already used on PROBA-2/DSLP. Future design could be based on the proprietary DC/DC converter with multiple outputs aiming to increase the conversion efficiency.

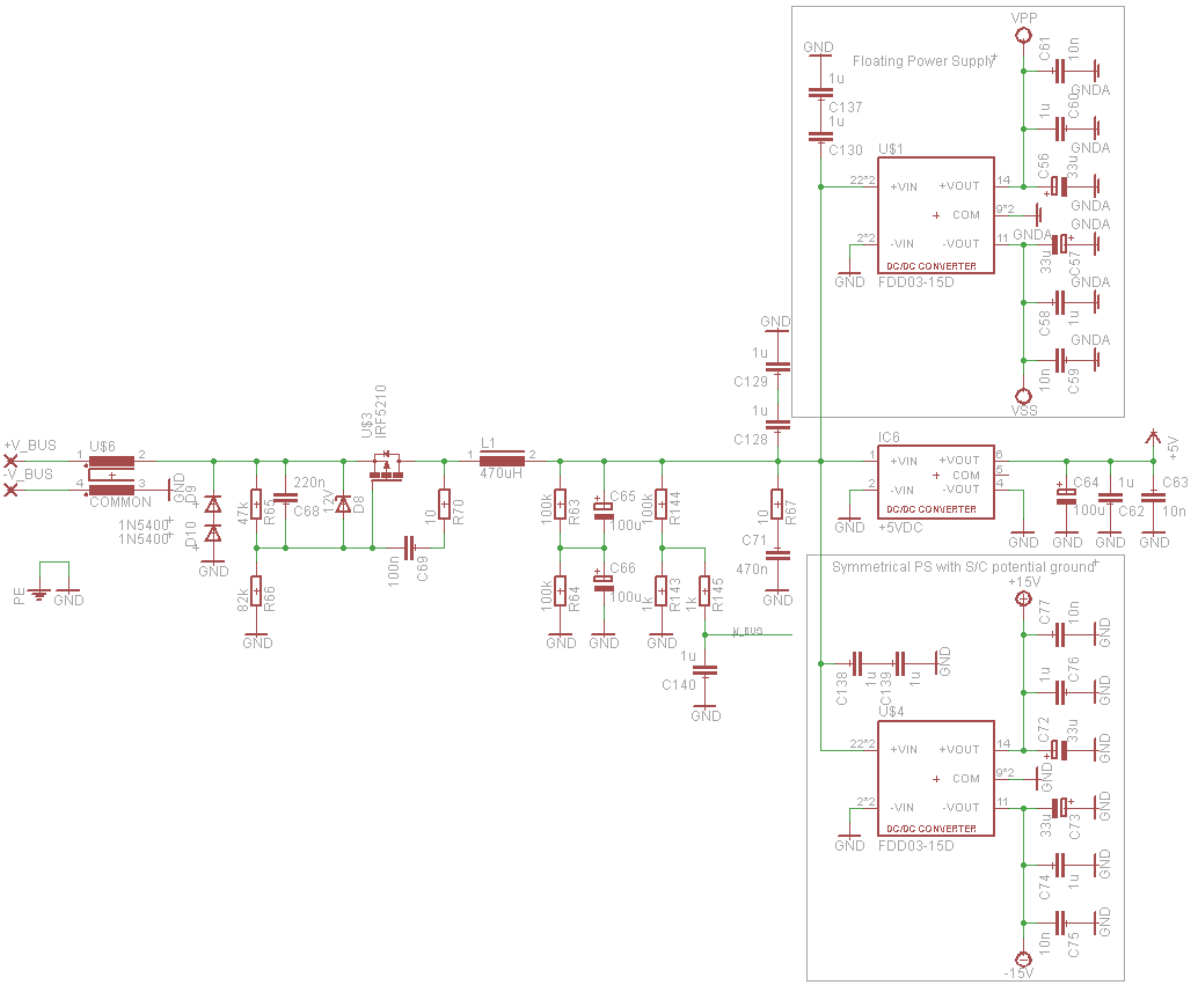


Fig. 36 Input filter, In-Rush Limiter, DC/DC converters and Main Bus Voltage Sensing circuit.

5.2.2.3. LPM PoC High Voltage Power Supply

The Bias Unit is powered by the push-pull forward DC/DC high voltage (Step-up) converter with *EFD-20* transformer (primary winding N_1 = 10 + 10, secondary N_2 = 140 + 140, copper wire with 0.15 mm in diameter, Ferroxcube ferrite core, type *3F3*) and two BJT drivers (Semelab LCC1 Rad Tolerant equivalent *2N2222ADCSM*, see Fig. 37) to prolong the operational lifetime and reduce cost. This implies also that very expensive Rad Hard MOSFETs in this stage are not necessary. High voltage converter runs with duty cycle of 50 %. This is achieved by the D-type flip-flops making this design very easy, reliable and space-saving. Switching spikes on the primary side are suppressed by the RC snubber (10 nF + 10 Ω) serving as a filter network.

Converter does not include any feedback, output voltage uncontrolled rising is reduced by the bleeding resistors connected to the bank of high voltage capacitors at the output. Next feature of this converter is frequency synchronization, which can be easily implemented in the

next L-DEPP project development stages within the FPGA. Currently the switching frequency is set fixed to 50 kHz.

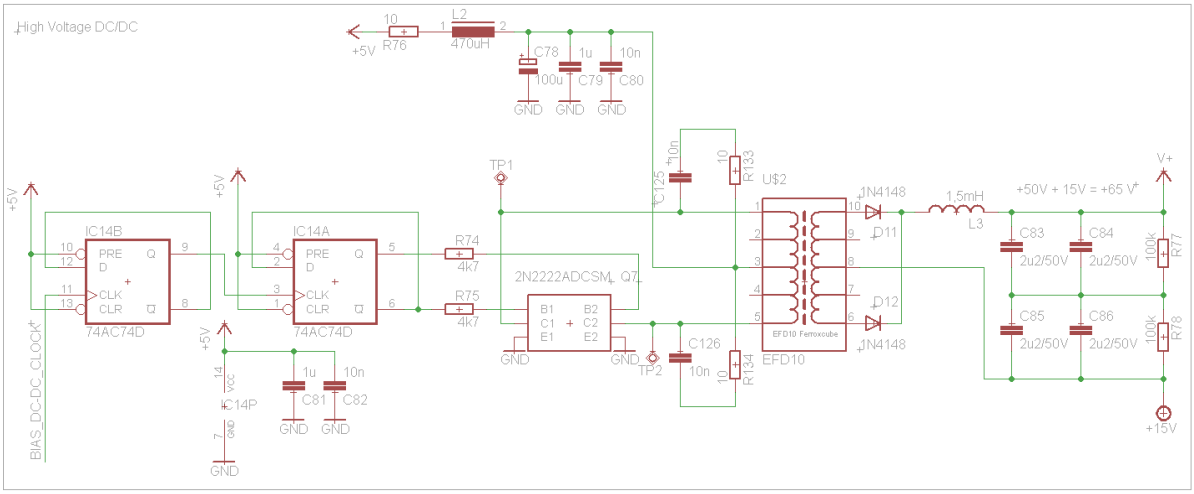


Fig. 37 Schematics of the High voltage DC/DC converter for LPM PoC Bias Unit.

5.2.2.4. LPM PoC Bias Unit

The core of the Bias Unit is based on the dual low noise op-amp *LT1024CN* (COTS substitution to space-grade Linear Technology *RH1013* Rad Hard op-amp) and high-voltage BJT power stage. High voltage, low current bipolar transistors *2N5415, 2N3439* were selected from the European Preferred Part List [R-21] to be compatible with Rad Hard versions intended for flight model. The BJT stage has a capability to control output voltage set on the DAC in order of tens of volts over the op-amp supply voltage range.

The circuit has been simulated and tuned manually to use E-series resistor values. Simulation scheme and input/output waveforms are summarized in Fig. 38. The simulation shows outputs from both op-amps *LT1024*. First (U3A) is connected as a summing amplifier, sum of control voltage (10 Hz sine wave generator with 2.048 V_{DC} offset and 4.096 V_{P-P}) and negative bias current derived from R12 and negative voltage source of -15 V. Output of the first op-amp serves as a driving voltage for the second stage (U3B) with high voltage bipolar BJT-based amplifier.

Even if the DAC output is only in the range of 0 - 4.096 V, the Bias Unit can handle the output voltage in the range of -10.2 up to +51.2 V, because of negative voltage adding and voltage multiplier (total forward gain = 15). Thus, bias voltage can be controlled with 15 mV steps (61.4 V range divided by the DAC 4096 steps). Overall electrical scheme of the Bias Unit, including 12-bit DAC, blocking capacitors and output LC filter tuned (cut-off frequency ~ 2.8 kHz) to attenuate DC/DC converters' ripple voltage, capable to operate at high voltages including discharging resistors is given in Fig. 39. Slightly positive feedback is included by the C2 (220 pF) capacitor to speed-up the response of the BJTs to increase the frequency response of the power supply ripple voltage.

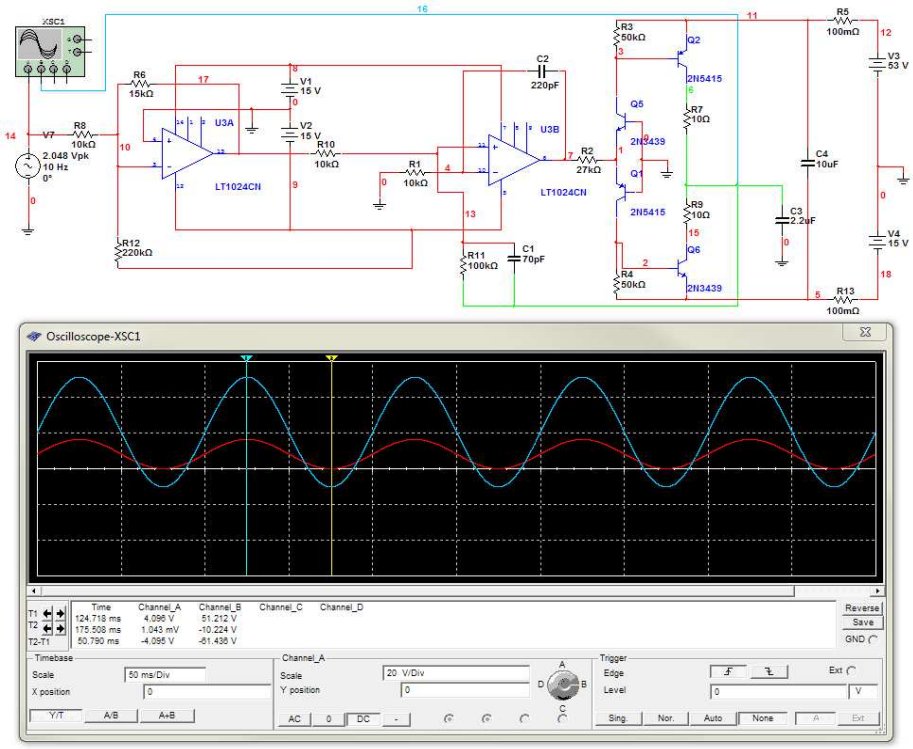


Fig. 38 The Bias Unit, BJT Boost Voltage stage circuit simulation, NI Multisim 10. Note amplitude of 4.096V (red trace) has a response of 51.2V (blue trace), zero input has a response of -10.2 V.

The Op-amp DC offset nulling resistors *R81-84* are implemented as pads on the PCB, but tuning resistors have never been necessary there. To decrease the Bias Unit output voltage ripple to a minimum, the RC filter R36 + C99 has been employed at the DAC voltage output.

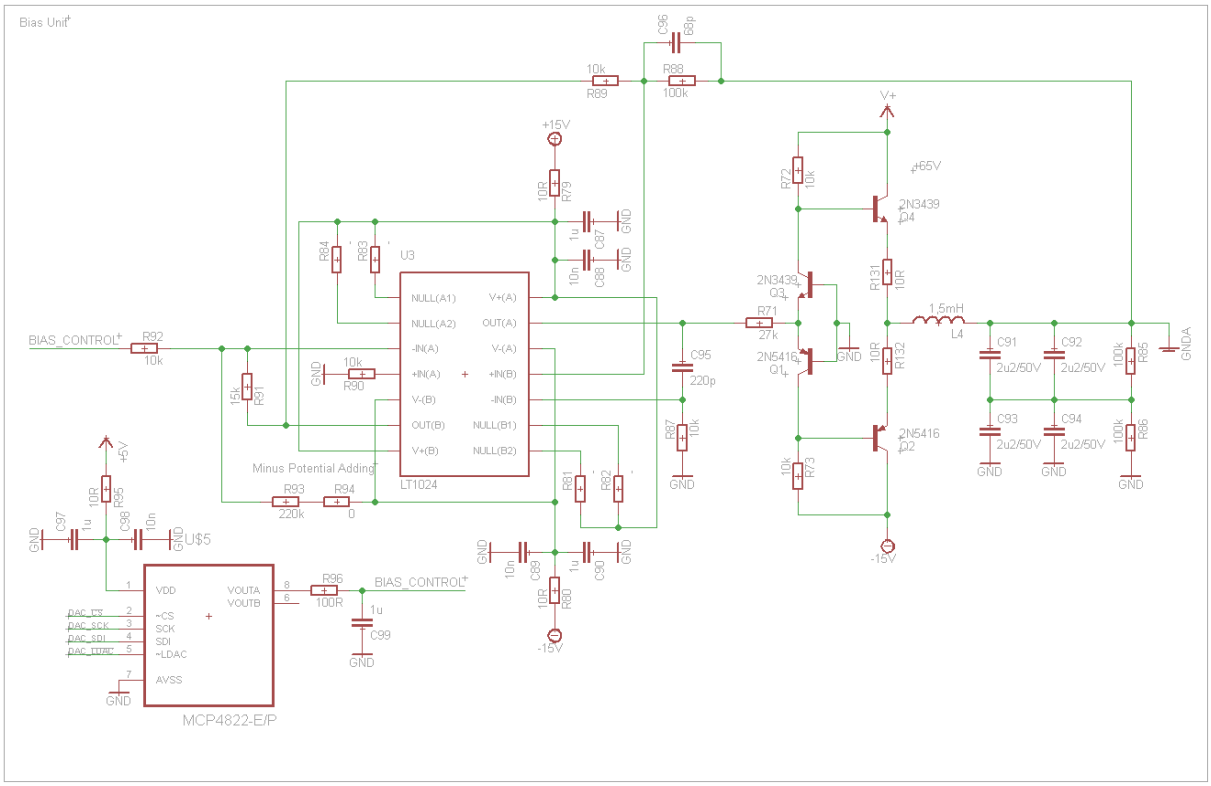


Fig. 39 The Bias Unit control block, including 12-bit DAC and LC high voltage output filter, note discharging resistors included.

5.2.2.5. LPM PoC Microcontroller

In Fig. 40 the *ATMEGA128A* microcontroller (MCU) is shown as a core for controlling whole LPM PoC board functionality. Running at 16 MHz, providing data throughput of up to 16 MIPS, the MCU controls the micro relays, DAC in Bias Unit and perform the housekeeping measurement including temperature and voltage sensing on main voltage bus and on external reference to check the analog voltage chain in terms of degradation in potentially radiation environment. The PWM-based predefined waveform (triangle wave) generation is one of the next MCU tasks as well as dual channel period and duty cycle determination (digital processing of preamplifiers output).

Regardless the used MCU is not intended to flight model (no Rad Hard either Rad Tolerant equivalent exist), this functionality (analog voltage chain self check) has been implemented to sustain high instrument reliability during entire LPM experiment development flow to maximize the scientific return of the L-DEPP in terms of working in harsh environment.

For future design, the FPGA is assumed to be used as a control core, combining LP data acquisition chain and Fluxgate magnetometer control logic and signal processing. A radiation tolerant, Flash-based version of the Actel ProAsic3 family, namely Actel *RT3PE600L* would be recommended. Development of the VHDL code and preliminary test of the period and duty cycle measurements have been done during the LPM PoC design period.

The communication interface is implemented as the TTL full-duplex single ended non-isolated serial bus with 115200 Baud, no parity, 1 stop bit, 8-bit data length format. Internal 10-bits Analog to Digital Converter (ADC) is used to sense the main bus voltage (divided by a factor of 101, see resistor divider R143, R144 in Fig. 36 and then RC filtered, see R145, C140 in Fig. 39), perform analog temperature sensor readout and reference voltage source self-check.

The ADC is referenced to external *AD580H* 2.500V precision voltage reference during the nominal operation. Output of this chip is filtered by the *R135* and *C104* RC filter. Reference voltage can be measured by the *V_REF* input directly (expected digital value readout is closest as possible to 3FFh, or the full range). Other value can be considered as a fault of ADC, because the input shall be the same as a reference, when everything runs properly. In the case of internal failure, the ADC reference can be switched to VCC (or +5 V_{DC}), then the 5 V output is connected to the *AREF* pin and thus connected as a voltage source against the “voltage sink” (5 V connected to the 2.500V *AD580H* output). To protect the reference against sink current overloading, the resistor divider is included, decreasing 5 V output by a factor of more than 2 (2.25, as a result of division by (1k5+1k2)/1k2) to get the output voltage less than the *AD580* output.

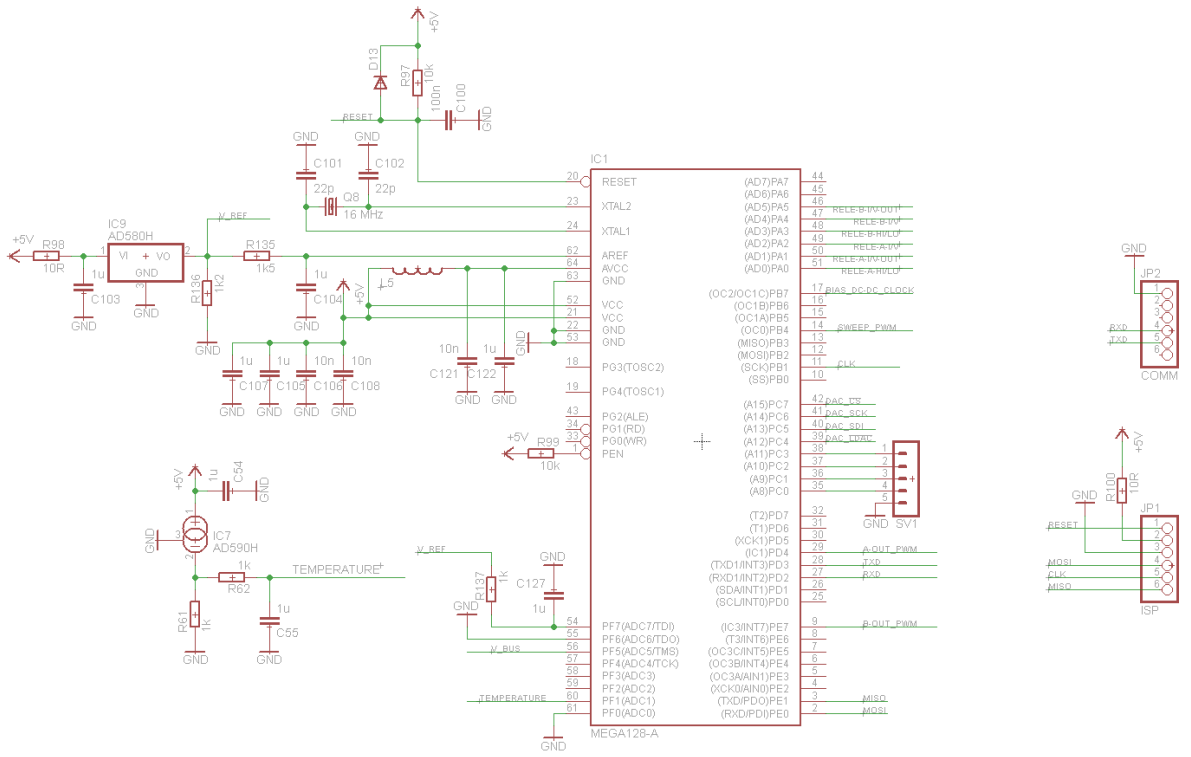


Fig. 40 The Microcontroller with the Housekeeping measurement inputs, temperature sensing and reference voltage readout.

5.2.2.6. LPM PoC Voltage Sweep Generator

To allow preamplifiers to sweep their virtual grounds (sweeping the potential between the probe and a floating ground) by a predefined waveform (typically a triangle wave) superimposed along the floating ground potential, the PWM-based sweep circuitry has been developed, including transformer-based galvanic insulation. A miniature complementary pair of *EPPL* selected BJTs *2N2907ACSM* and *2N2222ACSM* serving as current booster is driven by the PWM signal (SWEEP_PWM, see Fig. 41) from the microcontroller. Output of such push-pull amplifier is then fed via DC canceling ceramic capacitor to primary winding of custom-made pulse transformer.

Secondary winding is then attenuated by the R23 resistor to flatten the derivative shaped waveform and produce square wave output. One output is then referenced to a floating ground (analog ground, GNDA) and second output to the input of voltage limiting op-amp IC3.

Originally, on the *PROBA-2/DSLP*, the voltage sweep has been provided by the S/C ground potential referenced 12-bit DAC and dedicated op-amp, delivering sweep range approx. ±7 V only. Without the DC coupling, the sweep circuitry referenced to floating ground potential had to be realized in a different way. The PWM modulation is demodulated by a fast op-amp acting as a comparator and Zener diode voltage limiter. Combination of two anti-serially connected TVS/Zeners (Transient Voltage Suppressors) provides a temperature compensation, if they are intended to voltages around 6.2 V, since both thermal coefficients are almost the same for a forward and reverse bias with opposite polarity. Microsemi, Aeroflex or even COTS product *1N829A* has an excellent effective temperature coefficient of less then 0.0005% of threshold voltage per °C. Running at a switching frequency of 7.8125 kHz, these diodes are periodically switched and constant current driven to produce a temperature compensated and amplitude stable PWM. To get symmetrical „comparator“ output, the typical comparator without symmetrical push-pull stage cannot be used. This is

valid as well for use of the operational amplifier running from saturation to saturation (with the open loop). The slew rate and slope linearity is not so high to serve as a driver for the following low pass filter properly and the temperature or radiation derating can change the maximum amplitude obtained from this setup and then potentially also the recovered DC signal. Because the limited amplitude is far below the rail-to-rail voltage (approx. ± 7.9 V below, note the square wave amplitude is ± 7.1 V), the op-amp *OPA602* is then fast enough to drive it, since it does not require full 30 V_{PP} swing. Amplitude stability is the most important aspect for a proper function of this topology. Then the square wave is filtered and amplified to produce desired sweep waveform and amplitude with sweep frequency of 1 Hz. This signal is present at *SWEEP_Recovery* signal.

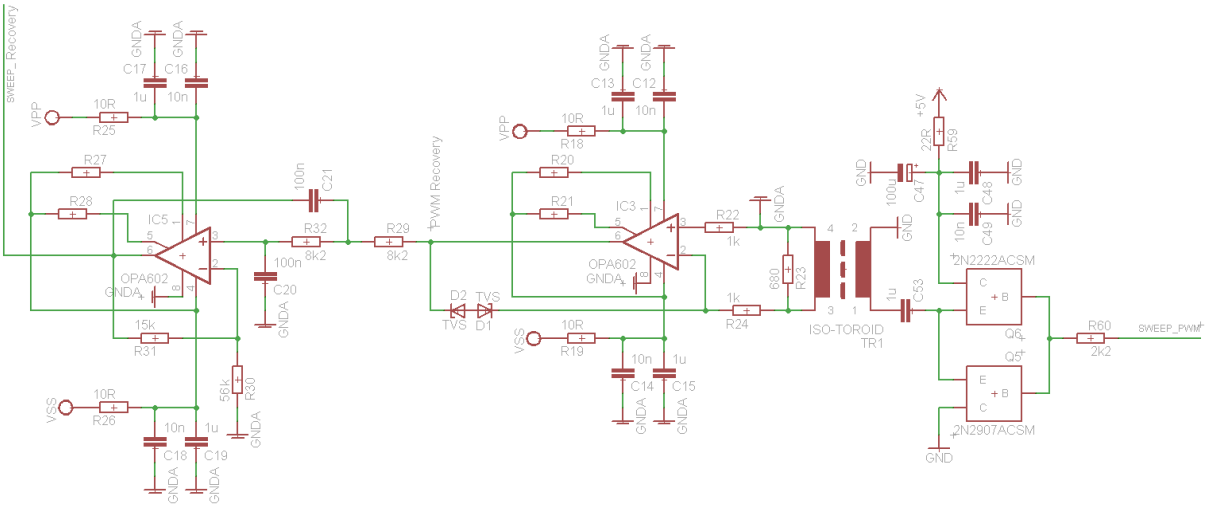


Fig. 41 The PWM-based transformer-insulated and thermally compensated voltage sweep circuitry.

The triangular waveform is composed of 240 binary samples calculated in MCU, repeating period is then 1 second. With the PWM frequency of 7.8125 kHz, each sample (dedicated PWM duty cycle) is held for approx. 4.1 ms (1/240 samples) or 32 PWM periods during which the data acquisition chain has a time slot to proceed the measurement. The example of the low-pass filtered triangular wave pattern generated by the sweep circuitry based on PWM generator is displayed in Fig. 42.

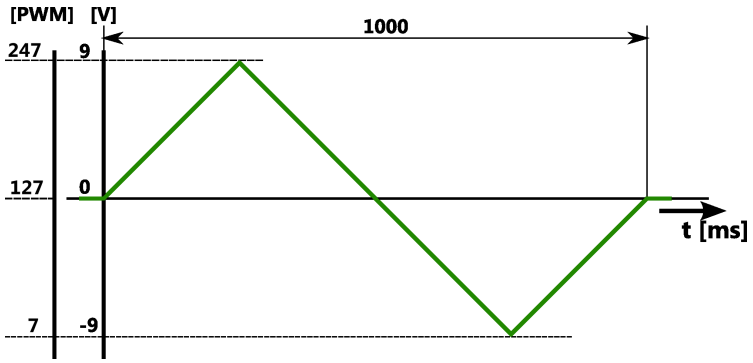


Fig. 42 The Triangular waveform pattern used for voltage sweep, single period, composed of 240 8-bit PWM samples, note: x-axis in ms, y axis in Volts and PWM duty cycle value of 0 - 255.

5.2.2.7. LPM PoC Preamplifiers 1 & 2

There are two identical preamplifier units depicted in Fig. 43 and Fig. 44, combining I/V converters (plasma current sensing) and voltage followers (plasma potential with respect

to massive Lunar Lander spacecraft body). Tens of femtoampere-grade op-amp *OPA128J* is used to minimize the input current leakage influence on very small current sensing measurement. Signal from LP sensor is connected via *LP-A(B)-LIVE* pin through input mode selector realized by the miniature TO-5 package *Teledyne 735D-5* relay. To simplify the concept, latching relays are not used. However, their utilization have to be considered for future LPM instrument development mainly to minimize power consumption and heat dissipation. Since the LPM requirement is to handle ± 200 V, it was decided not to change the relay provider nor relay family except to change the double pole double throw (DPDT) with internal recovery spring to a latching (bistable) DPDT version.

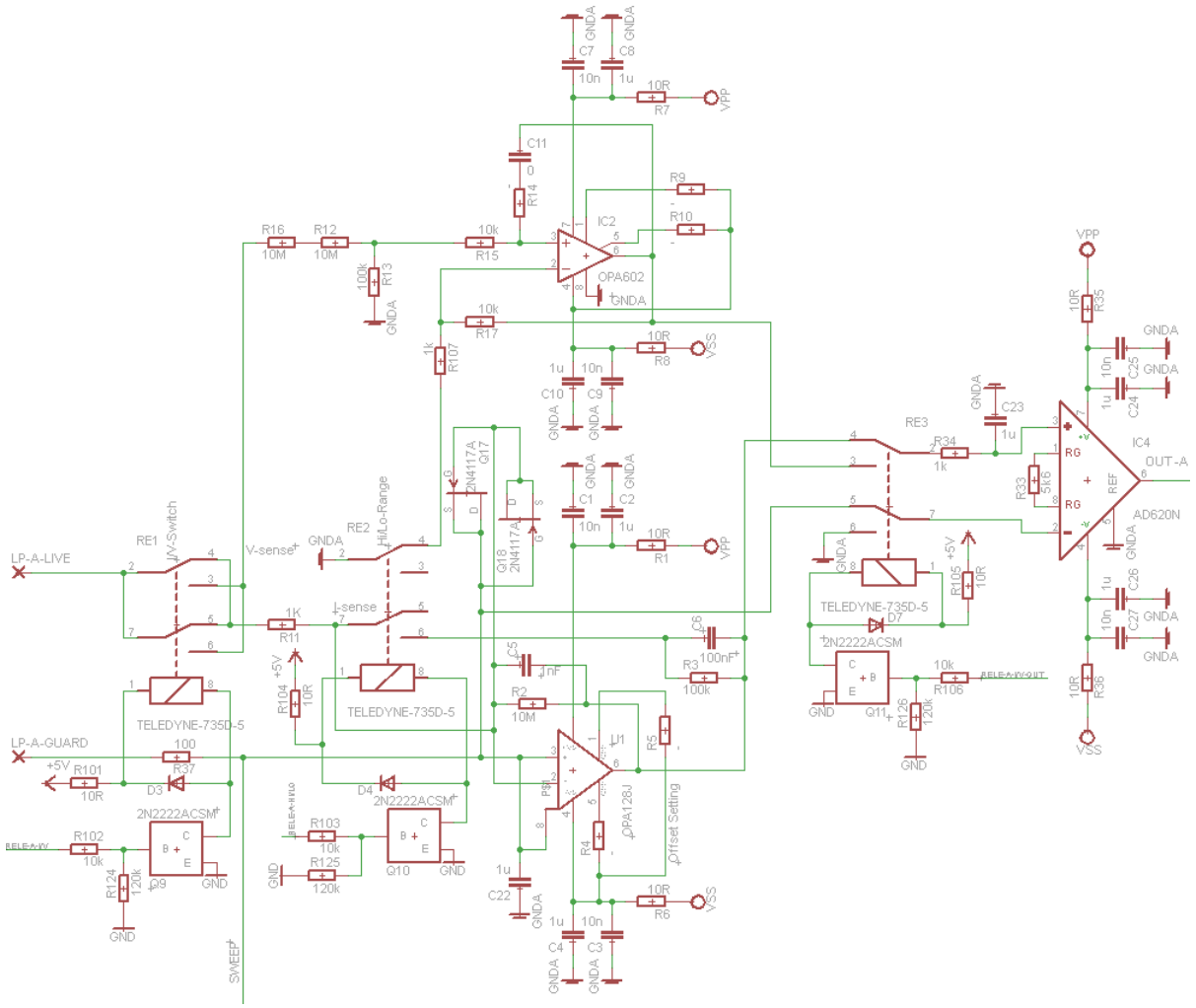


Fig. 43 Channel-1 of the LP preamplifier, Current-to-Voltage converter and Voltage follower, relay switches and instrumentation amplifier circuitry.

The signal for I/V converter is protected by 1 kΩ resistor to reduce potentially high currents able to damage op-amps. Input is then fed directly to negative input of *OPA128J* amplifier. To protect whole I/V converter against hazardous currents (order of mA) two ultra low leakage *JFETs* (0.2 pA typ.) are employed based on application note provided in RD8. Here, working in diode mode (junction to drain and source) transistors serve as an over-voltage shunt protectors. Harmful currents from LP_A(B)_LIVE input are bypassed throughout 1 k∧ resistor (R11 in Figure 11 or R118 in Figure 12) then via mentioned JFET diodes down to Sweep Generator output op-amp *OPA602* (IC5 in Figure 8) referenced to the Bias Unit floating ground potential. Since JFET gate diode current can be operated up to a maximum of 50 mA, the Bias Unit sink current is limited by the inductor maximum current

(100 mA) and BJT stage current rating of a maximum of 1 A, the main current overload criterion is the maximum output current of the OPA602 which is defined as ± 25 mA.

Because the whole analog chain is considered as a bipolar (processing of positive and negative currents) JFETs are used in anti-parallel configuration to protect each other from negative voltage gate breakdown destruction. Hard limit for preventing the *LPM PoC* against damage is thus defined as ± 25 mA as a sum of currents on LP Live and Guard for each A/B channel and ± 250 V wrt. S/C ground.

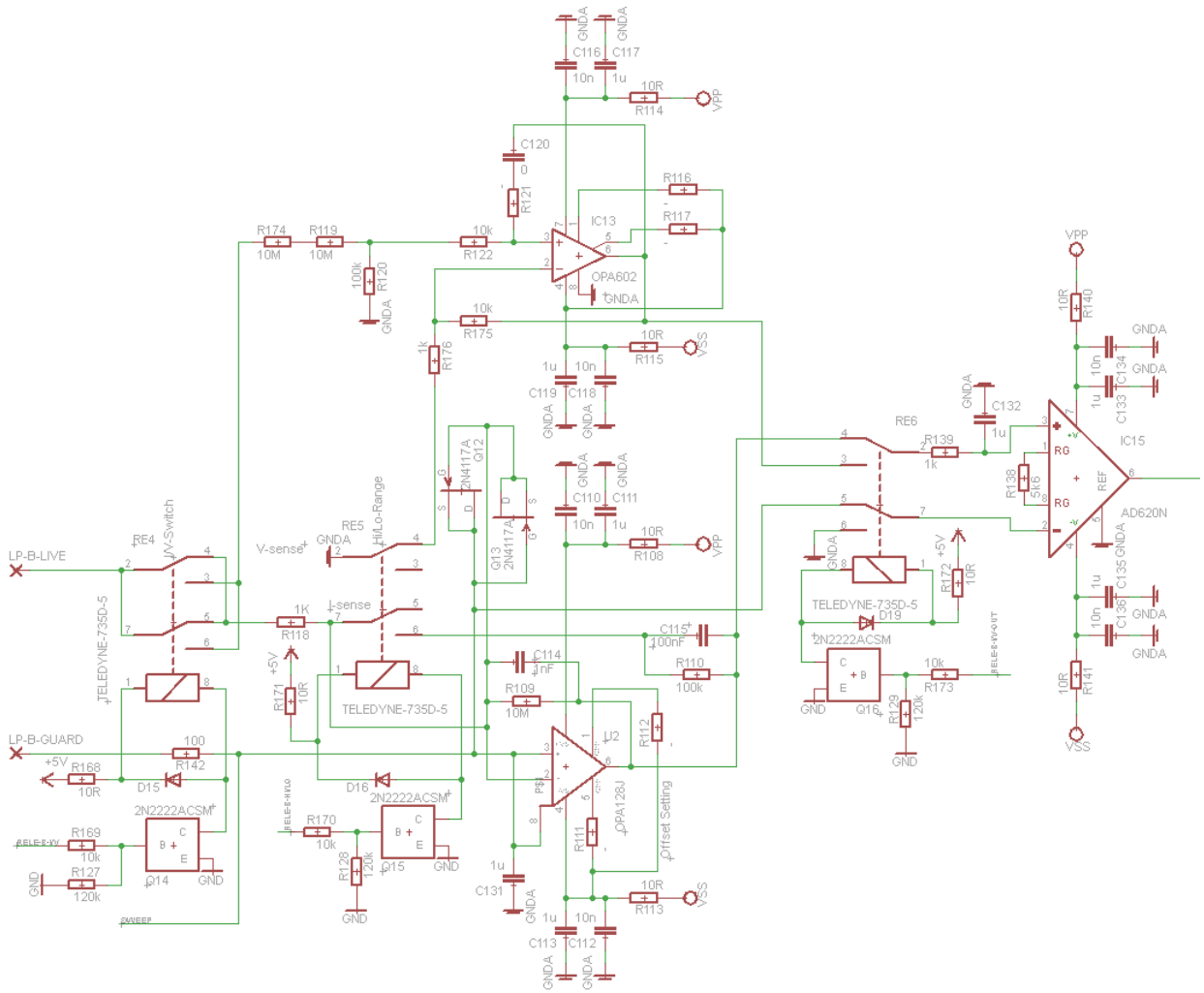


Fig. 44 Channel-2 of the LP preamplifier, current-to-voltage converter and voltage follower, relay switches and instrumentation amplifier.

Two different gains could be selected via relay switch. High gain fixed feedback resistor (10 MΩ) is bridged by the low gain one (100 kΩ) with relay contact. Gain switching between high and low without any fixed connected current path should cause charge accumulation and potentially current overloading of the preamp during mechanical movement of the switch.

To suppress the noise two capacitors are added to this resistive feedback, 1 and 100 nF respectively. Because the output of the I/V converter is proportional to a sum of sweep and measured current converted to voltage, the sweep potential has to be subtracted and then multiplied by the instrumentation amplifier *AD620AN*. Total range of the signal after sweep subtraction is just ±1 V (the range of the I/V converter at maximum gain and maximum allowed input current defined by feedback resistor). This is to keep the *OPA128J* in non

saturated region (note the sweep range is ± 9 V, signal ±1 V, ±10 V in total). The gain is set by the R_G resistor to be close to 10, by the E-series value 5600 Ω, the final value is then A_U = 9.82. High output swing of the instrumentation amplifier is necessary to reduce the noise superimposed to signal, because such trimmed signal is then used to be modulated using the PWM.

The voltage potential measurement chain is similar, but based on high impedance input resistive divider (factor 1:201) with total input impedance (excluding the ultrahigh impedance of the DiFET op-amp equal to 10^{13} Ω) close to 20.1 MΩ. Here, the analog chain is still upper-limited by the relay breakdown voltage of 250 V_{DC} but the input resistive divider and op-amp circuit are capable to operate up to an order of thousand volts, depending on breakdown voltage of the input MDM-25 connector, and electrical strength of the PCB and divider resistors. Output voltage is then fed directly to non inverting input of the instrumentation amplifier. Inverting input is referenced to floating ground (GNDA). Mode selection is realized by the third relay switch. Several additional pads for tunable components such as DC offset correction or feedback loop tuning were prepared to improve the system quality, however the op-amps performed well enough, so most of these parts were not necessary during design and testing period.

5.2.2.8. LPM PoC Isolation Amplifiers

The measured voltage referenced to a floating ground potential is necessary to be insulated between the floating potential ground and system ground, transferred for processing and digitized. There are two possible solutions: an optical or magnetic signal separation. No optical or magnetic-based isolation amplifiers were available on the Radiation Tolerant/Hardened semiconductor market. In April 2013, the Intersil company announced High Rel/RH Space Product Roadmap where introduces the *ISL71901SEH* chip as an intended concept of radiation hardened development with beginning in 2014. It should be an upgraded version of the *Texas Instruments UC1901* feedback generator which is used as a transformer based Isolated Feedback Generator delivered in industrial and military grade. However, the RH qualified version or equivalent is not available. The proprietary solution had to be developed, introduced, implemented and tested.

The signal obtained as the output of the instrumentation amplifiers (either A or B channel) is used as a reference in comparison with the triangular wave periodically generated in the astable flip-flop circuit. Then the fast op-amp is used as an analog comparator which then feeds the primary side of the isolation transformer. Square wave PWM modulated signal can be transferred to the secondary side, where is recovered by the second comparator – here the digital comparator, with TTL output. Demodulation is based on digital signal processing, not by the AD conversion of the low pass filtered PWM signal.

Precision, high voltage swing triangle wave generator has been designed as a two stage “window comparator/integrator” flip-flop. The amplitude is determined only by the Schmitt trigger resistors connected into positive feedback. This comparator based on *LT1056* produce a full swing square wave which feeds the next stage – an active integrator based on the same precision and high speed op-amp. Because the trigger operates with a limited bipolar voltage window, the integrator will never reach both rails (+ or – 15 V). Thus, this circuit is well tolerant in terms of the radiation damage. Capacitor aging and its capacity changes (decrease or drift) can cause the frequency drift which is then canceled by the digital signal processing further described at the end of this chapter. The duty cycle is determined by an internal MCU clock sampling method, where the measured signal is slower than system clocks (order of MHz) and acts as a gate signal. With certain bit precision (order of 12-16 bits) the measured signal frequency have to be in order of kHz. The lower the PWM

(triangular waveform) frequency is, the better for high speed clock gating and the bit precision, but the worse for signal isolation over the ferrite transformer core (FERROCORE ferrite ring core, type *TF12x4x6*). Slow PWM means less time to proceed oversampling and worse conditions for overall system response time. Theoretical lowest PWM frequency with oversampling factor equal to 1 is 240 Hz. This follows from 1/240 samples per second during single sweep period measurement. However, such low frequency is hard to feed to the transformer with maintaining the square wave shaping needed for proper function of the TTL comparator. The inductance play a significant role here, thus the compromise has been chosen between the transformer core (ferrite), number of turns, power consumption and volume with respect to PWM sampling clock speed (2 MHz), 16-bit precision and oversampling factor of 16. Primary inductance is equal to 18.8 mH, secondary to 1.26 mH. The PWM frequency has been chosen to be close to 5 kHz ± 25 % (depending on passive components drift). The simulation circuit, wave form plot and a measured frequency is given in Fig. 45.

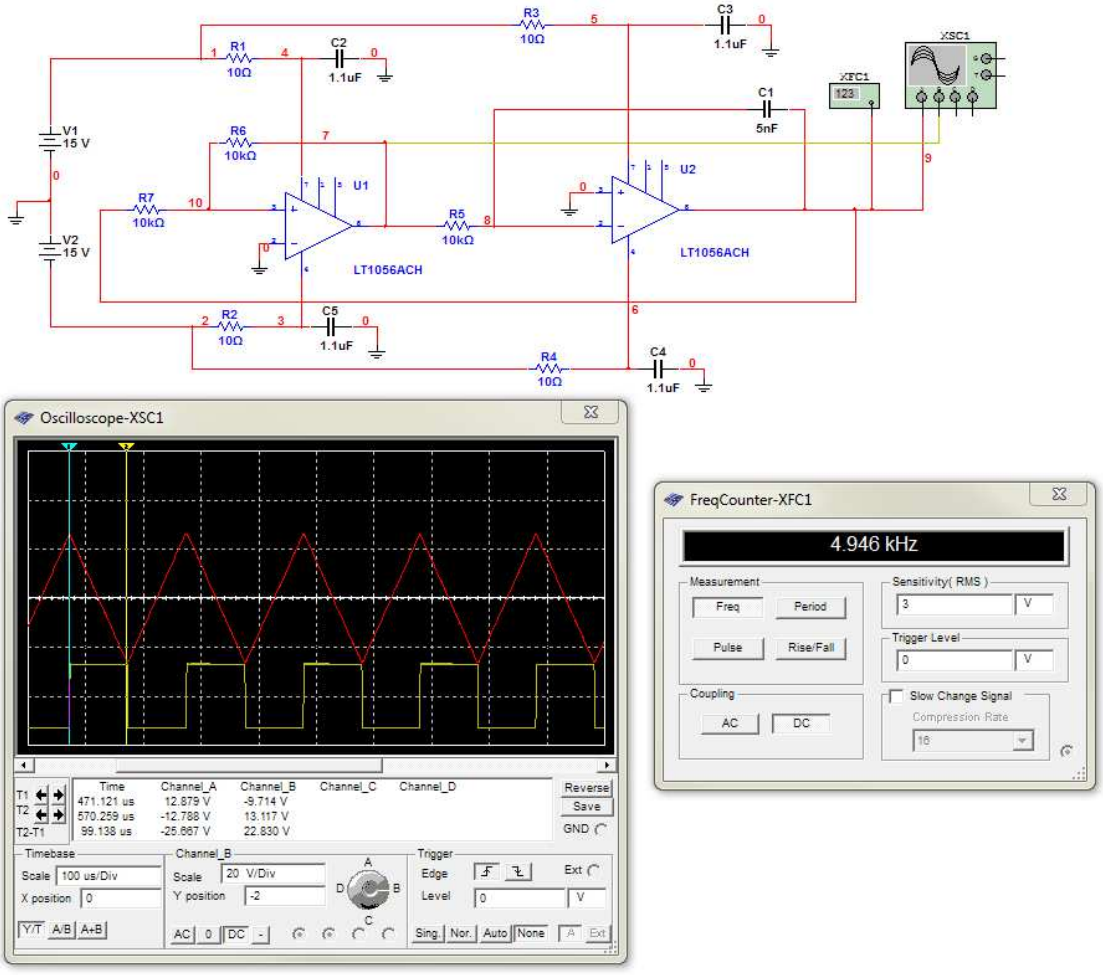


Fig. 45 The Triangular waveform generator with constant amplitude referenced to a floating ground. Frequency set close to 5 kHz.

As it is graphically mentioned in Fig. 35, low frequency outputs from both preamplifiers (either running in V/V or I/V mode) are compared with a triangle wave generator referenced to a floating ground potential (i.e. to the same ground as preamplifiers). Comparison between these two signals (triangle, measured) is done in a full-swing, open-loop running op-amp LT1056. Product of this comparison is then fed via the current limiting and DC-cancellation RC network to the primary side of the isolation transformer. The PWM product is then transferred to the secondary winding where it is freed from spikes by a

resistive attenuation and referred to the threshold level of the recovery comparator AD8561.

The practical implementation of the triangle wave generator matched with the comparator, low-pass filtered signal from Channel-1, isolation transformer and comparator with resistor-defined threshold voltage reference is depicted in Fig. 46, the same situation utilizing signal from the Channel-2 is provided in Fig. 47.

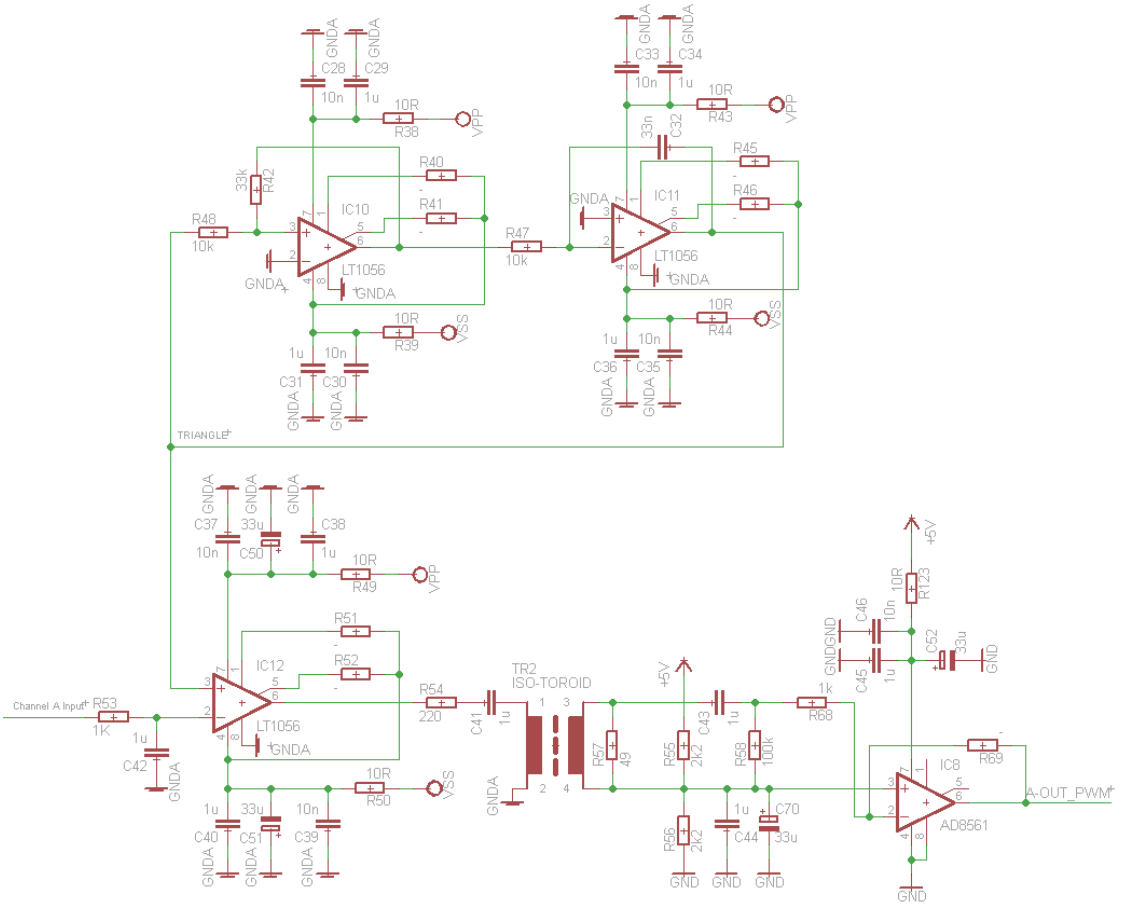


Fig. 46 The Channel-1 PWM isolation amplifier, including triangle wave generator.

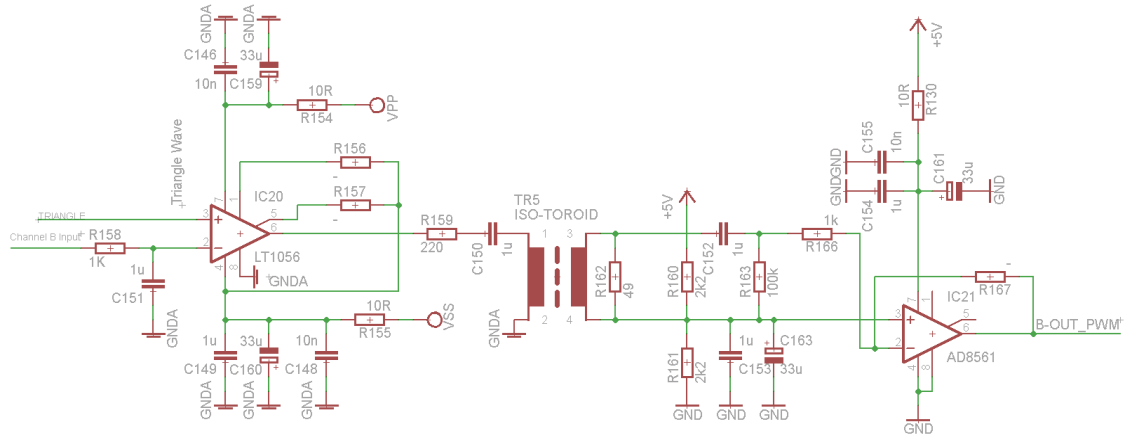


Fig. 47 Implementation of the Channel-2 PWM isolation amplifier.

Both channels' recovered output trimmed to the TTL levels are connected to the MCU timer inputs, where are processed in terms of determination of the duty cycle. Two different periodical signal parameters (turn on time and period) are measured to ensure that the triangle

wave generator frequency shift or signal jitter caused by i.e. thermal drift, supply voltage changes, radiation damage, passive components aging, etc., as is depicted in Fig. 48, will have a minor effect on the duty cycle precision in determination of the useful signal from preamplifiers. Thus a ratio between time length of the log. 1 state (time t_{on}) and the whole PWM signal period (time T) including the log. 0 is determined and the duty cycle factor D then calculated by a formula: $D = t_{on}/T$.

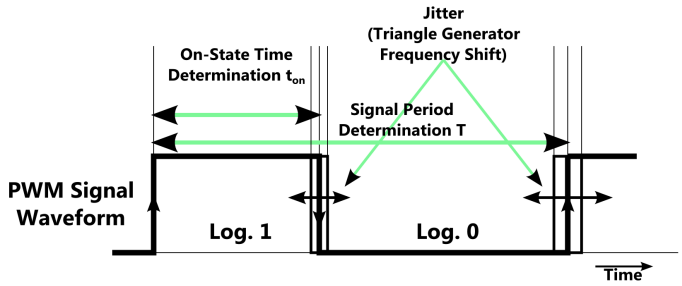


Fig. 48 On-State Time and Period determination definition.

5.2.2.9. LPM PoC FPGA Firmware Design and Digital Data Processing

In parallel with the LPM PoC hardware development, the VHDL routine for commercial equivalent of proposed *Actel/Microsemi FPGA A3PE1500*, was developed to demonstrate the PWM demodulation, duty cycle determination stability and overall implementation of digital signal processing. The VHDL project benefits from the available *Actel/Microsemi IP cores* (UART, logic gates) and signal demodulation hardware description has been realized. Hardware implementation including short cable loopback, *USB-to-Serial* cable and FPGA kit is shown in Fig. 49.

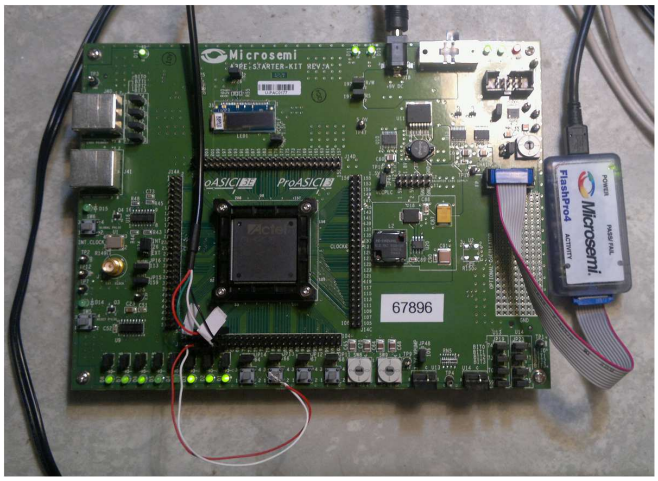


Fig. 49 The Microsemi A3PE Starter Kit, JTAG Programmer TTL UART to USB cable and loopback connected to determine duty cycle of internally generated PWM signal.

The VHDL firmware counts lengths of active pulses (log. 1) and measures PWM signal period, both then sends via UART interface to the upper level (PC). The measurement principle is based on two periods of investigated PWM signal. Time of log. 1 is determined as a gating of very high speed system clock obtained in PLL by multiplying external 40 MHz clock up to 260 MHz. Value of 16 bit counter is stored to 16 bit latch during falling edge. Delay block is inserted between the asynchronous counter clear signal and measured PWM signal input. Therefore, counter can be periodically filled, value stored and then cleared periodically, without lost of counted value.

The same principle of positive pulse time detection is used for PWM signal period. For system robustness, the period is obtained by edge-synchronized D flip-flop, connected as a frequency divider by a factor of two. Thus the PWM signal is divided, thus period is equal periodically to positive and zero states of divided signal. Using the timer gating method as in the case of duty determination, two values are obtained after two original PWM signal reception as is described graphically in Fig. 50.

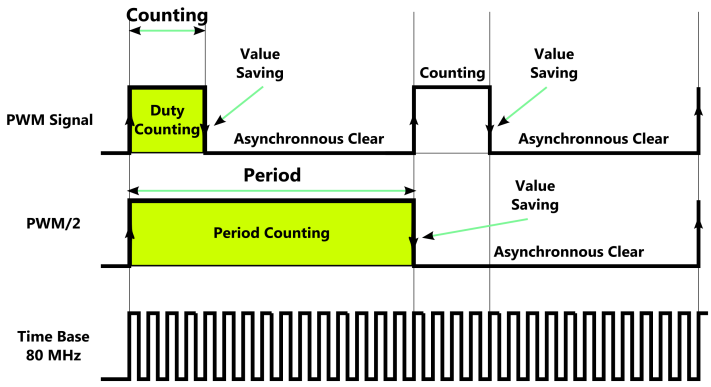


Fig. 50 The Logic 1 Duty-cycle and Period length determination example. The timebase is displayed not to scale.

The Duty Cycle Counter and Period Counter are implemented with logical gates, D-flip flop divider and capture (latch) registers and maintains the actual value here every two periods of input PWM signal. If there is no log. 1 on the input, the system still sustain the last value. Values are divided each to the two eights, low and high byte capture registers.

Then the state machine is represented by periodical three bit wide counter providing periodical readout addressing between latching registers, eight channel multiplexer and UART IP core parallel input. Sending of data is realized while the TX Ready signal allow the rising edge clock synchronizer represented by the D-flip flop to produce a single pulse. Then the flip flop is cleared again by the Not TX Ready signal occurred when the UART blocks start of the serial data transmission.

The Lunar Plasma Monitor given in Fig. 51 as a result of L-DEPP Definition Study has been realized introducing a reliable Floating Ground Potential Concept for high voltage range plasma environment measurements intended for the *ESA/Lunar Lander* mission.

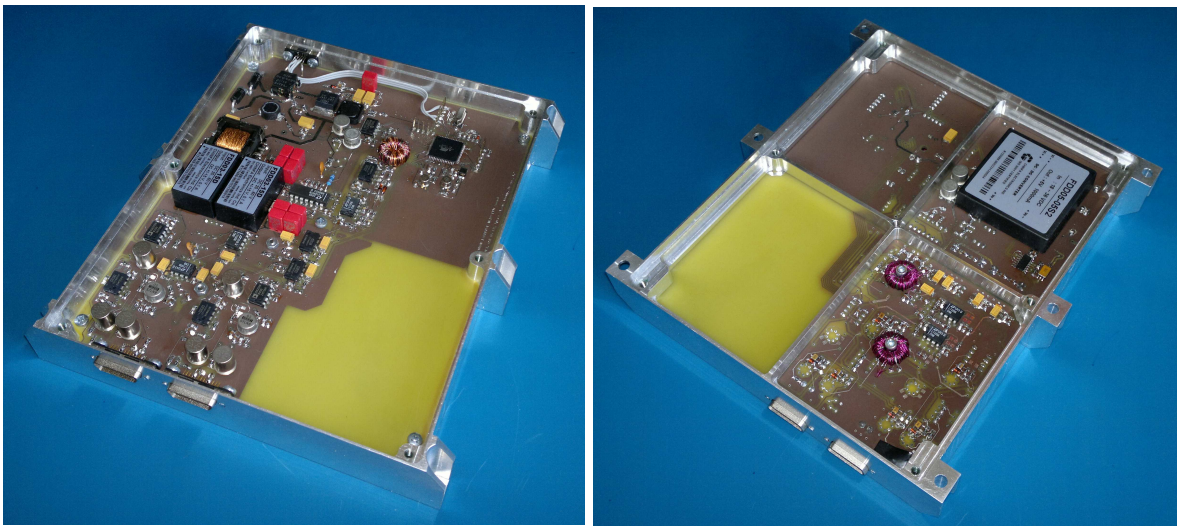


Fig. 51: The L-DEPP Definition Study result, Lunar Plasma Monitor Floating Ground Potential Proof-of-Concept.

5.3. Objective C)

The third objective of the seven years of development and research was to develop the cold-redundant, ultra low noise and reliable *Low Voltage Power Supply (LVPS)* unit intended for the 10 years long interplanetary mission *ESA / JUICE* in Fig. 52, [I-10] as the part of the *RPWI* instrument.

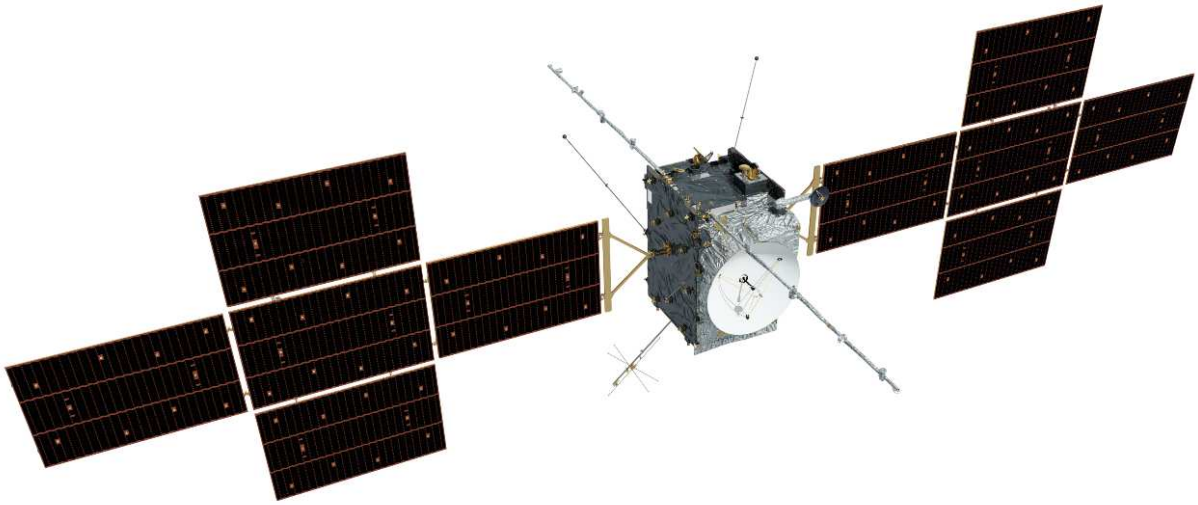


Fig. 52 The ESA JUICE Spacecraft with several instruments, including the RPWI package and associated antennas, [I-10].

The *Radio and Plasma Waves Investigation (RPWI)* instrument is intended for in-situ plasma and radiofrequency spectra sampling to study the second biggest magnetic field in the Solar system and its influence on plasma particles, movement and interaction. As one of the onboard instrument (the Fluxgate magnetometer) is planned to measure sub-surface currents induced by salty water under the ice crust on moon Ganymedes, the whole LVPS have to be composed of electronic components with minimized magnetic dipole (i.e. minimized amount of relays with permanent magnets). It shall be designed to withstand *50+ krad(Si), LDR*.

The LVPS have to convert, condition, control, monitor and distribute electrical power to the RPWI units depicted in Fig. 53 from two S/C unregulated 28 V buses. It shall be designed to be able to work without damage with both buses powered on, with ability to internally switch-off the dedicated bus line upon command. Short circuit protection of dedicated loads or on/off switching shall be maintained autonomously via implemented *Power Distribution Unit* (*PDU*) and controlled via telecommands via *Data Processing Unit (DPU)*. The LVPS shall implement a common source of high frequency (50 MHz) synchronization clock signal to be distributed to all subsystems. The LVPS clock synchronization and switching frequency synchronization together with housekeeping measurement shall be realized within the FPGA softcore to optimize the self-generated emissions, as multiple harmonics or clock random walk would lower the dynamic range and noise floor of measured spectra, when fed to ADCs.

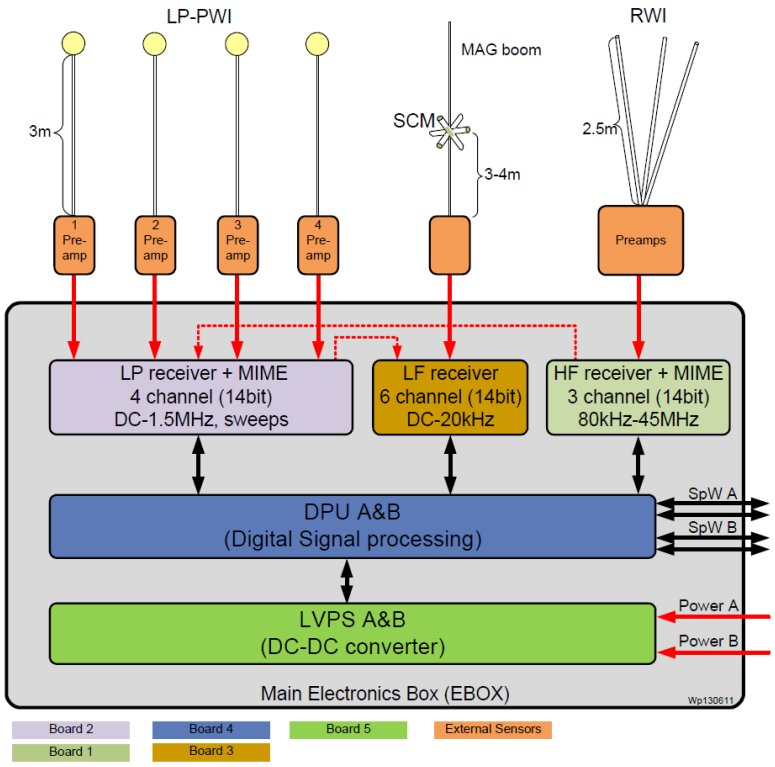


Fig. 53 The Radio and Plasma Waves Investigation instrument Block Diagram. Two Cold-Redundant LVPS power the Cold-redundant Data Processing Units, Low Frequency receiver (LF), Langmuir Probe receiver (LP) and Mutual Impedance Measurement Instrument (MIME) , High Frequency (HF) receiver, Search Coil Magnetometer (SCM) and sensor preamplifiers.

5.3.1. RPWI LVPS Topology

The *RPWI* power generation is secured by the dedicated Low Voltage Power Supply, comprising of two independent, fully cold-redundant DC/DC converters isolating the S/C *Power Conditioning and Distribution Unit (PCDU)* out of the RPWI subsystems power inputs, Power Distribution Unit and Housekeeping Monitors (voltage, current sensing on secondary side of the converter). The concept of the LVPS is given in the block diagram in Fig. 54.

The converter is based on the first stage step-down converter (Buck regulator) serving as a stable voltage feed for the push-pull driver of the main (and/or redundant) power transformer. Thus the assumed converter topology is called Voltage-Fed Push-Pull Converter. The push-pull stage is fed with fixed duty cycle assuring stable operations, low noise (not changing duty cycle) and also decrease the current loading of the output rectifiers which are working up to 100% of duty cycle (~50 + ~50) with small dead time introduced to prevent shooting through currents. Dead-time is in order of 300 ns and is realized using RCD network and AND gate circuit. Fixed duty cycle is assured using D-type Flip Flop.

Output switches are protected using current mirrors reacting to voltage drop at current sensing shunt resistors. In case of high voltage drop, the current mirror pull the output FET pair to off state. To avoid output FETs burnout during linear conducting mode, the current is also digitally read-out using FPGA core and ADCs with BW of ~1kHz. For this purpose the same shunt resistor is used for two purposes to prevent additional power losses.

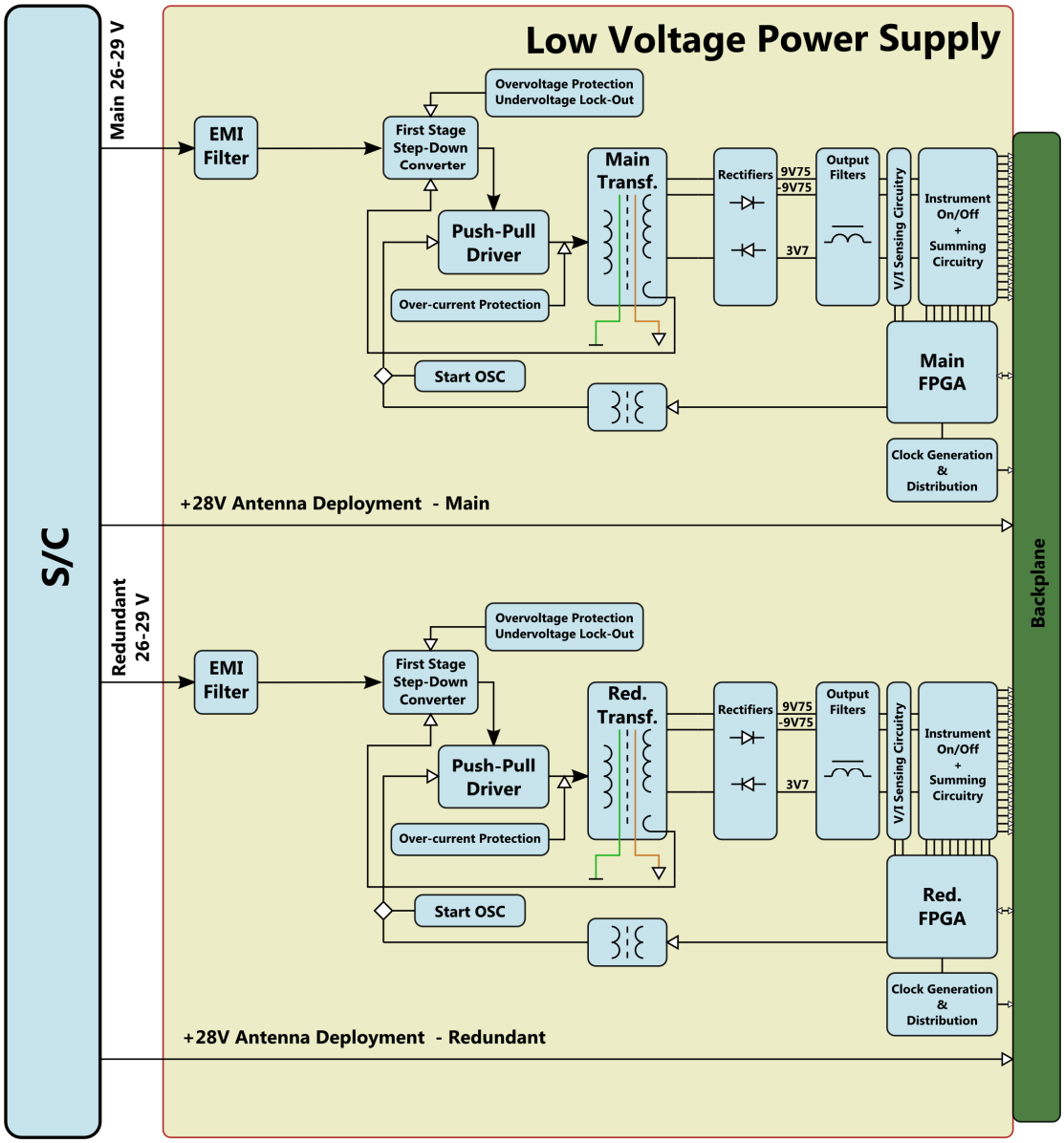


Fig. 54 The RPWI LVPS Block Diagram.

Two cold-redundant LVPS power converters contain power switches to fulfill On/Off function for dedicated lines for each RPWI subsystem separately. Output of both redundant parts is interconnected together by summing circuitry making the Single Point of Failure Free (*SPF-Free*) design. For high current loads on digital voltage rail, switch mode PoL regulators are used on load side, synchronized to clock (1 MHz) derived from the distributed 50 MHz LVDS signal to minimize the frequency random walk of PoL's internal oscillators.

The insulation between primary and secondary power lines in the RPWI is ≥ 1 MΩ and less than 150 nF. Power required for LP/MIME Antennas is routed via LVPS frame to the backplane and to the LP/MIME and HF subsystem. The antenna deployment is not controlled by the LVPS.

A special requirement is taken on the converter Common Mode conducted emissions, because the RPWI instrument principle is to (among other) sample the variation in the voltage and current field between probes, ambient plasma environment and the spacecraft ground potential, which is considered as non-ideal at medium and high frequencies (up to 50 MHz).

5.3.2. *RPWI LVPS Thermal Design*

The board is connected to the frame via 19× M4 screws. Ground planes cover 95% of the circuit board area and below the FPGA two supply planes are implemented.

Main power switches are mounted close to the border of the PCB to increase the thermal conductivity into the main electronics box frame. No electrical components are mounted to the frame itself, except interfacing MDM connectors which are flying leads-wired to the board. The specified temperature ranges in different modes of operations are listed in Tab.: 5

Tab.: 5 Temperature ranges summary.

Mode	Temperature range (°C)	
	T_{Min}	T_{Max}
Non-Operating	-30°C	+65°C
Operating	-30°C	+65°C
Non-Operating Qualification	-40°C	+75°C
Non-Operating Acceptance	-35°C	+70°C
Operating Qualification (ON)	-40°C	+75°C
Operating Acceptance (ON)	-35°C	+70°C

There are two units located in two dedicated frames accommodating LVPS units A and B. From left to right frames are stacked as follows: *HF, LP-MIME, LF, DPU-B, DPU-A, LVPS-B, LVPS-A*. All frames are screwed together and mounted to the spacecraft via the dedicated thermal bottom plate Fig. 55.

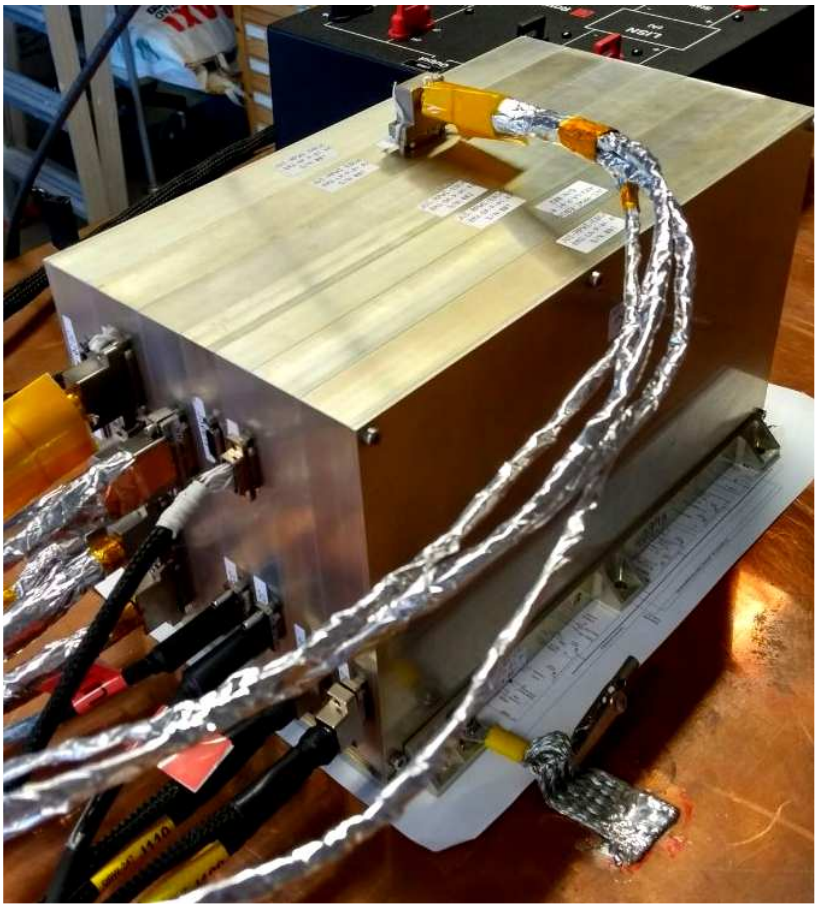


Fig. 55 The assembled RPWI EBOX in Engineering Model grade with associated harness during the functional testing. Note the high frequency grounding stud on the bottom-right.

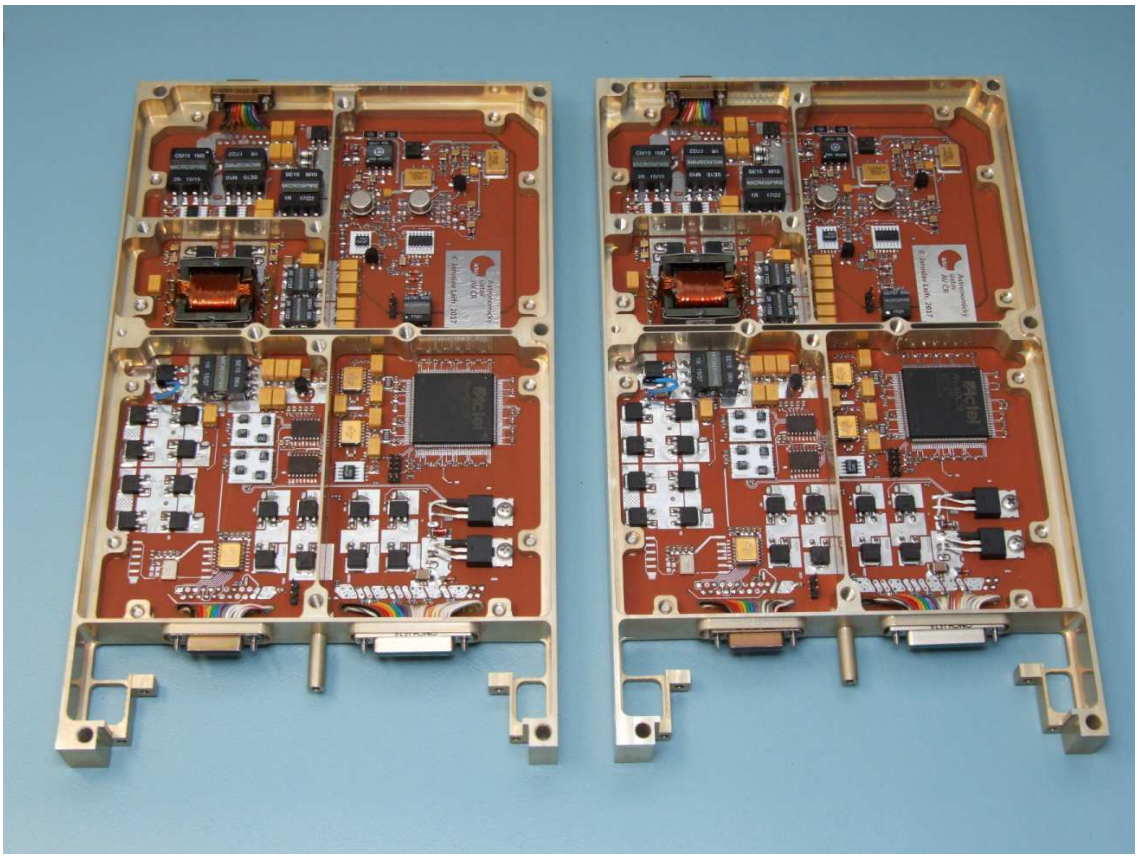


Fig. 56 RPWI LVPS Engineering Models 2, C (left), D (right). Top view.

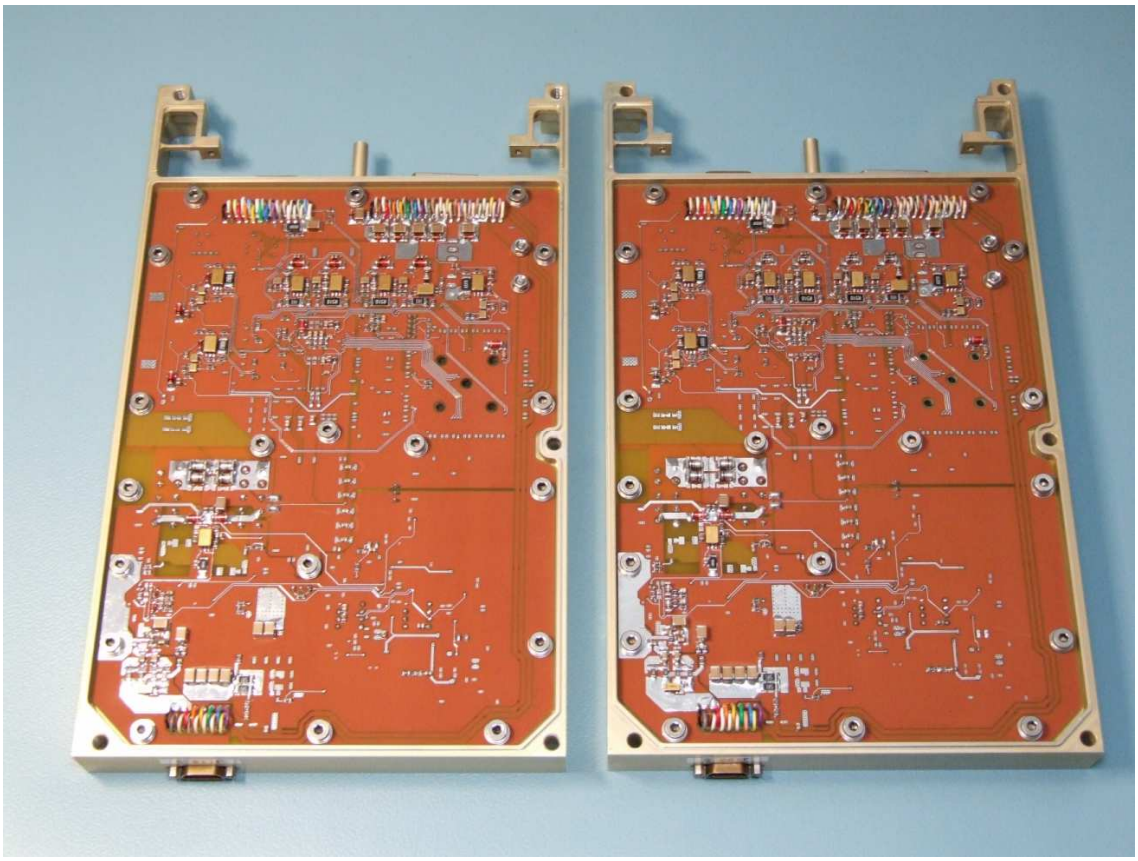


Fig. 57 RPWI LVPS Engineering Models 2, C (left), D (right). Bottom view.

Only one out of two units are nominally running and producing thermal dissipation at a time. Image of the Engineering Model unit below captured using the thermal camera shows hotspots during 28 V, 0.78A input conditions, with a maximum of 30±2°C at a room temperature. Bottom side of the frame is facing to S/C structure.

Fig. 58 RPWI LVPS EM2 Thermal Footprint under full load conditions.

5.3.3. RPWI LVPS Electrical Interfaces

The LVPS is connected directly to the *S/C PCDU* via two identical insulated power connector inputs. The antenna deployment power, both Main and Redundant, is routed together with respective (Main, Redundant) power connectors.

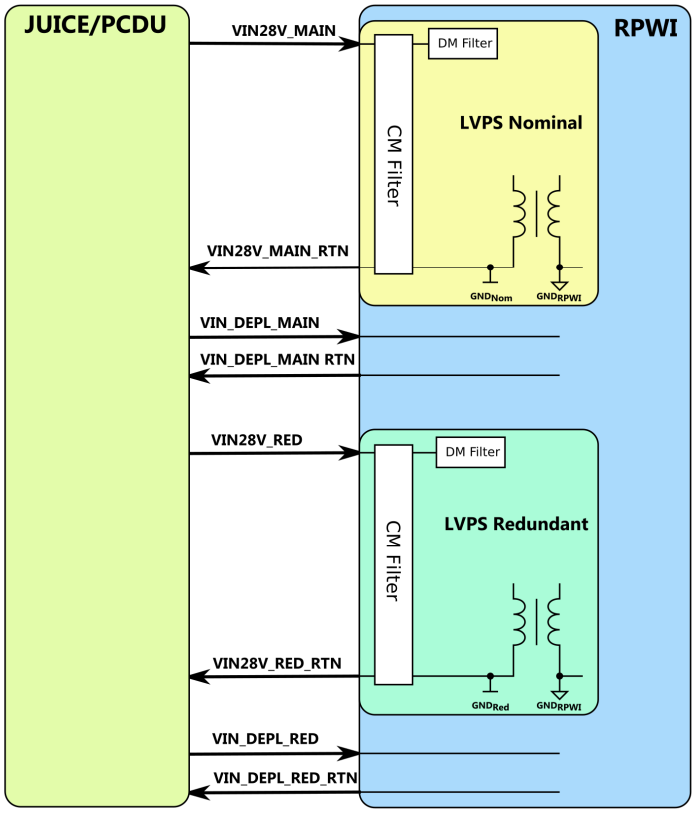


Fig. 59 The JUICE Spacecraft interfacing with the Cold-Redundant RPWI LVPS.

The electrical realization of the LVPS input interface (example of Main part interfacing with S/C PCDU) is described by the schematic diagram Fig. 60.

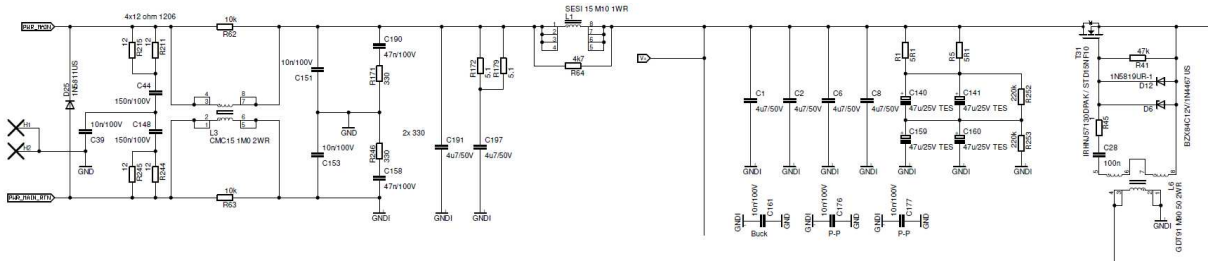


Fig. 60 RPWI LVPS Input Filter schematics optimized to suppress the CM and DM emissions.

Overvoltage protection of secondary side loads is realized based on continuous measurement of main transformer central tap voltage with fast reaction. The time constant in order of several tens of microseconds is implemented to prevent reaction on fast transients on input bus to suppress false reactions on Conducted Susceptibility test. Once the overvoltage on step-down converter output (main transformer feeding input = central tap) is detected, the sensing comparator immediately blocks the push-pull driving circuits using AND gates logic on cycle-by-cycle principle. Implemented principle together with output capacitor bank brings additional rise time constant assuring that the output voltage remain below the maximum voltage threshold within 5% of maximum allowed voltage. Under multi-cycle overvoltage conditions, the permanent SCR structure reacts and keeps the converter under no power transfer conditions until the S/C PCDU will power cycle (reset) the converter.

On the same AND gate input, the overcurrent sensing BJT current-mirror based circuit is implemented to limit current flow in each cycle.

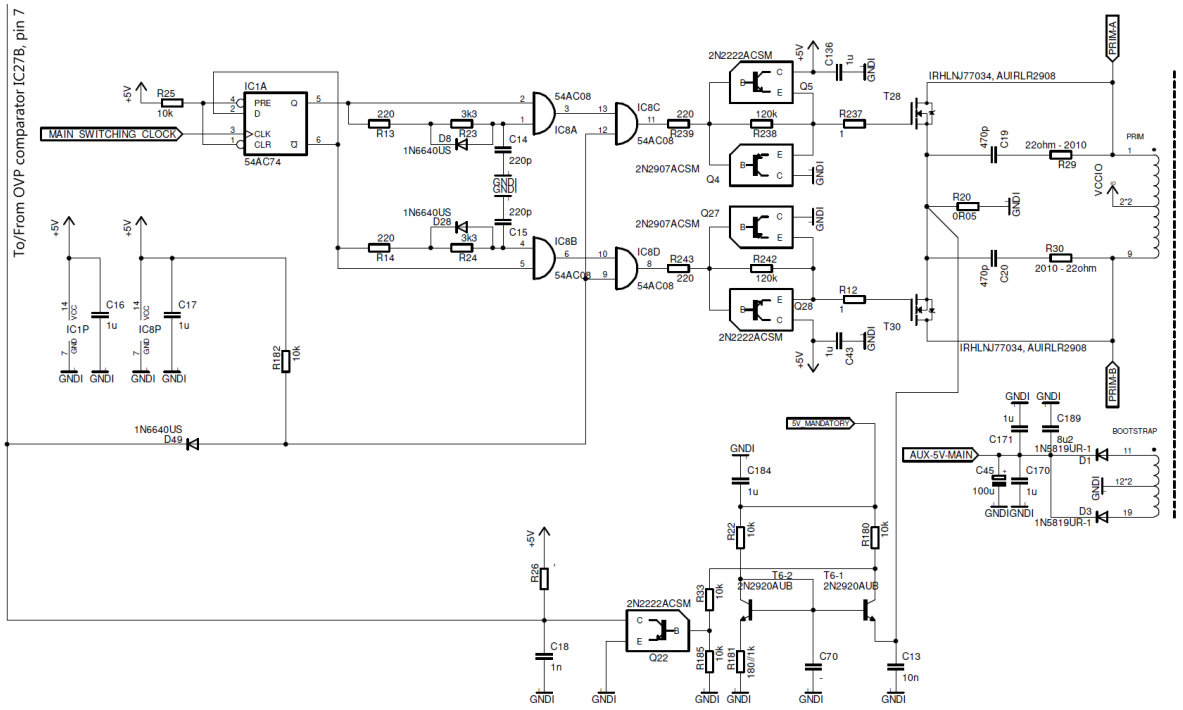


Fig. 61 Discrete based push-pull driver with cycle-by-cycle overcurrent and overvoltage protection.

The independent overvoltage protection and *Under Voltage Lockout (UVLO)* circuits are OR-ed with the *SCR-like* latch circuit activated by the primary side over-current event. In case of overcurrent or push-pull stage overvoltage event, the total input voltage turn-off

initiated by the *S/C PCDU* is the only means of resetting the latch circuit. The *UVLO* is not latching and thus react even in very slow turn-on voltage ramp (when input power ramp is in order of seconds or more).

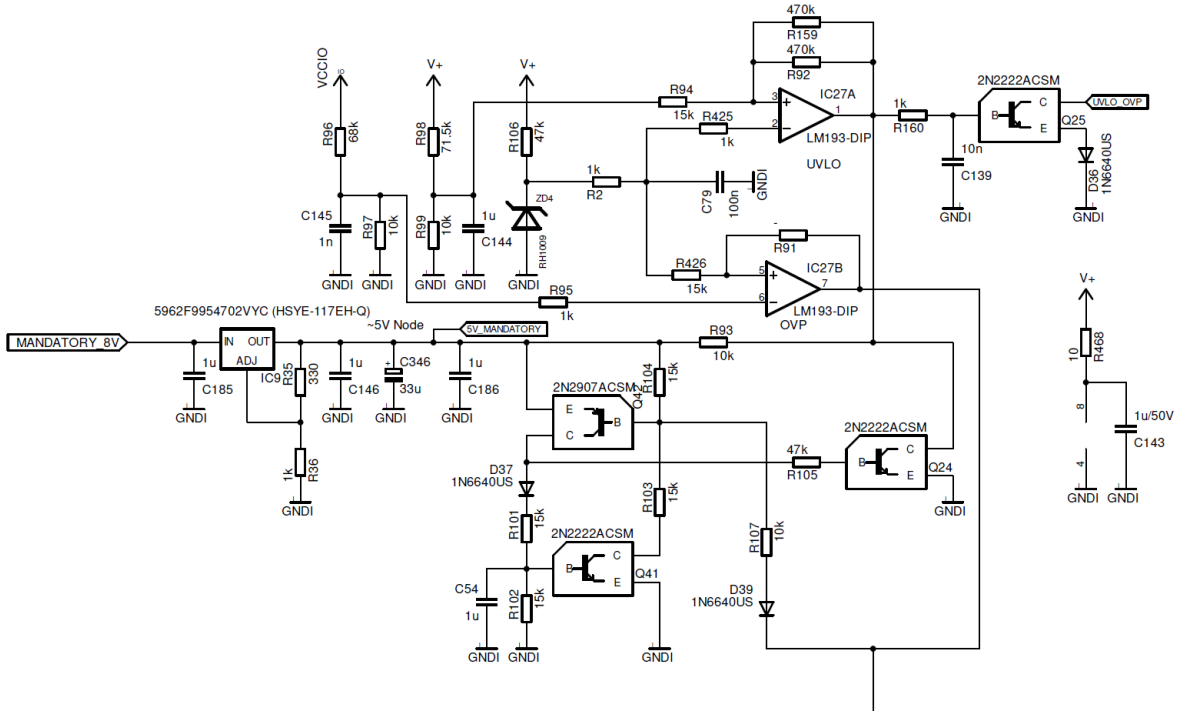


Fig. 62 The discrete-based UVLO, latching SCR and overvoltage sensing circuitry.

In case the LVPS protection is permanently latched (failure conditions), the nominal power consumption falls down to idle mode (around 8 mA @ 28 V). Such status is permanent and will be restored only by power cycle: 28 V ⇨ 0 V ⇨ 28 V with at least 5 seconds with 0V applied between PWR and RTN wires.

The *UVLO* threshold is set with hysteresis between 21.6 to 22.7 V. The Buck stage OVP threshold is 19V +/- 0.5V. Physical connection with *S/C PCDU* is realized via two Micro-D 15-pin Connectors. To assure the OVP and UVLO will react as fast as possible, their shutting down signal is fed directly to AND gates driving the Push-Pull stage. Whilst latching SCR circuit time constant is about 8 ms, to does not react to initial startup transients, the AND logic control assures maximally fast protection to output circuits.

5.3.4. RPWI LVPS Grounding Block Diagram

A star grounding concept is used for LVPS secondary side (output). The converter performs galvanic insulation between primary S/C bus (+28V & return wire) and secondary side-bound instruments of the RPWI via power transformer. To minimize the grounding connections impedance and common mode noise levels important for proper and sensitive measurements referenced to S/C chassis, all power and digital interfaces towards the RPWI *EBOX* are grounded to chassis. Associated ground wires are used to deliver the ground potential to the *EBOX* backplane with aim to further minimize the ground tracks impedance.

All power outputs, *LVDS* bus driver and Serial link driver are all referenced to chassis ground potential through the PCB grounding copper planes and via M4 mounting screws.

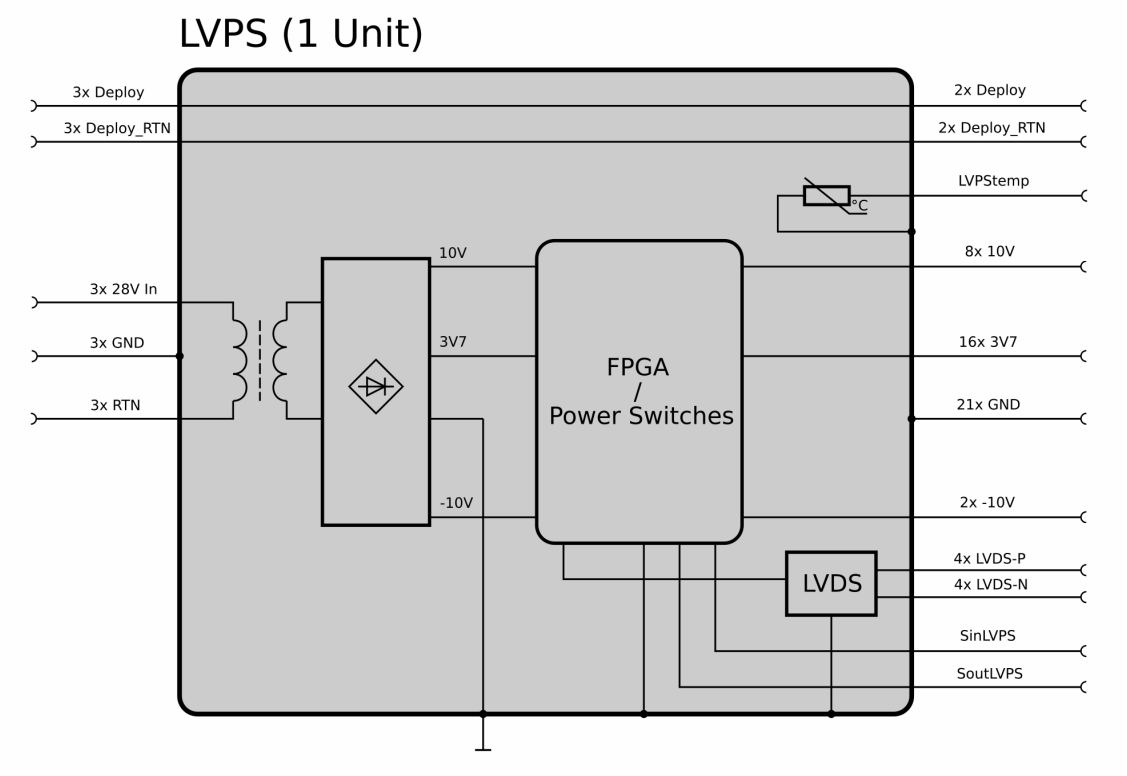


Fig. 63 RPWI LVPS Grounding Block Diagram.

5.3.5. RPWI LVPS Frequency Plan

The LVPS self-generated main frequencies are summarized in the table below. Unwanted spectra peaks identified or sampled by the respective instruments are then possible to be determined and removed from the data.

Tab.: 6 LVPS First harmonics-based Frequency Plan.

Function	Nominal Frequency	Range
Base clock frequency	50 MHz	± 50 ppm or better
Switching frequency of the step down stage	250 kHz	± 100 ppm
Switching frequency of the push-pull stage	125 kHz	± 100 ppm
LVCMOS Communication Baud Rate	115207.37 Hz	Duty cycle depending on transferred data

5.3.6. RPWI LVPS Magnetics and Main Transformer Design

The LVPS includes several types of inductive electrical components, according to the following list:

1) The DC/DC Converter main Transformer: *EFD-25, FLUX.DK*, Custom-made
2) DC/DC Converter Filter Coils: *Microspire* product grade selection
3) DC/DC Converter Gate Drive Transformers: *Microspire* product grade selection

There are no permanent magnetic materials used in the LVPS. Whilst power inductors are selected from the predefined families *CMC-15, SESI-9.1, SESI-15* and *GDT-91*, the main power transformer is a custom made element with parameters summarized in Tab.: 7.

Tab.: 7 LVPS Main Power Transformer Summary.

	Value	Note
Core Size	EFD25	
Al [nH]	2660	
Core Material	3C95	FERROXCUBE, no air-gap
Bobbin	EFD25 Plastic, Black	10 pin + 10 flying leads (or External Adapter)

Parameter		Value	Unit
Ve	**Effective volume**	3300	mm^3
Le	**Effective length**	57	mm
Ae	**Effective area**	58	mm^2
Amin	**Minimum area**	55	mm^2
m	**EFD25/13/9**	≈ 8	g/pcs

The *EFD-25* low profile transformer bobbin with standard 10 pin footprint is extended to 20 pin by the external header, as depicted in Fig. 64. The design description in Fig. 65 and Tab.: 8 shows the construction of the push-pull transformer with central taps and multiple output windings. However, central taps are interconnected on the PCB to form the push-pull coil topology, and could decrease up to the half the leakage current due to the suppression of the inter-winding and PCB traces capacitive coupling.

To utilize the bobbin length and minimize the copper losses, parallel coil winding is used, with interleaving of layers to maximize the energy transfer through the magnetic field in the center of the core, where the highest load current secondary coils are wound. The schematic is shown in Fig. 66. No primary-to-secondary copper shielding is used, except the Kapton tape to suppress the capacitive coupling.

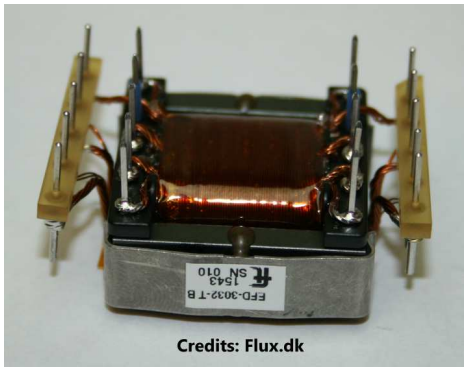


Fig. 64 The space-qualified EFD-25 transformer with extension headers to allow up to 20 coils with up to 4 wire-ends per pin. Credits: FLUX.DK

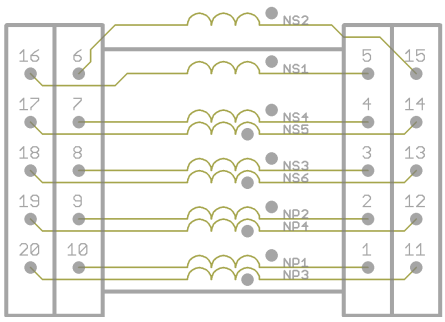


Fig. 65 The wiring names (Top) and coil names (Bottom) description of the EFD-25 RPWI LVPS transformer. The top view is depicted.

Tab.: 8 EFD-25 Transformer winding parametric summary.

Winding Name	Winding Start Pin	Winding End Pin	Number of Turns	Number of Wires	Wire Diameter [mm]	Magnetization Inductance [uH]	Leakage Inductance [%]	Winding Ratio Nx/NP1 [-]
NP1	1	10	16	2	0.4	681 ± 20%	≤ 0.5	1
NP2	2	9	16	2	0.4	681 ± 20%	≤ 0.5	1 ± 0.1%
NP3	11	20	8	2	0.4	170 ± 20%	≤ 0.5	0.5 ± 1%
NP4	12	19	8	2	0.4	170 ± 20%	≤ 0.5	0.5 ± 1%
NS1	5	16	9	2	0.4	215 ± 20%	≤ 0.5	0.563 ± 1%
NS2	15	6	9	2	0.4	215 ± 20%	≤ 0.5	0.563 ± 1%
NS3	3	8	4	2	0.4	42.6 ± 20%	≤ 0.5	0.25 ± 1%
NS4	4	7	4	2	0.4	42.6 ± 20%	≤ 0.5	0.25 ± 1%
NS5	13	18	4	2	0.4	42.6 ± 20%	≤ 0.5	0.25 ± 1%
NS6	14	17	4	2	0.4	42.6 ± 20%	≤ 0.5	0.25 ± 1%

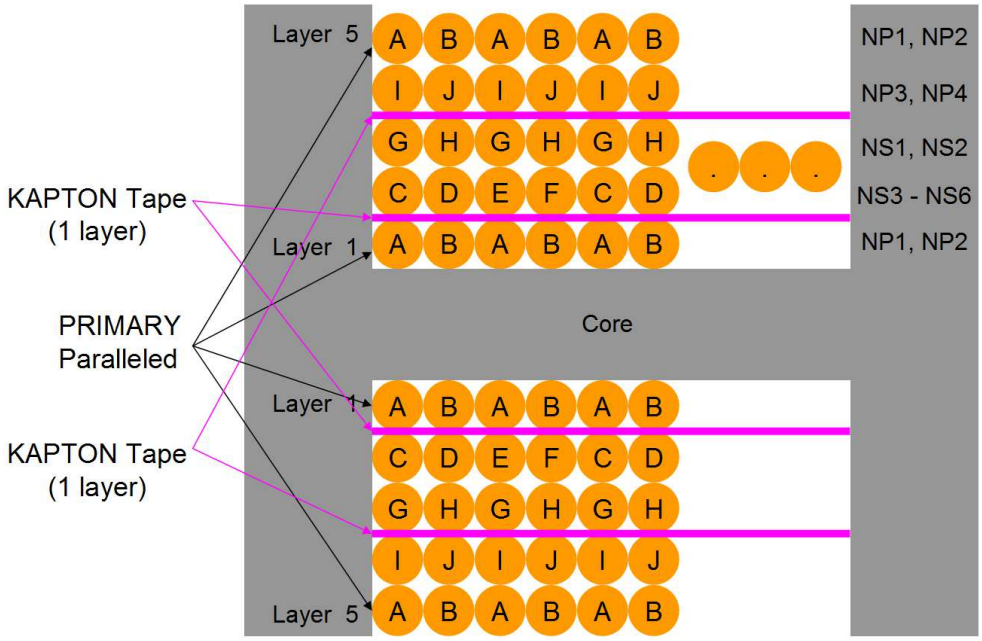


Fig. 66 Copper wire interleaving description. A cross-section of the EFD-25 Transformer bobbin is shown with insulating layers made of Kapton.

5.3.7. RPWI LVPS FPGA Firmware Block Diagram and Functionalities

Functions implemented in the LVPS FPGA firmware are described in the block diagram below. The FPGA core has the *ADC128S102 AD* converters interfaced at its inputs to provide Housekeeping measurements. It controls the output power switches and divides the external 50 MHz oscillator to generate the primary switching frequency of 250 kHz. The communication interface is implemented as conventional UART VHDL core. Based on the features, the RPWI LVPS FPGA design was implemented in VHDL by Jan Mareš, Astronomical Institute of the Czech Academy of Sciences.

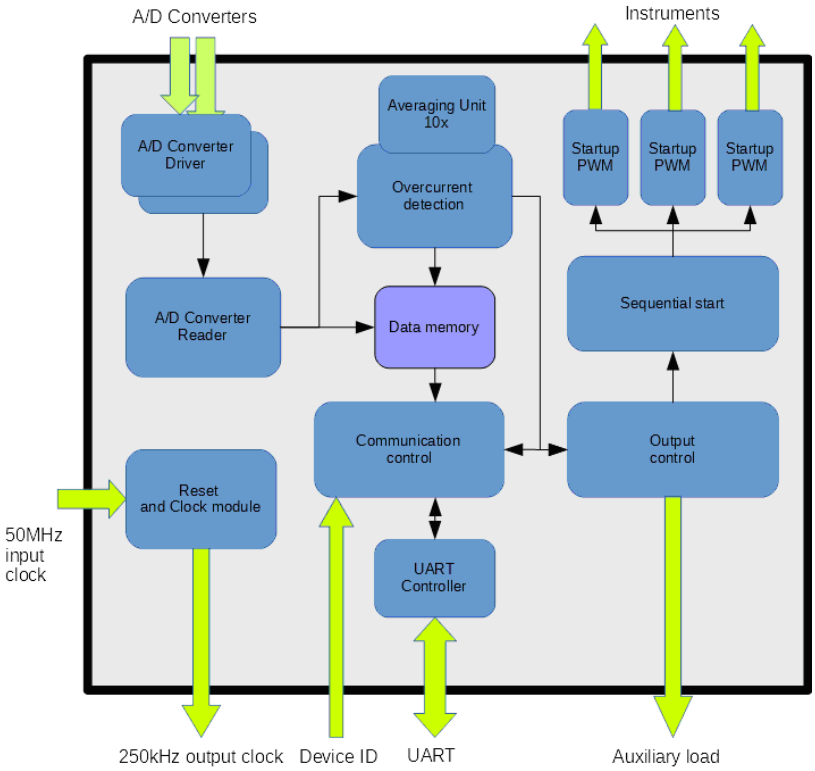


Fig. 67 LVPS FPGA Block diagram with interfaces.

The FPGA start-up sequence is initiated by system power up and stabilized by R/C circuit as depicted in Fig. 68. Steps performed since start-up are defined as follows:

1. 50 MHz input oscillator starts, FPGA powers on,
2. FPGA is held in reset state by R/C circuit for about 2 ms after input voltage rises,
3. The Reset is prolonged internally and synchronized (Synchronous Deassertion Reset),
4. FPGA starts normal operation,
5. The LVPS sync signal is started after 150 ms,
6. All output power MOSFET switches are turned Off.

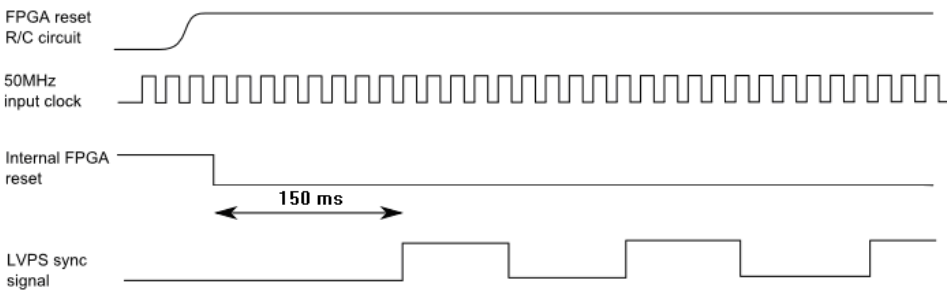


Fig. 68 LVPS FPGA Startup timing diagram. Time not to scale.

There are two 8 channel ADCs in each LVPS unit dedicated to measure housekeeping data. The Voltage sensing is performed on power converter output directly (sensing of the voltage at the rectification capacitors filter banks), i.e. before the output switching matrix. It means that the output voltage readout is showing non-zero voltages in Telemetry even when all output switches are OFF. Loading outputs by instruments usually means a marginal drop of the voltage readout value which is caused of physical loading of respective output wrt. no load conditions.

5.3.8. *RPWI LVPS FPGA Communication Interface*

Fast 50 MHz LVDS Clock distribution and switching frequency synchronization together with housekeeping measurements is realized within the FPGA softcore together with the outstanding stable Rad-Hard crystal oscillator.

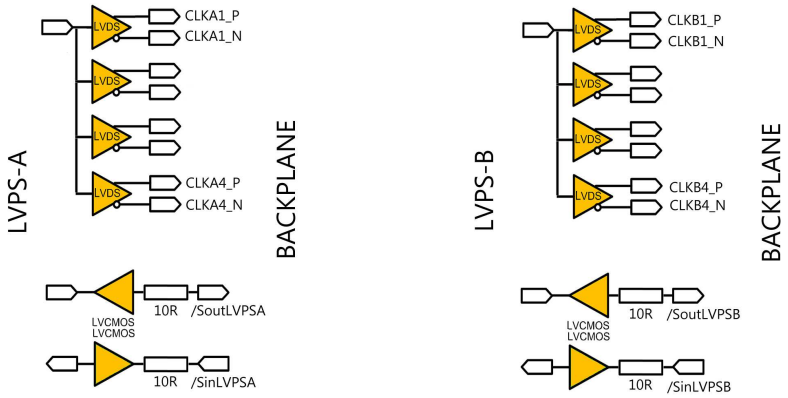


Fig. 69 The RPWI LVPS Communication interface buffering schematics. Both LVPS-A and B are mentioned. CLKxy_P and CLKxy_N forms LVDS pairs. Serial link is single-ended.

There is a dedicated LVDS driver with a single source of 50 MHz clock signal delivering a star-like clock signal distribution to subsystems in each LVPS unit. All differential pairs are expected to be properly routed with identical track length as well as properly terminated on backplane and user's side. LVDS driver is grounded directly to LVPS chassis ground potential.

The *TM/TC UART* serial link is driven directly from FPGA pins via 10 ohms isolation resistors used to slightly suppress EMC on 115200 bps link during data transfer. Whilst the LVDS transmission is routed via differential pairs, the UART serial link is routed as single ended, referenced directly to LVPS chassis ground potential as depicted in Fig. 69.

For a serial data transfer between the LVPS and DPU a basic infinite program loop is processed inside of the LVPS FPGA state-machine. The flow is described in the diagram Fig. 70. It is depicted from the prospective of the LVPS to be a slave. “Waiting for Packet” is understood as a waiting for the DPU data transmission. “Send” is understood as the transmission from LVPS to the DPU.

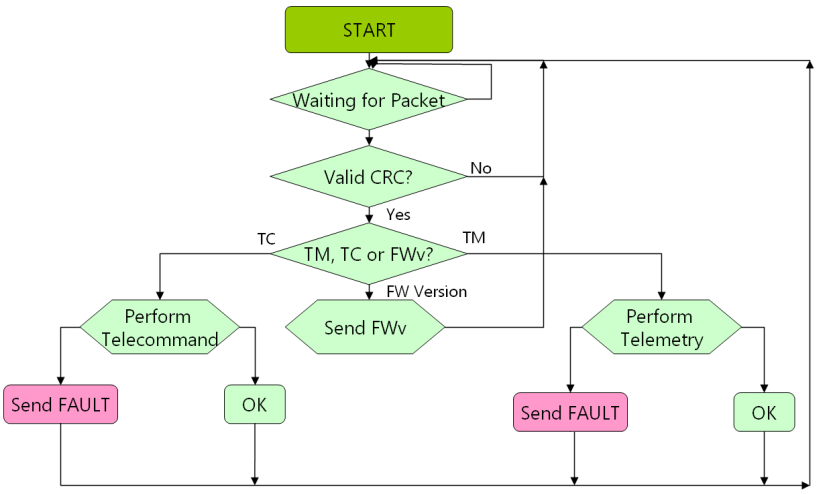


Fig. 70 RPWI LVPS FPGA Communication firmware block diagram.

To increase the safety by simplicity of the LVPS-DPU communication controller implementation, the UART data transmission is performed using packets of fixed length (4 bytes) for all types.

Synchronization of whole data packet is performed using unique data mark labelling of the beginning of the packet. In this case, the header byte is the only one containing logic 1 at the MSB position. All the rest three bytes have logic 0 fixed bit in MSBs. To keep the 8 bits wide data field, the header is divided into two different bytes – the 0xF0h or 0xF1h representing data range of 0-127 and 128-255 respectively in case of Telecommand and 0xE0h or 0xE1h in case of Telemetry.

TELECOMMAND Request Format (TC REQUEST): (LVPS ⇐ DPU)

Byte 0	Header	**0xF0h** Fixed
Byte 1	Address	Address of the telecommand, see the list below. Value from 0 to 15.
Byte 2	Data	Data of the telecommand, see the list below.
Byte 3	CRC	**0ddd dddd**, where "d" is 0ddd dddd, where "d" is Checksum, XNOR of three previous bytes.

TELECOMMAND Response Format (TC REPLY): (LVPS ⇒ DPU)

Byte 0	Header	**0xF0h** in case data field contains number 0-127 **0xF1h** in case data field contains number 128-255
Byte 1	Address	Address of the telecommand, see the list below. Value from 0 to 15.
Byte 2	Data	Data of the telecommand, see the list below.
Byte 3	CRC	**0ddd dddd**, where "d" is 0ddd dddd, where "d" is Checksum, XNOR of three previous bytes.

TELECOMMAND FAULT Response Format (TC FAULT): (LVPS ⇒ DPU)

Byte 0	Header	**0xF0h** Fixed
Byte 1	Address	**0X7Eh** Fixed
Byte 2	Data	**0X7Eh** Fixed
Byte 3	CRC	**0ddd dddd**, where "d" is Checksum, XNOR of three previous bytes.

TELEMETRY Request Format (TM REQST): (LVPS ⇐ DPU)

Byte 0	Header	**0xE0h** Fixed
Byte 1	Address	Address of the telemetry request see the list below. Value from 32 to 127.
Byte 2	Data	Data of the telecommand, see the list below.
Byte 3	CRC	**0ddd dddd**, where "d" is Checksum, XNOR of three previous bytes.

TELEMETRY Response Format (TM REPLY): (LVPS ⇒ DPU)

Byte 0	Header	**0xE0h** in case data field contains number 0-127 **0xE1h** in case data field contains number 128-255
Byte 1	Address	Address of the telemetry request see the list below. Value from 32 to 127.
Byte 2	Data	Data of the telemetry, see the list below.
Byte 3	CRC	**0ddd dddd**, where "d" is Checksum, XNOR of three previous bytes.

TELEMETRY FAULT Response Format (TM FAULT): (LVPS ⇒ DPU)

Byte 0	Header	**0xE0h** Fixed
Byte 1	Address	**0X7Eh** Fixed
Byte 2	Data	**0X7Eh** Fixed
Byte 3	CRC	**0ddd dddd**, where "d" is Checksum, XNOR of three previous bytes.

The FPGA contains 8-bit long registers which could modify the behaviour of the LVPS unit during the flight upon Telecommand.

To boot-up and work safely even without the DPU aid, the initial upload of implicit values is performed based on hardwired register settings stored in FPGA ROM memory.

Registers are by default filled with predefined values given in the table below. Respective trip-off values of the digital *OVP* and *OVC* protections are mentioned.

Address - Telecommands	Trip-Off Value	Default Value in ROM [DEC]	Default Value in ROM [HEX]
01 - Power Output Set ON/OFF		0	0
04 - Overcurrent Threshold Limit Register - LP/MIME 3.7V OVC	0.591 A	143	8F
05 - Overcurrent Threshold Limit Register - LP/MIME 9.75V OVC	0.200 A	141	8D
06 - Overcurrent Threshold Limit Register - LP/MIME -9.75V OVC	0.200 A	141	8D
07 - Overcurrent Threshold Limit Register - LF 3.7V OVC	0.716 A	142	8E
08 - Overcurrent Threshold Limit Register - LF 9.75V OVC	0.161 A	143	8F
09 - Overcurrent Threshold Limit Register - HF 3.7V OVC	3.274 A	144	90
10 - Overcurrent Threshold Limit Register - HF 9.75V OVC	0.191 A	141	8D
11 - Overvoltage Threshold Limit Register 3.7V OVP	4.07 V	159	9F
12 - Overvoltage Threshold Limit Register 9.75V OVP	11.70 V	173	AD
13 - Overvoltage Threshold Limit Register -9.75V OVP	-11.71 V	173	AD
14 - Digital Inrush Current Limiter LP/MIME Duty Cycle - WRITE		30	1E
15 - Digital Inrush Current Limiter LF Duty Cycle - WRITE		30	1E
16 - Digital Inrush Current Limiter HF Duty Cycle - WRITE		7	7
17 - Digital Inrush Current Limiter LP/MIME Delay length - WRITE		7	7
18 - Digital Inrush Current Limiter LF Delay length - WRITE		3	3
19 - Digital Inrush Current Limiter HF Delay length - WRITE		7	7
Address - Telemetry			
32 - Read Firmware Version		35	23
33 - Voltage Level on DPU3.7V Line		N/A	N/A
34 - Voltage Level on DPU+9.75V Line		N/A	N/A
35 - Voltage Level on LP/MIME 3.7V line		N/A	N/A
36 - Voltage Level on LP/MIME +9.75V Line		N/A	N/A
37 - Voltage Level on LP/MIME -9.75V Line		N/A	N/A
38 - Voltage Level on LF 3.7V Line		N/A	N/A
39 - Voltage Level on LF 9.75V Line		N/A	N/A
40 - Voltage Level on HF 3.7V Line		N/A	N/A
41 - Voltage Level on HF 9.75V Line		N/A	N/A
43 - Output Current Level on DPU3.7V Line		N/A	N/A
45 - Output Current Level on LP/MIME 3.7V Line		N/A	N/A
46 - Output Current Level on LP/MIME +9.75V Line		N/A	N/A
47 - Current level on LP/MIME -9.75V line		N/A	N/A
48 - Output Current Level on LF 3.7V Line		N/A	N/A
49 - Output Current Level on LF 9.75V Line		N/A	N/A
50 - Output Current Level on HF 3.7V Line		N/A	N/A
51 - Output Current Level on HF 9.75V Line		N/A	N/A
53 - Overvoltage Detection on Output Lines		0 on startup	0 on startup
54 - Overcurrent Detected on Output Lines		0 on startup	0 on startup
55 - Instrument Status ON/OFF		0 on startup	0 on startup
58 - Overcurrent Threshold Limit Register - LP/MIME 3.7V OVC - READ		143 on startup	8F on startup
59 - Overcurrent Threshold Limit Register - LP/MIME 9.75V OVC - READ		141 on startup	8D on startup
60 - Overcurrent Threshold Limit Register - LP/MIME -9.75V OVC - READ		141 on startup	8D on startup
61 - Overcurrent Threshold Limit Register - LF 3.7V OVC - READ		142 on startup	8E on startup
62 - Overcurrent Threshold Limit Register - LF 9.75V OVC - READ		143 on startup	8F on startup
63 - Overcurrent Threshold Limit Register - HF 3.7V OVC - READ		144 on startup	90 on startup
64 - Overcurrent Threshold Limit Register - HF 9.75V OVC - READ		141 on startup	8D on startup

65 - Overvoltage Threshold Limit Register 3.7V OVP - READ		159 on startup	9F on startup
66 - Overvoltage Threshold Limit Register 9.75V OVP - READ		173 on startup	AD on startup
67 - Overvoltage Threshold Limit Register -9.75V OVP - READ		173 on startup	AD on startup
68 - Digital Inrush Current Limiter LP/MIME Duty Cycle [%] - READ		30 on startup	1E on startup
69 - Digital Inrush Current Limiter LF Duty Cycle [%] - READ		30 on startup	1E on startup
70 - Digital Inrush Current Limiter HF Duty Cycle [%] - READ		7 on startup	7 on startup
71 - Digital Inrush Current Limiter LP/MIME Length [ms] - READ		7 on startup	7 on startup
72 - Digital Inrush Current Limiter LF Length [ms] - READ		3 on startup	3 on startup
73 - Digital Inrush Current Limiter HF Length [ms] - READ		7 on startup	7 on startup
74 - Unit ID Readout - READ		Hardwired (range 0 to 15)	Hardwired (range 0 to 0F)

5.3.9. RPWI LVPS Clock Distribution and Management

There are two sources of switching clock implemented inside of the LVPS. The first random walk RC-oscillator based clock source is used to maintain the switching clock since the LVPS power up (applied power exceeding UVLO limit). The converter is working in the range of 220-240 kHz free running oscillator, until the secondary side digital rail (3.7 V) is not properly biased and all filtering capacitors charged to nominal voltage. Then the secondary side precise crystal oscillator starts to provide with the 50 MHz clock, which is fed to the FPGA. The high frequency clock signal mandatory for the stable converter operations is buffered by the circuitry given in Fig. 69. The short-circuit of single LVDS bus isolates the converter from a lack of the clock signal. It is thus SPF-Free.

The softcore in the FPGA adds up to 150 ms of the delay and then begins to drive the divided clock output (250 kHz) to the pulse transformer. The square wave signal transferred to the primary-side ground potential is then utilized to re-synchronize the converter from the free-running to synchronous mode. The RC-oscillator shut-off signal may collide with the synchronized clock and generate up to 3 missing pulses fed further to the buck converter. It was proved that in all cases when missing pulses occurred, the step-down switch was always in the off-state due to the applied bleeding resistor between the Gate and Source pins (floating gate drive). The clock-takeover solution is given in Fig. 71, the missing pulses are captured in Fig. 72 and published in [PP-14].

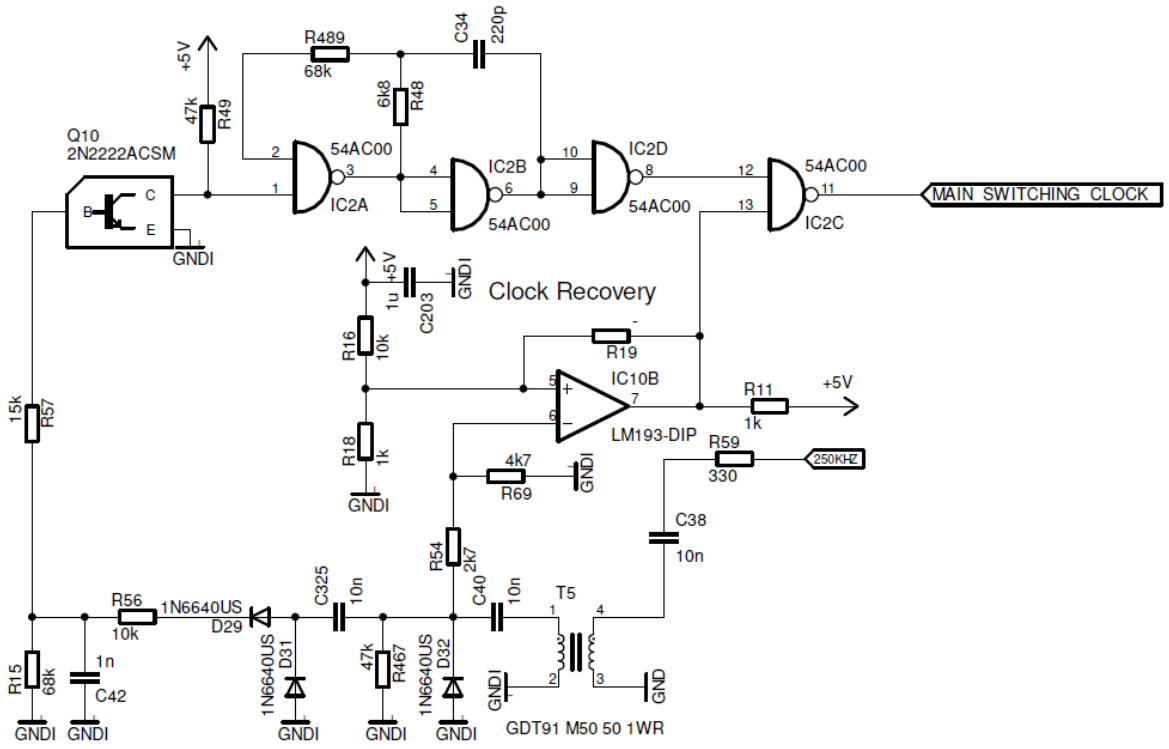


Fig. 71 The main LVPS Clock generator with the Sync Clock circuitry.

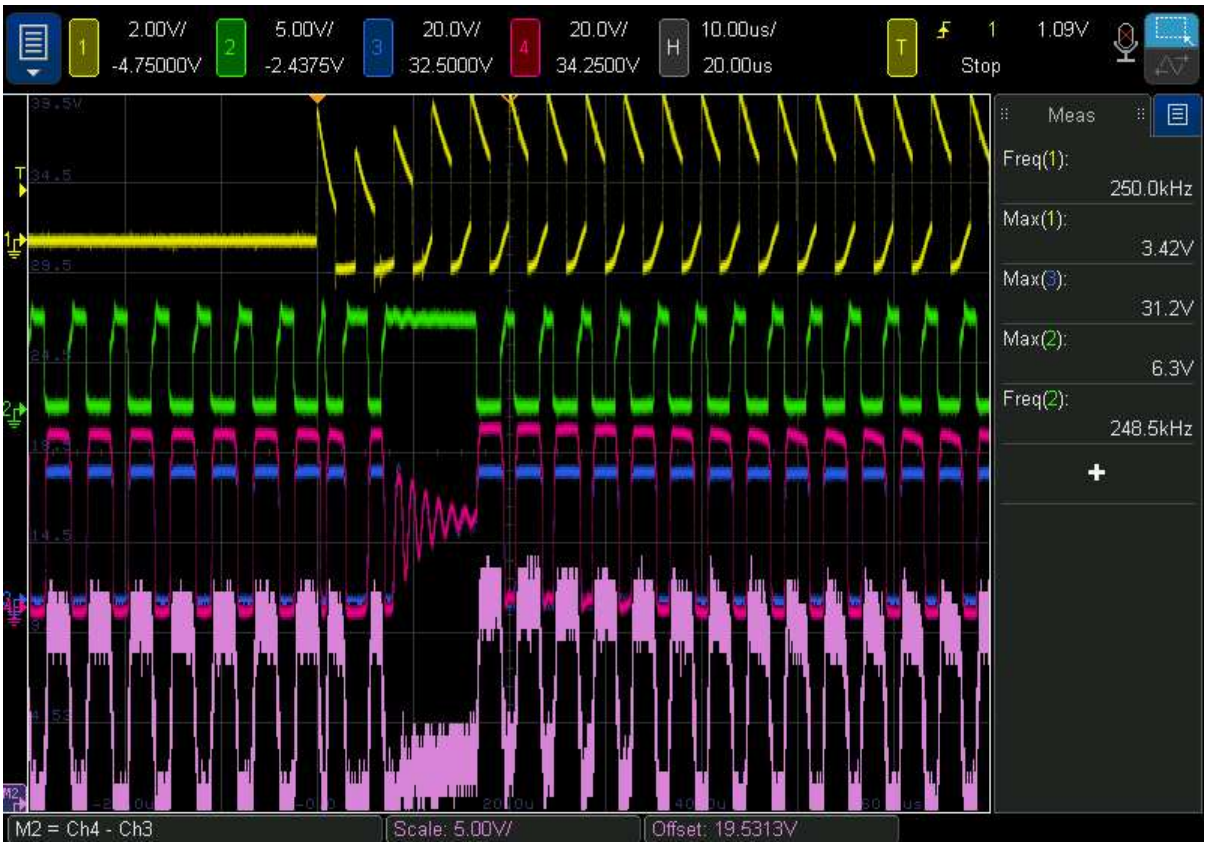


Fig. 72 The typical synchronization clock takeover event with two missing pulses. RC (248 kHz) and XO (250 kHz) controlled clock. From top to bottom: Recovered FPGA clock signal referenced to primary ground potential, buck MOSFET driving signal, buck MOSFET Gate + Source potential, buck MOSFET V_{GS} driving signal waveform.

5.3.10. RPWI LVPS Thermal Testing

The temperature dependence on output voltages was measured within the ambient pressure clima chamber in Fig. 73 filled with flow of atmospheric-pressure nitrogen to prevent icing/ice melting around the freezing point crossings. The measured data mentioned in following temperature dependency plots shows variations with respect to temperature to be below ±1% in the extended temperature range (-30 to +80°C).

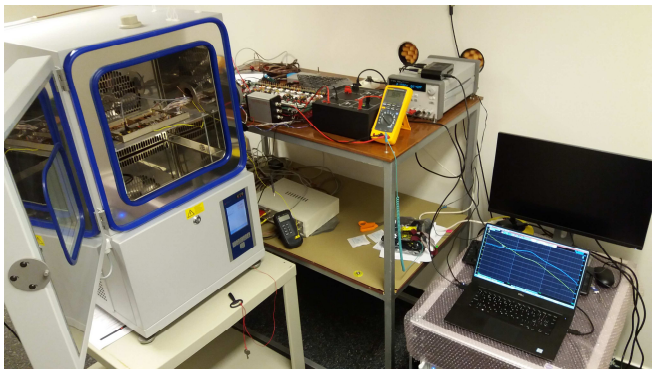
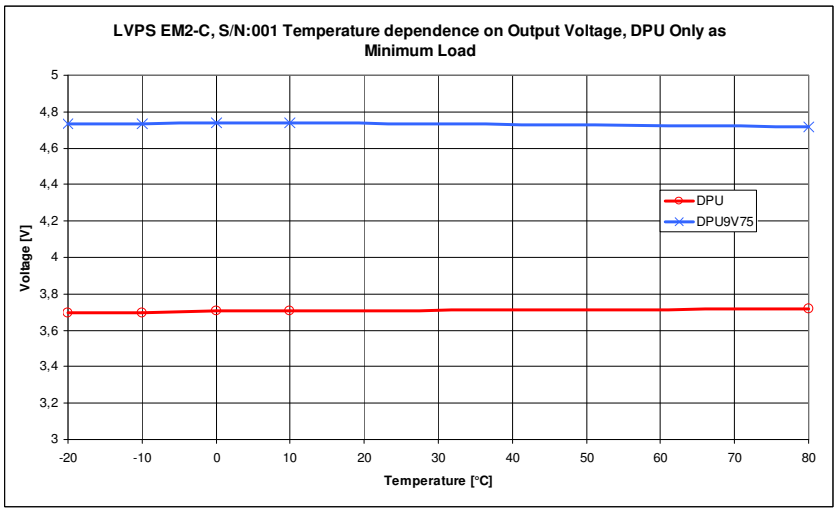
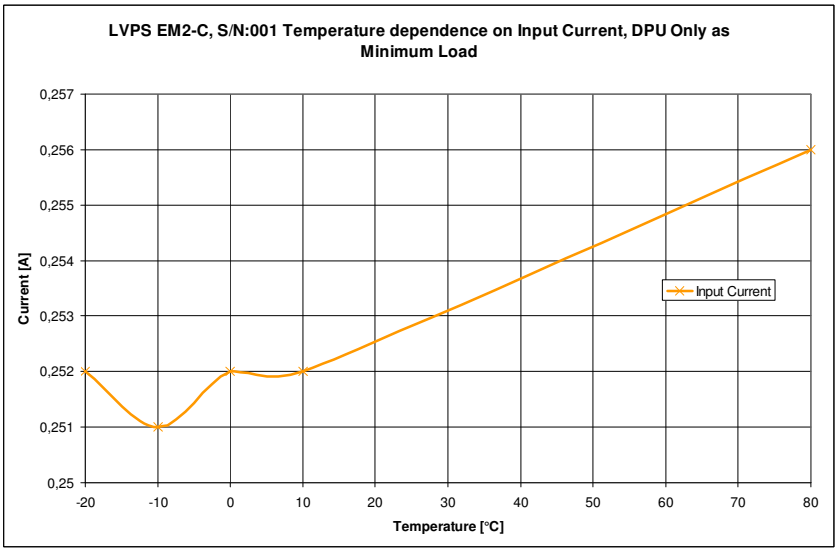
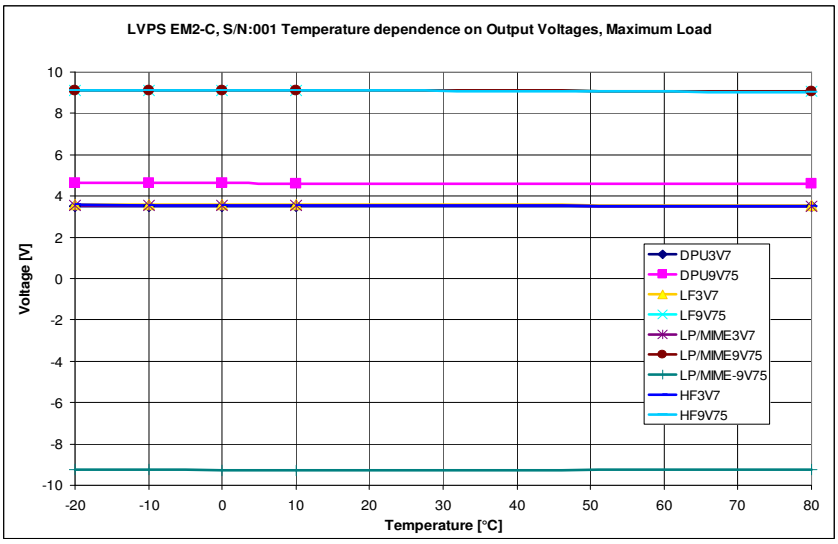
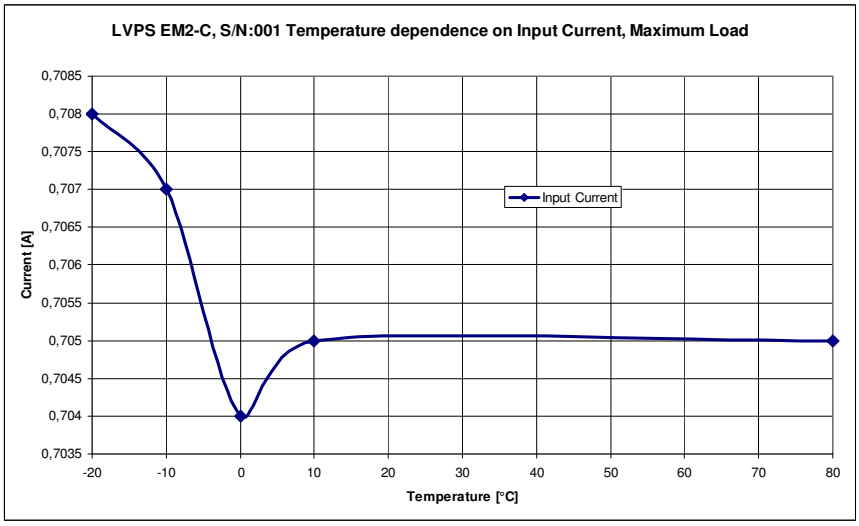


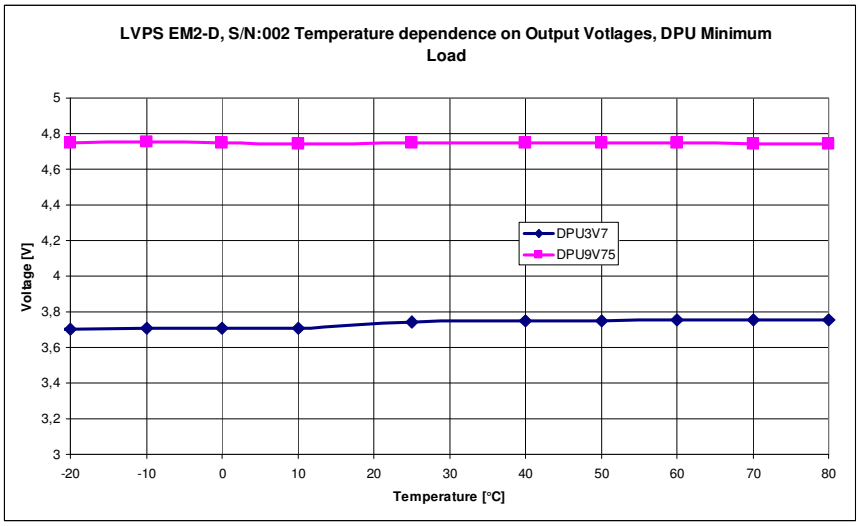
Fig. 73 Clima Chamber with the LVPS under test.

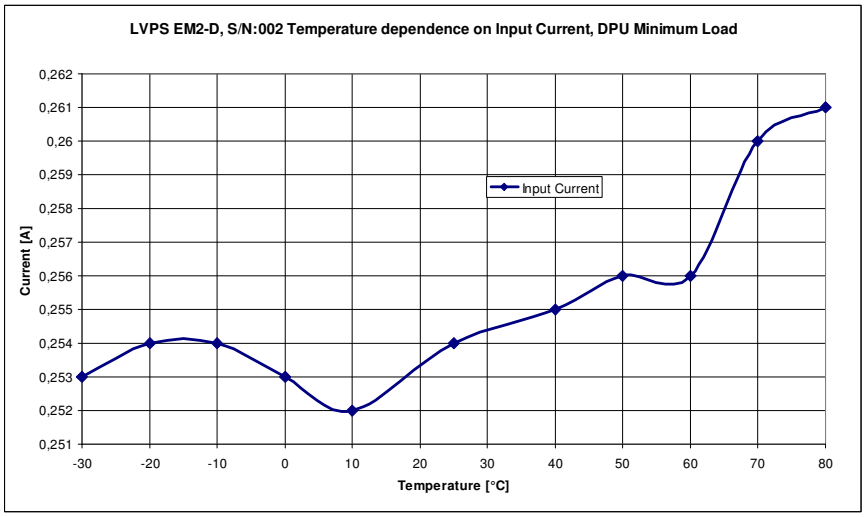


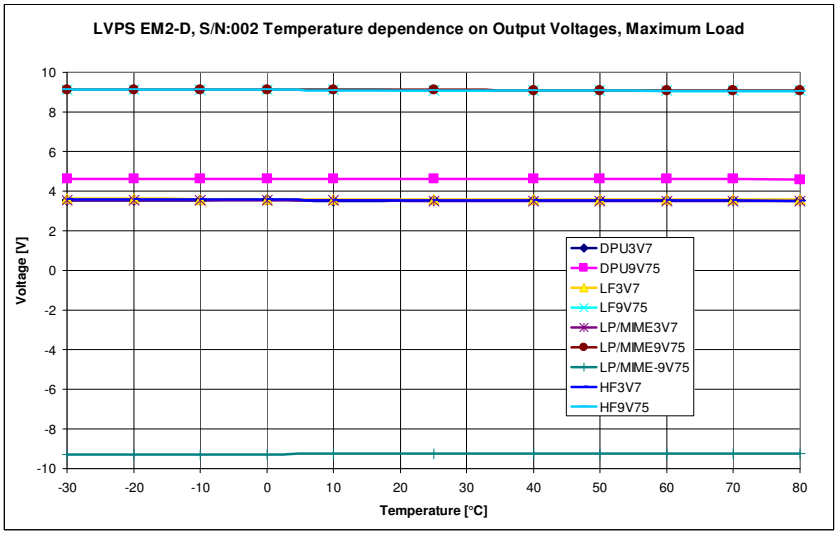



LVPS EM2-C, S/N:001 Temperature dependence on Output Voltages, Maximum Load
Voltage [V]
Temperature [°C]
DPU3V7
DPU9V75
LF3V7
LF9V75
LP/MIME3V7
LP/MIME9V75
LP/MIME-9V75
HF3V7
HF9V75


LVPS EM2-C, S/N:001 Temperature dependence on Input Current, Maximum Load
Current [A]
Temperature [°C]
Input Current


LVPS EM2-D, S/N:002 Temperature dependence on Output Votlages, DPU Minimum Load
Voltage [V]
Temperature [°C]
DPU3V7
DPU9V75





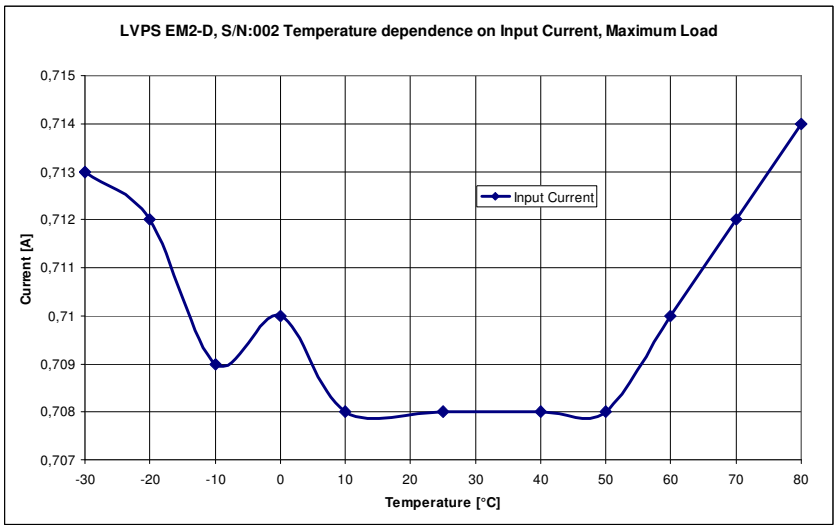


Fig. 74 Temperature dependency plots for two identical LVPS units (EM2-C and EM2-D). Measured parameters (voltage rails) are described in legend of each plot. All measurements were performed under full load conditions.

5.3.11. RPWI LVPS EMC Measurements

The EMC Conducted Emissions requirements imposed on the input bus were met, as mentioned by the switching frequency peaks being below the predefined emission masks in Fig. 76 and Fig. 77. The range of interest is specified as 100 kHz to 50 MHz. Measured data is published in [PP-14]. The voltage ripple on the highest current output (HF receiver 3.7 V) was determined as less than 700 μV_{RMS}. The test setup with proper grounding and copper plated table is depicted in Fig. 75.

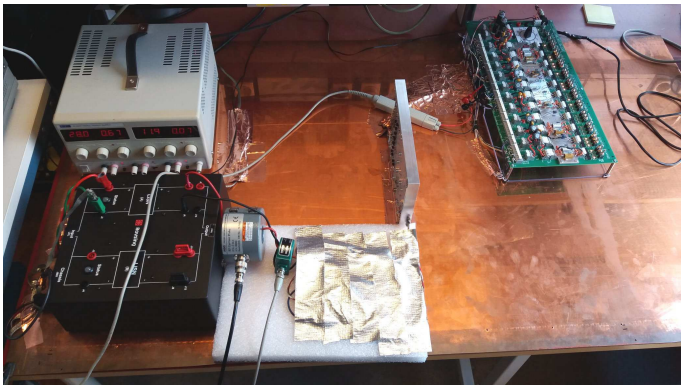


Fig. 75 The RPWI LVPS EMC test setup. Left top - bench power supply, left bottom - LISN, middle - wide bandwitdh current probes, LVPS DUT and right - dummy loads board.

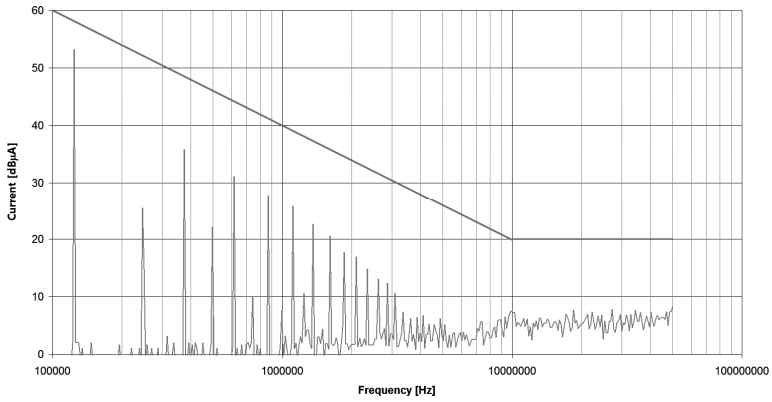


Fig. 76 The Conducted Emissions measured on the input power bus with the Differential Mode probing at the full load conditions [PP-14].

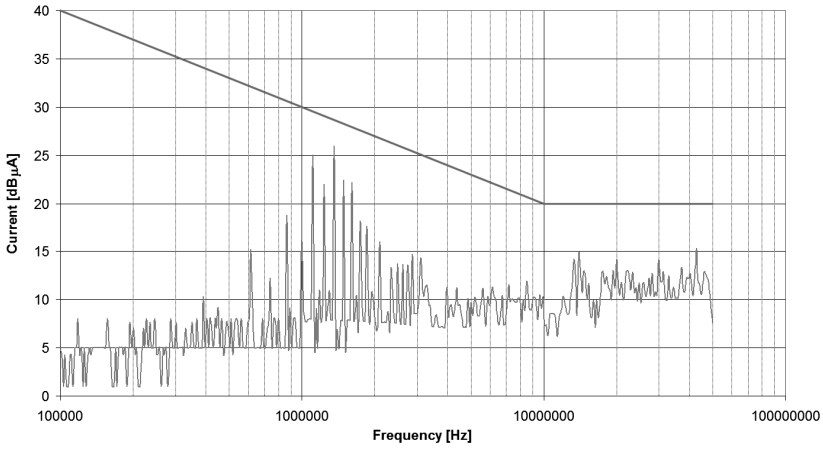


Fig. 77 The Conducted Emissions measured on the input power bus with the Common Mode probing at the full load conditions [PP-14].

5.4. A Novel Digital Inrush Current Limiter

5.4.1. RPWI LVPS Power Distribution Unit

The output switching matrix of power MOSFETs is prepared to be able to turn On and Off respective instrument. Whilst the required turn Off time is expected to be as short as possible (below 3 ms or less) to prevent burnout of chip bond wires etc., the leading turn On ramp shall be longer than just sudden voltage/current step to suppress the inrush current to reasonable low level. With high inrush current detected, the power supply may suffer from overloading with reaction of overcurrent/overload protection, which shall not be utilized under any nominal load conditions. The analog current limiting circuits may be utilized to suppress the inrush currents, but some subunits like HF receiver requires high nominal current threshold, which is settled too high to work correctly to suppress the capacitor bank charging current.

To implement both (short turn Off time and long turn On time) a special set of components applied to each output channel (7×) controlling the *dV/dt, dI/dt* is required, increasing the unit complexity, decreasing reliability and increasing cost. A novel approach, the digital inrush current limiter was employed rather. Two independent measures were implemented to suppress output inrush currents in LVPS.

The first method is a digital sequencer controlled by the FPGA softcore which prevents from turning on two or three units at the same time upon reception of such TC. Instruments are turned On with 50 ms delay between each other if they are commanded to turn On at the same time. The example of the input current spikes measured on the main 28 V input bus are depicted in Fig. 78. Without the sequencing, the sum of all three inrush currents is able to activate the LVPS overload protection and shut it permanently off.

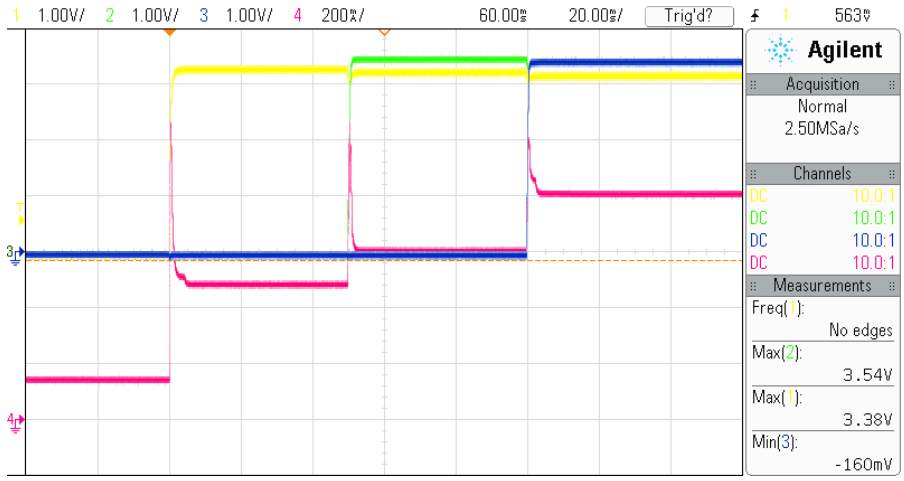


Fig. 78 The input power bus current captured during the sequenced instrument power on. Separation of 50 ms between HF, LP/MIME and LF instruments are visible, [SP-1].

The second feature of the FPGA softcore implemented is the so-called Digital Inrush Current Limiter, which utilizes similar approach as PWM modulation to chop the current flow through each power switch. Internal resistance of the output load as well as impedance of switches together with subunit capacity makes the current smoothing RC link. The maximum inrush current spikes suppressed by the reaction of proposed Digital Inrush Current Limiter could be seen in Fig. 79, where the same input and loading conditions were used.

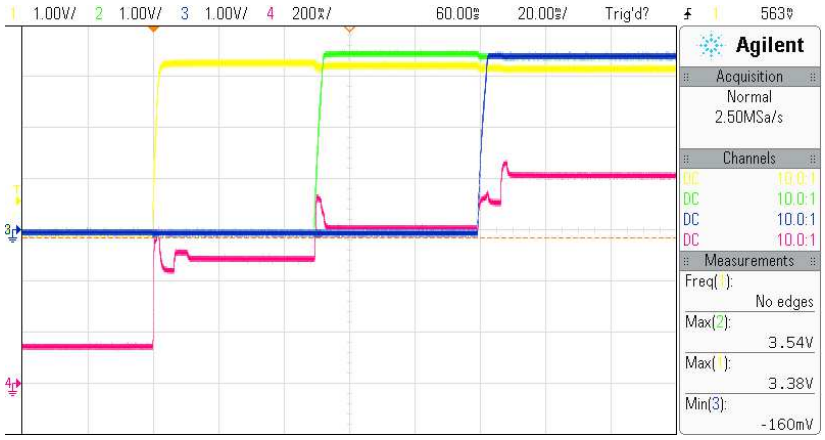


Fig. 79 The input power bus current captured during the sequenced instrument power on with suppressed inrush current spikes by the use of Digital Inrush Current Limiter, [SP-1].

Following paragraph is the auto-citation of the submitted paper [SP-1]: "The proposed minimum component count normally-off cold-redundant positive voltage rail power switch circuit implementation is given in Fig. 80.

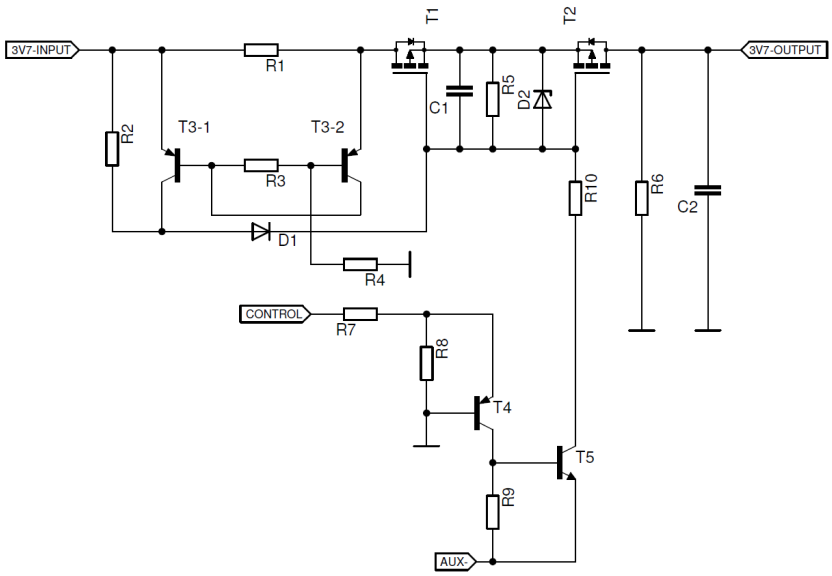


Fig. 80: SPF-Free Design Schematic Diagram of power distribution unit, positive 3.7 V Channel depicted, [SP-1].

The *MOSFET T1* acts as reverse protection diode minimizing voltage drop loss under nominal conductive conditions, whereas *T2* works as power switch in nominal conductive mode or constant current source shunt during the current limiting mode, driven by common control bias signal. Resistors *R5, R10* defines safe applied gate voltage region to fit the bias voltage between maximum gate-source and threshold voltage. The Zener diode *D2* is used to clamp the excessive voltage spike in case the over-voltage transient is applied to either 3V7-Input, AUX- or both. Low gain discrete voltage comparator realized using thermally coupled double transistor pair *T3-1, T3-2* and biasing set of passives *R2, R3, R4*, diode *D1* and current sensing resistor *R1* works together with *T1, T2* as short-term analogue current limiter for excessive current surges such as hard short circuit, inrush current or Single Event Latchup (SEL). Whilst total power dissipation on *T1* is mainly determined by internal body diode voltage drop and the current passing through, the most power dissipative part is *T2* which

have to be carefully thermally coupled to the unit chassis and/or sufficiently large copper plane.

Bleeding resistor *R6* and bypass capacitor *C2* shall be populated just once per cold-spared load rail. Transistors *T4, T5* serves as level shifter between LV-CMOS or TTL signaling with respect to GND potential and P-MOSFET V_{GS} drive with enough negative bias to operate both *T1* and *T2* in saturated regions. The circuitry operates with positive logic, thus log. 1 turns the switch on and vice versa.

Optionally, a fast free-wheeling diode could be installed in antiparallel to *C2* to prevent over-voltage damage caused by inductive loads. As a negative bias potential, the -9V75 rail is utilized. Cold-sparing assumes that each power supply has its own AUX- voltage source, which is at 0 V during the converter off state. Summing is performed by the interconnection of 3V7-OUTPUT and GND between all cold-redundant power supply units. Auxiliary negative bias voltage has to be left with no connection.
Conventional state-of-the-art power MOSFETs in space-grade with no heat sink mount (such as *SMD.5, SMD1, SMD2*) allows scaling of this circuit up to the level of 6 Amps when current limiting mode and associated power loss vs. time product is considered and kept within the de-rated Safe Operating Area.",

"The adoption of more than two cold-spared units based on proposed design is feasible and by principle not limited. Leakage currents of the respective switch have to be taken into account, however to prevent permanent low current DC biasing of associated loads."

Each current sensing channel is electrically set by gain resistors to match the output readout up to 175% of peak current and trip off on 140% as default value, which could be modified using the Telecommand from the DPU whenever, during the flight. The maximum of 175% is hardware defined value, which could not be changed during the flight, as it is given by the gain setting output resistor connected to the each output of MSK496 I/V converters. Nearest values of gain settings resistors, whilst keeping two 100 ohm differential input resistors on all channels (by the *MSK496* datasheet), are picked up to be contained in E96 resistor value series.

In Tab.: 9 all measures in current and voltage sensing and processing chain, including digital values expected to be read at respective 140% and 175% levels are summarized.

Whilst the ADC has a reference voltage of V_{DD} (3.3 V), the maximum available voltage on I/V converter output is about 2.5V, thus direct optimal fit to 0-3.3V scale is not possible, which reduces amount of discrete readout steps and precision. Calculations assumes fit of the I/V converter output to max. 2.32 V (at 175% load) to keep the I/V converter output in linear mode. Note: DPU rail line is for housekeeping measurements fit only. No switch is implemented.

Tab.: 9 Current and voltage readout conversion table for the FPGA digital OVC, OVP threshold settings.

Rail	Current Sensing R [ohm]	Maximum Readout	Desired Limit in %	Desired Trip Off Limit in %	Maximum Peak Current Declared by Instruments ICD	Maximum I/V Converter Output Voltage	Necessary I/V Converter Gain	Voltage Output at gain = 1	Voltage Output at gain = 100	Maximum Output at Corrected Gain	Maximum Output at Corrected Gain, 175% overload	Trip Off Voltage (140% of Peak Current) to FPGA Registers	Trip Off Digital Value (140% of Peak Current) to FPGA Registers	Maximum Digital Value in 175% Load	Corrected Gain	I/V Converter Output Loading Resistor (E96 Series)
DPU 3V7	0,039	180	175	140	0,773	2,320	43,981	0,0301	3,01	1,302	2,2791132	1,8232906	**141**	**177**	43,2	**4320**
LF 3V7	0,039	180	175	140	0,505	2,320	67,321	0,0197	1,97	1,310	2,2920056	1,8336045	**142**	**178**	66,5	**6650**
LF 10V	0,2	180	175	140	0,114	2,320	58,153	0,0228	2,28	1,313	2,29824	1,838592	**143**	**178**	57,6	**5760**
LP 3V7	0,039	180	175	140	0,42	2,320	80,946	0,0164	1,64	1,320	2,310399	1,8483192	**143**	**179**	80,6	**8060**
LP 10V	0,2	180	175	140	0,14	2,320	47,353	0,0280	2,80	1,299	2,2736	1,81888	**141**	**176**	46,4	**4640**
LP -10V	0,2	180	175	140	0,14	2,320	47,353	0,0280	2,80	1,299	2,2736	1,81888	**141**	**176**	46,4	**4640**
HF 3V7	0,027	180	175	140	2,335	2,320	21,031	0,0630	6,30	1,324	2,3169038	1,853523	**144**	**180**	21	**2100**
HF 10V	0,2	180	175	140	0,133	2,320	49,846	0,0266	2,66	1,295	2,266985	1,813588	**141**	**176**	48,7	**4870**

Rail	Desired Maximum Limit in %	Desired Trip Off Limit in %	Required Divider Ratio to fit 3.3V at 175%	R1 low side resistor Selection	R2 high side resistor	R2 High Side resistor (E96 series)	Maximum Readout Value at 175%	Nominal Readout Value at 100%	Trip Off Value for Desired Trip Off Limit
3,70	175	110	0,50965251	3300	3175	3240	253	**145**	**159**
9,75	175	120	0,19340659	3300	13762,5	14000	252	**144**	**173**
-9,75	175	120	-0,19340659	Input Divider 10k + 10k, feedback R = 1k91			252	**144**	**173**

Following paragraph is the auto-citation of the submitted paper [SP-1]: "All three secondary side rectifiers are equipped with a bank of capacitors based on high capacity tantalums and high-quality *MLCCs* to provide with excellent noise reductions from DC up to the desired 50 MHz operational band. Ultra-low ESR capacitors in a total of *2000 μF* per voltage level require special current limiting technique to be implemented to prevent the surge damage of either subsystem loads and/or *LVPS* itself. Each load adds its own local capacitor bank to furthermore improve the total *RPWI* self-generated noise performance. The direct start-up current is then theoretically limited only by internal impedance of all capacitors, power switches, harness and current sensing resistor *R1*.

Analog (hardwired, BoL) current limit threshold of the proposed power switch shall be set to 200% of nominal full power load to prevent unwanted voltage drop at the unit EoL in case of dramatic aging or unexpected radiation damage. For the 5 A nominal current, 10 Amp level shall be thus set. For example in the case of 3.7 V voltage rail the total power limit is then close to 37 Watts. Assuming non-ideal converter efficiency and 28 V input voltage, the converter is drawing approximately 50 W of peak power during turn-on output load command.

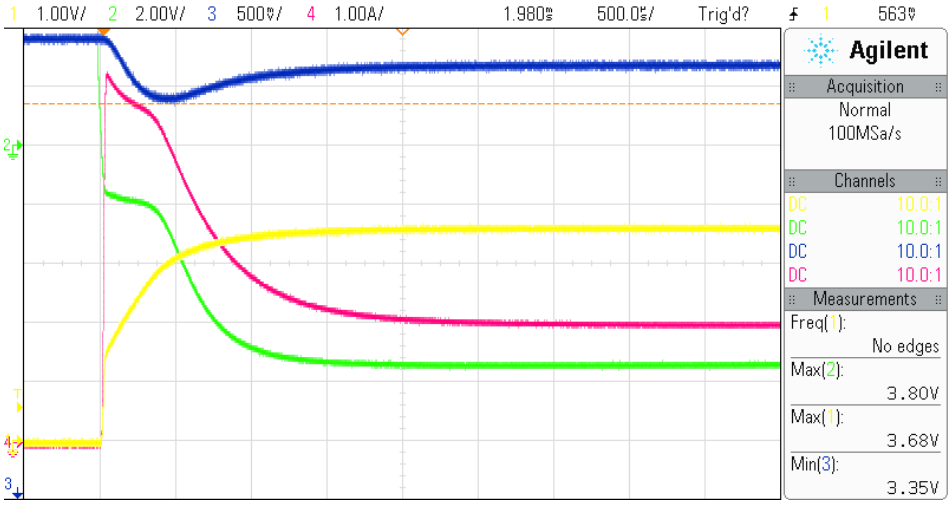


Fig. 81 Full load inrush current profile using the analog current limiter only, [SP-1].

In converter with no direct feedback between the secondary outputs and the primary side of the pre-regulating Step-down stage, high current surge loads the respective voltage rail and causes the undervoltage condition. Subsystems are equipped by the low drop (100-200 mV) Point-of-Load (*PoL*) regulators to provide with firm locally stabilized 3.3 V. In Fig. 81 the undervoltage conditions with the analog current limiter set to a maximum of 6 A shows the unacceptable undervoltage drop down to a level of 3.35 V prior the *PoL*.

In Fig. 81. the channel 1 (yellow) represents output load voltage, channel 2 (green) MOSFETs Gate-GND voltage, channel 3 (blue) DPU or 3.7V internal converter voltage and channel 4 (red) displays the output load inrush current reaching 6 Amps. A plateau holding the gate voltage for 500 μs around the transistors' threshold voltage displayed in channel 2 trace shows the MOSFET operating in linear mode as the current source. The *RPWI DPU* utilized as a minimum load to keep the converter in continuous conduction mode (*CCM*) with no power switch between LVPS-DPU may be experienced with brown-out resets or sudden system freezing during such events. The reaction time of the analog power switch (turn-on ramp) could be prolonged using capacitor C1 to a desired value. However, the turn-off time is then delayed accordingly and could not be changed during the flight where it might be required.

In case the converter is not connected to any minimum load or such load needs to be disconnectable, the softcore implements control outputs to artificial load switch to keep it in the CCM. Auxiliary load outputs shall be then connected to BJT switch with an associated dummy.

The plot timescale shows the undervoltage transient takes approximately 1 ms. It is very impractical to implement balancing capacitive bank for such a long period of time and several Amp load.

To suppress the peak inrush current level and sustain the converter (3.7V-INPUT) internal voltage within specified boundaries, the pulsed inrush current limiter with variable duty cycle and length was developed, implemented into the FPGA softcore and validated. In Fig. 82 the chopped inrush current profile is indicated in channel 4 (red).

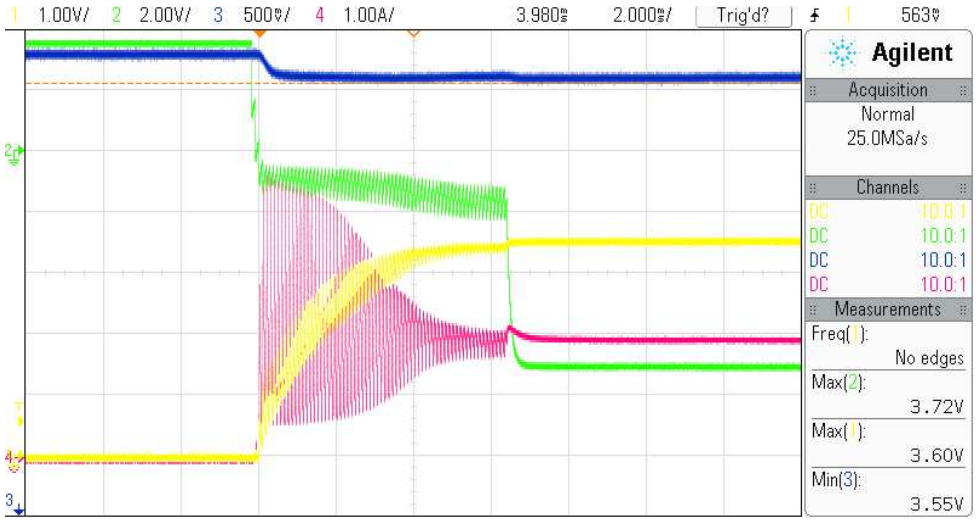


Fig. 82 Full load inrush current profile using the Digital Inrush Current Limiter, [SP-1].

Longer timescale in Fig. 82 indicates that the linear mode of MOSFET switches (channel 2, green) is easily utilized in order of magnitude longer time. With optimized duty-cycle vs. pulse length factors, no out-of-specification undervoltage condition is observed on converter internal voltage during the subsystem load charging period. Minimum reached voltage is determined as 3.55 V, or 200 mV higher than without the pulse control. Pulse frequency is set to 10 kHz. Not populated C1 capacitor keeps the turn-off reaction time determined mostly by the MOSFETs gate charge and discharging resistor R5. Practical shutdown times are in order of tens to hundreds of microseconds, whilst turn on ramps could be as of 50 ms long."

5.5. Objective D)

A new European structural funds research project on high-energy physics in atmosphere has started in the Czech Republic, under the name CRREAT (Research Center of Cosmic Rays and Radiation Events in the Atmosphere), [R-22]. The project is according to [R-22] focused on deepening the knowledge about the relation between the atmospheric phenomena and ionizing radiation (IR) and clarifying the phenomena causing variations of the secondary cosmic rays (CR) in the atmosphere. For this project, a miniature solid-state dosimeter based on the low voltage biased silicon sensor was developed, tested and flown on the High Altitude Balloon in January, 2018.

With dimensions of 53×32×14 mm, power consumption below 70 mW @ 5 V continuous, the gamma sensitivity range of 0.2 up to 10 MeV and digital signal processing, the developed piDOSE-DCD Digital CubeSat Dosimeter belongs to the state-of-the-art radiation measurement sensors, fully replacing obsolete and fragile Geiger-Müller tubes or RadFET (cumulative dosimetry) based dosimeters. The data from the flight in were published in [PP-12], [PP-13].

The instrument is depicted in Fig. 83 and measured in-flight data in Fig. 84.

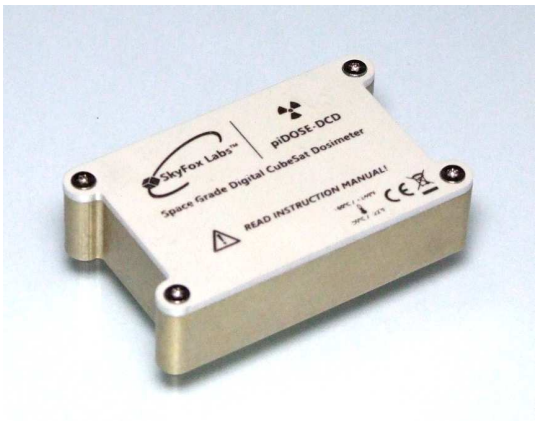


Fig. 83 The Digital CubeSat Dosimeter piDOSE-DCD used during the HAB flight.

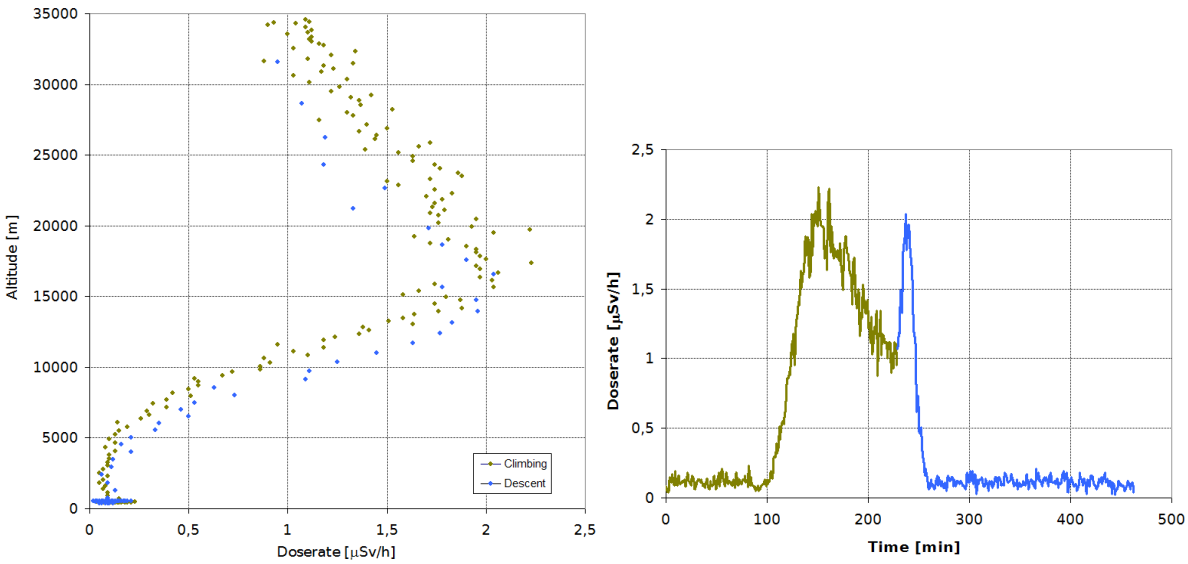


Fig. 84 The doserate vs. altitude dependency (left), doserate vs. mission elapsed time (right) were measured by the piDOSE-DCD Digital CubeSat Dosimeter, [PP-12].

6. Conclusions

The trend of the space electronics and satellite design in the past decade after the massive deployment of CubeSats and microsatellites shown the importance of the knowledge base to maximize the mission operations. So far, about 50% of all small satellite missions were not able to achieve planned mission goals due to various design issues.

The Thesis is a result of the seven years long research of the space environment impact on the modern electronic parts. The space vacuum, radiation and thermal stress differs mission by mission, however if processes degrading the physical properties of individual part are understood, the designer is able to apply special measures which will increase the lifetime.

There are a total of ***four goals addressed***, studied and ***successfully concluded***. At first, to analyze the state-of-the-art space grade power supply converters and power electronics and publish the summary. Next, to identify bottlenecks of electrical components and propose novel power electronics concepts with aim for deep space and interplanetary missions. In both cases find its applications within the *CzechTechSat* and *ESA LPM/L-DEPP* projects. Next, to implement the application of proposed methods for very low noise, cold-redundant low voltage power supply unit for *ESA/JUICE* scientific instrument. Last, but not least to develop the miniature, low power solid-state dosimeter for small satellites with aim to cover wide energy spectra of gamma rays and to perform the high-altitude balloon test flight to validate the system for the project *CRREAT*. All above mentioned goals were achieved successfully with published results together with a total of ***14 validated scientific hypotheses***.

The novelty of the proposed PhD candidate work could be seen in following achievements:

1) The field of space radiation impact on semiconductors was studied with the aim for modern commercial electronics. Results from the study were published and implemented in the CubeSat-class mission ***CzechTechSat***, such as the ***FRAM-based Triple Module Redundancy Cold-Redundant On-Board Computer*** or in-flight reconfigurable ***Fluxgate Magnetometer Payload***. As the extension of the work, principles were implemented in the ***ESA/Lunar Lander Langmuir Probe and Magnetometer (LPM)***, under the frame of *L-DEPP* project.

2) A novel concept of the ***Discrete Component based Cold-redundant Ultra Low Noise DC/DC Power Converter*** for deep space mission with no optical or magnetic feedback was designed, developed and tested. It represents the single point of failure free solution which does not exist as a single chip or ready-made product, such as radiation hardened hybrid power converters. The application of the concept is tailored to the *ESA/JUICE* mission, *RPWI* instrument.

3) The ***In-Flight Reconfigurable Cold-Redundant Power Distribution Node with Digital Inrush Current Limiter*** for deep space missions was developed, implemented and tested with results sent for publishing. It is a smart power distribution circuit suppressing greatly the in-rush currents in space-grade power systems with the on-the-fly parametric change feature.

4) The ***Advanced Ultra Low Power Miniature Dosimeter*** for small satellites with solid-state radiation sensor and digital output covering the spectra of gamma rays between ***0.2-10 MeV*** was developed and tested. It replaces the vintage and fragile *Geiger-Müller* tubes and slow (cumulative) dose sensing *RadFETs* not suitable for in-situ measurements at orbital velocities. The unit provides with the immediate radiation situation monitoring with up to 1 second update rate radiation alarm, miniature dimensions *53×32×14 mm*, ***70 mW @ 5 V***.

7. List of Publications

7.1. Published Papers

[PP-1] *Laifr, et al.: The CzechTechSat – A Space-friendly CubeSat-class Picosatellite, 10th Annual CubeSat Developers' Workshop, Cal Poly, Apr. 24th 2013, San Luis Obispo, CA, USA*

[PP-2] *Hans-Ulrich Auster, Stuart D. Bale, Gregory T. Delory, Pierre Devoto, William M. Farrell, Karl-Heinz Glassmeier, Lars Guicking, Jasper S. Halekas, Petr Hellinger, David Hercik, Mihaly Horanyi, Dhiren Kataria, Zdenek Kozacek, Jaroslav Laifr, Christian X. Mazelle, Yoshiharu Omura, Christopher J. Owen, Roman Pavelka, Ferdinawnd Plaschke, Helmut O. Rucker, Yoshifumi Saito, Zoltan Sternovsky, Stepan Stverak, Pavel M. Travnicek, Paul Turin, Petr Vana: LUNAR DUST ENVIRONMENT AND PLASMA PACKAGE FOR LUNAR LANDER – DEFINITION STUDY. Poster, American Geophysical Union Fall Meeting, 7 December 2012, San Francisco, CA, USA*

[PP-3] *Laifr, J.: Review of Ionizing Radiation Impact on Semiconductors. In ICMT'13 - Proceedings of the International Conference on Military Technologies. Brno: Univerzita obrany, 2013, p. 1001-1014. ISBN 978-80-7231-917-6.*

[PP-4] *Laifr, J. - Papaj, J.: Space-Friendly Attitude Determination and Control Subsystem for CubeSat-class Mission. In ICMT'13 - Proceedings of the International Conference on Military Technologies. Brno: Univerzita obrany, 2013, p. 873-878. ISBN 978-80-7231-917-6.*

[PP-5] *Laifr, J. et. al.: Lunar Dust Environment and Plasma Package for Lunar Lander - Definition Study, In: 9th INTERNATIONAL PLANETARY PROBE WORKSHOP,[USB]. Toulouse: ISAE campus, 2012*

[PP-6] *Laifr, J.: Design of the Fault Tolerant On-Board Computer for CubeSat-class Satellite. In POSTER 2012 - 16th International Student Conference on Electrical Engineering [CD-ROM]. Praha: Czech Technical University in Prague, 2012, p. 1-6. ISBN 978-80-01-05043-9.*

[PP-7] *Laifr, J., Papaj, J., Pačes, P., Plaček, V., Houštecký, L., The CzechTechSat Project - Experimental University 2U-format Picosatellite, Small Satellites Systems and Services - the 4S Symposium 3 - 8 June 2012 Grand Hotel Bernardin Convention Centre, Portorož, Slovenia, [CD-ROM], Noordwijk: ESA Publications Division, 2012. p. C17-1-C17-11.*

[PP-8] *Pačes, P., Šipoš, M., Laifr, J., Batěk, M.: Small Satellite Systems Control for University Curriculum. In 62nd International Astronautical Congress [CD-ROM]. Cape Town: South African National Space Agency (SANSA), 2011, ISSN 1995-6258.*

[PP-9] *Laifr, J., et al. The CzechTechSat Stratospheric Balloon Flight Preparatory. In: Proceedings of 2014 PEGASUS-AIAA Student Conference. 2014 PEGASUS-AIAA Student Conference. Prague,23.04.2014 - 25.04.2014. Praha: České vysoké učení technické v Praze. 2014, ISBN 978-80-01-05459-8.*

[PP-10] *Laifr, J., Yang, N. Telemetrický, sledovací a povelovací datový spoj pro stratosferické balonové experimenty. [Funkční vzorek]. 2014*

[PP-11] *Laifr, J. Low Voltage Power Supply for Radio and Plasma Waves Investigation (RPWI) instrument, ESA JUICE. In: ŠIPOŠ, M., ROHÁČ, J., a ALAM, M., eds. Sborník konference "What's New in Aerospace?". What's New in Aerospace?. Praha, 29.11.2016 - 30.11.2016. Praha: České vysoké učení technické v Praze. 2016, ISBN 978-80-01-06042-1. http://aerospace.fel.cvut.cz/conference2016*

[PP-12] *Laifr, J.; Kovář, P. HIGH ALTITUDE BALLOON TEST FLIGHT OF MINIATURE LOW POWER DOSIMETER FOR SMALL SATELLITES, Slaboproudý obzor. 2018, 74 1-3. ISSN 0037-668X.*

[PP-13] *Puričer, P.; Laifr, J.; Kovář, P.; Mikeš, J. Telemetry System of FIK III. Stratospheric Balloon, In: 2018 28th International Conference Radioelektronika. IEEE (Institute of Electrical and Electronics Engineers), 2018. ISBN 978-1-5386-2485-2.*

[PP-14] *Laifr, J., Draxler, K., Štverák, Š., Trávníček, P. M., Design of the Low Voltage Power Supply for Radio and Plasma Waves Investigation instrument and ESA/JUICE Mission, International Journal of Applied Science and Technology. 2018, 8(2), ISSN 2221-0997*

7.2.Submitted Papers

Note: Review Pending to date of the Thesis delivery (August 2018).

[SP-1] *Laifr, J., Draxler, K., Štverák, Š., Trávníček, P. M., In-Flight Reconfigurable Cold-Redundant Power Distribution Node for Deep Space Missions, IEEE Transaction on Aerospace and Electronic Systems, Manuscript no.: TAES-201800875 , ISSN: 0018-9251*

7.3.Functional Samples

[FS-1] *Laifr, J., Speciální pomaloběžná navíječka, Functional Sample. 2011.*

[FS-2] *Laifr, J.: Papaj, J., Straka, M.: Reliable Attitude Determination and Control Subsystem, 2013*

[FS-3] *Laifr, J.: Papaj, J.: Reliable Onboard Computer for CubeSat-class Picosatellite, 2013*

[FS-4] *Laifr, J. Zařízení pro testování stabilizačních subsystémů a zdrojů elektrické energie pro satelity třídy CubeSat. 2013, Dostupné z: http://czechtechsat.cz*

[FS-5] *Laifr, J.; Yang, N., Telemetrický, sledovací a povelovací datový spoj pro stratosferické balonové experimenty, Functional Sample. 2014.*

[FS-6] *Laifr, J., Kovář, P. Special CubeSat LED Flash Panel Demonstrator for Space Use. 2015*

7.4.Associated Master Theses

During this Ph.D. candidate work, several associated Master theses were conducted directly or indirectly with students from Faculty of Electrical Engineering and Faculty of Mechanical Engineering, CTU in Prague. All topics were related to the CzechTechSat project, its subsystems and related ground support equipment. All published Theses could be found via the National Technical Library of the CTU in Prague or at dedicated department libraries. Note: The list below uses English translations of particular Theses names.

[MT-1] *Bc. Jan Papaj, "On-Board Computer for CubeSat-class Satellite", Faculty of Electrical Engineering, CTU in Prague, 2013*

[MT-2] *Bc. Ning Yang, "Telemetry, Tracking & Commanding Subsystem for the CzechTechSat Picosatellite", Faculty of Electrical Engineering, CTU in Prague, 2014*

[MT-3] *Bc. Radovan Vlach, "Miniature combined VHF/UHF antenna mechanism for the CzechTechSat Satellite", Faculty of Mechanical Engineering, CTU in Prague, 2014*

[MT-4] *Bc. Lukáš Houštecký, "CubeSat-class Magnetometer Payload", Faculty of Electrical Engineering, CTU in Prague, 2014*

[MT-5] *Bc. Lukáš Forman, "Thermal analysis of the modern-concept small satellite", Master Thesis, Faculty of Mechanical Engineering, CTU in Prague, 2015*

[MT-6] *Bc. Matej Straka, "Simulation software for the satellite attitude control", Faculty of Electrical Engineering, CTU in Prague, 2016*

7.5. Media and Public Relations

[PR-1] *Pražská technika, PT 1/2013, "Evropský projekt studentského satelitu CzechTechSat", p. 10, 13, printed*

[PR-2] *Deník Metro, 17.9. 2014, "ČVUT má satelit", p. 3, printed*

[PR-3] *5+2 / Praha, 26.9. 2014, "Česko má vlastní družici. Díky studentům", front page, printed*

[PR-4] *7 statečných, "Družice studentů ČVUT se chystá na oběžnou dráhu", 10.10. 2014, http://www.sedmstatecnych.cz/clanek/druzice-studentu-cvut-se-chysta-na-obeznou-drahu/, online*

[PR-5] *Technický týdeník, 23-29.9. 2014, "Kosmická kostka z Fakulty elektrotechnické ČVUT je technologický unikát", p. 4, printed*

[PR-6] *TECNICALL, II 2014, "Vesmírná kostka / Studenti sestavují družici", p. 3, printed*

[PR-7] *Náš REGION, Čtvrtek 11.2. 2016, "Mise na Jupiter s přispěním českých vědců", front page, printed*

[PR-8] *Česká televize, Studio 6, Ranní infoservis, "Vývoj studentského satelitu", https://www.ceskatelevize.cz/ivysilani/1096902795-studio-6/214411010100917/obsah/350788-vyvoj-studentskeho-satelitu, online, TV shot, 17.9. 2014*

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[PR-10] *Slovenská Televize (RTVS), Svet v obrazoch, "Projekt CzechTechSat", http://www.rtvs.sk/televizia/archiv/13097/52968#58, TV shot recorded, 0:00 - 3:27.*

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[R-8] *A.M. Albadri, R.D. Schrimpf, K.F. Galloway, D.G. Walker, Single event burnout in power diodes: Mechanisms and models, Microelectronics Reliability, Volume 46, Issues 2–4, 2006, Pages 317-325, ISSN 0026-2714*
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