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August 2018 *Ing. Tomáš Nápravník*

Czech Technical University in Prague
Faculty of Electrical Engineering
Department of Microelectronics

AN AUTOMATED METHOD FOR CALIBRATION OF MODELS OF INTEGRATED ESD PROTECTION STRUCTURES

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Ing. Tomáš Nápravník

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Abstract (EN)

Electro-static discharge (ESD) presents serious threat for reliability and lifetime of any integrated circuit and has to be carefully addressed in every design. Without ESD protection circuits, yield of IC production would drop dramatically as the electro-static discharge occurs not only in field applications of ICs but also during their fabrication, testing, packaging, and installment of the final part to a module. To aid ESD designer to achieve optimal level of protection, dedicated macro-models must be introduced to process design kits (PDK). Characterization of such macro-models is time and resource demanding task that is performed by experienced personnel. Simplification of this characterization task is thus desirable and is one of the goals of this thesis. Novel automated simulator-independent ESD model characterization method based on Differential evolution and Nelder-Mead Simplex algorithms is presented. It offers an alternative for time and human-resources demanding manual characterization that is still widely used in industry. Instead of a large quantity of independent measurements of an ESD protection device, single TLP or TLP-like measurements are used to calibrate macro-models of ESD protection devices. As modern TLP measuring systems are often automated, it further alleviates the engineering effort required for the calibration. Additionally, computationally stable macro-models of the four most often used snapback based protection devices in bulk CMOS technologies are presented. Those include ESD NMOST and three variants of silicon-controlled rectifier structure. These macro-models were used to benchmark the proposed calibration method. Custom designed integrated circuit with set of NMOST-based ESD protection structures was fabricated in 130nm bulk CMOS process as part of the presented research. Finally, to help the reader understand the complexity, challenges, and possible compromises in a field of an integrated circuit ESD protection design, basic overview of ESD resilient design practices are included in the work.

Abstract (CZ)

Elektrostatický výboj (ESD) představuje velmi nebezpečný jev, který dokáže v několika málo okamžicích poškodit analogové i digitální bloky integrovaných systémů. Bez efektivních ochranných prvků by prudce klesla výtěžnost výrobních linek integrovaných obvodů, neboť ESD není jevem spojeným jen s používáním konečného produktu, ale je často se vyskytujícím fenomenem při výrobě, testování, pouzdření a osazování integrovaného obvodu do finálního modulu zařízení. Významnou výhodou při návrhu systému ESD ochran je dostupnost speciálních ESD macro-modelů v používaných knihovnách součástek. Charakterice takovýchto macro-modelů je netriviální, časově náročná operace, vyžadující zkušeného odborníka. Možnost zjednodušení procesu charakterizace je proto velmi žádoucí a je jedním z cílů této práce, která představuje vyvinutou metodu automatizované charakterizace ESD macro-modelů za použití standardního TLP či TLP-podobného měření. Alternativní přístup k charakterizaci ESD macro-modelů zahrnuje měření mnoha separátních charakteristik a vyžadují značné množství času. Další součástí práce je analýza dostupných metod modelování jevů spojených s ESD v CMOS ochranných prvcích. Představuje vhodné macro-modely pro čtyři z nejčastěji používaných ESD ochranných struktur v CMOS výrobních procesech: ESD NMOST a tři varianty tyristorové struktury. Představená metoda byla otestována právě na charakterizaci těchto čtyř macro-modelů. Jako vstupní data pro ESD NMOST byla použita TLP měření provedená na testovacích strukturách vyvinutých speciálně pro tento výzkum ve 130nm CMOS technologii. Poslední významnou součástí práce je stručný úvod do návrhu ESD ochranných struktur v integrovaných obvodech, který by měl čtenáři přiblížit problematiku designu a charakterizace těchto struktur.

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List of Acronyms

Notation	Description	Page List
BJT	bipolar-junction transistor	7–10, 40, 42, 43, 45, 46, 49, 54
BSIM	Berkeley short-channel IGFET model	42–44, 54
CAD	computer-aided design	5
CDM	charged-device model	22, 27, 30
CMOS	complementary MOSFET	20, 35, 79, 80, 84
DC	direct current	9, 72, 76, 104
DE	differential evolution	7, 8, 17, 18, 62, 64, 68, 70, 71, 73, 74, 85, 102
DRC	design rule check	80
DUT	device under test	8, 9, 29, 30, 57–59, 73, 89, 91, 96, 98
ESD	electrostatic discharge	8, 9, 15–21, 23–30, 32, 35–37, 40, 41, 44–47, 54, 57, 59, 61, 69, 70, 72, 73, 79, 80, 87, 91, 94, 96, 101–105
GCNMOST	gate-coupled NMOST	11, 38–40

Notation	Description	Page List
GGNMOST	gate-grounded NMOST	11–13, 18, 35–38, 48, 53, 79–82, 87–90, 102, 105
GIDL	gate-induced drain leakage	70
GPIB	general purpose interface bus	69
HBM	human body model	12, 13, 18, 27–29, 36, 57–59, 84, 87, 89, 91, 92, 94–96, 98–100, 102, 104, 105
I-V	current versus voltage	9, 10, 12, 13, 17, 24, 25, 28, 36, 38, 45–47, 57, 59, 70, 72–74, 76, 87–92, 94–96, 98, 99, 103–105
I/O	input/output	11, 18, 20, 21, 23, 28, 30, 35, 36, 38, 46, 48, 69, 79, 84, 87, 91, 94, 96
IC	integrated circuit	9, 15, 19, 20, 22, 27, 46, 59, 69, 79, 80, 101, 102
IP	intelectual property	32
LVS	layout versus schematic	80
LVTSCR	low-voltage triggered silicon controlled rectifier	11–13, 17, 18, 35, 53–55, 79, 84, 96, 98–100, 102, 103
MLSCR	modified lateral silicon controlled rectifier	11–13, 18, 35, 50–53, 79, 84, 94–98, 102
MM	machine model	27–29, 57, 84
MOSFET	metal-oxide-semiconductor field-effect transistor	7–10, 21, 25, 37, 42, 47, 70, 79, 81

Notation	Description	Page List
NMOST	n-channel MOSFET	9, 11, 17, 21, 35–38, 42–45, 47, 49, 53, 54, 74, 76, 87, 90, 99, 103
NMSA	Nelder-Mead simplex algorithm	7–10, 17, 18, 64, 68, 71, 73, 74, 86, 102
NPN	type of bipolar transistor with n-type collector and emitter and p-type base	17, 35, 36, 42, 45, 46, 50, 53, 54, 76, 90, 93, 97, 99, 103
PDK	process design kit	42, 44, 54, 70, 102, 104
PMOST	p-channel MOSFET	21
PNP	type of bipolar transistor with p-type collector and emitter and n-type base	17, 46, 49, 50, 53, 54, 76, 93, 97, 103
RAM	random-access memory	15
RF	radio frequency	70, 84
SCBE	substrate current induced body effect	70
SCR	silicon controlled rectifier	9, 11–13, 17, 18, 25, 35, 46–53, 70, 74, 76, 79, 84, 91–94, 102
SGP	SPICE Gummel-Poon	17, 43, 49, 50, 54, 93, 97, 103
SPICE	simulation program with integrated circuit emphasis	5, 17
TCAD	technology CAD	102, 104, 105
TLP	transmission-line pulse	9, 12, 13, 17, 18, 27, 28, 57–59, 69, 72, 81, 87, 88, 90, 103, 104

Notation	**Description**	**Page List**
VBIC	vertical bipolar inter-company	7–9, 17, 42–44, 49, 50, 54, 90, 93, 97, 99, 103
WRMSD	weighed root-mean-square deviation	72

List of Symbols

Notation	Description	Page List
A_{VC1}	linear avalanche-current coefficient of VBIC BJT model (V^{-1})	43, 49
A_{VC2}	exponential avalanche-current coefficient of VBIC BJT model (V^{-1})	43, 49
α_0	absolute MOSFET macro-model length-dependency substrate-current coefficient (AV^{-1})	43
α_1	linear MOSFET macro-model length-dependency substrate-current coefficient ($AV^{-1}m^{-1}$)	43, 44
α_{n}	electron impact-ionization factor (1/m)	51
α_{NMSA}	reflection coefficient in NMSA (−)	65, 66
α_{p}	hole impact-ionization factor (1/m)	51
β	exponential MOSFET macro-model V_{DSeff}-dependency substrate-current coefficient (V^{-1})	40, 41, 43, 46, 76
β_{NMSA}	contraction coefficient in NMSA (−)	67
CR	paramater of differential evolution; crossover coefficient (−)	63, 85
D	paramater of differential evolution and Nelder-Mead simplex; number of variables in vector of parameters, dimensionality of population member in DE and number of polyhedron vertices in NMSA (−)	9, 62, 63, 65, 67
ϵ_{stop}	error of the simplex vertices function values used to terminate the NMSA flow	67
F	paramater of differential evolution; weighing factor in DE population-member calculation (−)	85
f_{obj}	objective function (−)	64, 72

Notation	Description	Page List
$f_{\text{obj}}^{\text{TERM}}$	termination value of the objective function (−)	73, 74, 85, 86
f_{w}	weighting vector, part of the calibration method objective function definition (−)	72
G	paramater of differential evolution; generation index (−)	62, 64
G^{II}	impact ionization generation rate (1/s)	51
γ_{NMSA}	expansion coefficient in NMSA (–)	66
$I_{\text{gc}}^{\text{BJT}}$	impact-ionization current of MOSFET macro-model, internal-VBIC part (A)	43, 49
I_{C}	collector current of BJT (A)	43, 74
I_{D}	drain current of MOSFET (A)	43, 74
I_{DUT}	current through DUT (A)	58
I_{dsa}	MOSFET drain current without impact-ionization effect (A)	43
I_{gen}	junction avalanche current (A)	43, 74
I_{h}	snapback or hold current of ESD protection device (A)	36, 45, 90, 94, 98, 99
$I_{\text{sub}}^{\text{MOS}}$	substrate current of MOSFET macro-model, internal-MOSFET part (A)	43
I_{S}	saturation current of BJT or diode (A)	76
I_{t1}	current corresponding to the trigger voltage V_{t1} (A)	36, 40, 45, 47, 90, 94, 98, 99
I_{t2}	failure or second-breakdown current (A)	10, 25, 26, 40, 41, 105
I_{tot}	total leakage current through the base-collector junction of VBIC BJT model (A)	43, 49
L	MOSFET channel length (m)	81
$L_{\text{d,noSAL}}$	length of un-salicided drain region of MOSFET (m)	81
L_{eff}	effective length of MOSFET channel, resistor or other relevant device (m)	43, 44
M	avalanche multiplication factor (−)	36, 43, 74, 76
M_C	VBIC BJT base-collector junction gradient coefficient (−)	43, 49
n	concentration of free electrons in a semiconductor (m^{-3})	51
N_{f}	number of fingers (or *folds*) of MOSFET (−)	81
NP	paramater of differential evolution; size of a population in a single DE generation (−)	62, 64, 85
$\bar{P}$	simplex centroid in NMSA	65–67

Notation	Description	Page List
P	single point of a simplex in D-dimensional space in NMSA	65–67
p	concentration of free holes in a semiconductor (m^{-3})	51
R_{sh}	sheet resistance (Ω)	44
$R_{d,noSAL}$	resistance of the integrated drain-side ballast resistor using salicide blocking mask used in MOSFET-based ESD protection structures (Ω)	37, 44
R_{L}	matching resistance at the end of TLP transmission line (Ω)	58
R_{nw}	n-well resistance of SCR-based devices (Ω)	49, 54
R_{on}	dynamic resistance in snapback or hold state (Ω)	37, 40, 41, 45, 59, 87, 89–91, 94, 96, 98, 99
R_{pw}	p-well resistance of ESD NMOST or SCR-based devices (Ω)	36, 44, 49, 54
$\boldsymbol{t}$	vector of differential evolution; auxiliary vector containing random numbers following uniform distribution	63
$\boldsymbol{u}$	vector of differential evolution; trial vector derived from population members of the same generation	62, 64
$\boldsymbol{v}$	vector of differential evolution; crossover vector (new parameter vector for single member of the $(G+1)$-th generation)	63
V_{bci}^{mod}	built-in potential of VBIC BJT base-collector junction diminished by voltage drop accross the junction (V)	43, 49
V_{bd}	first-breakdown voltage of an ESD device (V)	25, 36, 41
V_{DD}	positive DC power voltage of IC (V)	26
V_{DUT}	voltage measured on DUT (V)	58
V_{DS}	drain–source voltage of MOSFET (V)	43, 74, 76
V_{dsat}	drain saturation voltage of MOSFET (V)	43, 44, 74, 76
V_{DSeff}	effective drain–source voltage of MOSFET (V)	7, 43
V_{GS}	gate–source voltage of MOSFET (V)	44, 76
V_{h}	snapback or hold voltage of ESD protection device (V)	25, 26, 36, 41, 45–47, 52, 53, 89–91, 94, 96, 98, 99
V_{in}	DC voltage of an input voltage source (V)	58
V_{meas}	measured set of voltage data, e.g., I-V characteristic (V)	72
v_{n}	electron velocity (m/s)	51
v_{p}	hole velocity (m/s)	51

Notation	Description	Page List
V_{sim}	set of voltage data gathered by a simulation, e.g., I-V characteristic (V)	72
V_{t1}	trigger voltage of protection device (V)	8, 24–26, 36–38, 40, 41, 45, 47, 51–53, 89–91, 94, 96, 98, 99
V_{t2}	voltage corresponding to the failure current I_{t2} (V)	37, 38
V_{th}	threshold voltage of MOSFET (V)	44
w_{B}	effective width of parasitic BJT in MOSFET (m)	40
w_{BD}	depletion width of the reverse-biased junction between the drain diffusion and the bulk of MOSFET (m)	40
$w_{\mathrm{eff,tot}}$	effective total width of MOSFET, resistor or other relevant device (m)	44
w_{f}	finger width of MOSFET (m)	81
$\boldsymbol{x}_{i,G}$	vector of differential evolution; i-th parameter vector of G-th generation	62–64
y	function value of the objective function at a given vertex in Nelder-Mead simplex algorithm	65–67

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CHAPTER 1

INTRODUCTION AND THE STATE OF THE ART

Electrostatic discharge (ESD) presents serious threat for reliability and lifetime of any integrated circuit and has to be carefully addressed in every design. It has been so since the first steps on a field of very-large-scale integration in early 70s when more and more complex integrated circuits (ICs) like large dynamic random-access memory modules or microprocessors were introduced. Each advance in lithography and other fabrication steps of IC fabrication process emphasize this fact. As technological nodes – expressed as transistor minimal gate length – shrink, transistors thus integrated become increasingly sensitive to a charge introduced to them during an ESD. Even though duration and total charge of an ESD event is relatively small (approx. tens of nanoseconds and order of units to hundreds of nanocoulombs), deep sub-micron dimensions of transistors (especially their gate oxides which are in modern nodes with high-κ dielectric reaching physical thickness below 20 Å) make them extremely vulnerable. K. Allen in 2002 [3] demonstrated that more than 35 % of IC production is lost due to ESD damage costing companies almost 6 % of annual gross sales.

To increase IC robustness against ESD events, full-chip protection design has to be carefully integrated. Introduction of special models that are able to describe behavior of a protection device during an ESD event may substantially decrease number of iterations necessary for full-chip ESD protection system design to be refined. As price per lot dramatically increases with decreasing technological node (along with the

ESD sensitivity as mentioned earlier) it is even more pressing to limit this number of iterations – design spins – to minimize final product cost. This is especially valid in case when special custom ESD protections are required (foundry supplied protection blocks can't be used for any reason) and thus in-house development is unavoidable.

1.1 State of the Art

Research teams around the world presented different approaches to model ESD protection devices based on different techniques, but all of them are using traditional manual characterization methods [2, 4, 5]. These methods require large number of specific measurements to be performed, thus increasing demand on dedicated specialists and total characterization time. In most of the cases, the measurements require all terminals of a protection device to be connected to external pads which increases systematic error of the measurements as all those pads shall be always protected by at least a basic ESD protection device that adds parasitics and consequently may influence the measurements. The model calibration process is then iterative calibration of all the model fitting parameters until the whole device model emulates the protection behavior with sufficiently low error. This standard calibration approach will be further designated as *standard model calibration method* and will be in more detail described in Chapter 6.

Author is not aware of any commercial ESD-dedicated automated macro-model calibrating software available. Numerous commercial software packages exist for generic model calibration though those would present large investment and for design houses without in-house fabrication factory this software has virtually no additional use cases to rationalize the purchase. Also, there may be issues with voltage and current levels that are orders of magnitude higher than in case of standard transistor models. Article noting use of such a software package is for example [6].

1.2 Research Contribution to the State of the Art

The goal of the research is to maximally automate the ESD protection device macro-model calibration procedure and also more importantly to limit total number of mea-

surements required and to measure structures in form they will be used in production designs without any additional probing contacts or terminals.

The author developed new approach to calibrate ESD macro-models requiring minimal resources. Research on effective optimization algorithm was done by the author yielding differential evolution (DE) as the most fitting one for the required task. Additional improvement was later achieved by the author by introduction of Nelder-Mead simplex algorithm (NMSA) to the final stage of the optimization flow where DE loses its efficiency. Proposed combination of DE and NMSA was published before in [7] but their implementation is different than the author's and is not suitable for presented method.

Contribution to ESD modeling was done by the author by introduction of 4-terminal vertical bipolar inter-company (VBIC) bipolar model instead of 3-terminal variant with additional SPICE Gummel-Poon (SGP) PNP bipolar model in case of low-voltage triggered silicon controlled rectifier (LVTSCR) ESD protection macro-model. This improvement allowed to limit number of fitting parameters to a half of the original 32 without significantly affecting macro-model precision. Additionally, the author made a study to asses sensitivity of important regions of I-V characteristics of ESD NMOST macro-model to parameters of all the macro-model sub-models (e.g., core NMOST, VBIC NPN bipolar transistor, and substrate resistance models). This is presented in Chapter 3.

The final contribution of the author is limiting number of required measurements for a macro-model calibration to a single TLP measurement which is then used as a calibration template. This contribution significantly simplifies the calibration procedure, especially if fully automated TLP setup is available. This alleviates the need for ESD specialist to waste time by manually measuring set of characteristics that are otherwise necessary (e.g., [8, 2]). Additionally, it enables to characterize ESD protections structures as they are implemented in final designs, i.e., without additional terminals used only for the characterization.

Future development of the method may include introduction of macro-model scalability with respect to device dimensions, introduction of impedance characterization to SCR-based protection structures, etc. Temperature and statistical effects were omitted

in this research as those properties are not sought by ESD designers but may be useful during development of new ESD protection structures.

This research is based on author's original work done as part of his master's thesis in years 2010 and 2011 [9].

This thesis is organized as follows: Chapter 2 introduces the reader to basic ESD design practices and to device-level ESD models. Comprehensive list of ESD protection devices and approaches to their modeling are summarized in Chapter 3. Chapter 4 explains properties and necessity of TLP characterization and possibility to employ HBM measurements instead of TLP in case the required equipment is not readily available. Introduction to differential evolution and Nelder-Mead simplex algorithm which are essential part of proposed model calibration method is made in Chapter 5. In Chapter 6, calibration method itself is described in detail along with analysis and comparison with alternative *standard model calibration methods*. Benchmarking methodology of the proposed calibration method is explored in detail in Chapter 7 and so are specific case studies – I/O ESD GGNMOST, LVTSCR, modified lateral silicon controlled rectifier (MLSCR), and basic silicon controlled rectifier (SCR) structures fabricated, measured and eventually calibrated by the method. Chapter 8 presents results of the proposed method benchmarking and discusses them and finally, conclusions are drawn and possible further directions of the research are explored in Chapter 9.

CHAPTER 2

BASICS OF ESD-RESISTANT DESIGN

In the current state of IC production, full-chip level ESD-protection-device implementation is essential part of the whole IC design. Without it, as companies are currently mostly fabricating their ICs in deep sub-micron technologies, there would be substantial losses during production, packaging, final-product assembly, and also during regular operation by end users. Therefore, it is necessary to obey several most critical design rules during the IC development. The basic introduction to the design rules are presented in the first part of this chapter.

Prior to release to the market, validation of a new IC has to be performed comparing its operational performance and characteristics with the design specifications created in the early stage of the development process. It is difficult to exactly quantify "quality" of ESD-protection devices, and to be able to objectively compare such measurements performed with a different equipment and in different environments. To address this need to characterize and benchmark ESD-protection designs, the component and system level models were defined and later transformed into a set of standards which will be presented in the later part of this chapter.

2.1 System-Level Design Methodology

During the standard ESD-robust design in multi-power-domain complementary MOSFET (CMOS) ICs, three essential protection measures shall be always implemented: ESD protection of all the I/O pads (interface between IC core and outside of the chip), voltage-clamping devices inserted between each power and respective ground, and inter-domain power-coupling devices (between all the power domains) [10]. Example of such a system is shown in Figure 2.1.

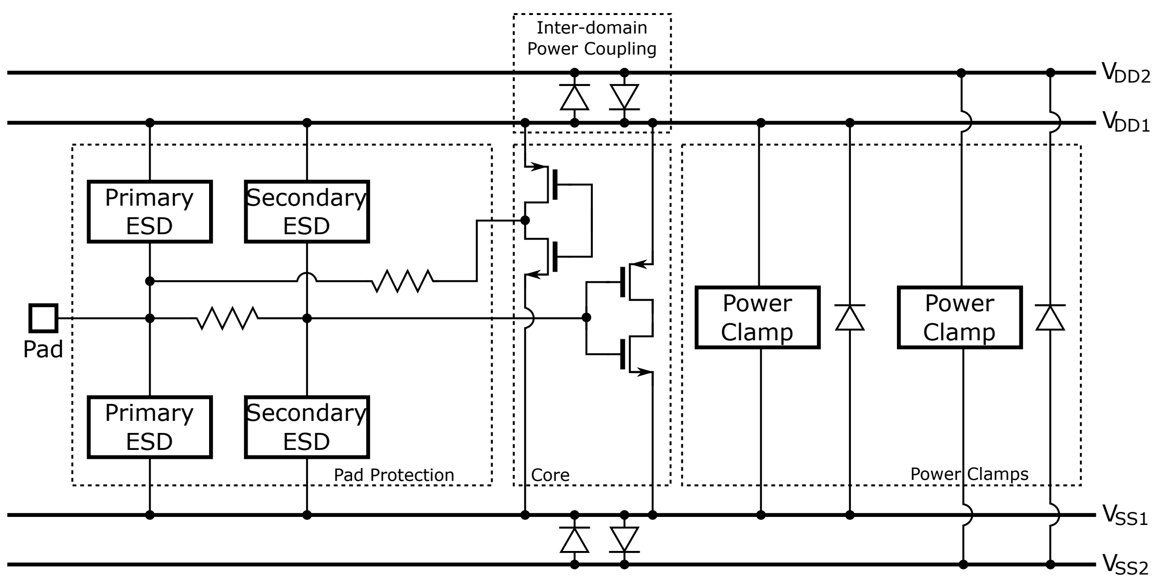

Figure 2.1: *Schematic Representation of the Full-Chip Level ESD Protection System*

2.1.1 I/O Protection Devices

Generally, the protective ESD circuits of a standard digital bidirectional I/O pad consist of two components [11]: *primary* and *secondary* protection circuits. The primary ESD circuit protects an output buffer by limiting the over-voltage caused by the ESD event and diverts major part of the ESD current away from peripheral circuits. It is now common practice to merge output buffers and the primary protection circuit into single structure by means of a layout style. The secondary protection circuit, which is usually a down-scaled version of the primary ESD device (therefore, it triggers

much faster), guards input buffers or a Schmitt-trigger-based signal-shaping circuits by clamping induced over-voltage. Therefore, it protects the gates of the input block against a dielectric breakdown. The secondary part shall be always divided from the pad-bonding area by a current-limiting resistor. The secondary part may be omitted only if the primary protection structure triggers fast enough and if the current-limiting resistor is implemented. Even if those two requirements are met, it is a good practice and sometimes necessary to verify the ESD robustness by a measurement of a testing structure. Example of digital I/O self-protected by the output driver using salicide blocking on drain sides of NMOST and PMOST and using current-limiting resistor in the signal path and down-sized gate-grounded MOSFETs as a secondary protection is shown in Figure 2.2.

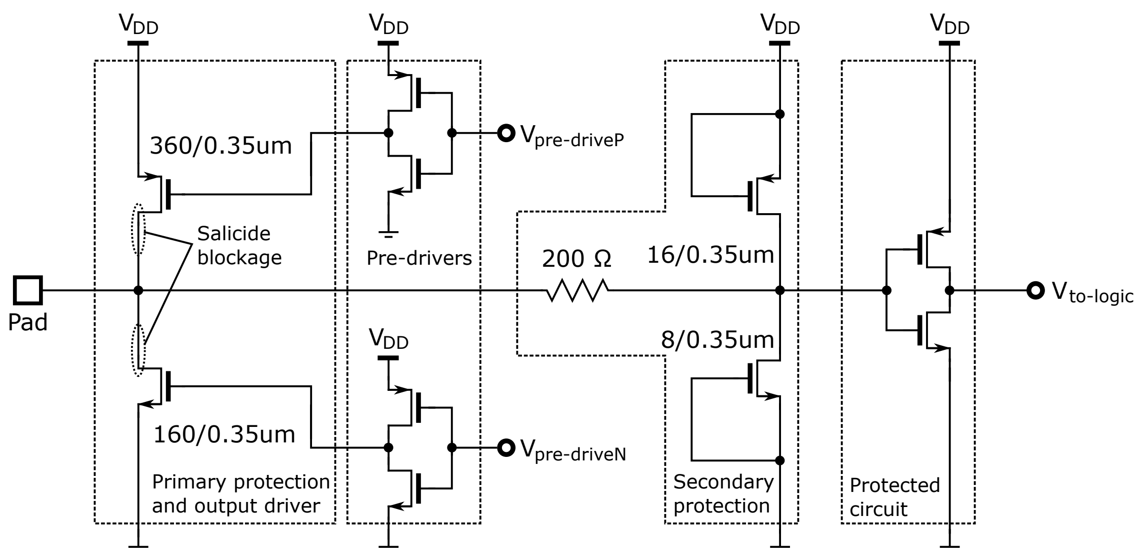

Figure 2.2: *Example of a Digital I/O Pad Protection Using Primary and Secondary ESD Protection Elements*

2.1.2 Power-Clamp Devices

Power voltage-clamping devices or power clamps are core protection devices implemented to shunt discharges on power lines. Dynamic-triggered devices are usually used as it is possible to set a time-constant of the power-clamp internal RC element to trigger on a specific rising-edge time of an ESD pulse. Power clamps are always distributed

throughout the power and ground rails in a pad-ring to minimize ESD path resistance – this is especially important for countermeasures against CDM-like events. Illustrative example of very simple power clamp protection between power and ground lines is shown in Figure 2.3. Time constant *RC* sets edge speed sensitivity of the clamp.

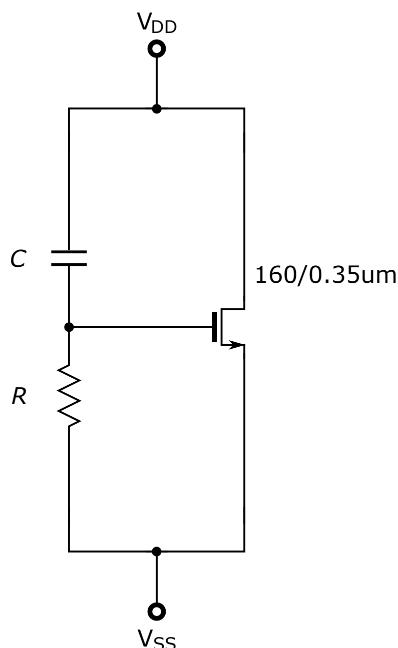

Figure 2.3: *Example of a Simple NMOST-Based Power Clamp Between V_{DD} and V_{SS}*

2.1.3 Inter-Domain Power-Coupling Devices

Finally, all the power lines of the multi-power-domain system shall be interconnected by the power-coupling elements that clamps potential over-voltage on one of the lines and transfers the charge through the other to the respective ground. Similarly, multiple grounds of the IC (e.g., digital, analog) shall incorporate these structures too. Anti-parallel-connected diodes are very often used as an inter-domain power-coupling devices (see Figure 2.4). Partitioning of the IC power distribution is done usually due to noise isolation between power domains otherwise on the same potential, thus care must be taken to correctly optimize between robustness and noise coupling (size) of the diode(s).

All the three described countermeasures shall be designed in such a way that there

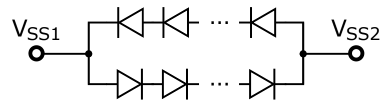

Figure 2.4: *Example of an Inter-Domain Power-Coupling Diode Structure Between V_{SS1} and V_{SS2}*

always exist low impedance paths between all the possible sources of an ESD event (e.g., pad) and the ground – either via single protection structure directly to the ground or via pad ESD protection and power clamp to the ground. The purpose is to divert as much of the ESD energy as possible from the core blocks via carefully designed low-impedance rather than completely random paths. Example situation showing correctly designed low-impedance paths between two pads is shown on Figure 2.5. Low-impedance path exists between each pad and its respective power and ground, both I/O power domains are coupled to the core domain and the core domain power lines are bypassed by a power clamp.

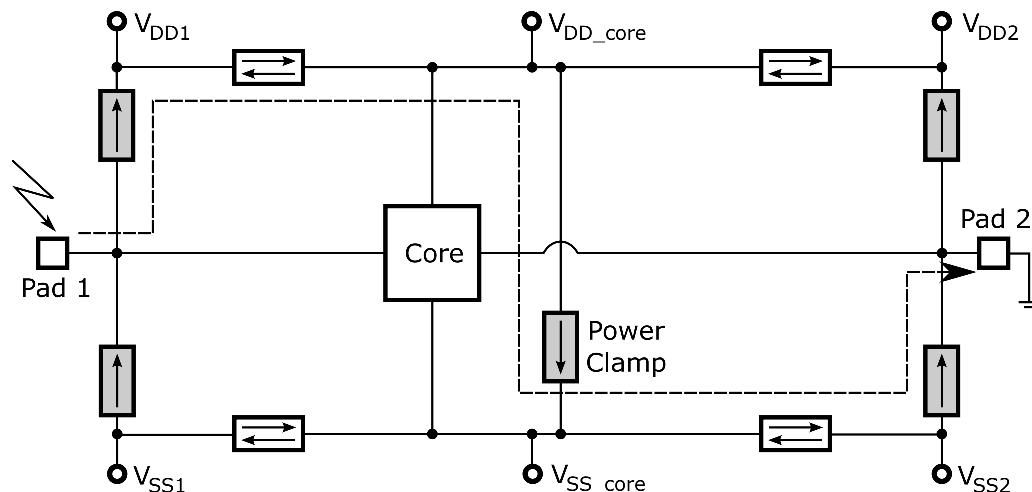

Figure 2.5: *Example of an ESD Current Path in a Protected System*

Important aspect of any ESD protection circuit is a behavior during on and off states. The protective circuits should affect neither incoming nor outgoing signals while operating in the off-state; during on-state, the device shall effectively protect core circuits. That means as small leakage in the off-state as possible, short trigger time (in

order of nanoseconds [10]), and very small resistance during the on-state. Protection devices shall hold in on-state until the end of an ESD event and shall not be fatally damaged by it.

Two general ESD-protection mechanisms are known: a *simple turn-on current versus voltage (I-V)* and a *snapback I-V* [10].

2.1.4 Simple Turn-on I-V Devices

The simple turn-on I-V device turns on after an incoming voltage reaches a turn-on voltage V_{t1} and then conducts with low resistance as long as the voltage is higher then the V_{t1}. Robustness of such a protection device is dependent mainly upon maximum power dissipation of the device. Diode experiencing forward bias voltage higher then "cut-in" voltage (approx. 0.75 V for standard silicon or 0.3 V for Schottky diodes) demonstrates such a behavior. Figure 2.6 shows the simple turn-on I-V.

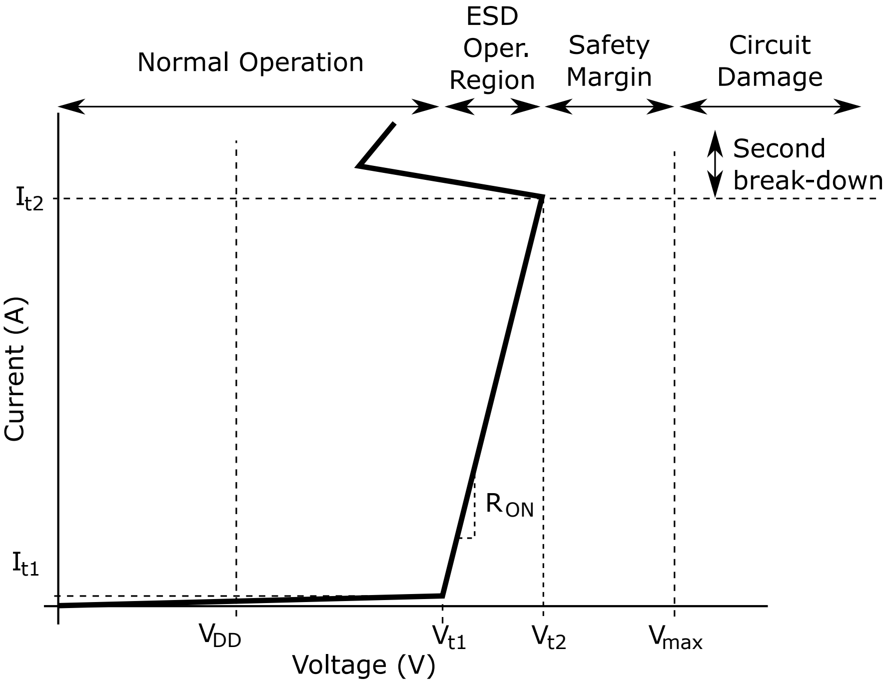

Figure 2.6: *Simple Turn-on I-V Characteristic*

2.1.5 Snapback I-V Devices

Four parameters are most important for the snapback I-V based devices: V_{bd} as a first-breakdown voltage, V_{t1} as a trigger voltage, V_h as a holding (snapback) voltage, and I_{t2} as a second-breakdown current. Current versus voltage characteristic of an ideal snapback-mechanism-ESD-protection device is shown in Figure 2.7. Mechanism of snapback in MOSFET and SCR-based protection structures is presented in Chapter 3.

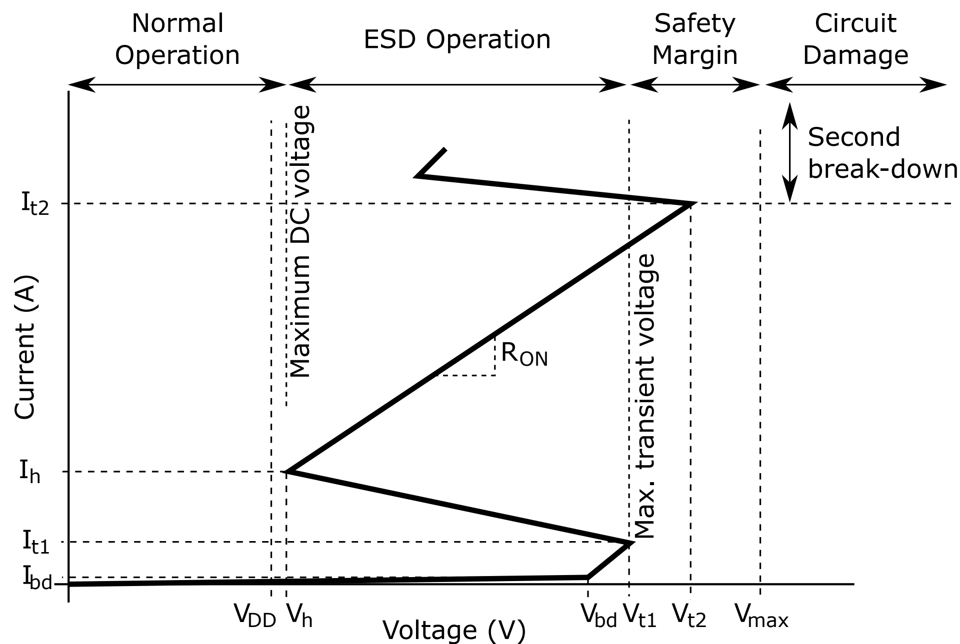

Figure 2.7: *Snapback I-V Characteristic*

What is behind of such a high popularity of the snapback-based ESD protection devices? The snapback phenomenon is very effective way to exhibit surprisingly low power losses even with relatively high trigger voltage. It is thanks to a negative-differential-resistance part of the snapback I-V that the holding voltage may be only a fraction of the trigger voltage in the high-current state. All the focus of this thesis is dedicated to the snapback I-V ESD protections as these are the most widely used devices for their attractive properties.

The most of the static properties of the snapback protection device is apparent from its I-V characteristics in the so called *ESD design window*. It basically defines all the operational regions of a device including its destruction by a high-current-induced

thermal damage. It is extremely important to correctly size the ESD design window of a protection device for a specific block that it shall protect; otherwise, no matter how robust and quick the protection device would be, the protected circuit will be damaged if e.g. the protection-device trigger voltage would be higher than the protected circuit breakdown voltage (see Figure 2.8).

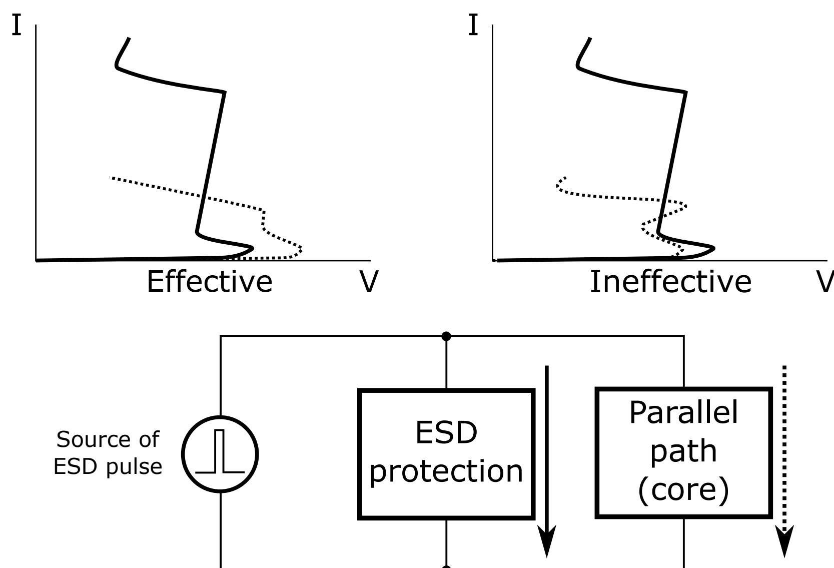

Figure 2.8: *Example of the Correct and Wrong ESD-Protection Designs*

Although the snapback-based devices have many advantages, the ESD design window of an effective and robust ESD protection structures have to follow specific requirements. Parameter V_{t1} shall always be higher than the supply voltage V_{DD} to avoid self-triggering during the normal operation and shall be simultaneously lower than a specific maximum voltage that is tolerable by internal blocks (e.g., gate oxides). To prevent a lock-up in the snapback state, the snapback (or holding) voltage V_{h} shall always be higher than V_{DD}. Turn-on resistance of the device shall be as low as possible because even relatively low current flowing through a too high resistance may cause too high power dissipation in the conductive channel which induces temperature high enough to melt the silicon channel. The current that causes such extreme rise of a temperature is called second-breakdown current I_{t2} and shall be in any case high enough that the protection device withstands the strongest ESD event possible (ideally more

than 2 kV HBM). There are always compromises to be made. In this case between the ESD-protection robustness and size, and the IC-operational performance.

During a technology shrinking, modifications to ESD design along with the new design validation are usually required, the reason being introduction of new fabrication steps (e.g., retrograde well, halo implants, etc.) and changes to doping profiles that usually have significant impact on properties of ESD protection circuits.

In order to be able to characterize and benchmark ESD protection devices, so called *component-level ESD models* were developed. Basic summary of their properties follows.

2.2 Component-Level Models

In any stage of design, there is always need to exactly quantify performance of a specific block. The situation around ESD protection circuits is no different. Unfortunately, there are many difficulties in determining robustness of an ESD protection device as measurements are extremely sensitive to environmental effects, shape of a testing pulse and interpretation of results. This ambiguity lead to creation of standardized component and system-level models and test methods which can unambiguously benchmark different ESD protections and even protection families with respect to their robustness. These models are widely used for reliability testing and as an aid for development of ESD protection circuits. Even though the only information that are the component and system-level models able to give to a designer is a maximum voltage level of the stress pulse that the protection can withstand (thus effectively protecting core circuits), they are often the only information about ESD performance of an IC in a device technical datasheet. Component-level models differ in terms of a pulse-waveform properties: peak current, rise time, decay rate of the pulse, etc. These properties are exactly defined in the appropriate standard. In the present, three basic component-level models are most widely used [10, 12]: *human body model* (*HBM*), *machine model* (*MM*), and *charged-device model* (*CDM*). Aside from those models with their limited information value, the more recent approach to evaluate the ESD protection properties was developed by T. Maloney and N. Khurana in 1985 – the *transmission-line pulse* (*TLP*).

Transmission-line pulse is able to describe the whole I-V characteristic of an ESD protection device and to suggest designer valuable information about weak points of a specific ESD design. Details about TLP are available in Chapter 4 along with details how to utilize a standard HBM tester fitted by additional measuring tools to produce TLP-like characterization results. This is especially useful due to the fact that price of a TLP measuring system is much higher than ordinary manual-operated HBM/MM tester, amended by high-bandwidth oscilloscope that is usually essential part of well-equiped laboratory.

2.2.1 Human Body Model

The human body model (HBM) describes discharge between any I/O or analog/power pad and a limb of a human body, for example during manipulation. This model consists of the high voltage generator (hundreds of volts to units of kilovolts) and 100 pF shunt capacitor and 1.5 kΩ series resistance. The charged capacitor and resistor model electric charge stored in a human body and resistance of a human limb respectively. Illustrative scheme is shown in Figure 2.9. Values of the passive components and properties of the high-voltage generator as well as of the voltage pulse waveform are defined in the HBM standard [13]. Capacitor charged to the specific voltage (definition of voltage levels are also part of the standard) is discharged through the series resistor into any I/O or analog/power pin with one arbitrary pin grounded while other pins remain unconnected. This discharge is repeated three times and then the pin is inspected for change in leakage current. All the pins are tested in such a way one by one. Based on maximum voltage level that the pin ESD protection is able to withstand without significant change in the leakage current the pin becomes rated for this specific HBM voltage, e.g., if a pin passes 4 kV pulse testing but fails for 8 kV, it is 4 kV HBM tolerant.

The rise time of the HBM waveform is in order of units or tens of nanoseconds and discharge rate is in order of GV/s. Peak current of the HBM event can exceed 2 A for 4 kV stress. More information about the standard, waveform parameters, and requirements for the HBM tester can be found in [13]. Example block diagram for HBM tester is shown in Figure 2.10.

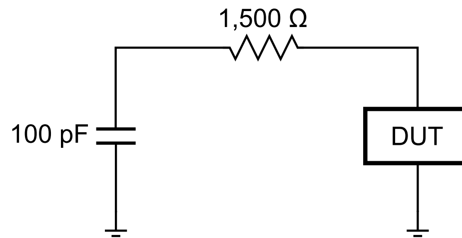

Figure 2.9: *Human Body Model Representation*

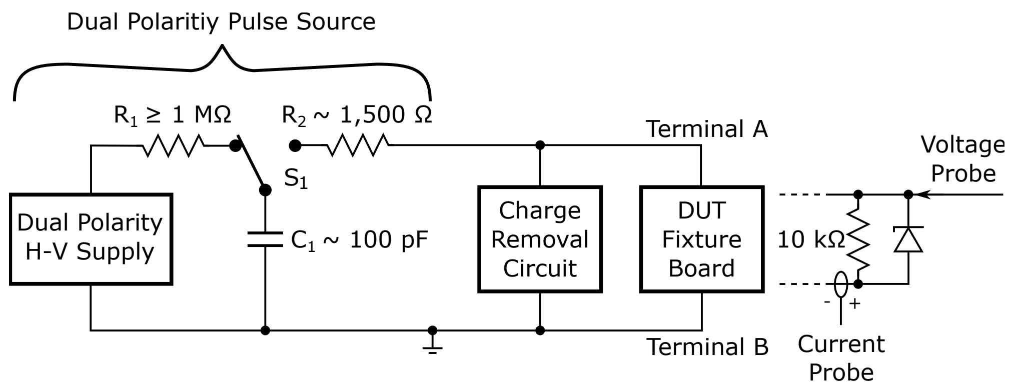

Figure 2.10: *HBM Tester Schematic*

2.2.2 Machine Model

The machine model (MM), as its name suggests, emulates an ESD event during manipulation by automatons. The major difference against the HBM is a size of the series resistor. Because of the nature of this resistance (metal machines) its value is much lower than in the HBM model (usually units of Ohms); therefore, parasitic components of a discharge path has the major impact to a pulse properties. Parasitic inductance of about 0.7 μH and resistance of 10 Ω [14], both due to measuring leads and a device under test (DUT), make the pulse oscillatory. The rise time of a MM-induced ESD pulse is approximately 15–30 ns and the peak current can reach 5 A for 400 V pulse level. MM characterization measurement follows the same procedure as the HBM one. Figure 2.11 presents circuit representation of MM measuring bench. As HBM, the MM uses classification based on the ESD voltage level the device can withstand – from approximately 25 V to 400 V. For additional information about the MM see [14].

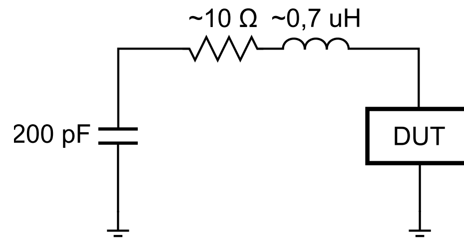

Figure 2.11: *Machine Model Representation*

2.2.3 Charged Device Model

The charged-device model (CDM) is based on different assumption. The pulse is not generated outside of the DUT but within the DUT itself. This model emulates discharge of a charged package through a grounded pad as it can happen during for example post-packaging manipulation. As opposite to the previous component-level models, the capacity of the DUT package has important impact to the results in the CDM. Two different methods are used to create CDM ESD stress: the direct charging and field-induced methods. The first method is based on charging the device through the pad with the best contact to the substrate or through all pins at once (see Figure 2.13a for a tester conceptual schematic). Then each pin is discharged one by one. During measuring by the second method, the DUT itself is charged by an induction of a field plate on which the DUT resides and then discharged through the internal circuits by one of its I/O or analog/power pads to the ground (see Figure 2.13b for a tester conceptual schematic). The CDM event is the fastest – rise time less than 1 ns and duration in units of nanoseconds [12] – and most dangerous of all the three component-level models; and therefore, it is very difficult for protective circuits to react fast enough to clamp majority of the ESD energy away from vulnerable internal circuits. CDM-induced electrostatic discharge current can rise close to 30 A for 2 kV pulse. Devices are also ranked by a CDM voltage level they can withstand without major damage. Representation of scheme of the CDM with the parasitics is shown in Figure 2.12. The charged-device model is subjected to the standards, see [15] for details.

All the component-level models are used to test the ESD circuits using standardized methods which make all the results reproducible. They are often used during a design

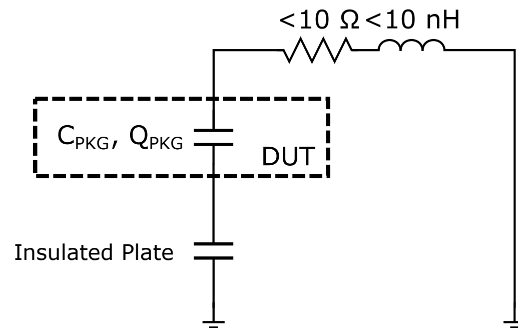

Figure 2.12: *Charged-device Model Representation (Discharge Phase)*

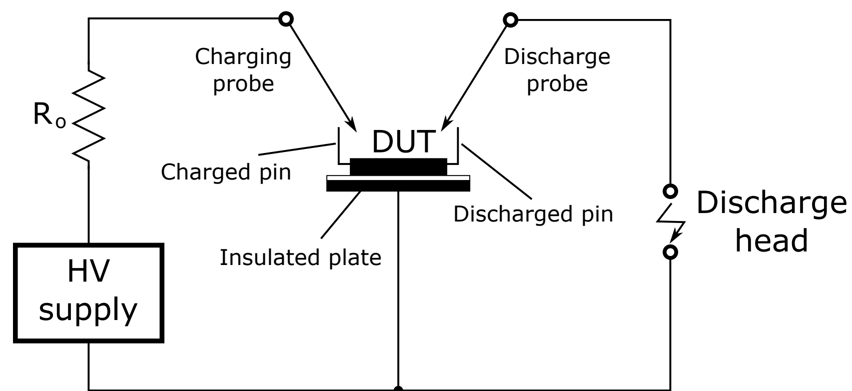

Figure 2.13a: *Conceptual Schematic of CDM Tester (Direct Charging Method)*

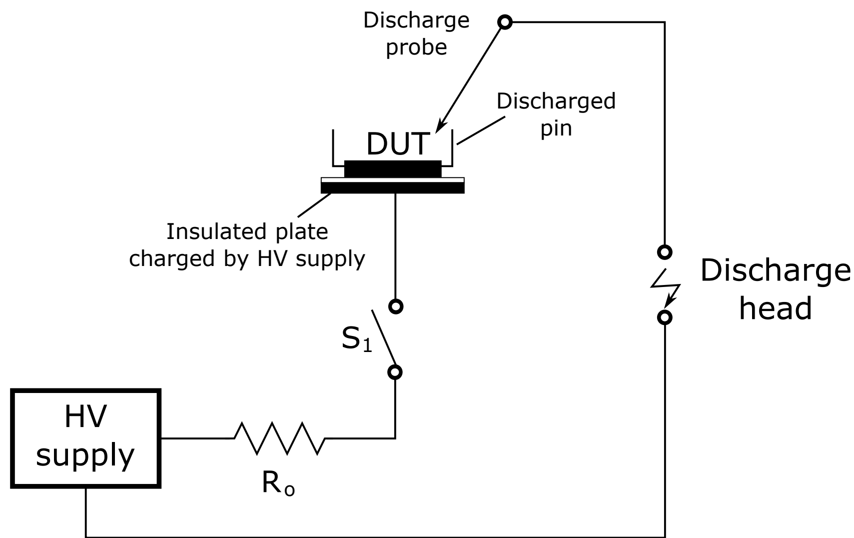

Figure 2.13b: *Conceptual Schematic of CDM Tester (Field-Induced Method)*

phase as it makes it possible to compare quality of many different protection system designs and implementations and based on component-level model results select the most robust of them. The ESD testers that meets all the specifications in the respective standard are available ranging from a manually operated testers to a fully automated systems for mass-volume characterization or validation. Exact standardization [13, 14, 15] of all the important parameters of the testers ensures consistent and reproducible measurement and ability to compare designs across different IP vendors.

For completeness, comparison of typical current waveforms of the three component-level model pulses is presented in Figure 2.14.

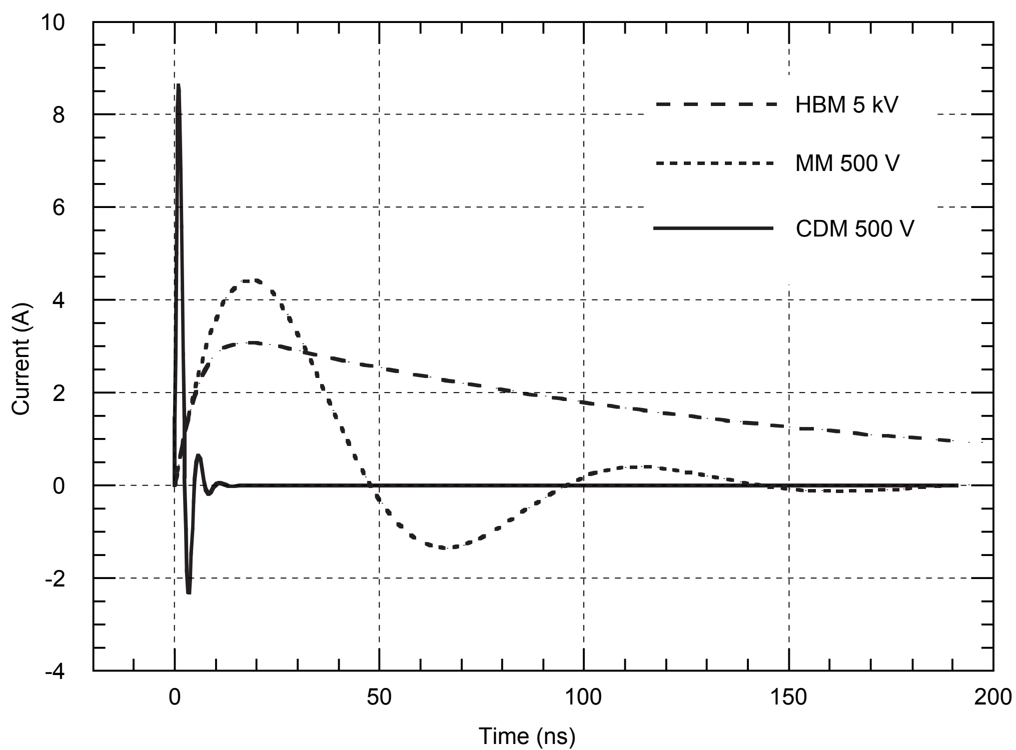

Figure 2.14: *Comparison of Current Waveforms of HBM, MM, and CDM Pulses*

CHAPTER 3

OVERVIEW OF ESD PROTECTION DEVICES

Following paragraphs summarize basic principles, properties and approaches to model ESD protection devices most often used in modern deep-submicron bulk CMOS processes: gate-grounded NMOST, silicon controlled rectifier, modified lateral silicon controlled rectifier, and low-voltage triggered silicon controlled rectifier.

3.1 Gate-Grounded NMOST

Gate-grounded NMOST (GGNMOST) is one of the most widely used digital I/O protection devices in standard CMOS processes. It's mainly because of its proven robustness and easy implementation without any additional masks required.

Structure of NMOST inherently contains a parasitic NPN bipolar transistor consisting of drain, source, and bulk connection (forming collector, emitter, and base respectively). Even though exhibiting very poor parameters compared to non-parasitic bipolar transistors available in modern CMOS processes it plays essential role in GGNMOST operation. See Figure 3.1 with highlighted bipolar transistor.

During normal operation, the GGNMOST having its gate and bulk contacts tied to a potential of a source terminal conducts virtually zero current through its drain terminal (except thermal leakage). Because the bulk terminal is effectively shorted to the source terminal, increasing drain—source voltage also increases electric field

on reverse-polarized n+ drain—p-well junction giving gradual rise to velocity of free minority carriers that are being pulled into a depletion region of the junction. When critical electric field (and thus also the velocity of the carriers) is reached, avalanche impact ionization boosts the leakage current by following equation

$$J_h(w) = M J_h(0) \tag{3.1}$$

where $J_h(x)$ denotes current density of minority carriers in a specific depth of the depletion region of the drain—p-well junction, w is thickness of the depletion region, and M is an impact ionization multiplication factor. This state corresponds to reaching drain voltage of V_{bd} (first break-down voltage) in Figure 3.4 showing simplified I-V characteristics of a typical GGNMOST structure. Important fact to note is that even though the bulk terminal is shorted to the source one, the nature of a low-doped p-well in which the NMOST is manufactured means that there exists inherent substrate resistance between the drain—p-well junction and the bulk contact (it is denoted as R_{pw} in Figure 3.1). Ohm's law then dictates that where a current flows through a resistance, there is a voltage drop on that resistance. Remembering the parasitic NPN transistor formed by drain—p-well and p-well—source junctions the mechanism of GGNMOST snapback operation can be easily explained: when the current flowing through the p-well resistance reaches level needed to forward-bias the p-well—source junction (i.e., local potential below gate and near the source contact reaches turn-on voltage of the p-well—source junction), the parasitic NPN transistor starts to operate in forward mode abruptly decreasing GGNMOST drain—source resistance and voltage drop on the protection device to holding voltage V_{h} while increasing the drain current – this behavior corresponds to a negative resistance (rise to current causes voltage to drop). The voltage at which the protection starts to exhibit the negative resistance is called trigger voltage (point $\{V_{t1}, I_{t1}\}$ in Figure 3.4). This mechanism is called *snapback*. Point on the I-V characteristics in Figure 3.4 $\{V_{\mathrm{h}}, I_{\mathrm{h}}\}$ is thus often instead holding called snapback voltage.

Design of GGNMOST-based I/O protection is always a compromise between tolerance to ESD pulse energy (i.e., HBM voltage level) and a size of the protection. As it is usually necessary to use very wide transistor (hundreds of micrometers for

example), it is essential to optimize also its layout. Solution is to partition this wide transistor into multiple fingers with smaller width per finger but the same total width of the whole device. Unfortunately this creates its own issues: non-uniform bulk contact and with that related non-uniform triggering and conduction of individual fingers during ESD event. As the finger in the center of multi-finger structure sees largest resistance to the bulk contact, the snapback occurs earlier. As snapback effectively abruptly decreases voltage drop across the protection device, other fingers does not activate leaving all the energy to be shunted by the center finger. If the trigger voltage V_{t1} of the protection is higher than a second break-down voltage V_{t2} and if the ESD energy is high enough to reach the second break-down voltage, then the protection is irreversibly damaged before any other finger can trigger (see dashed line in Figure 3.4). To overcome this issue, there are numerous possible solutions. Elegant and the most often used is addition of a balast resistance to drains of all the fingers (either lumped poly-resistors or integrated diffusion resistances using salicide blocking on the drain side of the MOSFET – the latter is denoted in Figure 3.1 as $R_{\mathrm{d,noSAL}}$). The additional ballast resistance increases turn-on resistance R_{on} and effectively shifts second break-down voltage V_{t2} higher – above the trigger voltage V_{t1} (see solid line in Figure 3.2).

In case of a negative ESD impulse to drain terminal, the drain—p-well junction of the NMOST is forward-biased and shunts the current away.

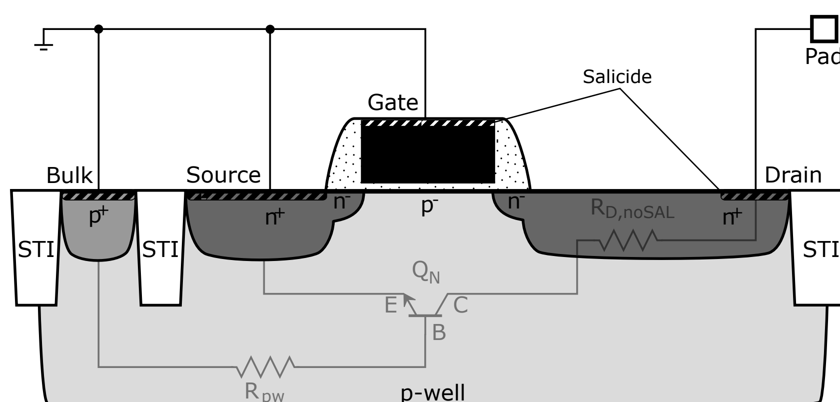

Figure 3.1: *GGNMOST Structure*

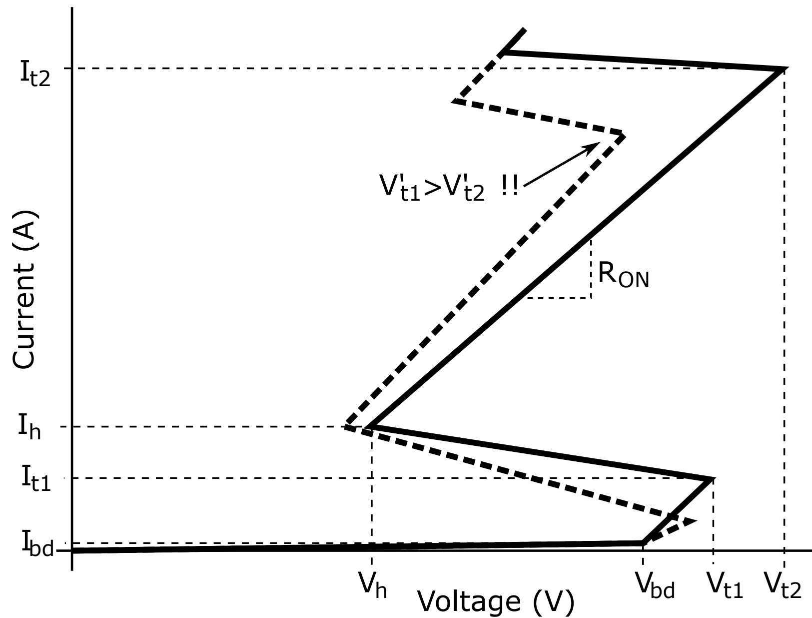

Figure 3.2: *NMOST Snapback I-V Characteristics (Dashed Line – Salicide Drain, Solid – Extended Drain with Salicide Blockage)*

3.1.1 Gate-Coupled NMOST

One of the other possible solutions of the non-uniform triggering of the multi-finger protection – decreasing its V_{t1} voltage below the second-breakdown voltage V_{t2} so that all the fingers can be triggered before the damage of the fingers in the center of the structure can occur – is to control the gate—source bias voltage of the device. The issue with this approach is the necessity to limit leakage in off state as much as possible – static gate biasing is thus not a viable option. Dynamic *RC* coupling of the gate to the protected rail or I/O depicted in Figure 3.3 exhibits decrease of the trigger voltage due to forward transient gate biasing and also off state leakage is comparable to standard GGNMOST as the gate is weakly pulled to ground. The high-pass *RC* constant of the GCNMOST has to be set such that signal changes on the protected I/O during normal operation do not trigger the protection. A ratio of *C* and *R* which sets the transient gate biasing dictates change to the trigger voltage V_{t1} [12]. Resulting improvement to the GGNMOST I-V characteristic is depicted in Figure3.4.

Position of some of the important points of the GGNMOST or GCNMOST I-V

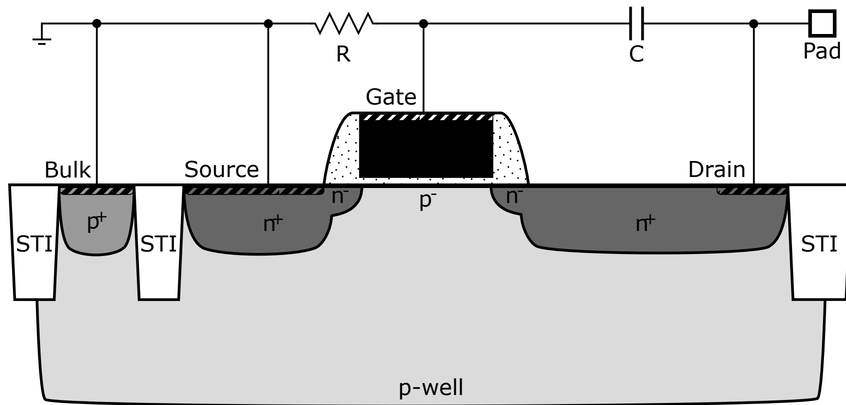

Figure 3.3: *GCNMOST Structure*

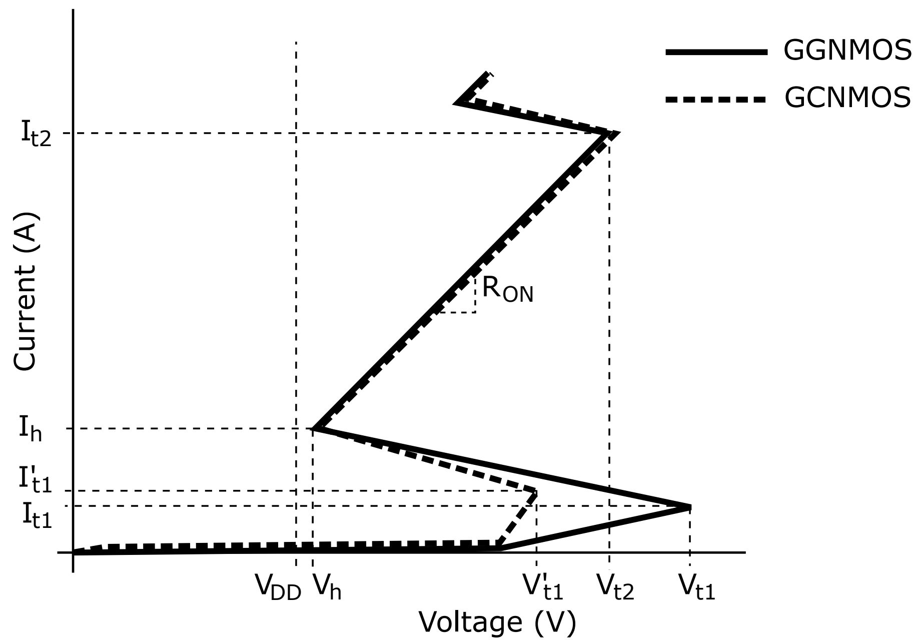

Figure 3.4: *GCNMOST I-V Characteristics*

characteristics can be controlled by some of the device design parameters and also a layout style. Some of those parameters are discussed below.

Gate Width

Neglecting non-uniformity of finger conduction for a moment, the gate width (w_g) implies increase in overall robustness of the device. More current is needed to turn on or breakdown the device so the currents I_{t1} and I_{t2} increase. As the voltage V_{t1} should not change with change of gate width the on-state resistance (R_{on}) should decrease. If the non-uniformity is taken into account in multi-finger systems, the R_{on} should decrease with increased number of individual fingers (all fingers have the same width w_f). This was not observed during the measurement of the test on-chip protection devices. The turn-on resistance may decrease less than anticipated because of the non-uniform finger conduction. Basically, as not all the device fingers conducts the ESD current, the on-state resistance does not improve proportionally to number of the fingers [16]. The solution of this problem can be the GCNMOST structure as described above. Non-uniform conduction within a single finger is also a factor that needs to be considered during a design. From specific finger width, further increase does not yield further improvement to the on-state resistance as only a part of the finger conducts. Based on report in [11], this phenomenon is mainly caused by non-uniform distribution of dopants in the finger body. The solution would be to extend a total width of a protection device by increasing number of fingers instead of a finger width.

Gate Length

As mentioned in [10] and [16], the gate length defines to some extent effective width of a parasitic bipolar transistor base w_{B} and a width of a depletion region of a reverse-biased p—n junction w_{BD} consisting of a drain diffusion and a p-well:

$$w_{\mathrm{B}} + w_{\mathrm{BD}} \propto L. \tag{3.2}$$

This increase of effective BJT base width means that the bipolar current gain factor β decreases dramatically. As the first break-down voltage of a p—n junction depends

only on its doping profile, V_{bd} does not change. On the other hand as snapback voltage V_{h} is inversely proportional to β and β decreases with second power of the gate length [10], following relation may be drawn

$$V_{\mathrm{h}} \propto L^{2/n}, \tag{3.3}$$

where n is a technology constant. Trigger voltage V_{t1} is also inverse proportional to β as transport efficiency of the bipolar transistor decreases and also the electric field on drain—p-well junction decreases with increasing channel length, so the onset of the impact ionization is also negatively impacted. The on-state resistance R_{on} also increases because of increased series resistance of the longer channel. The second break-down current I_{t2} is higher due to larger volume where the heat generated in the depletion region is dissipated [10].

Salicide Blocking on Drain Diffusion

Silicide is a silicon compound with another more electro-positive element such as tungsten or titanium. The advanced process called salicide (self-aligned silicide) process utilizes fact that used transition metals don't react with silicon oxides or nitrides and don't need additional lithographic masks. The silicidation of diffusion and poly-silicon gate contacts are applied to decrease series resistance of the contacts thus enhancing performance of analog and digital circuits, but in ESD circuits the ballast resistance is important part of a protection device. Reduction of ballast resistance by introduction of salicide process step on ESD device may lead to non-uniform finger conduction causing degradation of the second break-down current I_{t2} but also implies reduction of R_{on}, V_{h} and trigger voltage V_{t1} [10]. It is thus desirable to introduce selective silicide blocking mask which is nowadays in most designs already available due to need for high-resistive, highly linear poly-silicon resistors.

3.1.2 ESD NMOST Macro-Model

Macro-model used for evaluation is based on model presented in [17] and comprises of appropriate technological n-channel BSIM NMOST core, n-type three-pin VBIC BJT model simulating parasitic NPN structure formed of drain and source n+ diffusions and p-well, and p-well and un-salicided drain diffusion resistances. Complete macro-model is shown in Figure 3.5.

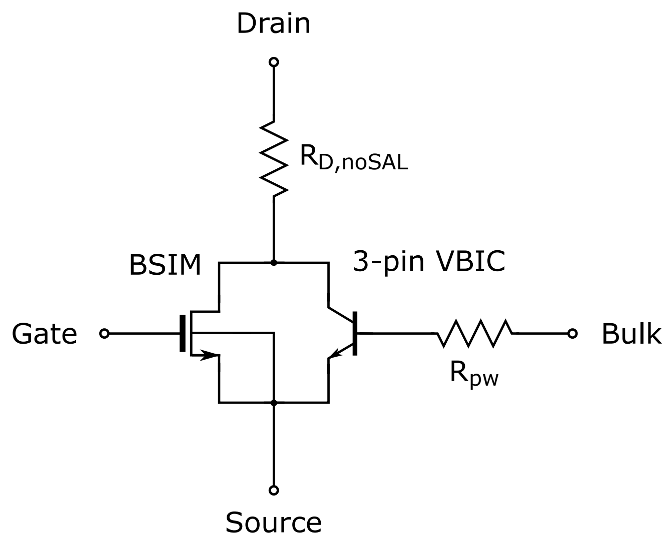

Figure 3.5: *Scheme of NMOST Macro-Model*

The core n-channel BSIM model is in fact already part of the process design kit (PDK) – available PDK contains BSIM MOSFETs in version 3.24 – and majority of its parameters is already correctly characterized by model engineers and process development team. Just three parameters of the substrate-current equations of the BSIM model have to be re-characterized to properly model substrate current. The second most important part of the macro-model is the n-type BJT modeled by VBIC model. VBIC is able to model collector-base breakdown by impact ionization and is thus used as second part of substrate current model. The NMOST part of the substrate current flowing through the bulk terminal can be described as

$$I_{\text{sub}}^{\text{MOS}} = \alpha \cdot V_{\text{DSeff}} \cdot \exp\left(\left(\frac{\beta}{V_{\text{DSeff}}}\right)^{I_{\text{dsa}}}\right) \tag{3.4}$$

$$\alpha = \alpha_0 + \frac{\alpha_1}{L_{\text{eff}}} \tag{3.5}$$

where V_{DSeff} is the effective drain—source voltage, I_{dsa} is the drain current without considering the impact ionization effect, L_{eff} is the effective channel length of the NMOST, and α_0, α_1, and β are the three n-channel BSIM model substrate current fitting parameters. The second part modeled by the collector-base impact-ionization breakdown model of the VBIC BJT model can be described as

$$I_{\text{gc}}^{\text{BJT}} = I_{\text{tot}}\, A_{VC1}\, V_{bci} \exp\left(-A_{VC2}\, V_{bci}^{\text{mod}}\right)^{M_C - 1} \tag{3.6}$$

where I_{tot} is the total leakage current through the base-collector junction, V_{bci}^{mod} is a built-in potential of the base-collector junction diminished by a voltage drop across the junction, M_C is a junction gradient coefficient, and A_{VC1} and A_{VC2} are fitting parameters. Total current is then calculated as the sum of the $I_{\text{sub}}^{\text{MOS}}$ and $I_{\text{gc}}^{\text{BJT}}$ currents.

Different approach was presented in [8] where dedicated current source is used to model the junction avalanche current. Instead of VBIC bipolar transistor model, standard SGP models the parasitic bipolar behavior. The avalanche current model is defined as

$$I_{\text{gen}} = (M-1) \cdot (I_{\text{D}} + I_{\text{C}}), \tag{3.7}$$

$$M = \frac{1}{1 - K_1 \cdot \exp\left(\frac{K_2}{V_{\text{DS}} - V_{\text{dsat}}}\right)}, \tag{3.8}$$

where M is avalanche ionization factor, I_{D} is a drain current of the NMOST model, I_{C} is a collector current of the SGP bipolar model, V_{DS} is drain—source voltage, V_{dsat} is drain—source saturation voltage, and K_1, K_2 are fitting parameters. On the other hand, this independent current source can very easily cause convergence difficulties during

complete system simulation and is problematic for implementation due to the fact that it requires value of V_{dsat} which is not accessible BSIM model parameter and have to be thus calculated twice – once in the NMOST model itself and second in the avalanche current model as

$$V_{dsat} = \frac{V_{GS} - V_{th}}{a_1 + b_1 (V_{GS} - V_{th})}, \tag{3.9}$$

where V_{GS} is the gate—source voltage, V_{th} is NMOST threshold voltage, and a_1 and b_1 are fitting parameters. Convergence difficulties were observed in early stages of the research when a Verilo-A model utilizing this substrate current source model was used and as a result this type of snapback model was abandoned.

Remaining parts of the macro-model are the substrate resistance that is modeled as a linear lumped voltage and temperature-independent resistor requiring single fitting parameter R_{pw}, and technological diffusion resistor modeling unsilicided drain extension of the ESD NMOST which is defined by the dimensions of the device. This technological diffusion resistor is also part of the standard PDK and does not have to be characterized – just modified to take into account the fact that the diffusion resistor in the ESD model has contact on only one side. PDKs use following model of un-salicided diffusion resistor (ommiting temperature and voltage dependences and removing one of the two contact resistances)

$$R_{d,noSAL} = R_{sh,ndiff} \cdot \frac{L_{eff}}{w_{eff,tot}} + R_{sh,contact} \cdot \frac{L_{contact}}{w_{eff,tot}}, \tag{3.10}$$

where $R_{sh,ndiff}$ and $R_{sh,contact}$ are sheet resistances of the drain unsilicided n-diffusion region and diffusion contact respectively, $w_{eff,tot}$ and L_{eff} are effective total width and length of the resistor respectively and $L_{contact}$ is length of the diffusion contact.

Total number of fitting parameters of the macro-model is 16. Two of them in the internal-NMOST BSIM model defining substrate-current model, one in the substrate resistance model, and remaining 13 parameters in the VBIC bipolar transistor model. NMOST fitting parameter ALPHA1 (or α_1 in equation 3.4) was omitted as it only adds

dependence to effective length of the transistor which is not desirable.

Table 3.1 summarizes effects of NPN bipolar transistor model, core NMOST model, and substrate resistance parameters to I-V characteristics of the final ESD macro-model. Cadence Spectre Model Reference Manual [18] was used as a reference.

Parameter	V_{t1}	I_{t1}	V_h	I_h	R_{on}
NPN BJT Parameters					
AVC1	⇓	→	⇓	⇓	→
AVC2	⇓	→	⇓	⇓	→
IBCI	↓	↑	→	→	→
IBCN	↓	↑	→	→	→
IBEN	→	→	↑	↓	→
IS	↓	↓	↓	→	↓
NEN	→	→	⇓	⇑	→
NF	⇑	⇑	⇑	⇑	→
RBI	↓	↓	↓	↓	→
RBX	↓	↓	↓	↓	→
RCI	→	→	→	→	↑
RCX	→	→	→	→	↑
RE	→	→	→	→	↑
Core NMOST Parameters					
ALPHA0	↓	↓	↓	↓	→
BETA0	⇓	⇓	⇓	⇓	→
Substrate Resistance Parameters					
RPW	↓	↓	→	→	→

[1] ↑ – directly proportional
[2] ⇑ – exponentially proportional
[3] → – none or insignificant dependence

Table 3.1: *Summary of Effects of NMOST Macro-model Parameters to its I-V Characteristics*

3.2 Silicon Controlled Rectifier

The SCR ESD protection devices are based on usually strictly prevented phenomenon – the latch-up. The basic rule during the IC design is to avoid the latch-up at all cost because within the core logic or analog blocks it may cause severe silicon damage. Unlike the core, the SCR protection structures are carefully designed, so they can be stressed by a high current many times without significant damage [11].

The basic SCR structure is demonstrated in Figure 3.6. The device consists of a vertical PNP and a lateral NPN bipolar transistors. The PNP transistor is made of a p^+ emitter diffusion in an n-well forming a base and a p-well as a collector. The NPN transistor consists of an n^+ emitter diffusion, the p-well for a base, and the n-well forming its collector. Resistances of the p-well and n-well regions are annotated as corresponding lumped resistors. An input of the SCR protection device called *anode* is tied to the emitter of the PNP parasitic transistor and n-well n^+ contacting diffusion and is terminated on an I/O pad, whereas a *cathode* consisting of the emitter of the NPN parasitic transistor and the p-well p^+ contacting diffusion is usually tied to the lowest potential on an IC.

The latch-up effect, which is driving behavior of SCR protection devices, occurs when the anode is charged positively with respect to the cathode. The junction formed of the n-well and the p-well is then polarized in the reverse direction and at some point, an avalanche breakdown of the junction substantially increases a current through the junction. The high avalanche current at some point polarizes the emitter—base junction of the NPN transistor in forward direction. As the base—collector junction is reverse-biased during an ESD event, the NPN transistor starts to operate in active mode and even though having low β factor, the resulting collector current flowing through the p-well resistance generates a voltage drop on it forward-biasing the PNP bipolar transistor base—emitter junction forcing the PNP BJT also into active mode. The resulted positive feedback drives the latch-up and causes self-sustaining biasing of all the active junctions [12]. At this point, the anode—cathode voltage quickly drops introducing negative differential resistance in SCR I-V characteristic manifesting itself as the snapback phenomenon. SCR usually exhibits lower holding voltage V_h than

MOSFET devices. Also, the total area of the SCR-based protection device is several-times smaller than the based on MOSFET and is therefore very useful in high-frequency pads where the parasitic area-dependent capacitance limits the useful frequency range.

In case of the negative voltage impulse on the anode with respect to the cathode, the p-well—n-well junction is forward biased and in case of wide enough junction area, no damage occurs. In this state, the protection exhibit *simple I-V* characteristics.

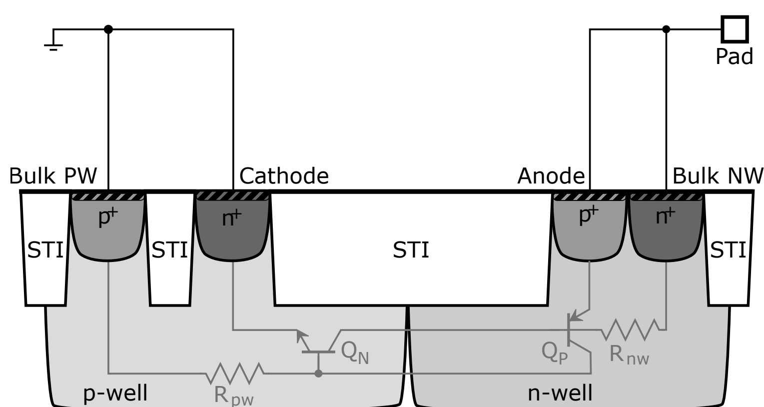

Figure 3.6: *SCR Structure*

The I-V characteristic of the SCR protection device is shown in Figure 3.7. The trigger point (V_{t1}, I_{t1}) is the voltage when the device latches up. Thanks to the low V_h, the current conducted during the latch up can be significantly higher than in case of MOSFET-based protection devices to generate the same amount of heat that needs to be dissipated into surrounding volume. For example, the 0.35 µm technology SCR device with $V_\mathrm{h} \approx 1$ V presented in [19] can withstand as much as six-times more current than an NMOST-based device fabricated in the same technology.

The major drawback of the SCR protection devices is the fact that because of their high trigger voltage (in some technologies more than 16 V) and relatively high time-to-trigger due to by order of magnitude longer onset of latch-up, their use is limited [19]. Solution to slow SCR reaction is complementing it by a secondary protection coupled to the SCR by a current-limiting resistor as shown in Figure 3.8. In this case, the smaller and faster secondary protection activates early protecting the core for short period before the SCR activates and shunts the majority of the ESD charge away.

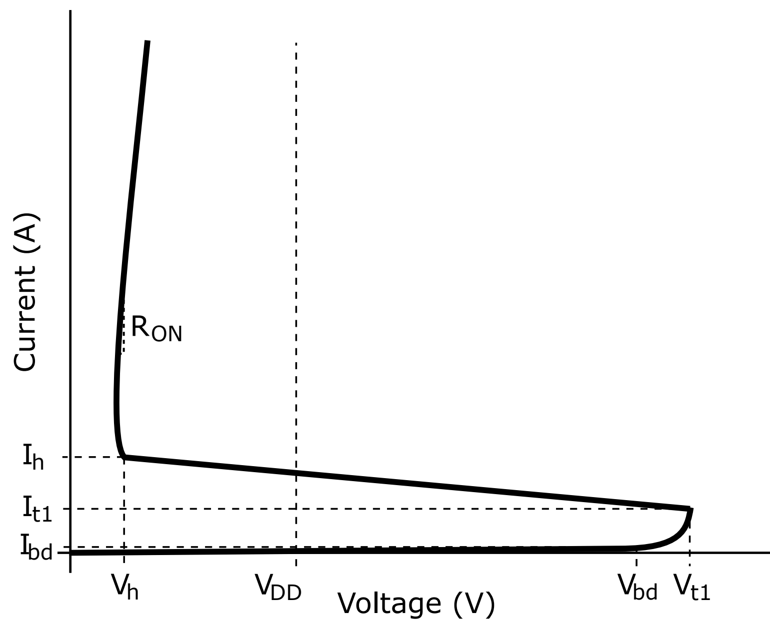

Figure 3.7: *I-V Characteristics of SCR Device*

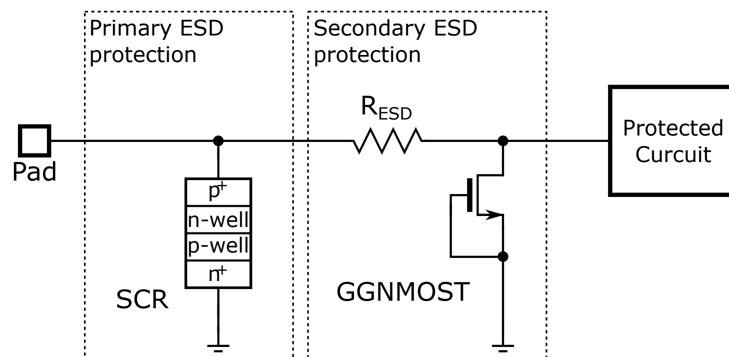

Figure 3.8: *Example of I/O Protection Circuit with Primary SCR and Resistor and GGNMOST as Secondary Protection*

3.2.1 SCR Macro-Model

Enhanced macro-model presented in [20] is used. It comprises of three-pin VBIC n-type BJT model, standard SGP p-type BJT model, p-well and n-well resistance models – both lumped temperature and voltage-independent. The VBIC model able to model avalanche ionization proved to be effective in modeling the snapback action in case of the NMOST macro-model. The PNP bipolar transistor may then be modeled by a standard SGP model which should speed up simulations. The avalanche ionization current is in the VBIC modeled as

$$I_{\mathrm{gc}}^{\mathrm{BJT}} = I_{\mathrm{tot}}\, A_{VC1}\, V_{bci} \exp\left(-A_{VC2}\, V_{bci}^{\mathrm{mod}}\right)^{M_C-1} \qquad (3.11)$$

where I_{tot} is the total leakage current through the base-collector junction, V_{bci}^{mod} is a built-in potential of the base-collector junction diminished by a voltage drop across the junction, M_C is a junction gradient coefficient, and A_{VC1} and A_{VC2} are fitting parameters. This new approach replaces external variable current source used for impact ionization substrate current modeling in many papers [8, 21]. Even though widely used in the case of NMOST model, the current source may cause convergence difficulties during simulations.

Figure 3.9 shows the complete SCR macro-model.

P-well and n-well resistances each require a fitting parameter: R_{pw} and R_{nw} respectively.

Totally, 30 fitting parameters are required for the SCR macro-model calibration: 13 in the VBIC BJT core model, 15 in SGP BJT model, and the two remaining for the p-well and n-well resistance models.

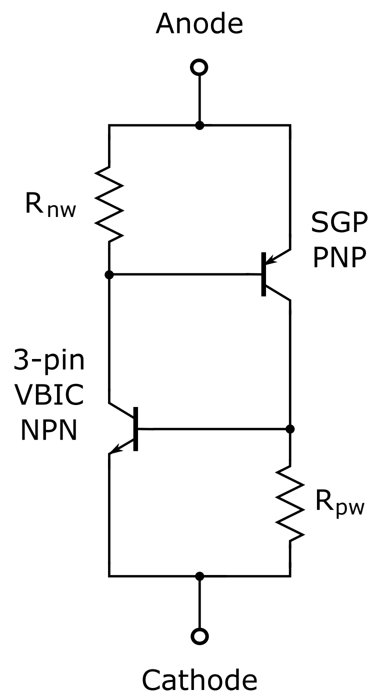

Figure 3.9: *Macro-Model of the SCR and MLSCR Devices*

VBIC NPN Model	SGP PNP Model	Resistance Models
AVC1	BF	RNW
AVC2	NF	RPW
IBCI	BR	
IBCN	NR	
IBEN	ISE	
IS	NE	
NEN	ISC	
NF	NC	
RBI	VAF	
RBX	VAR	
RCI	IKF	
RCX	IKR	
RE	RB	
	RC	
	RE	

Table 3.2: *Summary of SCR and MLSCR Macro-model Parameters*

3.3 Modified Lateral SCR

One of the possible modifications of the SCR structure that decrease the high trigger voltage is implementation of an n^+ *bridging diffusion* into the interface between n-well and p-well that due to much higher doping level of the n^+ implantation increases electric field on the n^+—p-well junction forcing it to enter the avalanche breakdown for much lower junction voltage than the original p-well—n-well junction. The impact-ionization generation factor is defines as

$$G^{\mathrm{II}} = \frac{\mathrm{d}n}{\mathrm{d}t} + \frac{\mathrm{d}p}{\mathrm{d}t} = \alpha_{\mathrm{n}} n v_{\mathrm{n}} + \alpha_{\mathrm{p}} p v_{\mathrm{p}}, \tag{3.12}$$

where n and p are concentrations of electrons and holes respectively, α_{n} and α_{p} are impact-ionization coefficients of electrons and holes respectively, and v_{n} and v_{p} are velocity of electrons and holes respectively. Both α_{n} and α_{p} strongly depends on electrical field E as

$$\alpha \propto \exp\left(\frac{E}{E_{\mathrm{crit}}}\right), \tag{3.13}$$

Thus rise to electric field causes increase in impact-ionization generation rate thus increasing effective minority carrier current generated for the same anode–cathode voltage. The trigger voltage can as such be reduced to approximately 14 V.

As for the standard SCR protection, also for MLSCR-based structure applies the need for additional faster secondary device. The MLSCR structure is shown in Figure 3.10.

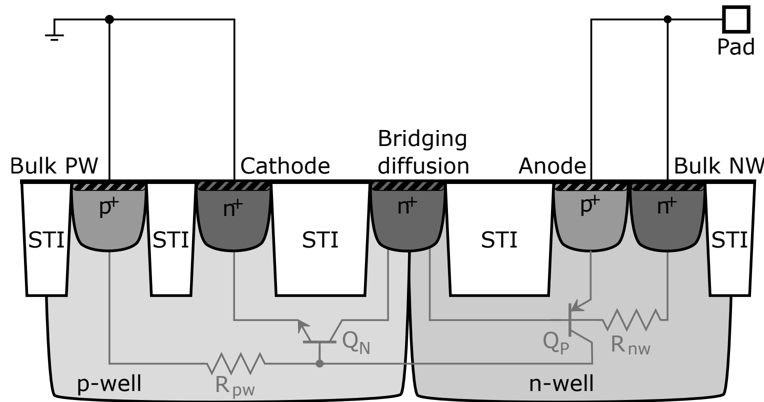

Figure 3.10: *MLSCR Structure*

3.3.1 MLSCR Macro-Model

Modified lateral silicon controlled rectifier is basically just a layout modification of the original SCR improved by introduction of the bridging diffusion. The MLSCR macro-model is thus formally identical to the one used for the SCR in Figure 3.9. Differences in the trigger and holding voltages V_{t1} and V_{h} can be reflected into the macro-model behavior through re-calibration of its fitting parameters. This also implies that the number of fitting parameters is identical to that of the SCR macro-model, i.e., 30 in total, and may be found in Table 3.2.

3.4 Low-Voltage Triggered SCR

Even though the structural modification in the MLSCR device decreases the trigger voltage V_{t1}, its level may still be too high for protection of low-voltage gate oxides. Further decrease of the trigger voltage is desirable and luckily possible by introduction of a single-finger GGNMOST structure instead of the bridging diffusion. The GGNMOST structure triggers at much lover voltage levels than reverse-biased n^+—p-well. Besides the snapback action of the GGNMOST with the NPN transistor, the anode current is further boosted by the NPN—PNP latch-up triggered by the snapback.

The LVTSCR protection device combines the best of both the NMOST and SCR-based protection devices. It has sufficiently low trigger voltage (units of volts), low holding voltage V_h, low area consumption, and faster trigger reaction. Additional advantage is possibility to modify the trigger voltage of the LVTSCR structure within limited range by a simple change of NMOST dimensions. The protection device may be therefore partially optimized for a specific need. A structure of the LVTSCR is shown in Figure 3.11.

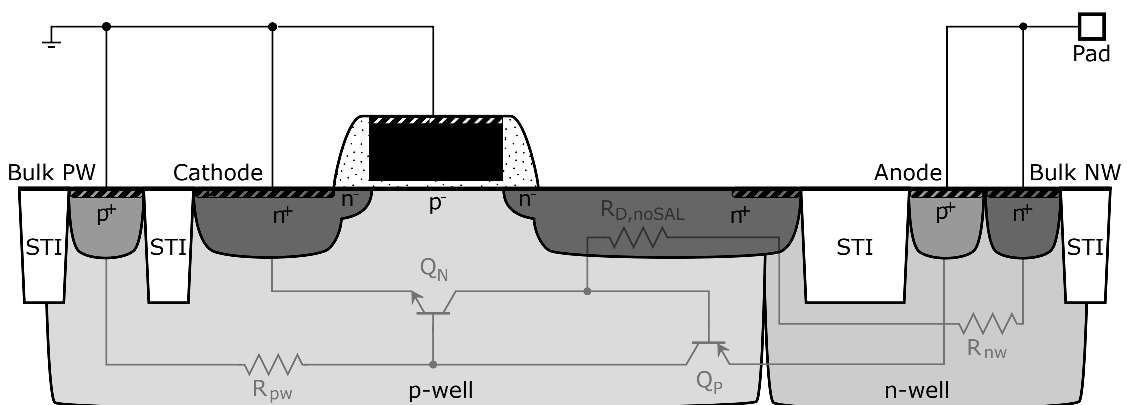

Figure 3.11: *LVTSCR Structure*

3.4.1 LVTSCR Macro-Model

As in case of NMOST macro-model, dedicate substrate current source and SGP NPN bipolar transistor model were replaced by a single VBIC model [20]. Also, the PNP bipolar transistor modeled by an SGP model was replaced by a parasitic model inside the VBIC model. It means that the number of fitting parameters may be further decreased. The macro-model also includes already characterized BSIM NMOST model from a standard PDK with extended drain modeled again as a lumped diffusion resistor and linear lumped voltage and temperature-independent resistors modeling p-well and n-well resistances (fitting parameters R_{pw} and R_{nw} respectively). NMOST substrate current that causes it to trigger is modeled identically to the ESD NMOST macro-model described in Section 3.1.2 – see equations 3.4 and 3.6. See Figure 3.12 for macro-model topology.

Total number of fitting parameters is 17: two in the NMOST substrate model, two in the substrate and n-well-resistance models, and remaining 13 in the VBIC BJT. Fitting parameter of the core NMOST model ALPHA1 was again excluded. Summary of the parameters is in Table 3.3.

BSIM NMOST Model	SGP PNP Model	Resistance Models
ALPHA0	AVC1	RNW
BETA0	AVC2	RPW
	IBCI	
	IBCN	
	IBEN	
	IS	
	NEN	
	NF	
	RBI	
	RBX	
	RCI	
	RCX	
	RE	

Table 3.3: *Summary of LVTSCR Macro-model Parameters*

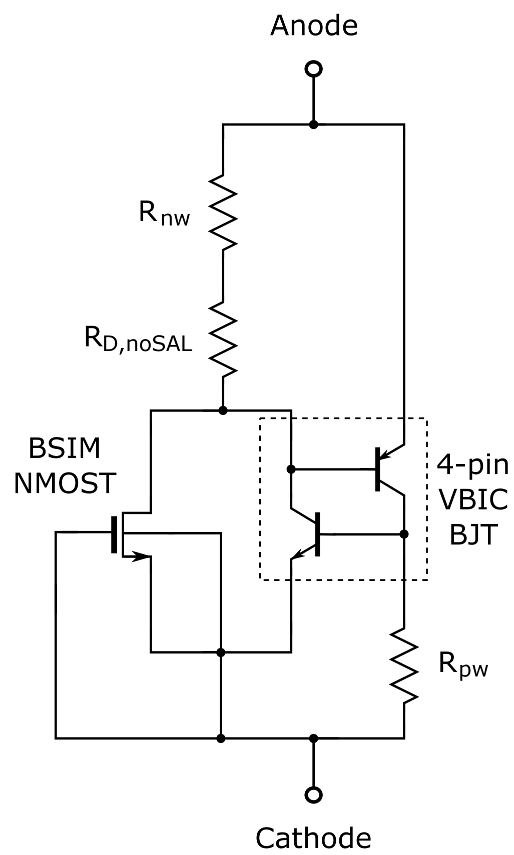

Figure 3.12: *Macro-Model of LVTSCR*

CHAPTER 4

CHARACTERIZATION OF ESD PROTECTIONS USING TLP AND HBM

Transmission-line pulse (TLP) is a modern approach to characterize ESD protection designs. It was presented in 1985 in [22]. In contrast with the component-level ESD models like HBM or MM whose output is only an ESD withstand voltage level, the TLP can provide much more information to the designers about various properties of a specific ESD protection device. It allows measurements of the high current I-V characteristic point-by-point and thus making understanding of the processes inside the protection circuits much more easier. Illustrative scheme and equivalent circuit of the TLP machine with simplified principle of I-V characteristic compilation procedure are shown in Figure 4.1a and Figure 4.1b.

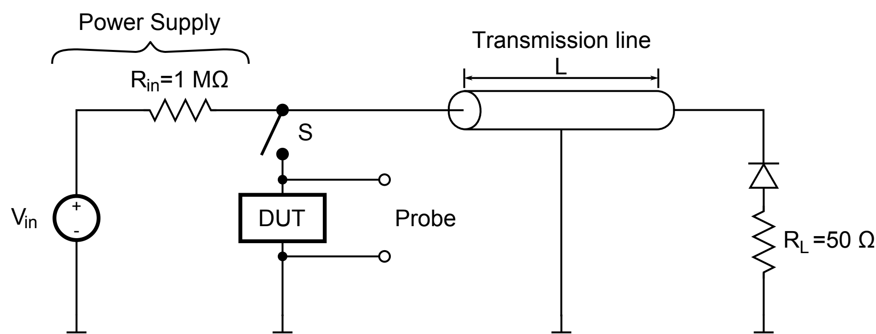

Figure 4.1a: *TLP Measuring System (Scheme)*

In a TLP tester, a transmission line is charged by the high-voltage generator, disconnected from it, and discharged into the DUT pad while the supply or ground pads are

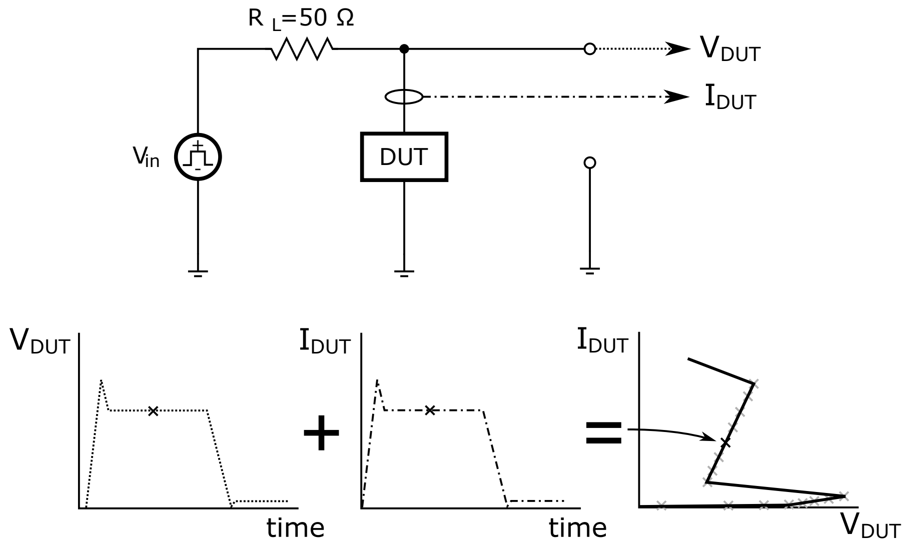

Figure 4.1b: *TLP Measuring System (Equivalent Circuit and Principle of I-V Char. Composition)*

connected to the TLP tester ground creating short current pulse forced to the DUT. Pulse width can be varied by choosing different length of the coaxial cable (approx. 10 ns per meter for a 50 Ω cable). The transmission line has its impedance at the opposite end matched by a polarized load to the characteristic impedance of the transmission line to prevent reflections of the pulses. The pulse waveform has much steeper edges than for example the HBM pulse. This is caused by a distributed capacitance of the transmission line making the rise time lower than 2 ns [10]. Also, in contrast with HBM pulses whose waveforms are of RC shape, pulse of TLP is due to a distributed nature of the transmission line shaped like square wave presenting quasi-static part in the waveform. Measurements are done in this quasi-static part of the pulse. The raw output of single TLP measurement is a set of pair values – voltage across the DUT and current through the DUT. The current waveform doesn't have to be captured, the current in the steady-state region can be calculated (based on the knowledge of the characteristic impedance) as

$$I_{\mathrm{DUT}}(t) = \frac{(V_{\mathrm{in}} - V_{\mathrm{DUT}}(t))}{R_{\mathrm{L}}}, \tag{4.1}$$

where R_{L} is the characteristic impedance of the coaxial cable.

The final I-V characteristic is then simply a set of current versus voltage points derived in given number of TLP measurements.

4.1 Obtaining I-V Characteristics Using HBM Tester

Possibility of utilizing HBM tester to obtain I-V characteristics was suggested in [1]. In principle, when both current through and voltage across the ESD protection device is being captured during an HBM stress test, it is possible to ascertain approximate values of the most important regions of the ESD protection I-V characteristics, i.e., trigger and snapback (holding) voltages and on-state resistance R_{on}.

The major differences between TLP and HBM I-V characteristic capturing methods are:

1. Necessity to measure both transient voltage and current of the protection due to undefined impedance of the IC or probe fixture and high voltage source which would otherwise link those two quantities together,

2. Absence of quasi-static portion of the TLP in HBM pulse that would allow precise capturing of transient voltage and current and also enables time averaging to further refine the final I-V characteristics.

The first point can be addressed simply by using two dedicated probes, the second by performing several measurements and averaging the results before compiling the final I-V characteristics.

Figure 4.2a shows transient voltage and current through a ESD protection DUT measured using two-pin HBM method described in [1]. After both curves are aligned accounting for different time delays between voltage and current probes, final I-V characteristic is shown in Figure 4.2b. All the important regions of the DUT are clearly apparent and measurable. For additional details about the method see [1].

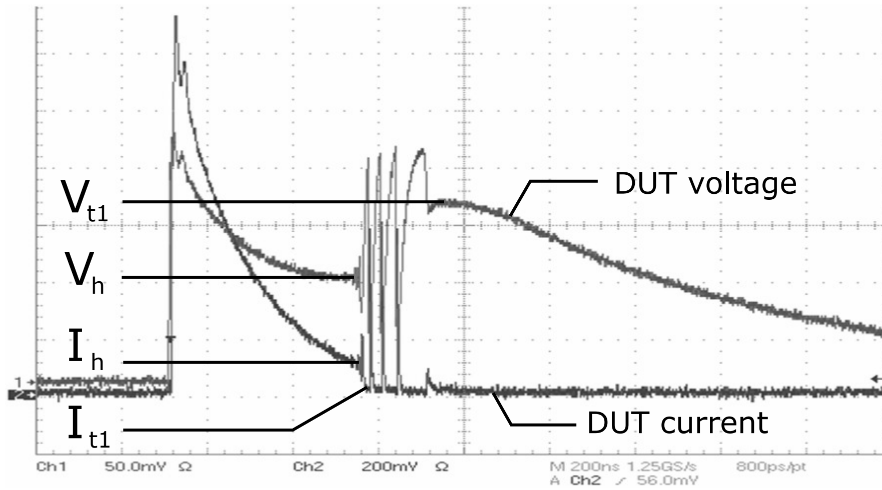

Figure 4.2a: *Transient Voltage on and Current through DUT Obtained by HBM ([1])*

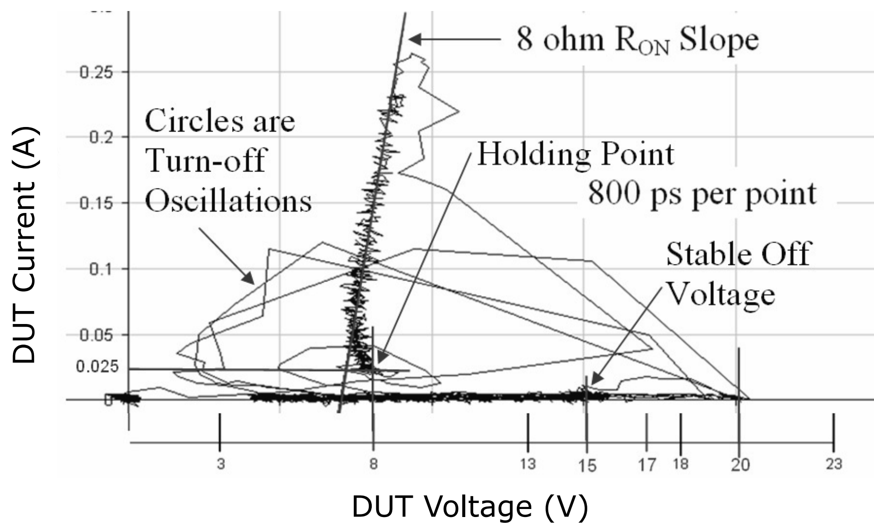

Figure 4.2b: *Final DUT I-V Characteristic Measured by HBM Pulse ([1])*

CHAPTER 5

DIFFERENTIAL EVOLUTION AND NELDER–MEAD SIMPLEX

Following chapter introduces reader to the basic principles and properties of optimization algorithms used it the ESD model calibration method. It should not be in any case considered an exhaustive study of the algorithms, further details may always be found in original papers [23, 24].

5.1 Differential Evolution

Evolutionary optimization algorithms are in general very robust and fast-to-converge algorithms. They are less susceptible to fall into local optimum due to their *global exploitation* nature as in case of standard gradient-based optimization algorithms (hill-climbing, Tabu search, etc.). Global exploitation methods cover large portion of an optimization space and as such shall be always bounded to ensure reasonable coverage density and exclude unreasonable values of fitting parameters. Thanks to the natural selection of the most fitted member of the population of parameter vectors, the possibility of the premature convergence in a local minimum is minimized [23]. Moreover, the DE is in contrast with gradient-based optimization methods able to optimize in non-continuous objective-function-space and enables the designer to introduce for example penalty coefficients to detect optimization violations. The algorithm was in past proven

to be very effective and robust in global optimum search tasks of various problems, e. g., [25, 26].

The functionality of DE algorithm can be described in the following way: let the vector of system parameters for specific member of the specific generation be designated as

$$\mathbf{x}_{i,G}, \qquad i = 0, 1, \ldots, NP - 1, \tag{5.1}$$

where NP is a number of D-dimensional parameters in the parameter vector (D doesn't change during optimization process) and G determines the sequence of the generation. All the parameter vectors $\mathbf{x}_{i,G}$ of the same generation are called *population*. If the initial values of parameters within the parameter vector are unknown, their values can be generated randomly using uniform probability distribution. After each generation, new parameter vector (population member) is generated and is used in next iterative step. It is derived as a weighted difference of the first and the second member and then summed with the third member. If the newly created parameter vector yields lower value of the objective function than a previous "best" population member, the new member replaces the former "best" one. In addition, the best fitted member of the population (i.e., the parameter vector with lowest objective function) is stored to keep track of the progress of the optimization process.

The detailed principle of generation and selection of the best fitted member of the population is as follows: for each parameter vector $\mathbf{x}_{i,G}$, a trial vector $\mathbf{u}$ is calculated as

$$\mathbf{u}_i = \mathbf{x}_{r_1,G} + F \cdot \left(\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G}\right), \tag{5.2}$$

$$i = 0, 1, \ldots, NP - 1, \tag{5.3}$$

where integers $r_1 \neq r_2 \neq r_3 \neq i \wedge r_1, r_2, r_3 \in \langle 0, NP - 1 \rangle$ are randomly chosen with uniform probability distribution, F is a real weighting constant determining the influence of the differential variation vector $\left(\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G}\right)$. The role of the trial vector can be seen in Figure 5.1.

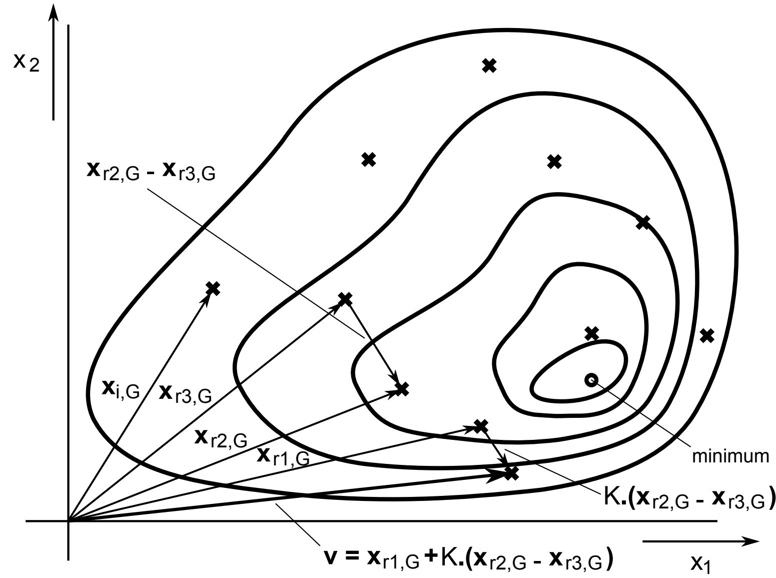

Figure 5.1: *Representation of the Differential Evolutionary Algorithm*

To implement the principle of a mutation and crossover, the new D-dimensional vector $\boldsymbol{t}_i$ needs to be created. The elements of the $\boldsymbol{t}_i$ vector are random numbers with uniform probability distribution, where $t_{i,j} \in \langle 0, 1 \rangle$, $j = 0, 1, \ldots, D-1$. Now, each element $t_{i,j}$ of the $\boldsymbol{t}_i$ vector is compared against the value of CR crossover coefficient and in case the value of CR is higher than $t_{i,j}$, the $u_{i,j}$ is placed in the crossover vector $\boldsymbol{v}_i$ as j-th element, else the original value $x_{i,j,G}$ is used. In addition, the dimension index j is compared against randomly generated integer $R = 0, 1, \ldots, D-1$ with uniform probability distribution and in case of match, the $v_{i,j,} = u_{i,j}$. This can be mathematically described as

$$v_{i,j} = \begin{cases} u_{i,j}, & t_{i,j} \geq CR \vee j = R \\ x_{i,j,G}, & \text{otherwise} \end{cases}, \tag{5.4}$$

$$j = 0, 1, \ldots, D-1. \tag{5.5}$$

The graphical representation of the equation 5.4 is shown in Figure 5.2.

The final step is to solve objective function for the crossover vector $\boldsymbol{v}_i$ and compare its value against the value of objective function of the original vector $\boldsymbol{x}_{i,G}$. The vector

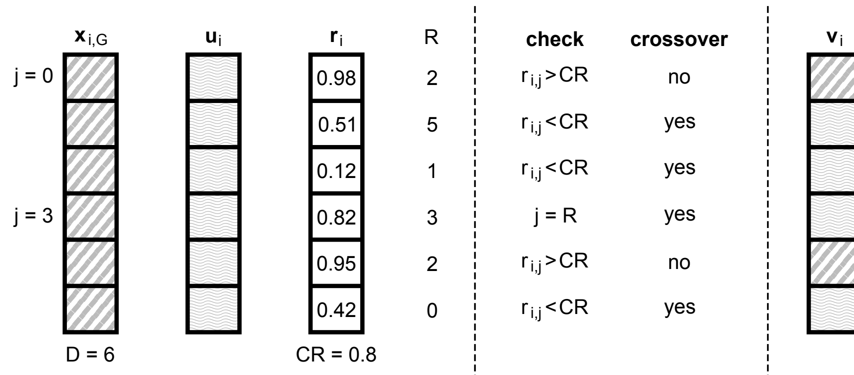

Figure 5.2: *Example of the Crossover Process*

with lower objective function becomes the new member of $(G + 1)$-th generation, mathematically written as

$$\boldsymbol{x}_{i,(G+1)} = \begin{cases} \boldsymbol{u}_i, & f_{\text{obj}}(\boldsymbol{u}_i) < f_{\text{obj}}(\boldsymbol{x}_{i,G}) \\ \boldsymbol{x}_{i,G}, & \text{otherwise} \end{cases}, \tag{5.6}$$

$$i = 0, 1, \ldots, NP - 1, \tag{5.7}$$

where $f_{\text{obj}}(\boldsymbol{y})$ represents the value of the objective function for $\boldsymbol{y}$ vector in its argument. After each generation, the best member (the one with the lowest value of the objective function) is selected and stored for the next generation. This ensures the progress of determination of the best set of parameters. The algorithm can be repeated indefinitely, until the ideal solution is found, or the maximum number of generations can be specified to limit the number of iterations of the optimization.

5.2 Nelder–Mead Simplex Algorithm

The NMSA, developed in early 60s, was designed to be effective in solving standard unconstrained optimization problems. NMSA belongs into so called *local exploitation method* family which performs optimum search in a local area in sense of optimization space coverage – this is in contrast with the DE which is considered to be a global exploitation method as explained in previous section. The NMSA is based on comparison

of function values of endpoints (*vertices*) of a *simplex* accompanied by adaptation of this simplex to the objective function surface – *landscape*. A simplex may be defined as a generalized set of vertices in arbitrary number of dimensions forming an object (formally named *polytope*) with a convex hull. It is basically generalization of terms polygon in two and polyhedron in three dimensions for any number of dimensions.

The algorithm is generalization and improvement of the original idea presented in [27]. It brings more efficient and robust tracking of the optimization space by adapting the simplex transformation based on the space landscape.

Initial simplex is defined during random generation of $D{+}1$ vertices $P_0, P_1, P_2, \ldots P_D$. The $(D+1)$-dimensional simplex covers the whole parameter space. Each vertex P_i has a value of the objective function y_i. Let's also define vertices where the y_i has lowest and highest values as

$$P_\mathrm{l} : \; y_\mathrm{l} = \min_i \left(y_i \right), \tag{5.8}$$

$$P_\mathrm{h} : \; y_\mathrm{h} = \max_i \left(y_i \right). \tag{5.9}$$

Finally, let's also denote the centroid of the simplex as $\bar{P}$.

Three transformations of the simplex are defined: *reflection*, *contraction* and *expansion* [24]. Each of those transformations changes position of an arbitrary vertex (usually the one with the highest value of the objective function y_h) in such a way that all the vertices move towards the global optimum which will very probably be eventually reached.

Reflection

Let's denote the reflection of the P_h as P^*, function value at the reflected vertex as y^*. Then the reflection may be defined as

$$P^* = (1 + \alpha_\mathrm{NMSA}) \, \bar{P} - \alpha_\mathrm{NMSA} P_\mathrm{h}, \qquad \alpha_\mathrm{NMSA} > 0, \tag{5.10}$$

where α_{NMSA} is a reflection coefficient. It is obvious that new reflected point P^* lies on the line that interconnects the centroid $\bar{P}$ and P_{h} and is located on the other side of the line than P_{h} with respect to the centroid. It also sets following relation to distances between the two vertices and the centroid

$$\mathbf{distance}\left(P^*, \bar{P}\right) = \alpha_{\mathrm{NMSA}} \cdot \mathbf{distance}\left(P_{\mathrm{h}}, \bar{P}\right). \tag{5.11}$$

There are three outcomes of the reflection process:

1. $y_{\mathrm{l}} \leq y^* \leq y_{\mathrm{h}} \ \wedge \ y^* \leq \max_i \left(y_i\right), \ i \neq \mathrm{h}$: the reflection process is repeated with vertex P_{h} in the simplex replaced by P^* but as there exists other $P_i, \ i \neq \mathrm{h}$ having higher function value than y^*, the new P^* does not become new P_{h},

2. $y^* < y_{\mathrm{l}}$: algorithm continues with expansion process with vertex P_{h} in the simplex replaced by P^* becomming new P_{l},

3. $y^* > y_{\mathrm{h}} \ \vee \ \left(y_{\mathrm{l}} \leq y^* \leq y_{\mathrm{h}} \ \wedge \ y^* > \max_i \left(y_i\right), \ i \neq \mathrm{h} \right)$: algorithm continues with contraction process, P^* replaces the original P_{h} and becomes new P_{h} if it has lower function value, otherwise there is no change to the simplex.

Expansion

Vertex P^{**} that is the endpoint of expanded line formed by vertex P^* and centroid $\bar{P}$ may be defined as

$$P^{**} = \gamma_{\mathrm{NMSA}} P^* + \left(1 - \gamma_{\mathrm{NMSA}}\right) \bar{P}, \qquad \gamma_{\mathrm{NMSA}} > 1, \tag{5.12}$$

where γ_{NMSA} is an expansion coefficient. It is a ration between a distance from the centroid and P^* vertex and the centroid and P^{**} vertex:

$$\gamma_{\mathrm{NMSA}} = \frac{\mathbf{distance}\left(P^{**}, \bar{P}\right)}{\mathbf{distance}\left(P^*, \bar{P}\right)}. \tag{5.13}$$

If $y^{**} < y_{\mathrm{l}}$, original P_{h} is replaced by the new vertex P^{**}. On the other hand the expansion operation failed in case $y^{**} > y_{\mathrm{l}}$ and the whole algorithm is restarted with new simplex having the worst vertex P_{h} replaced by P^{*}.

Contraction

Vertex P^{**} that is the endpoint of contracted line formed by vertex P_{h} and centroid $\bar{P}$ may be defined as

$$P^{**} = \beta_{\mathrm{NMSA}} P_{\mathrm{h}} + \left(1 - \beta_{\mathrm{NMSA}}\right) \bar{P}, \qquad 0 > \beta_{\mathrm{NMSA}} > 1, \tag{5.14}$$

where β_{NMSA} is a contraction coefficient relating the three vertices in following way

$$\beta_{\mathrm{NMSA}} = \frac{\mathbf{distance}\left(P^{**}, \bar{P}\right)}{\mathbf{distance}\left(P_{\mathrm{h}}, \bar{P}\right)}. \tag{5.15}$$

If the new value $y^{**} > \min\left(y_{\mathrm{h}}, y^{*}\right)$, the function value of the new vertex P^{**} is worse than better of P_{h} or P^{*} and the simplex is modified by replacing all the vertices as

$$P_i = \frac{\left(P_i + P_{\mathrm{l}}\right)}{2}, \qquad i = 0, 1, 2, \ldots D. \tag{5.16}$$

and the algorithm is restarted. In case vertex P^{**} is better than both P_{h} and P^{*}, this vertex replaces the original P_{h} and again the whole algorithm is restarted.

The algorithm is stopped when a *standard error* of the function values, as it is called in [24], falls below a pre-defined critical value. This standard error is defined as

$$\epsilon_{\mathrm{stop}} = \sqrt{\frac{\sum_{i=0}^{D} \left(y_i - \bar{y}\right)^2}{D}}. \tag{5.17}$$

This criterion prevents the algorithm to indefinitely search the optimization space

which would happen if the simplex becomes too small.

Details and benchmarking information about the NMSA may be found in [24].

The NMSA was additionally implemented along the DE to overcome one of the shortcomings of the DE algorithm, i.e., slow convergence rate in the end of the optimization process [28]. Even though this fusion or hybridization of DE and NMSA was already presented in [7], their implementation follows different philosophy and requirements than the proposed variant. Instead of applying the NMSA after each DE iteration which may potentially affect optimization space coverage, the NMSA is applied only at the end of the optimization flow, after DE reaches critical point where the space coverage is low and population members are located near the best local (potentially global) optimum.

CHAPTER 6

PROPERTIES OF PROPOSED MODEL CALIBRATION METHOD

Main advantage of presented ESD model calibration method is the possibility to calibrate models using TLP or TLP-like measurement data (see Chapter 4 for details). This significantly simplifies and speeds up the calibration and also decreases requirements on technological process engineers who are then able to focus on more complex tasks. Majority of industrial TLP characterization systems are highly automated thus requiring only preparation of functional samples and their probing in case of bare IC dies. Even in-house developed TLP setups can be easily automated using either simple scripting or industrial-grade visual hardware-platform programing environments (e.g., LabView) and control over industrial interface buses like general purpose interface bus (GPIB).

Other advantage of the presented method is the fact that ESD protection devices have usually just two external nodes (or terminals) they interface with other parts of the IC with. The first is a pad terminal in case of I/O-type protections or power rail terminal in case of power-clamp or inter-domain power-coupling devices, the second one is a ground rail terminal. It is thus only necessary to do a single measurement of the pad or power rail terminals with the other terminal grounded exactly as it then operates in a real IC. The standard model calibration method which will be presented in later part of this chapter is based on separate calibration of each macro-model element thus requiring additional terminals to be exposed via dedicated I/Os introducing further error

into the measurements.

In case of MOSFET-based protection devices, MOSFET core model available in a PDK of a given technology may be used without any significant modifications. It is due to the fact that those devices are correctly calibrated for all the valid dimensions and range of biasing with all the transient properties and advanced effects (such as gate-induced drain leakage (GIDL) or substrate current induced body effect (SCBE) that have impact on behavior during ESD-related events) characterized by the technology process engineers. The only components of those models that may need to be re-characterized are the high current high voltage effects like models of substrate or impact ionization currents. It dramatically decreases number of fitting parameters of the final ESD macro-models to be extracted without any significant loss of precision. Structures that can't benefit from availability of already characterized core models like SCR-based protections may require also proper extraction of transient-related parameters like intrinsic and extrinsic capacitances and other parasitic elements, especially if those ESD macro-models are to be used in RF design characterization or verification. Extraction of those parts of macro-models is not part of this thesis but possible approaches are presented in Chapter 9.

The proposed automated ESD macro-model calibration method leverages benefits of the differential evolution algorithm such as ability to search for the global optimum in non-continuous parameter space, possibility to introduce penalization factors to emphasize specific parts of I-V characteristics or dismiss unrealistic parameter sets. With large enough population size it is also more resilient to presence of local optima in the parameter space as it covers larger part of the space more densely. The negative aspect of large populations is slow progression toward the global optimum [28]. As all the population members of a generation have to be processed before advancing to a next one, larger population inherently requires more simulation runs to be performed slowing down the progress, especially in the final stage of the optimization process where all or majority of the population members are in a "gradient well" of the global optimum. Second optimization algorithm was thus implemented to improve efficiency of the calibration method. Even though a simple gradient-based algorithm applied on the best population member would seem to be sufficient, experience showed that the

best population member derived by DE algorithm may not necessarily be related to the global optimum. One possibility would be to run the DE unless the majority of population members differs in their objective function value less then some pre-set amount. This would increase the probability that what is reported by the DE algorithm as the global optimum is in fact really the global optimum. Unfortunately, it was shown during the method development that the number of generations required to satisfy this condition is enormous. In the end, different type of optimization algorithm was chosen: *Nelder-Mead simplex algorithm*. In contrast with other gradient-based algorithms it reuses the whole set of the final population generated by the DE and using specific set of transformations, thoroughly described in Chapter 5.2, further refines nearly optimal parameter set. Probability of reaching local optimum is dramatically decreased and the speed-up comparing to the DE is up to a factor of 2 in some cases.

Differential evolution optimization algorithm as well as all the control and auxiliary functions of the proposed method were implemented as modules in software package *Octave* which is an open-source alternative of commercial Matlab numerical software. The NMSA code was already implemented as a function in the Octave package and was used in the calibration flow. Languages and the phylosophy of both Octave and Matlab match in major aspects and both implements similar functionality in compatible way. One important benefit that tipped the balance in favor of Octave is the fact that it is open-source and free to be used in industrial environment.

An optimization problem definition was also implemented as a module thus enabling efficient switching between different scenarios. The method was for example also tested on optimization of an folded-cascode operational amplifier design. Effort required to port the method to this type of optimization problem was question of few minutes spent by re-definition of an objective function and fitting parameters.

The proposed method does not rely on any specific simulator. It may be easily ported to use any spice simulator available (e.g., Cadence Spectre, M. G. Eldo, NgSpice, etc.) providing that the simulator can be controlled via a command line. Cadence Spectre was selected as a simulation tool for the method benchmarking, simply because it was readily available in the author's workspace. It is also possible to run the Octave core process on a local computing machine but execute a design simulation on a computation farm

available in most industrial environments. This may speed-up macro-model calibration even more as computation farms are often equipped with large number of processors and operating memory enabling to introduce parallelism to design simulations.

New form of objective function used to quantify fitness of a specific population member was developed to suit the needs of the proposed method, i.e., enable possibility of penalization and to make meaningful benchmarking across macro-models possible. The function was designated as *weighed root-mean-square deviation* (WRMSD) and is defined as

$$f_{\mathrm{obj}} = \sqrt{\frac{\sum_{i=1}^{n}\left(f_{\mathrm{w}}[i]\cdot(V_{\mathrm{meas}}[i]-V_{\mathrm{sim}}[i])^2\right)}{n}}, \tag{6.1}$$

where V_{meas} and V_{sim} are measured and simulated voltage vectors respectively and f_{w} is a vector of weighting coefficients having the same dimension as both the V_{meas} and V_{sim} vectors. This weighting vector is used to emphasize specific parts of an I-V characteristic (e.g., breakdown and trigger regions are often more important than for example off-state leakage of an ESD protection device).

6.1 Requirements of Proposed Calibration Method

Current calibration method implementation requires following items in specific format: design test-bench netlist file instantiating a macro-model to be calibrated, file with TLP or TLP-like data in comma-separated format of current and voltage of ESD protection device, and a configuration file containing all the setup of the calibration method.

As the TLP measurements are done in the quasi-static region of the current pulse and then averaged within the limits of the pulse, it is valid to assume that a DC simulation is sufficient to capture the protection device I-V characteristic. The simulation netlist thus consists of a DC current source connected to the pad-interfacing terminal of an instance of the macro-model. It may also be necessary to include parasitic elements such as track resistances, etc. The netlist file must also define a simulation to be performed – in this case DC current sweep. The last essential part is definition of the custom

ESD model library that contains definition of the calibrated macro-model. Schematic depiction of one possible calibration test-bench is shown in Figure 6.1 (macro-model being calibrated is designated as *DUT*).

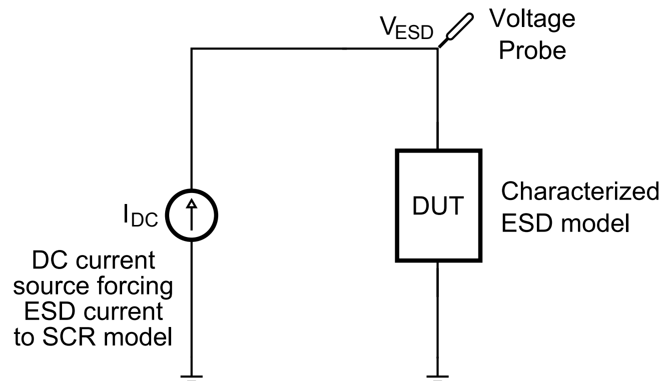

Figure 6.1: *Scheme of the DC Simulation Test-Bench for Macro-Model Calibration.*

The configuration file defines the all required properties of the optimization algorithms such as population size, crossover probability and differential weighting factors, and the highest acceptable value of the objective function $f_{\text{obj}}^{\text{TERM}}$ in case of differential evolution and termination relative size of a simplex and algorithmic method type of Nelder-Mead simplex algorithm. Parameter $f_{\text{obj}}^{\text{TERM}}$ was added to limit calibration precision in favor of speed as especially in case of DE, benefit of decreased calibration error is progressively more time costly and at some point even wasteful. Additionally, option to limit total number of iterations was implemented for both algorithms. This is useful in case it's not possible to reach the maximum acceptable value of the objective function which may be caused by for example too narrow limits of one or more fitting parameters. Important part of the file is section with fitting parameters definition. It groups all the fitting parameters along with their respective upper and lower bounds to limit optimization space size by excluding unreasonable parameter values. Last useful option offers possibility to define regions of an I-V characteristic with higher weight thus setting penalization if those regions differs against measured data.

6.2 Flow of Proposed Calibration Method

Differential evolution starts by generating an initial population of the first generation. Values of the fitting parameters are generated randomly with uniform probability distribution withing bounds specified in the method configuration file. Evaluating objective function value of each population member means to execute one simulation run. When the whole population exists, the DE algorithm progresses by steps described in detail in Chapter 5.1. Each population generation yields its best fitted member having the lowest objective function value. If the maximum value of the objective function $f_{\text{obj}}^{\text{TERM}}$ is reached, population member having or surpassing its value is reported and the calibration process is terminated. In case when maximum number of iterations is reached without satisfying $f_{\text{obj}}^{\text{TERM}}$, the DE is terminated and NMSA continues with the current generation population members using simplex transformations described in Chapter 5.2 until the relative simplex size is lower than the value specified in the configuration file or the maximum number of iterations was performed whichever variant occurs first. The flow diagram of the proposed calibration method is presented in Figure 6.2 (actions highlighted in gray are performed by a circuit simulator).

6.3 Standard Model Calibration Method

Macro-model parameters extraction flows available in literature is presented for NMOST and SCR structures as comparison cases.

Procedure for NMOST macro-model parameters extraction is described in [8]. Model presented in the paper uses avalanche current definition in equation (6.2).

$$I_{\text{gen}} = (M-1)\cdot(I_{\text{D}}+I_{\text{C}}), \tag{6.2}$$

$$M = \frac{1}{1-K_1\cdot\exp\left(\frac{K_2}{V_{\text{DS}}-V_{\text{dsat}}}\right)}, \tag{6.3}$$

Parameter M is avalanche multiplication factor, and K_1 and K_2 are additional fitting parameters. First, the NMOST core model part I-V characteristics are extracted by

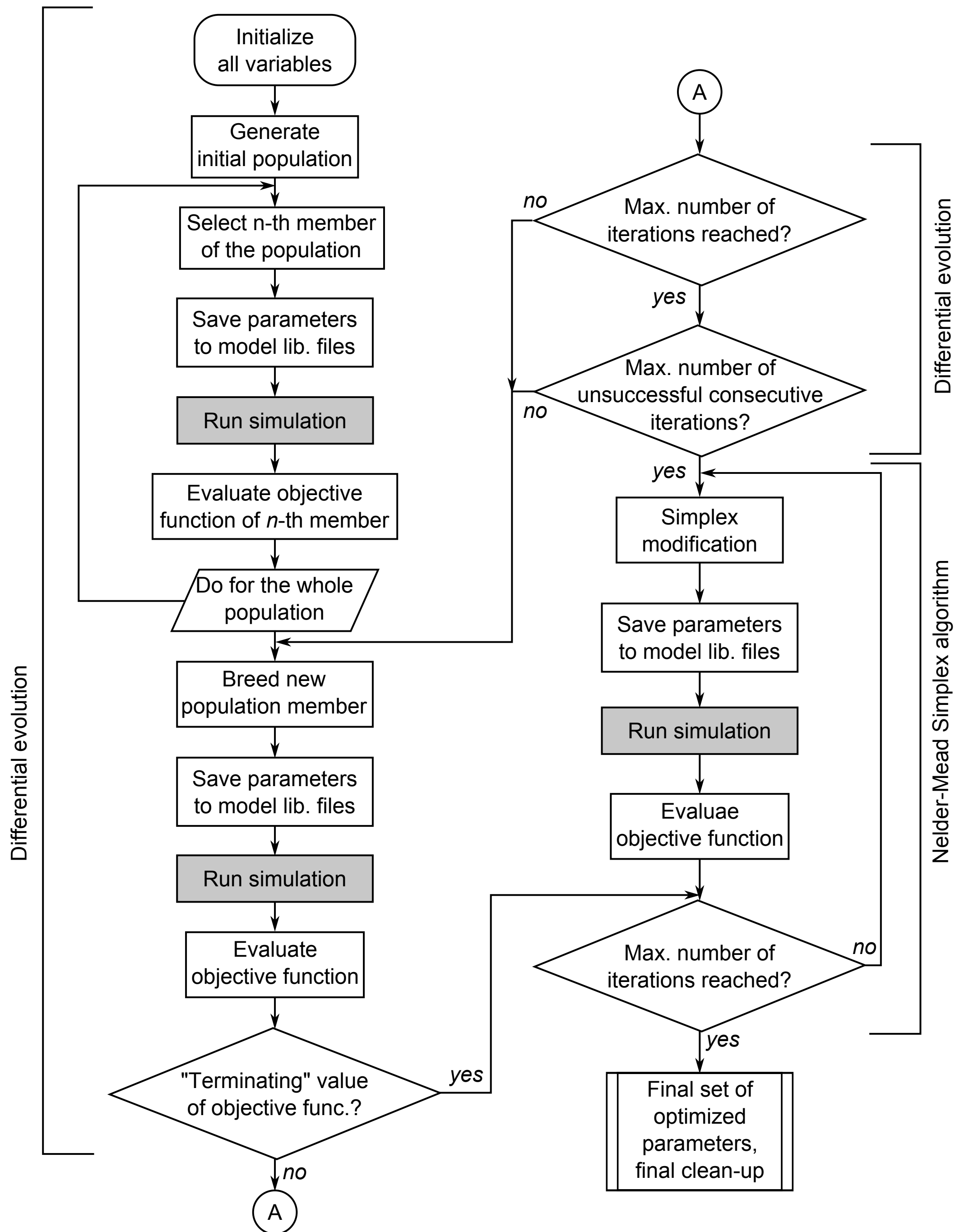

Figure 6.2: *Flow Diagram of Proposed Model Calibration Method*

forcing drain current and observing drain–source voltage for varying V_{GS}. The paper suggests using a special parametric analyzer HP4156 for this measurements. Additional measurements for avalanche voltage V_{av} and substrate resistance have to be performed. Extraction of M is performed in NMOST low-current region (prior to device trigger) where avalanche conduction dominates the drain current. The extraction is done by fitting slope $\ln\left(1-\frac{1}{M}\right)$ vs $\frac{1}{V_{DS}-V_{dsat}}$ yielding value of K_2. Parameter K_1 is then extracted using equation

$$k_1 = \exp\left(\frac{k_2}{V_{av}}\right). \tag{6.4}$$

Remaining parameters to be extracted are related to the parasitic bipolar transistor. Those are extracted by capturing drain and bulk current in high-current region of the measured NMOST I-V characteristics, already extracted substrate resistance, and avalanche multiplication factor M. It is obvious that all the device terminals shall be accessible for probing. Furthermore, large number of different measurements have to be performed to extract all the required parameters.

SCR macro-model and methodology for it's parameters extraction is presented in [2]. The macro-model structure corresponds to the one shown in Figure 6.3 and is formally identical to the one presented in this thesis in Chapter 3.2.

Focusing on a DC portion of the macro-model, the extraction flow is as follows: NPN bipolar transistor parameters I_S and β are extracted using parameteric analyzer measuring current through the n-well and p-well contacts with cathode grounded and anode floating. Similarly, the same parameters of parasitic PNP transistor are extracted measuring current through the p-well and n-well contacts having anode grounded and cathode floating. Remaining n-well and p-well resistors are used as fitting parameters for manual iterative calibration. Again, all terminals (even those that are not contacted in production SCR protection structures) must be accessible for probing.

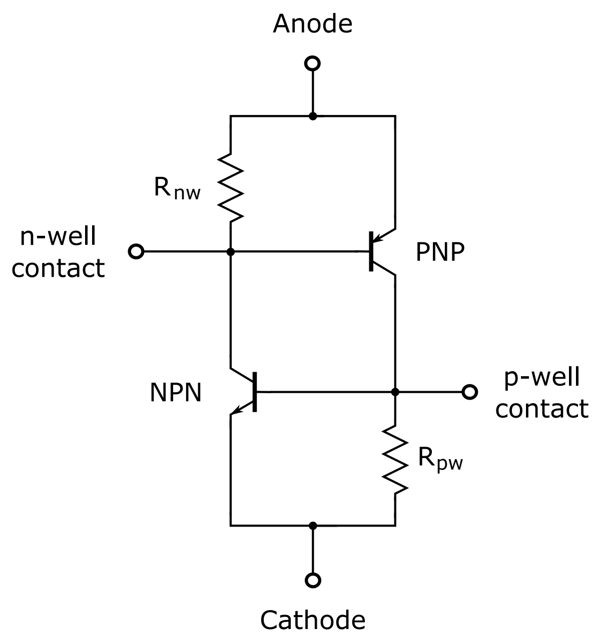

Figure 6.3: *Macro-Model of the SCR Device Presented in [2]*

CHAPTER 7

CALIBRATION METHOD BENCHMARKING METHODOLOGY

The benchmarking and evaluation of the proposed automated ESD macro-model calibration method was performed in four case studies, each by calibrating respective ESD macro-model on data of designed, fabricated and TLP or HBM characterized protection structure. Those case studies are all the protection structures presented in Chapter 3: *I/O ESD GGNMOST* protection – specifically its multi-finger variant, *silicon controlled rectifier* and its improved variants *modified lateral silicon controlled rectifier* and *low-voltage triggered silicon controlled rectifier*. Design and benchmarking flow will be summarized for each of the case studies in following paragraphs.

7.1 I/O ESD GGNMOST

I/O ESD protection devices based on standard thick gate oxide MOSFETs are probably the most often used ESD protection structures found in modern bulk CMOS integrated circuits. Its benefits and drawbacks were in detail described in Chapter 3. It is relatively simple to design and layout this type of ESD protection as principles and methodology for its optimum design are well documented [12]. The real challenge is always ESD design in unknown technology as ESD robustness of the final design is to some extent always dictated by the technology itself - doping profiles, usage of advanced techno-

logical steps like retrograde well implantation profile, halo implants, lightly-doped drain pockets, etc. Its one of the reasons why more GGNMOST-based structures with different dimensions were in the end designed as part of the multi-project IC developed at Department of Microelectronics at Czech Technical University in Prague (CTU) using 130nm CMOS technology. Figure 7.2a shows the complete un-packaged die (bonding pads around its perimeter are clearly visible along with metal tiling in the middle section, logo of fabrication company and of CTU are shown in Figure 7.2b. The other reason to design multiple structures with varying dimensions was to enable the author to develop scalable macro-models in the future. The multi-project IC consists of four independent sections with isolated power and ground rings and dedicated supply pins for each of the segments. The bulk substrate is the only shared part of the IC so the segments are physically separated to limit possible noise coupling. Top-level floorplan and output GDSII data were prepared in collaboration with other PhD. students at Department of Microelectronics at CTU. Author's section with the ESD structures is located in the south-west part of the pad-ring – pins 6 to 15 (see Figure 7.2c). Fabricated dies were packaged by a packaging house into suitable QFN40 packages – the package type and size were dictated by required silicon area that then has to fit into the package cavity and by required number of pins.

The design consisted of schematic synthesis where the structure dimensions were determined based on required ESD robustness and also compliance with fabrication ESD and latch-up design rules. As in this phase of the design no ESD models were available, next step was done without any kind of functional verification. Designed GGNMOST structures were placed into dissected pad cells each having its own bonding pad. The final design step was to verify compliance with fabrication rules called *design rule checks* (or often abbreviated as DRC) and automated comparison of schematic and layout designs called *layout versus schematic* (LVS). Prior to generating final output GDSII data, top-level was finalized (scribe lane was added to protect dies during wafer sawing, logos and identification hash were added, etc.) and DRC and LVS was performed on the final top-level design.

Table 7.1 summarizes a list of structures included in the fabricated IC with all important dimensions and comments where applicable. The one most suitable structure

selected as the test case for the method benchmarking is marked in the *Notes* column. Layout snapshot of the structure is shown in Figure 7.1.

The selected structure was characterized using custom in-house TLP measuring setup kindly provided by Dr. Vincent Mortet of Department of Functional Materials of Institute of Physics of the Czech Academy of Sciences. This setup is used for characterization of ion-doped diamond structures targeting for its semi-conducting properties.

Pin Number	**w_f (um)**	**L (um)**	**$L_{d,noSAL}$ (um)**	**N_f (–)**	**Notes**
6	40	1.20	4.0	8	Used for benchmarking
7	40	0.50	4.0	8	
8	40	0.13	4.0	8	
9	80	1.20	4.0	1	
10	–	–	–	–	Ground pin
11	80	0.50	4.0	1	
12	80	0.13	4.0	1	
13	80	1.20	2.5	1	
14	80	0.50	2.5	1	
15	80	0.13	2.5	1	

w_f – MOSFET finger width.
L – MOSFET channel length.
$L_{d,noSAL}$ – length of the un-salicided part of a MOSFET drain.
N_f – number of MOSFET fingers.

Table 7.1: *Summary Table of Designed GGNMOST Structures*

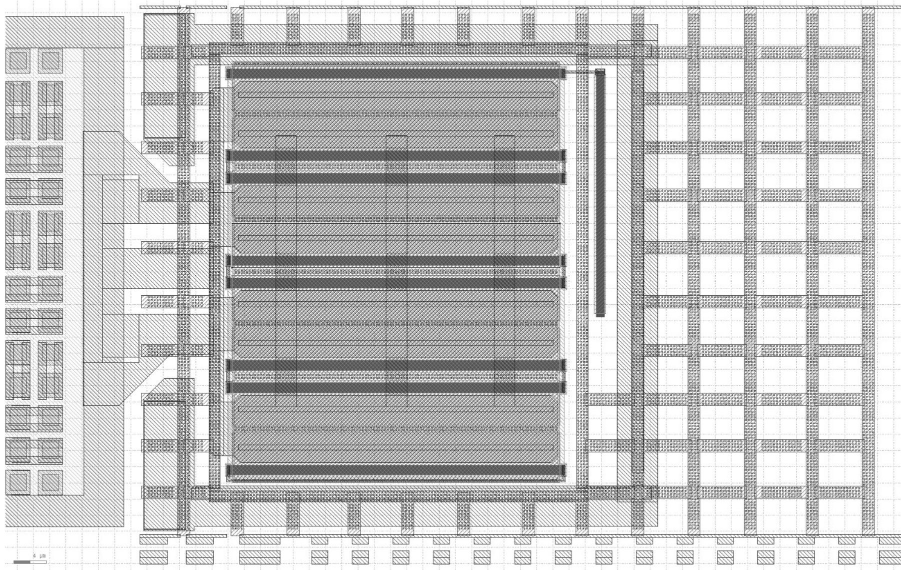

Figure 7.1: *Layout Snapshot of the Selected GGNMOST Protection Structure.*

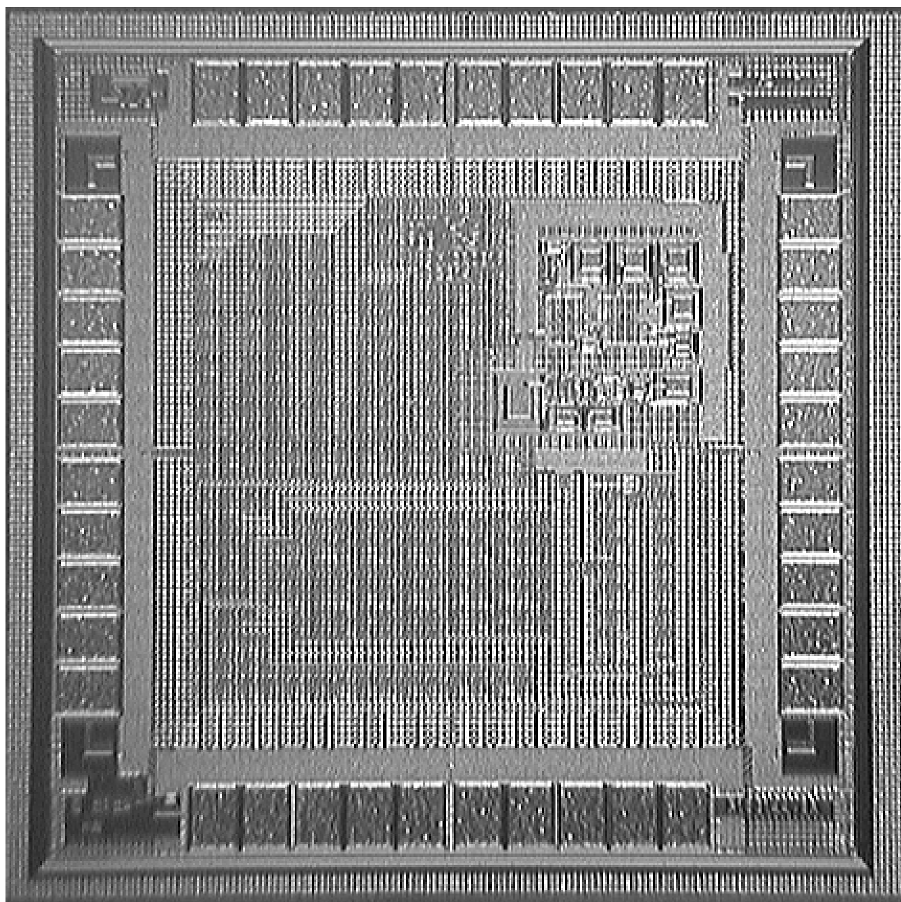

Figure 7.2a: *Micro-photograph of the Designed and Fabricated Multi-project IC Die.*

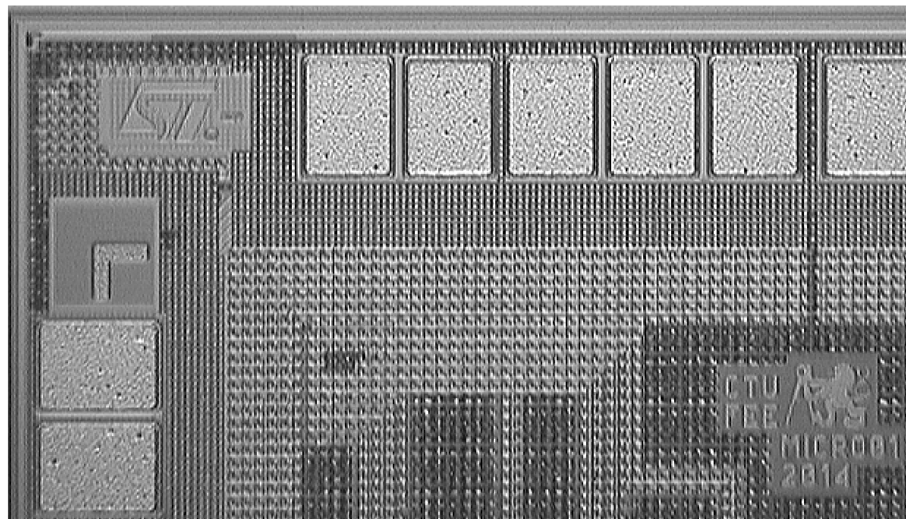

Figure 7.2b: *Micro-photograph of the North-West Part of the Die with ST and CTU Logos.*

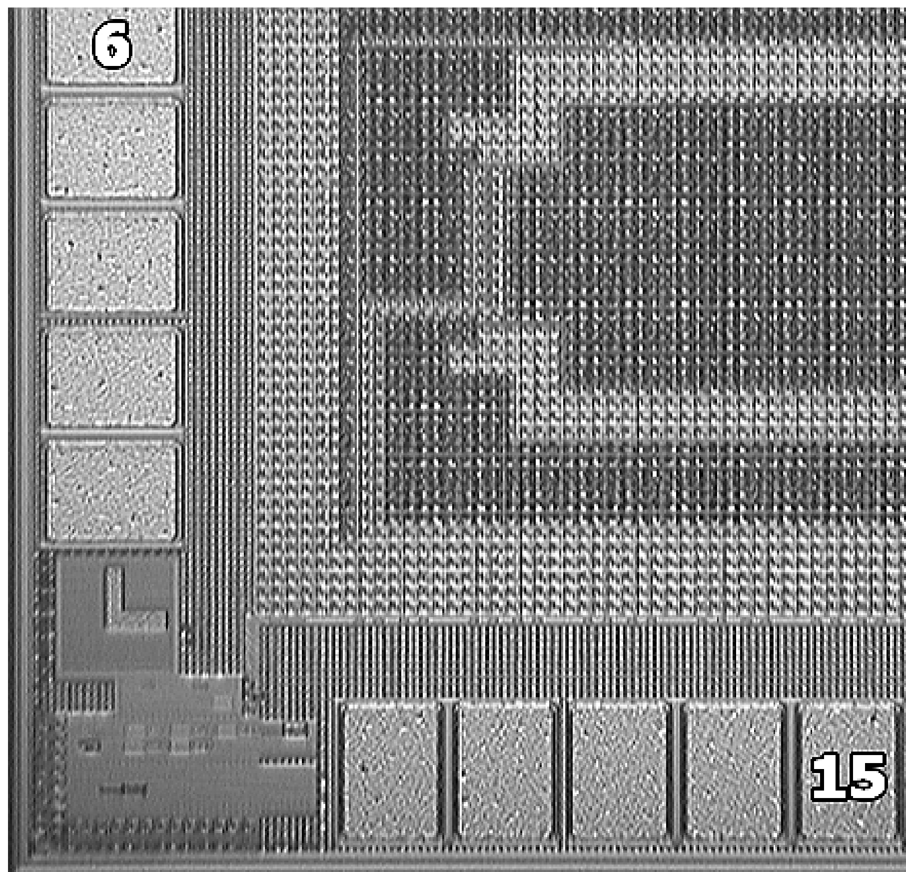

Figure 7.2c: *Detail of the South-west Pad-ring Section with ESD Protection Structures with Added Pin Numbers.*

7.2 SCR-Based Structures

Remaining SCR-based protection structures were designed as part of an internal I/O development program for author's employer using RF flavor of 180nm in-house low-power CMOS technology. Neither design procedures nor layout snapshots may be disclosed due to company internal processes regarding know-how protection.

Three modifications of silicon controlled rectifier were designed in numerous configurations with different sizing, spacings between structure sections, etc.:

- Silicon controlled rectifier
- Modified lateral silicon controlled rectifier
- Low-voltage triggered silicon controlled rectifier

Characterization was performed by Oryx Intruments Corporation ICMS–700 HBM/MM tester as part of human body model and machine model characterizations based on procedure described in Chapter 4.1.

Final step of benchmarking of each test-case device was to check macro-model convergence properties. To verify that no convergence problems occur if a device is instantiated in a larger circuit, complete digital I/O circuit equipped with both input and output signal paths was designed in both CMOS technologies used. The input signal path consists of a Schmitt trigger circuit, I/O-to-core voltage domain digital level-shifter, and digital buffers; output path of a core-to-I/O voltage domain digital level-shifter, open-drain NMOST driving circuit with selectable high-impedance state and a buffer chain feeding the open-drain NMOST. Core logic is simulated by a combinational logic of approx. 200 gates. 4 kV HBM transient pulse is used as a stimulus of the I/O circuit – which is fully powered and operational – and is applied on the I/O input (pad) of the digital I/O circuit. Transient response of each case study macro-model instantiated in such an I/O circuit to the HBM pulse will then be plotted. Scheme is shown in Figure 7.3.

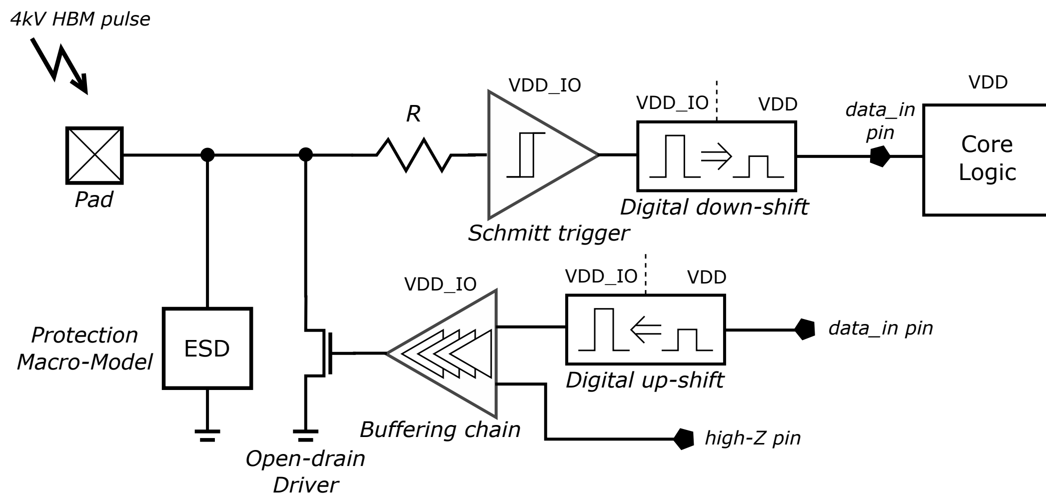

Figure 7.3: *Scheme of the Digital I/O Circuit for Demonstrating Correct Convergence Properties of Calibrated Macro-models.*

7.3 Equipment and Software Setup

Equipment used for benchmarking was supplied by Department of Microelectronics of Czech Technical University in Prague. The benchmarking methods were executed in single-thread mode to limit load to the servers and utilization of simulator licenses as those are shared among all the students. Run times are thus longer than they may be when parallel execution would be enabled.

Software versions used for benchmarking were following: Cadence Spectre 14.1.0 988 ISR20, Octave 3.4.3, base operating system CentOS 6.10.

The optimization algorithms were set as follows:

- Differential evolution
  - Population size $NP = 1000$
  - Crossover probability factor $CR = 0.9$
  - Weight factor $F = 0.68$
  - Maximum number of iterations = 2000
  - Termination value of the objective function $f_{\mathrm{obj}}^{\mathrm{TERM}} = 10$

- Nelder-Mead simplex algorithm
  - Relative simplex size = 10^{-3}
  - Maximum number of iterations = 2000
  - Termination value of the objective function $f_{\text{obj}}^{\text{TERM}} = 10$

CHAPTER 8

RESULTS OF CALIBRATION METHOD BENCHMARKING

Calibration results of all the case-studies follows. All the macro-models were characterized by the same hardware and software setup and using the same calibration method setup. Summary tables with additional setup of the method, final values of calibrated macro-model parameters and comparison of TLP or HBM-extracted and macro-model I-V characteristics regions along with plot of both I-V characteristics and transient response to 4 kV HBM pulse is presented for each case-study.

8.1 I/O ESD GGNMOST

During the I/O ESD GGNMOST macro-model calibration, trigger, snapback and R_{on} regions were accented by penalization factor whose values are summarized in Table 8.1a. Resulting I-V characteristics of TLP measured structure and the macro-model and their absolute error is shown in Figures 8.1a and 8.1b. Transient response of the macro-model instantiated in I/O circuit as described in Chapter 7 is plotted in Figure 8.1c. Resulting values of calibrated parameters of the NMOST macro-model are recapitulated in Table 8.1b. Comparison of important I-V regions of the macro-model are shown in Table 8.1c.

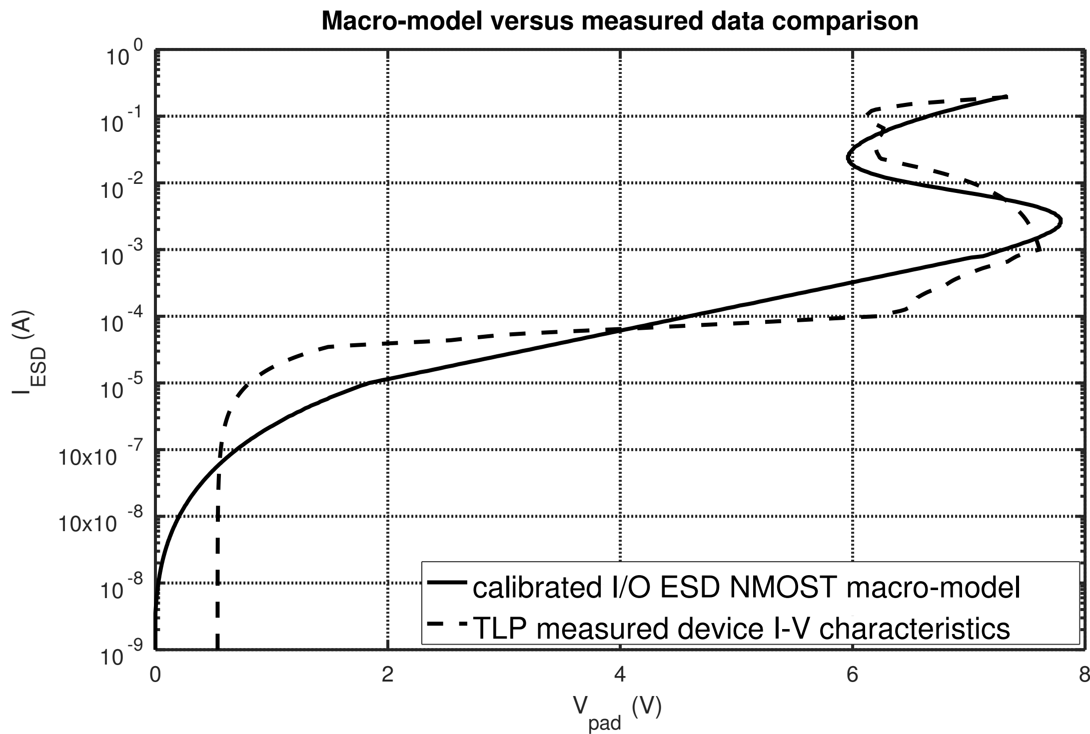

Figure 8.1a: *Comparison of GGNMOST TLP and Macro-model I-V Characteristics.*

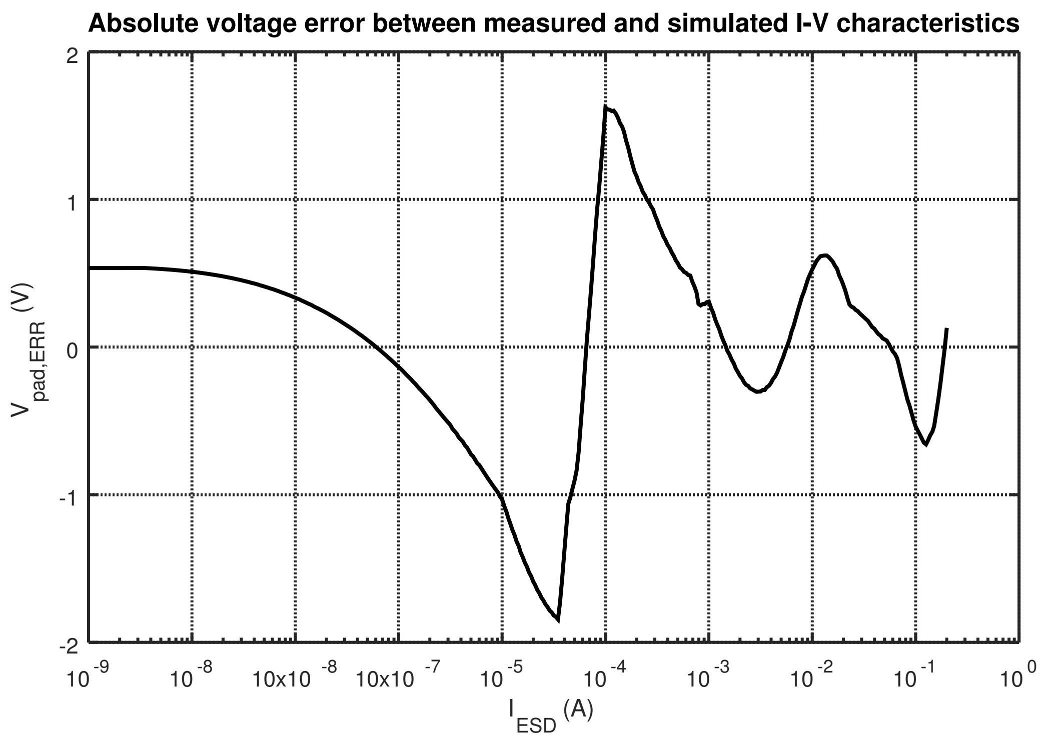

Figure 8.1b: *Absolute Error of GGNMOST TLP and Macro-model I-V Characteristics.*

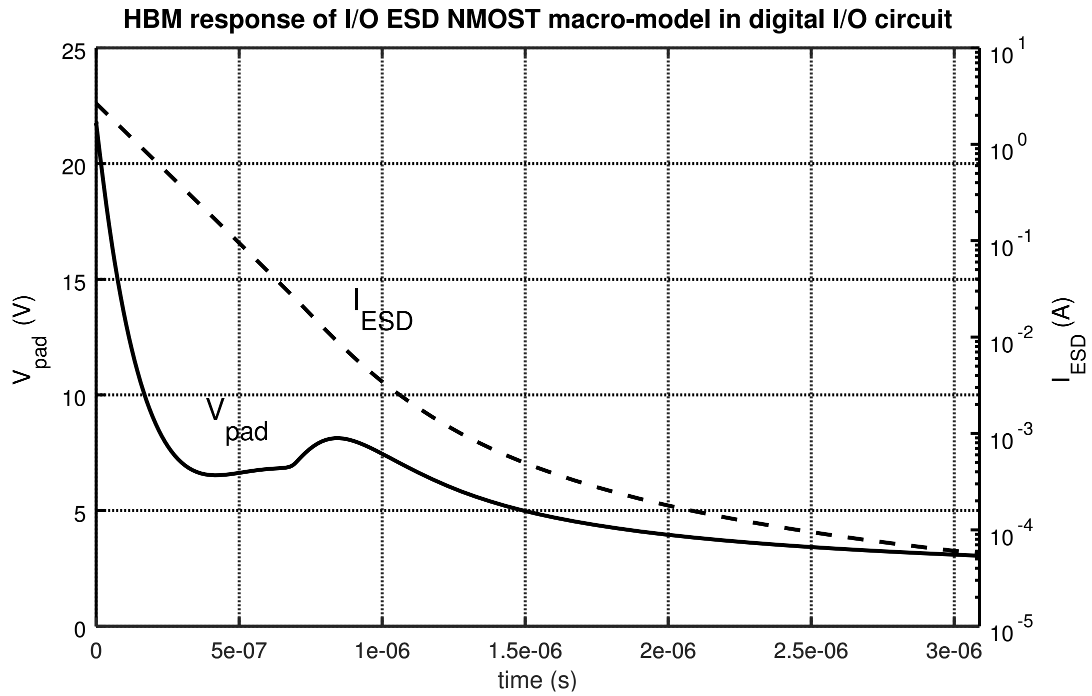

Figure 8.1c: *HBM Transient Response of GGNMOST Macro-model.*

I-V Region	Range of DUT Current	Penalty Factor
V_{t1} Region	0.5 – 5.0 mA	20
V_{h} Region	30.0 – 300.0 mA	20
R_{on} Region	900 – 1000 mA	15

Table 8.1a: *GGNMOST I-V Characteristics Penalization Setup*

Parameter	Value
VBIC NPN Parameters	
AVC1	$2.3966 \cdot 10^{10}$
AVC2	9.5626
IBCI	$4.7208 \cdot 10^{-14}$
IBCN	$5.2343 \cdot 10^{-15}$
IBEN	$6.1408 \cdot 10^{-16}$
IS	$1.5867 \cdot 10^{-19}$
NEN	1.1482
NF	1.9593
RBI	5.7736
RBX	5.7976
RCI	0.0012186
RCX	0.0045265
RE	0.69236
Core NMOST Parameters	
ALPHA0	1.8462
BETA0	17.771
Substrate Resistance Parameters	
RPW	1892.1

Table 8.1b: *Calibrated Parameters of GGNMOST Macro-model.*

I-V Identity	TLP Measurement	Macro-model
V_{t1}	7.03 V	7.79 V
I_{t1}	10.10 mA	2.89 mA
V_{h}	6.20 V	5.96 V
I_{h}	38.02 mA	28.80 mA
R_{on}	12.60 Ω	8.00 Ω

Table 8.1c: *Comparison of Important Regions of the GGNMOST Macro-model and TLP Measured I-V Characteristics.*

8.2 Silicon Controlled Rectifier

During the ESD SCR macro-model calibration, trigger, snapback and R_{on} regions were accented by penalization factor whose values are summarized in Table 8.2a. Resulting I-V characteristics of HBM measured structure and the macro-model and their absolute error is shown in Figures 8.2a and 8.2b. Transient response of the macro-model instantiated in I/O circuit is plotted in Figure 8.2c. Resulting values of calibrated parameters of the SCR macro-model are recapitulated in Table 8.2b. Comparison of important I-V regions of the macro-model are shown in Table 8.2c.

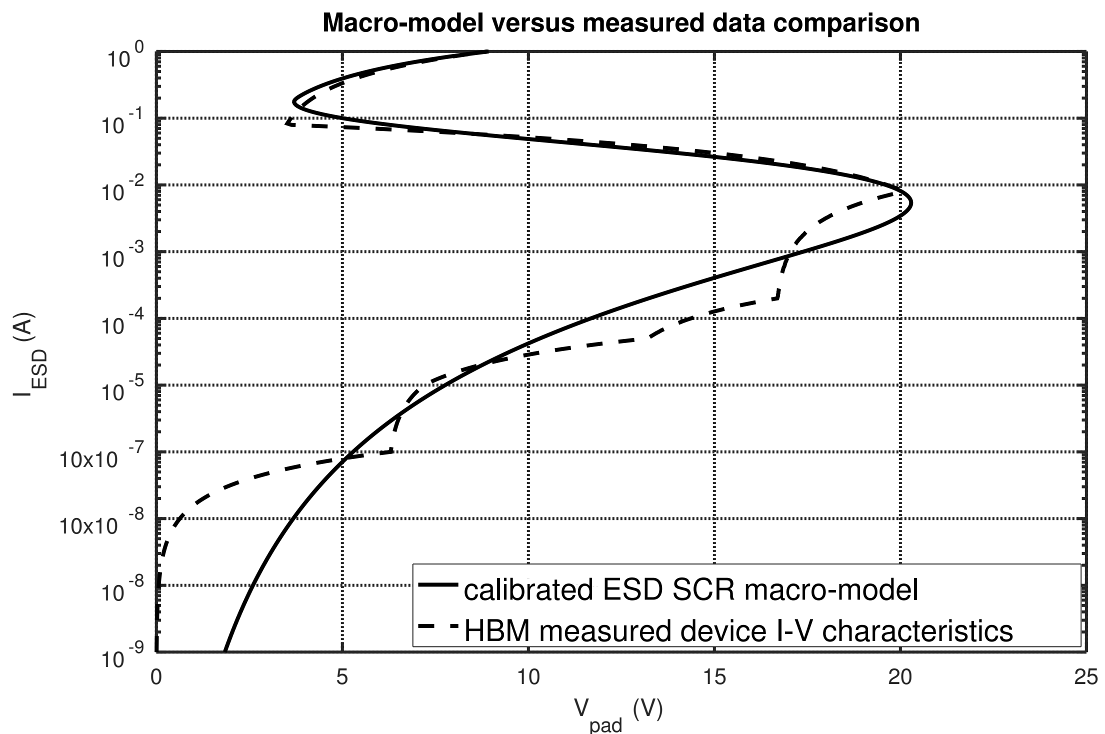

Figure 8.2a: *Comparison of SCR HBM and Macro-model I-V Characteristics.*

I-V Region	Range of DUT Current	Penalty Factor
V_{t1} Region	0.17 – 10.0 mA	20
V_{h} Region	50.0 – 350.0 mA	20
R_{on} Region	900 – 1000 mA	15

Table 8.2a: *SCR I-V Characteristics Penalization Setup*

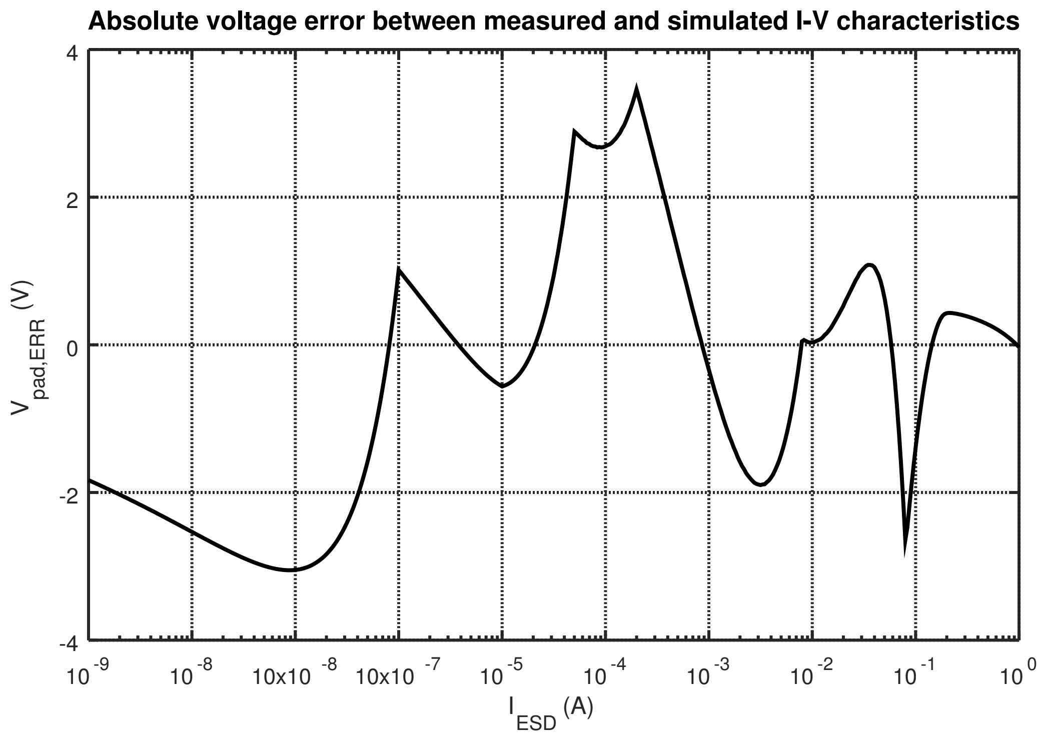

Figure 8.2b: *Absolute Error of SCR HBM and Macro-model I-V Characteristics.*

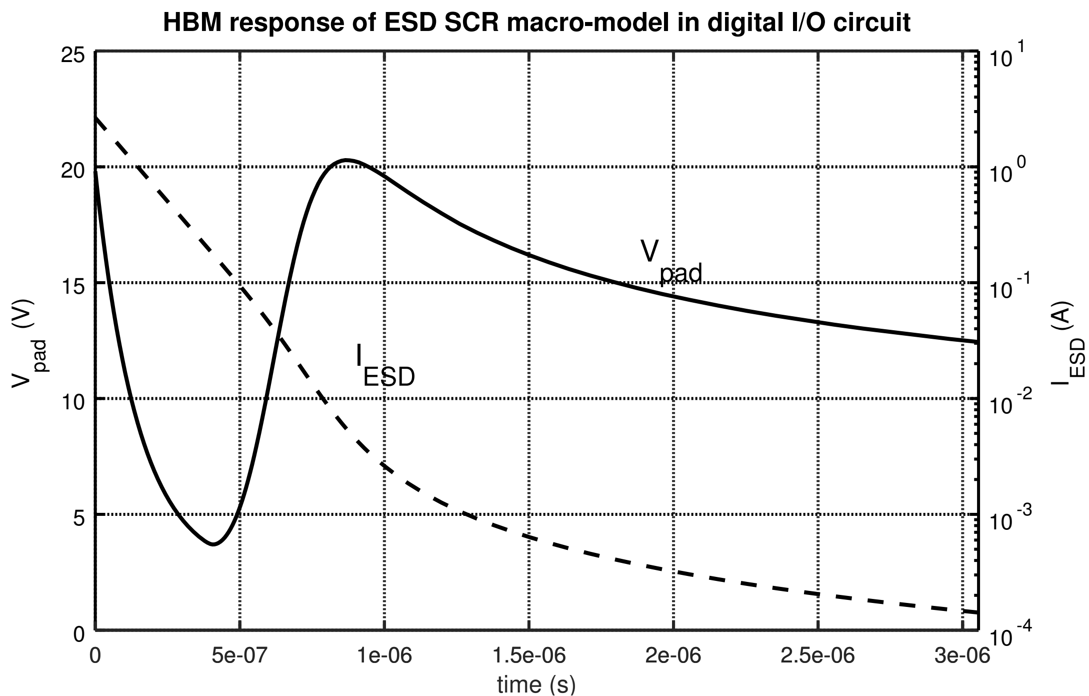

Figure 8.2c: *HBM Transient Response of SCR Macro-model.*

Parameter	Value
VBIC NPN Parameters	
AVC1	$1.5473 \cdot 10^{14}$
AVC2	29.839
IBCI	$3.9732 \cdot 10^{-17}$
IBCN	$2.5866 \cdot 10^{-18}$
IBEN	$7.4194 \cdot 10^{-15}$
IS	$1.0105 \cdot 10^{-16}$
NEN	8.8429
NF	2.8066
RBI	1.2247
RBX	0.010988
RCI	0.98519
RCX	0.84084
RE	0.22799
SGP PNP Parameters	
BF	16.03
NF	0.31804
BR	7.8986
NR	5.1491
ISE	$2.0283 \cdot 10^{-16}$
NE	0.97472
ISC	$3.437 \cdot 10^{-16}$
NC	2.4378
VAF	98.591
VAR	8.7863
IKF	0.13149
IKR	$9.114e-05$
RB	1.0284
RC	0.66461
RE	9.8136
Substrate Resistance Parameters	
RNW	8573.0
RPW	8630.4

Table 8.2b: *Calibrated Parameters of SCR Macro-model.*

I-V Identity	HBM Measurement	Macro-model
V_{t1}	20.08 V	20.03 V
I_{t1}	7.94 mA	5.50 mA
V_{h}	3.52 V	3.70 V
I_{h}	83.18 mA	173.40 mA
R_{on}	5.87 Ω	6.33 Ω

Table 8.2c: *Comparison of Important Regions of the SCR Macro-model and HBM Measured I-V Characteristics.*

8.3 MLSCR

During the ESD MLSCR macro-model calibration, trigger, snapback and R_{on} regions were accented by penalization factor whose values are summarized in Table 8.3a. Resulting I-V characteristics of HBM measured structure and the macro-model and their absolute error is shown in Figures 8.3a and 8.3b. Transient response of the macro-model instantiated in I/O circuit is plotted in Figure 8.3c. Resulting values of calibrated parameters of the MLSCR macro-model are recapitulated in Table 8.3b. Comparison of important I-V regions of the macro-model are shown in Table 8.3c.

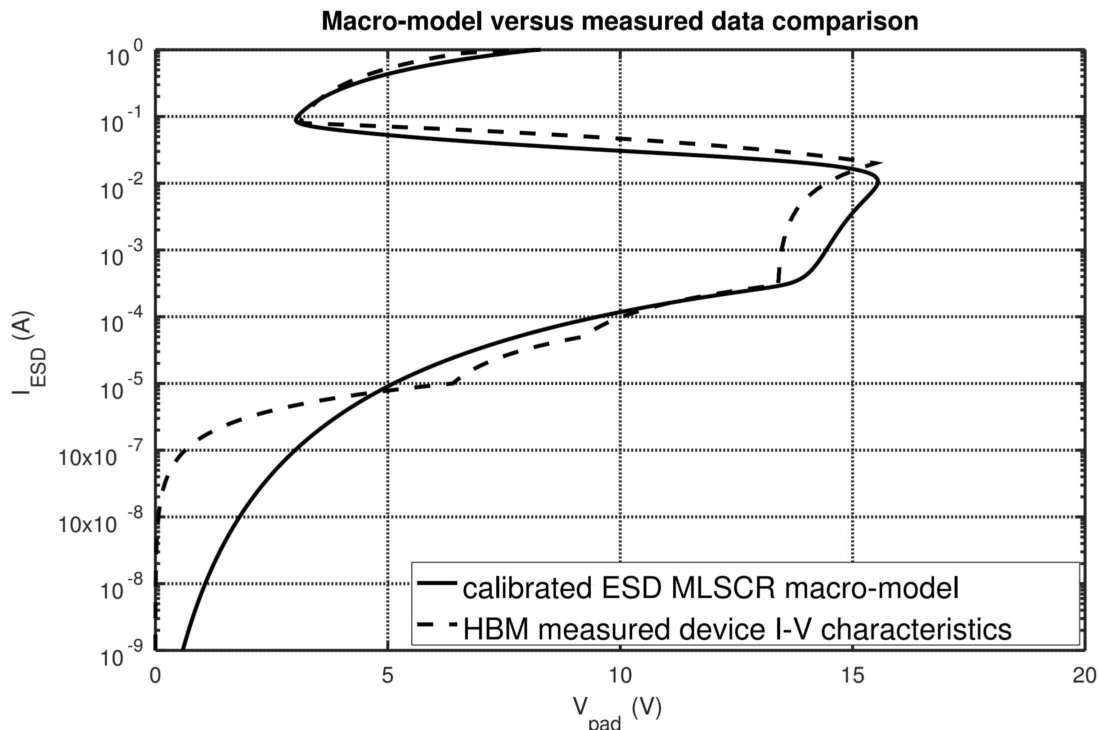

Figure 8.3a: *Comparison of MLSCR HBM and Macro-model I-V Characteristics.*

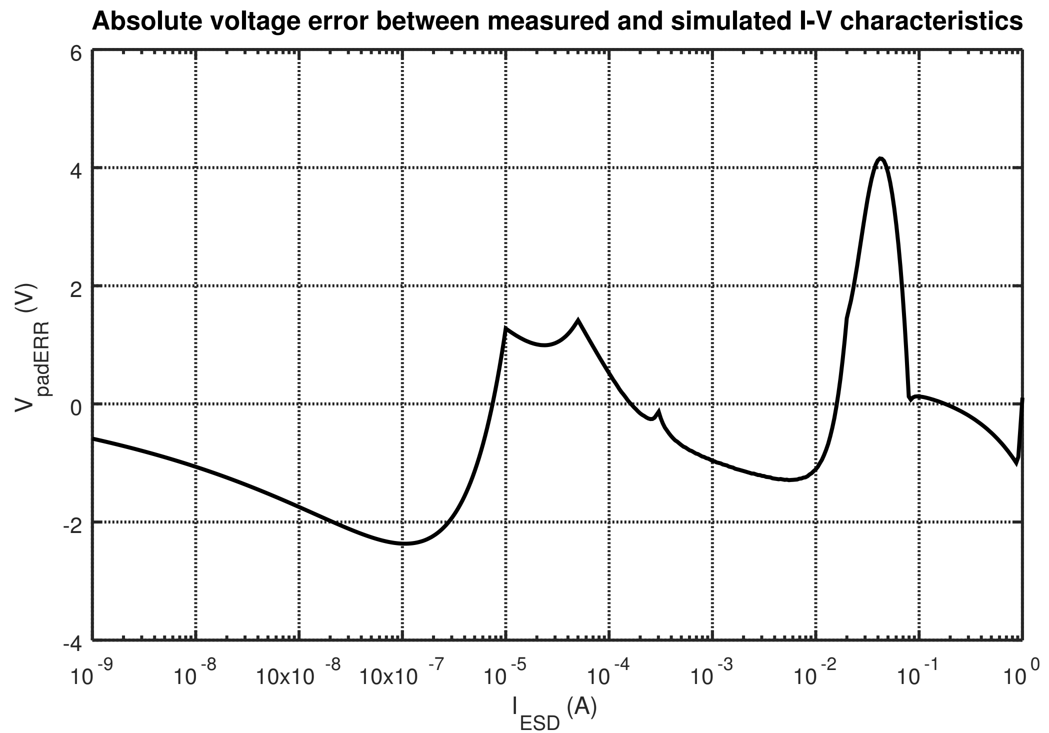

Figure 8.3b: *Absolute Error of MLSCR HBM and Macro-model I-V Characteristics.*

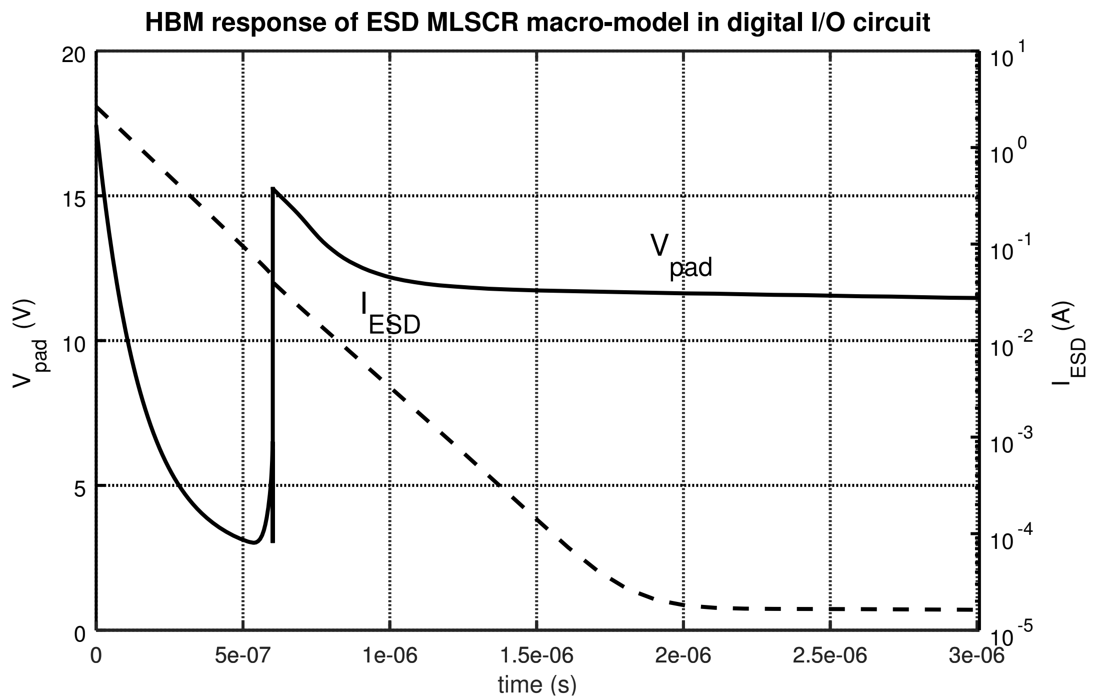

Figure 8.3c: *HBM Transient Response of MLSCR Macro-model.*

I-V Region	Range of DUT Current	Penalty Factor
V_{t1} Region	1.6 – 13.0 mA	20
V_h Region	70.0 – 200.0 mA	20
R_{on} Region	900 – 1000 mA	15

Table 8.3a: *MLSCR I-V Characteristics Penalization Setup*

8.4 LVTSCR

During the ESD LVTSCR macro-model calibration, trigger, snapback and R_{on} regions were accented by penalization factor whose values are summarized in Table 8.4a. Resulting I-V characteristics of HBM measured structure and the macro-model and their absolute error is shown in Figures 8.4a and 8.4b. Transient response of the macro-model instantiated in I/O circuit is plotted in Figure 8.4c. Resulting values of calibrated parameters of the LVTSCR macro-model are recapitulated in Table 8.4b. Comparison of important I-V regions of the macro-model are shown in Table 8.4c.

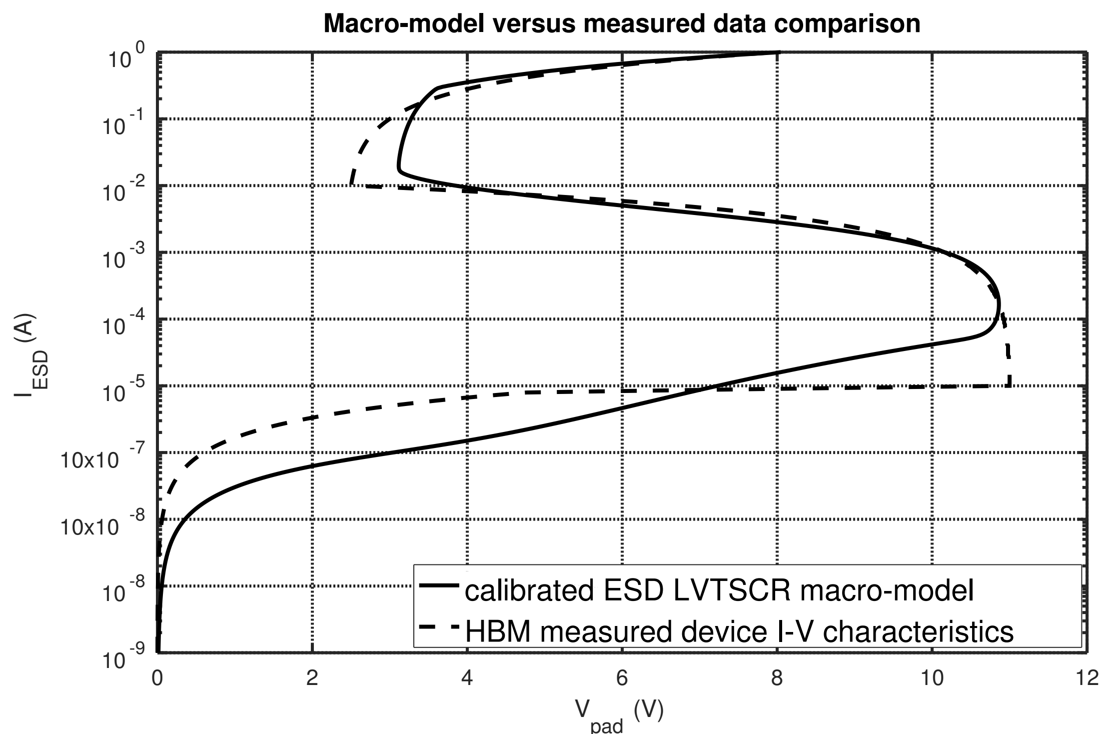

Figure 8.4a: *Comparison of LVTSCR HBM and Macro-model I-V Characteristics.*

Parameter	Value
VBIC NPN Parameters	
AVC1	$4.2339 \cdot 10^{11}$
AVC2	19.556
IBCI	$8.5062 \cdot 10^{-15}$
IBCN	$4.124 \cdot 10^{-15}$
IBEN	$1.5472 \cdot 10^{-15}$
IS	$3.4741 \cdot 10^{-17}$
NEN	4.0073
NF	1.3068
RBI	11.374
RBX	1.6584
RCI	0.18297
RCX	2.5145
RE	1.6958
SGP PNP Parameters	
BF	14.984
NF	2.22
BR	1.3776
NR	7.776
ISE	$4.1522 \cdot 10^{-16}$
NE	9.1814
ISC	$5.3812 \cdot 10^{-16}$
NC	2.7272
VAF	2.4825
VAR	97.093
IKF	0.07007
IKR	0.083269
RB	1.5079
RC	27.423
RE	0.41075
Substrate Resistance Parameters	
RNW	8257.6
RPW	9716.4

Table 8.3b: *Calibrated Parameters of MLSCR Macro-model.*

I-V Identity	HBM Measurement	Macro-model
V_{t1}	15.49 V	15.54 V
I_{t1}	19.95 mA	10.47 mA
V_{h}	3.11 V	3.02 V
I_{h}	83.18 mA	87.10 mA
R_{on}	5.66 Ω	5.67 Ω

Table 8.3c: *Comparison of Important Regions of the MLSCR Macro-model and HBM Measured I-V Characteristics.*

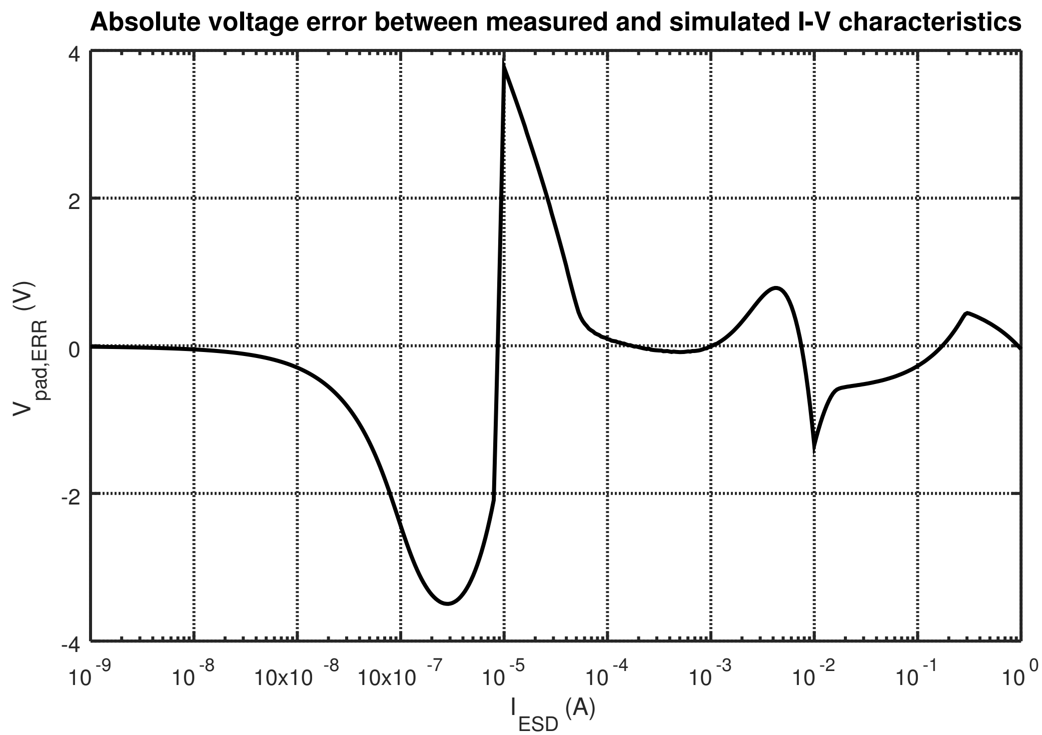

Figure 8.4b: *Absolute Error of LVTSCR HBM and Macro-model I-V Characteristics.*

I-V Region	Range of DUT Current	Penalty Factor
V_{t1} Region	0.01 – 0.5 mA	20
V_{h} Region	11.0 – 100.0 mA	20
R_{on} Region	900 – 1000 mA	15

Table 8.4a: *LVTSCR I-V Characteristics Penalization Setup*

Parameter	Value
VBIC NPN Parameters	
AVC1	$1.7161 \cdot 10^{14}$
AVC2	29.705
IBCI	$8.9319 \cdot 10^{-17}$
IBCN	$5.7653 \cdot 10^{-17}$
IBEN	$2.2301 \cdot 10^{-15}$
IS	$4.8654 \cdot 10^{-17}$
NEN	3.943
NF	3.3629
RBI	4.7248
RBX	2.0297
RCI	98.196
RCX	0.43729
RE	0.27754
Core NMOST Parameters	
ALPHA0	2.1645
BETA0	34.735
Substrate Resistance Parameters	
RNW	11934
RPW	8694.3

Table 8.4b: *Calibrated Parameters of LVTSCR Macro-model.*

I-V Identity	HBM Measurement	Macro-model
V_{t1}	11.00 V	10.86 V
I_{t1}	0.01 mA	0.16 mA
V_{h}	2.51 V	3.11 V
I_{h}	11.12 mA	21.9 mA
R_{on}	5.56 Ω	6.27 Ω

Table 8.4c: *Comparison of Important Regions of the LVTSCR Macro-model and HBM Measured I-V Characteristics.*

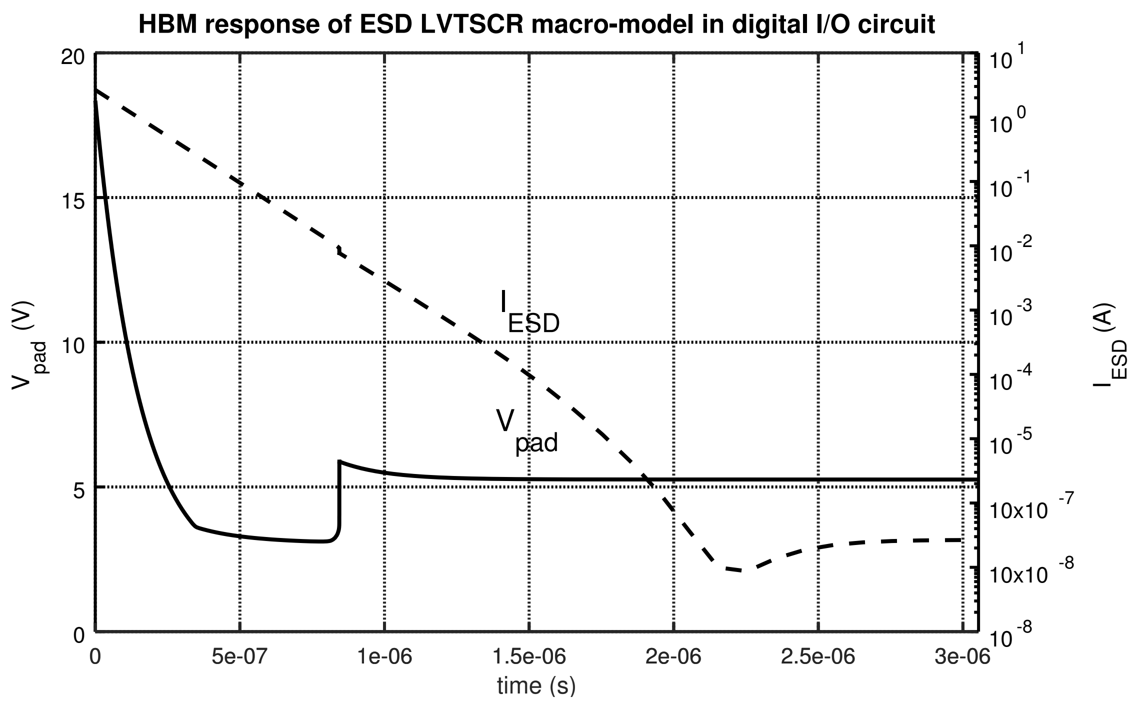

Figure 8.4c: *HBM Transient Response of LVTSCR Macro-model.*

CHAPTER 9

CONCLUSIONS

Electrostatic discharge has presented serious problem for integrated circuits reliability and lifetime since the first steps on a field of high integration. Energies that may be transferred during this relatively short event can completely destroy sensitive analog or digital blocks within an IC if this phenomenon is not taken into account during every phase of the design.

To increase IC robustness against ESD events, full-chip protection design has to be carefully integrated. Introduction of special models that are able to describe behavior of a protection device during ESD event may substantially decrease number of iterations necessary for full-chip ESD protection system design to be refined. To calibrate these ESD models, number of specific measurements has to be performed, thus increasing demand on dedicated specialists and total characterization time. In most of the cases, the measurements require all terminals of a protection device to be connected to external pads which increases systematic error of the measurements as all those pads shall be always protected by ESD protection devices that add parasitics into the measured device terminals. The calibration process is then an iterative work of fine-tuning of all the fitting parameters.

Proposed automated ESD macro-model calibration method simplifies this task by requiring only single measurement of IC characteristics of a protection structure and by utilizing robust optimization algorithms as a driving force instead of an engineer.

Benchmarking results were presented along with transient HBM responses of the structures that proved excellent convergence properties of calibrated macro-models. Precision of performed calibrations is well within required limits for full mixed-signal IC system verification with respect to ESD performance. One of the limitations of current implementation of used ESD macro-models is absence of second break-down modeling that would enable designers to predict ESD robustness of scalable macro-models (i.e., macro-models with adjustable dimensions). But as this complex feature would require cross-domain simulation approach interlinking circuit and TCAD simulators having enormous impact on performance of the calibration process and as the scalability is not required for ESD design because only tested and characterized structures are used, this was omitted in the research.

9.1 Contribution

The goal of this research was to develop an automated ESD macro-model calibration method requiring as small number of measurements to be performed and as low effort as possible without sacrificing macro-model performance. Simplifying characterization process in such a way may significantly increase efficiency of development of PDKs able to model behavior of specific structures during ESD events – especially if human resources are limited.

1. The author developed new approach to calibrate ESD macro-models requiring minimal resources. Research on effective optimization algorithm was done by the author yielding DE as the most fitting one for the required task. Additional improvement was later achieved by the author by introduction of NMSA to the final stage of the optimization flow where DE loses its efficiency. Proposed combination of DE and NMSA was published before in [7] but their implementation is different than the author's and is not suitable for presented method. Method efficiency and versatility were tested by four case studies – GGNMOST, SCR, MLSCR, and LVTSCR which were designed and fabricated and finally measured by the author.

2. Contribution to ESD modeling was done by the author by introduction of 4-terminal VBIC bipolar model instead of 3-terminal variant with additional SGP PNP bipolar model in case of LVTSCR ESD protection macro-model. This improvement allowed to limit number of fitting parameters to a half of the original 32 without significantly affecting macro-model precision as proved by calibrated macro-model in Chapter 8. Additionally, the author made a study to asses sensitivity of important regions of I-V characteristics of ESD NMOST macro-model to parameters of all the macro-model sub-models (e.g., core NMOST, VBIC NPN bipolar transistor, and substrate resistance models). This is presented in Chapter 3.

3. The final contribution of the author is limiting number of required measurements for a macro-model calibration to a single TLP measurement which is then used as a calibration template. This contribution significantly simplifies the calibration procedure, especially if fully automated TLP setup is available. This alleviates the need for ESD specialist to waste time by manually measuring set of characteristics that are otherwise necessary (e.g., [8, 2]). Additionally, it enables to characterize ESD protections structures as they are implemented in final designs, i.e., without additional terminals used only for the characterization.

The author did not find any other paper dealing with automation of ESD macro-model calibration thus comparison against achievements of similar work was not possible.

The research results were presented at several conferences and in two journals one of them impacted [29], the other reviewed [30]. List of all the related and unrelated author's publications may be found in Appendix A.

9.2 Suggested Future Development

Performed benchmarking proved that presented method is fully capable to calibrate various ESD macro-models using both TLP and HBM-measured I-V characteristics. Possible improvements to the method flow can be divided into upgrades to the method itself and into upgrades to the ESD macro-models.

9.2.1 Improvements to the Calibration Method

Introduction of Impedance Characterization

Some of the macro-models presented in the thesis does not take advantage of using fully calibrated core model contained in a PDK of a technology used. Those may exhibit large deviation from real behavior when simulated by other than DC simulation. This arise from the fact that TLP measurement approach constructs device's I-V characteristics in quasi-static part of the transient impulse thus obscuring high-frequency properties of a protection device. This may be improved by additional characterization of impedance of the protection in reasonable range of frequencies and by incorporating this impedance into a macro-model of the protection device. The calibration method would then perform two simulations per one population member and use so called *multi-objective function* constructed from criteria based on DC I-V characteristics and frequency response.

Using Simulation Results of TCAD instead of TLP

Other possibility to obtain I-V characteristics of a protection structure instead of the TLP approach may be via use of TCAD. If a modeling deck of used technology is available for a TCAD tool, ESD designer may take advantage of its thermal and other advanced models. The need for fabrication of functional samples of protection structures would then be eliminated and design process would be further simplified and sped up.

9.2.2 Improvements to the ESD Macro-models

Scalable Macro-models

Macro-model scalability is not required during implementation of specific system-level ESD protection design. It is only useful during development of new structures, specifically having structure type fixed (e.g., selecting GGNMOST) and optimizing structure dimensions to achieve required ESD and e.g. high-frequency performance. Having scalable macro-model would make this task much more efficient. Unfortunately, scalability in case of ESD macro-model would require additional research on sensitivity of dimensions to macro-model parameters which is nontrivial task and requires full set of functional samples to be manufactured.

Implement Second-breakdown Model

As already mentioned, second-breakdown model is not available in current ESD macro-models presented in this thesis. They are only equipped with Verilog-A module that senses current flowing through the stressed pin and that asserts error message in case that the current rises above set threshold (I_{t2} point on its I-V characteristic) notifying designer that at these circumstances the protection probably suffered catastrophic failure. This value can be relatively easily obtained by HBM measurement as described in Chapter 4.1. This value is of course not easily scalable with dimensions of the protection device as thermal properties are not directly proportional during scaling and advanced effects such as non-uniform conduction within a finger starts to affect robustness as a technological node is being scaled down below 90 nm. Development of comprehensive second break-down model would possibly require introduction of TCAD simulator either inter-linked with standard circuit one providing information about temperature gradients within a structure or as a tool for development of some novel model. In both cases, used technology would have to have TCAD model deck available.

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APPENDICES

APPENDIX A: List of Author's Publications

A.1 Publications Related to the Topic of This Work

Publications in Impacted Journals

NAPRAVNIK T., JAKOVENKO J. An automated ESD model characterization method. *Radioengineering*, vol. 28, no. 3, September 2018, **Co-authorship: 90 %**

Publications in Reviewed Journals

NAPRAVNIK T., JAKOVENKO J. ESD MOSFET model calibration by differential evolutionary optimization algorithm. *ElectroScope*, no. 6, 2012, ISSN 1802-4564, **Co-authorship: 60 %**

Publications Excerpted by WoS

NAPRAVNIK T., KOTE V., MOLATA V., JAKOVENKO J. Differential evolutionary optimization algorithm applied to ESD MOSFET model fitting problem. *2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, April 2012, p. 155–158, **Co-authorship: 70 %**

NAPRAVNIK T., ZISKA P., JAKOVENKO J. Novel model calibration method based on differential evolution used for SCR model fitting. *2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, April 2013, p. 297–298, **Co-authorship: 50 %**

Other Publications

NAPRAVNIK T., KOTE V., MOLATA V., JAKOVENKO J. Utilization of differential evolutionary optimization algorithm for ESD MOSFET model fitting. *Proceedings of Electronic Devices and Systems EDS 2012. Electronic Devices and Systems 2012,*

Brno, 2012-06-28/2012-06-29, June 2012, p. 33–38, ISSN 978-80-214-4539-0, **Co-authorship: 70 %**

NAPRAVNIK T., ZISKA P., JAKOVENKO J. ESD LVTSCR model calibration by differential evolutionary optimization algorithm. *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*, February 2013, **Co-authorship: 50 %**

NAPRAVNIK T., ZISKA P., JAKOVENKO J. Automated model calibration flow based on differential evolution used for ESD MVTSCR model fitting. *Proceedings - Electronic Devices and Systems - EDS '13. Electronic Devices and Systems, Brno, 2013-06-26/2013-06-27*, June 2013, ISSN 978-80-214-4754-7, **Co-authorship: 50 %**

Functional Samples

NAPRAVNIK T., KOTE V., VACULA P., JAKOVENKO J. Single-finger and multi-finger MOST structures for ESD characterization and model development. Functional sample, 2014, **Co-authorship: 75 %**

A.2 Publications Unrelated to the Topic of This Work

Other Publications

KOTE V., NAPRAVNIK T., MOLATA V., JAKOVENKO J. Structure, modeling and realization of true random number generator with analog noise amplification. *Proceedings of Electronic Devices and Systems EDS 2012. Electronic Devices and Systems 2012, Brno, 2012-06-28/2012-06-29*, June 2012, p. 145–150, ISSN 978-80-214-4539-0, **Co-authorship: 10 %**

MOLATA V., KOTE V., NAPRAVNIK T., JAKOVENKO J. Capacitor-less LDO regulator in CMOS technology. *Proceedings of Electronic Devices and Systems EDS 2012. Electronic Devices and Systems 2012, Brno, 2012-06-28/2012-06-29*, June 2012, p. 54–59, ISSN 978-80-214-4539-0, **Co-authorship: 10 %**

MOLATA V., KOTE V., NAPRAVNIK T., JAKOVENKO J. Capacitor-less LDO regulator with NMOS power transistor. *Proceedings - Electronic Devices and Systems - EDS '13. Electronic Devices and Systems, Brno, 2013-06-26/2013-06-27*, June 2013, p. 50–55, ISSN 978-80-214-4754-7, **Co-authorship: 5 %**