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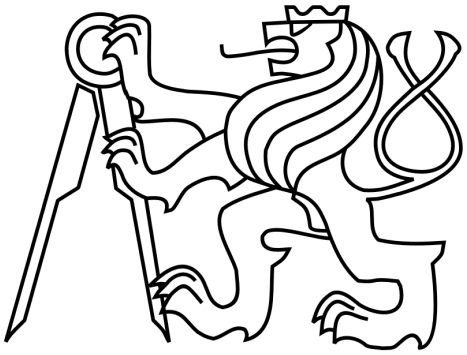

# DOCTORAL THESIS

August 2018 Ing. Vladimír Molata

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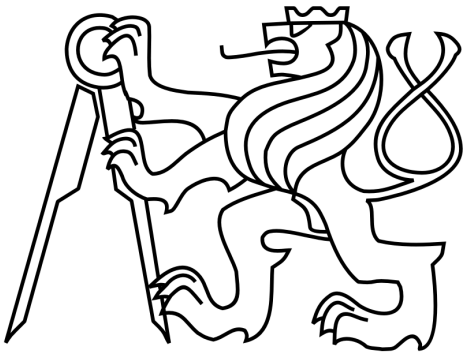

# Advanced Power Management for Portable Devices

## DOCTORAL THESIS

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Prague, August 2018

Ph.D. Programme: P2612 Electrical Engineering and Information Technology
Branch of study: 2612V015 Electronics

Supervisor: doc. Ing. Jiří Jakovenko, Ph.D

**Declaration**

I declare I have completed my doctoral thesis on my own with the contribution of my supervisor and consultants. I used only materials (literature, projects, articles) specified in the attached list.

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In Prague, August the 31st, 2018

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Vladimír Molata

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## Abstract

The dissertation thesis deals with the design, verification, optimization, and characterization of basic blocks and sub-blocks that are used in power management for portable devices for which only a limited power supply is available. The reason is that power management is being assigned an ever higher priority by trying to prolong the life of the batteries and hence the whole device powered by this battery.

The work aims to inform readers about issues and possible solutions in the area of power management for portable systems where only a limited power source is available. In particular, it focuses on two basic elements which are most commonly used in power management, linear regulators and switching converters. Each of these elements has certain advantages and disadvantages. Depending on the requirements that are imposed on the supply voltage, we need to choose the optimal configuration.

It also discusses the latest trends in the field of power management, both capacitor-less linear regulators and switching converters. In the case of switching converters, it is divided into parts, namely synchronous converters, which are used for example supplying of the radio frequency power amplifier which is based on Envelope Tracking technique, and then on frequency control for asynchronous converters.

Research in the field of linear regulators for the system on chip applications brings a new solution for the reduction of dedicated capacitors of the regulators and thus the price reduction. Instead of such dedicated capacitors, the capacitor-less regulator is loaded only with capacities (in the range from several hundreds of picofarads to several single nanofarads) of systems it powers. And thanks to this approach, for example, the internal parts of the switching converter or true random number generator can be powered by an uninterrupted power supply, thereby improving its performance.

The work is also focused on the design of switching converters. On one hand, it deals with the synchronous converters, sub-blocks in the PWM controller like ramp generator and also the issue of increasing the efficiency of a three-level switching inverter, where a special sensor is used to determine the orientation of the current in the coil, which is based on the indirect sensing method. And further, stabilization of the switching frequency for asynchronous converters based on the trans linear circuit while preserving their excellent transient properties. The proposed concept avoids the need for a frequency feedback control such as a PLL or DLL.

**Keywords:** Power management unit (PMU), capacitor-less linear regulator, switching-mode power supply (SMPS), current direction sensor, ramp generator, frequency predictor.

## Abstrakt

Předložená disertační práce se zabývá návrhem, verifikací, optimalizací a charakterizací základních bloků a dílčích podbloků, které se využívají ve správě napájení pro přenosná zařízení, u kterých máme k dispozici pouze omezený zdroj energie. Je to z důvodu, že správě napájení se přiřazuje stále vyšší priorita a to je dáno tím, že se snažíme stále více prodlužovat životnost baterie a tím i celého zařízení, které je touto baterií napájené. Zejména se pak zaměřuje na dva základní prvky, a tj. lineární regulátory a spínané konvertory, které jsou pro správu napájení používány nejčastěji. U každého z těchto prvků lze najít jeho výhody či nevýhody, které musíme brát při návrhu systému v potaz.

Práce se věnuje nejnovějším trendům v oblasti správy napájení a to zejména bez-kapacitním lineárním regulátorům a spínacím měničům. U spínacích měničů se pak dělí na dvě části a to na synchronní spínací měniče, které se využívají například pro napájení vysílacích vysokofrekvenčních zesilovačů, kde pro zvýšení účinnosti vysílacích částí se zde využívá například technika zvaná „Envelope Tracking“ a dále pak na měniče s proměnnou spínací frekvencí.

Výzkum v oblasti lineárních regulátorů pro SOC přináší nová řešení pro odstranění velkých vnějších (externích) kondenzátorů u těchto regulátorů a tím i snížení ceny. Na místo těchto externích kondenzátorů je výstup bez-kapacitních regulátorů zatížen pouze kapacitou jednotlivých systémů, které napájí. Tato kapacita se pohybuje v rozmezí stovek pikofarad až jednotek nanofarad. Díky tomuto přístupu lze například interní části spínaného měniče nebo generátor náhodných čísel napájet nezarušeným napájením a tím zlepšit jeho vlastnosti.

Další část je zaměřena na problematiku týkající se spínaných napájecích zdrojů. Jednak se věnuje vylepšení podbloku v PWM kontroléru a problematice zvyšování účinnosti tříúrovňového spínaného měniče, kde se využívá speciální senzor pro určení orientace proudu v cívce, který je založen na nepřímé metodě snímání. A dále pak stabilizaci spínací frekvence u měničů s proměnou frekvencí při zachování jejich přechodových vlastností, kde navrhovaný koncept stabilizace spínací frekvence nevyžaduje zpětnou vazbu, oproti systémům pro řízení frekvence pomocí PLL nebo DLL.



**Klíčová slova:** Správa napájení, bez-kapacitní lineární regulátor, spínaný měnič, senzor pro určení orientace proudu, generátor rampy, frekvenční prediktor.

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# Nomenclature

| | |
|---|---|
| 3G | Third Generation |
| APT | Average power tracking |
| BCD | Bipolar, CMOS, DMOS |
| BW | Bandwidths |
| CCM | Continuous Conduction Mode |
| DAC | Digital-to-analog converter |
| DCM | Discontinuous Conduction Mode |
| DLL | Delay-locked Loop |
| DSP | Digital signal processor |
| EA | Envelope Amplifier |
| EM | Envelope modulator |
| EMI | Electro-Magnetic Interference |
| EPP | End point prediction |
| ESR | Equivalent Series Resistance |
| ET | Envelope Tracking |
| FCC | Floatinig Capacitor Converter |
| GPS | Global Positioning System |
| HM | Hysteretic Mode |
| ICs | Integrated Circuits |
| LDO | Low Dropout |

LQ Low Quiescent

LTE Long Term Evolution

LTE-A Long Term Evolution Advanced

MP3 Digital Audio Format

NFC Near Field Communication

OVD Output Voltage Detector

PA Power Amplifier

PAPR Peak-to-Average Power Ratio

PLL Phase-locked Loop

PMU Power Management Unit

PWM Pulse-Width Modulation

RSS Redundant state selection

SDRAM Synchronous Dynamic Random Access Memory

SMPS Switching-mode Power Supply

TL Trans Linear

TRNG True Random Number Generator

Tx Transmitter

ULQ Ultra Low Quiescent

DC Direct Current

$C_{diff}$ Error amplifier output capacitance

$P_x$ Pole

$R_{diff}$ Error amplifier output resistance

$V_{dsat}$, $V_{sat}$ Saturation voltage

$V_{ds}$ Drain-source voltage

$V_{out}$ Output voltage

$V_{plus}$ Supply voltage

DC Direct Current

DC-DC converters Convertor is an electronic device which is supposed to change one DC voltage to another DC voltage level

ET PA Envelope Tracking Power Amplifier

FCC Flying Capacitor Converter

RF Radio Frequency

SoC System on Chip

WiMAX Worldwide Interoperability for Microwave Access

# 1 Chapter Introduction

Currently, the portable devices go through rapid development in order to help us in many ways in our daily life. Their main functions contain a GPS and NFC module, a display, a high performance audio/video subsystem, modem for wireless communication or a radio receiver module, a memory subsystem with SDRAM and Flash, an application processor with graphics acceleration, etc. Great emphasis is placed especially on increasing the computing power. However, we need to ensure also adequate lifetime and reliability of these devices. The new processing technologies, especially for the processor and memory, evolve rapidly. Reducing power consumption is still difficult to achieve. On the contrary, power consumption increases, due to increasing operating frequency. The development of battery technology is not improving sufficiently either. The solution of the above can be found in advanced power management, which is the key factor to achieve the required properties.

Increasing priority of optimized power management and consequently prolonging battery life of portable devices is one of key reasons why chip design changes towards system on chip (SoC) solutions. The power consumption of such a system varies extremely over the different use cases; the lowest power consumption of below $50\,mW$ is measured for MP3 audio playback to the headphone and over $3\,W$ are required for video decoding including the power for color display and the stereo speaker. Many different use cases have to be considered and for each one the overall power consumption must be optimized to guarantee a long battery operation. In addition to the power consumption, the overall size is a key differentiator for a portable device. Of course, lower power consumption enables the usage of smaller batteries, but in addition, the devices get smaller every year with increased functionality which is only possible by higher integration. The main task of power management unit (PMU) is to establish a flow of energy from a battery to a device in the most efficient way and so to contribute to extension of lifetime of such a complex system.

PMU deals with a distribution of energy depending on actual power supply demand of particular circuits (active, stand by, sleep and power off). PMU is usually divided into several parts according to voltage levels demanded by particular blocks. The most frequent demands are low noise and constant supply voltage. The blocks that are most commonly used in power management are switching converters and linear regulators.

With the increasing effort to integrate all circuits into a single chip, thereby establishing a SoC solution, the demands for PMU and its integration are growing [1]. Ideally, each block in the SoC should be supplied by independent regulated voltage. This can be achieved for example by using a dedicated on-chip linear voltage regulator for each circuit in the SoC. The main assumptions concerning these regulators in the SoC are small silicon area, low power dissipation, and last but not least the absence of external components that must be connected to the chip, and thus increasing the price of the whole system and occupying pins of the chip. The main objective in this part of research is to develop possible architectures for capacitor-less linear regulators, which can be used in SoC applications. There will be presented two topologies of the capacitor less linear regulators. The first one is based on PMOS power transistor and the other on NMOS power transistor.

Due to the quickly changing nature of the load, which is often determined by the software applications, the supplies are required to have fast dynamic response and high efficiency over the full range of operation. These requirements can be achieved by switching regulators that have been used in ICs for many years.

The power amplifier (PA) is the most power-consuming component in portable devices for wireless communication and its low amplification efficiency leads to a short battery life. Moreover, as new generation of wireless communication systems is developing (such as LTE, LTE-A, and WiMAX) and their information content increases, modulation systems need to have wider bandwidths (BWs) and a higher peak-to-average power ratio (PAPR). To satisfy the linearity specification of the signals, a PA should be operated at a back-off output power region, where the efficiency is low. To improve the low efficiency at the back-off power region, many efficiency enhancement techniques have been proposed.

The envelope tracking (ET) technology is a promising approach to achieve both high linearity and high efficiency. Because supply voltage of the PA is modulated by a supply modulator, the efficiency of the envelope tracking power amplifier (ET PA) is proportional to the efficiency of the supply modulator. In an ET PA, a supply modulator tracks the radio frequency (RF) envelope and supplies an instantaneous collector bias voltage to the PA, which is minimized to ensure high efficiency without linearity degradation for a given instantaneous input power. Several topologies for the ET have been proposed such as: fast buck converters, multi-level buck, parallel hybrid structure with a Class-AB amplifier AC-coupled with a buck converter. For an improved efficiency, a feed-forward signal,

a dual-switch, a multi-phase PWM control, or multi-level power stage is used. These techniques enable more accurate tracking of the switching converter without increasing of the switching frequency. In this part of the research we will focus on three-level flying capacitor converter (FCC). More precisely, we will engage the issue of efficient regulation of the flying capacitance voltage in the three-level FCC for 4G RF PA.

Switching DC-DC converters (e.g. Buck) with voltage-mode PWM controller (Fig. 1.1) are widely used as basic building blocks for portable devices due to their high power efficiency. Due to the increasing demands (e.g. switching frequency, low current consumption and good regulation of these regulators) we need to develop new design approaches, which will bring the required properties. One of the essential blocks in the PWM controller is the ramp generator. We can improve the performance of the whole system by designing a precise ramp, which will be proportional to the input voltage (to generate feedforward effect), to decrease the current consumption (by excluding the comparators from this block) and significantly increase ramp frequency by omitting the comparator's delays.

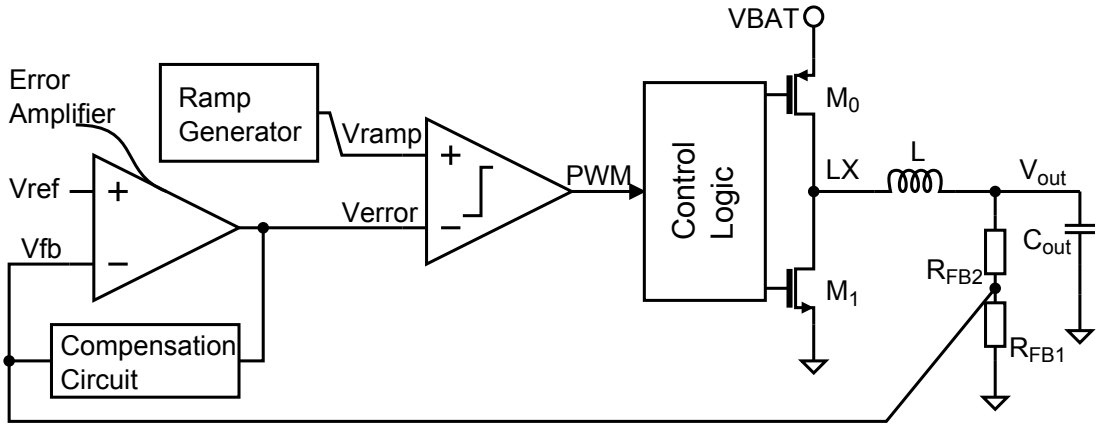
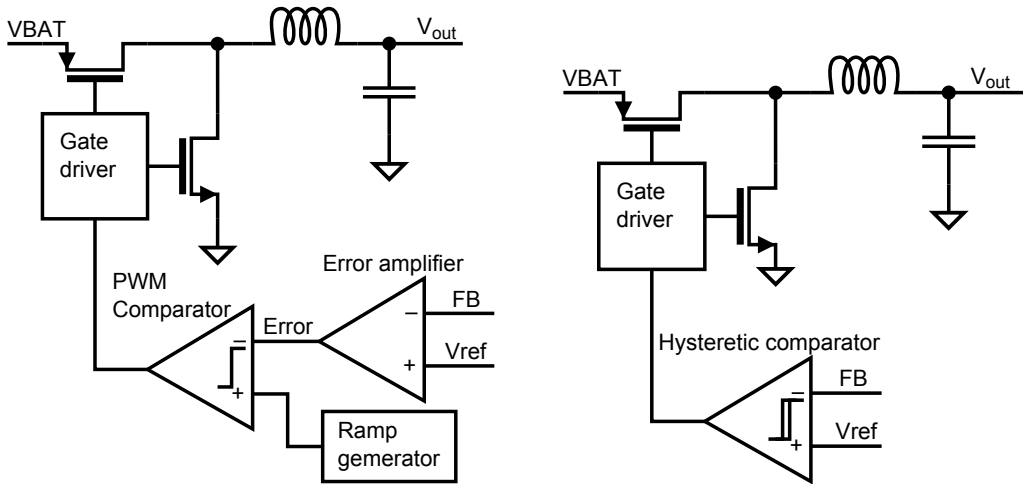



Figure 1.1.: Block diagram of a voltage-mode PWM buck regulator

The most essential principle of a switching converter (for example a Buck converter) is that the controller computes $T_{ON}$ and $T_{OFF}$ times for the power stage based on the various conditions of the Buck.

In a synchronous converter such as a PWM one, the period $T = T_{ON} + T_{OFF}$ is a constant defined by the frequency of the modulation ramp and the ratio $T_{ON}/(T_{ON} + T_{OFF})$ is determined by a feedback loop set to regulate the output voltage of the converter (Fig. 1.2a). On the opposite, an asynchronous converter such as an Hysteretic Mode (HM) controller (Fig. 1.2b), has no external definition of $T = T_{ON} + T_{OFF}$. It is derived as a result of the converter parameters ($L$, $C$, hysteresis for example) and the external parameters ($VBAT, V_{out}, I_{LOAD} \ldots$). For specific type of the converter, the relation between $T$, the converter parameters and the external parameters can be analytically derived.

A timing system that controls such a DC-DC converter switching frequency in a feed-




(a) Synchronous converter (b) Asynchronous converter

Figure 1.2.: Basic types of switching converters

forward way (i.e. with no direct measurement of the switching frequency), should in consequence implement this analytical derivation based on the measured external parameters. This paper presents the new concept of the feed-forward frequency control for asynchronous converters based on Trans Linear (TL) circuit. Stabilization of the switching frequency is based on modulating of hysteresis for comparator, which guarantees that the switching frequency is as constant as possible, thus avoiding the need for a frequency feedback control such as a PLL or DLL. The proposed solution preserves excellent transient properties of the asynchronous converters.

## 1.1. Organization of this thesis

This thesis is organized as follows. The topic of this work together with descriptions of author's contributions and the state of the art are introduced in chapter 1. The PMU fundamentals and elementary building blocks are summarized in chapter 2. Chapter 3 details the principle, design, implementation and measured results of capacitor-less linear regulators. Chapter 4 deals with the synchronous PWM converter for ET technique especially the sensors for current direction sensor. Chapter 5 describes the principle, design, implementation, and measured results of a new concept of triangular ramp generator. Frequency control technique for asynchronous switching converters is discussed in chapter 6. Finally, in chapter 7 are summarized the achieved results and recommendations for future research.

## 1.2. Author's scientific contributions

The scientific contributions of this research are in the area of power management for portable systems where only a limited power source is available. However, the concepts and techniques used in the proposed linear regulators, the apparatus for current direction detection, triangular ramp generator with single ended output and frequency control for asynchronous converters can be utilized in other general purpose power management systems. The contributions can be categorized into these sections:

- Author has developed new architectures for capacitor-less linear regulators with low current consumption for SoC applications. In order to achieve the research goals, the transient characteristics of capacitor-less regulator was improved by new method which compensates lack of capacity of eliminated dedicated capacitors. This can be achieved by implementing of fast feedback loops, so critical for this type of regulators. Author has developed two new topologies of the capacitor less linear regulators which were designed in 130 $nm$ bulk CMOS technology known as HCMOS9A.

- Author has designed new sensor for current direction detection in the inductor, which is used in apparatus for efficient regulation of the flying capacitance voltage in the three-level flying capacitor converter for 4G RF PA (switching frequency > 80MHz). For the implementation of this control technique special triggered comparators have been developed. With these comparators we can create the sensor for current direction detection, which is based on indirect measurement of the coil current through. The basic principle is based on the voltage drop that is generated at the power switches. The switching convertor with current direction sensor was designed by the author in the technology known as HCMOS9A.

- Author has developed new concept of dual edge ramp generator with single ended output. This ramp generator can be used in PWM application (e.g. for DCDC converters, D-class inverters or amplifiers). Originality of the design of the saw tooth signal generator consists mainly in the use of new control loops, ensuring a low power consumption in a wide range of operating frequencies. This new solution has been proposed due to the fact that comparators are not used in the proposed generator for detecting threshold levels of the output signal. The device is fully integrated and is manufactured in 130 $nm$ bulk CMOS technology known as HCMOS9GP.

- Author has designed new concept of feed-forward frequency control for asynchronous converters based on TL circuit. Novel architecture and configuration of the feed-forward frequency control circuit for asynchronous DC-DC switching converters has been developed. The proposed solution preserves excellent transient properties

of the asynchronous converters. Proposed feed-forward frequency control method is based on modulating of hysteresis for the comparator, which guarantees that the switching frequency is as constant as possible. The proposed concept avoids the need for a frequency feed-back control such as a PLL or DLL. The implementation techniques are experimentally verified on a prototype chip manufactured in $160\,nm$ BCD technology known as BCD8sP and operates at the switching frequency of up to $2\,MHz$.

All of these technologies have been provided by STMicroelectronics.

## 1.3. State of the art

With each new technology, demands on the power supply of the blocks in the system are growing, especially low noise or high performance [2, 3, 4]. Furthermore, it also increases the number of voltage domains, which occur in the individual systems. With the increase of the voltage domains, it is necessary to develop and upgrade the existing approaches in power management, so that we can meet these requirements. One of the biggest challenges for distribution of the power supply is to create devices that meet the strict requirements and occupy a small area.

In power management, there are three commonly used general circuit topologies [5], which provide DC supply voltage on the chip [6]. The first group includes switching converters, which are employed to regulate high-performance integrated circuits like processor or RF PA due to their high power efficiency [7]. Another possible topology is created by charge pump regulators. These circuits are usually utilized to generate high voltage for lighting or memory units. And finally linear regulators that are used to provide low noise supply voltage with very low ripple for noise sensitive blocks like analog/RF circuits [8, 9]. Typically, these all devices require external components that must be connected to the chip, and thus increase the price of the whole system and occupy pins of the chip. In the last decade, a considerable number of the authors working in the field of power management deal with the problems associated with the elimination of external components, because by removing of external components of power supply devices we bring new possibilities in power management.

For example the limitation of the classical LDO regulators is caused mainly due to the associated single pole-zero cancellation scheme, in which an external capacitor with a high equivalent series resistance (ESR) is required. With help of ESR we are able to create a zero point which can be placed near to the second pole of the system and so we gain the necessary phase shift and the circuit is stable. However, this solution brings difficulties which are associated mainly with the bandwidth limitations and thus short response time

[10, 11, 12]. There are several different principles how to narrow this dependence on ESR. To the most common methods belongs compensation inside the regulator, or creating of inner zero or creating adaptive modulation of dominant pole. Another method is also elimination of a large external capacitor [11]. However, the removal of the external capacitor at the LDO regulator brings disadvantages such as the deterioration of the transient response [10, 13]. Furthermore, there may be problems with stability at low current load due to the fact that output pole is moved significantly with this load.

From this reason it is necessary to extend the circuit by fast loops, which will be responsible for fast response of the circuit and which will have greater bandwidth than the bandwidth of the slow regulating loop. At the same time we need to ensure stability of the regulators.

There are several approaches how to deal with these problems, which have been published. The first approach uses direct current feedback to improve line and load regulations [14]. In this structure, symmetrically-matched voltage mirror is employed in sensing the load current. Next solution uses a Dual-Loop for transient improvement [15]. In this concept there are two OTAs, one for slow voltage loop and another for current loop. Voltage-Spoke detection circuit for improving of transient response of capacitor-less LDO is proposed in [16]. The detection circuit is based on capacitive coupling and it makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Other authors propose capacitor-less LDO with a low power output voltage detector (OVD) [17]. The OVD is based on an R/C high-pass filter which is able to detect the fast-changing voltage at the LDO output and activate an additional path to control the power transistor. Last but not least paper presents a capacitor-less LDO regulator with a slew-rate enhancement circuit [18]. This proposed slew-rate enhancement circuit senses the transient voltage at the output of the LDO to increase the bias current of the error amplifier for a short duration.

Another important area of power management, which engineers currently investigating, is power supply for RF PA for broadband 3G/4G wireless standards. It is due to the fact that these standards utilize highly spectral-efficient modulation schemes with inherently non-constant-envelope signals having high PAPR. The non-constant envelope signals with high PAPR require the PAs to be backed off from their saturation power to satisfy the stringent linearity specs. This is a major bottleneck for realizing highly efficient mobile 3G/4G transmitters (Txs).

Envelope tracking technique is a dynamic supply modulation scheme, and this technique is among the most effective approach to enhance both high linearity and high efficiency of efficiency of PA. Recent literature has demonstrated several topologies for the envelope amplifier (EA).

The topology of the first approach, which is most common, is based is based on a hybrid modulator [19]. This modulator combining a class-AB buffered linear amplifier and a highly efficient switching-mode buck converter in a master–slave configuration. The linear stage must have large bandwidth to suppress the switching ripples. Next solution uses high-frequency buck PWM converter [20]. This modulator has constant switching frequency, which is equal $130 MHz$. Other authors propose dual switcher hybrid architecture [21]. The supply modulator has a combined structure of a linear amplifier and two phase switching converter. This parallel combination of switching converters enable more accurate tracking without increase of the switching frequency. Least but not last concept ET modulator is three level buck converter in [22]. This is an improved version of a regular buck converter where are two additional switches and flying capacitor. With this arrangement, the circuit can apply three different voltage levels to the filter and thereby doubling its effective switching frequency. However, there are several practical challenges for designing the ET systems, such as the bandwidth limitation of the envelope modulator, and the precise timing alignment between the envelope and the RF paths.

The PWM voltage-mode converters (e.g. Buck) require a ramp generator to generate the ramp signal. This ramp generator should have as low power consumption as possible in order to achieve high efficiency of the converter, free of the external components for reducing board cost, and at the same time small deviation of the ramp for both amplitude and timing. That is important specially for higher switching frequencies of converters, because this ramp deviation causes a shift of harmonic frequencies at high frequencies. It affects the noise performance of the circuits powered by the PWM voltage converter. The voltage-mode PWM controller and the ramp generator have been proposed and used for years. Typically it contains a capacitor, a charging current branch, a discharging current branch and the comparators [25, 26]. One of the possible solutions to reduce the power consumption is to create more efficient comparator [23] or to exclude it from this block.

For improving the current consumption, the ramp generator with Schmitt trigger was introduced in [24]. This paper proposes a ramp generator with Schmitt trigger circuit replacing the conventional ramp circuit using two comparators and one S-R latch circuit. However, in this case, the ramp is generated in dependence on the hysteresis voltage $V_{SPH}$ and $V_{SPL}$ on the Schmitt trigger circuit and therefore no longer guarantees the constant switching frequency of the converter. A similar approach was also chosen in [23], with the difference that a hysteresis comparator is used here. This reduces the consumption but the switching frequency is no longer constant. In [25] 10/30MHz PWM buck converter with an accuracy-improved ramp generator is proposed. To shorten the delay time of the comparator in the ramp generator, a high speed two-stage push pull comparator is used. This is associated with higher generator consumption. The presented proposal in this work

deals with the second option, which is the complete removal of comparators from the ramp generator.

Asynchronous converters (e.g. hysteric control) offers an unsurpassed transient response in comparison with other analog and digital techniques, which makes it advisable to adopt this technique in all cases where wide bandwidth and robustness are required [34]. However, the drawback is that its switching frequency changes with varying input voltage, output voltage or load current, which might result in severe electro-magnetic interference (EMI).

At present, many works have been presented in order to keep the operating frequency of the converters stable, including adaptive hysteresis methods [27, 30, 32, 33] and external signal methods with injection of fixed frequency [31]. The self-adaptive window controller is proposed in [27, 33] to adjust hysteresis window according input voltage, output voltage and load current adaptively. In this system frequency-to-Voltage Converter (FVC) is used to transform the switching frequency $f_s$ and reference frequency $f_{ref}$ to its corresponding voltage $V_s$ and $V_{ref}$. Then the error between $V_s$ and $V_{ref}$ is used to set the correct hysteresis to achieve constant switching frequency. Although the frequency stabilization is excellent, the disadvantage of this solution is in its complexity, size and overall consumption. The second-order sliding-mode (SOSM) control approach is applied to synchronous buck dc–dc converters, proposed in [28, 29]. Here, the digital state-machine structure is used to stabilize the switching frequency. The novel architecture and configuration of the feed-forward frequency control circuit for asynchronous DC-DC switching converters is presented.

# 2 Chapter
# Power Management Unit

Every electrical and electronic system needs a power supply to be able to operate. The PMU is especially important in applications requiring high efficiency such as portable electronic systems. This unit can control the charging time, current, and voltage of the battery charger and is responsible for balanced energy distribution according to actual supply-demand of particular circuits and their mode (for example, a device which is in standby mode does not need much energy).

When designing the power supply for the system, consideration needs to be given to the number of supply voltages required, the power handling capabilities of the supplies as well as the ultimate generator of the input. Depending on the power supply requirements of the system, there are several building blocks that could be used to make up the PMU. The combination of the building blocks depends on the input source and output power constraints of the system.

As can be seen from the Fig. 2.1 where is depicted a block diagram for MP3 Player / Recorder, PMU consists of several parts according to requirements of particular blocks in the system. The blocks that belong into PMU are mainly switching converters, charger and linear regulators [35]. Parts of this chapter has been published by the author of this thesis in [55].

## 2.1. Regulation principles

Each electronic power regulator consists of a power element, a controller, and a voltage reference [38], as shown in Fig. 2.2. The input power coming from the supply is converted by the power element and provided to the load. The power conversion can be used a current, a voltage, or a frequency converter (or any combination of these physical quantities). The feedback controller compares the output voltage of the power element with a reference voltage value and acts on the power element so that the error between the two is

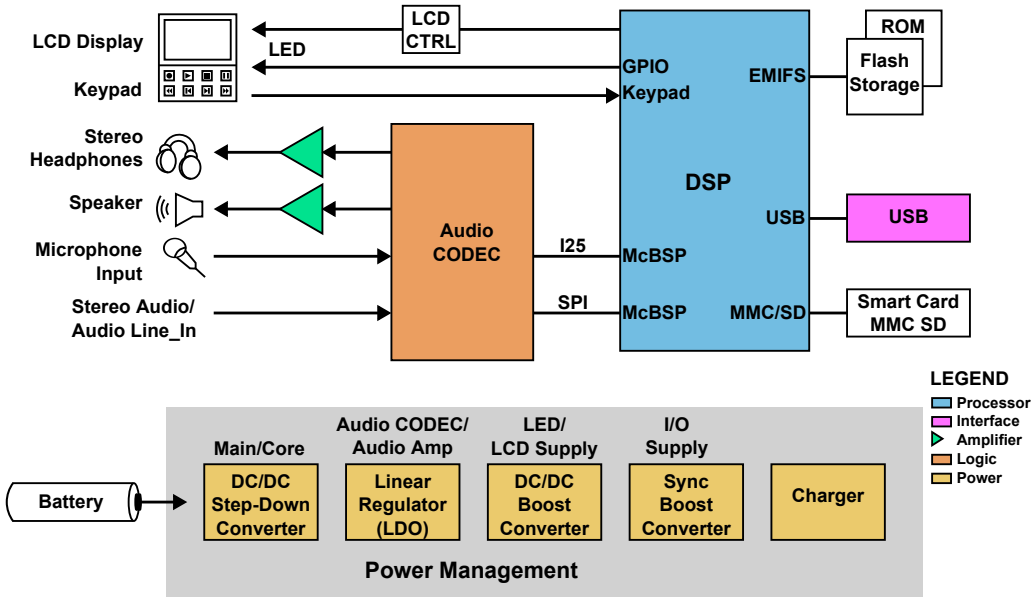



Figure 2.1.: Block diagram of MP3 player [36]

minimized. Both linear regulators and switching regulators use this elementary regulation principle.

## 2.2. Linear regulators

A linear regulator is a circuit that keeps a constant set voltage across its load despite changes in load, temperature, and power supply, among other things. Consequently, such a device has to have the temperature properties of a voltage reference, a good driving capability, and flexibility in output setting. The linear regulator uses a feedback control of sensing the resistive voltage drop to regulate the output voltage as shown in Fig. 2.3. It is constituted of a Power Transistor, a voltage reference ($V_{ref}$) and an error amplifier with a resistive feedback loop composed of R1 and R2. The capacitor $C_{out}$ is used for adjusting the stability in the loop compensation.

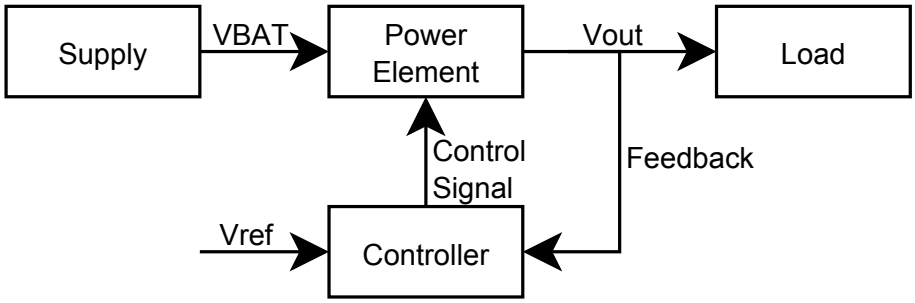



Figure 2.2.: Block diagram of a typical electronic power conversion system

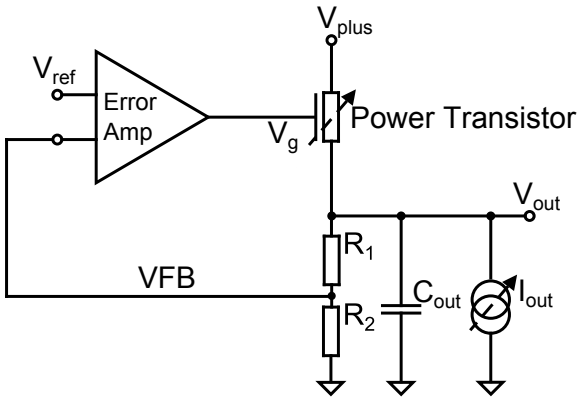



Figure 2.3.: Principal block diagram for linear regulator

The power transistor used in a linear regulator works as an adjustable resistor that reduces the voltage by dissipating the power that is not needed. The error amplifier adjusts the gate voltage $V_g$ so that the voltage drop across the power transistor gives the desired output voltage value $V_{out}$. The regulated voltage value is controlled by the gain of the resistive feedback loop. The error amplifier tends to equalize the voltage at its inputs, and therefore, the load voltage $V_{out}$ is given by:

$$V_{out} = V_{ref} \frac{R_1 + R_2}{R_2} \tag{2.1}$$

Linear regulators are very popular due to low electrical noise, the design is less complex and output ripple is smaller in comparison to switching converter, but linear regulators also have some drawbacks. Their efficiency is poor, which means the power dissipated is generally high.

The power loss in the linear regulator mainly comes from the voltage drop across the power transistor. The maximum efficiency of a linear regulator is defined in the formula 2.2 where $V_{out}$ is the output voltage, $I_{out}$ is the output current and $V_{plus}$ is the supply voltage [37].

$$Eff = \frac{V_{out} I_{out}}{V_{out} I_{out} + \left(V_{plus} - V_{out}\right) I_{out}} \approx \frac{V_{out}}{V_{plus}} \tag{2.2}$$

Linear regulators can be divided into two basic groups [39]:

- Conventional linear regulators
- LDO regulators

The only difference between these two topologies is in the orientation of a power transistor. Conventional linear regulator utilizes a transistor which is connected in common drain, or this transistor is replaced by BJT transistor or two transistors in Darlington configuration.

In contrast, LDO regulator uses configuration with a common source. Both these basic configurations are depicted in the Fig. 2.4. The orientation of a power transistor has a general influence on both working mode and stability of the linear regulator.

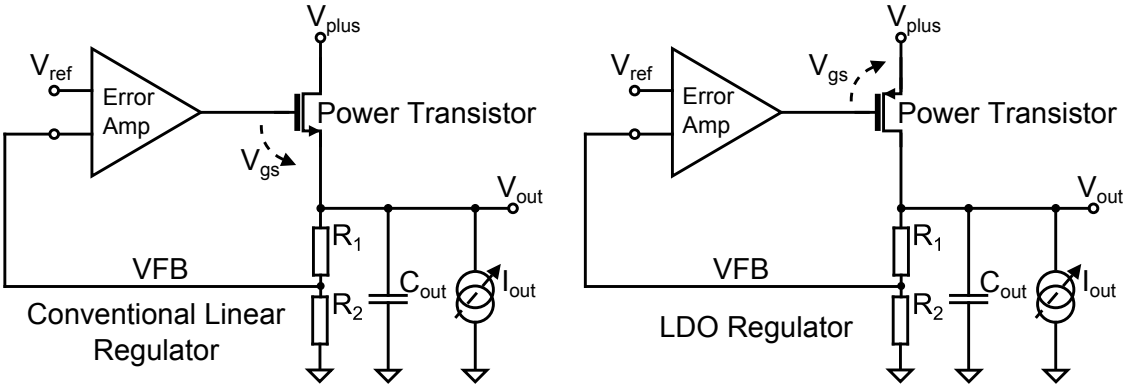



Figure 2.4.: Topologies of linear regulators

One of the main drawbacks of the conventional linear regulator is that the gate voltage of power transistor must be at least by $V_{gssat}$ greater than the output voltage. This is not a problem in itself, but in addition to the ever decreasing supply voltage, this leads to the fact that the supply voltage gets below a possible level of gate voltage. However, this leads to a fact that such a circuit is difficult to use in low voltage applications. In order to use such a regulator for low voltage applications, it is necessary to use a charge pump and this way we can reach required gate voltage level at the gate of a power transistor.

An LDO regulator does not need a charge pump because the power element is in the configuration called common source. Saturation voltage $V_{ds}$ of such a transistor creates a limit in which a regulator can work. This drop of voltage, or also $V_{dsat}$, depends on the maximum output current of the regulator and also on parameters of the power transistor.

As has been mentioned earlier, the orientation of the power transistor has an influence on the stability of the regulator. Fig. 2.5 depicts typical small signal AC responses for both topologies. As it appears from the figure, the conventional linear regulator is stable thanks to its small output impedance. First pole, $P_1$, which is dominant, is created by the output impedance of an error amplifier and input parasitic capacitance of the power transistor. Second pole, $P_2$, which is output pole, moves with loading impedance. The position of this pole is on much higher frequencies in comparison to the first pole.

LDO regulator can work in low voltage applications without having to use a charge pump but its disadvantage is that it can become unstable during a change of load. Big loading capacitance together with large output impedance create dominant pole $P_1$. However, pole $P_2$ from an error amplifier is much nearer to the pole $P_1$ and this can lead to instability of such a system. In order to use this regulator, it is necessary to use internal or external compensation, which ensures the stability of the circuit.

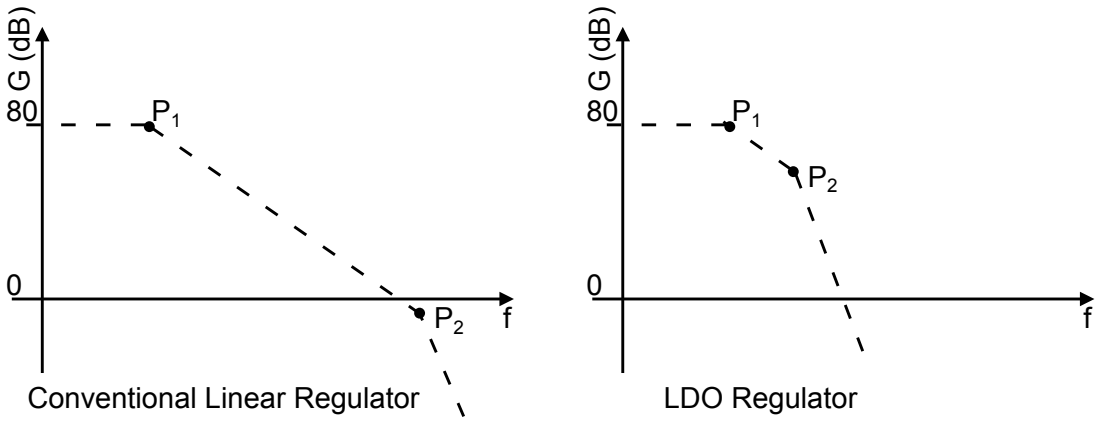



Figure 2.5.: Magnitude characteristics with shown poles for both topologies without compensation circuits [55]

### 2.2.1. LDO regulators

The voltage regulator of the LDO type creates a small family of elements which belong to power management. Its main usage is for supplying blocks where low noise and high accuracy of voltage are necessary. As it is apparent from its name the task of LDO regulator is quite simple - output voltage regulation to keep the output voltage constant, independent of change in load or change of battery voltage. In other words, LDO is a voltage source which keeps the output voltage constant even in the case that battery voltage fluctuates or supply-demand is changing [40].

This regulation of output voltage is the most necessary during fast changes in load current which change depending on the working modes of each particular block. At all portable devices, we try to reduce their consumption and so to prolong their endurance. For this reason, the circuits which are not actually needed are cut off and it decreases the total energy consumption. These kinds of circuits are used for a large group of circuits not only because of low voltage drop but also for its low noise, low price and low internal consumption. As has already been said, linear regulators suffer from low efficiency. The efficiency of such a regulator is inversely proportional to the voltage drop on power transistor ($V_{plus} - V_{out}$). From this reason, in some PMU the LDO regulator is used as a post-regulation element.

#### Properties of transient responses

Presence of a large external capacitor ($C_{out}$) in conventional LDO regulators (Fig. 2.4) generally improves properties of the regulator during transient responses [40]. It is due to the fact that the external capacitor stores energy which is proportional to the output voltage. This energy is transformed into current during a load transient. Equation 2.3

roughly describes relation between variation of output voltage, $\Delta V_{out}$ , variation of output current caused by load transient, $\Delta I_{out}$, size of the external capacitor $C_{out}$, $t_{lp}$ is delay caused by limited loop bandwidth and $t_{SR}$ is delay caused by limited slew rate.

$$\Delta V_{out} \cong \frac{\Delta I_{out}}{C_{out}} \left(t_{lp}+t_{SR}\right) \tag{2.3}$$

As can be seen from the equation 2.3, a variation of the output voltage is inversely proportional to the size of the external capacitor. Transient properties of a regulator can be improved by increasing of this external capacitor, or by reducing $t_{lp}$ and $t_{SR}$ i.e. to increase control loop bandwidth and the slew rate at the gate of pass element. Usually, inserting a buffer with a large bias current and small output resistance as the output stage of error amplifier can implement a good slew rate. On the other hand, however, increasing the bandwidth of LDO loop and maintaining the precision of output voltage of LDO may cause high power consumption, and is not very easy to implement [41, 42].

If the load transients are much faster than time response of the regulator, which is common with increasing clock frequency of IC, then the meaning of the equation 2.3 is much more evident. Fig. 2.6 depicts this situation for conventional LDO regulator.

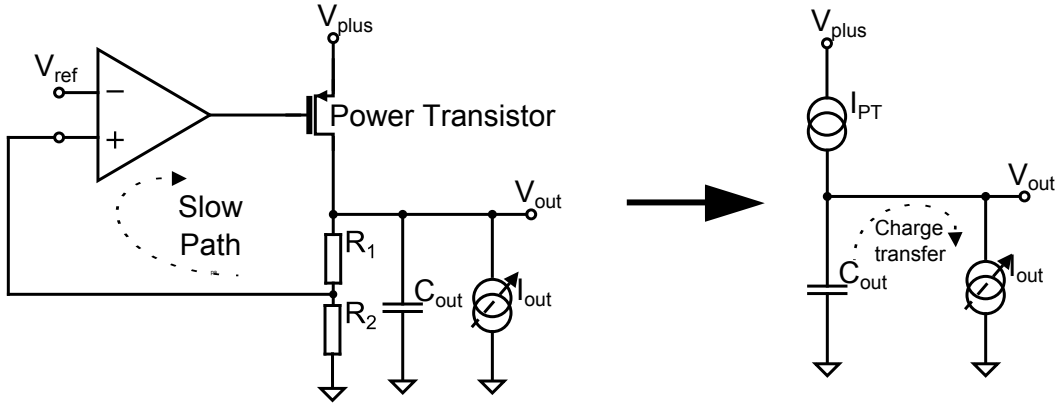



Figure 2.6.: Conventional LDO regulator with reduced loop bandwidth and its equivalent circuit diagram for fast load transients [50]

If the time response of the regulator is much smaller than load transients, we can suppose constant gate voltage and the power transistor can be replaced by constant current source. With this in mind, the change of the output voltage is described directly by equation 2.3.

To improve these properties it is necessary to replace constant current source from Fig. 2.6, where the power transistor is shown, by an adaptive source of current, which can react to fast changes of loading current.

## 2.3. Switching converters

Switching converters are favored for portable applications because of their high efficiency and large power handling capability, but the primary design limitations in the switching converter are switching noise, large electromagnetic interference (EMI) emission, and a large size due to the use of external components.

The principle of these switching converters is based on the conversion of energy accumulated in an energy storage element, such as an inductor. It is the main difference from linear regulators, e.g. LDO regulator. Linear regulators are built on a dissipative element (such as power transistor). For this reason, switching converters can achieve a higher efficiency than linear regulators. A more flexible and powerful type of switching converters is DC-DC converter using both capacitive and magnetic passive devices, in combination with active switching devices. These DC-DC converters are established to change input DC voltage to either a higher, lower, or negative DC voltage.

In Fig. 2.7 is shown the block diagram of the DC-DC converter which converts an unregulated battery source voltage $V_{in}$ to the desired regulated *DC* output voltage $V_{out}$. From this unregulated input voltage via the switch generates a rectangular wave having an average voltage equal to the desired output voltage. Output filter (low-pass) filters the rectangular wave signal so that the output voltage has the desired *DC* value, with an acceptable ripple.

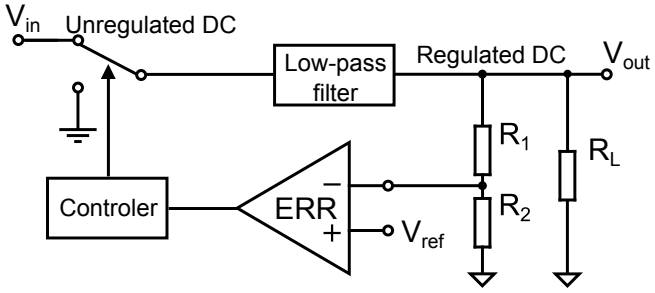



Figure 2.7.: Block diagram of the switching regulator

### 2.3.1. Basic DC-DC converter topologies

There are several different basic DC-DC converter topologies arrangements of the switching and filter components that can be used to produce the required output voltage.

Three main topologies are:

- step-down topologies (like the buck converter shown in Fig. 2.8), which are only able to provide an output voltage lower than the input voltage
- step-up topologies, which are only able to provide an output voltage higher than the input voltage

- topologies able to perform both step-up and step-down conversion with a single switching converter

There are also circuits which are able to perform opposite polarity at the output. Furthermore, we can divide the inverters into isolated topologies (in which mostly transformers are used) and non-isolated topologies with the inductor. However, in this research work, only non-isolated topologies are considered, because transformers are not easily integrate into portable systems. Each topology can be used for any application, but each of these topologies has its specific benefits and disadvantages, depending on a number of operating conditions and specifications. Examples of such specifications are the voltage conversion ratio range, the maximal output power, power conversion efficiency, power density, etc. To select the best topology for a given application, it is very important to know the basic operation, advantages, disadvantages and complexity of a particular topology [35].

A typical diagram for step-down PWM switching converter is shown in Fig. 2.8 and we can see that a switching regulator usually consists from power stage, driver and control loop. The output voltage $V_{out}$ is sensed via the divider $R_1/R_2$ and compared to the reference voltage $V_{ref}$. The Error amplifier amplifies difference of these two signals drives the modulator, which has a square wave output that is buffered and reproduced to the intermediate output node $LX$. The $LC$ filter yields the average of this square wave to the final output node $V_{out}$.

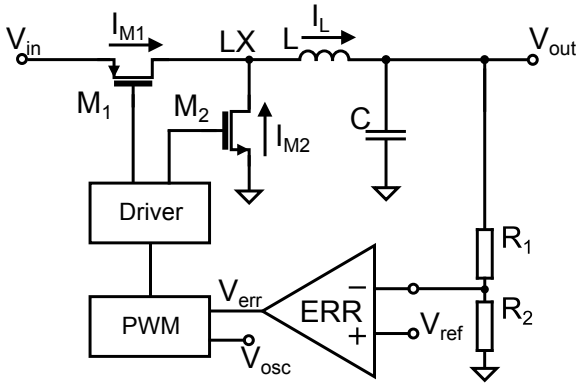



Figure 2.8.: Schematic of a typical step-down switching converter

### Step-Down converter (also called Buck converter)

This topology of the converter can only produce a lower output voltage than the input voltage but the output current is higher than the input current. The buck converter is shown in Fig. 2.9. It is the simplest step-down switching topology. It is made of a $Q$ acting as the energizing switch for the inductor $L$, a power diode $D$ assuring the continuity of the

current in $L$, and a filtering capacitor $C$ reducing the output voltage ripple on $V_{out}$. The power input is represented by the voltage $V_{in}$ and on the output voltage $V_{out}$ is required.

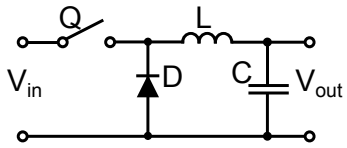



Figure 2.9.: Buck converter

The regulation of the output voltage $V_{out}$ can be done by the voltage mode controller previously illustrated in Fig. 2.8. It consists in generating a PWM signal based on the feedback voltage. In a steady state of operation, when the switch ($Q$) is closed ($ON$) for a period of $t_{on}$, the current in the inductor $L$ increases linearly and the free-wheeling diode $D$ is reverse biased. At the instant after opening the switch ($OFF$), the inductor current continues to flow in the same direction and the voltage changes its polarity. The current flows through the diode and decreases linearly.

Depending on the current load, if the current $I_L$ does not reach zero during $t_{off}$, the converter operates in the continuous conduction mode (CCM). If $I_L$ reaches zero during $t_{off}$, it tries to reverse but it is blocked by the diode $D$ and the converter operates in the discontinuous conduction mode (DCM). Some definitions are made in Equation 2.4:

$$\begin{cases} f_{sw} = \frac{1}{t_{sw}} \\ t_{sw} = t_{on} + t_{off} \\ D = \frac{t_{on}}{t_{sw}} \end{cases} \tag{2.4}$$

The output voltage of the buck converter can be calculated:

$$V_{out} = V_{in}\frac{t_{on}}{t_{on}+t_{off}} = V_{in}\frac{t_{on}}{t_{sw}} = V_{in}D \tag{2.5}$$

The average output voltage value $V_{out}$ depends on the ratio of $t_{on}$ to $t_{sw}$. In other words, the output voltage $V_{out}$ depends exclusively on the duty cycle $D$ of the PWM signal generated by the controller when it is operating in CCM. D can vary between 0 and 1.

Compared with the other three basic topologies, the output ripple is the lowest because of the location of the inductor. This makes it appropriate for noise-sensitive loads. The disadvantages of this topology are that the switch has to be a PMOS-transistor or a floating drive must be used for the switch.

### Step-Up converter (also called Boost converter)

The boost converter topology shown in Fig. 2.10 is used when an output voltage $V_{out}$ higher than the input voltage $V_{in}$ is required. In a steady state of operation, when the switch ($Q$) is closed ($ON$) for a period of $t_{on}$, the input provides energy to the inductor. During the $t_{on}$ period, the current in the inductor increases linearly and no current is delivered to the output. During this $t_{on}$ period, the output load current $I_{out}$ is supplied from the output capacitor $C$. As soon as the switch is opened, the voltage changes its polarity and is added to the input voltage. The inductor current continues to flow in the same direction and decreases linearly. The output voltage of the boost converter can be calculated:

$$V_{out} = V_{in}\left(1 + \frac{t_{on}}{t_{off}}\right) = V_{in}\frac{1}{1-D} \tag{2.6}$$

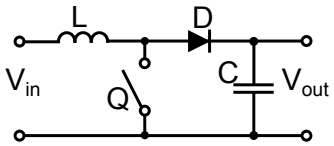



Figure 2.10.: Boost converter

The output voltage ripple of the topology is relatively high. A step-up converter is very useful for low voltages or low power applications, for example in battery-driven systems where some devices need higher supply voltage. This converter has a low input current ripple due to the inductor placed at the input, but the biggest disadvantage of this topology is the high output voltage ripple because the output capacitor has to supply the entire load during the transistor on-time.

### Inverter (also called Buck-Boost converter)

The output voltage of an inverting switch mode power supply is negative and can be higher or lower than the input voltage (Fig. 2.11). As long as the switch is closed, the current in the inductor increases linearly. When the switch is opened, the voltage across the inductor changes its polarity instantaneously. The current through the inductor stays the same and flows through the diode to the output and the capacitance and decreases linearly. The output ripple is also high because the output capacitor has to supply the entire load during one portion of the switching cycle. Some battery-driven systems like mobile phone need a negative voltage to supply some RF amplifiers.

$$V_{out} = -V_{in}\left(\frac{t_{on}}{t_{off}}\right) = -V_{in}\frac{D}{1-D} \tag{2.7}$$

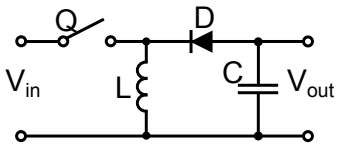



Figure 2.11.: Buck-Boost converter

### 2.3.2. Switching mode control techniques

In a switching converter, the controller drives the power devices, and its principal role is to regulate the output voltage $V_{out}$ to the requested value of voltage, as it was illustrated in Fig. 2.8. In order to achieve this, the controller can be designed to use different operation control methods. In the next part these operation control methods are discussed. The most popular regulation modes (i.e., voltage mode, current mode and hysteretic mode) are analyzed in Section 2.3.2.

#### Modulation

Mainly PWM and PFM modulations are commonly used in portable devices to maximize battery life. They provide high efficiency in step-down applications and can also convert the low battery voltage to the higher levels required for LED backlights and display bias. One of the concerns with switch-mode power converters is the generation of unwanted EMI. PWM converters are often preferred by system designers because they operate at a specified known frequency, which may make the EMI filtering design process easier. PFM converters inherently have a variable operating frequency, and therefore many system designers have concerns about using this type of architecture in portable products with sensitive audio or RF subsystems. The concerns associated with the use of variable-frequency-converter architectures are valid ones and should not be dismissed. However, the use of PFM architectures can offer significant performance improvement in certain applications. These improvements include better low-power conversion efficiency, lower total solution cost, and simple converter topologies that do not require control-loop compensation networks.

Understanding variable-frequency operating modes can help the system designer know when it may be beneficial to use a PWM, PFM, or dual mode architecture for the converter circuit. By combining both of these operation control methods into one controller, the converter can be made very efficient over a wide range of output power [63, 73].

**Pulse-width modulation -** With the pulse-width modulation control illustrated earlier in Fig. 2.12, the regulation of output voltage is achieved by varying the duty cycle $D$ of the switching devices, keeping the operating frequency constant. Usually, the pulse width

modulation control method is preferred because constant frequency operation greatly simplifies the design of the regulation feedback loop and the output ripple filter, thus avoiding stability issues. However, since the switching frequency is constant in the PWM control scheme, the switching losses (e.g., the losses due to the charging/discharging of the gate and output capacitances of the power transistors) are independent of the load current. The direct consequence is that PWM becomes inefficient when a light load is supplied because the switching losses are more dominant than conduction losses, which are load dependent [73].

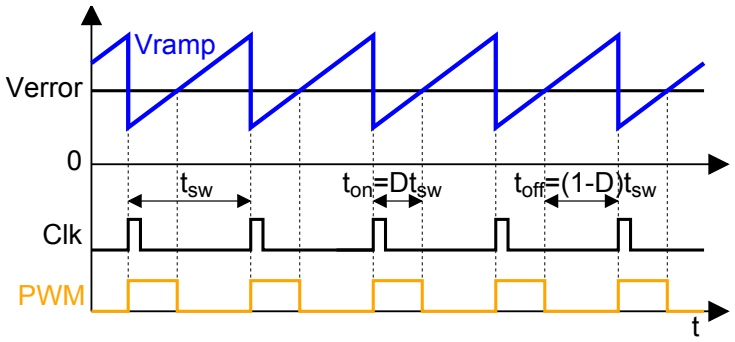



Figure 2.12.: Steady-state PWM timing diagram of the buck converter shown in Fig. 2.8

**Pulse-frequency modulation -** To overcome the dramatic efficiency reduction in lightly loaded PWM converters, an additional operation control scheme called pulse frequency modulation (PFM) has been developed. PFM is a nonlinear operation scheme in which pulse trains are applied to the energizing switch to maintain the output voltage within the preset voltage range. This mode lowers the frequency of the switching-cycle events, therefore lowering the switching losses, which are dominant to the conduction losses at light output loads (i.e., when the requested output current is low). Although PFM control has become prevalent in battery-operated mobile equipment because its light-load efficiency exceeds that of PWM, PFM is more difficult to design because this operation control scheme has some important issues concerning the stability in the frequency domain since it is a variable-frequency control scheme. PFM allows extending the battery life of the mobile equipment in the suspend and standby modes of operation. However, the low frequencies can cause switching noise to enter the audio band. This can be avoided by sizing the passives so that the PFM converter is forced to operate above the audio band at the minimum load condition.

In DC-DC converters for mobile equipment, the PFM operation control is never used standalone. It is always coupled to a PWM controller. The current trend in today‘s DC-DC converters is to increase the switching frequency of the controllers so that the passive device sizes (i.e., inductors and capacitors) can be reduced. To enable future on-chip hybrid

integration of power inductors [72], the switching frequencies are approaching $10MHz$ and they will continue to increase [71]. Therefore, the most efficient way to reach high efficiency in both heavy and light load conditions is to combine both PWM and PFM operation control schemes [63, 73].

### Control techniques

There are three main regulatory strategies in DC-DC converters. The first and most intuitive one, referred to as the voltage mode control, consists of sensing the voltage proportional to the output voltage for regulating it (as with the linear voltage regulator). The second, known as the current mode control, consists of sensing voltage proportional to the output voltage and its used as a set point for an internal current control loop for output voltage regulation. The third, called hysteresis mode control, uses a comparator to control the output voltage instead of the error amplifier. All of these methods have their own advantages and disadvantages and there is no single control mode that would be optimal for all applications [64]. In 1978, current mode control technique was introduced to respond to problems with a voltage mode [65], but using new approaches and technologies, voltage-mode can compete with the current mode [73].

**Voltage-mode control -** Arguably the most common of control techniques is voltage-mode. Thanks to its simplicity, the approach was used for the first switching regulator designs. Fig. 2.13 shows an example of a basic voltage mode regulation based on a buck converter [74]. In the voltage mode regulation, there is only a single voltage feedback loop. This loop is usually formed by a resistive network that acts as a voltage divider and a compensator network made with resistors and capacitors to ensure loop stability. The pulse-width modulation is performed by comparing the error amplifier output voltage with the ramp waveform. This duty-cycle ultimately determines the output voltage $V_{out}$. The switching frequency, set by the frequency of the modulating ramp waveform, is by default constant, which is an advantage in some applications from the point of view of filtering out the switching noise.

Fig. 2.14 shows the waveforms of the signals in a voltage mode PWM controller. The ramp waveform is generated by using the clock pulses (i.e., clk) as the command for the charging/discharging of a capacitor with a constant current. The advantages of the voltage mode regulation are [64]:

- A single feedback loop is easier to design and analyze.
- A large amplitude saw tooth waveform provides good noise margin for a stable modulation process.

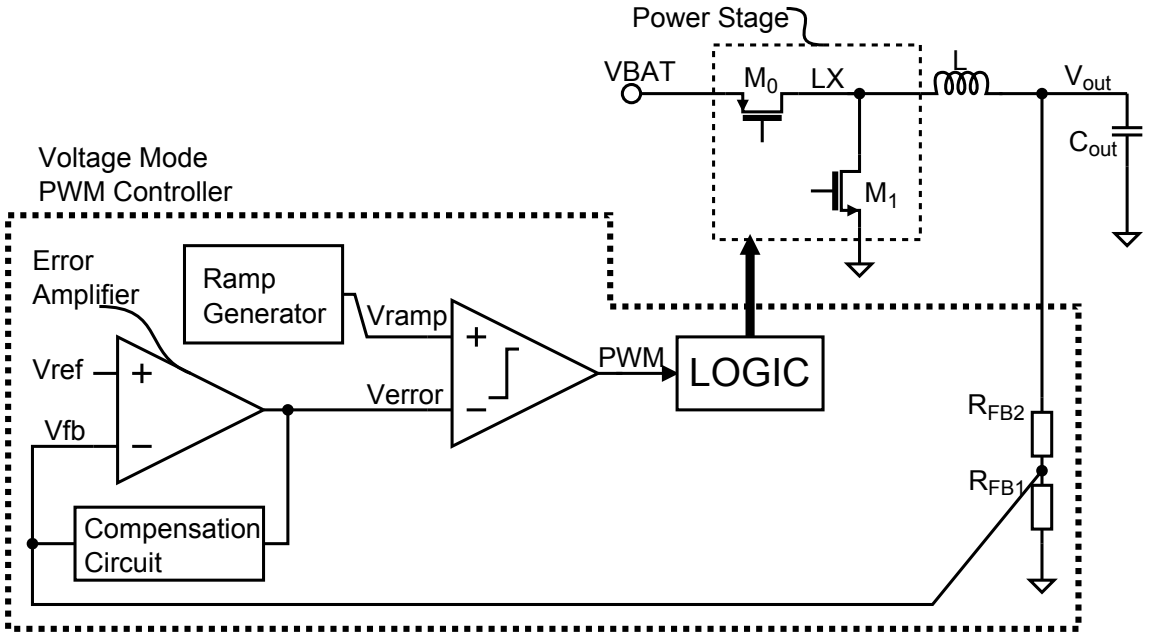



Figure 2.13.: Schematic of the voltage mode regulation principle.

- An accurate CMOS voltage sensor is easy to design and nearly lossless.

The disadvantages of the voltage mode regulation are [64]:

- Any change in input voltage $V_{in}$ or in the output voltage $V_{out}$ must first be sensed as an output change and then corrected by the feedback loop. This provides a slower transient response.

- The compensation is further complicated by the fact that the loop gain depends on the input voltage $V_{in}$.

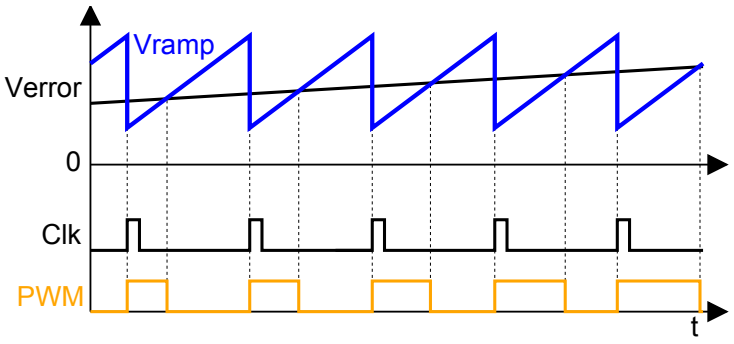



Figure 2.14.: Signal waveforms of the voltage mode regulation principle shown in Fig. 2.13

**Current-mode control -** As previously analyzed, the disadvantages of the voltage mode control are relatively significant. Therefore, as the current mode regulation was introduced in 1978 [65], designers were highly motivated to consider the various regulatory options offered by the current mode (e.g. Peak, Valley, Average Current Mode) because it seemed able to overcome all disadvantages of voltage mode control.

In current-mode control, the inductor current is regulated in a separate control loop that operates at a higher bandwidth than the voltage loop [74]. As a result, the inductor and its control loop look like a voltage-controlled-current-source for all frequencies of interest to the voltage loop. A simplified schematic of a peak current mode controlled dc-dc converter is shown in Fig. 2.15. In this case, the power transistor $M_0$ is turned on periodically at fixed instants determined by a clock, while it turns off when the peak inductor current reaches its reference current level, determined by the voltage error signal *Verror*. The ramp waveform is no more generated by the oscillator.

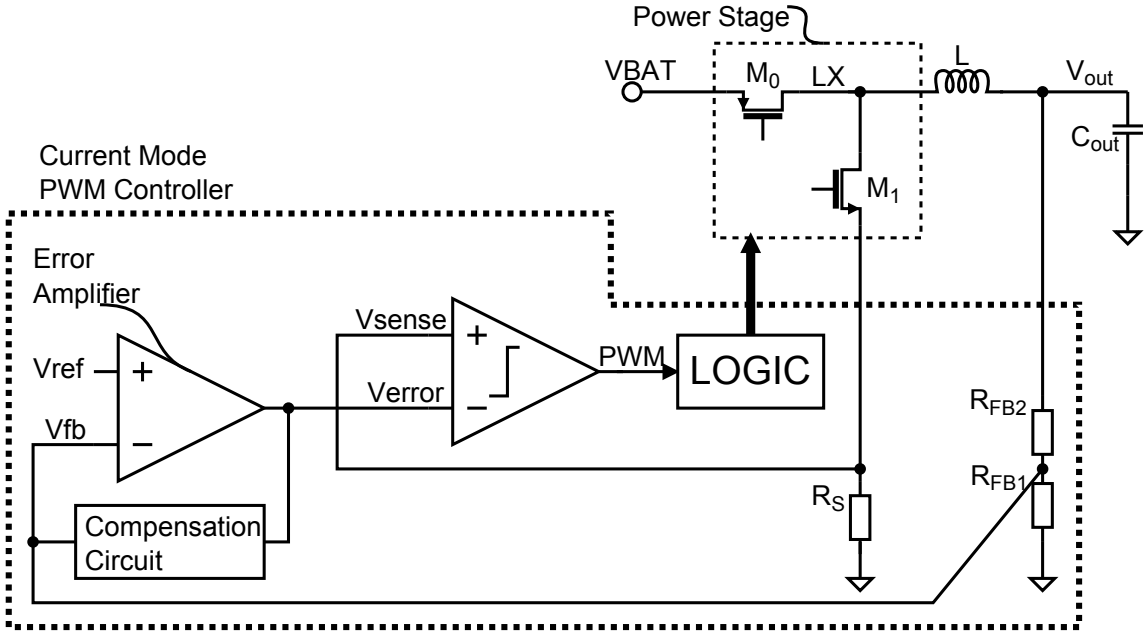



Figure 2.15.: Schematic of the peak-current mode regulation principle

Fig. 2.16 shows the waveforms of the signals in a peak-current mode PWM controller. The ramp carrier is replaced by a voltage image of the current flowing through the inductor. It is generated by using the clock pulses as the command for the charging of a capacitor at constant current [73].

The advantages of the peak-current mode regulation are [64]:

- Since the inductor current $I_L$ rises with a slope determined by the difference between $V_{in}$ and $V_{out}$, this waveform responds immediately to input voltage changes, elimi-

nating both the delayed response as well as the gain variation with changes in the input voltage.

- Since the error amplifier is now used to command an output current rather than an output voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop. This allows both simpler compensation and a higher gain bandwidth product over a comparable voltage mode circuit.

- An additional benefit of current mode regulation includes an inherent pulse-by-pulse current limiting by merely clamping the command from the error amplifier.

While the improvements offered by current mode regulation are impressive, this method also comes with its own unique set of problems, which must be solved in the design process. The disadvantages of the peak-current mode regulation are [64]:

- There are two feedback loops, making the circuit analysis more difficult.

- The control loop becomes unstable at duty cycles above 50% unless slope compensation to the voltage image of the inductor current is added.

- Since the control modulation is based on a signal derived from the output current, oscillations in the power stage can insert noise into the control loop.

While current mode regulation corrects many of the limitations of voltage mode regulation, it also creates new challenges for the design engineers. However, with the knowledge gained from the most recent developments in power control technology [66, 67, 68], a re-evaluation of voltage mode regulation indicated that there are efficient ways to correct its major weaknesses [69].

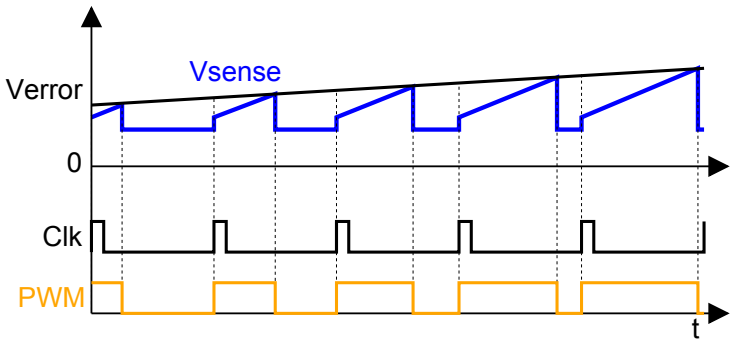



Figure 2.16.: Signal waveforms of the peak-current mode regulation principle shown in Fig. 2.15

**Hysteretic control -** A hysteretic control is a simple method for control of a DC-DC conversion circuit and it is the only mode that does not employ an error amplifier but consists of a hysteretic comparator [70]. Both hysteretic voltage mode and hysteretic current mode control exist. This hysteretic comparator senses the output voltage ripple and regulates it to within its hysteresis window by controlling the switching frequency and duty cycle of the power stage. This architecture is sometimes also referred to as a "ripple regulator" or "bang-bang controller" because it continuously shuttles the output voltage back and forth to just above or below the ideal set point. An example of a hysteretic mode buck converter is shown in Fig. 2.17.

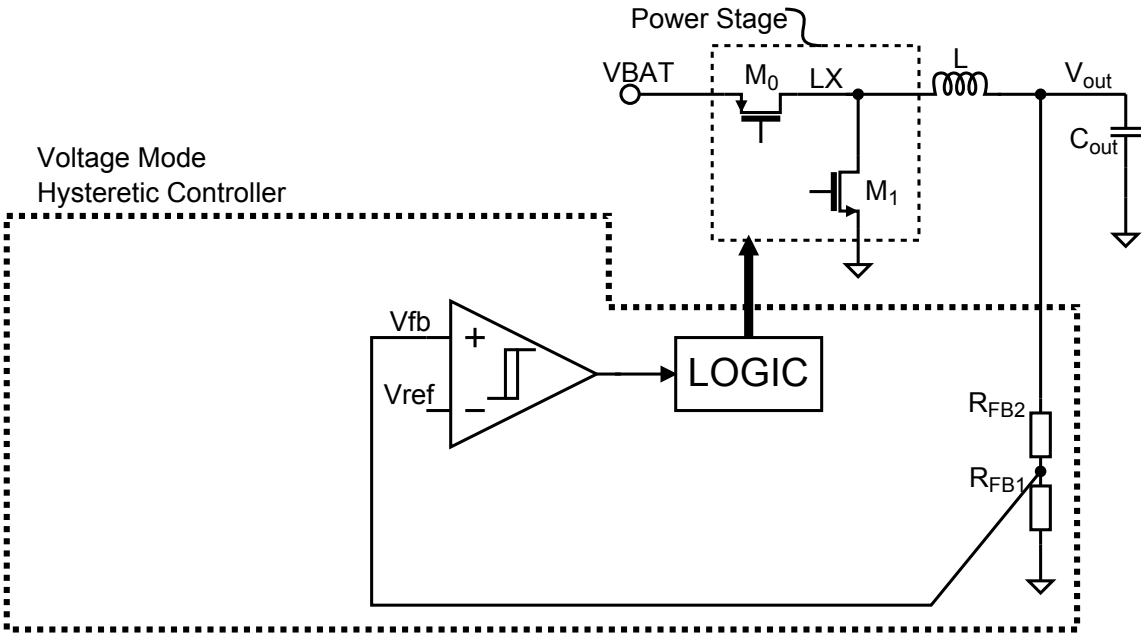



Figure 2.17.: Schematic of the hysteretic voltage mode regulation principle

The hysteretic voltage mode control is very simple to build since no oscillator is needed. The control loop responds very quickly to voltage and current changes in the line and load since it only depends on the propagation delay and not on waiting for the oscillator to start a new cycle. The structure is simplified and prevents instability. However, since no oscillator is present and the hysteresis architecture changes the control signal based on circuit operating conditions, the switching frequency is not constant. The hysteretic approach is, therefore, one type of PFM architecture. Not all converter topologies are adapted to be easily controlled by a hysteretic regulation.

# 3 Chapter
# Capacitor-less Linear Regulators

Conventional LDO regulators are in common use and they are still being developed [41, 42, 43, 44]. However, a considerable part of the current research of regulators aims at capacitor-less linear regulators [45, 46, 47, 48, 49, 50]. By removing an external capacitor of linear regulator we introduce new possibilities in power management like reduction of chip area, fewer pins are necessary and this leads to a decrease in the price of the whole system. The principle of developed capacitor-less linear regulators can be used to generate the internal supply voltage for the internal part of the switching converter and True Random Number Generator (TRNG) [51, 60]. This ensures protect against interference from the power supply and external attack in the case of TRNG.

On the Fig. 3.1 one can see that there is still a capacitor present at the output of a capacitor-less LDO regulator. But contrary to conventional LDO regulators (Fig. 2.4) (where the output capacitor is in the range of several microfarads) the value of this internal capacitor for capacitor-less LDO regulators is much smaller (in the range of several

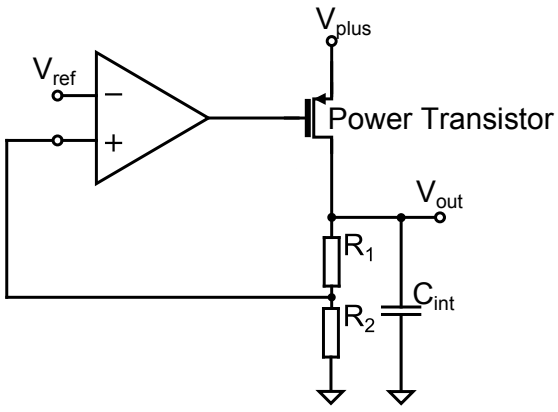



Figure 3.1.: Capacitor-less LDO voltage regulator [55]

hundred picofarads) and consequently, its transient properties are much worse. For this reason, it is necessary to implement enhancement structure (fast loops) to improve transient response.

## 3.1. PMOS capacitor-less LDO regulators

PMOS Capacitor-less LDO Regulator was the subject of my diploma thesis and in the follow-up doctoral studies, I continued to research in this field. The first part of this chapter is based on my diploma thesis [55] and is continuously followed by further research, verification, and validation in the area of the capacitor-less linear regulators.

### 3.1.1. Poles of capacitor-less LDO regulator

If we take into account a conventional LDO regulator and if we begin to decrease the value of the output capacitance, we find out that its properties fundamentally change. The result of making the output capacitance smaller and smaller can be especially seen on stability, its degeneration and also on fast load transient properties.

Fig. 3.2 depicts uncompensated capacitor-less LDO regulator together with its transfer characteristic. This LDO regulator has two main poles, the first one is caused by an output of an error amplifier, $P_1$, and the second pole is created by an output of the regulator, $P_2$ [48, 50].

The position of the first pole is described by equation 3.1 [50]. As it is apparent from the equation, the position of $P_1$ depends mostly on the output impedance of the error amplifier and also on equivalent input capacitance of the power transistor. For capacitor-less LDO regulator the first pole is located at relatively high frequencies.

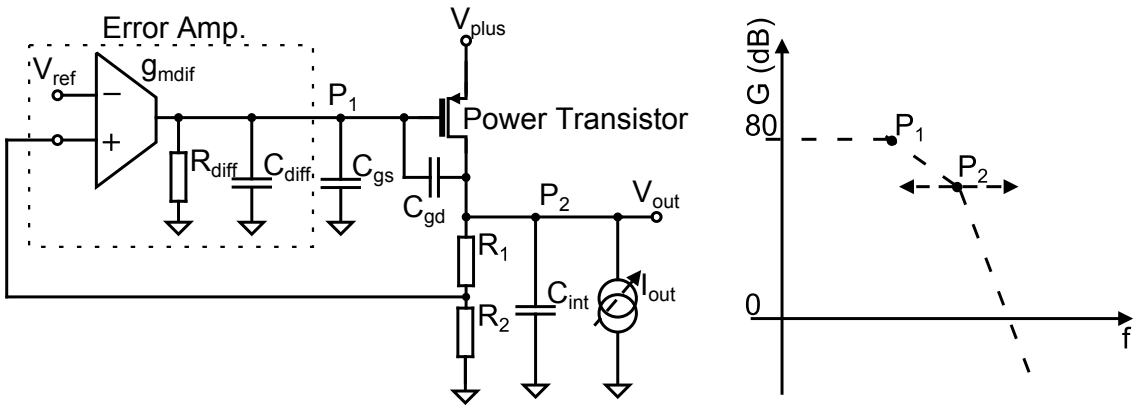



Figure 3.2.: Illustration of pole position for uncompensated capacitor-less LDO regulator [55]

$$\omega_{P1} = \frac{1}{R_{diff}\left(C_{diff} + C_{gs} + A_{power}C_{gd}\right)} \tag{3.1}$$

Where $R_{diff}$ and $C_{diff}$ are the error amplifier output resistance and error amplifier load capacitance, respectively, and $A_{power}$ is the gain of the power transistor. The position of the pole $P_1$ is not constant but it changes with changes of loading current. This is caused by the fact that the amplification of the power transistor changes with the loading current. But this dependence of the pole $P_1$ on the loading current is much smaller than at pole $P_2$.

$$\omega_{P2} = \frac{1}{C_{int}\left(R_{out}||R_{load}\right)} \tag{3.2}$$

The output of the LDO regulator creates second pole $P_2$. The position of this pole is described by equation 3.2 and movement of this pole is directly proportional to loading current. This is caused by the fact that output resistance decreases with increasing loading current.

Where $R_{load}$ and $C_{int}$ form load of LDO regulator and $R_{out}$ is the output resistance of the regulator. Capacitor-less LDO regulator is usually stable for large loading current range because this current pushes output pole $P_2$ into higher frequencies. On the other hand, at low loading current, the value of effective resistance increases rapidly and this brings the fact that pole $P_2$ moves towards lower frequencies and thus it gets to the proximity of the pole $P_1$. In such a case the stability of the regulator cannot be guaranteed. From this, we can conclude that uncompensated capacitor-less LDO regulator is not stable at low or non-existing load [50].

### 3.1.2. Design of a capacitor-less LDO regulator

The aim of this part of work is to design a capacitor-less LDO regulator for SoC applications. It is important for the circuit to be stable at all loading currents, mainly during small loading currents. Also, it is necessary that the circuit has acceptable reactions to the fast change of load.

For this reason, it is necessary to extend the circuit by fast loops, which will be responsible for fast response of the circuit and which will have greater bandwidth than the slow regulating loop. It is necessary to add these circuits due to the absence of an external loading capacitor.

The basic concept of the designed circuit is depicted in the Fig. 3.3. In the concept one can see a fast loop, that improves transient parameters of the circuit, and also slow loop is shown. This slow loop sets the required output voltage during the steady state or during slow change of an loading current [47, 48, 49, 50, 52].

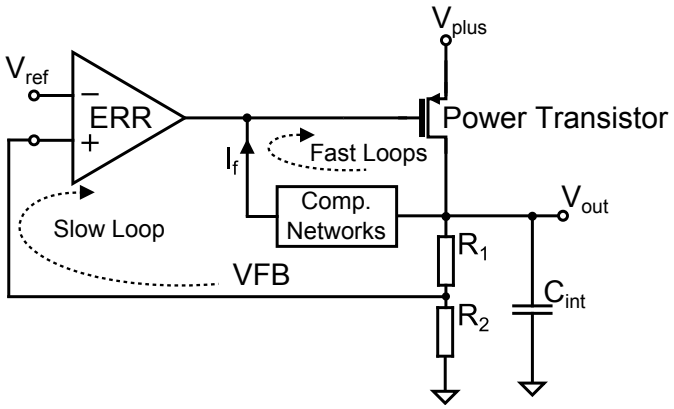



Figure 3.3.: Basic capacitor-less LDO concept [55]

On the other hand, the fast loop should react on the fast transient changes of loading current and as such to control changes in output voltage. Also, low consumption of the whole regulator belongs into aims of this work. It is from the reason that in power management more and more emphasis is laid on efficiency.

### Core of LDO

In the following part we will describe core of the circuit [52] (Fig. 3.4) and implementation of enhancement structure (Fig. 3.5), which are used for realization of the capacitor-less LDO regulator. The basis of the circuit is the power transistor ($M_{PT}$) similarly as the topology of classic LDO regulator. This type of regulator is like a voltage source which keeps the output voltage constant and independent of change in load or change of battery voltage. Current $I_{PT}$, which is controlled by gate voltage on the $M_{PT}$, is divided between the load ($I_{out}$) of LDO regulator and the transistor $M_5$ ($I_5$), as depicted in the Fig. 3.4.

Transistor $M_5$ similarly like the power transistor $M_{PT}$, works in saturating mode and a

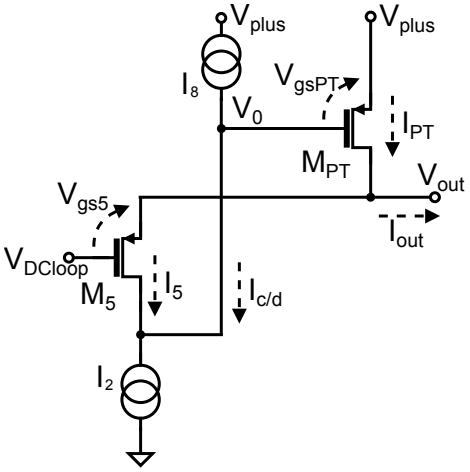



Figure 3.4.: The core of the capacitor-less LDO regulator [55]

control voltage from slow loop ($V_{DCloop}$) is applied to its gate. The current $I_5$, flowing through this transistor is dependent on the voltage $V_{gs5}$ ($V_{gs5} = V_{DCloop} - V_{out}$) and so we can say that it works as a comparator. The magnitude of the current, which flows from current source $I_2$, is constant and in the steady state given by a sum of currents $I_5$ and $I_8$, as depicted in the Fig. 3.4.

Like in the basic topology of LDO regulator, even here a loop of feedback closes at comparator. The feedback is used to set the output voltage. Adjustment is based on the fact that current from source $I_2$ is constant, therefore the change of the current $I_5$ causes a change of the current $I_{c/d}$, which has an influence on the amount of charge on the gate of the power transistor.

### Improving LDO regulator

The concept of LDO regulator, which was introduced in the previous part, needs to be rearranged in order to be realized in integrated form and also to improve its parameters like current consumption (Fig. 3.5).

To the most fundamental changes belongs adding a differential amplifier, which maintains required operation point of the whole regulator. What more, we added cascade transistor $M_6$. This transistor´s task is to keep such voltage on the gate of the power transistor, which allows the transistor to work in the saturated area. Furthermore, we added capacitive differentiator ($C_f$, $R_f$, $M_{10}$, $M_{11}$) [48, 49, 50], which compensates transient response, and finally a discharge transistor $M_7$ [52]. Fig. 3.5 depicts the elementary parts which we mentioned.

By adding differential amplifier into the concept of LDO regulator we created a series connection of two feedback loops. The previous loop, depicted in the Fig. 3.4, repre-

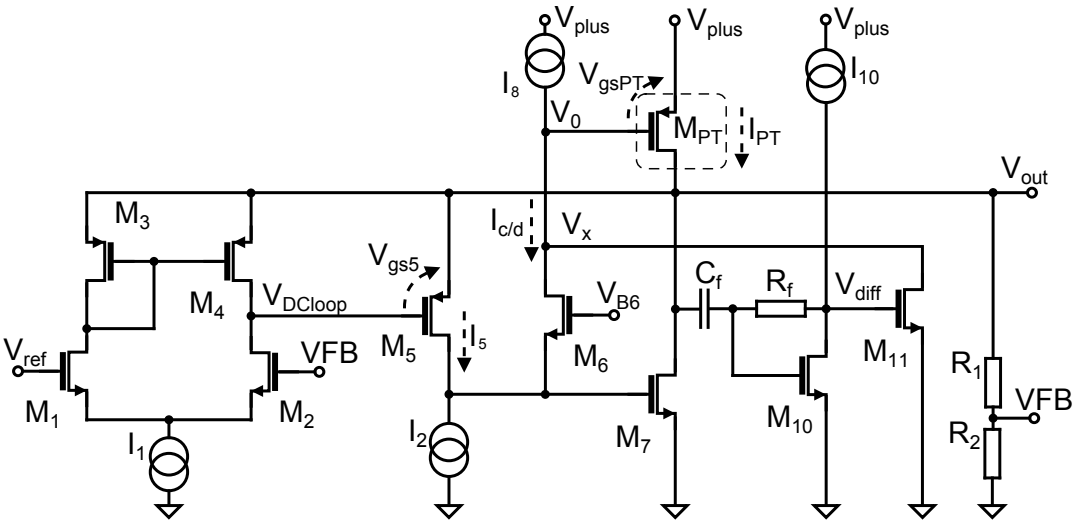



Figure 3.5.: Topology for proposed capacitor-less LDO voltage regulator [58]

sents series fast loop while the differential amplifier creates a slow loop. For improvement of PSRR (Power Supply Rejection Ratio) of the circuits, we used a possibility to supply differential amplifier directly from the output of LDO regulator.

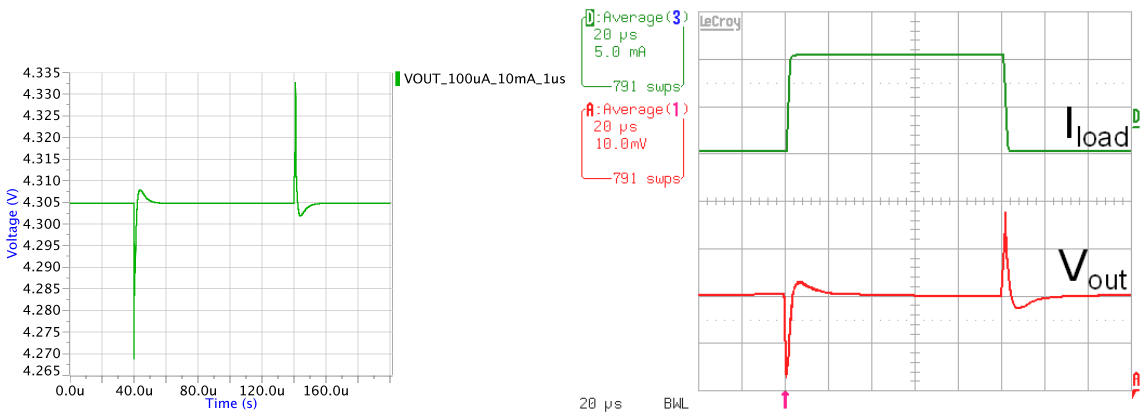
Subliminal mode of the power transistor significantly slows down the response of the circuit. This can cause degradation in voltage regulation for applications where loading currents drop to very low levels in a very short time. This degradation in the transient response of LDO regulator can be eliminated by adding a discharge circuit. This is another arrangement of circuits of the LDO regulator which should improve the transient response of LDO regulator during the fast decrease of loading current. Fig. 3.5 depicts principal connection of LDO regulator together with discharge transistor. This discharge circuit works only if regulating loop does not work in common mode but it is in saturation (during very fast changes of loading currents).

### 3.1.3. Achieved results

Part of the presented results in this section was published on the in EDS Conference [57] and the Student Conference POSTER [58].

#### Load transient

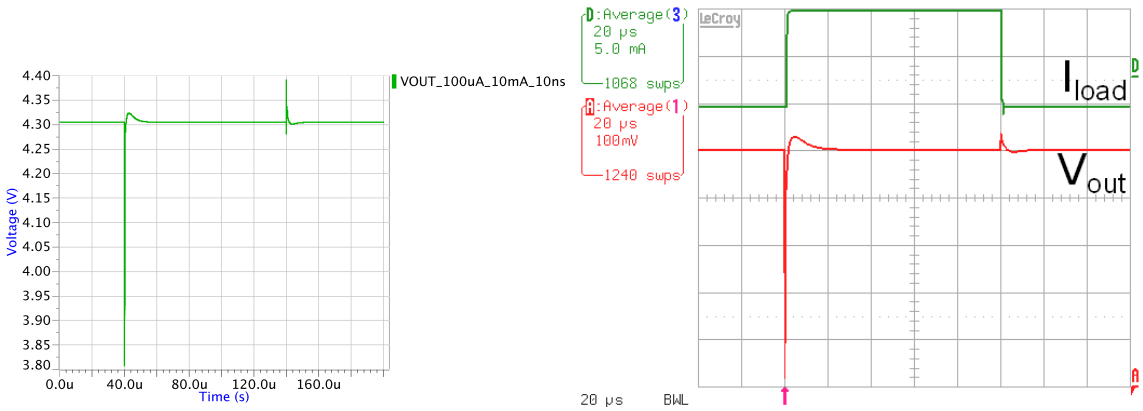
Fig. 3.6a depicts typical behavior of output voltage during a change of loading current from $100\,\mu A$ to $10\,mA$ with $t_{rise}$ resp. $t_{fall}$ $1\,\mu s$ which was obtained from the simulation. As can be seen the maximum deviation of the output voltage from the nominal value is $41\,mV$ for the typical case. This transient characteristic can be compared with the course, which was measured at the realized circuit (Fig. 3.6b). In this case, the maximum deviation is $20\,mV$




(a) Simulation [55]

(b) Measurement [57]

Figure 3.6.: Comparison of LDO transient response on the load step from $100\,\mu A$ to $10\,mA$ with $t_{rise}$ resp. $t_{fall}$ $1\,\mu s$




(a) Simulation [55] (b) Measurement [57]

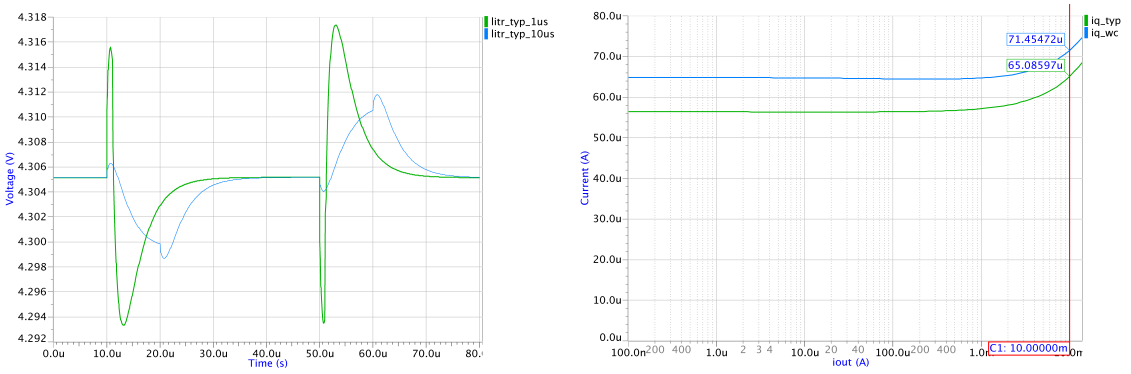
Figure 3.7.: Comparison of LDO transient response on the load step from $100\,\mu A$ to $10\,mA$ with $t_{rise}$ resp. $t_{fall}$ $10\,ns$

which is better than the result obtained in the simulation and shape is very similar.

Comparison of results for very fast load transient can be seen in Fig. 3.7a and 3.7b. Loading current is changed in the same way as it was in the previous case with the difference that $t_{rise}$ resp. $t_{fall}$ edge is now equal to $10\,ns$. In this case, the maximum deviation of the output voltage of the LDO regulator from its nominal value is equal to $496\,mV$ for simulation and $480\,mV$ for measurement. And how can one see from Fig. 3.7a and 3.7b measurement results approximate to simulation results.

### Line transient

The behavior of output voltage for the typical case during line transient can be seen in the Fig. 3.8a. Here, the maximum deviation of the output voltage from its nominal value is




(a) (b)

Figure 3.8.: Line transient, typical case, $step = 500\,mV$ in $1\,\mu s$ and in $10\,\mu s$ (a). Current consumption versus $I_{out}$, typical case and worst case (b) [55]

$13\,mV$ for the step of voltage equal to $500\,mV$ in $1\,\mu s$.

### Current consumption

Maximum current consumption of this LDO regulator is $72\,\mu A$ regardless of the load current. In the following Fig. 3.8b one can see the dependence of the total current consumption of LDO regulator on loading current. Here we have 2 curves; one represents dependence for the typical case and the other for the worst case at maximum loading.

### Layout

As mentioned above, the capacitor-less LDO regulator was created in $130\,nm$ CMOS technology. The layout of this structure is the important part of the whole design and is depicted in Fig. 3.9. The proposed LDO regulator contains two parts.

The external part (EXT) with dimensions$176\,\mu m x 50\,\mu m$ contains PMOS power transistor with channel width $750\,\mu m$ and channel length $0.5\,\mu m$, which is capable to supply continuously $10\,mA$, and internal output decoupling capacitors with the total capacity $53\,pF$. The first two capacitors are made as metal-insulator-metal (MIM) capacitors with a capacity of approximately $35\,pF$ and the third is a poly-silicon-N-well capacitor with capacitance $18\,pF$.

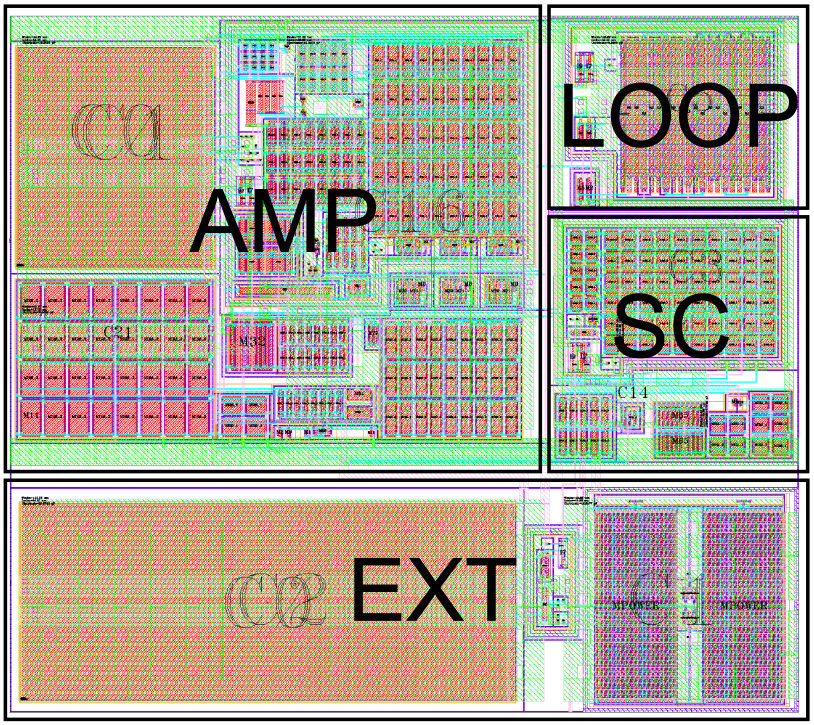



Figure 3.9.: Layout of capacitor-less LDO regulator [55]

The internal part (INT) with dimensions $176\,\mu m\,x\,100\,\mu m$ is bigger than EXT. INT contains input programmable resistor divider (LOOP), short circuit protection (SC) and operation amplifier with fast loops (AMP) that directly regulates PMOS power transistor. Very well matched structures can be found in AMP. For current mirrors, common centroid technique was used. The input differential pair was cross-coupled. In this way, parasitic resistances and capacitances are minimized.

### 3.1.4. Conclusions and future work

We introduced the capacitor-less LDO voltage regulator, which is capable of delivering $3.6\,V$ or $4.3\,V$ at loading currents up to $10\,mA$. This LDO voltage regulator does not require any external components and is stable in a wide load current range with a capacitive load up to $5\,nF$. Proposed capacitor-less LDO regulator was designed in collaboration between ST-Ericsson (Prague) and Czech Technical University in Prague and manufactured leveraging $130\,nm$ technology *HCMOS9A*.

Achieved results show that this capacitor-less LDO regulator has a fast transient response and low current consumption, approximating to $72\,\mu A$. The most important pa-

Table 3.1.: Comparison of results from simulation / post layout simulation (PLS) / measurement for proposed PMOS capacitor-less LDO regulator [58]

| | | | Simulation | | | PLS | Meas. | |
|---|---|---|---|---|---|---|---|---|
| ***Parameter*** | ***Name*** | ***Test conditions*** | ***Min*** | ***Typ*** | ***Max*** | ***Typ*** | ***Typ*** | ***Unit*** |
| Input supply voltage | $V_{plus}$ | $(V_{plus})-(V_{gnd})$ | 3.77 | 4.8 | 5.5 | | | $V$ |
| Output current | $I_{out}$ | | 0 | | 10 | | | $mA$ |
| Output voltage | $V_{out}$ | $VSEL =$ '0' | 3.583 | 3.6 | 3.626 | 3.6 | 3.606 | $V$ |
| | | $VSEL =$ '1' | 4.276 | 4.3 | 4.334 | 4.3 | 4.304 | |
| Expected | $C_{out}$ | | 0.1 | | 5 | | | $nF$ |
| parasitic load | $ESR$ | | 0 | | 250 | | | $m\Omega$ |
| Current consumption | $I_{dd}$ | $I_{out} = 10\,mA$ | | 65 | 72 | 63 | 60 | $\mu A$ |
| | | $I_{out} = 0.1\,\mu A$ | | 58 | 67 | 57 | 58 | |
| Line Transient | $Litr$ | $\Delta V = 500\,mV$ | | | | | | |
| | | $trise = tfall = 1\,\mu s$ | | 13 | 23 | 12 | | $mV$ |
| | | $-30°C to 125°C$ | | | | | | |
| | | $\Delta V = 500\,mV$ | | | | | | |
| | | $trise = tfall = 10\,\mu s$ | | 7 | 11 | 7 | | $mV$ |
| | | $-30°C to 125°C$ | | | | | | |
| Load Transient | $Ldtr$ | $I_{out}\,(in\,1\,\mu s)$ | | | | | | |
| | | $from\,100\mu A\,to\,10\,mA$ | | 41 | 72 | 44 | 20 | $mV$ |
| | | $from\,10mA\,to\,100\,\mu A$ | | 27 | 47 | 32 | 20 | |
| | | $-30°C to 125°C$ | | | | | | |

rameters (like Load transient) of the capacitor-less LDO regulator are shown in the Tab. 3.1, where parameters from the final circuit schematic simulation, post-layout simulation and measurement are depicted. This regulator offers a promising choice for the area, cost and power efficiency of SoC applications.

Next step in the evolution of this topology we will search for circuit implementation, which allows increasing the maximum load current without any negative impact on the transient response and quiescent current consumption. Another improvement of the circuit lies in the implementation of the low quiescent (LQ) mode and the ultra-low quiescent (ULQ) mode, which ensure a sufficiently reduce consumption for a low current load.

## 3.2. NMOS capacitor-less linear regulators

This section is based on the publication "Capacitor-less Linear Regulator with NMOS Power Transistor" [56] published in ElectroScope and [59].

The most significant element which has the greatest influence on the transient response of the linear regulator is the power transistor. This transistor delivers the required current into the load impedance which results in the required output voltage. A delay which is caused by the power transistor in the control loop is caused by the fact that gate capacitance of this power transistor represents the current-voltage converter. The greater gate capacitance, the greater is the delay. This delay has a dominant role in the entire delay of the control loop.

In conventional LDO regulators, a PMOS transistor (Fig. 2.4) is used in common source configuration as a power element. However, with this configuration, several disadvantages occur. The first drawback of using PMOS transistor is its lower mobility when compared to NMOS transistor. It means that the PMOS transistor needs a larger silicon area than NMOS transistor for comparable properties [53]. But this larger power transistor reduces the rate of charging / discharging of the input capacitance of its power transistor gate. Secondly, the output pole occurs at a relatively low frequency. It is due to fact that PMOS transistor is connected in a configuration called common source. This configuration has higher output impedance than the source follower configuration in the NMOS regulator (Fig. 2.4). For conventional LDO regulators, this adds an additional low-frequency pole whose frequency is dependent both on load resistance and output capacitance. To ensure the stability of a large external capacitor and another compensation circuit is needed. Other drawbacks associated with the low-frequency dominant pole are bandwidth limitation and the slow load regulation response. This can be enhanced by fast loops that increase regulator bandwidth [54]. Capacitor-less LDO regulator can be unstable for low load currents and therefore its operating range is limited.

All these disadvantages associated with the PMOS transistor can be eliminated by using the NMOS transistor. This power transistor is connected in a configuration known as a source follower. An important characteristic of this circuit is low output impedance, which means the output pole is placed at a high frequency. With this in mind we do not use the output pole as the dominant pole and thus we do not need an external capacitor. Moreover, because the NMOS transistor has greater mobility, for the same output current a significantly smaller area of silicon is required. On the other hand, even with the NMOS power transistor, several disadvantages are associated. One of the main drawbacks is that the gate voltage of power transistor must be at least by $V_{gssat}$ greater than the output voltage. This itself is not a problem, but in addition to the ever decreasing supply voltage, this leads to the fact that the supply voltage gets below the possible level of gate voltage. The result is

that the power transistor requires a charge pump. An alternative to raising the gate voltage is approach known as gate overdrive [52], which uses a floating voltage supply to elevate the control voltage into a range high enough to keep the NMOS pass element operating in the saturation region. The basic concept of the designed circuit is depicted in the Fig. 3.10. In that concept one can see a few fast loops, which improve the transient parameters of the circuit; also, a slow loop is shown [55].

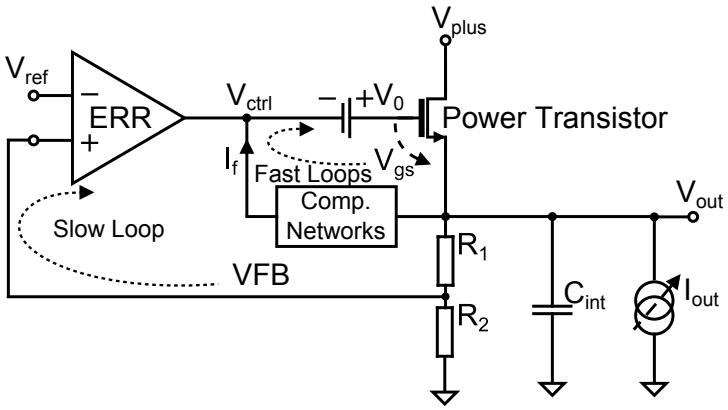



Figure 3.10.: Basic concept of capacitor-less linear regulator with NMOS power transistor [56]

### 3.2.1. Design of a NMOS capacitor-less linear regulator

In the following part we will describe core of the circuit (Fig. 3.11) and implementation of enhancement structure (Fig. 3.12), which is used for realization of the NMOS capacitor-less linear regulator. The core of this topology is similar to the core for capacitor-less LDO regulator which was described above. With the difference that for this topology we need to invert the control signal and it is also necessary to ensure that the gate voltage of power transistor must be at least by $V_{gssat}$ greater than the output voltage. To ensure this condition, the circuit uses the approach known as gate overdrive, which uses a floating capacitor to elevate the gate control voltage.

The basis of the circuit is the power transistor ($M_{PT}$) like with the topology of classic LDO regulator. This type of regulator is like a voltage source which keeps the output voltage constant and independent of change in load or change of battery voltage. Current $I_{PT}$, which is controlled by gate voltage on the $M_{PT}$, is divided between a load of the LDO regulator and the transistor $M_5$, as depicted in the Fig. 3.11. Current source $I_8$ delivers constant current, charging the gate capacitance of the power transistor. Transistor $M_5$ similarly like the power transistor $M_{PT}$, works in saturating mode and a control voltage from slow loop ($V_{DCloop}$) is applied to its gate. The current $I_5$, flowing through this transistor is dependent on the voltage $V_{gs}$ ($V_{gs} = V_{ref} - V_{out}$) and so we can say that it works as a

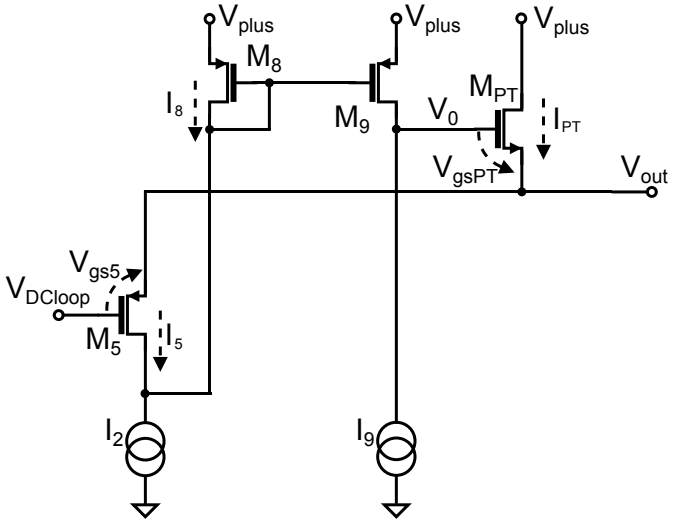



Figure 3.11.: The core of the NMOS capacitor-less linear regulator

comparator. The magnitude of the current, which flows from current source $I_2$, is stable and in the steady state given by a sum of currents $I_5$ and $I_8$, as depicted in the Fig. 3.11.

After a general introduction of basic elements in the circuit, we can describe the principle which this linear regulator works on. In the same way, as it is at the basic topology of the regulator, even here a loop of feedback closes via a comparator. The feedback is used to set the output voltage. Adjustment is based on the fact that current from source $I_2$ is constant, and the change of the current $I_5$ causes a change of the current $I_{c/d}$, which has an influence on the amount of charge on the gate of the power transistor and related gate voltage on the power transistor. As it was stated earlier, transistor $M_5$ regulates the amount of current $I_5$ which depends on the change of load. As it is apparent from the equation 3.3, the output voltage of the regulator, $V_{out}$, depends only on constants and on the current $I_5$.

$$V_{out} = \left(V_{ref} - V_t\right) - \sqrt{\frac{2I_5}{\frac{W_5}{L_5}\mu C}} \tag{3.3}$$

Even during the change of load, the current source $I_8$ still delivers constant current, which means, that gate voltage of the power transistor $V_0$ is controlled by change of current $I_{c/d}$. Thus the current which flows through the power transistor is controlled by the current $I_2$, resp. by the current $I_5$ thereby closing feedback.

The great advantage of this circuit is its speed due to the fact that the circuit works in a current mode. Simultaneously the circuit has one dominant disadvantage – great stand-by current consumption for an acceptable transient response. Maximum charging speed of the input gate capacitance of the power transistor is limited by current source $I_8$. The magnitude of the current, which is delivered by this source, is usually half of the $I_2$ current. The reason is that the charging/discharging of the power transistor gate need to have the

same maximum speed.

The circuit implementation of the proposed NMOS capacitor-less linear regulator is depicted in Fig. 3.12. Like in PMOS capacitor-less LDO regulator, we can see fast loops, which improve transient parameters of the circuit and also, a slow loop for the setting of DC operating point [55].

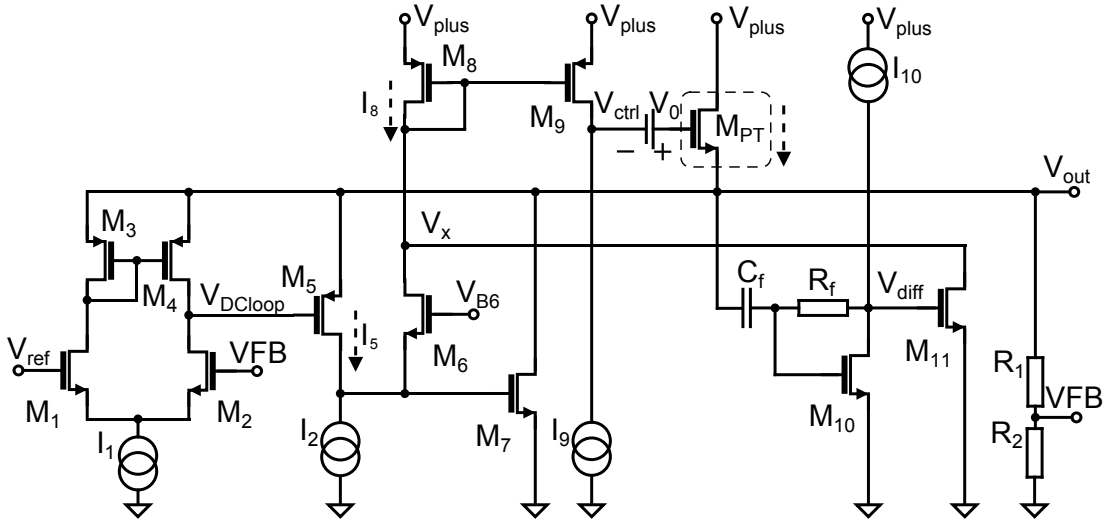



Figure 3.12.: Circuit implementation of the capacitor-less linear regulator with NMOS power transistor [56]

As shown in Fig. 3.12, the NMOS capacitor-less LDO control loop consists of the error amplifier, the floating voltage source, the power transistor, the compensation networks and the feedback network. The control voltage ($V_{ctrl}$) is raised above the supply level by a constant floating voltage source. In theory, the floating voltage source could be implemented as a charged floating capacitor. However, the voltage across the capacitor would drop due to its leakage current. This problem is solved by using two switched floating capacitors.

Like in previous regulator the PSRR (power supply rejection ratio) of the proposed regulator is improved by the fact that supply for the error amplifier is directly taken from the output of the regulator. The detailed circuit implementation of the differentiator block can be found in the right part of Fig. 3.12. When $V_{out}$ begins to rise, the differentiator senses this variation, and decreases the gate voltage $V_{diff}$ of transistor $M_{11}$. When $V_{diff}$ is low enough, $M_{11}$ will exit saturation region and $V_x$ will increase. In an opposite case, when $V_{out}$ begins to fall, the principle of regulation is inverse. Differentiator loop has one zero at frequency $0\,Hz$, and two poles, thus it is a stable loop. On the other hand, the large signal model of the differentiator block shows that the whole loop is working only when $V_{out}$ is rising fast enough.

The concept of the linear regulator, which was introduced in the previous part, needs to be rearranged in other to be realized in integrated form and also to improve its parameters

like current consumption.

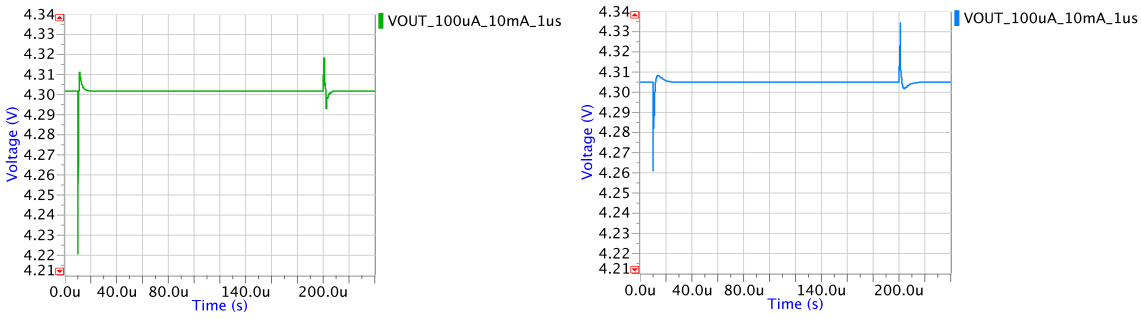
To the most fundamental changes belongs adding the differential amplifier, which maintains required operation point of the whole regulator. What more, we added cascade transistor $M_6$. Furthermore, we added capacitive differentiator($C_f$, $R_f$, $M_{10}$, $M_{11}$) [49] and [50], which compensates transient response, and finally a discharge transistor $M_7$ [52]. Fig. 3.12 depicts the elementary parts which are mentioned.

By adding differential amplifier into the concept of the regulator is created a series connection of two feedback loops. The previous loop, depicted in the Fig. 3.11, represents series fast loop while the differential amplifier creates a slow loop. For improvement of PSRR (Power Supply Rejection Ratio) of the circuits is used a possibility to supply differential amplifier directly from the output of the regulator.

Subliminal mode of the power transistor significantly slows down the response of the circuit. This can cause degradation in voltage regulation for applications where loading currents drop to very low levels in a very short time. This degradation in the transient response of regulator can be eliminated by adding a discharge circuit. This is another arrangement of circuits of the regulator which should improve the transient response of the regulator during the fast decrease of loading current. Fig. 3.12 depicts the principal connection of the regulator together with discharge transistor. This discharge circuit works only if regulating loop does not work in common mode but it is in saturation (during very fast changes of loading currents).

### 3.2.2. Comparison of results and future work

The proposed NMOS capacitor-less linear regulator was designed in a $0.13\,m$ CMOS technology. It provides a regulated output of $3.6V$ or $4.3V$. The regulator is designed for delivering a maximum output current of $50\,mA$ with a minimum drop-out of $100\,mV$. The



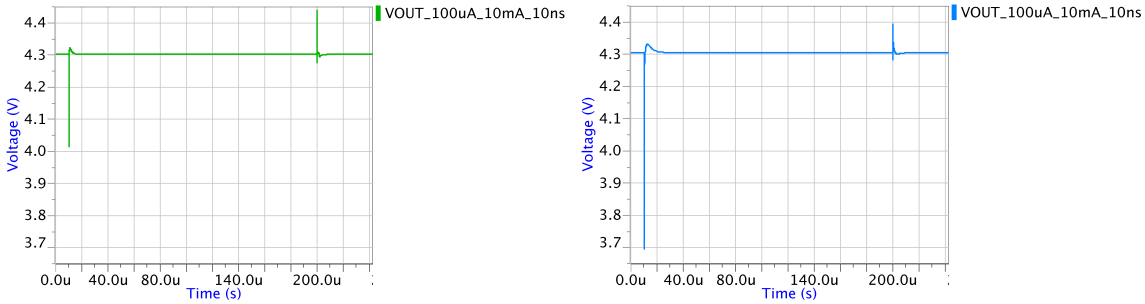

(a) NMOS capacitor-less linear regulator [56]

(b) PMOS capacitor-less LDO regulator [55]

Figure 3.13.: Comparison of transient response on the load step from $100\,\mu A$ to $10\,mA$ with $t_{rise}$ resp. $t_{fall}$ $1\,\mu s$

power transistor has a $W/L$ (width/length) ratio equal to $4000\,\mu m\,/\,0.5\,\mu m$. The maximum quiescent current of the regulator is $150\,\mu A$, which corresponds to less than $0.5\,\%$ of the maximum load current. The load regulation response of the regulator is tested by switching the load current from $100\,\mu A$ to $10\,mA$ and vice versa with $t_{rise}/t_{fall}$ edge $1\,\mu s$ (Fig. 3.13) resp. $10\,ns$ (Fig. 3.14). Maximum output voltage variation for typical conditions which was obtained from the simulation for NMOS capacitor-less linear regulator is about $76\,mV$ (Fig. 3.13a) and for PMOS capacitor-less LDO is about $41\,mV$ (Fig. 3.13b). One can see that for edge $1\,\mu s$ PMOS capacitor-less LDO has better results (variation of the output voltage is almost twice smaller than NMOS capacitor-less linear one). Opposite case occurs in the situation when $t_{rise}/t_{fall}$ edge is very fast ($10\,ns$). Variation of output voltage for PMOS capacitor-less LDO (Fig. 3.14b) is about $210\,mV$ higher than for NMOS capacitor-less linear regulator (Fig. 3.14a). Table 3.2 summarizes the performance of the proposed NMOS capacitor-less linear regulator and PMOS capacitor-less LDO regulator [55].

For a concept that is used to boost the gate control voltage of the NMOS power transistor, is necessary to find approach how to decrease the noise which is generated by this circuit. Like for the PMOS capacitor-less regulator, we need to implement both modes LQ and ULQ to decrease current consumption of the regulator for a low current load. And also it is necessary to validate and verify this NMOS regulator in the laboratory.




(a) NMOS capacitor-less linear regulator [56]

(b) PMOS capacitor-less LDO regulator [55]

Figure 3.14.: Comparison of transient response on the load step from $100\,\mu A$ to $10\,mA$ with $t_{rise}$ resp. $t_{fall}$ $10\,ns$

Table 3.2.: Comparison of simulation results between proposed NMOS capacitor-less linear regulator and PMOS capacitor-less LDO regulator [56]

| | | | NMOS linear regulator | | | PMOS LDO | | | |
|---|---|---|---|---|---|---|---|---|---|
| ***Parameter*** | ***Name*** | ***Test conditions*** | ***Min*** | ***Typ*** | ***Max*** | ***Min*** | ***Typ*** | ***Max*** | ***Unit*** |
| Input supply voltage | $V_{plus}$ | $(V_{plus}) - (V_{gnd})$ | 3.77 | 4.8 | 5.5 | 3.77 | 4.8 | 5.5 | $V$ |
| Output current | $I_{out}$ | | 0 | | 50 | 0 | | 10 | $mA$ |
| Output voltage | $V_{out}$ | $VSEL =$ '0' | 3.587 | 3.6 | 3.621 | 3.583 | 3.6 | 3.626 | $V$ |
| | | $VSEL =$ '1' | 4.283 | 4.3 | 4.3324 | 4.276 | 4.3 | 4.334 | |
| Expected parasitic load | $C_{out}$ | | 0.1 | | 5 | 0.1 | | 5 | $nF$ |
| | $ESR$ | | 0 | | 250 | 0 | | 250 | $m\Omega$ |
| Current consumption | $I_{dd}$ | $I_{out} = 10\,mA$ | | 100 | 135 | | 65 | 72 | $\mu A$ |
| | | $I_{out} = 0.1\,\mu A$ | | 100 | 142 | | 58 | 67 | |
| Load Transient | $Ldtr$ | $I_{out}\,(in\,1\,\mu s)$ | | | | | | | $mV$ |
| | | $from\,100\mu A\,to\,10\,mA$ | | 76 | 97 | | 41 | 72 | |
| | | $from\,10mA\,to\,100\,\mu A$ | | 16 | 27 | | 27 | 47 | |
| | | $-30°C\,to\,125°C$ | | | | | | | |
| | | $I_{out}\,(in\,10\,ns)$ | | | | | | | $mV$ |
| | | $from\,100\mu A\,to\,10\,mA$ | | 280 | 547 | | 591 | 890 | |
| | | $from\,10mA\,to\,100\,\mu A$ | | 107 | 297 | | 71 | 186 | |
| | | $-30°C\,to\,125°C$ | | | | | | | |

# 4 Chapter
# Current direction sensor for three-level flying capacitor converter

In today's world, the demand for new wireless communication services is growing every day. One of the direct consequences of this development is the growth of the networks which have to provide these services and one of the major problems is their energy consumption. The total efficiency of radio base stations for the first generation of the 3G network was just on the order of several percent's, and the efficiency of the PAs was less than 10% [61]. One of the main reasons for such a poor efficiency is the poor efficiency of the linear PAs which are used to transmit the signal.

Due to the rapid development of wireless communication technologies, the bandwidth has become very important. In order to increase the spectral efficiency, modern wireless communication techniques use digital communication protocols such as LTE, LTE-A, and WiMAX that use time variable envelopes. Given that these systems use the amplitude and phase modulation, it is necessary to use linear PA. Although this type of PA offers high linearity, its efficiency is low.

When the supply voltage is much higher than the signal's maximal amplitude, then a linear PA operates in the back-off region and this leads to degradation of the efficiency. Low efficiency means that a significant portion of the supply power is wasted, increasing cooling requirements, size of devices and at decreased lifetime portable devices. Having in mind that long lifetime is for portable devices very important, the problem of low efficiency of RF PA gains on its importance.

There are several techniques which are used to increase the efficiency and linearity of the RF PA. The envelope tracking technique (Fig.4.1) is a promising approach to improve the global efficiency of the RF transmission chain. It is based on the idea that the supply

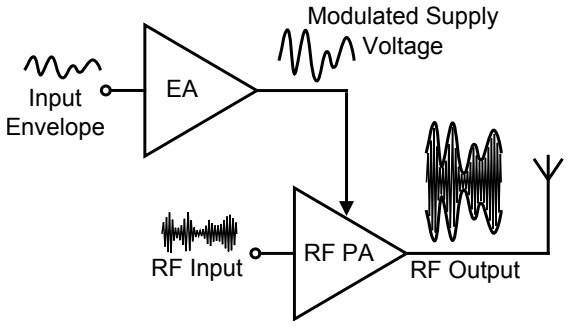



Figure 4.1.: Block diagram based on Envelope Tracking technique

voltage of the transmitter varies dynamically, according to the signal's envelope, but with certain excess in order to allow the RF PA to operate in a linear mode. The envelope and phase modulations are done through the linear RF PA, and the supply voltage is varied just to save the energy. This technique has raised interest in the optimization of the fast supply envelope modulator (EM), the most critical component in the system. Several topologies of the EM exist such as fast buck converters, multilevel buck converters [84] and parallel hybrid structures with a class-AB amplifier AC-coupled to a buck converter [85].

In AC-coupled architectures, the high PAPR envelope signal is decomposed into low and high-frequency (LF, HF) spectral components. The LF part that carries a larger portion of the power is efficiently provided by a switching buck regulator, whereas the remaining HF power is supplied by the less efficient class-AB amplifier. AC coupling gives the added benefit that instantaneous peak envelope voltages (higher than battery level) can be generated without requiring a dedicated boost converter. Nevertheless, this structure also has some drawbacks. Firstly, the class-AB amplifier becomes less efficient as the output power decreases. Secondly, as the DC output voltage cannot be boosted, the maximum average value of the PA supply stays lower than battery voltage [82].

## 4.1. Topologies for 4G PA

Firstly, it should be noted that the purpose of using any linearization technique such as ET technology is to improve the efficiency. For this reason, most of the designs are based on a buck topology because this topology is the best candidate to achieve a high efficiency.

There are known several different topologies, which can be used for implementation of the ET. In this section, commonly used topologies of the ET will be described, such as switching converter in parallel connection with a linear regulator, multiphase buck converter, and three-level flying capacitor converter [62, 83].

### Switching converter in parallel connection with linear regulator

This topology uses the advantages of both linear regulators (sufficient bandwidth) and switching converters (high efficiency). It is based on the parallel combination of a linear regulator with a switching converter [19, 62]. In this way, the slow dynamics, which is associated with a switching converter, is improved by the linear regulator. A simplified schematic of an ET implemented using a buck converter in parallel connection with a linear regulator is shown in Fig. 4.2. The main task of the regulator is just to give sufficient current (a small portion of energy, which is needed) in order to avoid distortion of the output envelope, while most of the required energy is supplied by switching converter.

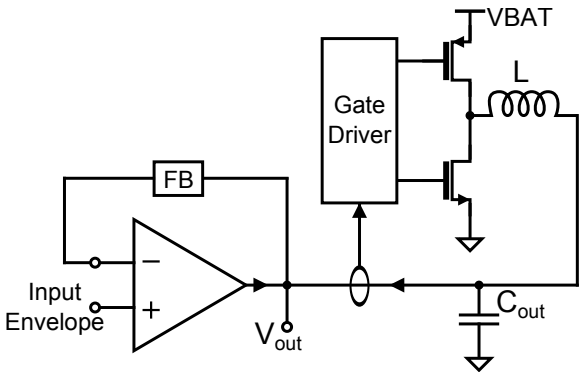



Figure 4.2.: Concept of the switching converter in parallel connection with linear regulator

The idea is based on the fact that each part of the ET should reproduce a certain part of the envelope's spectrum. Based on the analysis of the spectrum of envelope signal, it can be concluded that the major part of the envelope energy is included in the low-frequency components, which can be easily and efficiently reproduced by switching converter. The linear regulator, which has much lower efficiency than the switching converter, has to handle just a small portion of the energy, and its task is to reproduce part of high-frequency spectrum, which is necessary to achieve the correct envelope. With this approach, we can achieve both high linearity and sufficient bandwidth of the ET, but one of the main problems is the separation of the spectrum.

### Multiphase buck converter

Another topology which can be used is multiphase. In this topology, several switching converters can be interleaved like it is shown in Fig. 4.3 [62]. This leads to maximizing of the overall efficiency and minimizing of the output voltage ripple. Compared to a conventional buck converter, the ripple voltage is lower and canceled for duty cycles that are equal to a multiple of $1/N$, where $N$ is the number of phases. However, the ripple current in each inductor is usually larger because of the lower inductance. With the reduction of the

output voltage ripple it is possible to further reduce the inductance and capacitance of the output filter, which leads to improved dynamic behavior of the EA. One of the disadvantages of this topology is the possibility of unbalanced current sharing among phases and that the control becomes more complex with a higher number of phases. Also increasing the number of inductors raises the problem of magnetic coupling between the inductors, which is a major concern in multiphase topology.

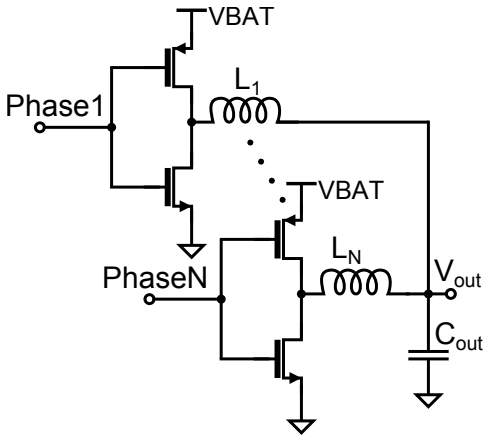



Figure 4.3.: Concept of the multiphase buck converter

### Three-level flying capacitor converter (FCC)

Three-level FCCs are usually employed as a solution for inverters, however it is also possible to use this topology for the ET [22, 62, 83]. This topology is an improved version of a regular buck converter where are four power switches ($M_1, M_2, M_3, M_4$) and flying capacitor; $C_{MID}$, which is connected between the nodes $TOP$ and $BOT$ (Fig. 4.4). The extra degrees of freedom in this type of converter can be used to improve the performance offered by a standard converter. The consequence is that the current ripple is reduced (or a smaller filter can be used) for the same power losses but at the cost of extra power switches and higher control complexity of the circuit. Another advantages of this kind of topology are a lower output voltage ripple, reduced harmonic distortion and lower electromagnetic concerns.

Among most of the solutions based on flying capacitor, this capacitor is approximately equally charged and discharged during one period of a sine wave and in that way, the voltage level used is roughly equal. However in the case of a nondeterministic signal, this equilibrium cannot be guaranteed and we need an additional control circuit to control the voltage on this flying capacitor. The control circuit is used for deciding which combination of switches to be used thereby achieving charging or discharging the flying voltage. However, if we do not know the period of the signal, it is very difficult to determine the correct combination of switches in order to achieve the required voltage level.

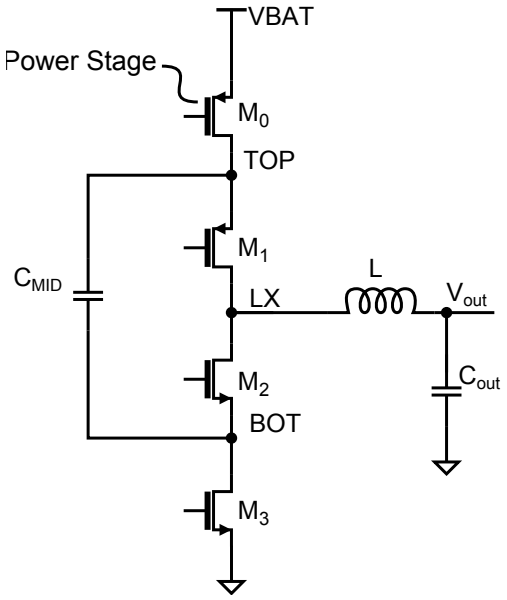



Figure 4.4.: Concept of the three-level buck converter

## 4.2. An apparatus for efficient regulation of the flying capacitance voltage in three-level FCC

This section is describing an integrate, high-speed and low-cost apparatus for the control of the flying capacitance in a multilevel converter [75] and my primary task on this apparatus was to design a sensor of current direction in the inductor. Parts of this chapter has been published in patent "Efficient regulation of capacitance voltage(s) in a switched mode multilevel power converter" [75].

Multilevel converter structures are known in power converter applications. Floating-capacitor converter topology, hereafter noted FCC, was introduced in 1992 [79] for inverter application. Advantages of this kind of topology are a lower output voltage ripple, reduced harmonic distortion and lower electromagnetics concerns [76]. For simplicity, we are going to discuss mainly the 3-level power converter with one flying capacitance, but the principle can be extended to any multilevel converter based on FCC topology.

As depicted in the Fig. 4.4, the 3-level power converter is constituted of 4 power switches. 2 high side switches, $M_0$ and $M_1$ and 2 low side switches, $M_2$ and $M_3$. A middle capacitance also called Flying capacitor in the literature; $C_{MID}$ is placed between the nodes $TOP$ and $BOT$.

The 3-level power stage can be configured in 4 operational configurations or states described in Table 4.1 and Fig. 4.5, given that $V(C_{MID})$ is equal to $VBAT/2$. Both states $S_1$ and $S_2$ are generating the level $VBAT/2$ on the $LX$ node. $S_1$ and $S_2$ are hereafter called redundant states.

| State | $M_0$ | $M_1$ | $M_2$ | $M_3$ | $V_{LX}$ |
|---|---|---|---|---|---|
| $S_0$ | ON | ON | OFF | OFF | $VBAT$ |
| $S_1$ | OFF | ON | OFF | ON | $VBAT/2$ |
| $S_2$ | ON | OFF | ON | OFF | $VBAT/2$ |
| $S_3$ | OFF | OFF | ON | ON | 0 |

Table 4.1.: Configurations of the power stage [75]

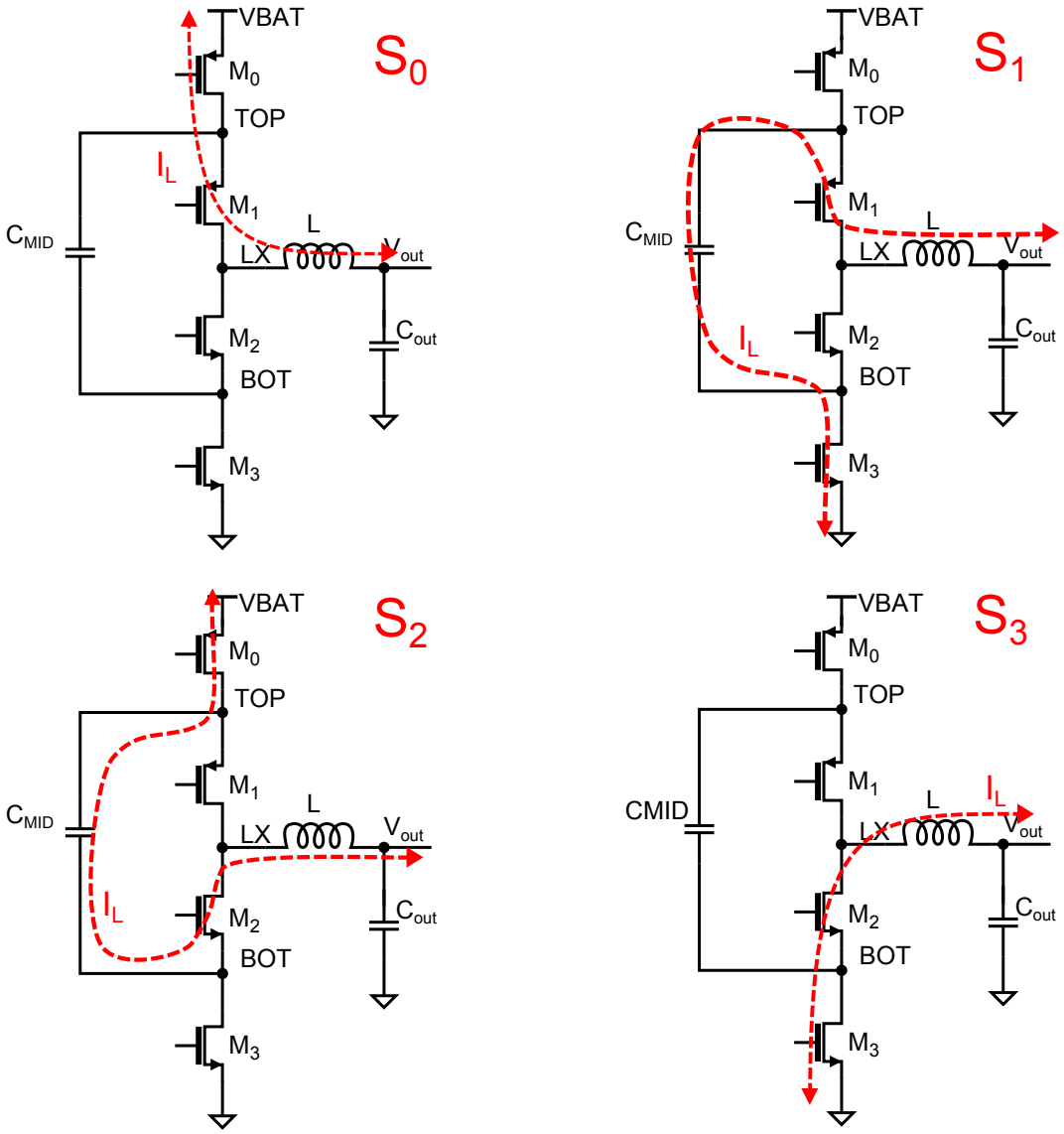



Figure 4.5.: States of three-level FCC [75]

The functionality of the FCC depends on the correct balancing of the flying capacitor. For a 3-level converter, the $C_{MID}$ capacitance has to be maintained at $VBAT/2$ voltage. Several methods have been introduced to address this function. In [81], "natural-balancing" techniques of FCC have been explored. Active regulation techniques such as modifying the duty-cycle or redundant state selection (RSS) have been described in the

literature. In [77], the flying capacitor voltage is maintained by adjusting the duty cycle according to the error between the measured voltage and a reference. In [78] a regulation technique for an N-level FCC is presented using RSS. In this regulation scheme, the presence of redundant state for generating some voltage levels ($VBAT/2$ in the 3-level case) is leveraged for the regulation of the flying capacitor. When several states are available to generate a given output level, some of the states will lead to charging the flying capacitance when other will lead to discharge. The charging/discharging property of a given state depends on the current polarity in the inductor. Thus based on the voltage level of the flying capacitance, the direction of the current in the coil and the voltage level to be generated on the output, it is possible to select the best state for maintaining the flying capacitor voltage level.

### Redundant state selection applied to the 3-level converter

Fig. 4.6 depicts the general block diagram of a 3-level converter RSS flying voltage regulator. In addition to the power structure already presented, it features a current direction sensor whose output is a Boolean information giving the direction of the current in the coil. This information, hereafter called *Il_dir* is log.1 when *Il* is positive and log.0 when *Il* is negative. The Boolean information whether the voltage across the $C_{MID}$ capacitor, *Vmid_lvl* is above or below $VBAT/2$ is generated by the $C_{MID}$ Voltage sensor block. *Vmid_lvl* is log.1, respectively log.0, when$V(C_{MID})$ is above, respectively below, $VBAT/2$ level. A controlling part of the system is generating the command of which level shall be generated on the *LX* node. This command signal is called PWM. PWM signal can take three values: 0, 1 or 2 giving the command to set the *LX* node to respectively 0V, $VBAT/2$ or $VBAT$. A state selection circuit is in charge, based on *Il_dir*, *Vmid_lvl,* and PWM to set the power stage to the right state. The decision is made based on Tab. 4.2.

| PWM | *Il_dir* | *Vmid_lvl* | State |
|---|---|---|---|
| 0 | X | X | $S_3$ |
| 1 | 0 | 0 | $S_1$ |
| 1 | 0 | 1 | $S_2$ |
| 1 | 1 | 0 | $S_2$ |
| 1 | 1 | 1 | $S_1$ |
| 2 | X | X | $S_0$ |

Table 4.2.: State selection circuit decision table [75]

Applying this algorithm to the 3-level converter will result in a regulated voltage on the $C_{MID}$ capacitance. This behavior is illustrated in Fig. 4.7. In this figure, it is assumed that the $V_{out}$ node is connected to a grounded capacitance. An algorithm as described in [78] can then be used to determine which state should be chosen based on:

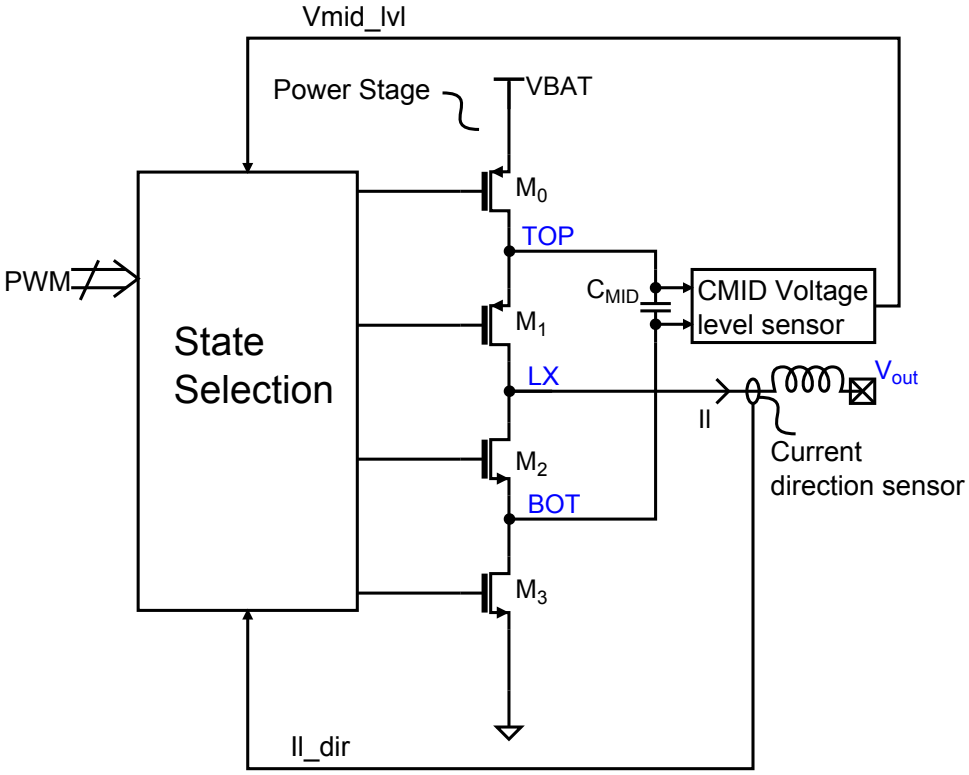



Figure 4.6.: 3-level converter RSS regulation circuit [75]

- The value of the PWM signal
- The direction of the current in the coil
- The relative value of each flying capacitor versus its reference

### 4.2.1. Problems with existing solutions

FCC Technique has been developed mainly for power inverters. Thus for the application running with discrete switching elements under voltages of several hundreds of Volts and switching frequencies in the range of 1 to $10 kHz$.

The computing part linked to the regulation is usually implemented in a DSP or a PC, the current sensing in the coil is performed with discrete Hall Effect sensors and DACs are ensuring the conversion of analog signals to digital.

In the scope of using those types of converters as power-supply for RF Power Amplifier in envelope tracking application inside mobile communication devices, it is required that the control system is fulfilling the following requirements:

- High speed: The switching frequency of mentioned power supplies is in the range of $50-200 MHz$.

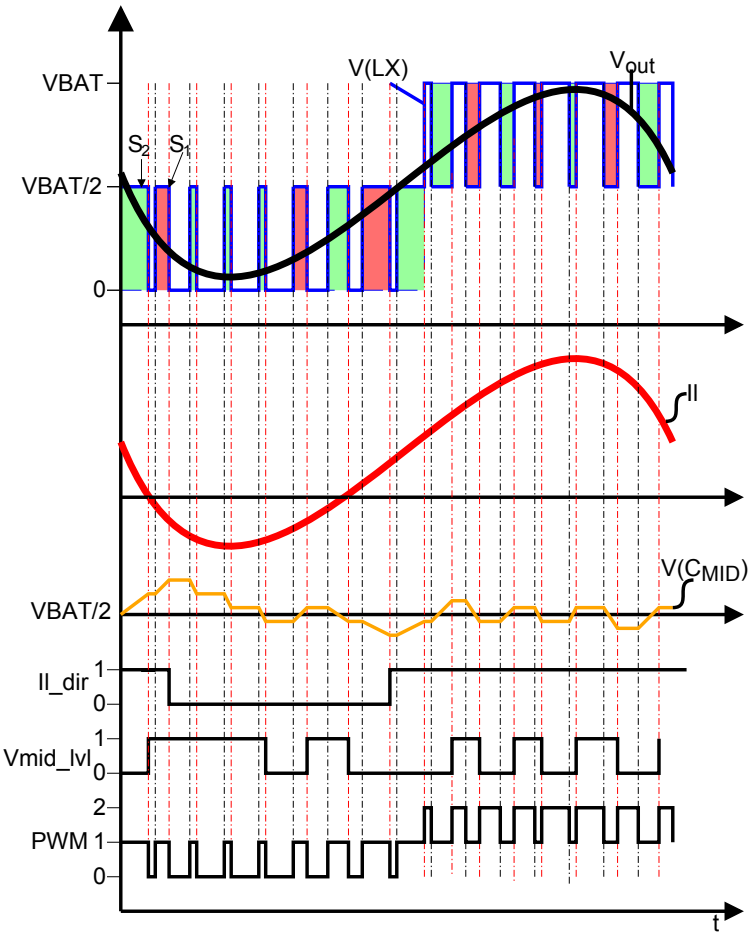



Figure 4.7.: RSS algorithm applied to 3-level converter [75]

- Low cost: The control solution should fit in the reasonable area of an integrated circuit or IC to fit both price and footprint constraints.

The two previous constraints are disqualifying the Hall Effect sensor, DAC, and DSP which are large and costly solutions.

### 4.2.2. Detailed description

The proposed apparatus is aimed at implementing the functions described as $C_{MID}$ level voltage sensor and $Il$ current direction sensor in Fig. 4.6. The basic principle of the proposed solution is based on the indirect measurement of the coil current through the voltage drop, generated on the power switches. For the $C_{MID}$ voltage sensor, a combination of differential configured operational amplifier and comparator is proposed. Fig. 4.8 depicts the embodiments of the circuit:

- An operational amplifier in a differential configuration, Vmiddle Buffer, converting the flying voltage $V(C_{MID})$ to a single-ended analog signal: *VmidBuf*.

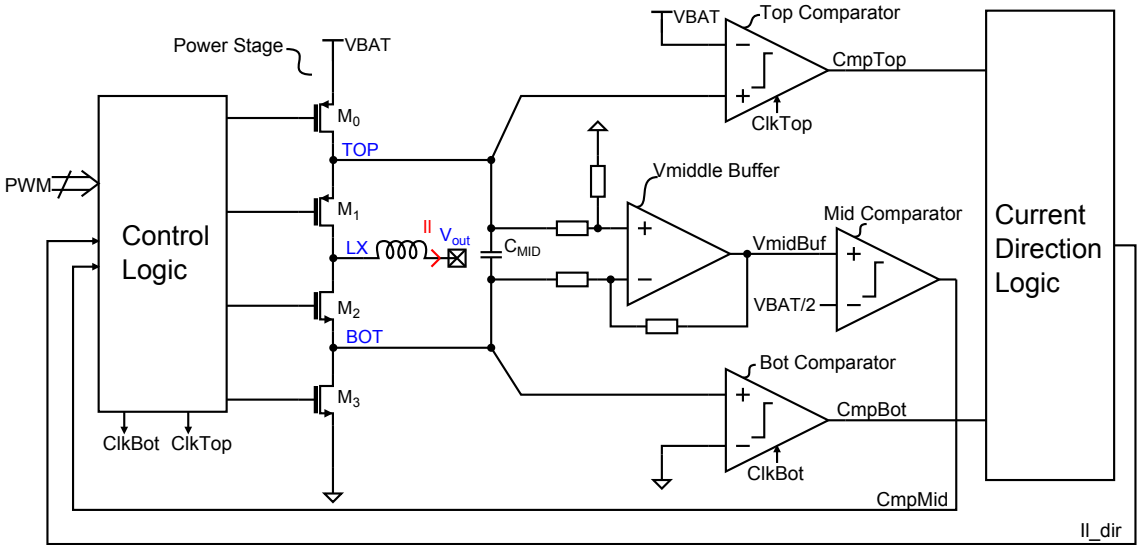



Figure 4.8.: Block diagram of the proposed circuit

- Two triggered comparators, Top Comparator, and Bot Comparator respectively comparing $TOP$ with $VBAT$ and $BOT$ with $GND$.
- A comparator comparing $VmidBuf$ with $VBAT/2$ : Mid Comparator.
- A first logic circuitry (current direction logic) determining the direction of the current in the coil based on $TOP$ and $BOT$ comparators outputs. Its output is *Il_dir*.
- A second logic circuitry (Control logic) generating the commands of the power switches and the Top and Bot comparators clocks based on PWM, the output of the Mid Comparator and *Il_dir*.

### CMID voltage sensor

The Vmiddle buffer, an operational amplifier connected in differential configuration, is translating the flying voltage $V(TOP, BOT)$ to a single-ended voltage *VmidBuf*. The signal *VmidBuf* is then compared with $V_{bat}/2$ by the Mid Comparator. The output of this comparison, logical signal *CmpMid* is providing the Control Logic with the information whether $V(C_{MID})$ is above or below $VBAT/2$, and thus if it should be charged or discharged.

### Current direction sensing circuitry

The switches $M_0, M_1, M_2, M_3$ have a non-zero resistance when turned-on, hereafter called $r_{on}$. Thus when the inductor current is passing through them, it is inducing a voltage drop in the amount $Il * r_{on}$ across the switch. So when $M_0$ ($S_0$ and $S_2$ states) is conducting and $Il$

is positive, the quantity $V(TOP, VBAT)$ is negative. Then if Top Comparator is triggered, *CmpTop* will output log.0. Similarly, if Il is negative, $V(TOP, VBAT)$ is positive and *CmdTop* outputs log.1.

In case $M_3$ is conducting ($S_1$ and $S_3$ states), The quantity $V(BOT, GND)$ polarity is directly linked to $Il$ polarity. At ClkBot rising edge, depending on whether $Il$ is negative or positive, *CmpBot* will output respectively log.1 or log.0.

The current direction logic then processes the *CmpTop* and *CmpBot* and based on which state was the last used ($S_0$ and $S_2$ for *CmpTop*, $S_1$ and $S_3$ for *CmpBot*), will generate a signal giving the direction of the current in the coil *Il_dir*.

This behavior is illustrated in Fig. 4.9. This current sensing circuitry present the advantage to prevent using a Hall Effect probe or a sensing resistor which are techniques requiring external components and thus increasing the cost. A second advantage is a speed at which the decision can be made, triggered comparators being components compatible with operation in the $100MHz$ range.

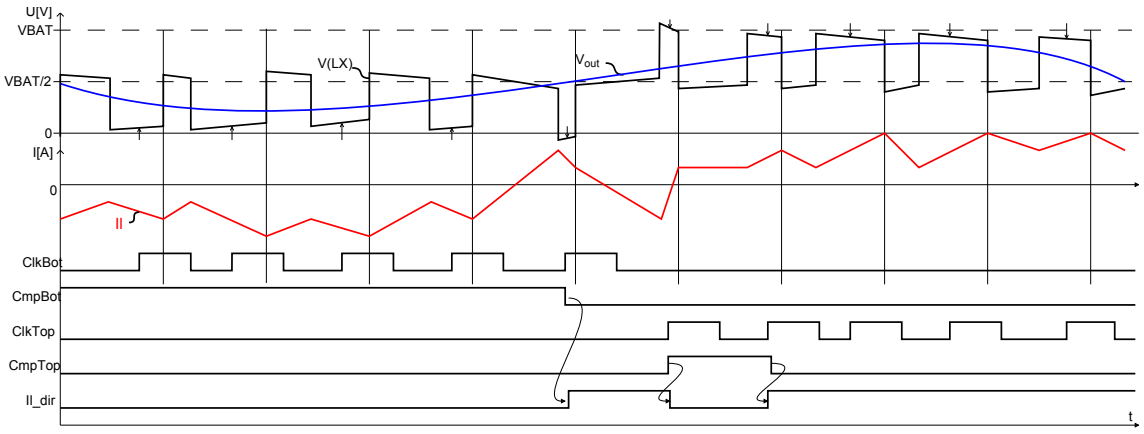
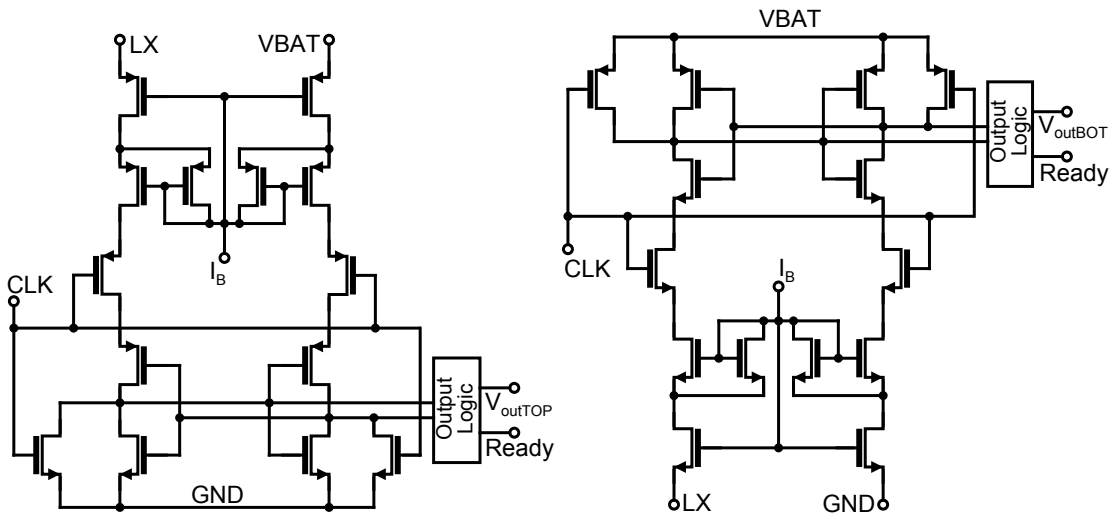



Figure 4.9.: Sensing circuitry operation [75]

Two designed triggered comparators, Top Comparator (Fig. 4.10a) resp. Bot Comparator (Fig. 4.10b) comparing *LX* node with *VBAT* resp. *GND*. Requirements to be met by triggered comparators are as follows:

- Low delay, due to the operating switching frequency of the converter
- A low offset, because $r_{on}$ of power switching is relatively small and thus the voltage drop, which is used for current direction detection in the order of several tens of $mV$ depending on the value of current. This offset causes incorrect detection of the current direction.
- Immunity of the inputs comparators: due to the fact that the inputs of comparators are connected to *GND* resp. *VBAT* and especially *LX* node.On the node *LX* may




(a) Top Comparator (b) Bot Comparator

Figure 4.10.: Simplified schematics of the proposed triggered comparators

appear voltage in the range from $VBAT + 2V_D$ to $GND - 2V_D$ , where $V_D$ is the diode voltage created between the drain and body of the power switch.

## 4.3. Example of use for a three-level FCC

As an example of usage and implementing a three-level FCC, there are presented the results of the project „Envelope Modulator for Multimode Transmitters with AC-Coupled Multilevel Regulators“ [82] on which I cooperated with colleagues from ST-Ericsson and STMicroelectronics. On this project, I have been working on circuits for three-level FCC buck regulator - fast regulator ( Fig. 4.11). Namely on the above mentioned triggered comparators for current direction sensor, on the input reference converter which converts differential input signal *Vref* into a single-ended signal, on the fast comparator for PWM and finally on double edge, double ended ramp generator which generates a triangular linear ramp up to $70MHz$.

The above-mentioned three-level FCC was used in EM design for the ET technique. In this case, parallel AC-coupled switching converters were used that improve both high and mid-range power efficiency. This modulator is composed of two switching regulators:

- Three-level FCC buck regulator - fast regulator
- Buck-boost converter - slow regulator

The complete modulator has been designed to supply multimode transmitters. Besides ET operation, it is compatible with both 3G/4G average power tracking (APT) operation

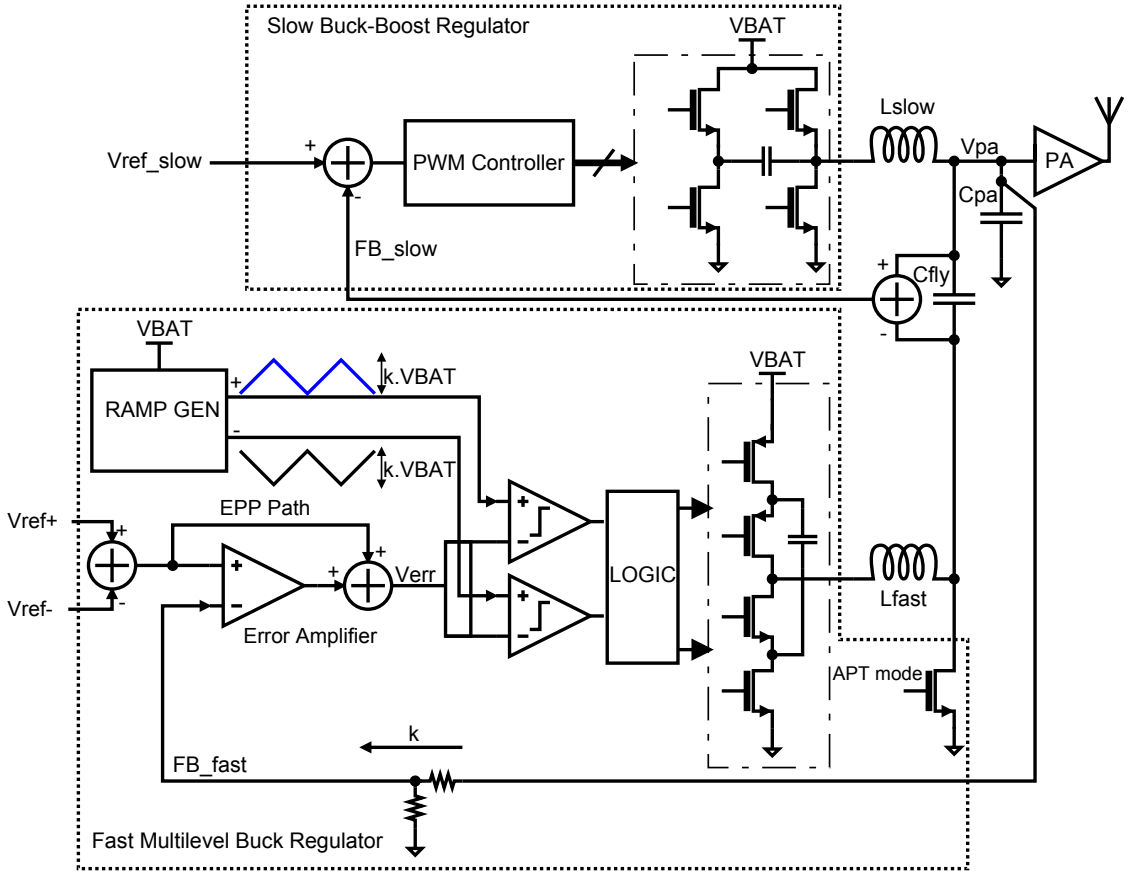



Figure 4.11.: Envelope Modulator architecture [82]

and GSM power ramping. The architecture of the parallel AC-coupled EM shows Fig. 4.11. When the system is configured for ET operation, the fast regulator output is controlled by the differential envelope reference *Vref*. On the other hand, the slow regulator is configured to regulate the voltage across the AC-coupling capacitor (*Cfly*) according to *Vref_slow* reference. The slow regulator feedback signal (*FBslow*) is originated by sensing the voltage across *Cfly*. Thanks to the differential sensing, *FBslow* signal has only a DC component and the loop does not require an additional low-pass filter to remove the AC part of the modulation. Both fast and slow loops use voltage-mode regulation and the pairs *Lslow*, *Cfly* and *Lfast*, *Cpa* are their respective LC output filters. Moreover, $Cfly \gg Cpa$ and $Lslow \gg Lfast$. The multilevel fast regulator power stage can switch between ground, $VBAT/2$ and $VBAT$, whereas the slow regulator can switch between ground, $VBAT$ and $2VBAT$. When needed, the system can be reconfigured for APT operation and, in this case, only the slow buck-boost regulator stays on while the APT switch shunts the bottom plate of *Cfly* to ground. Thus, the inductor *Lslow* and capacitor *Cfly* form its output LC low-pass filter. The PA supply voltage *Vpa* is sensed by the feedback and the voltage-mode PWM controller produces a constant output voltage at *Vpa* proportional to the reference voltage *Vref_slow*.

There are several advantages of using a three-level power stage instead of a standard two-level architecture. Firstly, switching losses are lowered by a factor of 2 [86]. Furthermore, the current ripple in the output coil is divided by 2 and lastly, the output voltage ripple is attenuated by a factor of 4, leading to an improved frequency spectrum [84].

The controller of the fast regulator employs a voltage-mode PWM scheme extended with an end-point prediction (EPP) path. There are several benefits of this fixed-frequency control scheme over variable-frequency ones such as lower near-channel noise, well-controlled spurious frequencies and a linear transfer function from PWM modulator input to output voltage [87]. In this architecture, the differential input reference *Vref* is converted into a single-ended signal that becomes the reference for both the parallel-connected EPP path and the error amplifier. For a PWM controlled buck converter, the duty cycle can be estimated knowing *Vref*, $VBAT$, and $k$, the ratio *Vref/Vpa*. In our system, this estimation is performed by the EPP through a feed-forward path from *Vref* to *Vpa* as shown in [87]. In addition to this open-loop path, a standard proportional, integral, derivative (PID) closed loop compensation inside the error amplifier ensures the stability of the fast regulator. Outputs of the EPP path and error amplifier are summed into a *Verr* signal. The comparison of *Verr* with two 180°-shifted triangular ramps results in 2 PWM signals having the same duty cycle but opposite phases. Each signal drives one pair of power switches $M_0$, $M_3$ and $M_1$, $M_2$ as in [84]. Furthermore, the 2 ramps used for modulation are proportional to $VBAT$ variations, leading to an additional direct feed-forward to the PWM signals, which ensures the independence of the regulator loop gain from $VBAT$.

The EM has been designed and manufactured leveraging $130nm$, 4.8V, n-well CMOS technology known as HCMOS9A.

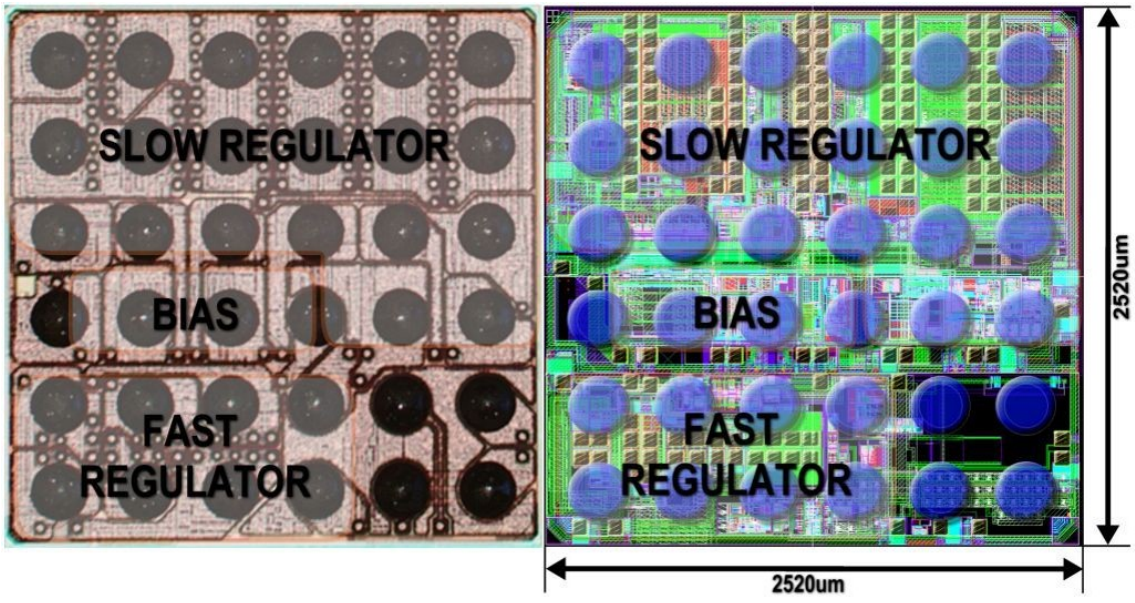



Figure 4.12.: Micrograph and layout of the EM [82]

The package is a 400 $\mu m$ pitch wafer level chip scale package (WLCSP). A micrograph and layout are shown in Fig. 4.12. The Slow buck-boost regulator operates from 1.9 $MHz$ to 7 $MHz$ (2 $MHz$ typ), whereas the switching frequency of the fast regulator can reach up to 140 $MHz$ (80 $MHz$ typ).

An LTE 10MHz (6.7dB of PAPR) test signal is used for all the measurements. Fig. 4.13 shows measured waveforms of the envelope reference signal (*Vref_scaled* - delayed and scaled to *Vpa*) and modulator output voltage with resistive load *(Vpa)*. Fast modulator three-level output (*Vlx_fast*) is also presented.

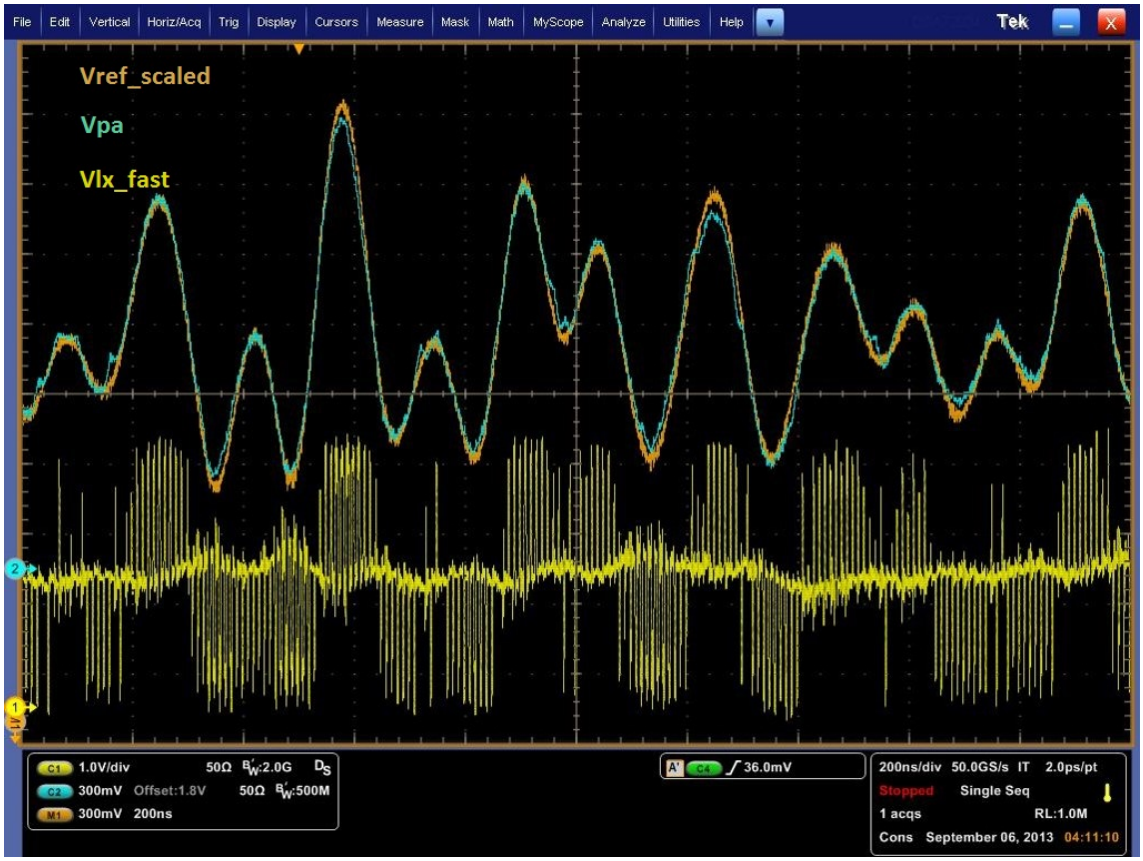



Figure 4.13.: Tracking performance for LTE10 signal [82]

# 5 Chapter
# Dual Edge Ramp Generator

The following sections deal with the new dual edge single ended ramp generator concept. Switching DC-DC converters (e.g. Buck) with voltage-mode PWM controller (Fig. 5.1) are widely used as basic building blocks for portable devices due to their high power efficiency [88]. Due to the increasing demands (e.g. switching frequency, phase selection, low current consumption and good regulation of these regulators) we need to develop new design approaches, which will bring the required properties. One of the essential blocks in the PWM controller is the ramp generator. We can improve the performance of the whole system by designing a precise ramp [88, 90, 92, 93, 94], which will be proportional to the input voltage (to generate feedforward effect), to decrease the current consumption (by excluding the comparators from this block) and significantly increase ramp frequency by omitting the comparator's delays [90, 93].

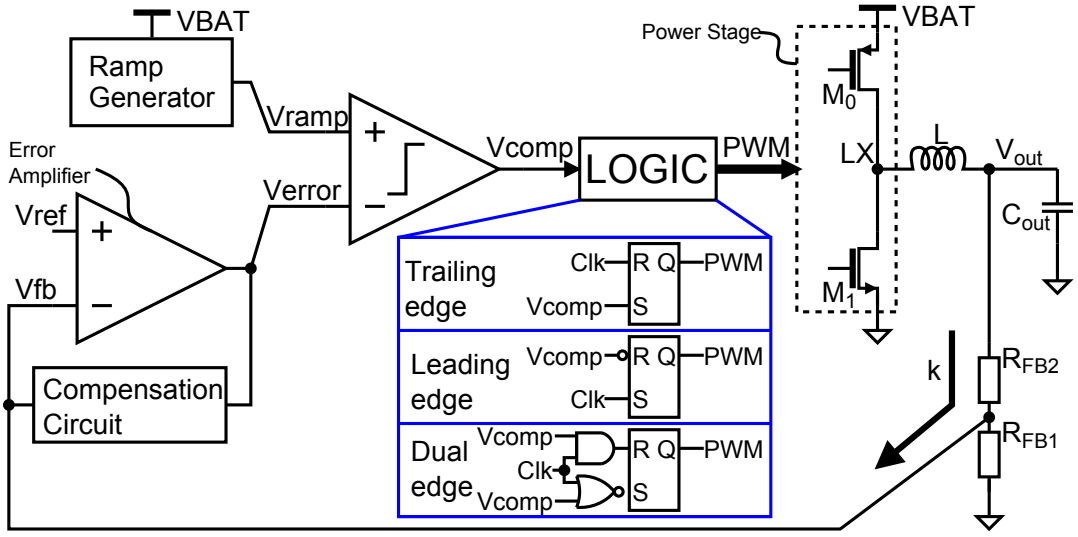



Figure 5.1.: Buck converter with voltage-mode PWM controller

## 5.1. Basic idea of the ramp generation

We can choose one of the following modulation techniques for PWM modulation: leading edge, trailing edge or dual edge modulation (Fig. 5.2) [95, 96, 97, 98]. The most suitable solution for high-frequency applications is the dual edge modulation, because the unavoidable delay of the PWM comparator is not generating error in the duty cycle if the rising and falling delay are similar. With the leading or trailing edge modulation, the error would be significant, as can be seen from the Fig. 5.2.

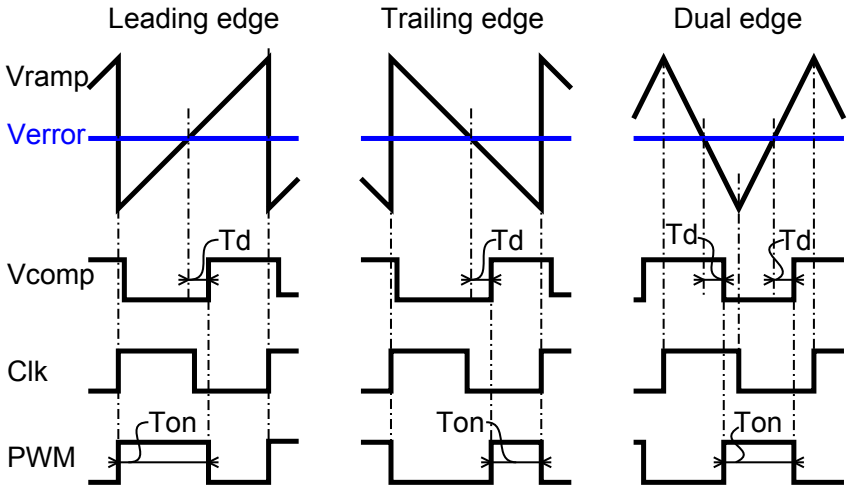



Figure 5.2.: PWM modulation wave

Another advantage of this ramp shape is that it helps to improve transient characteristics of the system by creating the desired output waveforms. This is due to the fact that, the error signal (*Verror*) is sampled twice every period. Also high speed edges are avoided thanks to the fact that the discharge current peaks [88], created by the generator with the output signal form of the saw, disappear.

## 5.2. Proposed ramp generator principle

The core and concept of the proposed ramp generator is shown in Fig. 5.3, where a capacitor $C_0$ is alternatively charged and discharged by a constant current $I$ for an equal duration, resulting in a triangular voltage across the capacitor. Originality of the design of the saw tooth signal generator consists mainly in the use of new control loops, ensuring a low power consumption in a wide range of operating frequencies. This is due to the fact that comparators are not used in the proposed ramp generator for detecting threshold levels of the generated triangular signal, unlike when leading edge or trailing edge modulation is used [92, 93, 94, 95, 96].

For other considerations there are some definitions in equations [89] 5.1, 5.2 and 5.3:

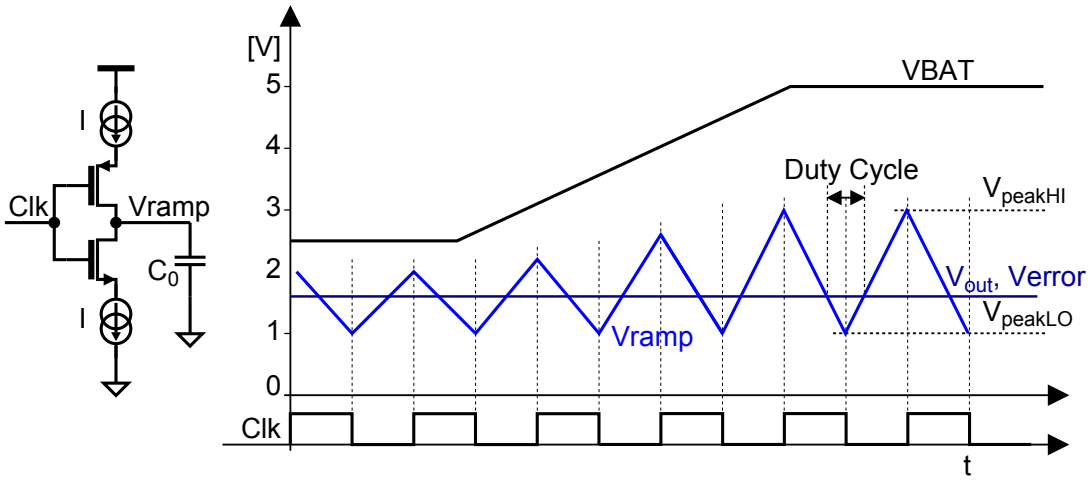



Figure 5.3.: The core of the proposed dual edge ramp generator

$$V_{peakLO} = const. > ground \tag{5.1}$$

$$V_{peakHI} = kVBAT + V_{peakLO} \tag{5.2}$$

$$Duty\,Cycle \Rightarrow D = \frac{V_{out}}{VBAT} \tag{5.3}$$

If we use the concept that the generated ramp will be proportional to the supply voltage ($VBAT$), it will have a positive effect on the internal $Verror$ signal within the control section ($Verror = const.$ for any $VBAT$, for given $V_{out}$, this is a feedforward effect) [89]. To achieve this effect we need to generate a voltage references proportional to the power supply.

To confirm this statement, we first give the Duty Cycle from Fig. 5.3

$$D = \frac{Verror - V_{peakLO}}{V_{peakHI} - V_{peakLO}} \tag{5.4}$$

Substituting equation 5.3 into 5.4 and solving for $Verror$ gives

$$Verror = \frac{V_{out}}{VBAT}\left(V_{peakHI} - V_{peakLO}\right) + V_{peakLO} \tag{5.5}$$

And finally, substituting equation 5.2 into 5.5 which can be further simplified to

$$Verror = kV_{out} + V_{peakLO} \tag{5.6}$$

and $V_{peakLO}$ must not be function of $VBAT$. This confirms that with the ramp so created, the internal signal $Verror$ in the converter is independent of the power supply change.

The core in a simple form, as shown in Fig. 5.3, intrinsically exhibits 2 kinds of drifts

and makes this circuit unusable. In the case of duration mismatch between charging and discharging phases a differential drift will arise. For example if the clock duty cycle is higher than *50 %*, the capacitor $C_0$ will at each cycle be charged more than it is discharged, leading the voltage to drift up. Also a control of the common mode voltage could drift if for example the top and bottom current source are un-matched.

In order to use the basic concept of the generator ramp from Fig. 5.3, it needs to be supplemented by control loops and techniques that prevent the above-mentioned drifts. Fig. 5.4 shows a simplified block diagram of the proposed dual edge ramp generator. As shown on this diagram, two loops are created for the correct function, namely amplitude loop and common mode loop. Next, there is a phase generator that takes care of charging and discharging phases of the ramp generation, and also generates control signals for sensors that are based on sample-hold (SH) for the common mode and amplitude loops. The phase generator must be designed as symmetrical as possible and with accurate timing, for the accuracy of the generated ramp.

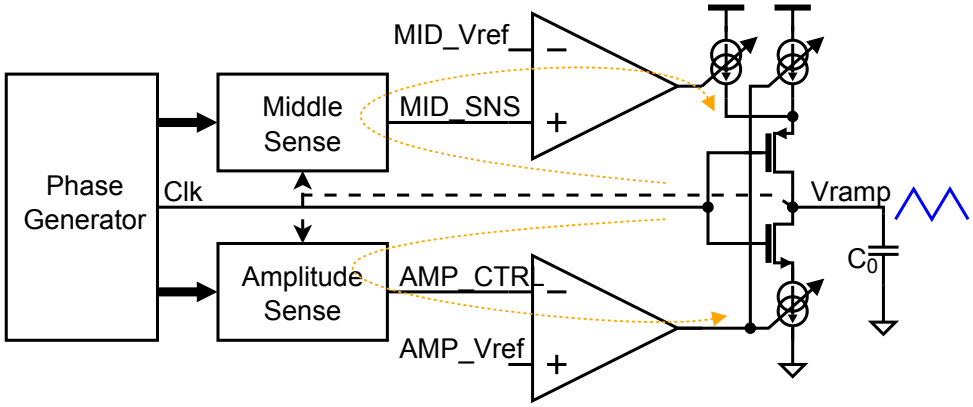



Figure 5.4.: Simplified block diagram of the proposed dual edge ramp generator

### 5.2.1. Common mode loop

The task of common mode loop is to manage the correct position between ground and supply.

There are two paths for common mode inside of the proposed ramp generator. The first one is the "Slow" path shown in Fig. 5.4. Furthermore, the “Fast” feedforward for rapid change of *VBAT*, which is reflected by the proportional change of the reference voltage *MID_Vref*. This reference voltage is compared to the sampled voltage *MID_SNS*. This voltage is generated by two-phase sampling circuitry where samples are taken in each half-period of charging resp. discharging cycle as shown in Fig. 5.5 to produce the desired common loop signal.

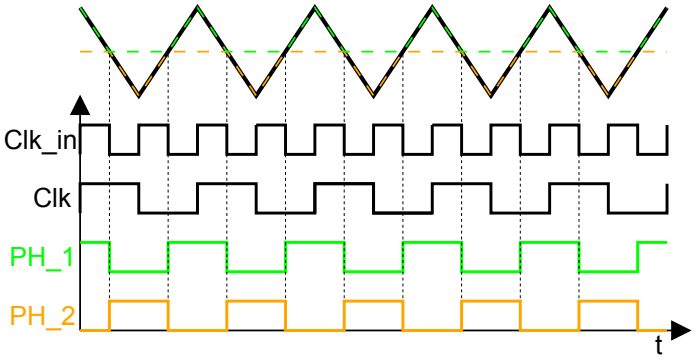



Figure 5.5.: Timing diagram of the sampling principle for generating the *MID_SNS* signal

The common mode sensing circuit is proposed in Fig. 5.6. It features two switched capacitors, $C_1$ and $C_2$ which alternatively connect to the main capacitor $C_0$.

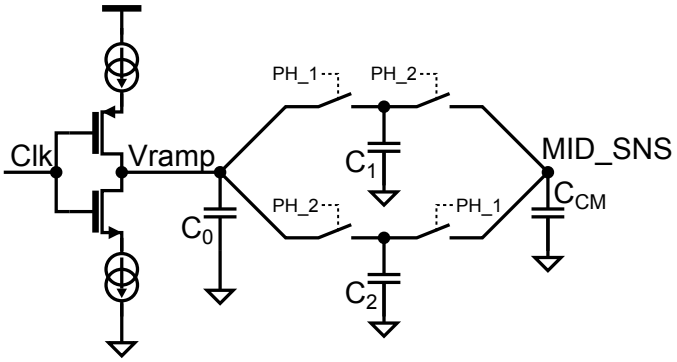



Figure 5.6.: Principal schematic for generation of the *MID_SNS* signal

## 5.2.2. Amplitude loop

The purpose of this loop is to manage the correct amplitude of the ramp (to take out the corner of R and C). The principle is, as with the Common mode loop, based on the sampling of the generator output signal (*Vramp*). However, with the difference that three-phase sampling is used here, instead of two-phase as shown in Fig. 5.7. This results in the *VTOP* and *VBOT* voltage values representing the upper and lower limits of the generated ramp. These values can then be used to control the amplitude, i.e. to adjust the discharging and charging current, so that the output ramp has the desired amplitude. Using three-phase sampling technique does not generate pulses at the beginning of sampling. As mentioned, great emphasis is placed on timing.

Part of the amplitude sensing circuit is proposed in Fig. 5.8. It features one switched capacitor, $C_a$ which alternatively connect to the main capacitor $C_0$.

On this capacitor, $C_a$, the upper and lower ramp boundaries are sampled alternately. A simplified time diagram for one of the three phases is illustrated in the Fig. 5.9.

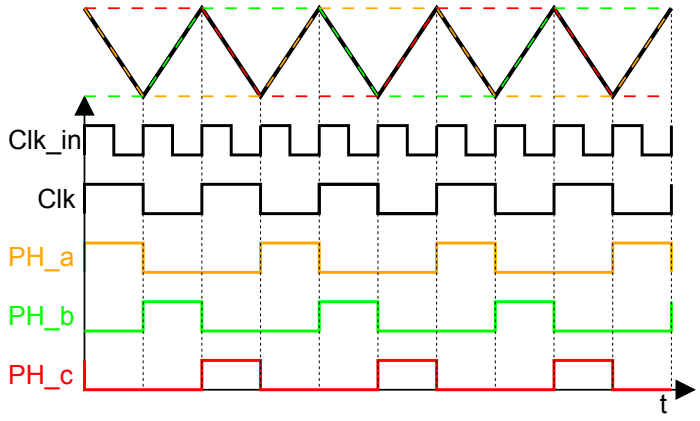



Figure 5.7.: Timing diagram of the sampling principle for generating the *AMP_CTRL* signal

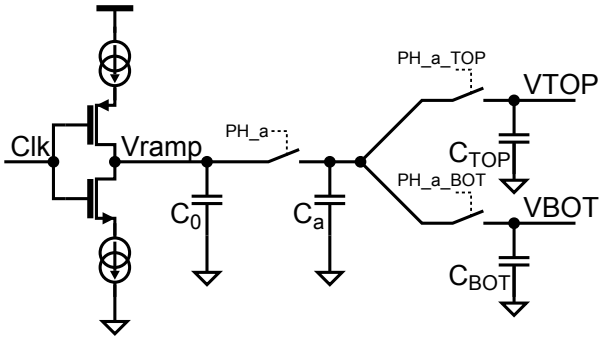



Figure 5.8.: Principal schematic for generation of the *AMP_CTRL* signal - Phase_a

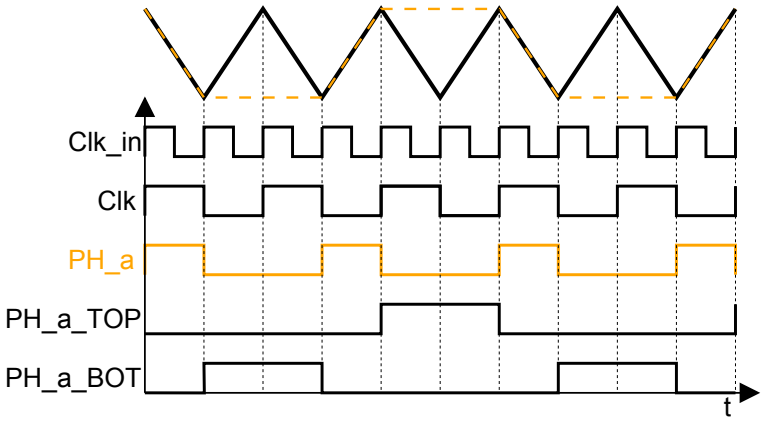



Figure 5.9.: Timing diagram of the sampling principle for generating the *AMP_CTRL* for one phase

## 5.3. Achieved results

The actual generator requires no external components and also does not need trimming. High linearity of the output signal as well as the autonomy of the generator is ensured by

the control loops that control the amplitude, and the mean value of the output signal. The device is fully integrated and is manufactured in CMOS technology HCMOS9GP *130 nm*. The fabricated die is packaged in QFN 40 package.

The designed dual edge single ended ramp generator is a part of a multi-project test chip, which consists of four projects and was funded by the Grant Agency of the Czech Technical University in Prague, grant No. SGS17/188/OHK3/3T/13. The first project is True Random Number Generator - TRNG for modern communication systems. A mismatch among different types of MOSFETs is studied in the third project. The aim of the last project is testing new electrostatic discharge ESD protective structures in customized pads. The first three projects are protected by pads containing standard ESD protections available in the used process. A layout of the whole test chip is depicted in Fig. 5.10.

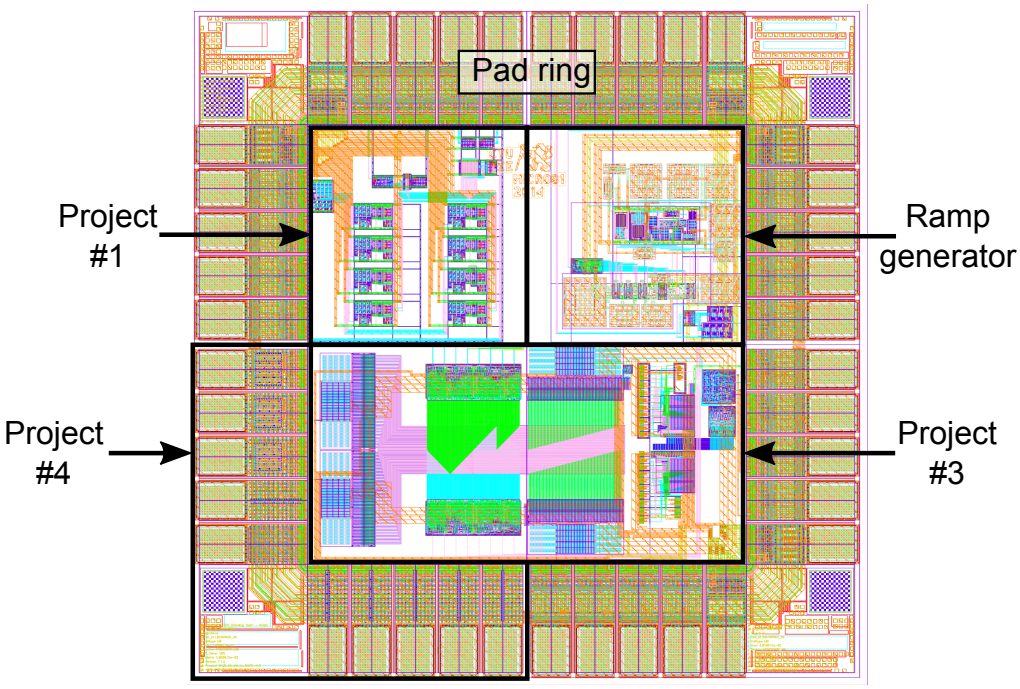



Figure 5.10.: The layout of the multi-project test chip without displayed tiles for better layer planarization

The die photo is shown in Fig. 5.11. The designed device occupies an area of $0.0625\,mm^2$ including all described parts – analogue core of the ramp generator, common mode loop, amplitude loop, phase generator and also testing circuitry. In Fig. 5.11, there are not clearly visible any structures, which are visible in Fig. 5.10 because the fabricated die contains so-called tiles, which are intended to better planarization of individual layers during chemical-mechanical polishing. For unambiguous identification, the fabricated chip includes emblems of the Czech Technical University in Prague, whose microphotography is shown in Fig 5.12.

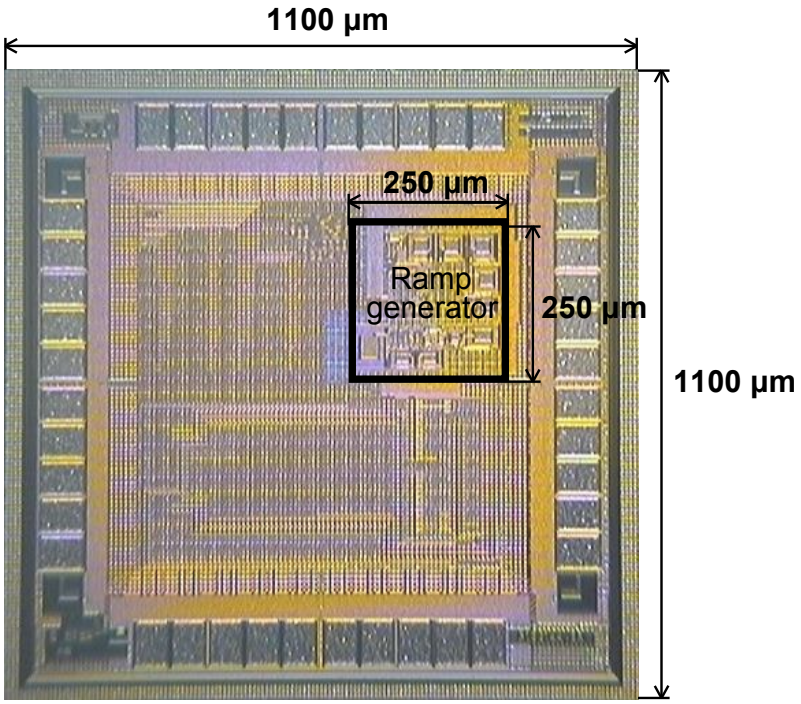



Figure 5.11.: Photo of the fabricated die. The proposed dual edge single ended ramp generator occupies the marked area


Figure 5.12.: Emblems of the Czech Technical University in Prague which is located on the fabricated chip

### 5.3.1. Measurement

Block diagram and principle of measurement linearity, which was used for validation of the designed ramp generator is shown in Fig. 5.13. We used an indirect method for validation with integrated comparator. Output of this comparator is *PWM* signal which is modulated with reference voltage *Vref_ramp*. Furthermore, Fig. 5.14 is a snapshot of the oscilloscope, which shows the reference voltage *Vref_ramp* and output *PWM* signal from the comparator with a magnification of three sections of this signal.

Comparison of the ideal and real curves of the duty cycle for different supply voltage is shown in Fig. 5.15. The maximum error in the linearity of the proposed ramp generator, in the range of the duty cycle *5 % - 95 %,* is less than $\pm 3$ % of the theoretical value. In

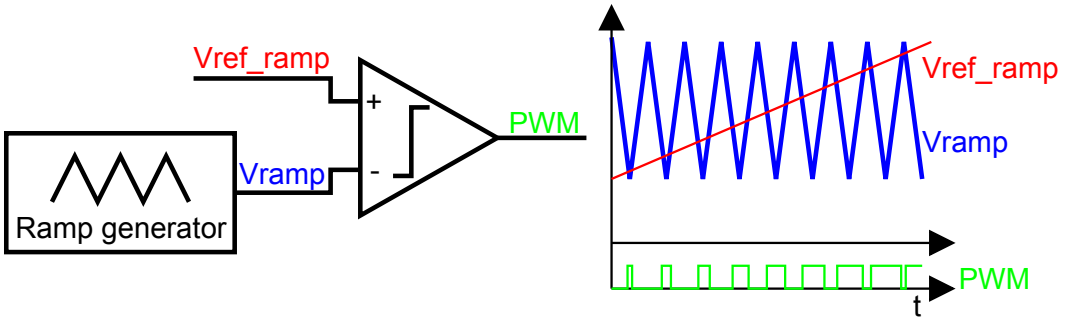



Figure 5.13.: Block diagram and principle of measurement linearity of the proposed ramp generator

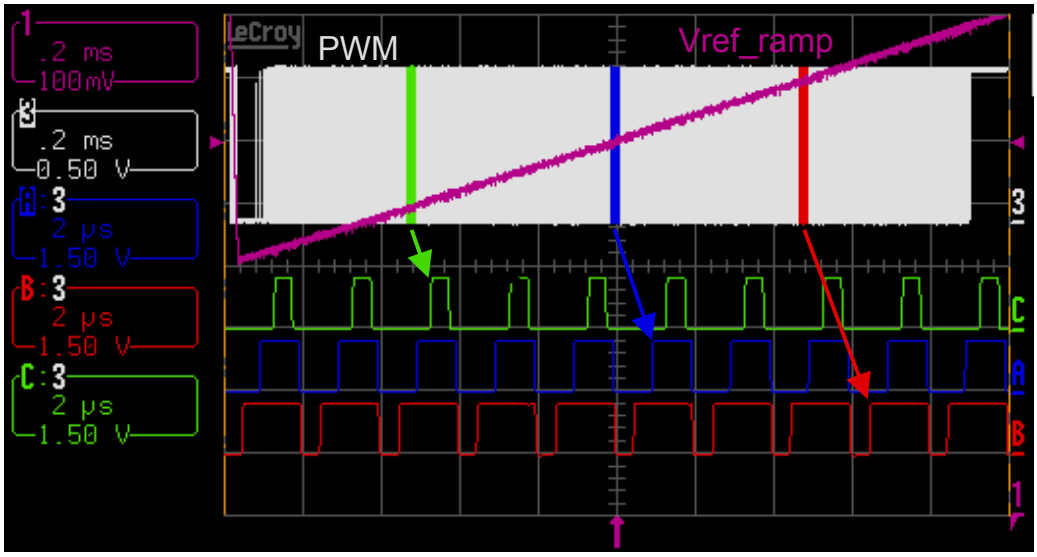



Figure 5.14.: Demonstration of lab results, voltage reference *Vref_ramp* and *PWM* signal with zooms

addition, proposed ramp generator was designed to generate ramp with frequency *1 MHz*, but thanks to the amplitude control loop, it can be used in the range from 0.5 up to 2 MHz.

## 5.4. Conclusions

This chapter introduces a new ramp generator concept that uses dual edge modulation. As described above, this modulation itself will bring a number of benefits, see section 5.1. However, the main benefit of the proposed generator is that it does not use comparators to generate a ramp for detection but is built on switched capacitor circuits. This reduces the consumption even with the ever-increasing frequency of the generated ramp. The measured results (Fig. 5.15) show that the proposed concept works properly and that the generated ramp has excellent linearity over a wide range. However, it is necessary to emphasize that the design emphasis was also placed on the phase generator and its symmetry,

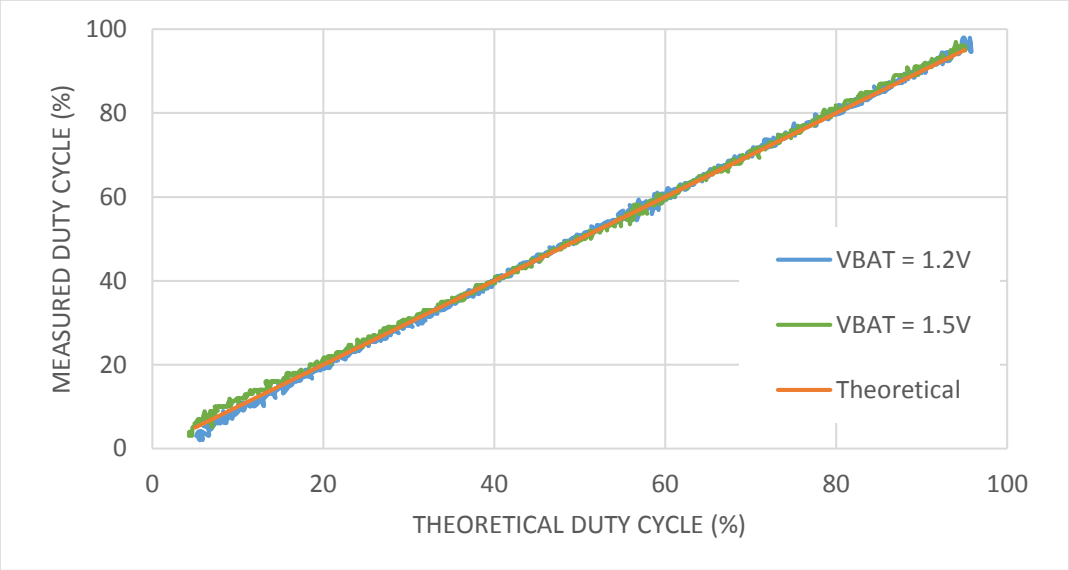



Figure 5.15.: Comparison of ramp linearity for different supply voltage with theoretical calculation

even though it is a digital part. This is because the inaccurate timing of the switched capacitor circuits causes an error in the control loops and thus in the generated ramp.

# 6 Chapter
# Frequency control of non-oscillator referenced DC-DC switching converters

This part presents the new concept of the feed-forward frequency control for asynchronous converters based on Trans Linear circuit. Novel architecture and configuration of the feed-forward frequency control circuit for asynchronous DC-DC switching converters is presented. The proposed solution preserves excellent transient properties of the asynchronous converters. Proposed feed-forward frequency control method is based on modulating of hysteresis for the comparator, which guarantees that the switching frequency is as constant as possible. The proposed concept avoids the need for a frequency feedback control such as a PLL or DLL. The implementation techniques are experimentally verified on a prototype chip in a CMOS $130\,nm$ double-oxide process by STMicroelectronics in BCD8sP technology and operate at the switching frequency of up to $2\,MHz$.

## 6.1. Theoretical study of feed-forward frequency control

In almost any analog implementation of such $T_{ON}$ and $T_{OFF}$ computations, equations 6.1 and 6.2 would be applied

$$T_{ON} = C\frac{V_{ON}}{I_{ON}} \tag{6.1}$$

$$T_{OFF} = C\frac{V_{OFF}}{I_{OFF}} \tag{6.2}$$

which express a process of charging and discharging a capacitor. The relation between $T_{ON}$ and $T_{OFF}$ times is the duty cycle

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \tag{6.3}$$

The novel solution presented in this paper is to maintain the switching frequency of a Buck as constant as possible, independent on operating conditions of the buck, hence the sum of $T_{ON}$ and $T_{OFF}$ must remain constant

$$F_S = \frac{1}{T_{ON} + T_{OFF}} = const. \tag{6.4}$$

Now, the $T_{ON}$ and $T_{OFF}$ times specified in equations 6.1 and 6.2 have to be such that both equations 6.3 and equations 6.4 are satisfies. There are two options for achieving that:

a) controlling $V_{ON}$ and $V_{OFF}$, i.e. the threshold voltages to which timing capacitor is charged by constant charging current (further referred to as constant charging current timer)

b) controlling $I_{ON}$ and $I_{OFF}$, i.e. the currents by which the timing capacitor is charged while the threshold voltage remains constant (further referred to as constant threshold voltage timer)

For constant charging current ($Iconst$) timer (option $a$), the solution can be found by substituting equations 6.3 and 6.4 into equations 6.1 and 6.2 and solving for $V_{ON}$ and $V_{OFF}$

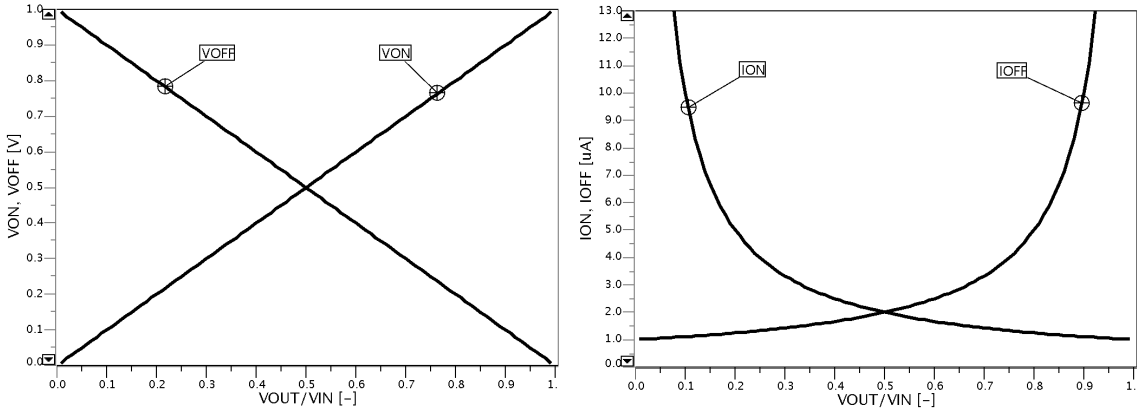
$$V_{ON} = D\frac{I_{const}}{CF_s} \tag{6.5}$$

$$V_{OFF} = (1-D)\frac{I_{const}}{CF_s} \tag{6.6}$$

Where $C$ is capacity of the external capacitor and $F_s$ is switching frequency of the DC-DC converter. Depending on the type of DC-DC converter, the duty cycle $D$ is a function of $V_{in}$ and $V_{out}$. For a Buck converter, for example, the first order approximation of the dependence of the duty cycle on input/output voltages is

$$D = \frac{V_{OUT}}{V_{IN}} \tag{6.7}$$

To achieve constant switching frequency of a DC-DC converter, the threshold voltages of the constant charging current timer must be




(a) Constant charging current timer for $I_{const}/(CF_S) = 1\,V$

(b) Constant charging voltage timer for $V_{const}CF_S = 1\,\mu A$

Figure 6.1.: Transfer function of a required ideal predictor

$$V_{ON} = \frac{V_{out}}{V_{in}} \frac{I_{const}}{CF_s} \tag{6.8}$$

$$V_{OFF} = \frac{V_{in} - V_{out}}{V_{in}} \frac{I_{const}}{CF_s} \tag{6.9}$$

In consequence the predictor has to compute $V_{out}/V_{in}$ and $(V_{in} - V_{out})/V_{in}$ expressions. Fig. 6.1a shows the dependence of $V_{ON}$ and $V_{OFF}$ thresholds on duty cycle $D$ (meaning on $V_{out}/V_{in}$) ratio for $I_{const}/(CF_S)$ term equal to $1\,V$.

For constant threshold voltage ($V_{const}$) timer (option $b$) the solution can be found for option $a$) described above except solving for $I_{ON}$ and $I_{OFF}$

$$I_{ON} = \frac{1}{D} V_{const} CF_s \tag{6.10}$$

$$I_{OFF} = \frac{1}{(1-D)} V_{const} CF_s \tag{6.11}$$

Accordingly, the predictor for a DC-DC converter with a constant threshold voltage timer has to calculate $V_{in}/V_{out}$ and $V_{in}/(V_{in}–V_{out})$ expressions

$$I_{ON} = \frac{V_{in}}{V_{out}} V_{const} CF_s \tag{6.12}$$

$$I_{OFF} = \frac{V_{in}}{V_{in} - V_{out}} V_{const} CF_s \tag{6.13}$$

as graphically shown in Fig. 6.1b for $V_{const}CF_S$ equal to $1\,\mu A$. This is somewhat less

straightforward compared to case $a$) because such predictor has to deal with divide by zero problems at limiting conditions ($V_{out} \longrightarrow 0$, $V_{out} \longrightarrow V_{in}$); hence a theoretical predictor should generate infinite current which is of course not practically possible.

## 6.2. Practical implementation of a predictor

The transistor level implementation of the predictor could be very tricky because in both cases (constant charging current and constant threshold voltage timer) mathematical division must be realized. The mathematical division functions can be efficiently realized using trans-linear circuits [99, 100, 101] or also called trans-linear loops (further referred to as "TL" circuits or "TL" loops), for example using bipolar transistors.

The TL circuits are well-known concepts that were originally based on an exponential relationship between $V_{BE}$ and IC of a bipolar transistor. The most basic TL cell is the well-known current mirror composed of two bipolar transistors as shown in Fig. 6.2a. For practical implementation, we have used the BCD technology of STMicroelectronics [102]. This technology is particularly suitable for this implementation while it offers both high-quality NPN as well as PNP transistors together with regular MOS devices. Shockley equation expresses the first order relationship between the collector current $I_{C1}$ and the base-emitter voltage $V_{BE1}$ of the master transistor $M_1$

$$I_{C1} = I_S \left( e^{\frac{V_{BE1}}{V_T}} - 1 \right) \tag{6.14}$$

Where $I_{C1}$ is the diode current, $I_S$ is the reverse bias saturation current, $V_{BE1}$ is the voltage across the diode, $V_T$ is the thermal voltage $kT/q$ (Boltzmann constant times temperature divided by electron charge).

The same relationship applies to the copy transistor $M_2$ provided both $M_1$ and $M_2$ are on the same die (are matched)

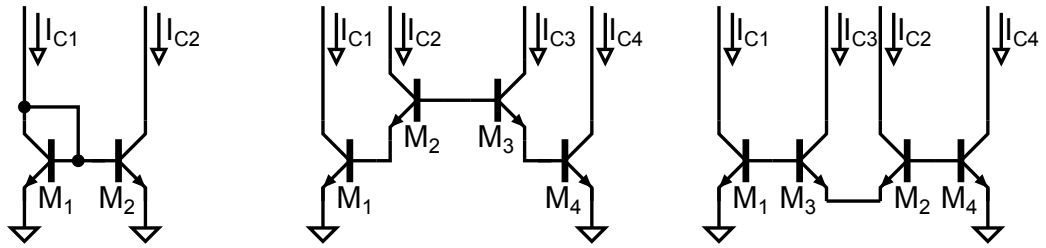
$$I_{C2} = mI_S \left( e^{\frac{V_{BE2}}{V_T}} - 1 \right) \tag{6.15}$$

where $m$ is the emitter area ratio between $M_1$ and $M_2$. The two transistors $M_1$ and $M_2$ are connected in such a way that their base-emitter voltage equals

$$V_{BE1} = V_{BE2} \tag{6.16}$$

Substituting from equation 6.14 and equation 6.15 into equation 6.16 gives

$$V_T ln \left( \frac{I_{C1}}{I_S} + 1 \right) = V_T ln \left( \frac{I_{C2}}{mI_S} + 1 \right) \tag{6.17}$$




(a) 2-transistor TL circuit (a current mirror)

(b) 4-transistor TL circuit (stacked TL loop)

(c) 4-transistor TL circuit (alternating TL loop)

Figure 6.2.: Example of trans-linear circuits

which can be further simplified to

$$I_{C2} = mI_{C1} \tag{6.18}$$

This explains the principle of a current mirror.

The extension of a 2-transistor TL loop (of the current mirror) is a 4-transistor TL loop as shown in Fig. 6.2b and 6.2c. The following equations apply to Fig. 6.2b stacked 4 transistor TL loop as well as Fig. 6.2c alternating 4 transistor TL loop.

$$V_{BE1} + V_{BE2} = V_{BE3} + V_{BE4} \tag{6.19}$$

$$V_T ln\left(\frac{I_{C1}}{I_S} + 1\right) + V_T ln\left(\frac{I_{C2}}{I_S} + 1\right) = V_T ln\left(\frac{I_{C3}}{I_S} + 1\right) + V_T ln\left(\frac{I_{C4}}{I_S} + 1\right) \tag{6.20}$$

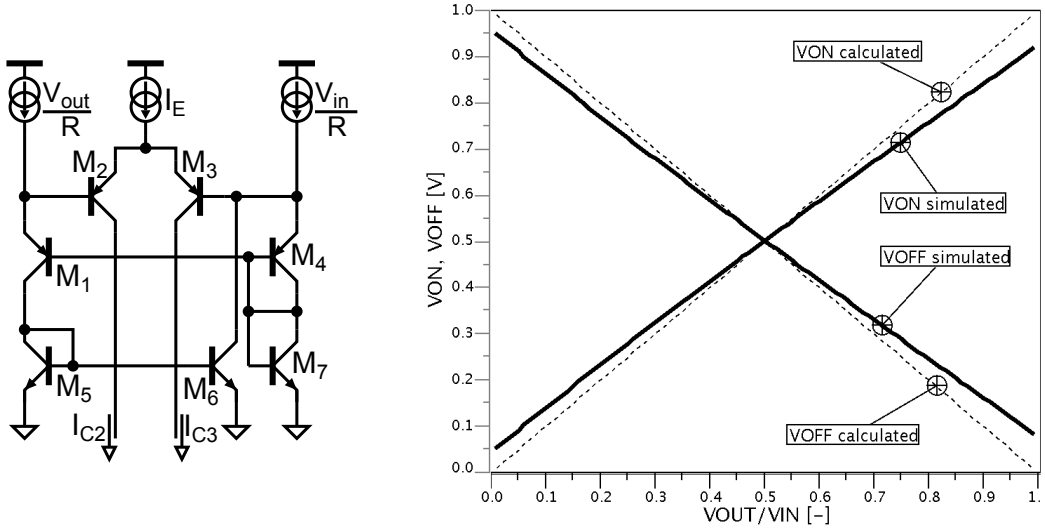
Supposing that all 4 transistors of the TL loop have identical emitter size and that $I_C \gg I_S$ for each of the 4 transistors (neglecting the $+1$ term in the Shockley equation), the equation 6.20 can be simplified to

$$I_{C1} I_{C2} = I_{C3} I_{C4} \tag{6.21}$$

As a consequence, the 4-transistor TL loop can be used to realize mathematical multiply, mathematical divide and/or square functions by proper biasing of the 4 transistors.

## A) TL Predictor for constant charging current timer

One possible and relatively simple implementation of the function in equations 6.8 and 6.9 (constant charging current timer) is shown in Fig. 6.3a. The TL loop is formed by transistors $M_1$, $M_2$, $M_3$ and $M_4$. Transistors $M_5$ - $M_6$ forming an auxiliary current mirror is not part of the TL loop and transistor $M_7$ assures the voltage bias of the TL loop, specifically




(a) Example implementation using PNP (b) Comparison of the simulated predictor with ideal transfer function for $RI_{bias} = 1\,V$

Figure 6.3.: TL predictor for constant charging current timer

the correct voltage bias of the bases of $M_1$ and $M_4$. It is obvious that transistor $M_1$ delivers a current linearly proportional to $V_{out}$

$$I_{C1} = \frac{V_{out}}{R} \tag{6.22}$$

This current $I_{C1}$ is mirrored using $M_5$ - $M_6$ current mirror and subtracted from a current $V_{in}/R$ before entering $M_4$. Hence the collector current of $M_4$ is

$$I_{C4} = \frac{V_{in}}{R} - \frac{V_{out}}{R} \tag{6.23}$$

As transistors $M_2$ and $M_3$ share the same tail current $I_{bias}$, the following two equations can express the functionality of the complete circuit:

$$I_{C1}I_{C2} = I_{C3}I_{C4} \tag{6.24}$$

$$I_{C2} + I_{C3} = I_{bias} \tag{6.25}$$

Substituting equation 6.22 and 6.23 into 6.24,6.25 and solving for $I_{C2}$ and $I_{C3}$ gives

$$I_{C2} = I_{bias}\frac{V_{in} - V_{out}}{V_{in}} \tag{6.26}$$

$$I_{C3} = I_{bias}\frac{V_{out}}{V_{in}} \tag{6.27}$$

As long as the $I_{C2}$ and $I_{C3}$ currents (these are the outputs of the TL circuit) are then led into a matched $R$, the resulting thresholds are

$$V_{ON} = RI_{C3} = RI_{bias}\frac{V_{out}}{V_{in}} \tag{6.28}$$

$$V_{OFF} = RI_{C2} = RI_{bias}\frac{V_{in} - V_{out}}{V_{in}} \tag{6.29}$$

where typically the $RI_{bias}$ term would be related to the on-chip bandgap reference voltage.

The circuit of Fig. 6.3a has been implemented using a bipolar PNP transistor of STMicroelectronics BCD8sP technology and the simulated transfer function is shown in Fig. 6.3b in comparison with ideal mathematical calculation. The difference between the simulated and the ideal results is caused by the real characteristics of the used bipolar transistors. The maximum difference between real and ideal transfer function is less than *7 %*. The maximum is only in marginal cases, where duty cycle $D(V_{out}/V_{in})$ is less than *10 %* resp. more than *90 %*. The error in the used range is so small that it can be ignored.

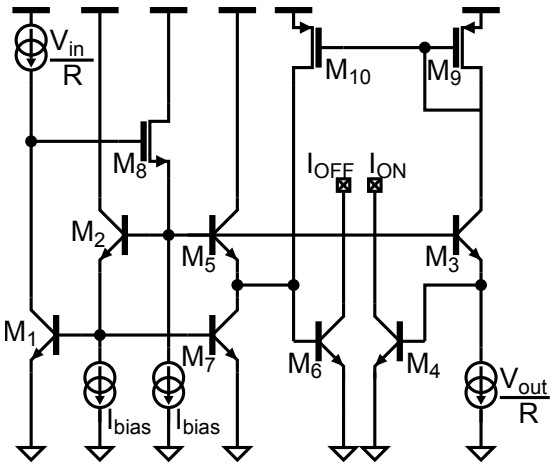
## B) TL Predictor for constant threshold voltage timer

The implementation of the equations 6.12and 6.13 (constant threshold voltage timer) is somewhat more complex. One way to implement this equation is shown in Fig. 6.4a. Two interleaved 4 transistor TL loops are used to compute $I_{ON}$ and $I_{OFF}$. The first TL loop is formed by $M_1$, $M_2$, $M_3$ and $M_4$. The second TL loop reuses the transistors $M_1$ and $M_2$ from the first TL loop and adds transistors $M_5$ and $M_6$. This is possible because the numerators of equations 6.12and 6.13 are identical. Transistors $M_9$ and $M_{10}$ form an additional auxiliary current mirror and transistor $M_7$ serves as a slave transistor in a $M_1$, $M_7$ current mirror. Transistor $M_1$ thus has 3 functions to perform in the circuit altogether:

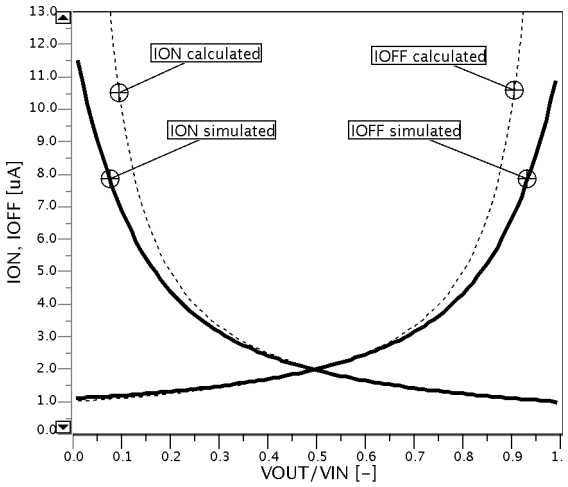
- $M_1$ is part of the $M_1$, $M_2$, $M_3$, $M_4$ TL loop
- $M_1$ is part of the $M_1$, $M_2$, $M_5$, $M_6$ TL loop
- $M_1$ is master transistor in $M_1$, $M_7$ current mirror

Transistor $M_8$ operates as a gain transistor in a local $M_8$, $M_2$, $M_1$ loop (this is not a TL loop!) to provide biasing to the base of $M_2$ and thus maintain the correct operating point of $M_1$ and $M_2$. All the transistors $M_7$-$M_{10}$ are not part of any TL loop; they only contribute to generating correct biasing for the $M_1$-$M_6$ transistors forming the two TL loops.

Transistor $M_1$ delivers a current linearly proportional to $V_{in}$ thanks to the gain transistor The collector of $M_1$ is, in fact, a high impedance node that forces $V_{BE1}$ through the action




(a) Example implementation using NPN




(b) Comparison of the simulated predictor with ideal transfer function for $I_{bias} = 1\,\mu A$

Figure 6.4.: TL predictor for constant threshold voltage timer

of $M_8$ and $M_2$ to such a voltage that makes collector current of $M_1$ to match with current sourced to this net, hence

$$I_{C1} = \frac{V_{in}}{R} \tag{6.30}$$

Both $M_2$ and $M_8$ are biased with a constant current to operate correctly, hence

$$I_{C2} = I_{bias} \tag{6.31}$$

A current linearly proportional to $V_{out}$ is injected to the emitter of $M_3$ and then further mirrored by $M_9$-$M_{10}$ current mirror. However, this mirrored current is used for the second TL loop described later and does not play any role in the TL loop being described. Transistor $M_4$ is the output transistor of the first TL loop and the collector current of $M_4$ is

$$I_{ON} = I_{C4} = I_{bias}\frac{\frac{V_{in}}{R}}{\frac{V_{out}}{R}} = I_{bias}\frac{V_{in}}{V_{out}} \tag{6.32}$$

The $V_{out}/R$ current mirrored via $M_9$-$M_{10}$ current mirror is subtracted from a current copy of $V_{in}/R$current ($M_1$, $M_7$ current mirror) before entering the transistor $M_5$. Then the resulting collector current of $M_7$ is

$$I_{OFF} = I_{C6} = I_{bias}\frac{\frac{V_{in}}{R}}{\frac{V_{in}}{R} - \frac{V_{out}}{R}} = I_{bias}\frac{V_{in}}{V_{in} - V_{out}} \tag{6.33}$$

The circuit of Fig. 6.4a has been implemented using a bipolar NPN transistor of STMicroelectronics BCD8sP technology and the simulated transfer function is shown in Fig. 6.4b in comparison with ideal mathematical calculation. There is a clearly visible degradation of the transfer function at limit conditions, i.e. at $V_{out} = 0$ and $V_{out} = V_{in}$. This is because the circuits should theoretically compute divide by zero at these conditions and hence collector current of $M_4$ and $M_6$ should theoretically limit to infinity. This is of course practically not possible and hence the gain of the circuit is limited to a finite value.

Comparison of the results from Fig. 6.3b and Fig. 6.4b shows that the error is much smaller for TL predictor for constant charging current timer. Therefore we have decided to use this variation for implementation.

## 6.3. Application of a TL predictor to a hysteretic converter

A modern hysteric control concept of a DC-DC converter is based on active coil current reconstruction. The coil current reconstruction circuitry fundamentally consists of a capacitor that is charged by current linearly proportional to $(V_{in} - V_{out})$ during the $T_{ON}$ phase and discharged by a current linearly proportional to $V_{out}$ during the $T_{OFF}$ phase. This is because the voltage integrated across this reconstruction capacitor should represent the coil current. Hence

$$I_{ON} = \frac{V_{in}}{R} - \frac{V_{out}}{R} \tag{6.34}$$

$$I_{OFF} = \frac{V_{out}}{R} \tag{6.35}$$

It means that both threshold voltages $V_{ON}$, $V_{OFF}$ as well as charging currents $I_{ON}$, $I_{OFF}$ of equation (1) are functions of $V_{in}$ and $V_{out}$. The voltage hysteresis of a hysteretic converter that can maintain a constant switching frequency of such converter can be found by substituting equation 6.34 resp. 6.35 into 6.1 resp. 6.2 and then solve a set of equations 6.1, 6.2, 6.3, 6.4 and 6.7 for $V_{ON}$ and $V_{OFF}$ which gives

$$V_{ON} = \frac{V_{out}\,(V_{in} - V_{out})}{V_{in}} \frac{1}{F_s RC} \tag{6.36}$$

$$V_{OFF} = \frac{V_{out}\,(V_{in} - V_{out})}{V_{in}} \frac{1}{F_s RC} \tag{6.37}$$

The result presented in equations 6.36 and 6.37is interesting in a sense that $V_{ON}$ and

$V_{OFF}$ are equal; i.e. the same hysteresis threshold is applicable in both $T_{ON}$ and $T_{OFF}$ phases. Thus a TL predictor suitable for a hysteretic converter has to compute 3 (and not 4) signals

$$I_{ON} = \frac{1}{R}V_{in} - V_{out} \tag{6.38}$$

$$I_{OFF} = \frac{1}{R}V_{out} \tag{6.39}$$

$$V_{TH} = V_{ON} = V_{OFF} = \frac{V_{out}\,(V_{in} - V_{out})}{V_{in}} \tag{6.40}$$

To simplify the equations for the hysteretic threshold 6.36 and 6.37, we can assume the term $F_S RC$ equal to 1. An example implementation of TL predictor suitable for a hysteretic converter is shown in Fig. 6.5. The TL loop is formed by $M_1$, $M_2$, $M_3$ and $M_4$ transistors. All other components are used for correct biasing of the TL loop elements.

The current through transistor $M_1$ is managed in a similar manner as in the previous TL circuit example of Fig. 6.4a. The $V_{BE1}$ is controlled via the $M_8$, $M_2$ gain loop in such a way that

$$I_{C1} = \frac{V_{out}}{R} \tag{6.41}$$

Also, the current through $M_4$ is managed by a gain loop. In this case, the gain loop is composed of only a single transistor $M_9$ which controls the $V_{BE4}$ in such a way that

$$I_{C4} = \frac{V_{in}}{R} \tag{6.42}$$

In other words, this TL circuit has 2 internal high impedance nodes, the collector of

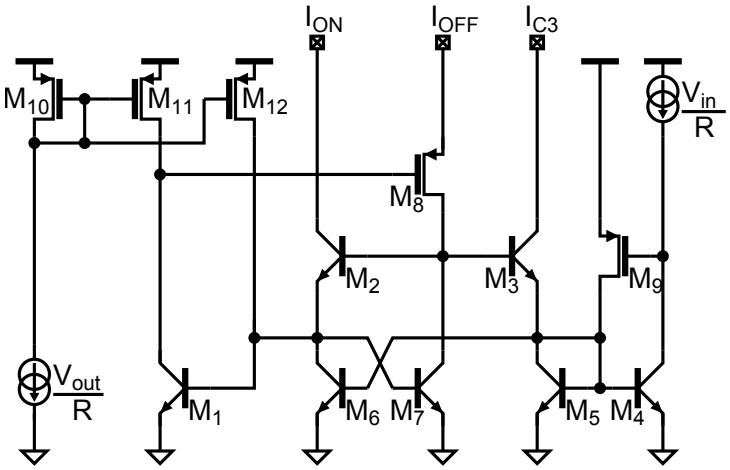



Figure 6.5.: Example implementation of a TL predictor for a hysteretic converter

$M_1$ and collector of $M_4$, which drive the gates of the two gain transistors $M_8$ and $M_9$ respectively. The $M_4$ collector current is then mirrored twice using the $M_4$, $M_5$, $M_6$ current mirror. From collector current of $M_6$ a copy of $V_{out}/R$ current sourced by $M_{12}$ is subtracted before being injected into the emitter of $M_2$. Transistor $M_2$ thus sees a current of

$$I_{C2} = \frac{V_{in}}{R} - \frac{V_{out}}{R} \tag{6.43}$$

The second current copy of $M_4$ current, the current through $M_5$, is then divided into 2 parts: the $M_3$ collector current and the current through $M_9$ in such a way that the basic equation of a 4-transistor TL loop 6.21 is satisfied.

Substituting equations 6.41, 6.42 and 6.43 into 6.21 and solving for $I_{C3}$ gives

$$I_{C3} = \frac{1}{R}\frac{V_{out}\left(V_{in} - V_{out}\right)}{V_{in}} \tag{6.44}$$

It should be noted that transistor $M_9$ has two functions in this TL circuit:

- $M_9$ manages the $V_{BE}$ of $M_4$,
- $M_9$ disposes of the excess of $M_5$ collector current.

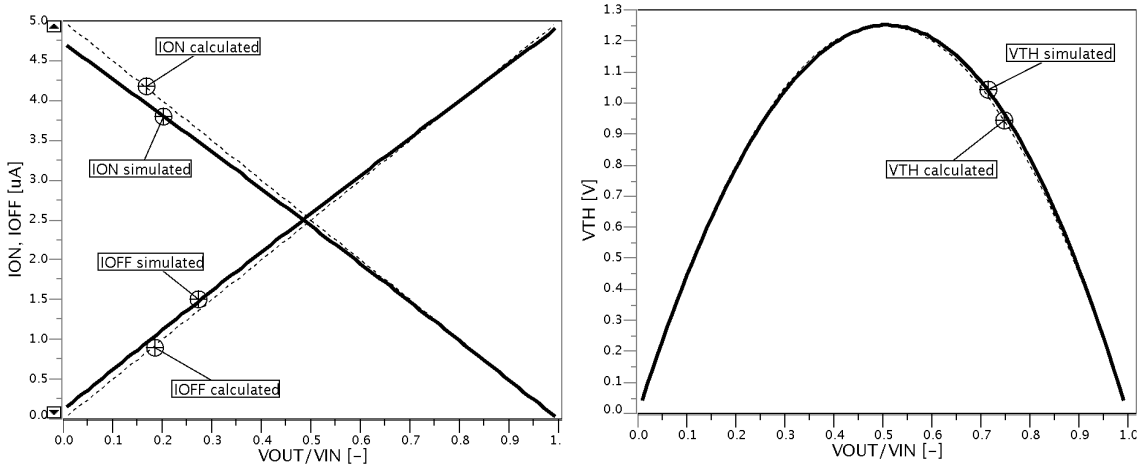
Should the $I_{C3}$ collector current be led into a matched resistor, then the resulting hysteretic threshold voltage will be

$$V_{TH} = RI_{C3} = \frac{V_{out}\left(V_{in} - V_{out}\right)}{V_{in}} \tag{6.45}$$

Transistor $M_7$, generating a current copy of $M_1$ collector current ($V_{out}/R$), is only to provide some bias for $M_8$. However choosing $V_{out}/R$ to bias $M_8$ makes this TL circuit to generate the 3 required outputs $I_{ON}$, $I_{OFF}$ and $V_{TH} = RI_{C3}$ in an elegant way.

TL predictor for a hysteric converter (Fig. 6.5) has been implemented using a bipolar NPN transistor of ST-Microelectronics BCD8 technology. The simulated transfer function is shown in Fig. 6.6 in comparison with ideal mathematical calculation. For a linear dependence of the reconstruction capacitor charging/discharging currents $I_{ON}$ and $I_{OFF}$ on $V_{out}$, the dependence of the hysteretic threshold $V_{TH}$ on $V_{out}$ has to be quadratic as is apparent from equation 6.45 in order to maintain constant switching frequency.

To demonstrate the frequency stabilization effect of a hysteretic DC-DC converter containing such TL predictor, the real transistor TL predictor has been placed in a model of a hysteretic converter as shown in Fig. 6.7. Models of the remaining parts of the hysteretic DC-DC converter (the comparator, the summing circuit, and power stage) were used to speed up the simulation. The TL predictor is leading 2 fundamental components of the hysteretic controller:




(a) Dependence of $I_{ON}$ and $I_{OFF}$ on $V_{out}/V_{in}$ for $V_{in} = 5V$ and $R = 1M\Omega$

(b) Dependence of $V_{TH}$ on $V_{out}/V_{in}$ for $V_{in} = 5V$

Figure 6.6.: Transfer function of a TL predictor implementation of Fig. 6.5

- $C_{IL}$, the reconstruction capacitor on which the inductor current $I_L$ is reconstructed
- $R_{TH}$, the resistor on which the hysteretic threshold voltage is generated

The hysteretic DC-DC converter has been supplied by $V_{in} = 5V$ supply and the output voltage has been swept from 0 to $V_{in}$ with $500mV$ steps. At each step of sweep, the switching frequency has been recorded and the resulting graph is shown in Fig. 6.8. The frequency stabilization works very well and the trace is almost flat at around $2.4MHz$ for duty cycle ratios $D$ in range *30 % to 70 %*. When the duty cycle is unbalanced, i.e. $D < 30\%$ or $D > 70\%$, there is a visible degradation of the frequency stabilization effect, primarily due to the delays in a real system (e.g. non-overlap time). Nevertheless, for practical ap-

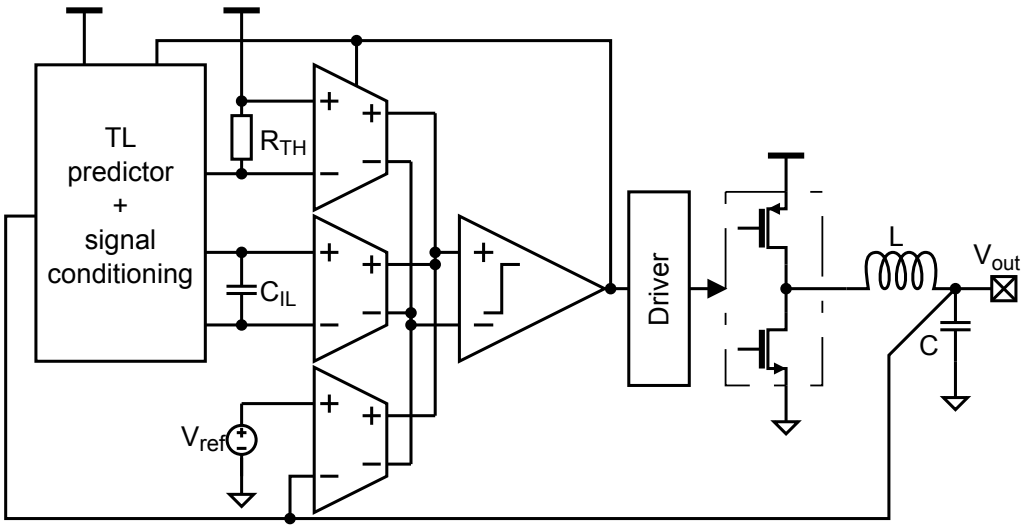



Figure 6.7.: Model of a hysteretic converter containing a TL predictor

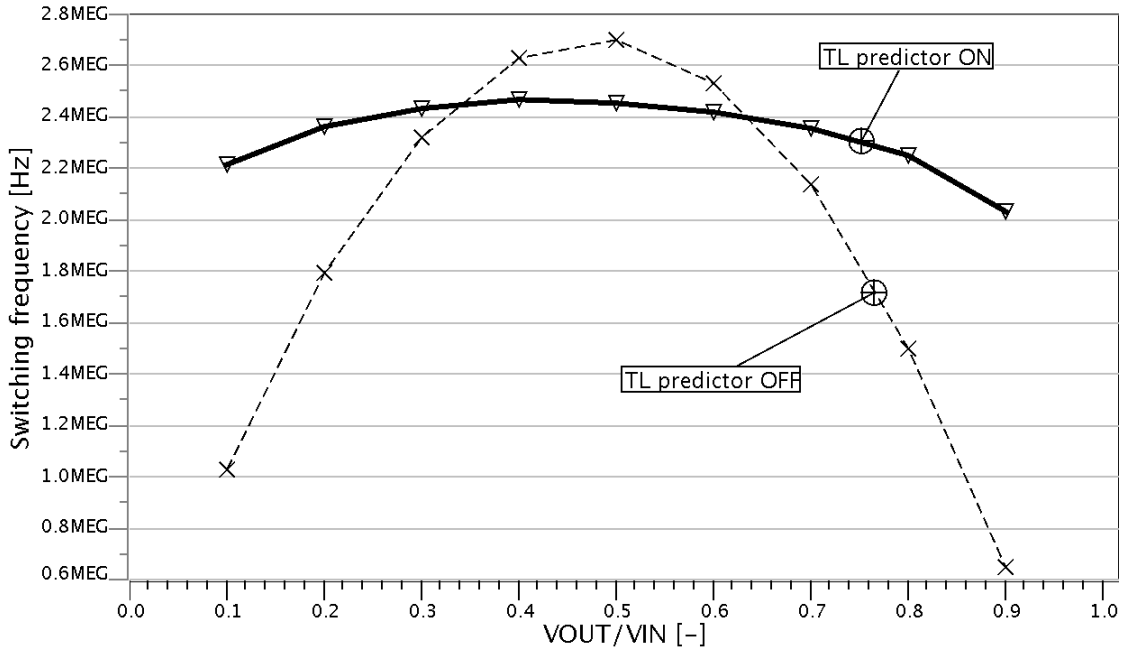



Figure 6.8.: Frequency stability of a hysteretic converter with and without the TL predictor (conditions: $V_{in} = 5\,V$, $I_{LOAD} = 1\,A$, $L = 1\,\mu H$, $C = 22\,\mu F$)

plication with duty cycle under *80 %* ($V_{out} < 4\,V$ for $V_{in} = 5\,V$), the frequency spread can be evaluated as

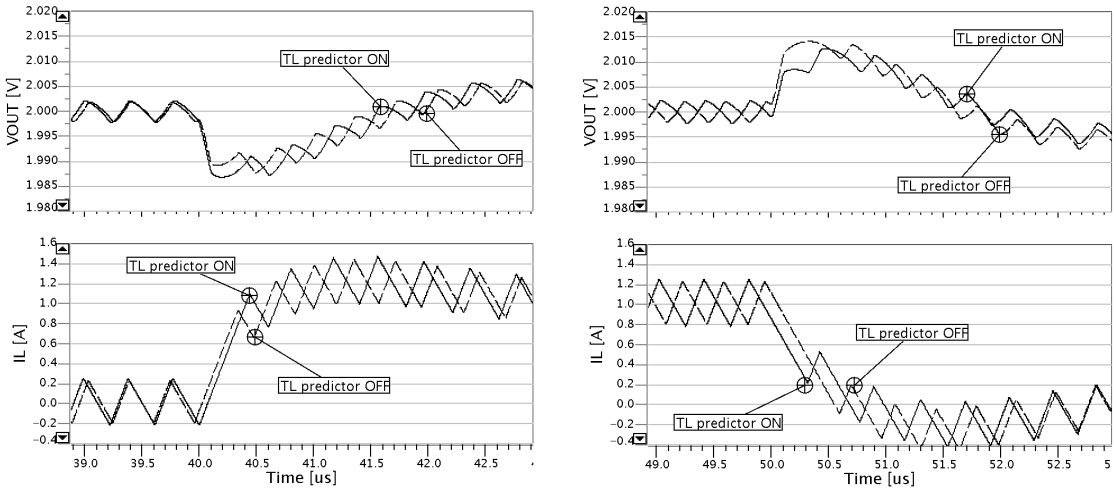
$$\frac{\Delta f}{F_S} = \pm\frac{2.5-2.2}{2.5+2.2} \approx \pm 6.4\,\% \tag{6.46}$$

To compare the influence of the predictor, the same simulation has been run for $V_{TH}$ locked to a fixed value, i.e. the TL predictor was off. In this case, the spread evaluated by the same measurement criteria is much large

$$\frac{\Delta f}{F_S} = \pm\frac{2.7-1.0}{2.7+1.0} \approx \pm 46\,\% \tag{6.47}$$

The TL predictor circuit thus improves the frequency stability by the factor of 7 times.

In addition to frequency stability, it has been examined whether the transient performance remained unaffected for variable $V_{TH}$; in other words, whether there is a penalty for improved frequency stability. Compares load transients from $I_{LOAD} = 10\,mA$ to $I_{LOAD} = 1\,A$ in $100\,ns$ Fig. 6.9a and from $I_{LOAD} = 1\,A$ to $I_{LOAD} = 10\,mA$ in $100\,ns$ Fig. 6.9b. It can be seen that the load transient performance is very similar and variation of the output voltage is under $15\,mV$ for all cases irrespective of the TL frequency predictor being on or off.




(a) Rising edge

(b) Falling edge

Figure 6.9.: Load transient performance of a hysteretic converter with and without the TL predictor (conditions: $V_{in} = 5V$, $V_{out} = 2V$, $L = 1\,\mu H$, $C = 22\,\mu F$)

## 6.4. Measurement results

The simplified block diagram of the produced asynchronous DC-DC converter is shown in Fig. 6.10. Besides the TL predictor for generating hysteresis, an internal ripple reconstruction active way - ramp reconstruction was created here. This approach takes precedence in the fact that external components are not required for the reconstruction filter, which reduces costs and overall size (footprint) requirements on PCB.

Proposed frequency predictor based on TL circuit was fabricated using a CMOS *130 nm* double-oxide process by STMicroelectronics in BCD8sP technology. The photograph of

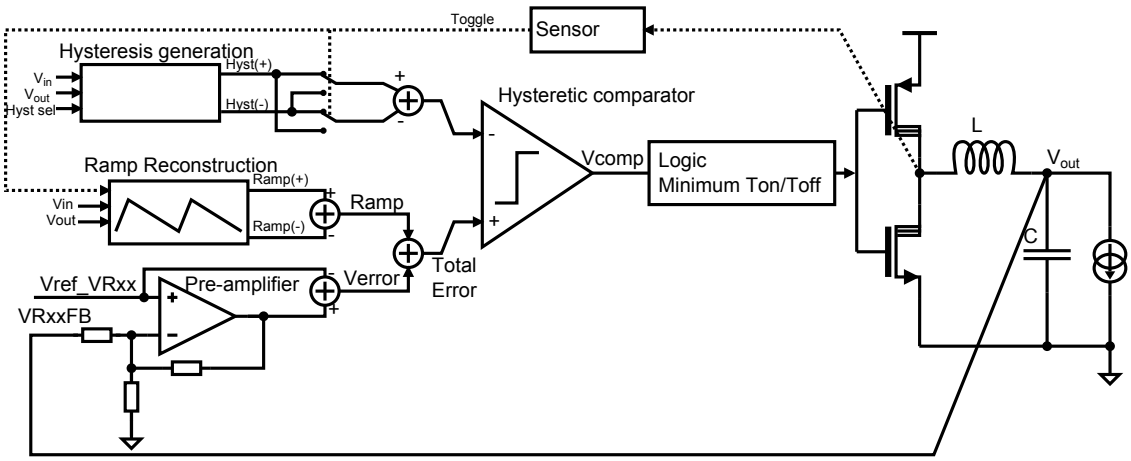



Figure 6.10.: Block diagram of the hysteretic regulator with proposed TL predictor (Hysteresis generation) and internal ripple reconstruction (Ramp Reconstruction)

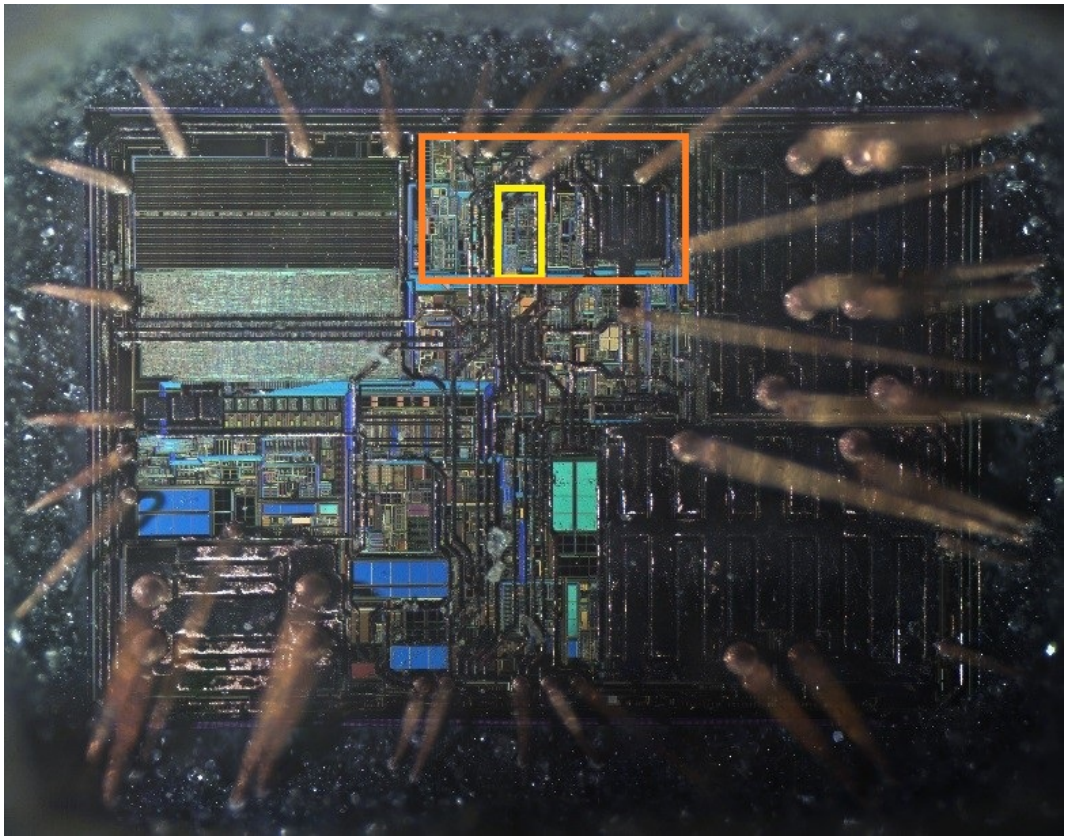


Figure 6.11.: Die of the chip with designation of the proposed circuit

the chip/die is shown in Fig. 6.11 and the area where the frequency TL predictor is located is highlighted with yellow. This circuit is part of the asynchronous DC-DC converter marked with an orange color. The main parameters of a converter are: desired output voltage $V_{out} = 3.3\,V$, input voltage $V_{in} = 5\,V$, inductance $L = 1\,\mu H$, capacitance $C = 22\,\mu F$ and maximal current load $I_{max} = 300\,mA$.

To verify the proper function of the proposed TL predictor, a function has been implemented that can deactivate this circuit. In this mode, a constant hysteresis is generated, independently of the controller's supply and output voltages. The measured transfer function of TL predictor is shown in Fig. 6.12 in comparison with scaled ideal mathematical calculations. The quadratic dependence of the generated hysteretic threshold $V_{TH}$ on $V_{out}$ corresponds to the theoretical value from equation 6.45 up to small deviations. In this figure, it is also possible to see the measurement results if the TL circuit is deactivated and the generated hysteresis is constant.

The hysteretic regulator switching frequency with resp. without proposed TL predictor for different load current is represented in Fig. 6.13a resp. 6.13b. As expected, the switching frequency exhibits a strong dependence on the input voltage.

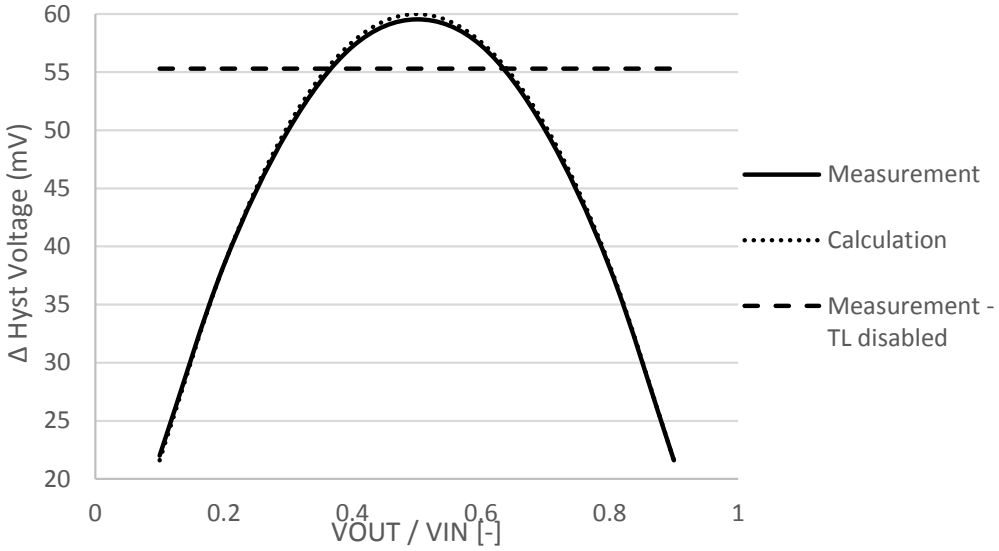
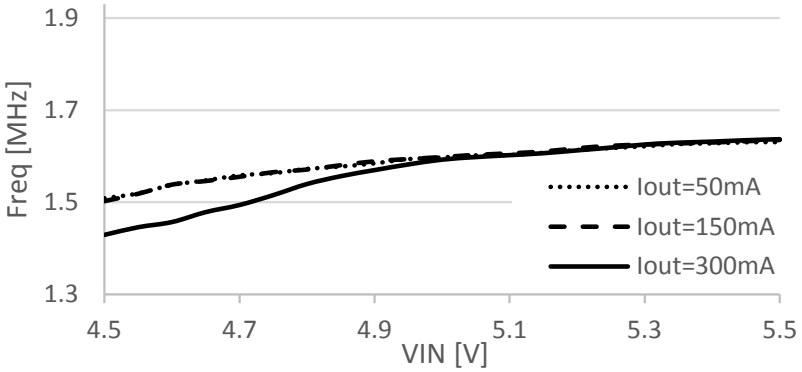
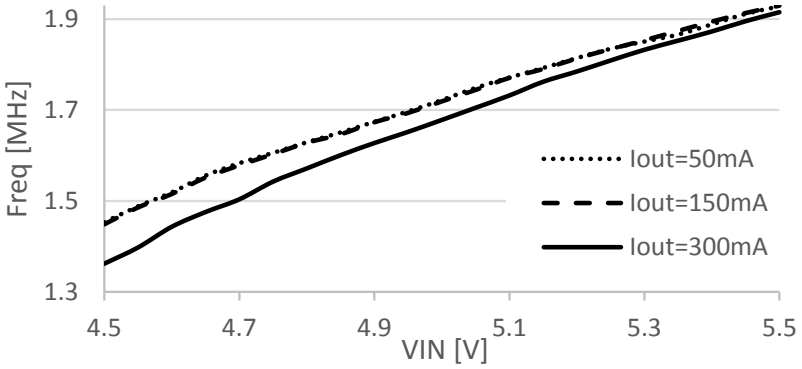



Figure 6.12.: Transfer function of a TL predictor implementation of Fig. 6.5 - Measurement and calculation




(a) TL predictor activated




(b) TL predictor deactivated

Figure 6.13.: Frequency stability of a hysteretic converter with and without the TL predictor - Measurement

## 6.5. Conclusions and future work

The TL predictor circuit for simulation improves the frequency stability by the factor of 7 times while in the measurement this factor is half. This decreasing of the switching frequency stabilization is due in particular to the selected range of input signals with which the hysteresis comparator works (tens of $mV$) and the parasitic influences (especially capacities). For this reason, it would be preferable to use a larger range of input signals but, while maintaining the transient properties, it brings an undesirable increase in consumption. However, despite this degradation, the benefit of the proposed TL predictor to stabilize the switching frequency of the asynchronous DC-DC controller is noticeable as can be seen from the comparison of Fig. 6.13.

# 7 Chapter Conclusions

The presented thesis was created to show the current state of research in the field of power management for portable systems where only a limited power source is available. Basic principles and devices, which are used in power management, as well as the latest trends in this field, were described. Next this work summarizes the knowledge, new architecture, and concept which were obtained during the development of both linear regulators for SoC solution and switching converters.

In this thesis there were presented two topologies for implementation of the capacitor-less linear regulators, which can be used in SoC applications in the chapter 3. This research brings a new solution for the reduction of dedicated capacitors of the regulators and thus the price reduction. Thanks to this approach, the internal parts of SoC can be powered by an uninterrupted power supply, thereby improving its performance. The first presented topopogy is based on the PMOS power transistor and the other one on the NMOS power transistor. The first topology was manufactured and validated in the laboratory. Simulation and especially the measurement results of the prototype demonstrate that this architecture is promising for use in the SoC applications (3.1, 3.2).

In the next section, the sensor for indirect current direction detection, which is used in apparatus for efficient regulation of the floating capacitance voltage in the three-level floating capacitor converter for 4G RF PA (switching frequency > $80 MHz$), was presented. Advantages of this three-level floating capacitor converter topology are a lower output voltage ripple, reduced harmonic distortion and lower electromagnetic concerns. The sensor is based on the voltage drop, which is generated on the power switches. This current sensing circuit presents the advantage to avoid using a Hall Effect probe or a sensing resistor, which are techniques requiring external components and thus increasing the cost.

In addition, a new concept of the dual edge single ended ramp generator was presented in the chapter 5. Selecting this dual edge modulation is advantageous because it limits the effect of the comparator delay on the PWM controller and also improves transient

characteristics of the system due to the fact that the error signal is sampled twice every period. The originality of the design of the saw tooth signal generator consists mainly in the use of new control loops (described in section 5.2.1 and 5.2.2), which ensures low power consumption and good linearity over a wide range of operating conditions without having to use comparators, as shown by prototype measurements (the results listed in Fig. 5.15). The device is fully integrated and is manufactured in 130 $nm$ bulk CMOS technology known as HCMOS9GP.

Last but not least this work has demonstrated that a frequency predictor based on TL (trans-linear) circuits can be used to keep the switching frequency of an asynchronous DC-DC converter under control. This is possible because TL circuits can realize mathematical multiplication, division and squaring functions with adequate precision in a simple and cost-effective way. Moreover, the well isolated bipolar transistors of STMicroelectronics BCD8sP technology allow for relatively low biasing currents of the bipolar transistors, hence the entire TL predictor can be made with consumption in the range of 10 $\mu A$. This is instrumental in reducing the overall quiescent current consumption of a DC-DC converter. Simulation and especially the measurement results of the prototype demonstrate that proposed frequency predictor based on TL circuit can be used for stabilization of switching frequency without impacting of excellent transient properties of the asynchronous converters (the results listed in Fig. 6.12 and 6.13).

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# Appendices

# A Appendix
# List of Author's Publications

## A.1. Publications Related to the Topic of This Work

### A.1.1. Publications in Impacted Journals

V. Kotě , P. Vacula, V. Molata, O. Vesely, O. Tlaskal, D. Barri, J. Jakovenko, M. Husak, *"A True Random Number Generator with Time Multiplexed Sources of Randomness,"* Radioengineering, 2018, (In press). Co-authorship: 15%

### A.1.2. Publications in Reviewed Journals

V. Kotě, V. Molata, and J. Jakovenko, *"Enhanced generic architecture for safety increase of true random number generators,"* ElectroScope, vol. 2014, no. 3, 2014. Co-authorship: 15%

Cited in:

- G. J. Croll, "BiEntropy of knots on the simple cubic lattice," in *Unified Field Mechanics II: Formulations and Empirical Tests*, 2018, pp. 447–453.

V. Molata,V. Kotě, J. Jakovenko, *"Capacitor-less Linear Regulator with NMOS Power Transistor,"* ElectroScope, vol. 2013, no. 5, 2013. Co-authorship: 80%

Cited in:

- N. Bansal and R. Gupta, "An NMOS low drop-out voltage regulator with -17dB wide-band power supply rejection for SerDes in 22FDX," in *31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID)*, Pune, India, 2018, pp. 341–346.

### A.1.3. Patents

M. Thomas, P. Arno, V. Molata, O. Tlaskal, *"Efficient Regulation of Capacitance Voltage(s) in a Switched Mode Multi-Level Power Converter,"* Patent US9160232B2. Co-authorship: 15%

Cited in:

- Ilan Yoscovich, Tzachi Glovinsky, Guy Sella, Yoav Galin, "Multi-level inverter with flying capacitor topology," Patent US9318974B2
- David Lidsky, Timothy Alan Phillips, "Resonant rectified discontinuous switching regulator," Patent US20160261185A1
- David Lidsky, Timothy Alan Phillips, Parag Oak, "Resonant rectified discontinuous switching regulator with inductor preflux," Patent US20160261189A1
- Nicolas Levilly, Philippe Ernest, Julien Bouhraoua, Janusz Rodziewicz, "Method and apparatus for controlling a multilevel soft switching power converter," Patent US9467065B2
- Dr. Stefan Goetz, "Electronic circuit for easier operation of multilevel converters," Patent US20170123014A1
- Tomoyuki TANISUGI, Yuji NAKAMARU, "Motor control device and motor control method," Patent US20170345288A1
- Kengo Nishimura, Seiji Ishibashi, Yuta Komatsu, Satoru Murakami, "Power conversion device." Patent JP2018007325A
- Ilan Yoscovich, "High frequency multi-level inverter," Patent US9941813B2
- Parag Oak, "Switching regulator with self-biasing high voltage swing switch stack," Patent US9985526B1
- Pavan Kumar, Harish K. Krishnamurthy, "Selectable-mode voltage regulator topology," Patent US20160190921A1
- Motoyoshi KUBOUCHI, "Chopper circuit," Patent US9812966B2
- Mark Mercer, Aravind Mangudi, Holger Petersen, "Multi-level buck converter with multiple control loops and flying capacitor regulation," Patent US9929653B1

### A.1.4. Publications Excerpted by WoS

P. Arno, M. Thomas, V. Molata, T. Jerábek, *"17.6 Envelope modulator for multimode transmitters with AC-coupled multilevel regulators,"* IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC) (2014), San Francisco, CA: 296-297, 2014.

Cited in:

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## A.1.5. Other Publications

V. Molata, V. Kotě, *"Capacitor-Less LDO Regulator With Low Consumption,"* in Proceedings of the International Student Scientific Conference Poster – 17/2013, Prague, Czech Republic, 2013, pp. 1–5. Co-authorship: 80%

V. Molata,V. Kotě, T. Nápravník, J. Jakovenko, *"Capacitor-less Linear Regulator with NMOS Power Transistor,"* in Electronic Devices and Systems IMAPS CS International Conference 2013, Brno, Czech Republic, 2013, p p. 50-55. Co-authorship: 70%

V. Molata, V. Kotě, T. Nápravník, J. Jakovenko, *"Capacitor-less LDO regulator in CMOS technology,"* in Electronic Devices and Systems IMAPS CS In-

ternational Conference 2012, Brno, Czech Republic, 2012, pp. 54-59. Co-authorship: 70%

### A.1.6. Functional Samples

V. Molata, V. Kotě, P. Vacula, and J. Jakovenko, Integrated single-ended low-power ramp generator for DC-DC converters. Functional sample. 2014. Co-authorship: 75%

## A.2. Publications Not Related to the Topic of This Work

### A.2.1. Publications in Reviewed Journals

V. Kotě, V. Molata, and J. Jakovenko, *"Improved structure of true random number generator with direct amplification of analog noise,"* ElectroScope, vol. 2012, no. 6, 2012. Co-authorship: 10%

### A.2.2. Publications Excerpted by Scopus

T. Nápravník, V. Kotě, V. Molata, and J. Jakovenko, *"Differential Evolutionary Optimization Algorithm Applied to ESD MOSFET Model Fitting Problem,"* in IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Tallinn, Estonia, 2012, pp. 155–158. Co-authorship: 10%

### A.2.3. Other Publications

V. Kotě, V. Molata, and P. Vacula, *"Behavioral models of true random number generators,"* in Proceedings of the International Student Scientific Conference Poster – 22/2018, Prague, Czech Republic, 2018, pp. 1–6. Co-authorship: 20%

V. Kotě, V. Molata, and J. Jakovenko, *"New structure of true random number generators with protective mechanisms,"* in Electronic Devices and Systems IMAPS CS International Conference 2014, Brno, Czech Republic, 2014, pp. 19–24. Co-authorship: 15%

T. Nápravník, V. Kotě, V. Molata, and J. Jakovenko, *"Utilization of Differential Evolutionary Optimization Algorithm for ESD MOSFET Model Fitting,"* in Proceedings of Electronic Devices and Systems EDS 2012, Brno, Czech Republic, 2012, pp. 33–38. Co-authorship: 10%

V. Kotě, T. Nápravník, V. Molata, and J. Jakovenko, *"Structure, modeling and realization of true random number generator with analog noise amplification,"* in Electronic Devices and Systems IMAPS CS International Conference 2012, Brno, Czech Republic, 2012, pp. 145–150. Co-authorship: 10%

### A.2.4. Functional Samples

V. Kotě, V. Molata, P. Vacula, and J. Jakovenko, Fully Integrated Pipelined Noise Source Based on Metastability for True Random Number Generators. Functional sample. 2014. Co-authorship: 10%

P. Vacula, T. Jerabek, V. Molata, V. Kotě, J. Jakovenko, and M. Hus´ak, Low specific onresistance MOSFET with waffle gate pattern for power management. Functional sample. 2014. Co-authorship: 5%

# B Appendix Recognition and Review

IEEE MTT/AP/ED/EMC Joint Chapter awarded Diploma for the best C+EI paper "Behavioral Models of True Random Number Generators presented at Poster 2018." *22nd International Student Conference on Electrical Engineering POSTER 2018*. Prague, Czech Republic, May 10, 2018.

Program Committee of POSTER 2018 awarded Certificate of Achievement in the Best Poster Competition for the work "Behavioral Models of True Random Number Generators." *22nd International Student Conference on Electrical Engineering POSTER 2018*. Prague, Czech Republic, May 10, 2018.

Program Committee of POSTER 2013 awarded Diploma for the work "Capacitor-Less LDO Regulator With Low Consumption." *17nd International Student Conference on Electrical Engineering POSTER 2013*. Prague, Czech Republic, May 16, 2013.

Best Ph.D. Poster Award – 1st Place for the work "Structure, modeling and realization of true random number generator with analog noise amplification." *IMAPS Electronic Devices and Systems International Conference 2012*. Brno, Czech Republic, June 29, 2012.