Czech Technical University in Prague
Faculty of Electrical Engineering
Department of Circuit Theory

Analysis and modeling of the modern charge pump circuits

Disertation thesis

Ing. Jan Marek

Ph.D. programme: P 2612 Electrical Engineering and Information Technology
Branch of study: 2602V013 Theoretical Electrical Engineering
Supervisor: Doc. Dr. Ing. Jiří Hospodka
Supervisor–specialist: Ing. Ondřej Šubrt, Ph.D.

Prague, September 2018

Thesis Supervisor:
Doc. Dr. Ing. Jiří Hospodka
Department of Circuit Theory
Faculty of Electrical Engineering
Czech Technical University in Prague
Technická 2
160 00 Prague 6
Czech Republic

Thesis Supervisor–Specialist:
Ing. Ondřej Šubrt, Ph.D.[1,2]
[1]Department of Circuit Theory
Faculty of Electrical Engineering
Czech Technical University in Prague
Technická 2
160 00 Prague 6
Czech Republic

[2]ASICentrum, a company of the Swatch group
Novodvorská 994
142 21 Prague
Czech Republic

Declaration

I hereby declare I have written this doctoral thesis independently and quoted all the sources of information used in accordance with methodological instructions on ethical principles for writing an academic thesis. Moreover, I state that this thesis has neither been submitted nor accepted for any other degree.

In Prague, September 2018

.....
Ing. Jan Marek

Abstract

The thesis presents the design process of the cross-coupled charge pump on the circuit-level hardware realization, which is used for supplying low current consumption peripherals on the chip. The unconventional approach to the discrete-time analogue circuit description arising from non-linear systems theory is offered. Design aspects of the SC circuits are firstly explained, including the analysis of the basic topologies of two-phase charge pumps. The main part deals with the steps of the cross-coupled charge pump design algorithm. Synthesis procedure includes the design of the pump functional blocks based on BSIM equations of MOSFET for long channel technology process and application of the pump stage complex model for estimation of the number of pump stages via state-space model description and using of the interpolation polynomial functions in the algorithm. Two available solutions are introduced satisfying particularly two criteria in terms of the circuit and economic optimization– high efficient, i.e. pump maximal voltage gain and an area-efficient charge pump. The whole procedure is summarized in the practical example, including the comparison between calculated and simulation results. Added functions of the design environment are explained, inclusive of the designed pump netlist generating for professional design environment Mentor Graphics including the real models of components that are available in library MGC Design Kit. In addition, the complex model allows the inclusion effects of higher-levels and is also applicable to other MOSFET technology process, as PSP or EKV. The main benefit is the charge pump synthesis precedure without long time-consuming optimization process.

Keywords: Cross-coupled charge pump, synthesis, BSIM model, state-space model, simulations, programme procedure.

Abstrakt

Dizertační práce se zabývá návrhem křížově vázané nábojové pumpy, jež se používá pro napájení nízkopříkonových obvodů na čipu. Používá netradiční přístup k popisu diskrétně pracujících analogových soustav vycházející z teorie nelineárních systémů. V úvodní části jsou shrnuty základní poznatky v oblasti SC obvodů včetně vlastností základních struktur dvoufázových nábojových pump. Hlavní část práce se zabývá řešením jednotlivých kroků návrhového algoritmu křížově vázané nábojové pumpy od analytického popisu a návrhu funkčních bloků až k sestavení komplexního modelu, jenž je využit k odhadu počtu stupňů reálné struktury prostřednictvím Lagrangeova interpolačního polynomu. Každá buňka v obvodu pumpy je popsána zjednodušenými rovnicemi BSIM modelu MOSFET tranzistoru s dlouhým kanálem. Jsou uvedena dvě možná řešení výsledné struktury, a to jednak na základě kritéria maximálního napěťového zisku (statická napěťová účinnost) a jednak dosažení minimální celkové plochy obvodu na čipu. Návrhový algoritmus je ukázán na praktickém příkladu, včetně srovnání dosažených parametrů se simulačními výsledky. Návrhové prostředí umožňuje mj. vygenerovat tzv. netlist výsledné struktury pro simulátor ELDO se zahrnutím modelů reálných prvků dostupných v knihovně MGC Design Kit. Popis struktury je univerzální jak z hlediska použitých modelů (PSP, EKV a další), tak i z hlediska implementace parazitních prvků vyšších stupňů. Hlavním přínosem práce je postup návrhu uvedeného typu nábojových pump bez časově náročného iteračního procesu, tedy bez nutnosti aplikace optimalizačních metod.

Klíčová slova: Křížově vázaná nábojová pumpa, návrh, BSIM model, stavový model, simulace, programová procedura.

Acknowledgements

I would like to express many thanks to my supervisor Doc. Dr. Ing. Jiří Hospodka and my supervisor-specialist Ing. Ondřej Šubrt, Ph.D. for their helpful support of my Ph.D. Thesis.

This work has been supported by the grant No. SGS17/183/OHK3/3T/13 of the CTU in Prague.

List of symbols and acronyms

a [–]	regressive parameter
A_{bulk} [–]	bulk charge effect
A_{bulk0}[–]	bulk charge effect at $(V_{GS} - V_{TH})_{eff} = 0$
A_{inv} [m^2]	inverter area
$C_L^,$ [F]	total load capacitance
C_{ij} [F]	capacitance value between electrods i, j
C_{min} [F]	minimal MOSFET capacitance
C_{mont} [F]	added strange capacitance
c_{oxe} [F]	electrical oxide capacitance
C_{pump} [F]	equivalent pump capacitance
C_{s_i} [F]	strange capacitance in i-node
$C_{si}^{,(k+1)}$ [V]	voltage on the strange capacitor in the next cycle
$C_{si}^,$ [F]	total strange capacitance
C_i [F]	main capacitance in i-node
C_L [F]	load capacitance
$C_L^,$ [F]	total load capacitance
E_{crit} [Vm^{-1}]	crititical electrical field
f_c [Hz]	driving frequency
f_s [Hz]	signal frequency
G_{v_i} [V]	voltage gain in i-node
$I_{D_{sat0R}}$ [A]	reverse drain switch current in saturation region
I_{DS0_F} [A]	forward switch drain current in triode region
I_{DS0_R} [A]	reverse switch drain current in triode region
I_{S_R} [A]	reverse switch current
$\hat{I}_{SR}$ [Am^{-1}]	drain current for unity width
$I_{0N(P)}$ [A]	drain current at $V_{GS} = 0$
$I_{1N(P)}$ [A]	linearized inverter cross current
I_{av} [A]	average curret value
i_{c_F} [A]	forward charge current
I_{cross} [A]	inverter cross current
I_D [A]	static drain current
I_{DD} [A]	current consumption
I_{DS0} [A]	drain current in the triode region
$I_{DS0N(P)}$ [A]	drain current in subtreshold region
I_{Dsat0} [A]	drain current at $V_{DS} = V_{DSsat}$
i_{inls} [A]	input current of the pump stage
I_{Lmax} [A]	maximal load current
I_{max} [A]	maximal current
i_{out1ls}, i_{out2ls} [A]	output current of the pump stage
I_L [A]	load current
I_r [A]	reverse current
I_s [A]	switch drain current
$I_{S0N(P)}$	drain current in subtreshold region at $V_{DS} = 0$

k [–]	multiply constant
$K_1, K_{1ox}, K_2, K_{2ox}$ [–]	body effect coeficients (BSIM)
L [m]	channel length
L_{eff} [m]	effective channel length
L_c [m]	MOS capacitor length
L_d [m]	diode transistor length
L_p [m]	PMOS inverter transistor length
L_s [m]	switch transistor length
n [–]	emission coeffecient
N [–]	number of the pump stages
$\hat{N}$ [–]	estimation of the number of the pump stages
$\hat{N}_{i_0}$ [–]	estimation of the initial number of the pump stages
$\tilde{P}_{DC}$ [W]	static power estimation
$P_{\bar{\phi}}$ [W]	power consumption of the second-phase clock signal
P_{ϕ} [W]	power consumption of the first-phase clock signal
P_{DC} [W]	static power
P_{out} [W]	output power
Q_{cc} [C]	total charge
q_{inj} [C]	injected charge
Q_i [C]	charge in i-node
R [–]	inverter MOSFETs sizes ratio
R_{ekv} [Ω]	equivalent resistor
R_{opt} [V^{-1}]	optimal inverter MOSFETs sizes ratio factor
R_{pump} [Ω]	equivalent pump resistance
R_{Smax} [–]	inverter MOSFETs sizes ratio factor at the maximal sensitivity
R_l [Ω]	leakage resistance
R_L [Ω]	load resistanece
S [V^{-1}]	sensitivity
S_{max} [V^{-1}]	maximal sensitivity
S_{pump} [m^2]	total pump area
t_{0_F} [s]	charge time in forward configuration
t_{0_R} [s]	charge time in reverse configuration
T_{clk} [s]	clock signal period
t_{HL} [s]	fall time
t_{LH} [s]	rise time
T_c [s]	period of the driving signal
T_r [s]	rise time
$V_{\bar{\phi}}$ [V]	the second-phase clock signal amplidue
V_{ϕ} [V]	the first-phase clock signal amplidue
$V_{BS_{eff}}$ [V]	effective bulk-source voltage
$V_{TH0_{N(P)}}$ [V]	threshold voltage of the N(P)MOS at zero bias voltages
V_{0_F} [V]	voltage value at the charge time
V_{ADIBL} [V]	dibl voltage
V_{bc} [V]	bulk-source voltage at $\mathrm{d}V_{TH}/\mathrm{d}V_{bs} = 0$
v_{bn} [V]	pump stage bulk NMOS voltage
V_{bound} [V]-	boundary of the bulk-source voltage
v_{bp} [V]	pump stage bulk PMOS voltage
$v_{C_{i_0}}^{(k+1)}$ [V]	voltage on the main capacitor in the next cycle
v_{c_R} [V]	voltage on the capacitor in reverse configuration
v_{cF} [V]	voltage on the capacitor in forward configuration
V_{DD} [V]	power supply voltage
V_{DSeff} [V]	effective drain-source voltage
V_{DSsat} [V]	saturation drain-source voltage

v_{fb} [V]	pump stage feedback voltage
V_{fin} [V]	final voltage valued
$V_{gs_{eff}}$ [V]	effective gate-source voltage
v_{i_∞} [V]	voltage in the steady state
v_{i_0} [V]	initial voltage value
V_{IH} [V]	input inverter voltage defines the output low logic level
V_{ij} [V]	volatage between electrods i, j
V_{IL} [V]	input inverter voltage defines the output high logic level
V_{in} [V]	input pump stage voltage
v_{inv} [V]	inverter output voltage
V_{off} [V]	cut-off voltage
$V_{out,av}$ [V]	average value of the pump output voltage
$V_{out,max}$ [V]	maximal pump output voltage
V_{out} [V]	output voltage
v_{out} [V]	pump stage output voltage
$V_{r_{max}}$ [V]	maximal ripple voltage
v_{sat} [ms^{-1}]	drift velocity saturation
V_{SP} [V]	inverter switching point
$V_{TH_{Mxi}}$ [V]	threshold voltage of the M_{si} MOSFET
V_{TH} [V]	threshold voltage
V_{TH0} [V]	threshold voltage at zero bias voltages
v_i [V]	node voltage
v_i^k	node voltage for $k - cycle$
V_r [V]	ripple voltage
V_t [V]	temperature voltage
v_z [V]	load voltage
$W_{M_{S_{opt}}}$ [m]	optimal switch transistor width
W_c [m]	MOS capacitor width
W_d [m]	diode transistor width
W_p [m]	PMOS inverter transistor width
W_s [m]	switch transistor width
α [V]	linearized body effect coefficient
α_D [–]	proportional voltage increment
β [–]	couple ratio
β_c [AV^{-2}]	current factor
β_D [AV^{-2}m^{-1}]	diode transistor current coefficient
δ [–]	sensitivity ratio factor
ϵ [V]	maximal voltage gain for the steady state detection
η_ε [–]	power efficiency
η_v [–]	static voltage efficiency
γ [–]	body effect coeficient
$\hat{\eta}_v$ [–]	estimation of the static voltage efficiency
$\hat{T}_r$ [s]	estimation of the pump rise time
λ [–]	capacitance ratio factor
μ_{eff} [m^{2}V^{-1}s^{-1}]	effective mobility
$\mu_{eff_{i0}}$[m^{2}V^{-1}s^{-1}]	effective mobility of the M_i MOSFET at the initial voltage values
ϕ_s [V]	surface voltage
ψ [–]	modulation factor
τ [s]	time constant
$\tau(v)$ [s]	Taylor aproximation of the voltage function at time
$\varepsilon_{r_{Vout}}$ [–]	relative error of the output voltage
ε_{Si} [–]	relative permittivity of silicon

ε_{Tr} [–]	Dynamic efficiency during rise time
φ, χ, ρ [C]	coefficients number of stages calculations
ϑ [°C]	temperature
ζ [V]	voltage factor

ARC	Active filter
CCD	Colony Collapse Disorder
CLK	Clock frequency
CLM	Channel length modulation
CTS	Charge-transfer-switch
DIBL	Drain-induced barrier lowering effect
DtAC	Discrete-time analog circuit
EEPROM	Electrically Erasable Programmable Read-Only Memory
H	high voltage level
L	low voltage level
HVT	high-voltage transistor
IC_i [V]	voltage initial condition
NDEP m^{-3}	substrate doping concentration
PDIBLC2, PDIBLCB [–]	DIBL effect coeficients
SC	Switched capacitor
SCBE	Substrate Current Induced Body effect
SI	Switched current
VFBCV [V]	flat band voltage
VTC	Voltage transfer characteristics
X_i	subcircuit of the i-pump stage
X_{LS}	subcircuit of the last pump stage

M_{D_i}	diode transistor
M_{si}	switch transistor
M_{pi}	inverter PMOS transistor
M_{ni}	inverter NMOS transistor
ϕ	the first-phase of the clock signal
$\bar{\phi}$	the second-phase of the clock signal

List of Tables

List of Figures

Contents

Chapter 1

Introduction

Discrete-time analog circuits (DtAC) have been developed since the second half of the 20th century. N-routes systems were originally used for the realization of the narrow bandpass filters (measurements purposes) and CCD sensors (system with the charge transition). Now, N-routes systems are on the decline. Subsequently, DtAC have been divided into two main groups according to the principle of the function as a result of the microelectronic technology development. Switched–capacitors circuits (SC) were firstly implemented in the early 80's and switched–current circuits (SI) [9] up in the 80's of the 20th century. The second mentioned group is still in the growth. These systems are characterized by analog switches operating in the dynamic mode, two variants are posibble from the view of its driving:

- Systems without driving–using mainly in the power applications.

- Systems with controlled switches. The circuits may include either internal or external clock signal circuit. Its using is in both power (high-voltage sources, controlled voltage rectifiers) and signal applications (integrated filters, A/D and D/A converters, modulators, *charge pumps*, special applications). A switch is nonlinear component that *samples* input analog signal. The sampling theorema must be respected: the digital clock signal frequency f_c must be at least an order greater then maximum value of the input signal frequency f_s, $f_c \gg f_s$ [7] (*Charge pumps are an exceptional case of DtAC, where the input "signal" is represented by the DC source voltage*).

Attention will be focused on SC circuits with the external clock signal designed for signal applications. Currently, SC circuits represent very perspective sector of quasi–analog systems. Options of the unipolar monolitic technology solve the basic problem associated with the integration of precise and stable resistor networks. The basic principle is based on the resistor simulated by the switched-capacitor [6], as it is shown in Figure 1.1. In case that the period of clock signal is sufficiently short compared to time change of the voltage $v_1(t)$ and the settling time of the switch is neglibly small, then the average current flowing through the capacitor is given by

$$i = \frac{\mathrm{d}Q}{\mathrm{d}t} \doteq \frac{\Delta \mathrm{Q}}{T_c} = \frac{C(V_1 - V_2)}{T_c} = \frac{C}{T_c}\Delta \mathrm{V} \tag{1.1}$$

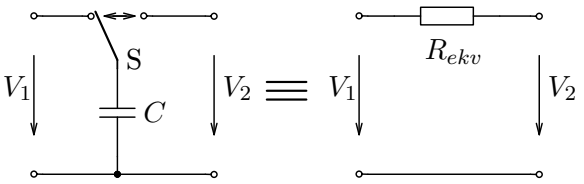


Figure 1.1: Equivalent circuit of the switched-capacitor

and the equivalent resistance value from (1.1) is equal to

$$R_{ekv} = \frac{T_c}{C} = \frac{1}{f_c C}, \tag{1.2}$$

where C is switched-capacitor value and $f_c = 1/T_c$ is clock frequency.

SC circuits are mainly used for the implementation of active filters–ARC structures. There are also special applications in an analog domain including integrated voltage converters–*charge pumps*. These circuits allow to convert (decrease, increase or invert) the input voltage. Charge pumps were originally constructed for high-voltage applications (particle accelerators that use electromagnetic field, high-voltage generators). Nowadays, charge pumps are important part of low-power integrated circuits [38], for example FLASH memories.

DtAC design represents the fundamental problem, which relates to the solution of the part steps of the design algorithm. The following three key steps are necessary for a successful design:

- *circuit model*,
- *simulation*,
- *evaluation of the simulation results.*

These are closed associated with the general description, as will be discussed bellow. Simulation must be exclusively done in *transient analysis*. Another type of analysis does not make sense in the *absence of the operating point*. It is a fundamental difference of approach compared to analog circuits. Optimization is usually long–time process due to many iterations to achieve of the required parameters (static, dynamic). *However, the optimal solution is not given unambiguously.* Feedback correction of the design procedure is very useful for this purposes (Fig. 1.2). Characterization system has been published in many books and research papers ([6,7]). However, universal design process has not been known. Quasi–analog systems take over some characteristics of the analog circuits and others from the digital circuits. Some important characteristics are summarized in the Table 1.1. DtACs (including SC circuits) behave as the digital circuit from the "system view" but during the period of the CLK signal are "seen" as an analog circuit. Respecting of this, two methods exist for the circuit description. First method takes into account the continuous nature of the processed signal. The system is described by the differential equations for each phase of the clock signal supplemented by the initial conditions. This method is complex but the computational algorithms are very difficult. Moreover, the transition into the frequecy domain often requires special form of the circuit functions. The second method neglects continuous signal in time and system is only described in the steady state

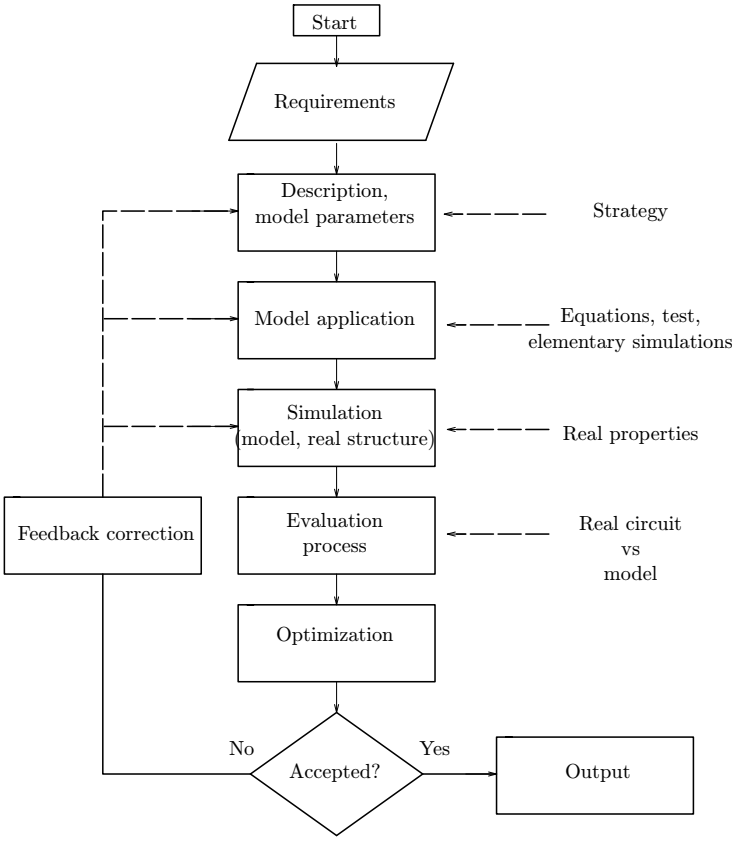


Figure 1.2: Simplified design algorithm of the DtAC

Table 1.1: Some properties of the DtAC

Analog systems	**Digital systems**
form of processed signal	signal processing in the discrete time
frequency limitation	clock signal
dynamic properties	ambiguous properties
environmental influence (temperature)	easy tunnable (filters)
reproducibility	easy integration

(digital circuit). Equations can be directly assembled in the frequency domain (Z–transform) [7]. It is very simple compared with the first method but the process leads to the *ideal case*. The following three methods are preffered for SC circuits in discrete–time domain [8]:

- **The equivalent resistors method.** Equivalent structure may be resolved by procedures that are specific for analog circuits. The most properties are not be considered (switch resistance, frequency properties, etc.), thus the output function is only an approximation of the real result.

- **The charge equation method.** The description is based on the SC circuit conversion to the frequency domain using the equivalent circuits. These circuits are derived from the charge matrix $\mathbf{Q} = \mathbf{C} \cdot \mathbf{U}$ that is equivalent of the admittance matrix $\mathbf{I} = \mathbf{Y} \cdot \mathbf{U}$.

- **State description.** The method is based on the principle that SC circuit is descibed by the state equations at the end of each phase. State equation from the last phase is also initial condition for the next phase (recurrent equations).

Notice that the inclusion of the real parameters into the calculation in discrete time is *limited to the mathematical tools to express transfer function* in the Z–transform. For example, it can be included: parasitic capacitances, finite gain of the active components.

Because DtAC is multiphase, it is also necessary to define the time interval in which the output of the circuit is active. Then DtAC is modeled by an N–branch circuit for each of the phase [8]. Control signal CLK is two–phase in the simplest case.

The thesis deals with specific type of the charge pump–**CROSS-COUPLED CHARGE PUMP** patented in 1998 [32], which rapidly solves the problem of the reverse current of the static pump. Nowaday this type of charge pump is still perspective block of the integrated structure; the main advantage is the simple topology, which is receiving the two-phase clock signal. Circuit may be commercially used (ASIC) without claims for patent right, thus **the pump is the subject of thorough research.** The analyzes were made in overview [33–39] but a detailed analysis and description has not been known yet. Published relationships [42–44] come from digital representation of the circuit whose consequences have been pronounced. Their application may not be automatically disapproved, but the model (described by the analytical equations) is usually accurate for a limited set of the parameters [41]. A slightly different path represents the addition of the digital model by the semi-emipric equations obtained by the simulation/measurement of the complex circuit. A number of blocks are modeled in this way, for example BSIM or EKV MOSFET models. Approximation of the measured curves is usually difficult process requiring special mathematical functions. Coefficients contained in the equations are, inter alia, dependent on the specific technological process.

The thesis offers an unconventional view on the charge pump, specifically one type of two-phase charge pump. Firstly, the basic conceptions of two-phase charge pumps are introduced, preceding the architecture of the cross-coupled charge pump. The main deals with the *description and design of the pump functional blocks as an analogue circuit* based on the *BSIM model equations*, i.e. operating modes of the active and nonlinear components are captured. Nonlinear system theory is applicable for both the estimation of the real N-stage pump properties (analysis part) and the pump design (synthesis part) via the *state-space model*.

The main benefit of Thesis is the design utility for analogue designers, which allows step by step synthesis on the circuit-level HW realization without the long-time numerical optimization process. High-voltage application asumes the long channel MOSFETs and strong inversion region, so that utility is compatible with other technology process, as PSP or EKV [29].

The program procedure for analysis and synthesis process was created in Maple SW [40] and all the formulae/procedures were verified in the professional design environment Mentor Graphics Design Architect-IC v2008.2_16.4 including the real models of the components, which are availabled in library MGC Design Kit [31].

Chapter 2

Two-phase charge pumps in overview

2.1 Dickson charge pump

The circuit topology in Fig. 2.1 consists of the chain of the diodes realized by the MOSFETs. Power supply voltage is connected to anode of M_{D_1} and load impedance R_L, C_L is connected to catode of M_{Dn+1}. Both the clock signals, labeled ϕ, $\bar{\phi}$, with amplitudes V_ϕ and $V_{\bar{\phi}}$, which are operating mutually in antiphase, are connected trough the main capacitors to node between catode of the M_{Di} and anode of the M_{Di+1}. Diodes ensure the transport charge and "isolates" the pump stages. In the first phase of the clock signal, when $V_\phi =$ "L", the main capacitors, which are connected to the odd stages, are charged (passive interval) and in the second phase, when $V_{\bar{\phi}} =$ "H", the potential in these nodes is increased and the charge is transported to the next stage (active interval). Voltage potential in the next node is reduced by the treshold voltage of the diode transistor V_{TH},

$$v_{i+1} - v_i^{'} \doteq V_{TH}$$

and voltage in the node i is reduced by the parasitic capacitor C_{si},

$$v_i^{'} = \frac{C}{C + C_{si}} v_i = \frac{1}{1+\beta} v_i,$$

where β is couple ratio.

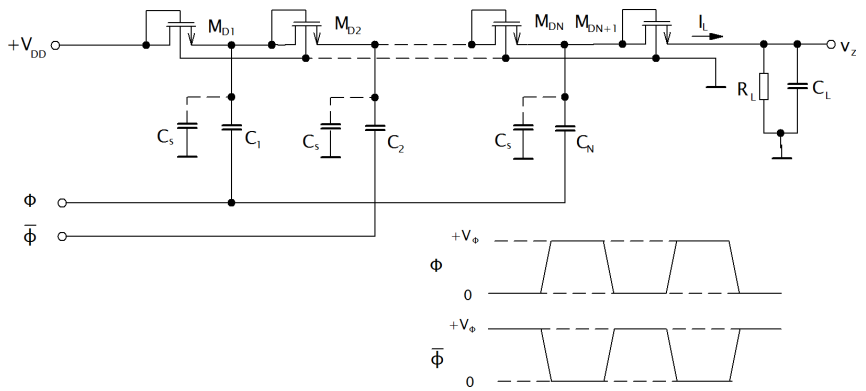


Figure 2.1: Dickson charge pump [38]

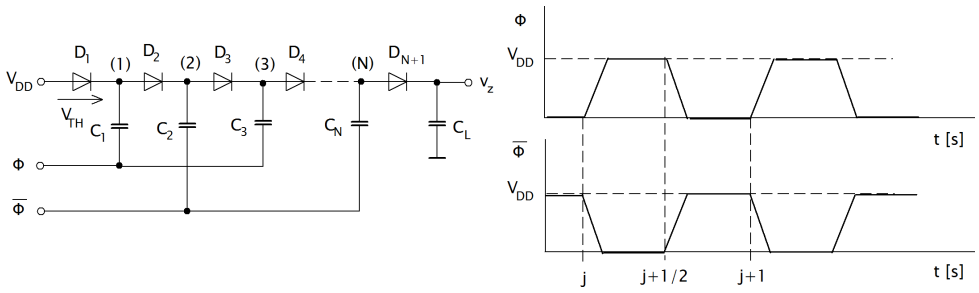


Figure 2.2: Timing in Dickson charge pump [4]

Repeating of the both cycles, output voltage v_{out} increases to the end voltage, whose maximal value is theoretically equal to

$$V_{out,max} = V_{DD} + N\left(\frac{\max\{V_\phi, V_{\bar{\phi}}\}}{1+\beta} - V_{TH}\right) - V_{TH}, \quad \text{for } I_L = 0. \tag{2.1}$$

When the pump output supplies load current I_L, then average value of the output voltage is given by

$$V_{out,av} = V_{out,max} = R_{pump} I_L = \frac{N}{f_c C(1+\beta)}, \tag{2.2}$$

where f is the cloc signal frequency and R_{pump} is an equivalent internal pump resistance calculated from SC technique (1.2).

Diode D_{n+1} is OFF in the low logic level of the V_ϕ, in this case, load capacitor C_L is discharged through the load resistance R_L. It causes the voltage drop, peak value is defined as [1, 2, 38],

$$V_r = \frac{I_L}{fC_L} = \frac{V_{out,av}}{fR_L C_L}. \tag{2.3}$$

2.1.1 Dynamic properties

In this section will be presented main dynamic pump properties: *rise time* and *internal pump equivalent capacitance*. Description of the circuit has character of the recurrent expression. Derivation is shown for only the pump with even number of stages, principle is the same for the second case. Accompanying scheme with timing diagram is in Fig. 2.2. Mathematical tool assumes the idealized structure. The following facts must be respected [1, 2, 4]:

- all the switches (MOSFETs) has the same and constant threshold voltage and zero leakage current,
- all the capacitors are ideal,
- parasitic capacitances are negligibly small,
- pulse width of the phase of the CLK is long enough for all the time RC constants in the circuit, amplitude of the CLK is V_{DD},
- rise time of the pump output voltage is very long in comparision with the clock cycle. Then, steady state in each of the pump nodes is assumed.

The capacitor C_1 is fully charged in the time j, in the node 1 is acumulated charge value,

$$Q_1 = C(V_{DD} - V_{TH}). \tag{2.4}$$

During the high logic level of $V_\phi = V_{DD}$, the charge is injected in node (1). Diode D_2 is ON and charge is transported to node (2). The transport is ended in the time $j + 1/2$ and potential in node (2) is increased,

$$V_2 = \frac{Q_2 + q_{inj}}{C}, \tag{2.5}$$

where Q_2 is the current charge in node (2) and q_{inj} is the part of the charge that is trasported after that the potential in node (1) was increased, i.e. $V_\phi = V_{DD}$ and $V_1 = V_2 + V_{TH}$.
New potential value in node (1) at the time $j + 1/2$ is equal to:

$$V_1 = V_{DD} + \frac{Q_1 - q_{inj}}{C}. \tag{2.6}$$

Combining (2.4) and (2.5),

$$V_{TH} = V_{DD} + \frac{Q_1 - q_{inj}}{C} - \frac{Q_2 + q_{inj}}{C}. \tag{2.7}$$

In the first phase, i.e. at the time j diode D_3 will be OFF and

$$V_{TH} = V_{DD} + \frac{Q_2}{C} - \frac{Q_3}{C}. \tag{2.8}$$

Combining (2.7) and (2.8),

$$Q_3 = 3C(V_{DD} - V_{TH}) - 2q_{inj}. \tag{2.9}$$

The following procedure is based on the same principle, as it was shown. In general form, the charge value in each of the nodes is defined as [41],

$$Q(2n-1) = C(2n-1)(V_{DD} - V_{TH}) - 2q_{inj}(n-1) \tag{2.10}$$

$$Q(2n) = 2nC(V_{DD} - V_{TH}) - 2q_{inj,} \tag{2.11}$$

where $1 < n < N/2$. Charge in the N$^{\text{th}}$ pump stage, when diode D_{N+1} is OFF, is given by

$$Q_N = C(V_{out,av} - V_{DD} + V_{TH}), \tag{2.12}$$

By comparing of both equations (2.11) and (2.12), relationship for injected charge was derived by Dickson [38]:

$$q_{inj}\frac{C}{N}\left[(V_{DD} - V_{TH})(N+1) - V_{out,av}\right]. \tag{2.13}$$

Combining (2.10), (2.11) and (2.13), the charge accumulated in each the main capacitor is calculated from:

$$Q(2n-1) = \frac{2C(n-1)}{N}\left(V_{out,av} - V_{DD} + V_{TH}\right) + C(V_{DD} - V_{TH}) \tag{2.14}$$

$$Q(2n) = \frac{2nC}{N}(V_{out,av} - V_{DD} + V_{TH}). \tag{2.15}$$

Total pump charge can be determined in 2 ways: *based on the charges that are stored in each of the capacitor* or from the *sum of the injected charges during the period of the CLK*. The sum of all the charges in the circuit, labeled $Q_{cc}(n,j)$, for $0 \leq n \leq N$ is given by [1, 2, 4, 38]:

$$Q^d_{cc}(j) = \sum_{n=1}^{N} Q_{cc}(k,j) = \sum_{n=1}^{N} n[Q(n,j) - Q(n,0)] + (N+1)[Q_{inj} - Q_{inj}(0)]. \tag{2.16}$$

Using the following initial conditions,

$$Q(2n,0) = 0, \tag{2.17}$$

$$Q(2n-1,0) = C(V_{DD} - V_{TH}), \tag{2.18}$$

$$Q_{inj}(0) = C_L(V_{DD} - V_{TH}), \tag{2.19}$$

which follow from (2.14) and (2.15). Using (2.12) (2.14) and (2.15), total charge in circuit is given by,

$$Q^d_{cc}(j) = (N+1)C_L^{'}(V_{out}(j) - V_{DD} + V_{TH}) \tag{2.20}$$

Load capacitance consists two parts: load capacitance C_L and pump capacitance C_{pump},

$$C_{pump} = \begin{cases} \frac{4N^2+3N+2}{12(N+1)}C, & \text{for even } N \\ \frac{4N^2-N-3}{12N}C, & \text{for odd } N. \end{cases} \tag{2.21}$$

Total charge, which is acumulated at time j is given by

$$Q_{cc}(j) = (N+1)\sum_{n=0}^{j} \frac{C}{N}\left[(N+1)\left(V_{DD} - V_{TH}\right) - V_{out}(m)\right]. \tag{2.22}$$

Combining (2.16) and (2.22), the follow charge equation is valid:

$$C_L^{'} = (V_{out}(j) - V_{DD} + V_{TH}) = \sum_{m=0}^{j} \frac{C}{N}\left[(N+1)(V_{DD} - V_{TH}) - V_{out}(m)\right] \tag{2.23}$$

and substituting of the the recursive expression to (2.23), then

$$C_L^{'}(V_{out}(j+1) - V_{out}(j)) = \frac{C}{N}\left[(N+1)(V_{DD} - V_{TH}) - V_{out}(j+1)\right]. \tag{2.24}$$

Substituting the initial condition $V_{out}(0) = V_{DD} - V_{TH}$ from (2.19) into (2.24), the output voltage at the time j becomes to

$$V_{out}(j) = (N+1)(V_{DD} - V_{TH}) + [V_{out}(0) - (N+1)(V_{DD} - V_{TH})]\,\lambda^j, \tag{2.25}$$

where $\lambda = \frac{1}{1+\frac{C}{NC_L'}}$.

Rise time, during of it the pump output voltage increases from initial value $V_{out}(0)$ to end voltage value V_{fin} was derived by Tanzawa and Tanaka [1]:

$$\boxed{T_r = \frac{\ln\left[1 - \frac{V_{fin} - V_{out}(0)}{N(V_{DD} - V_{TH})}\right]}{\ln(\lambda)} \frac{1}{f}} \tag{2.26}$$

Average value of the power supply current during the time T_r is calculated from:

$$I_{DD} \approx \frac{Q_{cc}(T_r)}{T_r} = \frac{(N+1)(V_{fin} - V_{out}(0))C_L'}{T_r}, \tag{2.27}$$

similarly, average value of the load current is given by:

$$I_L = \frac{C_L'(V_{fin} - V_{out}(0))}{T_r}. \tag{2.28}$$

Now, power dissipation and output power are defined as,

$$P_{in} = \sum_{j=0}^{T_r} \frac{q_{cc}(j)V_{DD}}{T_r} = \frac{(N+1)(V_{fin} - V_{out}(0)V_{DD}C_L'}{T_r}, \tag{2.29}$$

$$P_{out} = \sum_{j=0}^{T_r} \frac{q_{inj}(j)V_{out}(j)}{T_r} = \frac{1}{2}C_L' \frac{V_{fin}^2 - V_{out}^2(0)}{T_r} \tag{2.30}$$

and dynamic efficency during T_r is given by

$$\boxed{\varepsilon_{T_r} = \frac{P_{out}}{P_{in}} = \frac{V_{fin} + V_{out}(0)}{2(N+1)V_{DD}}}. \tag{2.31}$$

Dynamic efficiency is approximately equal to half of the efficiency in the steady state [38]:

$$\boxed{\varepsilon_s = \frac{V_{DD} + N\left[\frac{\max\{V_\phi, V_{\bar{\phi}}\}}{1+\beta} - V_{TH} - \frac{I_L}{fC(1+\beta)}\right]}{(N+1)V_{DD}}}. \tag{2.32}$$

The charge pump is modeled by the analogue prototype [38], see Fig. 2.3. However, it does not mean that circuit reflects the dominant effects of the real structure, as it was explained in introduction. The dominant parts of the pump losses are primarly threshold voltage and body effect and parasitic capacitances, which can be also included into the previous equations. Derivation was done, for example, in [4,5,41]. Mentioned description is usually used for practical design, despite its shortcomings. Simplicity of the implementation is main advantage of the description. Experiments and verification of all the pump characteristics are listed in [3, 5, 41].

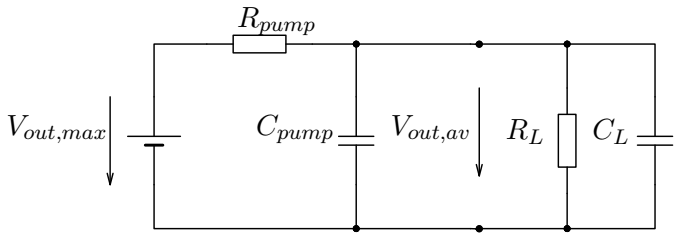


Figure 2.3: Equivalent circuit of the charge pump [38]

Problems of the circuit description exist in case of more advanced topologies. Although these increase efficiency, show the other effects, whose mathematical expression is difficult.

2.2 Static pump CTS-1

Static pump CTS-1 (Charge-Transfer-Switch) to some extent eliminates threshold voltage transfer elements so that the switch transistor is connected in parallel to the diode in each of the pump stages. Diagram is shown in Fig. 2.4 Each of the switch transistor, whose Drain and

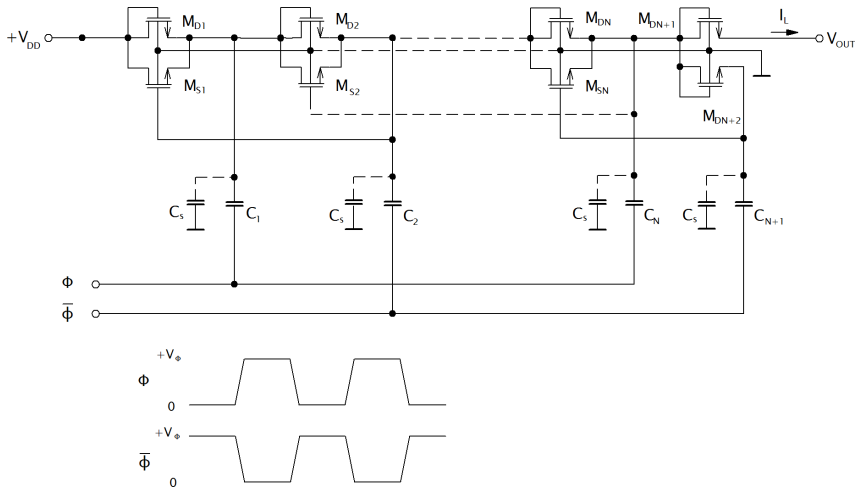


Figure 2.4: CTS-1 charge pump [32]

Source is connected between nodes i and $i+1$, is drived by the higher voltage from the next stage, i.e. Gate is connected to node $i+2$. The feedback is implemented locally in each stage. Principle is the same as the Dickson charge pump, however, M_D transistor is shorted in the phase of charging, thus its treshold voltage does not apply. Voltage drop between two nodes after the charge transport is theoretically given by the switch transistor saturation voltage,

$$G_v = v_{i+1} - v_i \to 0.$$

Threshold voltage (and body effect) is only applied at the last diode D_{N+1}, which is connected to load impedance. Considering the linearization function of the threshold voltage on the source-

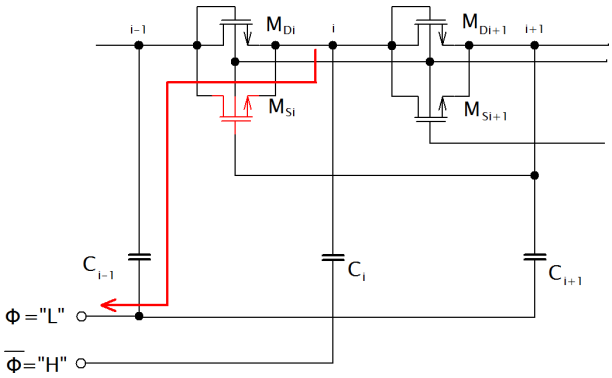


Figure 2.5: Reverse charge transport in CTS-1 charge pump [42]

bulk bias voltage [41],

$$V_{TH} \approx V_{TH0} + aV_{SB}, \tag{2.33}$$

where a is the regression parameter and V_{TH0} is the treshold voltage at zero bias voltages, then the theoretical value of output voltage is given by [41],

$$V_{out,max} = \alpha \left(V_{DD} + N \cdot \max\{V_{\phi}, V_{\bar{\phi}}\} \frac{1}{1+\beta} \right), \quad \text{for } \alpha > 0 \tag{2.34}$$

and relationship for equivalent internal resistance is the same as for Dickson charge pump. Parameter α is linearized body effect factor and it is calculated from [41]:

$$\alpha = \frac{1}{1+a}.$$

The real circuit does not work in spite of expectations, see Fig. 2.5. When ϕ = "H" and $\bar{\phi}$ = "L", voltage in the node i is $V_{DD} + V_{\phi}$ and voltage drop is G_{v_i}. Otherwise, when ϕ = "L" and $\bar{\phi}$ = "H" transistor M_{s_i} must be OFF because of the transport charge from node i to node $i+1$. Critical situation will happen, when the voltage at node $i+1$ exceeds the threshold voltage of the transistor M_{si}. After that M_{s2} is ON and charge is transported from node i to node $i-1$. *Reverse charge transport* is realized, provided that [38],

$$\boxed{2G_{v_i} > V_{TH_{M_{si}}}}. \tag{2.35}$$

This is a controversial moment, since condition 2.35 is also a necessary condition for closing the feedback in the circuit, i.e. the minimum voltage needed to turn ON the switch transistor. Many modified circuits are currently patented to eliminate this effect in part, among them, the cross-coupled charge pump.

Chapter 3

Cross-coupled charge pump

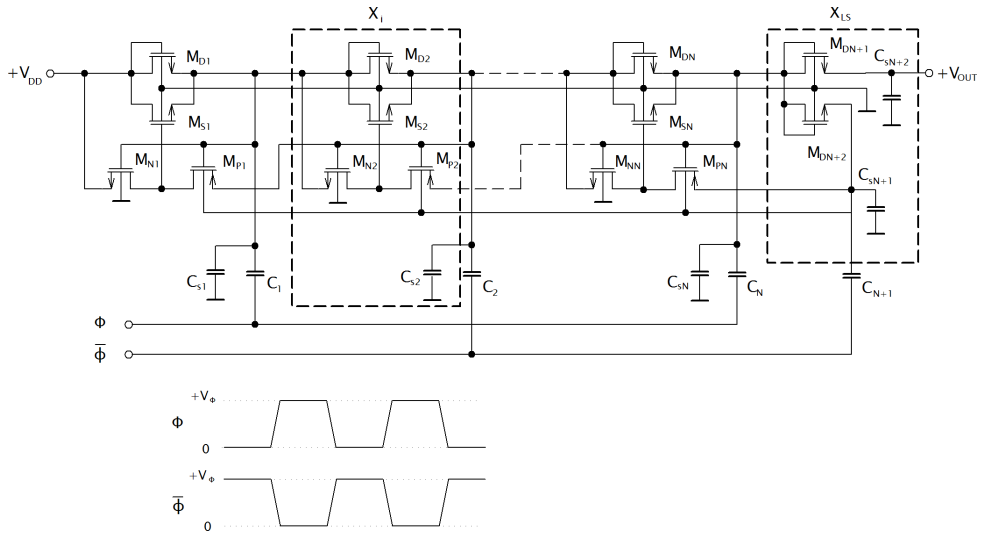


Figure 3.1: Cross-coupled charge pump [32]

Cross coupled charge pump is based on the principle of Dickson charge pump. N-stage architecture [32] is additionally supplemented by the switches (transistors M_{S1}–M_{SN}) in order to eliminate threshold voltage of the diodes realized by MOSFET transistors M_{D1}–M_{DN} (CTS-1 architecture [42]). Voltage drop between the Drain and Source of the switch MOSFET is theoretically determined by the saturation voltage at the end of the charge transport. It allows to achieve higher efficiency. Main capacitors C_i provides transport charge that is controlled by two–phase clock signal ϕ and $\bar{\phi}$. In the first phase, in low logic CLK level, the main capacitors belonging to this state are charged and in the second phase, at high logic level of CLK, node voltage is increased on the output of the stage and the stored charge in capacitor is transported into the next stage. Switch transistor in each stage is controlled by the output signal of the inverter (M_{Ni}, M_{Pi}) that is supplied by higher voltage from the next stage(feedback signal). The control circuit ensures that switches will be turned on/off in the time intervals defined by the logic levels of the clock signal. The maximal output voltage is theoretically given by

$$V_M = (N+1)V_{DD} - V_{THM_{DN+1}}, \tag{3.1}$$

where N is number of stages, V_{DD} is supply voltage and $V_{TH(DN+1)}$ is threshold voltage of the transistor $M_{D_{N+1}}$.

Discharging of the main capacitors due to load current in the passive interval of the CLK is indicated by the drop of the output voltage. Average value of the voltage on the resistive load is derived from SC technique (Eq. 1.2), then

$$V_{out,av} = V_{out,max} - \frac{N}{f_c C} I_L = \frac{V_M}{1 + \frac{N}{fCR_L}}, \tag{3.2}$$

where f_c is clock signal frequency, C is main capacitor and I_L is average value of load current.

Required number of stages to achieve a desired output voltage is characterized by pump voltage efficiency η_v[1],

$$\eta_v = \frac{V_{out,av}}{(N+1)V_{DD}}. \tag{3.3}$$

Some real properties of the charge pump will be discussed and shown in the simulation results in this section. Charge pump has been tested by the professional simulator ELDO. The various types of MOSFETs, M_{Si}, M_{N_i}, M_{Pi} and M_{D_i} are the same size in each pump stage.

Static and dynamic parameters were simulated for the specific parameters that are (unless noticed otherwise) given in Table 3.1. The elementary simulation of the output voltage in

Table 3.1: Simulation parameters

Parameter		**Value**
Temperature	ϑ	24 °C
Number of stages	N	2
Supply voltage	V_{DD}	1V
CLK frequency	f_c	10 MHz
Main capacitance	C	5 pF
Load ressistance	R_L	100 k
Load capacitance	C_L	10 pF
Threshold voltage of	V_{TH0_N}	0.35 V
NMOS and PMOS at V=0	$\lvert V_{TH0_P}\rvert$	0.33 V
Channel length of N(P)MOS	L	1μ m
W/L ratio of the M_{Si}	W_s/L_s	2
M_{Pi}	W_p/L_p	3
M_{Ni}	W_n/L_n	1
M_{Di}	W_d/L_d	25

steady state was performed in the first instance and compared with the known theoretical solution from the previous. The table 3.2 lists the average output voltage vs. number of stages including percent error ε_{Vout} of the calculation value from Eq. 3.2 and voltage pump efficiency η_v. Analysis results show definitely mismatch between measured and calculated values due to description of ideal case. There are many reasons why the transport charge is lossy. The losses can be divided into two main groups: static and dynamic losses. First, dynamic losses are

[1]Voltage static efficiency ignores power consumption, as is apparent from definition of it. Real energy efficiency is allways less than η_v.

Table 3.2: Static and dynamic paramters of the charge pump

N[-]	$V_{out,av}$[V]	$\varepsilon_{r_{Vout}}$[%]	η_v[%]
1	1.12	32.5	56
2	1.54	17.9	51.3
3	1.89	14.86	47.25
4	2.19	12.4	43.8
5	2.41	11.4	40.17

caused by the capacitive coupling between stages (charge injection). These occur at quick time changes, typically during rising and falling edge of the clock signal. Dynamic losses depend on the frequency and affect total current consumption.

Second, static losses decrease voltage at each node, thus limit output voltage. Strange capacitance [38] connected to each of the nodes (see Fig. 3.1) is significant component of the static losses. It can be interepreted by the parasitic capacitance of MOSFETs or layout capacitances, it creates the voltage divider with main capacitance,

$$V_{DD}^{'} = V_{DD}\frac{C}{C + C_s}.$$

Threshold voltage is critical parameter, because it represents potential barrier for the input voltage. A sufficiently high voltage must be applied to gate of the switch transistor M_{Si} for suppression of the threshold voltage of transistor M_{Di}. It means that the voltage gain G_V of the stage must be greater then

$$G_V > \frac{V_{TH}}{2} \tag{3.4}$$

for the correct function. *Provided the condition (5.12) is not satisfied, the circuit operation is the same as Dickson charge pump.* Therefore, the function of the output voltage and efficiency have discontinuities, as is shown in Fig. 3.4 and 3.6.

Threshold voltage is strongly dependent on the bulk–source bias voltage (Body effect), V_{TH} = f(V_{SB}). Body effect is applied when the source and substrate (body) are not at the same potential. Main capacitor is connected to the source of N-MOSFETs, while the bulk must be grounded(connected to the lowest potential in the circuit). The bulk of P-MOSFETs is connected to the pump output voltage. N-MOSFETs and P-MOSFETs will have a considerably different threshold voltage in the same technology process. Threshold voltage is given by the following simplified equation for *long channel* MOSFET [22–24, 38]:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\phi_s - V_{SB}} - \sqrt{\phi_s}\right), \tag{3.5}$$

where V_{TH0} is threshold voltage at zero bias voltages, ϕ_s is surface potential and γ is body effect coefficient (calculated from the model parameters). Condition (5.12) takes into account the threshold voltage of the switch transistor but must also comply to threshold voltage of the transistors M_{Pi} and M_{Ni}. Therefore, generalized condition for cross-coupled charge pump has

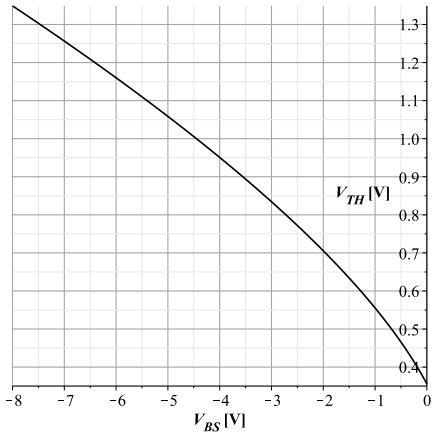


Figure 3.2: Threshold voltage vs bulk-source bias voltage

the following form:

$$\frac{V_{TH_{Msi}}(V_{SB})}{2} < G_V > \frac{|V_{TH_{MPi}}(V_{BS})| + V_{TH_{MNi}}(V_{SB})}{2}. \tag{3.6}$$

This circuit eliminates *moderately* reverse charge transport during the phase of the CLK, compared with the previous version CTS-1 [42], in which gate of the switch transistor is directly connected to the output of the next stage (without the inverter). However, this problem still exists in actual version (see Fig. 3.3). Reverse transport charge is caused by the *reverse current*

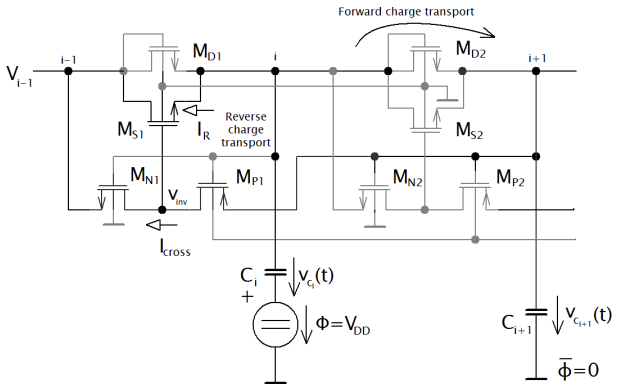
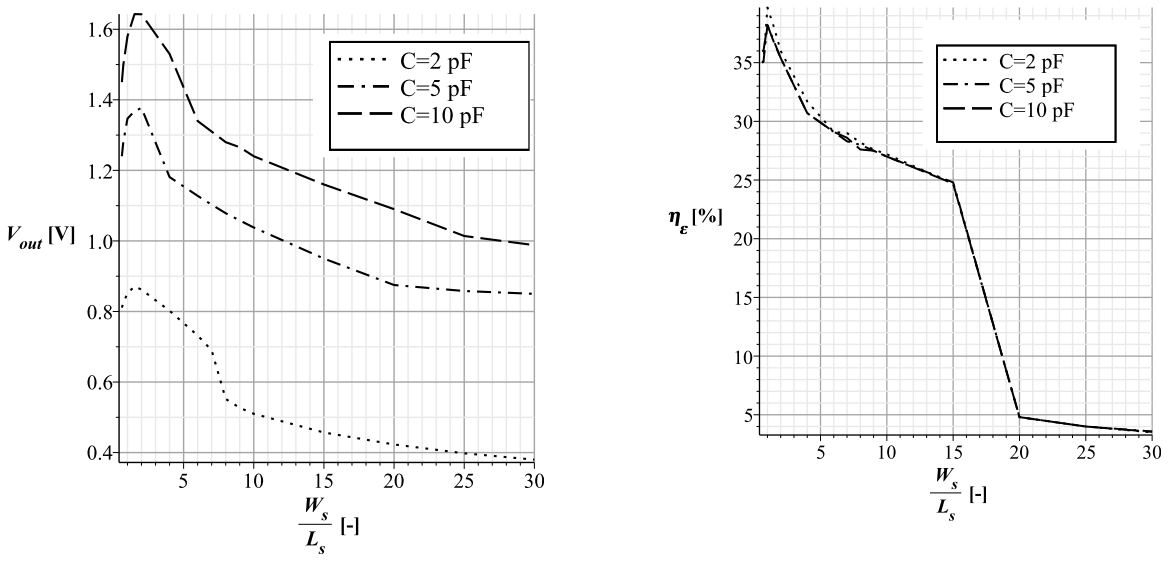


Figure 3.3: Reverse charge transport

of the switch transistor I_r and *the inverter cross current* I_{cross}. Both of the effects are the results of the fact that *the energy stored in capacitor(s) must be a continuous function of time.* Reverse current flows from node (i) to node $(i-1)$, while cross current I_{cross} flows from node $(i+1)$ to node $(i-1)$. Both the current loops are higlighted in Fig. 3.3.

Reverse current is carried out, if the immediate reverse voltage gain $\Delta V_r > 0$ and $v_{inv} - v_{(i-1)} > V_{TH_{Msi}}$. Implying that, disproportionately large ratio W_s/L_s of the switch transistor greatly decreases the output voltage. The optimal point exists in characteristics (see Fig. 3.4), in which the *output voltage* (Fig. 3.4a) and *pump efficiency* (Fig. 3.4b) come up to the maximum value. This is a very important knowledge for the practical design.



(a) (b)

Figure 3.4: Output voltage (a) and power efficiency (b) vs. W_s/L_s ratio and the main capacity as the parameter

Power efficiency from Fig. 3.4b as the dynamic parameter is determinated by the mean output power P_{out} divided by the total mean input power P_{in} in steady state (when the average value of output voltage and current will be constant with time).

$$\eta_\varepsilon = 100 \cdot \frac{P_{out}}{P_{in}} = 100 \cdot \frac{P_{out}}{P_\phi + P_{\bar{\phi}} + P_{V_{DD}}}, \tag{3.7}$$

where $P_\phi + P_{\bar{\phi}}$ is total mean power supported by the clock signal generator and $P_{V_{DD}}$ is mean power supported by the DC source voltage.

CMOS inverter [23] should switch on the transistor M_{Si} during charge transport and switch off it during charging of the main capacitor. However, inverter behaves as an analog block despite its primary function in the circuit. The output voltage of the inverter v_{inv} can be in undefined state from the view of logic levels. It means, the operating point is in the linear part of the voltage transfer characteristics (VTC) and both the transistors M_{Pi} and M_{Ni} are ON. The cross current is maximum at point $v_i = v_{inv}$. This point is called inverter switching point V_{SP} [23], see Fig. 3.5. Input voltage range of the linear part of the VTC (including point V_{SP}) is equal to difference $V_{IH} - V_{IL}$, where V_{IL} and V_{IH} are input voltages that define inverter output logic levels. These values are set by the values $(i+1)$, $(i-1)$ and *sizing of the inverter MOSFETs. The relationship between between* I_r *and* I_{cross} *is obvious because* $I_{cross} = f(V_{SP})$ *and* $I_r = f(V_{inv})$.

Thus, dependence of the pump output voltage on the cross current (via sizing of the transitors M_{Pi} and M_{Si}) should be analyzed respecting the following conditions because of the objective evaluation:

- Reverse current must be suprresed as much as possible, so that $I_r \to 0$. The ratio W_s/L_s is set to the point, in which the output voltage is maximum, as shown in Fig. 3.4.

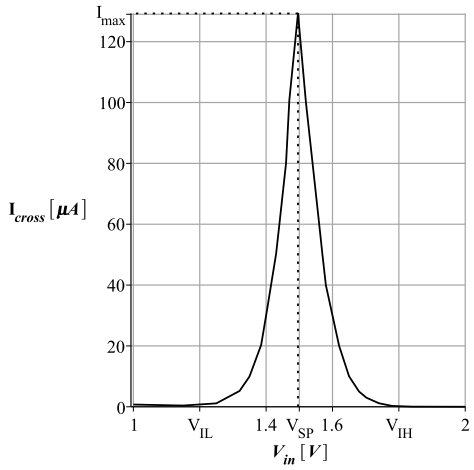


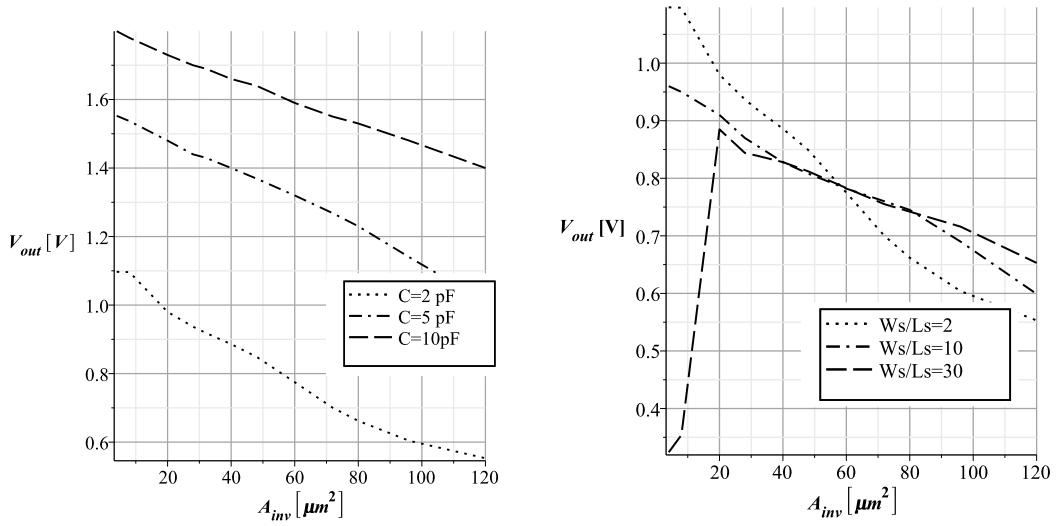
Figure 3.5: The CMOS inverter cross current characteristics

- Reverse control voltage of the switch transistor must be (about) same. It means that voltage range of the linear part of VTC characteristics is kept ($V_{SP} \approx$ const.) with increasing the ratio W_{Ni}/L_{Ni} and W_{Pi}/L_{Pi}. Consequently, it is necessery to increase together width of both transistors at fixed channel length (see Tab. 3.1).

Total inverter area, labeled A_{inv}, is calculated from:

$$A_{inv} = W_{Ni}L_{Ni} + W_{Pi}L_{Pi} \tag{3.8}$$

and the corresponding graph is shown in Fig. 3.6a, the relationship between sizing of the switch transistor and the inverter total area is shown in Fig. 3.6b. Both the characteristics were simulated for $\frac{W_{Ni}}{L_{Ni}}/\frac{W_{Pi}}{L_{Pi}} = 1/3$ (symmetrical inverter).



(a) (b)

Figure 3.6: Pump output voltage vs. total inverter area, main capacity (a) and the W_s/L_s ratio (b) as the parameter

Chapter 4

Disertation thesis targets

The current state of the issue is a challenge to build a credible pump model based on the symbolic description including the dominant properties of the real structure on the circuit-level, which allow to the synthesis without long-time simulation process. This is the main target of the thesis. The pump draft is focused on two main criteria from the set of the possible solutions, which are provided to designers through the design utility: **circuit optimal draft– maximal pump voltage gain** and **economically beneficial solution–minimal pump area on a chip**.

The secondary aim of the thesis is an alternative way of the systems description, whose algorithm can be applied in the circuits based on a similar principle, typically voltage converters.

Chapter 5

Description of the pump functional blocks

5.1 BSIM model equations

BSIM model involves many effects in real integrated structure, which are drescribed in BSIM manual [27]. It contains many model parameters and computation is very difficult (implicit form, solving of irational equations, etc.). So, the equations will be simplified for specific case. Satisfied for MOSFET operation in high voltage circuits is $V_{GS} >> V_{TH}$. Following conditions must be true:

- long channel MOSFET
- strong inversion region.

Channel length is important paremeter because of a *breakdown voltage*. Electrical field in structure induced by applied voltage must be more less than critical electrical field, $E = \frac{V}{L_{eff}} \leq E_{crit}$, where L_{eff} is effective channel length. Critical electrical field is limited to value given by semi-empiric model [27].

The effective channel length is relative to the applied voltage V_{max} (gate-source, drain-source) defined as

$$L_{eff} \gg V_{max} \frac{\mu_{eff}}{2v_{sat}}, \tag{5.1}$$

where v_{sat} is saturation velocity (model parameter) an μ_{eff} is effective mobility.

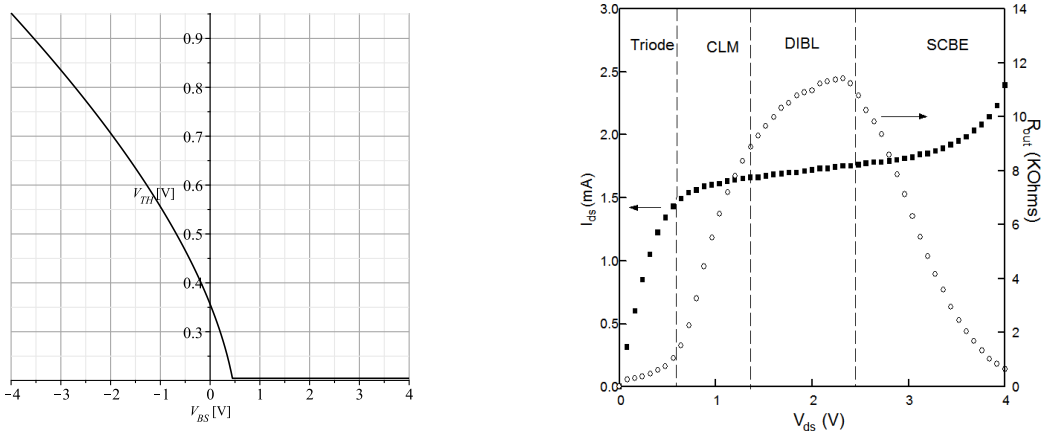
Accurate modeling of *threshold voltage* is important for precise description of device electrical characteristics. Threshold voltage for long and wide MOSFETs with non-uniform substrate vertical doping [27] is defined as

$$V_{TH} = \begin{cases} V_{TH0} + K_{1ox}\sqrt{\phi_s - V_{BS}} - K_1\sqrt{\phi_s} - K_{2ox}V_{BS}, & \text{for } V_{BS} \leq V_{bound}, \\ V_{TH0} + K_{1ox}\sqrt{\phi_s - V_{bc}} - K_1\sqrt{\phi_s} - K_{2ox}V_{bc}, & \text{for } V_{BS} \geq V_{bound}, \end{cases} \tag{5.2}$$

where V_{TH0} is threshold voltage at zero bias voltages, ϕ_s is surface potential, K_1, K_2 are body effect coefficients calculated from model parameters and V_{bc} is the maximum is the maximum allowable voltage V_{BS} calculated from $\mathrm{d}V_{TH}/\mathrm{d}V_{BS} = 0$ [27]. Threshold voltage is expressed by the single equation through the effective voltage $V_{BS_{eff}} = f(V_{BS})$ for smooth transition between forward and reverse polarity of the diode Source-Bulk[1]. Dependence of the threshold voltage on the voltage V_{SB} can be approximated by two simple functions in according to Eq. 5.2. Boundary point between both the regions, labeled V_{bound}, follows from condition

$$V_{TH}(V_{BS_{eff}})|_{V_{BS}\to+\infty} = V_{TH}(V_{BS_{eff}}). \tag{5.3}$$

Considering $V_{BS_{eff}} \approx V_{BS}$ (for $V_{BS} < 0$) then *this point is equal to surface potential* ϕ_s.



(a) (b)

Figure 5.1: Static characteristicsof MOSFET: threshold voltage vs source-bulk voltage (a) and output I-V characteristics and resistance [27]

.

Drain current model is given by single equation [27]. Transition from triode to saturation region is ensured through an effective drain-source voltage.

$$V_{DSeff} = \begin{cases} V_{DS}, & \text{for triode region} \\ V_{DSsat}, & \text{for saturation region} \end{cases} \tag{5.4}$$

and for long channel MOSFETs, saturation drain current $V_{DS} = V_{DSsat}$ is given by:

$$I_{Dsat0} = \frac{1}{2}\frac{W}{L} c_{oxe} \mu_{eff} V_{DSsat}(V_{GS} - V_{TH}), \tag{5.5}$$

where c_{oxe} is electrical oxide capacitance. Boundary between triode and saturation region is predicted by voltage $(V_{GS} - V_{TH})$, applies bias voltage effect and further model parameters (channel length and width...) included in bulk-charge equation [27], labeled A_{bulk}. A_{bulk} is

[1] $V_{BS_{eff}}$ is incorrectly defined in BSIM manuals [26–28]. The wrong relationship is copied into new versions of BSIM models

closed to unity for relatively high source-bulk bias voltage. In the other words,

$$V_{DSsat} = \frac{V_{GS} - V_{TH}}{A_{bulk}}. \tag{5.6}$$

Generally, the output I-V curve in saturation region ($V_{DS} > V_{DSsat}$) is written by several physical mechanisms, as it is shown in Fig. 5.1. Nevertheless, respecting condition (5.1) can be neglected short channel effect - channel length modulation (CLM) and Substrate Current Induced Body effect (SCBE). Then the drain current increases linerly with the V_{DS} voltage. The slope of the output characteristics is mainly determined by Early voltage V_{ADIBL} due to drain-induced barrier lowering (DIBL) effect [23,24,27,28]. V_{ADIBL} is directly proportional to the voltage V_{GS}, as shown bellow. Moreover, equation (5.7) contains model parameters PDIBLC2 and PDIBLCB [27],

$$V_{ADIBL} = \frac{1}{2}\frac{V_{GS} - V_{TH}}{\mathrm{PDIBLC2}\,(1 - \mathrm{PDIBLCB}\,V_{SB})}. \tag{5.7}$$

The complex drain current equation becomes

$$I_D = I_{Dsat0}\left(1 + \frac{V_{DS} - V_{DSsat}}{V_{ADIBL}}\right), \quad \text{for } V_{DS} \geq V_{DSsat} \tag{5.8}$$

Drain current in triode region is a function of the V_{DS} voltage (V_{GS} = const.). Maximum of parabolic function I_{DS0} =f(V_{DS}) corresponds to the voltage V_{DSsat} because of the neglecting CLM mechanism [23, 24, 27, 28]. Then, relationship between drain-source voltage V_{DS} and the saturation drain current I_{Dsat0} [24] can be simply written as

$$I_{DS0}\,(V_{DS}) = -\frac{I_{Dsat0}}{V_{DSsat}^2}V_{DS}^2 + \frac{I_{Dsat0}}{V_{DSsat}}2V_{DS}. \tag{5.9}$$

Dynamic part of the MOSFET uses Ward´s capacitance model [25,27,28]. The capacitances between electrods i and j, labeled C_{ij}, are derived from the charge Q_i and control voltage V_j to ground [27]:

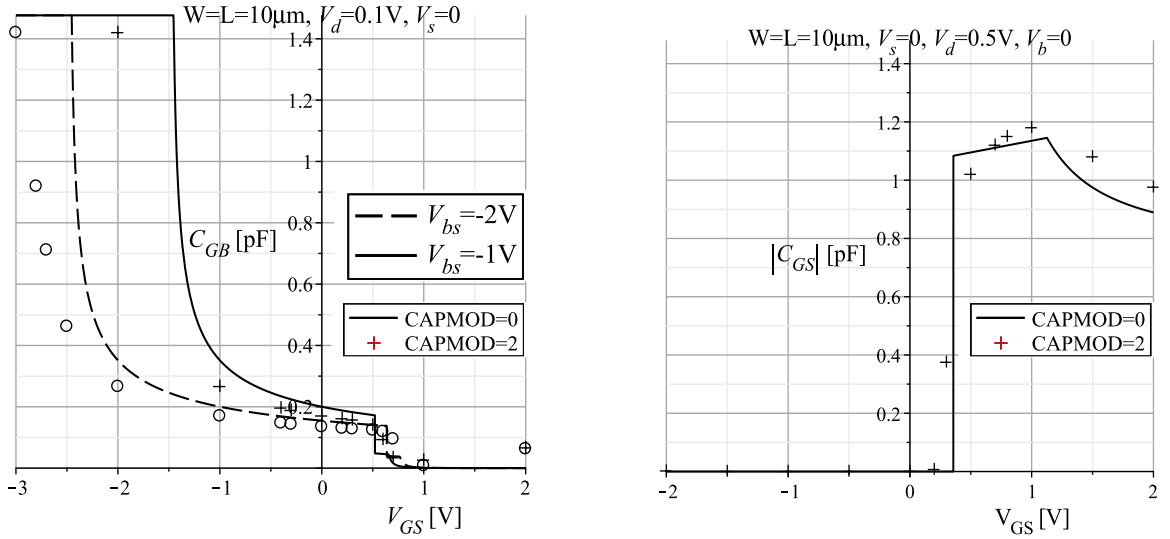
$$C_{ij} = \frac{\partial Q_i}{\partial V_j}. \tag{5.10}$$

Capacitances can be understood as the coefficients with Farad unit and sign ± 1 because of the definition of the time-varying currents. These model parameters are not physical capacitors. According to definition 5.10, the capacitive balance equation must be valid [27]:

$$\sum_i C_{ij} = \sum_j C_{ij} = 0 \tag{5.11}$$

BSIM model differentiates the expression of the charge equations Q_s, Q_d, Q_b and Q_g [27]. Capacitance model contains modified equations of the static model (threshold voltage, bulk charge effect, saturation drain-source voltage, ...) to define these charges. The expression for a particular circuit is set by the parameter CAPMOD. The basic model (CAPMOD=0 for BSIM 4.6.4) use the piecewise model, on contrary, modes CAPMOD=1,2 are using single-equation model including many other physical effects in real MOSFET structure (short channel effects,

charge thickness). Application of single charge equation is very complicated and using of this is even unnecessary with regard to the required capacitance accuracy (thents of pF). Comparison of the analysis results between the piece-wise model (CAPMOD=0) and single equation capacitance model (CAPMOD=2) is shown in Fig. 6.19. **Analytical description of HVT MOSFET capacitances for CAPMOD=0 is indicated by a line in graphs**.



(a) (b)

Figure 5.2: MOS gate capacitances: gate–bulk (a) and gate–source capacitance (b)

The charge division between the drain and the source is set according to the character of the signal in circuit through the parameter XPART. Simulating the charge pump, *XPART=1* (drain/source 0/100).

5.2 CMOS inverter

CMOS inverter is a basic block (Fig. 5.3) for digital design circuits which performs a logic operation of A to $\overline{A}$. Inspite of that, there are also aplications in analog domain, both continous–time circuits (oscillators, amplifiers) and discrete–time analog circuits (voltage converters). Results of

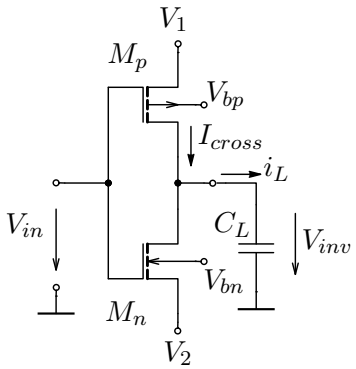


Figure 5.3: Diagram of the CMOS inverter.

the transient analysis (see Fig. 3.6) show the dominant part of losses in charge pumps is caused

by a DC cross current, while the propagation delays affects the dynamic power dissispation [13,15,16,22,24]. Description of the CMOS inverter characteristics represents complicated matter due to many combinations of the operating regions of both the MOSFETs [10,12,17,18,23]. Except for a typical case, when the inverter is operating in strong inversion region under basic condition (3.6) and $I_{cross} \gg 0$, other cases, as subtreshold region of MOSFETs [14], can occure. These are also modeled for three main reasons:

- guidlines on the inverter MOSFETs transistor sizing,
- inverter output voltage can put the switch transistor into a strong inversion region, i.e. $I_s \gg 0$ although the inverter is not operating in strong inversion region (inverter cross current is considered zero),
- inverter output voltage must be defined under all circumstance due to application of the complex model in state model (convergence of the numerical algorithm).

Diagram of the CMOS inverter schematic is shown in Fig. 5.3a. All voltages are referenced to the *ground*. It is considered that output voltage swings between values V_1 and V_2. When the input terminal is connected to the voltage $V_{in} \leq V_{IL}$, the output is pulled to V_1, when $V_{in} \geq V_{IH}$, the output is pulled to V_2.

5.2.1 Strong inversion

Power supply voltage of the invertor must fullfil the basic condition

$$V_1 - V_2 > \left|V_{TH_{M_{Pi}}}\right| + V_{TH_{M_{Ni}}} \tag{5.12}$$

to turn on both of the transistors M_1 and M_2 in the interval $V_{in} \in \langle V_{IL}, V_{IH} \rangle$, where V_{IL} and V_{IH} are the switching levels, see Fig. 5.4 Derivation of the Voltage transfer characteristics is based on the fact that drain current of both MOSFETs must be equal for each of the operating region, see Fig. 5.4a. In the first region, transistor M_{Pi} is operating in triode region, while transistor M_{Ni} in stauration region ($V_{in} - V_2 > 0$ and $V_{in} - V_2 < V_{TH_{MNi}}$). Cross current is practically zero, however, the following equality is valid:

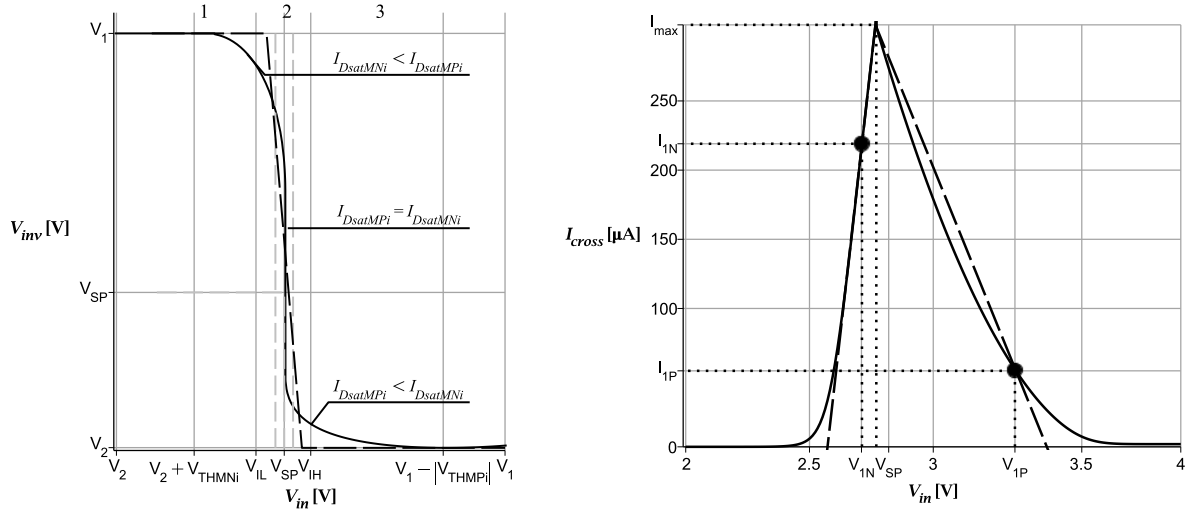
$$I_{Dsat0_{MNi}}|_{V_{GS}=V_{in}-V_2} = I_{DS0_{MPi}}|_{V_{SG}=V_1-V_{in}, V_{SD}=V_1-V_{inv}}, \tag{5.13}$$

where I_{Dsat0} is the drain current in saturation region at $V_{DS} = 0$ and I_{DS0} is the drain current in triode region of the respective transistor.

In the third region, the state of transistors is contrary to the previous case,

$$I_{Dsat0_{MPi}}|_{V_{SG}=V_1-V_{in}} = I_{DS0_{MNi}}|_{V_{GS}=V_2-V_{in}, V_{DS}=V_{inv}-V_2}. \tag{5.14}$$

and in the second region, both transistors M_{Pi} and M_{Ni} are in the saturation region ($V_{DS} > V_{DS_{sat}}$). The slope of the transfer characteristics is determined by Early voltage due to DIBL



(a) (b)

Figure 5.4: Inverter static characteristics: voltage transfer char. (a) and cross current char. (b) and their linearization

effect. Drain current both of MOSFETs in saturation region (Eq. 5.8) must be same,

$$I_{Dsat_{MPi}}|_{V_{SG}=V_1-V_{in},V_{SD}=V_1-V_{inv}} = I_{Dsat_{MNi}}|_{V_{GS}=V_{in}-V_2,V_{DS}=V_{inv}-V_2}. \tag{5.15}$$

Combining Equations (5.13), (5.14), (5.15), the complex equation of the inverter voltage transfer characteristics is calculated from

$$V_{inv}(V_{in}) = \begin{cases} V_1, & \text{for } V_2 \le V_{in} \le V_2 + V_{TH_{MNi}} \\ \frac{I_{Dsat0_{MPi}}(V_1 - V_{DSsat_{MPi}}) + \sqrt{I_{Dsat0_{Mpi}} V^2_{DSsat_{MPi}} (I_{Dsat0_{MPi}} - I_{Dsat0_{MNi}})}}{I_{Dsat0_{Mpi}}}, & \text{for region 1} \\ \frac{I_{Dsat0_{MPi}}[1+\lambda_{MPi}(V_1 - V_{DSsat_{Mpi}})] - I_{Dsat0_{MNi}}[1-\lambda_{MNi}(V_2 + V_{DSsat_{MNi}})]}{I_{Dsat0_{MNi}}\lambda_{MNi} + I_{Dsat0_{MPi}}\lambda_{MPi}}, & \text{for region 2} \\ \frac{I_{Dsat0_{MNi}}(V_2 + V_{DSsat_{MNi}}) - \sqrt{I_{Dsat0_{MNi}} V^2_{DSsat_{MNi}} (I_{Dsat0_{MNi}} - I_{Dsat0_{MPi}})}}{I_{Dsat0_{MNi}}}, & \text{for region 3} \\ V_2, & \text{for } V_1 \ge V_{in} \ge V_1 - |V_{TH_{MPi}}|, \end{cases} \tag{5.16}$$

where $\lambda = \frac{1}{V_{ADIBL}}$. The complex expression of the voltage transfer characteristics is not necessary for the practical results. The transfer part of the characteristics is well linearized between values V_{IL} and V_{IH}, as it is shown in Fig. 5.4a,

$$V_{inv}(V_{in}) \approx \begin{cases} V_1, & V_2 \le V_{in} \le V_{IL} \\ \frac{V_1 - V_2}{V_{IL} - V_{IH}}(V_{IN} - V_{IL}) + V_1, & V_{IH} > V_{in} > V_{IL} \\ V_2, & V_1 \ge V_{in} \ge V_{IH}. \end{cases} \tag{5.17}$$

The specific values V_{IL} and V_{IH} will be also determined. Under the above conditions, analytical

expression of the cross current is divided into the three cases:

$$I_{cross} = \begin{cases} I_{DsatN}|V_{GS} = V_{in} - V_2, & V_2 + V_{THN} \leq V_{in} \leq V_{SP} \\ I_{DsatP}|V_{SG} = V_1 - V_{in}, & V_{SP} \leq V_{in} \leq V_1 - |V_{THP}| \\ 0, & \text{otherwise} \end{cases} \tag{5.18}$$

Cross current is maximal at the switching point $V_{in} = V_{SP}$ [23]. Both transistors M_1 and M_2 are in saturation region for this case and the drain current of each MOSFET must be equal:

$$I_{DsatN}|_{V_{GS}=V_{SP}-V_2} = I_{DsatP}|_{V_{SG}=V_1-V_{SP}}, \tag{5.19}$$

thinking zero output current ($I_L = 0$). Equation (5.19) contains the voltage V_{SP} in more than third order, thus simplifying preconditions will be introduced. First, Early voltage limits to infinity, wherefrom is compared $I_{Dsat0N} \approx I_{Dsat0P}$. Second, the absolutely value of the drain currents of the PMOS and NMOS transistors for derivation V_{SP} are not important, only *transconductance* is important. The slope of the cross current characteristics on the each interval is mainly given by a linear part of the voltage $V_{GS} - V_{TH}(V_{SB})$ (MOS transconductance in strong inversion is linear function of the gate-source voltage), while other powers that voltage are not taken into account. Hence, bulk charge equation [27] is adjusted to

$$A_{bulk0}(V_{SB}) = A_{bulk}|_{(V_{GS}-V_{TH})_{eff}=0}$$

and with effective mobility is substituted into the equation (5.5) at zero bias voltages. Finally, the formula of switching point for BSIM model [23] can be expressed in the modified form:

$$\boxed{V_{SP} = \frac{V_1 - |V_{THP}(V_{BS})| + \sqrt{R\frac{\beta_{c_N}}{\beta_{c_P}}}[V_2 + V_{THN}(V_{SB})]}{1 + \sqrt{R\frac{\beta_{c_N}}{\beta_{c_P}}}},} \tag{5.20}$$

where

$$\beta_{c_a} = \frac{c_{oxeN}\mu_{effN}|_{V_{GS}=V_{SB}=0}}{A_{bulk0N}|_{V_{SB}=0}},\ \beta_{c_b} = \frac{c_{oxeP}\mu_{effP}|_{V_{SG}=V_{BS}=0}}{A_{bulk0P}|_{V_{BS}=0}} \text{ and } R = \frac{W_n}{L_n}\frac{L_p}{W_p}.$$

The switching point is an important parameter for calculation of the DC power because of the discontinuous of the cross current characteristics at it.

Static power during the inverter output voltage crossing between a logic 1 and a logic 0 is defined as

$$P_{DC} = \int_{V_2}^{V_1} I_{cross}\,(V_{in})\ \mathrm{d}V_{in} = \int_{V_2+V_{THN}}^{V_{SP}} I_{DsatN}\,(V_{in})\ \mathrm{d}V_{in} + \int_{V_{SP}}^{V_1-|V_{THP}|} I_{DsatP}\,(V_{in})\ \mathrm{d}V_{in}. \tag{5.21}$$

Solution of equation (5.21) exists, but it is confusing and unnecessary for estimation of the power dissipation. Results of the numeric integration of equation (5.21) shows, that function is

primarly determinend by the function *arcatn*[2], that *can be approximated by its argument (linear function) at zero* $\left(\lim_{x\to 0}\frac{\arctan(x)}{x}=0\right)$. Simpler approach is based on an approximation of the characteristics (Fig. 5.3) in intervals $V_{in}\in\langle V_2+V_{THN},V_{SP}\rangle$ and $V_{in}\in\langle V_{SP},V_1-|V_{THP}|\rangle$ by *linear interpolation* from two values:

- At point coressponding to the known voltage V_{SP} that is substituted into equation (5.7):

$$I_{max}|_{V_{in}=V_{SP}} = I_{DsatN}|_{V_{GS}=V_{SP}-V_2} \simeq I_{DsatP}|_{V_{SG}=V_1-V_{SP}}$$

- At the point $|V_{GS}|$, that must be greater than threshold voltage $|V_{TH}|$ (strong inversion region). Transistor is operating on the edge of the saturation region (M_1 for $V_{in}\in\langle V_{SP},V_1-|V_{THP}|\rangle$ and M_2 for $V_{in}\in\langle V_2+V_{THN},V_{SP}\rangle$), where the drain current is *approximately linear* function of the gate-source voltage. It means that quadratic part of V_{GS} voltage from expression $(V_{GS}-V_{TH})^2$ must be less than its linear part. Assuming the equality of these parts, then two solutions exists. The first one is $V_{GS}=0$, that is ignored and the second is $V_{GS}=2|V_{TH}|$[3]:

$$I_1=\begin{cases} I_{1N}=I_{Dsat0N}|_{V_{GS}=V_{1N}=2V_{THN}}, & \text{for NMOS}\\ I_{1P}=I_{Dsat0P}|_{V_{SG}=V_{1P}=2|V_{THP}|}, & \text{for PMOS}\end{cases}$$

thence, new formula for cross current characteristics can be expressed as

$$\tilde{I}_{cross}\approx\begin{cases} I_{1N}\frac{V_{SP}-V_{in}}{V_{sp}-V_2-2V_{THN}}+I_{max}\frac{V_2+2V_{THN}-V_{in}}{V_2+2V_{THN}-V_{SP}}, & V_2+V_{THN}\le V_{in}\le V_{SP}\\ I_{1P}\frac{V_{SP}-V_{in}}{V_{sp}-V_1+2|V_{THP}|}+I_{max}\frac{V_1-2|V_{THP}|-V_{in}}{V_1-2|V_{THP}|-V_{SP}}, & V_{SP}<V_{in}\le V_1-|V_{THP}|\\ 0, & \text{otherwise.}\end{cases} \tag{5.22}$$

Using the condition $\tilde{I}_{cross}=0$ for both of the intervals, where $I_{cross}\neq 0$, then the limit values of the input voltage for the valid output logic levels are given by

$$V_{IL}\approx\frac{I_{max}(V_2+V_{TH_{MNi}})-I_{1N}V_{SP}}{I_{max}-I_{1N}}|_{V_{inv}=V_1}, \tag{5.23}$$

$$V_{IH}\approx\frac{I_{max}(V_1-2\,|V_{TH_{MPi}})-I_{1P}V_{SP}}{I_{max}-I_{1P}}|_{V_{inv}=V_2}. \tag{5.24}$$

Equation (5.22) allows to calculate the static power as the triangle area:

$$\tilde{P}_{DC}\approx\frac{1}{2}I_{max}\left(\frac{I_{max}(V_1-2|V_{THP}|)-I_{1P}V_{SP}}{I_{max}-I_{1P}}-\frac{I_{max}(V_2+2V_{THN})-I_{1N}V_{SP}}{I_{max}-I_{1N}}\right). \tag{5.25}$$

Average current during the transition between both of logic levels is coinciding DC power divided by power supply voltage:

$$I_{av}=\frac{P_{DC}}{V_1-V_2}. \tag{5.26}$$

[2]Analytical expression is given by the sum of the functions *arcatn()* and *ln()*.

[3]This value is also included in the coefficient at the *arctan* in solution of Eq. (5.21).

Dynamic behavior is well known for all operating regions [11, 12, 15–17, 19–21, 23, 24]. As it was explained, the propagation delay is not critical parameter from the view of the pump static and dynamic properties in wide range of their values. However,it is useful to estimate propagation delays because of the optimal inverter draft. Providing the inverter capacitive load, labeled C_L, the dynamic properties follow from the state equations,

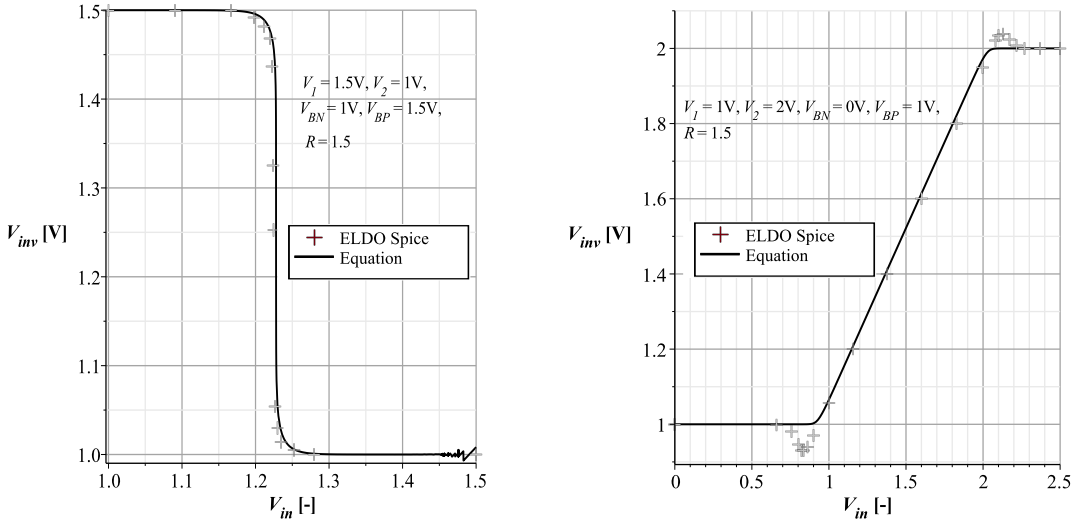
$$-\frac{i_{d_{Mn}}}{C_L^{'}} = \dot{v_{inv}}, \quad \text{for } v_{inv}(0) = V_1, \tag{5.27}$$

$$\frac{i_{d_{Mp}}}{C_L^{'}} = \dot{v_{inv}}, \quad \text{for } v_{inv}(0) = V_2, \tag{5.28}$$

where $i_{d_{Mn(p)}}$ is the N(P)MOSFET drain current and $C_L^{'}$ is total load capacitance consisting of the load capacitance and MOSFET capacitances. This part will be explained bellow. From Eq. 5.27 is posssible to calculate fall time and from Eq. 5.28 rise time.

5.2.2 Subtreshold region and other cases

Apart from the subtreshold region of the inverter, the uncommon configurations exists in the charge pump, for example, during the rise time when the pump output voltage starts from 0 to the final value in steady state, for low power supply voltage, $V_{DD} \to V_{TH}$, overlap of the clock signals, etc.. One of them admits the reverse inverter configuration, when $V_1 < V_2$. Transfer



(a) (b)

Figure 5.5: Voltage transfer characteristics of the CMOS inverter operating in subtreshold region: $V_1 > V_2$ (a) and $V_1 < V_2$ (b)

characteristics for both the subtrehold and reverse configuration are shown in Fig. 5.5. Equation for the drain current in subtrehold region is also valid for negative bias gate-source or drain-source voltage $V_{GS} \ll 0$, where the transistor is considered OFF. Description of the VTC comes

from equation for subtreshold region [27],

$$I_{D_s} = \underbrace{I_0 \cdot e^{\left(\frac{V_{GS_{eff}} - V_{TH} - V_{off}}{nV_t}\right)}}_{I_{S0}} \cdot \left[1 - e^{-\frac{V_{DS}}{V_t}},\right] \tag{5.29}$$

where n is subtreshold swing parameter, V_t is thermal voltage, $V_{GS_{eff}}$ is effective gate-source voltage, V_{off} is cutt-off voltage, which determines channel current at $V_{GS} = 0$ and

$$I_0 = \mu \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si}\mathrm{NDEP}}{2\phi_s}} V_t^2, \tag{5.30}$$

where q is electron charge, ε_{Si} is permittivity of silicon and NDEP is depletion doping concetration. Respecting Eq. 5.29 and $V_{gs_{eff}} \approx V_{GS}$ [4], the VTC is given by

$$V_{inv}\left(V_{in}\right) = V_t \cdot \ln\left(-\frac{1}{2}\frac{I_{S0_N} - I_{S0_P} - \sqrt{4I_{S0_P}I_{S0_N}e^{\frac{V_2 - V_1}{V_t}} + \left(I_{S0_N} - I_{S0_P}\right)^2}}{I_{S0_P}e^{-\frac{V_1}{V_t}}}\right)|_{n=1}, \tag{5.31}$$

where $I_{0_{N(P)}}$ is the drain current of the M_{N_i} (M_{P_i}) MOSFET for $V_{GS_N} = V_{in} - V_2$ and $V_{SG_P} = V_1 - V_{in}$.

This is only case from the description of the pump block, in which Eq. 5.29 is applied to express the voltage but not the current. In the first case of VTC (Fig. 5.29a) inverter has defined the output logic levels and in the second case (Fig. 5.29a), the characteristics has "continous character", output voltage is strongly dependent on the drain-source resistance. All the other cases are given by combining equations for strong (Eq. 5.8, 5.9) and subtreshold region (Eq. 5.29). In simulator this function is determined based on the single equation (only numerical solution).

5.3 Model of the pump stage

Full-description of the pump model allow to analyze the pump losses (reverse switch current, inverter cross current) and their relations between the component sizing (main capacitors value, transistors width and lengths) and other pump parameters, as the clock frequency. The aim is the to include dominant phenomena of the real circuit through the symbolic expression, so that the optimal circuit design will be done.

5.3.1 Static part of the model

One stage of the cross-coupled charge pump is shown in Fig. 5.6. The drain current of the each MOSFETs is controlled by the input voltage V_{in}. Adjustable DC source voltage is used for analysis instead of the main capacitor in real circuits. All other DC voltages in diagram are referenced to the ground. *The basic condition (3.6) must be valid.* The output voltage of the

[4] Expression is not very accurate because the effective gate-source voltage is not considered. Drain current calculation error strongly depends on the specific vales of the bias voltages–error increses, when V_{GS} is approaching the zero point.

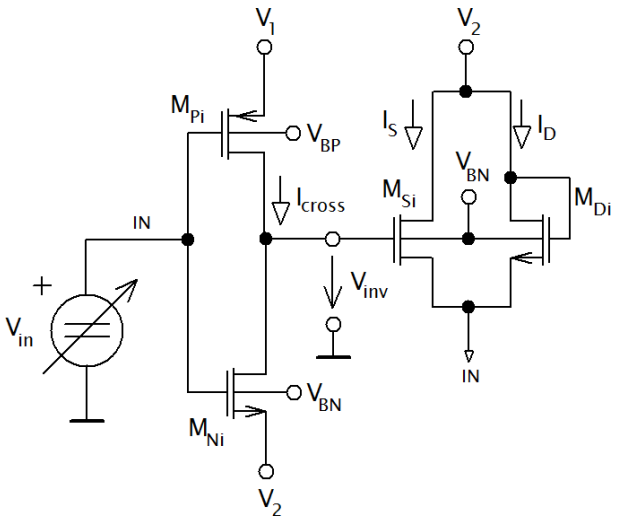


Figure 5.6: Diagram of the cross-coupled charge pump stage

inverter $V_{inv} = \mathrm{f}(V_{in})$ is setting the drain current of the switch transistor M_{Si}, labeled I_S. The linearized VTC (Eq. 5.16) is considered. Voltage on the capacitor is changing continuously from 0 to the supply voltage V_2 in the passive time interval and voltage at the terminal "IN" may be theoretically doubled in the active interval of the clock signal, i.e. $V_{IN} = 2V_2$.

Thus, the drain current I_S through the switch transistor M_{Si} (and its orientation) will be analyzed in the interval of the input voltage $V_{in} \in \langle 0,V_1 \rangle$ (the D,S pins of the switch transistor are not distinguished in the scheme). Orientation of the forward–"charging" current (that is required) matches the orientation in the scheme. The control voltages configuration for the setting both the forward (I_{S_F}) and reverse drain current (I_{S_R}) of the M_{Si} transistor are shown in Tab 6.9. Respecting the condition (5.12), transistor M_{Si} is *always* ON in the interval $V_{in} \in$

Table 5.1: M_{Si} transistor control voltages configuration for the setting of I_S

Parameter	Value	
I_S	> 0	≤ 0
V_{in}	$V_{in} \in \langle 0,V_2)$	$V_{in} \in \langle V_2,V_1 \rangle$
$V_{DS_{MSi}}$	$V_2 - V_{in}$	$V_{in} - V_2$
$V_{GS_{MSi}}$	$V_{inv} - V_{in} = V_1 - V_{in}$	$V_{inv}(V_{in}) - V_2$
$V_{SB_{MSi}}$	$V_{in} - V_{BN}$	$V_2 - V_{BN}$

$\langle 0,V_2)$. The bulk both of the M_{Ni} and M_{si} transistors is connected to the same bias voltage V_{BN} (usually to the ground) and $V_{SB_{MSi}} \leq V_{SB_{MNi}}$, then $V_{TH_{MSi}}(V_{SB}) \leq V_{TH_{MNi}}(V_{SB})$ in the same technology process. Moreover, this transistor is operating in the triode region, as it is shown bellow. In this case, the condition $V_{DS} < V_{DS_{sat}}$ is valid, where the saturation voltage is calculated from Eq. (5.6). Substituting the specific values from Table (6.9) into the $V_{DS_{sat}}$ equation, the inequality is obtained:

$$V_2 < \frac{V_1 - V_{in} - V_{TH_{MSi}}(V_{in},V_{BN})}{A_{bulk_{Msi}}(V_1,V_{in},V_{BN})} + V_{in} \tag{5.32}$$

Expression on the right hand sight of Eq. (5.32) must also satisfy the condition (5.12). Consid-

ering the worst case of the threshold voltage, $V_{TH_{MSi}} = V_{TH_{MNi}}$, then

$$|V_{TH_{MPi}}| + V_{in} > \underbrace{\left(1 - \frac{1}{A_{bulk_{Msi}}}\right)}_{\leq 0}(V_1 - V_{TH_{Msi}} - V_{in}). \tag{5.33}$$

Saturation voltage $V_{DS_{sat}}$ can be approximated by the function $V_{GS} - V_{TH}$ near the point

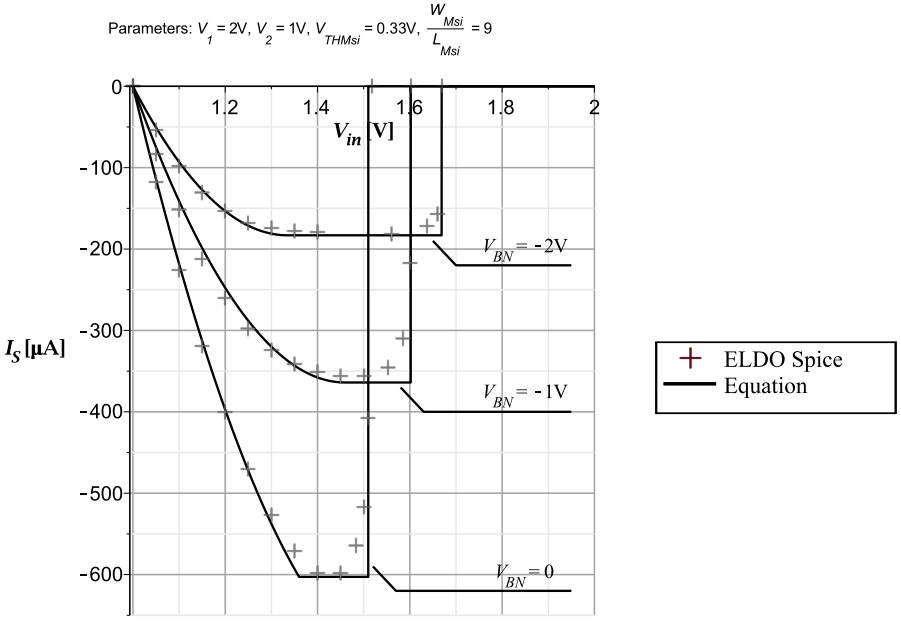


Figure 5.7: Reverse current of the switch transistor vs. input voltage

$V_{GS} = V_{TH}$ (long channel MOSFET is provided). However, real saturation voltage is greater than function expressed in Eq. (5.6) for higher voltage V_{GS}, $V_{DS_{sat}} > V_{GS} - V_{TH}$, i.e. $A_{bulk} < 1$, for $V_{GS} \gg V_{TH}$. Subsequently, the inequality (5.33) is always true. The drain current direction is changed and it is controlled by the constant gate-source voltage $V_1 - V_2$, while $V_2 < V_{in} \leq V_{IL}$. The gate-source voltage decreasing quickly in the interval $\langle V_{IL}, V_{IH}\rangle$, while a change of the drain-source voltage is negligible. Hence, the drain current achieves the maximal value at point V_{IL} and transistor is abruptly switched off after exceeding the switching point. Neglecting the transition part of the inverter transfer characteristic, drain current can be considered the constant in the interval $V_{in} \in \langle V_{IL}, V_{SP}\rangle$. Total current I_S is given by the following formula:

$$I_S(V_{in}) \approx \begin{cases} I_{DS0_F}, & V_{in} \in \langle 0, V_2) \\ I_{S_R}, & V_{in} \in (V_2, V_{SP}\rangle \\ 0, & V_{in} \in (V_{SP}, V_1\rangle \end{cases} \tag{5.34}$$

Current I_{S_R} is calculated on the basis of the two following cases:

- if $V_{IL} > V_2 + V_{DSsat_{MSi}}$, then

$$I_{S_R}(V_{in}) \approx \begin{cases} I_{DS0_R}, & V_{in} \in (V_2, V_2 + V_{DS_{sat}}\rangle \\ I_{D_{sat0R}}, & V_{in} \in (V_2 + V_{DS_{sat}}, V_{SP}\rangle \end{cases}, \tag{5.35}$$

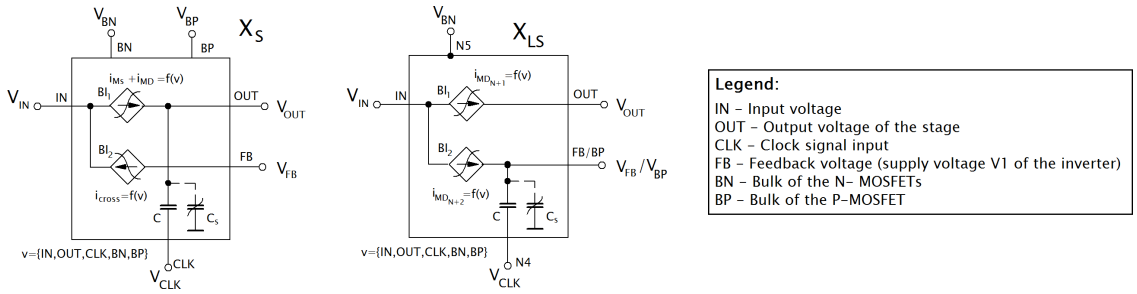
- if $V_{IL} \leq V_2 + V_{DSsat_{MSi}}$, then

$$I_{S_R}(V_{in}) \approx \begin{cases} I_{DS0_R}, & V_{in} \in (V_2, V_{IL}\rangle \\ I_{DS0_R}|_{V_{GS}=V_1-V_2, V_{DS}=V_{IL}-V_2}, & V_{in} \in (V_{IL}, V_{SP}\rangle\,, \end{cases} \tag{5.36}$$

where I_{DS0} is the drain current in triode region and $I_{D_{sat0}}$ is the drain current in saturation region at $V_{DS} = V_{DS_{sat}}$. Reverse current waveform for the both cases is shown in Fig. 5.7. The source-bulk bias voltages is the parameter. The drain current of the M_{Di} transistor is zero in the reverse configuration due to shorted its electrods gate and source,

$$I_D(V_{in}) = \begin{cases} I_{Dsat0}, & V_{in} \in \langle 0, V_2 - V_{TH_{MDi}}) \\ 0, & \text{otherwise.} \end{cases} \tag{5.37}$$

Pump model was created for the *test purposes* by numerical simulator (Spice). The static part of the i-pump stage is shown in Fig. 5.8a. Internal structure includes two nonlinear dependent current sources controlled by the voltage at the external terminals. Current source BI_1 represents both the currents through the diode and switch transistor(reverse+forward current) and BI_2 models the inverter cross current. Subcircuit of the last stage (Fig. 5.8 b) is different from the other stages–two controlled sources only represent the drain currents thhrough the diode transistors $M_{D_{N+1}}$ and $M_{D_{N+2}}$.



(a) (b)

Figure 5.8: Subcircuit of the i-pump stage (a) and the last stage (b)

5.3.2 Dynamic part of the model

Substrate capacitances comparable to main capacitances are well-known design complication because they significantly reduce the voltage potential at each of the stages. The stage model will be completed by the dynamic part including Ward's capacitance piece-wise model and relationships for the pump stage internal capacitances will be derived. The aim is to achieve the coincidence of the model and real circuit characteristics on the largest set of input pump parameters, as the low main capacitance ($C \to C_s$) or a wide range of the clock signal frequency. Then, the model is not devoid of its universality. The following procedure assumes that substrate capacitances are the key part of the model, other effects, like a charge injection, will not be taken into account. Individual capacitances of the subcircuit are transformed between the

external terminals and ground. The situation is in Fig. 5.9. Each of the blocks X_i, X_{LS} respective, in N-stage charge pump has input and output nonlinear capacitance. Other currents i_{in}, $i_{out}, \ldots$ represent static part of the model. Definition according to Eq. 5.10 makes it quite easy to express particular capacitances that are shown in Fig. 5.9 without calculation serial-parallel combinations of the MOSFETs capacitances. *Each of the input/output capacitance is approximately given by the sum of those MOSFETs capacitances, which are connected between the considered external subcircuit terminal and GROUND (substrate in case of the NMOS).* In according to Fig. 5.9, input pump stage capacitance C_{in} is determined by the drain capacitance of M_d and M_s transistors, gate capacitance of M_D transistor and source capacitance of the inverter transistor M_N,

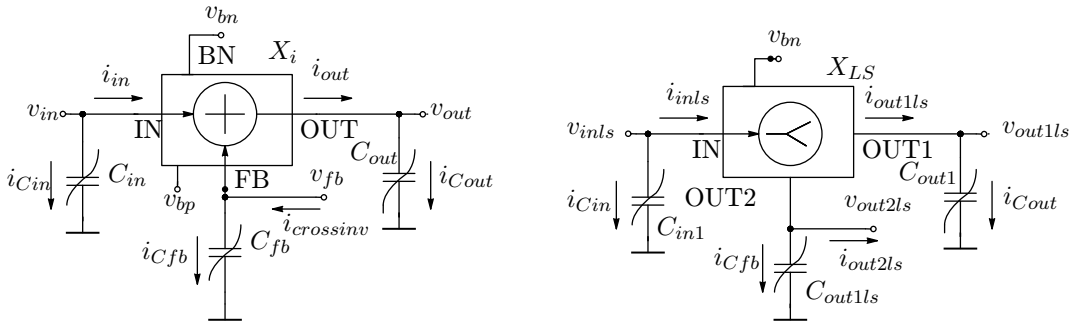
$$C_{in} \approx C_{DD_{MD}} + C_{GG_{MD}} + C_{DD_{Ms}} + C_{SS_{Mn}}. \tag{5.38}$$

Similarly, for other cases:

$$\begin{aligned} C_{out} &\approx C_{SS_{MD}} + C_{SS_{Ms}} + C_{SS_{Mp}}, \\ C_{fb} &\approx C_{GG_{Mn}} + C_{GG_{Mp}}, \\ C_{inls} &\approx C_{DD_{MDn+1}} + C_{GG_{MDn+1}} + C_{DD_{MDn+2}} + C_{GG_{MDn+2}}, \\ C_{out1ls} &\approx C_{SS_{MDn+1}}, \\ C_{out1ls} &\approx C_{SS_{MDn+2}}. \end{aligned} \tag{5.39}$$

That observation is not preferred because it is necessary to express three equations for the three charges Q_D Q_S and Q_G. Simplification process is based on using of the following equation for charge balance (Eq. 5.11) and minor components, as drain-source capacitance that is very small, can be neglected [23]. As an example, for capacitance $C_{DD_{MD}}$ is valid:

$$C_{DD_{Md}} = -\left(C_{DG_{Md}} + C_{DS_{Md}} + C_{DB_{Md}}\right),$$



(a) (b)

Figure 5.9: Complex model for synthesis procedure: pump stage (a) and the last pump stage (b) block diagram.

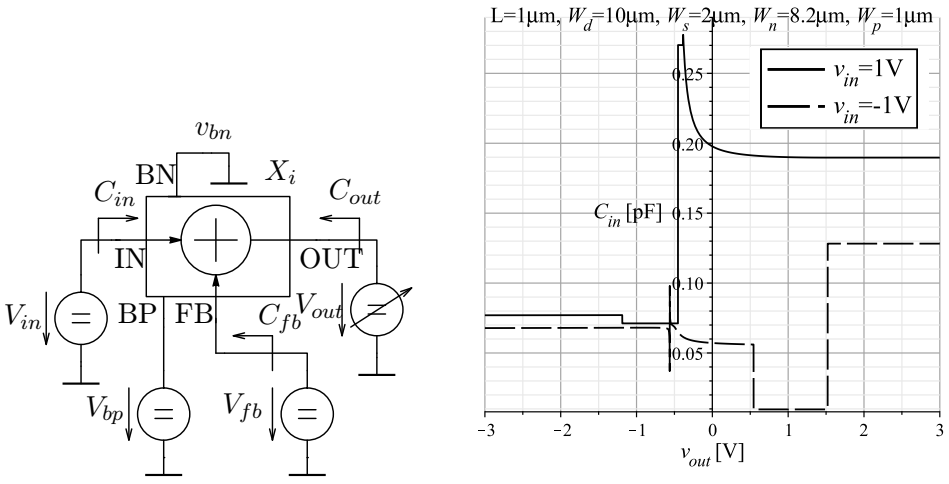
where C_{DG} is zero due to $V_{DG} = 0$ and $C_{DS} \to 0$, after that

$$C_{DD_{Md}} \approx -\frac{\partial Q_{d_{Md}}}{\partial V_g} = -\frac{\partial Q_{g_{Md}}}{\partial V_d}.$$

The other components can be rewritten in a similar way. Finally, spare models input/output capacitances, including maximal two charges Q_g and Q_s expressions, are defined as,

$$\begin{aligned}
C_{in} &\approx -\frac{\partial Q_{b_{Md}}}{\partial V_{d_{M_d}}} + \frac{\partial Q_{g_{Md}}}{\partial V_{g_{Md}}} - \frac{\partial (Q_{b_{Ms}} + Q_{g_{Ms}})}{\partial V_{d_{Ms}}} - -\frac{\partial (Q_{b_{Mn}} + Q_{g_{Mn}})}{\partial V_{s_{Mn}}} \\
C_{out} &\approx -\frac{\partial (Q_{b_{Md}} + Q_{g_{Md}})}{\partial V_{s_{Md}}} - \frac{\partial (Q_{b_{Ms}} + Q_{g_{Ms}})}{\partial V_{s_{Ms}}} - -\frac{\partial (Q_{b_{Mp}} + Q_{g_{Mp}})}{\partial V_{s_{Mp}}} \\
C_{fb} &\approx \frac{\partial Q_{g_{Mn}}}{\partial V_{g_{Mn}}} + \frac{\partial Q_{g_{Mp}}}{\partial V_{g_{Mp}}} \\
C_{inls} &\approx \frac{\partial (Q_{b_{Md}} + Q_{g_{Md}})}{\partial V_{d_{Md}}} + \frac{\partial Q_{g_{Mdn+1}}}{\partial V_{g_{Mdn+1}}} + + \frac{\partial (Q_{b_{Mdn+2}} + Q_{g_{Mdn+2}})}{\partial V_{d_{Mdn+2}}} + \frac{\partial Q_{g_{Mdn+2}}}{\partial V_{g_{Mdn+2}}} \\
C_{out1ls} &\approx \frac{\partial (Q_{b_{Mdn+1}} + Q_{g_{Mdn+1}})}{\partial V_{s_{Mdn+1}}} \\
C_{out2ls} &\approx \frac{\partial (Q_{b_{Mdn+2}} + Q_{g_{Mdn+2}})}{\partial V_{s_{Mdn+2}}}.
\end{aligned} \tag{5.40}$$

The waveform of the voltage-dependent pump stage input/output capacitance was tested in



(a) (b)

Figure 5.10: Analysis of the pump input capacitance: block diagram (a) and waveform (b)

the simulator by using linearized MOSFETs parameters in the operating point, i.e.small signal model (DCOP analysis) [30]. Capacitances were gradually measured depending on the selected control voltage, while other voltage sources have been set to a constant. Example of the input capacitance waveform $C_{in} = \mathrm{f}(v_{out})$ at $v_{in} = \pm 1\,\mathrm{V}$, $v_{fb} = 2\,\mathrm{V}$, $v_{bp} = 3V$ and $v_{bn} = 0$ is shown in Fig. 5.10.

5.4 Testing of the behavioral model in the simulator

The found analytical formulae of the subcircuit (Fig. 5.9) are tested in N-stage model by LT Spice in order to achieve the concurrence between model and real circuit characteristics, i.e. verifying of the dominant effects, which were be described in the previous sections. The main benefit is to find the design algorithm including the relationships for optimal transistors sizing and other pump parameters arising from the input application requirements. The pump parameters were

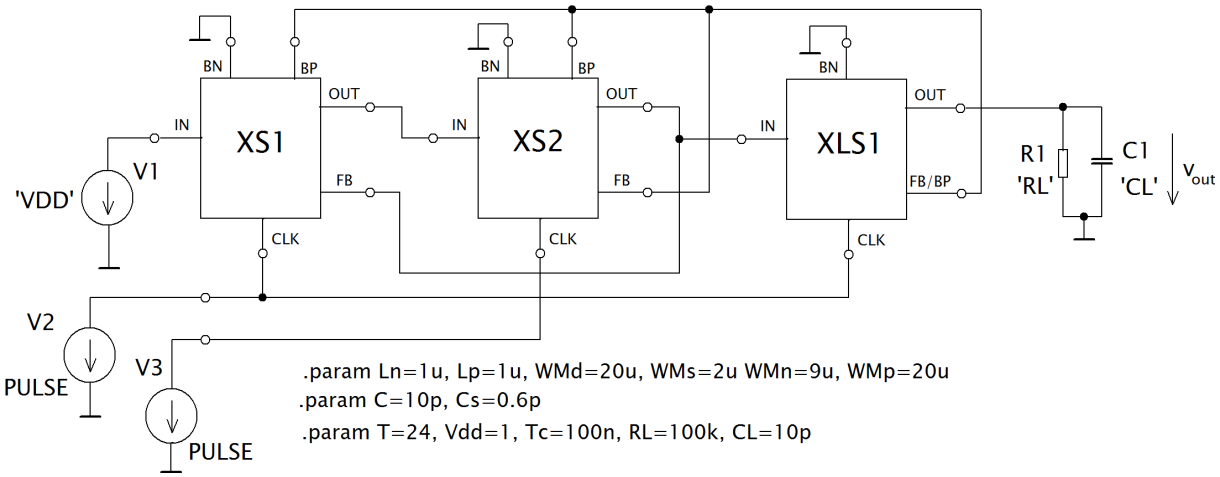


Figure 5.11: Two-stages charge pump model

tested in the two-stages charge pump, see Fig. 5.11. Some real charge pump properties have been analyzed by the professional simulator ELDO Spice including real models of the components (library MGC Design Kit). Simulation parameters are given in Tab.7.1.

Table 5.2: Simulation parameters

Parameter		**Value**
Temperature	ϑ	24° C
Supply voltage	V_{DD}	1V
CLK frequency	f_c	10 MHz
Main capacitance	C	10 pF
Parasitic capacitance	C_s	0.6 pF
Load resistance	R_L	100 k
Load capacitance	C_L	10 pF
Threshold voltage of	V_{TH0_N}	0.35 V
NMOS and PMOS at V=0	$\|V_{TH0_P}\|$	0.33 V
Channel length of N(P)MOS	L	1μm
W/L ratio of the M_{Si}	W_s/L_s	2
M_{Pi}	W_p/L_p	20
M_{Ni}	W_n/L_n	9
M_{Di}	W_d/L_d	20

Simulation results of the static and dynamic characteristics are shown in Fig. 5.12. Simulation results show conformity of the model and real circuits assuming defined conditions. Deviation of the output voltage increases, when the node voltage(s) drop(s) bellow a certain

limit (due to low supply voltage, high load current,...) so that MOSFETs are operating in subtreshold region, see Fig. 5.12b. This state is not suitable in high voltage circuit.

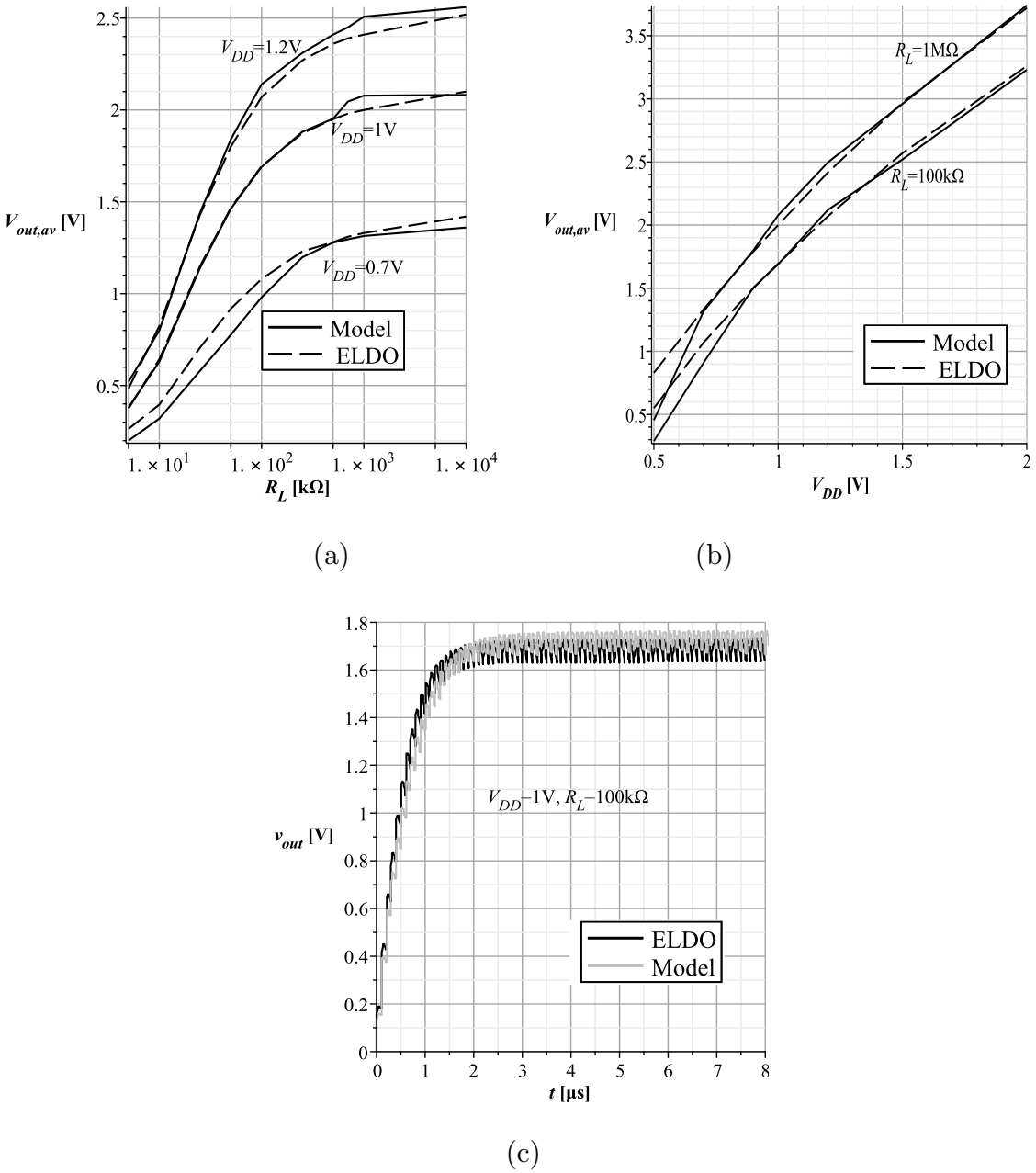


Figure 5.12: Comparison characteristics between the pump model and real circuit: Output voltage vs. load resistance (a) and supply voltage (b), dynamic char. (c)

5.5 Summary

The description of the pump functional blocks based on the simplified BSIM model v. 4.6.4 was discussed in this chapter. Long channel and strong inversion region of MOSFETs is expected, thus results are valid in the specified technology process, as PSP or EKV models. The complex model inlcudes equations, which faithfully represents behavior of the real circuit, as it was verified in section 5.4. Mathematical models allow to design circuit components in order to

achieve maximum voltage gain or other criteria. in summary, the primary phenomena used in the description of the model structure are:

- threshold voltage and body effect,
- bulk charge effect,
- dibl effect
- iverter voltage transfer characteristics for all MOSFETs operating regions,
- cross current characteristic of the inverter operating in strong inversion region,
- forward+reverse switch currents, diodes forward current,
- substrate input/output capacitances of the pump stage model expressed by the Ward's capacitance piece-wise model for *CAPMOD=0* and *XPART=1*,
- temperature effects.

Chapter 6

Design of the pump functional blocks

6.1 CMOS inverter draft

The inverter design for digital applications as the component in the combinational and sequential circuits is known The width of the PMOS must be 2-3 times width of the NMOS [23] (at the same MOSFET lengths) because of the symmetrical transfer characteristics. However, this setting may not suit in analog circuits. Inverter draft for charge pump applications is based on the minimize average cross current during the period of the clock signal.

6.1.1 Static power minimization

The principle of the draft is based on the shifting *inverter switching point* (see Fig. 6.1a), at this the cross current is maximal, to *down or up limit*, where one of the MOSFET is at the cut-off border. Because completely closed transistor can never be achieved, the transistors sizing was found from the sensitivity analysis of the switching point to the parameter $R = \frac{W_n}{L_n}\frac{Lp}{Wp}$ from in Section 5.2. The sensitivity is defined as

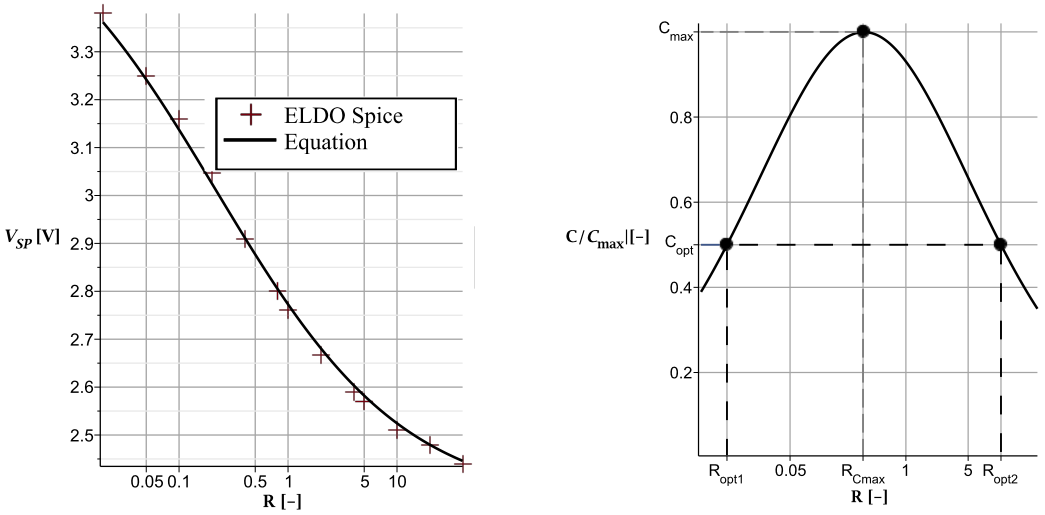
$$S = \frac{\mathrm{d}V_{SP}}{\mathrm{d}R}\frac{R}{V_{SP}} = -\frac{1}{2}\frac{\beta_{c_N} R\left(V_1 - |V_{THP}| - V_2 - V_{THN}\right)}{\left(\sqrt{\frac{\beta_{c_N} R}{\beta_{c_P}}} + 1\right)\sqrt{\frac{\beta_{c_N} R}{\beta_{c_P}}}\,\beta_{c_P}\left[\sqrt{\frac{\beta_{c_N} R}{\beta_{c_P}}}\left(V_2 + V_{THN}\right) + V_1 - |V_{THP}|\right]} \tag{6.1}$$

and decrease of the maximum sensitivity to the desired value is expressed by parameter δ:

$$\delta = \frac{S_{opt}}{S_{max}}. \tag{6.2}$$

The δ parameter will be determined from the simulations results, as it is shown bellow. δ is usually put to 0.5 because the voltage V_{SP} depends on the square root of R. Maximum sensitivity (in absolute value) given by condition $\frac{\mathrm{d}S}{\mathrm{d}R} = 0$ is at point

$$R_{Smax}|_{S=S_{max}} = \frac{V_1 - |V_{THP}|}{\frac{\beta_{c_N}}{\beta_{c_P}}\left(V_2 + V_{THN}\right)}. \tag{6.3}$$



(a) (b)

Figure 6.1: Switching point analysis – dependence on the ratio R and normalized sensitivity curve

Normalized sensitivity curve to the maximum absolute value is shown in Fig. 6.1b. Finally, the optimal parameter S is derived from equations (6.1), (6.2) and (6.3),

$$S_{opt} = \frac{1}{16}\left[\frac{2S_{max}\delta\left(V_{1a}+V_{2a}\right)+V_{12}\pm\sqrt{V_{12}}\sqrt{4S_{max}\delta\left(V_{1a}+V_{2a}+S_{max}V_{12}\delta\right)+V_{12}}}{\sqrt{\frac{\beta_{c_N}}{\beta_{c_P}}}S_{max}\delta V_{2a}}\right]^2, \tag{6.4}$$

where $V_{1a} = V_1 - |V_{THP}|$, $V_{2a} = V_2 + V_{THN}$ and $V_{12} = V_{1a} - V_{2a}$. Two solutions of the equation (6.4) exists. The first one: R_{opt1} for $\frac{W_n}{L_n} \gg \frac{W_p}{L_p}$ and the second one: R_{opt2} for $\frac{W_p}{L_p} \gg \frac{W_n}{L_n}$ (Fig. 6.1).

6.1.2 Switching characteristics

Equation 6.4 provides the ratio between MOSFET size that mus be kept to achieve the primary criterion. Absolutute dimensions–transistors width will be derived based on the propagation delays. For calculation of the time delay t_{HL} and t_{LH} from Eq. 6.7 is necessary to estimate the inverter load capacity value, labeled $C_L^{'}$. Due to the fact, the output is connected to gate of the switch transistor[1], special demands on the inverter are not put. This matter will be explained to supplement. Using the pump MOSFET capacitance model, the inverter load capacitance in each of the pump stage is approximately given by

$$C_L^{'} \approx C_{DD_{Mp}} + C_{DD_{Mn}} + C_{GG_{Ms}}, \tag{6.5}$$

where $C_{DD_{Mp}}$ is drain capacitance of the M_p transistor, $C_{DD_{Mn}}$ is drain capacitance of the M_n transistor and $C_{GG_{Ms}}$ is gate capacitance of the switch transistor M_s in (F). Expressing

[1]Switch MOSFET sizes are very small, as it will be proved.

the voltage-dependent capacitances by the time time derivation of the terminal charges Q_i and transformation according to (5.10) and (5.11), Eq. 6.5 now becomes to

$$C_L^{'} \approx \frac{\partial(Q_{D_{Mp}} + Q_{B_{Mp}})}{\partial V_{D_{MP}}} + + \frac{\partial(Q_{D_{Mn}} + Q_{B_{Mn}})}{\partial V_{D_{Mn}}} + \frac{\partial Q_{G_{Ms}}}{\partial V_{G_{Ms}}}, \tag{6.6}$$

As the consequence of Eq. 6.4, $t_{HL} > t_{LH}$, thus the fall time will guide on the PMOS sizing, i.e stricter criterion. Inverter is usually designed so that the propagation delay was negligible small to the pulse width. To satisfy of this, it is nenecessary choose the worst case of the inverter power supply voltages over all stages and maximal load capacitance. Calculation of the time delay besed on the general definition (Eq. 5.27, 5.28) is complicated, thus it is possible to use simplified equations [23],

$$t_{HL} = 0.7 R_n C_L^{'}, \tag{6.7}$$

$$t_{LH} = 0.7 R_p C_L^{'}, \tag{6.8}$$

where $R_{n(p)}$ is the equivalent N(P)MOSFET resistance [23].

6.1.3 Experimental part

Simulation circuit parameters are shown in Tab. 6.1. The dependence of the average cross current on the width of the PMOS (W_p) or NMOS (W_n) transistor was analyzed at the fixed channel lengths L_n, L_p that were determined from condition 5.1.

Table 6.1: Simulation circuit parameters

Parameter		**Value**
Temperature	ϑ	24°C
Power	$V_1 = V_{Bp}$	4 V
suppply voltage	$V_2 = V_{Bn}$	2 V
Threshold voltage	V_{THN}	0.356 V
of N(P)MOS at 0V	$\lvert V_{THP} \rvert$	0.33 V
Transcoductance	β_{c_N}	$3.43 \cdot 10^{-4}$ AV^{-2}
coefficients	β_{c_P}	$7.45 \cdot 10^{-5}$ AV^{-2}

Analysis results in Tab. 6.2 show, the effective reduction of I_{av} is achieved, when $R \gg R_{S_{max}}$ (solution R_{opt1} of Eq. 6.4), consequently $W_n \gg W_p$ and V_{SP} approaches lower limit, $V_{SP} \rightarrow V_2 + V_{THN}$. It is physically caused by greater mobility of electrons in the NMOS structure compared to mobility of holes in the NMOS dimensions. Otherwise, when $R \ll R_{smax}$, very large disproportion between sizes of both transistors adversaly affects other properties of the inverter (transistors area, dynamic properties,...), as is shown bellow.

Choice the solution R_{opt1} is also favorable from the view of the reverse switch current. Static characteristic of the pump stage in Fig. 6.2 shows that loss performance proportional to the total area below the v_{out} axis falls off with increasing of the parameter R. Morover, correlation between the inverter and switch transistors sizing is proved by the mathematical model.

Table 6.2: Simulation results

$L_p = L_n = 1\mu m$				
			$W_n = 40\mu$m	$W_p = 40\mu$m
$\delta\,(-)$	$\mathbf{R_{opt1,2}}\,(-)$	$\mathbf{V_{SP}}$ (V)	$\mathbf{I_{av}}$ (mA)	
0.51	**0.01**	3.47	1.92	**0.018**
0.63	**0.02**	3.4	1.69	**0.031**
0.92	0.1	3.16	1.07	0.106
0.985	0.2	3.047	0.798	0.159
1	0.34	2.76	0.309	0.309
0.83	2	2.67	0.186	0.372
0.7	4	2.59	0.107	0.430
0.66	**5**	2.57	**0.089**	0.447
0.5	**11.7**	2.5	**0.047**	0.507
0.41	**20**	2.46	**0.026**	0.541
0.31	40	2.42	0.013	0.582

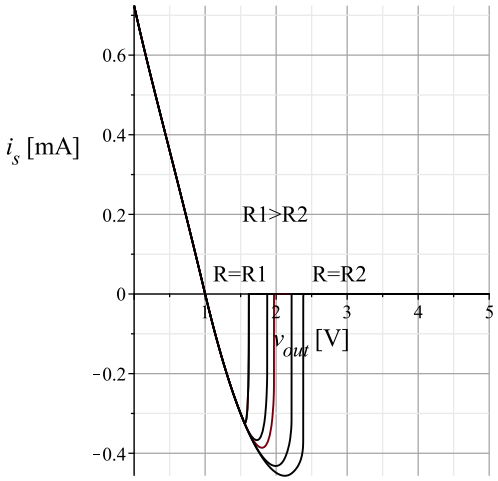


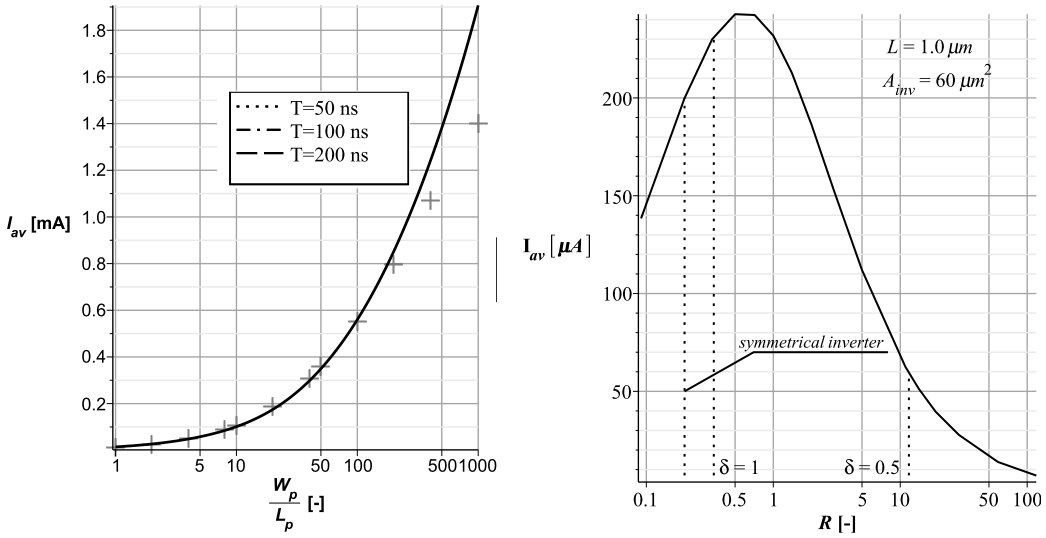
Figure 6.2: Static characteristic of the pump stage with parameter R

Of course, the mean value of the cross current is not only a function of R, but depends on the specific value of W_n/L_n, respectively W_p/L_p, as is shown in Fig. 6.3a. R factor is plotted on a logarithmic scale due to its wide range. *Experience says, that optimal value of parameter* δ *is* $0.4 \div 0.6$ *for practical design.* Values of the ratio R and average cross current I_{av} for this range of the δ parameter are bold in Tab. 6.2.

Analysis of I_{av} vs. the ratio R, while keeping the constant inverter area is shown in Fig. 6.3b However, optimal setting of the R is not responsible to the design of inverter operating in digital circuits, where the switching point should be closed to the ideal value of the half of the supply voltage. Therefore

$$R|_{V_{SP}=V_{DD}/2} = \frac{\beta_{c_P}}{\beta_{c_N}} \left[\frac{V_1 - V_2 - 2\,|V_{THP}(V_{BS})|}{V_1 - V_2 - 2V_{THN}(V_{SB})} \right]^2 \tag{6.9}$$

and corresponding sensitivity is about 0.98 and simulated I_{av} value is higher about ten times



(a) (b)

Figure 6.3: Average value of the cross current vs. the W_p/L_p ratio for $W_n = 40\,\mu$m(a) and I_{av} vs. R ratio for $A_{inv} =$ konst.(b)

compared to the optimization process. Width of the PMOS transistor is sized to $2 \div 3$ the width of the PMOS [23] transistor (lengths are the same), provided that $V_{THN} \approx |V_{THP}|$. This condition can not be satisfied in voltage convertors due to different supply voltage V_1, V_2 in each of convertors' stages and different threshold voltage of each of the transistors.

6.2 Switch transistor sizing

Switch a diode transistor sizing is derived from the the time response characteristics based on he static model of the pump stage presented in Section 5.3. The main benefit is the symbolic relationships for optimal transistors sizing, so that the pump voltage gain is maximal.

6.2.1 Time response characteristics

Step response is typical characteristic situation in the switched-capacitor circuits. Step response characteristics of the circuits are shown in Fig. 5.6. The time-varying voltage on the main capacitor to the clock signal will be found for both the forward and reverse configuration to determining pumping losses. The extreme values of the bias voltage have been chosen for the following optimization process. The time domain method must be used for the calculation due to the *nonlinerity behavior* of this system. It is also necessary to define the next conditions for the analysis process:

- parasitic capacitances are negligibly small compared with the main pumping capacitors, $C_s \ll C_i$.
- rise time and fall time delay of the clock signal and propagation delays of the inverter are very short compared with the charge/discharge time of the main capacitors.

- leakage currents of all the components are neglected.
- settling time of the switches is zero.

The main capacitor is charged, when the gate of the switch transistor is connected to high output voltage level of the inverter V_{inv} = "H" = V_1, drain is connected to the input stage voltage V_2 and the main capacitor is connected to ground. This situation is shown in Fig. 6.4. When the

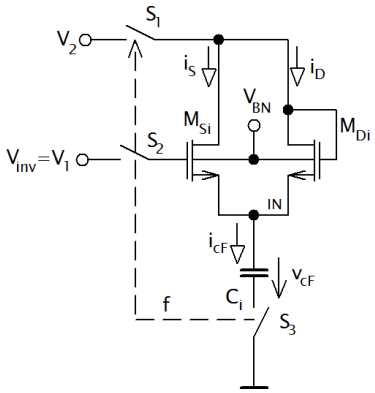


Figure 6.4: Configuration for the charging of the main capacitor

switches S_1, S_2 and S_3 will be on at $t = 0$, the current flowing through the capacitors i_{c_F} is supplied both of the transistor until the capacitor voltage does not exceed the value V_{0_F} at time t_{0_F}, see Fig. (6.4). Total current i_{c_F} is given by

$$i_{c_F}(t) = \begin{cases} i_s(t) + i_d(t), & \text{for } 0 < t \leq t_{0_F} \\ i_s(t), & \text{for } t > t_{0_F} \\ 0, & \text{otherwise.} \end{cases} \tag{6.10}$$

The voltage on the capacitor is equal to V_2 in steady state and the specific value of the voltage V_{0_F} can be derived from

$$V_{0_F} = V_2 - V_{TH_{MDi}}(v_{SB}), \tag{6.11}$$

Combining Eq. (6.11) and (5.2), the instantaneous value of the voltage in which the transistor M_{Di} will be OFF, is calculated from

$$V_{0_F} = \frac{V_2 + K_1 - V_{TH0_{MDi}}}{K_{2ox} + 1} + \frac{1}{2}\frac{K_{1ox}\left(K_{1ox} - \sqrt{\gamma}\right)}{\left(K_{2ox} + 1\right)^2}, \tag{6.12}$$

where

$$\gamma = 4\phi_s \left(K_{2ox} + 1\right)^2 + 4\left(K_{2ox} + 1\right)\left(K_1\sqrt{\phi_s} + V_2 - V_{TH0_{MDi}} + K_{1ox}^2\right).$$

Substituting the voltage v_{cF} in the static model for V_{in} and using equations for the drain current ([23]-[24]), time response characteristics is generally found by the solving of the differential equation

$$\int \frac{C}{i_{c_F}} \mathrm{d}v_c = t + \mathrm{IC} \tag{6.13}$$

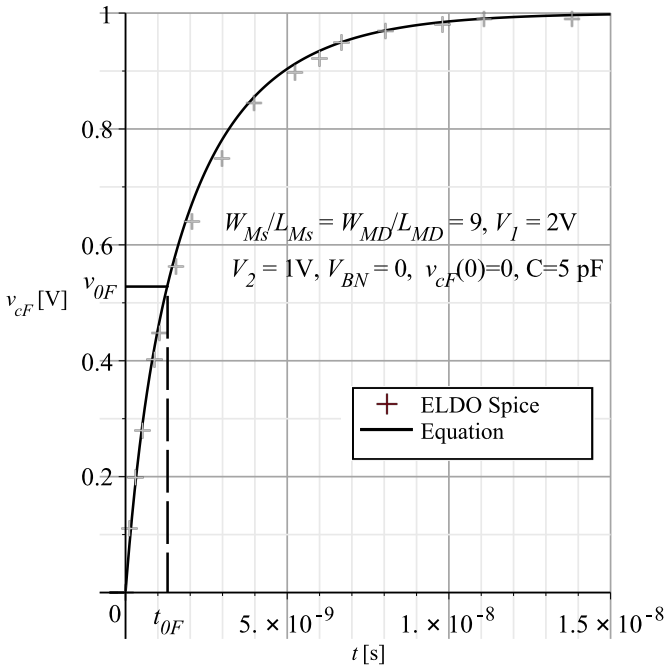


Figure 6.5: Time response characteristics of the circuit from Fig. 6.4

with the initial condition $v_c(t_0) = v_{c_0}$ for each of the intervals, as it is shown in Eq. 6.10. IC is the constant of integration. The drain current equation is the composite function (NF) in the form

$$i_c = \mathrm{f}\left[v_{ds}(t), v_{gs}(t), v_{TH}(v_c(t)), A_{bulk}(v_c(t)), \mu_{eff}(v_c(t))\right],$$

consequently, analytical solution would be unreasonably complicated for practical design. Thus, the estimation is done providing the *constant nested functions* v_{TH},A_{bulk} and μ_{eff} according this criteria: When $t \leq t_{0_F}$, the voltage v_{c_F} change in time is approximately same as in the beginning of the transient process. Contrariwise, when $t > t_{0_F}$ and $i_D = 0$ the characteristic curve is approximated by the nested function values which would acquire in the steady state.

The same principle is also used for the reverse configuration, as it is shown in Fig. 6.6. Bias voltages are listed in Table 6.3.

Table 6.3: Bias voltages of the nested functions (NF) V_{TH}, A_{bulk} and u_{eff}

Condition		Index of NF.		$\mathbf{V_{in}}$[V]	
		M_{D_i}	M_{S_i}	M_{D_i}	M_{S_i}
$i_s > 0$	$t < t_{0_F}$	D0	S0	$v_{c_F}(0_+)$	$v_{c_F}(0_+)$
	$t \geq t_{0_F}$	X	S	X	V_2
$i_s < 0$	$t < t_{0_R}$	X	SR	X	$v_{c_R}(0_+)$
	$t \geq t_{0_R}$	X	S	X	V_2

Therefore, solving of Eq. (6.13) can be only found by integrating the quadratic part of the voltage $[v_{gs}(t) - V_{TH}]^2$, eventually $v_{ds}(t)$ and $v_{ds}^2(t)$ for triode region. The time-varying voltage

v_{C_F} for the forward configuration is given by

$$v_{C_F}(t) = \begin{cases} V_{C_F}(0), & \text{for } t \leq 0 \\ \frac{\sqrt{C_1C_2}\cdot\tan\left[\frac{(t+\mathrm{IC}_{F1})\sqrt{C_1C_2}c_{oxe}}{2L\cdot CA_{bulk_{D0}}}\right]-C_3}{\mu_{eff_{D0}}W_{M_S}+C_1\left(A_{bulk_{S0}}-2\right)}, & \text{for } 0 < t < t_{0_F} \\ \frac{C_4 e^{\frac{t+\mathrm{IC}_{F2}}{C_5}}-V_2}{e^{\frac{t+\mathrm{IC}_{F2}}{C_5}}(A_{bulk_S}-2)-1}, & \text{for } t \geq t_{0_F}, \end{cases} \tag{6.14}$$

where L is channel length and c_{oxe} is electrical oxide capacitance. Integration constants, labeled IC_1 and IC_2, are generally calculated from the initial conditions that are substituted into Eq. (6.13) (Cauchy's equation):

$$\mathrm{IC}_1 = \frac{2LCA_{bulk_{D0}}}{\sqrt{C_1C_2}c_{oxe}}\arctan\left[\frac{v_{c_0}\left(\mu_{eff_{D0}}W_{M_S}+C_1\left(A_{bulk_{S0}}-2\right)+C_3\right)}{\sqrt{C_1C_2}}\right], \tag{6.15}$$

$$\mathrm{IC}_2 = C\frac{V_{DSsat_{Ms}}}{I_{Dsat0_{Ms}}}|_{V_{in}=V_2}\ln\left(\left|\frac{A_{bulk_S}\left[V_2-v_{c_0}\right]-2\left[V_1-V_{TH_S}-v_{c_0}\right]}{V_2-v_{c_0}}\right|\right)-t_0, \tag{6.16}$$

$$\begin{aligned} \mathrm{IC}_{F1} &= \mathrm{IC}_1|_{v_{c_0}=V_{C_F}(0_+)}, \quad \text{for } 0 < t < t_0 \\ \mathrm{IC}_{F2} &= \mathrm{IC}_2|_{t_0=t_{0F},v_{c_0}=V_{C_F}(0_+)}, \quad \text{for } t \geq t_0. \end{aligned}$$

Using the voltage V_{0_F} in Eq. (6.15), the initial time t_{0_F} is given by

$$t_{0_F} = \mathrm{IC}_{F1}|_{v_{c_0}=V_{0_F}} - \mathrm{IC}_{F1}|_{v_{c_0}=V_{C_F}(0_+)}, \quad V_{C_F}(0_+) < V_{0_F}. \tag{6.17}$$

Coefficients C_1, C_2, C_3, C_4 and C_5 are calculated from:

$$\begin{aligned} C_1 &= -A_{bulk_{D0}}\mu_{eff_{S0}}W_{M_S}, \\ C_2 &= -C_1(V_1-V_2-V_{TH_{S0}})^2 - \mu_{eff_{S0}}W_{M_D}(2V_1-2V_2-A_{bulk_{S0}}V_{THS0}), \\ C_3 &= -C_1(A_{bulk_{S0}}V_2-V_1-V_2+V_{TH_{S0}}) - \mu_{eff_{D0}}W_{M_D}(V_2-V_{TH_{D0}}), \\ C_4 &= A_{bulk_S}V_2-2(V_1-V_{TH_S}), \\ C_5 &= -C\frac{V_{DSsat_{MS}}}{I_{Dsat0_{MS}}}|_{V_{in}=V_2}. \end{aligned}$$

Discharge of the main capacitor is shown in Fig. 6.6. The CMOS inverter is modeled by the voltage source BV controlled by the time-varying voltage v_{cR}. The switch transistor is on after the switches S_1, S_2, S_3 are closed at $t = 0$ and the capacitor C_i was charged on the value in the interval of the voltages $v_{C_R}(0) \in (V_2, V_{SP})$.

The initial condition $v_{C_R}(0) \in (V_{IL}, V_{SP})$ will be considered to a complete description of time response characteristics. Then, the main capacitor is firstly discharged by the constant current I_S until the voltage of BV achieves V_1 at time $t = t_{0_R}$,

$$i_{C_R}(t) = \begin{cases} I_{S_R}, & \text{for } 0 < t \leq t_{0_R} \\ i_s(t), & \text{for } t \geq t_{0_R}. \end{cases} \tag{6.18}$$

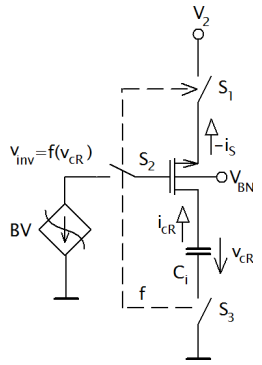


Figure 6.6: Configuration for the discharge of the main capacitor

Calculation of the constant current I_{S_R} follows from the static model, but it additionally considers the control voltages reffered in Table 6.3 (index SR). The default differential equation for

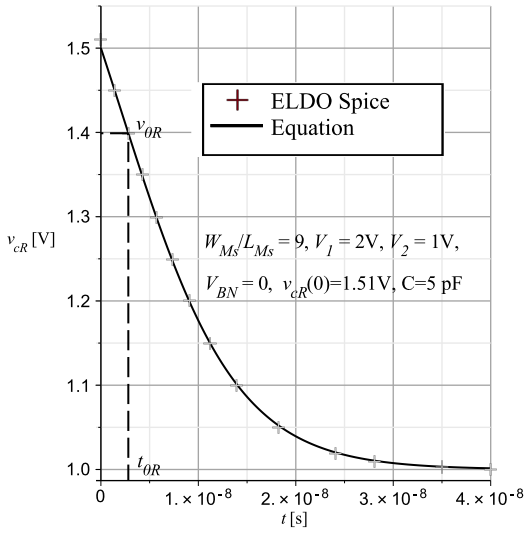


Figure 6.7: Time response characteristics of the circuit from Fig. 6.6

each of the time interval is the same as in the previous case,

$$v_{C_R}(t) = \begin{cases} v_{C_R}(0), & \text{for } t \leq 0 \\ -\frac{I_{S_R}}{C}t + v_{C_R}(0), & \text{for } 0 < t \leq t_{0_R} \\ \dfrac{V_2\left(A_{bulk_S} - e^{\frac{t+\mathrm{IC}_R}{C_5}}\right) + 2\left(V_1 - V_2 - V_{TH_S}\right)}{A_{bulk_S} - e^{\frac{t+\mathrm{IC}_R}{C_5}}}, & \text{for } t > t_{0_R}. \end{cases} \tag{6.19}$$

Because the voltages are equal to V_2 in steady state for both the configurations, the coefficients in the exponential functions are also the same. The integration constant IC_R can be easily expressed as

$$\mathrm{IC}_R = \mathrm{IC}_2|_{v_{c_0}=V_{C_R}(0), t_0=t_{0_R}} \tag{6.20}$$

and the point t_{0_R} is given by

$$t_{0_R} = \begin{cases} \frac{C}{I_{S_R}} \left[v_{C_R}(0) - V_{IL} \right], & \text{for } V_{SP} \geq v_{C_R}(0) > V_{IL}. \\ 0, & \text{otherwise.} \end{cases} \tag{6.21}$$

6.2.2 Minimization of the pumping losses

The sizing of the switch transistor will be discussed in this part. The main criterion of the optimal pump design is based on the maximum voltage gain at the end of each phase of the clock signal, as it is shown in Fig. 6.8. Sizing of the switch transistor M_{Si} can be set, so that the voltage gain is greater than $2V_2$, better V_{max} at point $T/2$. The transistor length is determined from condition (5.1) and the width is determined based on the following condition:

$$\max\{V_{C_F}(W_{MS}) + V_{C_R}(W_{MS})\}|_{t=T/2, t>t_0}. \tag{6.22}$$

The optimal width $W_{MS_{opt}}$ will be searched while using the *limit initial conditions* to satisfy the worst case that can be taken into account in the real circuit. Using the condition (6.22) and Eq. (6.14), (6.19) then the following equality is true:

$$\frac{\mathrm{d}V_{C_F}}{\mathrm{d}W_{MS}}|_{t=T/2, t>t_{0_F}} = -\frac{\mathrm{d}V_{C_R}}{\mathrm{d}W_{MS}}|_{t=T/2, t>t_{0_R}}, \quad v_{C_F}(0_+) = 0,\ v_{C_R}(0_+) = V_{SP}, \tag{6.23}$$

and it is giving desired value of the width at the known clock frequency. However, the optimal

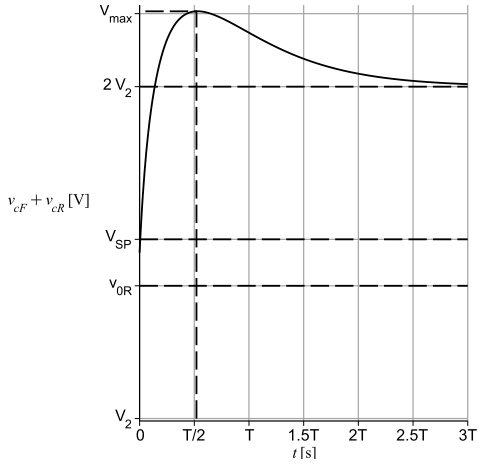


Figure 6.8: Time response characteristics for the pumping losses minimization

point can be estimated even in a simpler way. Both the time response characteristics $v_{C_F}(t)$ and $v_{C_R}(t)$ in the intervals $t > t_{0_F}$ and $t > t_{0_R}$ are compared to each other via its linearization in the initial time, as it is shown in Fig. 6.9. Providing the linear change voltage as in the initial time, transient process would be terminated at time τ–this parameter is equivalent to the time constant, but is function of the bias voltages (is not constant) unlike the first order linear

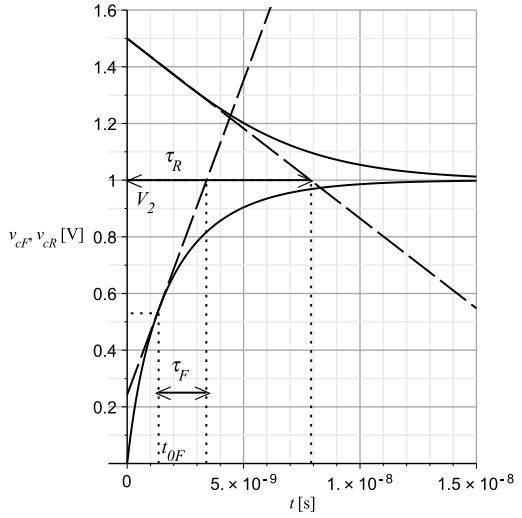


Figure 6.9: Linearization of the time response characteristics

systems. Generally, it is derived from the first order Taylor approximation,

$$\tau(v) = \frac{v_{C_\infty} - v_c|_{t=t_0}}{\dot{v_c}|_{t=t_0}}. \tag{6.24}$$

If the capacitor is charged from the inital value $v_c(t_0)$ to value in the steady state v_{c_∞}, then the voltage on the capacitor reaches the value $\Delta v_c = \alpha\,(v_{C_\infty} - v_{c_0})$ during time $t = k\tau$. Parameters $1 > \alpha > 0$ and $k \geq 0$ are multiple constants. The specific values of α and k parameters calculated for exponential function of $v_{C_R}(t)$, are shown in Table 6.4.

Table 6.4: Relationship between parameters k and α calculated from Eq. (6.14)

k	0.75	0.9	1	1.5	2	3	5
α	0.5	0.6	0.63	0.76	0.84	0.93	0.98

The voltage increment of the pump stage must not fall bellow the value $\Delta V_{max} \geq V_2$ during the half of the period, as it is shown in Fig. 6.6. Discharge time through the parameter τ_R primarily determines the amount of the pumping losses and $\tau_R > \tau_F$, thus

$$\{\Delta v_{C_F} + \Delta v_{C_R} \approx V_2\}|_{t=k\cdot\tau_R+t_{0_F}=T/2}. \tag{6.25}$$

Thence the parameter α is given by

$$\alpha = \frac{V_2}{V_{SP}}. \tag{6.26}$$

Parameter τ_R can be calculated from equation 6.24, however it is approximately given by the reverse current I_{S_R},

$$\tau_R(W_{M_S}) \approx \frac{(V_{SP} - V_2)C}{I_{S_R}|_{V_{inv}=V_1, V_{in}=V_{IL}}}. \tag{6.27}$$

Using the condition from Equation 6.25, the found width is given by

$$\boxed{W_{M_{S_{opt}}} = \frac{kC(V_{SP} - V_2)}{T\hat{I}_{S_R}} + \frac{\hat{I}_{S_R}(Tc_{t_0} + 2a_{t_0}) + \sqrt{D_{t_0}}}{2T\hat{I}_{S_R}b_{t_0}},} \tag{6.28}$$

where

$$\begin{aligned}
a_{t_0} &= \tfrac{2C \cdot A_{bulk_{D0}} W_{M_D} L \mu_{eff_{D0}} V_{0_F}}{c_{oxe}}, \\
b_{t_0} &= -A_{bulk_{D0}} \mu_{eff_{D0}} \mu_{eff_{SR}} W_{M_D} \left(V_{t_a} + V_{t_b} V_{t_c}\right), \\
c_{t_0} &= \left(\mu_{eff_{D0}} W_{M_D}\right)^2 \left(-V_2 + V_{TH_{SR}}\right) V_{0_F} + \left(\mu_{eff_{D0}} W_{M_D}\right)^2 \left(-V_2 + V_{TH_{SR}}\right)^2, \\
D_{t_0} &= \left[2kC \cdot b_{t_0}(V_2 - V_{SP}) - \hat{I}_{S_R}\left(Tc_{t_0} + 2a_{t_0}\right)\right]^2 + 16kCa_{t_0}b_{t_0}\hat{I}_{S_R}(V_2 - V_{SP}) \\
&\text{and} \\
V_{t_a} &= V_{TH_{SR}}\left(V_{TH_{SR}} A_{bulk_{SR}} - 2V_1 + 2V_2\right), \\
V_{t_b} &= V_2\left(A_{bulk_{SR}} - 1\right) - V_1 + V_{TH_{SR}}, \\
V_{t_c} &= V_{0_F} - 2\left(V_2 - V_{TH_{SR}}\right).
\end{aligned}$$

Parameter k is selected from Table 6.4 based on the parameter α from Eq. (6.26), $\hat{I}_{S_R}$ is the drain current calculated for the unity width $\left(\hat{I}_{S_R} = I_{SR}/W\right)$.

In case the multiple of the time constant satisfies the session $k\tau_R \gg t_{0_F}$, Eq. (6.28) now becomes to

$$\boxed{W_{M_{S_{opt}}} \doteq \frac{2kC(V_{SP} - V_2)}{T\hat{I}_{S_R}}.} \tag{6.29}$$

6.2.3 Sizing of the "diode" transistor

Analysis results show that dynamic properties are not practically dependent on the sizing of the transistor M_{D_i} in the wide range of the ratio W/L. It is only need to be adequately dimensioned for the pump output load current i_L in steady state. After the clock signal $\bar{\phi}$ goes to H logic level (corresponds to V_{DD}), the output voltage starts from the initial value $V_{out,av} - V_r/2$ and can theoretically achieve the maximum value $V_{out,max}$ during $T/2$; $V_{out,av}$ is the required average value of the output voltage and V_r is the peak value of the ripple voltage. Situation is shown in Fig. 6.10. The transistor $M_{D_{N+1}}$ is on in the active interval of the clock signal. Time response characteritics will be firstly determined. Providing the capacitive character of the load impedance, the state desription of the voltage on the capacitor $v_{out,av}(t)$ is in an accordance to Eq. (6.13) ($R_L \to \infty$). The step response characteristics of the circuit in Fig. 6.11 after closed S at t=0, when the capacitor is charged from the initial value $v_c(0_+) = v_{c_0}$ to the steady state v_{c_∞}, is given by

$$v_c(t) = \begin{cases} v_{c_0}, & \text{for } t \le 0, \\ \frac{W_{M_D}\beta_D v_{c_\infty} t(v_{c_\infty} - v_{c_0}) + C v_{c_0}}{W_{M_D}\beta_D t\left(v_{c_\infty} - v_{c_0}\right) + C}, & \text{for } t > 0. \end{cases} \tag{6.30}$$

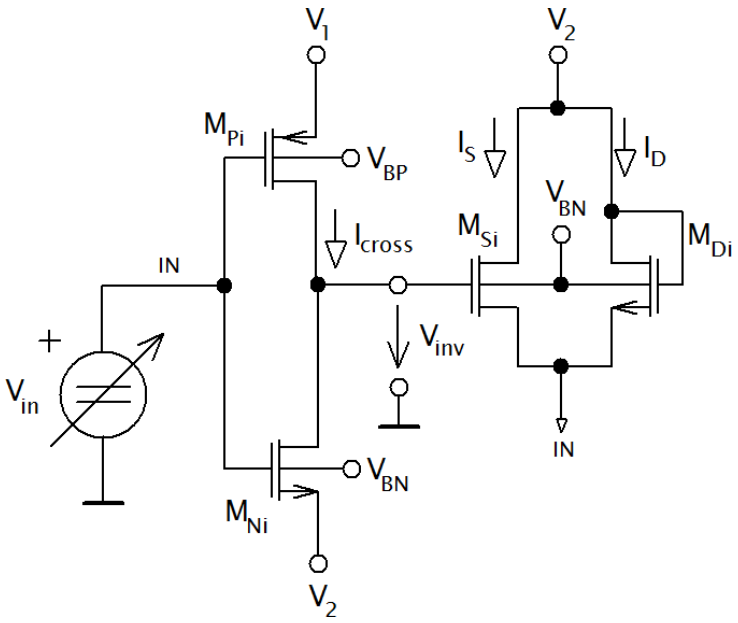


Figure 6.10: The last stage of the charge pump and waveform of the output voltage in the steady state

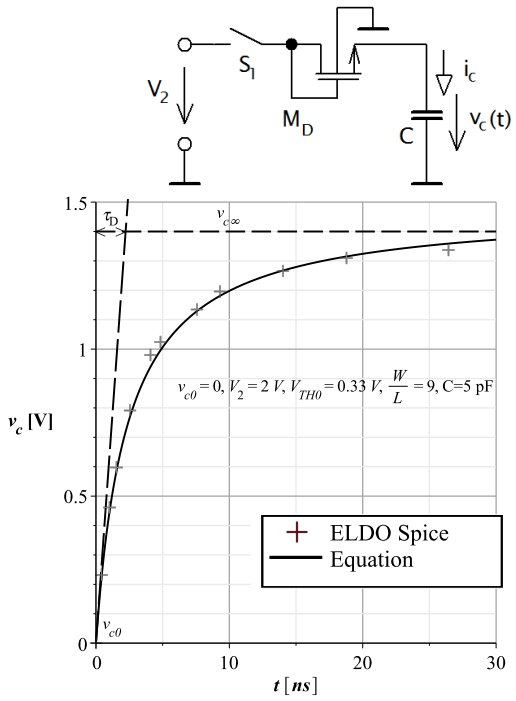


Figure 6.11: Time response characteristics of the diode transistor

The maximal output voltage value v_{c_∞} is equal to V_{0F} from Equation 6.12 and β factor is calculated at the bias voltages in steady state,

$$\beta_D = \frac{1}{2L}\frac{\mu_{eff}c_{oxe}}{A_{bulk}}|_{V_{GS}\doteq V_{DD},V_{SB}=V_{max}}.$$

The voltage increment α_D at time expressed as the multiples k of the τ_D parameter, $v_c|_{t=k\tau_D} = \alpha_D(v_{c_\infty} - v_{c_0})$, is listed in table 6.5.

Table 6.5: Relationship between parameters k and α_D calculated from Eq. (6.30)

k	0.5	0.7	1	2	5	10	20	40	∞
α_D	0.32	0.39	0.48	0.63	0.77	0.85	0.91	0.97	1

The optimal width of the M_D transistor is determined from condition, that the voltage v_{out} increment from Fig. 6.11 must achieve the maximal allowable ripple voltage V_r during T/2 at the desired average value of the output voltage. The maximal output voltage $V_{out,max}$ is calculated from Eq. (6.30), into which the concrete values are substituted for input voltage V_2,

$$v_{c_\infty} = V_{0_F}|_{V_2=V_{out,av}+V_{r_{max}}/2+V_{DD}}. \tag{6.31}$$

Of course, the specified amplitude of the AC voltage value $v_r(t)$ depends on both the external load R_L, C_L and on the equivalent internal pump impedance including R_{pump}, C_{pump}. Consequently, the following inequality must be true[2]:

$$\{V_{out}\,(W_{M_D}) \geq v_{c_0} + \alpha_D\,(v_{c_\infty} - v_{c_0})\}\,|_{t=T/2}. \tag{6.32}$$

Therefore,

$$\boxed{W_d \geq \frac{2\,(C_L + C_{pump})}{T\beta_D\,(v_{c_\infty} - v_{c_0})}\frac{\alpha_D}{1-\alpha_D},} \tag{6.33}$$

where pump capacitance may be neglected, provided $C_L \gg C_{pump}$ and $\alpha \geq \frac{V_{r_{max}}}{v_{c_\infty}-v_{c_0}}$ with the minimal value of the average voltage $V_{out,av}$. However, parameter α_D should be chosen, so that the load capacitor was charged by the large current all along of the active interval. Consequently, the transistor is fully switched on ($v_{gs} \gg v_{TH}$, strong inversion) and the load voltage is the approximately linear function of time. Results from Table 6.5 show that significant voltage change meets this assumption for α, which no exceeding the value about 0.7. *Otherwise, the width quickly grows with $\alpha \to 1$ despite the improvement of dynamic properties.* Example of the width calculation vs. α parameter is shown in Table 6.6.

Table 6.6: Width of the M_{D_i} transistor vs. α parameter

Parameters
$L = 5\mu$m, $\beta_D = 135\,\mathrm{AV^{-2}m^{-1}}$,$\mathrm{V}_{DD} = 1\,\mathrm{V}$, $\mathrm{V}_{out,av} = 3.3\,\mathrm{V}$,
$V_{r_{max}} = 50\,\mathrm{mV}$, $C_L = 20\,\mathrm{pF}$, $T = 100\,\mathrm{ns}$

$\alpha[-]$	0.1	0.2	0.4	0.6	0.8	0.9	1
$W_{M_D}[\mu\mathrm{m}]$	5	11	30	68	182	411	∞

6.2.4 Experimental part

All assertions from the previous parts were be verified in the three-stages charge pump including the real models of all the components. The various types of MOSFETs, M_{Si}, M_{N_i}, M_{Pi} and M_{D_i}

[2]The procedure will be further refined.

are the same sized in each the pump stage. Simulation parameters (unless noticed otherwise) are specified in Table 6.7. Firstly, the equation validity expressing the optimal point W_s/L_s

Table 6.7: Simulation parameters

Parameter		**Value**
Temperature	ϑ	24° C
Number of stages	N	3
Supply voltage	V_{DD}	1.5 V
CLK frequency	f_c	10 MHz
Main capacitance	C	40 pF
Load ressistance	R_L	200 kΩ
Load capacitance	C_L	20 pF
Channel length of N(P)MOS	L	1μ m
W/L ratio of the M_{S_i}	W_s/L_s	2
M_{P_i}	W_p/L_p	3
M_{N_i}	W_n/L_n	1
M_{D_i}	W_d/L_d	10

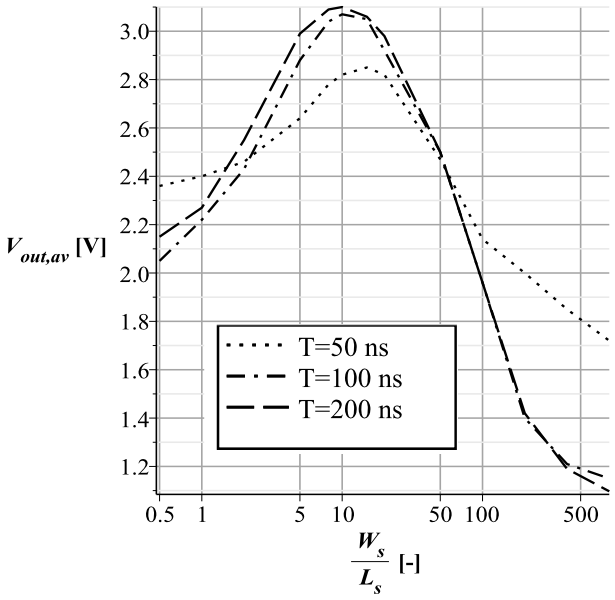


Figure 6.12: Pump output voltage vs. the ratio W_s/L_s

(Fig. 6.12) will be tested via the comparison of the calculated functional values $V_c = v_{C_F} + v_{C_R}|_{t=T/2}$ from Eq. (6.14, 6.19) and the pump output voltage value $V_{out,av}$ dependending on the ratio W_s/L_s. The optimal width calculated from simplified Eq. (6.29) is listed in the last line. Setting of the voltages V_1, V_2 and source-bulk bias voltage of the N/PMOS for the calculation must first be resolved. Starting from the fact, that the maximal output voltage value with change of the circuit parameters (clock frequency, main capacitances, etc.) is achieved, just when the voltage gain of the first pump stage is the maximal (it decreses with increasing the number of stages). In accordance to situation in Fig. 5.3, the power supplies of the pump stage (Fig. 5.6) are $V_2 = V_{DD}$, $V_1 = 2V_{DD}$. Bulk of the NMOS is connected to ground ($V_{SB_N} = V_{DD}$) and bulk

of the PMOS is selected, so that the inverter switching point was the maximum (at the constant setting of the inverter transistors sizing). Using the definition V_{SP} [23, 24], then $V_{BS_P} = 0$ (in the last pump stage). As a consequence, the worst case of the V_{SP} voltage, labeled $V_{SP_{max}}$ in the N-stages pump is taken into account. Then, general formula of the $V_{SP_{max}}$ ($V_{B_P} = V_{B_N} = 0$) can be written as,

$$V_{SP_{max}} = V_{SP}|_{V_2=V_{DD},V_1=2V_{DD},V_{SB_N}=V_{DD},V_{BS_P}=0}. \tag{6.34}$$

Table 6.8: Simulation results

$v_{c_\infty} = 2V_2 = 3\,\mathrm{V}$, $V_c(0) = V_{SP_{max}} = 2.41\,\mathrm{V}$						
	$T = 50\,\mathrm{ns}$		$T = 100\,\mathrm{ns}$		$T = 200\,\mathrm{ns}$	
$\frac{W_s}{L_s}\,[-]$	$V_c[V]$	$V_{out,av}[V]$	$V_c[V]$	$V_{out,av}[V]$	$V_c[V]$	$V_{out,av}[V]$
0.5	2.39	2.36	2.42	2.05	2.49	2.15
1	2.42	2.4	2.48	2.22	2.59	2.27
2	2.49	2.46	2.60	2.43	2.75	2.55
5	2.64	2.64	2.81	2.88	**2.99**	**2.99**
8	2.76	2.78	**2.94**	**3.04**	**3.06**	**3.09**
10	2.81	2.82	**2.99**	**3.07**	**3.07**	**3.1**
15	**2.92**	**2.85**	**3.05**	**3.05**	3.05	3.06
20	**2.98**	**2.82**	3.07	2.92	3.04	2.98
50	3.06	2.47	3.02	2.5	3.01	2.5
100	3.02	2.14	3.01	1.96	3.01	1.96
200	3.01	2.0	3.0	1.4	3.0	1.42
400	3.0	1.85	3.0	1.21	3.0	1.19
800	3.0	1.72	3.0	1.15	3.0	1.097
$W_{MS_{opt}}[\mu\mathrm{m}]$	43.8		21.9		10.9	

Example 6.1

Estimate the switch transistors width for the cross-coupled charge pump, when: $V_{DD} = 1.5\,\mathrm{V}$, $V_{Bn} = 0$, $V_{Bp} = 0$, $T = 100\,\mathrm{ns}$, $C = 40\,\mathrm{pF}$. Channel length $L = 5\,\mu\mathrm{m}$ is same for all the transistors.

- the maximal inverter switching point at appropriate bias voltage values $V_2 = V_{DD} = = V_{SB_N} = 1.5\,\mathrm{V}$, $V_1 = 2V_{DD} = 3\,\mathrm{V}$ and $V_{BS_P} = 0$ (Eq. 6.34) is $V_{SP_{max}} = 2.41\,\mathrm{V}$
- α factor is written as $\alpha = \frac{V_2}{V_{SP_{max}}} = \frac{1.5\,\mathrm{V}}{2.41\,\mathrm{V}} = 0.62\,[-]$,
- corresponding coefficient alpha detremined based on the data from Tab. 6.4 is $k \approx 1\,[-]$,
- value of the drain current is calculated from Eq. 5.36 as $\hat{I}_{S_R} = \hat{I}_{Dsat0}|_{V_{GS}=V_1-V_2=1.5\,\mathrm{V},V_{SB}=V_2=1.5\,\mathrm{V}} \approx 34$ A/m, for $V_{IL} > V_2 + V_{DSsat_{Ms}}$,
- finally, the strength from Eq. 6.29 is equal to

$$W_{M_S} \doteq \frac{2kC(V_{SP} - V_2)}{T\hat{I}_{S_R}} = \frac{2 \cdot 1 \cdot 40\,\mathrm{pF} \cdot (2.41 - 1.5)\,\mathrm{V}}{100\,\mathrm{ns} \cdot 34\,\mathrm{A/m}} \doteq \mathbf{21.9}\,\mu\mathrm{m}.$$

Conversely, the voltage gain is not change in a wide ratio range W_D/L_D of the diode

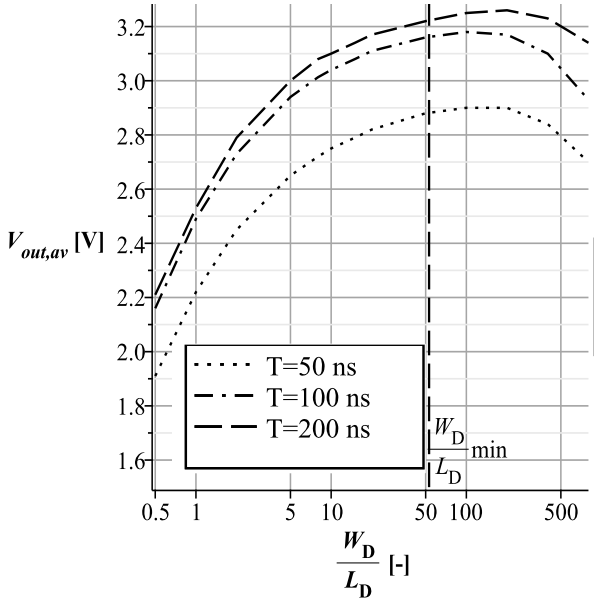


Figure 6.13: Pump output voltage vs. the ratio W_D/L_D

transistor, as it is shown in Fig. 6.13. The data from table show that the pump output voltage is the maximal, if the time response characteristic of the pump stage at time $T/2$ does not exceed the value V_{max}, as it is shown in Fig. 6.8. The optimal width W_s must be less than the calculated value from equation, otherwise, the pumping losses cause the discontinuous decrease of the output voltage due to the openning the feedback of the system (the condition 5.12 is not satisfied). It is a critical parameter from the view of the design process.

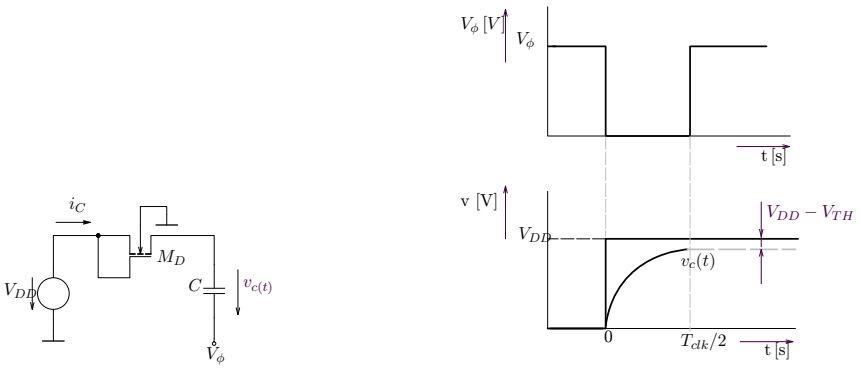
6.3 Guidlines on the main capacitor sizing

Value of the main capacitor(s) value is an important parameter for optimal voltage gain in each of the pump stages. The goal is to achieve such an equivalent internal impedance so that the pump provides the required output voltage at the defined load current I_L. As it is well known, the solution from this point of view is ambiguous because low pump equivalent impedance can be ensured by setting one or more of the other pump parameters, as the number of stages, clock frequency, etc. However, not only the voltage gain is a design criterion. Other design aspects, for example, power efficiency, total pump area, etc. should be taken into account. In this article, the main capacitor sizing is presented through the following two design criteria:

- maximal pump voltage gain, while the number stages is minimal

- satisfaction of dynamic properties–rise time

Relationship for the switch transistor sizing, which minimalizes dominant part of pump losses, assumes known main capacitor value. On the contrary, output voltage and other



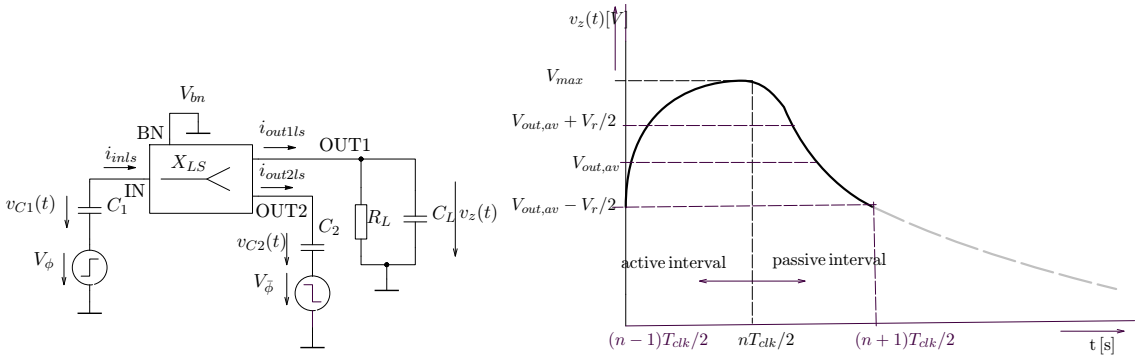
(a) (b)

Figure 6.14: Charge of the main capacitor in the first pump stage: diagram (a) and time response characteristics (b)

and other pump parameters in the steady state are not practically dependent on the diode transistor sizing, setting of the minimal ratio W_D/L_D is necessary to supply the current to load in the active interval of CLK. However, the situation may be quite different in terms of dynamic characteristics. Diode transistors ensure charge transport between capacitors when the output voltage rises from the initial (zero) to the final value. sufficient voltage increase at each node is a necessary condition that the feedback loop in each of the pump stage has been closed. Next part will be focused on the finding of both parameters C and W_D/L_D that fulfill the previous criteria. Diode transistors must transport the maximum possible amount of charge per half of the period of the clock signal, even if the switch transistor of the stage is OFF. The worst case occurs in the first pump stage when the power supply V_{DD} is connected and all the capacitors were discharged ($u_c = 0$) before initialization at $t = 0$. Fig. 6.14 shows the main capacitor charging from the DC voltage source through the M_D transistor in the first pump stage, while the main capacitor terminal is connected to a low logic level ($V_\phi = 0$) of the clock signal. The symbolic description of the time response characteristic of the equivalent circuit from Fig. 6.14a was derived in section 6.11. Relationship between main capacitor value and M_D transistor sizing follows from the stored charge in passive interval of CLK, $v_c|_{t=T_{clk}/2} = \alpha \cdot v_{c_\infty}$, where v_{c_∞} is the end (maximal) value in steady state and parameter α determines the proportion of total charge. After that,

$$\boxed{W_{MD} = \frac{2C}{v_{c_\infty}\beta_D T_{clk}} \frac{\alpha}{\alpha - 1}, \quad \text{for } \alpha \in (0,1).} \tag{6.35}$$

The second equation satisfying required pump voltage gain will be found based on the time response characteristic of the last pump stage, see Fig. 6.15. In active interval,



(a) (b)

Figure 6.15: Energy transport in the last pump stage: block diagram (a) and time response characteristics (b)

current through capacitor C_1 is splitted between main capacitor C_2, labeled i_{out2ls} and load impedance R_L and C_L, labeled i_{out1ls}. Then

$$i_{inls}(t) = i_{out1ls}(v(t)) + i_{out2ls}(v(t)).$$

Analytical description of the input/output current is following from simplified BSIM model equation, see Chapter 5. In steady state, the output voltage $v_z(t)$ is moving between values $V_{out,av} - V_r/2$ and $V_{out,av} + V_r/2$, where $V_{out,av}$ is average value of the output voltage and V_r is peak-ripple voltage value (Fig. 6.15b). Circuit from Fig. 6.15a is described by the three following state equations,

$$\begin{aligned} \dot{v_{c1}} &= \frac{-1}{C_1} i_{inls} \\ \dot{v_{c2}} &= \frac{1}{C_2} i_{out2ls} \\ \dot{v_z} &= \frac{1}{C_L}\left(i_{out1ls} - \frac{v_z(t)}{R_L}\right), \end{aligned} \tag{6.36}$$

with general initial conditions $v_{c1}(t_0)$, $v_{c2}(t_0)$, $v_z(t_0)$ and $V_\phi = V_{DD}$ for $t \in \left\langle (n-1)\frac{T_{clk}}{2}, n\frac{T_{clk}}{2} \right\rangle$, where $n = \{1,2,\ldots,k\}$. Graphical solution of Eq. 6.36 for specific values is shown in Fig. 6.16 Initial conditions for design purpose are determined from theoretical maximal end values of the node voltages in passive interval of CLK at $t = t_0 = (n-1)\frac{Tclk}{2}$, when $V_\phi = 0$ and $V_{\bar{\phi}} = V_{DD}$:

$$\begin{aligned} v_{C1}(t_0) &= \frac{1}{k} \cdot (V_{out,av} - V_r/2) - V_{DD} + +V_{TH}|_{V_{BS}=-1/k \cdot v_z(t_0)} \\ v_{C2}(t_0) &= v_{C1}(t_0)|_{k=1} + V_{DD} - V_r/2 - -V_{TH}|_{V_{BS}=-v_{C1}(t_0)|_{k=1}}, \\ v_z(t_0) &= V_{out,av} - V_r/2, \end{aligned} \tag{6.37}$$

where k has same meaning as parameter α from Eq. 6.35. It is assumed that $C = C_1 = C_2$

and $C \gg C_s$, where C_s is strange pump capacitance. Parameter k must be less than one, for example $k = 0.95$, because it is provided that internal transistor(s) is ON at the beginning of the transition and $v_z(t)$ must exceed the value $V_{out,av} + V_r/2 < V_{max}$. When k were too small, total storage charge would not be utilized in the real circuit. Final solution for charge pump design is given by numerical intersection of Eq. 6.35 and time response characteristic $v_z(t)$ from Eq. 6.36, which meets the inequality:

$$\boxed{v_z(W_{MD},C)|_{t=nT_{clk}/2} \geq V_{out,av} + V_r/2 \quad (\leq V_{max}).} \tag{6.38}$$

If the numerical algorithm will not find a suitable pair C and W_{MD}, then parameter α must be decreased in the next step. The optimal solution is at the point $v_z = V_{max}$ because load capacitor is not discharged in the active interval. It is favorable from the view of static efficiency. After that, the output voltage drop in the passive interval is caused by only the real part of the load impedance Z_L (leakage current is neglected) according to the known equation,

$$v_z(t) = V_{max} \cdot e^{-\frac{t}{\tau}}, \quad \text{for } t \in \langle nT_{clk}/2, (n+1)T_{clk}/2\rangle \tag{6.39}$$

Using the simplified formulae for start and end values $V_{max} \approx V_{out,av}+V_r/2$, $v_z|_{t=(n+1)T_{clk}/2} = V_{out,av} - V_r/2$, then the ripple output voltage for sufficiently small voltage change during

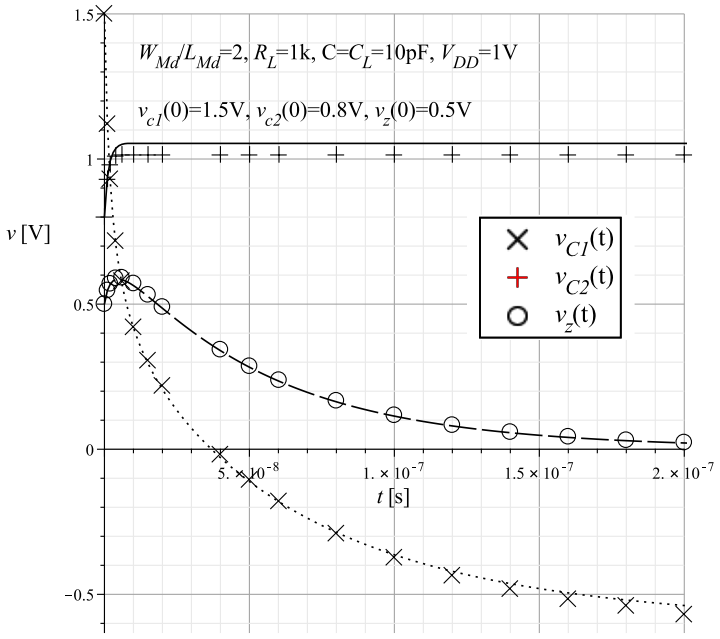


Figure 6.16: Time response characteristic of the last pump stage–calculated waveform and simulation results

period can be estimated from:

$$V_r \approx 2V_{out,av}\frac{1-e^{-\frac{T_{clk}}{2\tau}}}{1+e^{-\frac{T_{clk}}{2\tau}}}, \tag{6.40}$$

where $\tau = R_L C_L$ is time constant. Equation (6.40) is suitable for estimation of the output filter capacitor value:

$$\boxed{C_L \geq \frac{T_{clk}}{2R_L \cdot \ln\left(\frac{2V_{out,av}+V_{r_{max}}}{2V_{out,av}-V_{r_{max}}}\right)}.} \tag{6.41}$$

6.3.1 Experimental part

Verification of the mentioned procedure is done on the specific example. The task is to estimate main capacitor value and diode transistor sizing (under given criteria) for the charge pump, which gives output voltage $V_{out,av} = 4\,\mathrm{V}$ and load current $I_L = 4\mu\mathrm{A}$. The maximal peak value of the ripple output voltage at nominal load current must not exceed 20 mV. Power supply voltage is $V_{DD} = 1\,\mathrm{V}$ and clock signal frequency is $f_{clk} = 10\,\mathrm{MHz}$. Channel length of the MOSFETs is $L = 1\,\mu\mathrm{m}$.

- Minimum load capacitor value is calculated from Eq. 6.41 is,

$$C_L \geq \frac{1/10^7\mathrm{Hz}}{2\cdot(4\mathrm{V}/4\cdot10^{-6}\mathrm{A})\cdot\ln\left(\frac{2\cdot4\mathrm{V}+0.02\mathrm{V}}{2\cdot4\mathrm{V}-0.02\mathrm{V}}\right)} \doteq 10\,\mathrm{pF},$$

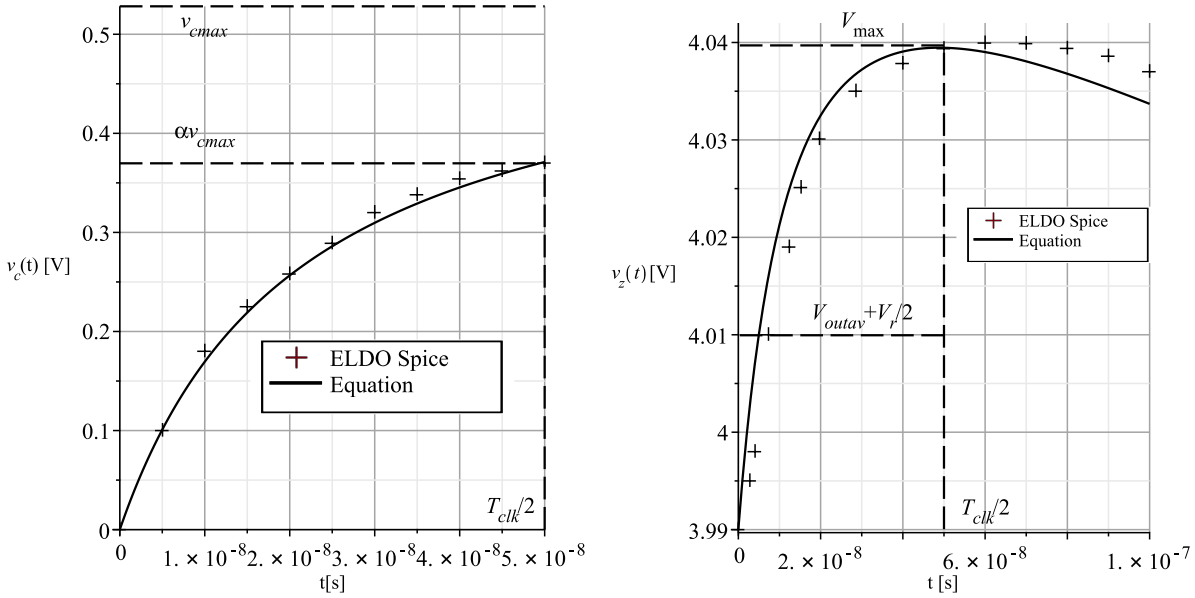
- initial conditions for solution of state equations (Eq.6.36) are calculated from Eq. 6.37 for $k = 0.95$ with using BSIM model parameters. Active interval, i.e. time range of the response characteristic lies in interval $t \in \langle 0, T_{clk}/2\rangle$,

$$\begin{aligned} v_{C1}(0) &= \frac{1}{0.95}(4-0.01)\mathrm{V} - 1\mathrm{V} + 0.93\mathrm{V} \doteq 4.17\,\mathrm{V}, \\ v_{C2}(0) &= (3.94+1-0.01-0.945)\,\mathrm{V} \doteq 3.986\,\mathrm{V}, \\ v_z(0) &= (4-0.01)\,\mathrm{V} = 3.99\,\mathrm{V}, \end{aligned}$$

- keeping both design criteria and condition 6.38, both the parameters are found from numerical solution of equations 6.35 and 6.36. One solution is also set

$$\boxed{\{C, W_{Md}\} = \{9.9\,\mathrm{pF}, 4.8\mu\mathrm{m}\}, \quad \text{for } \alpha = 0.7.}$$

Graphical representation of the responses is shown in Fig. 6.17. When the diode transistor was sized only under the fist criterion, width is $\mathbf{W_{Md}} \simeq \mathbf{26}\,\mu\mathrm{m}$ for $\alpha = 0.95$ at the same capacitor sizing.



(a) (b)

Figure 6.17: Time response characteristics of Example

It remains to verify obtained results in real-model pump structure, where the other component values are: $W_p = 5\,\mu$m, $W_n = 16\,\mu$m and $W_s = 2\,\mu$m. The minimal number of stages is $N = 4$, as implies from the following graph in Fig. 6.18. The characteristic is compared to the simulation results of the complex N-stage pump model. Relative error in the given range is listed in the graph. The following table shows that by re-

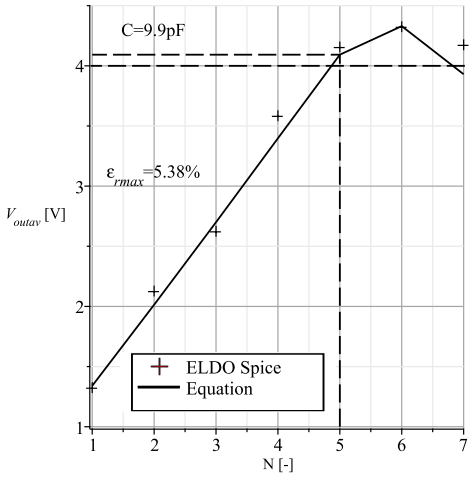


Figure 6.18: Pump output voltage vs number of stages

ducing the number of pump stages it is no longer possible to reach the required output voltage level while the main capacitor value is distinctly increased. Generally, condition $\lim_{C\to\infty} V_{out,av} = V_k$, for each $V_k \in R$ is allways valid.

Table 6.9: Pump output voltage vs. main capacitance value

							$N = 4$	
C [pF]	1	2	4	8	**9.9**	20	40	80
$\mathbf{V_{out,av}}$ [V]	2.055	2.5025	2.94	3.31	**3.40**	3.61	3.71	3.78

6.4 The MOSFET capacitor sizing

Main capacitors are commonly implemented using MOS transistors on design chip, where these MOSFETs are realized in the same technology process. This is one of the main advantages of realization. Nonlinear character of the component can be undesirable in these applications, where the emphasis is placed on analog signal processing (analog-digital converters). Charge transport in voltage converters via non-linear capacitances does not matter much (it may be even beneficial in some cases) but only the condition of the minimum capacitance value during its changes must be kept due to the correct function. Using BSIM model equations, the symbolic description of the MOS capacitor sizing will be introduced. Supposing the configuration from Fig. 6.19, total capacitance

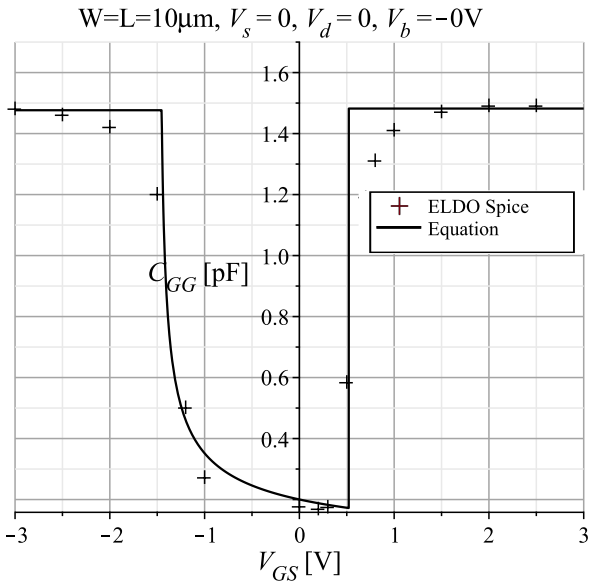


Figure 6.19: MOS gate capacitance

is given by

$$C_{MOS}(V) = \frac{\partial Q_g}{\partial V_g}. \tag{6.42}$$

If the MOS will be used as a capacitor, operation in accumulation region ($V_{GS} \ll V_{TH}$) is required. After that, for long channel technology process, total capacitance is approximately equal to $C \approx W_{eff} L_{eff} c_{oxe}$ [23]. However, during the pump rise time and overcharging, the voltage on capacitors can become to zero or negative value. In the subthreshold region, real MOS capacitance is markedly smaller, see Fig.6.19. Charge $Q_{g,sub}$

is defined as [27]

$$Q_{g,sub} = W_{eff} L_{eff} C_{oxe} \frac{K_{1ox}^2}{2} \left(-1 + \sqrt{\zeta}\right), \tag{6.43}$$

where $\zeta = \frac{4(V_{GS} - \mathrm{VFBCV} - V_{BS})}{K_{1ox}^2}$, C_{oxe} is electrical oxide capacitance, K_{1ox} is body effect parameter and $VFBCV$ is flat-band voltage. If the parameter $VFBCV$ is not given, then is calculated from [27]

$$VFBCV = V_{TH0} - \phi_s - K_1 \sqrt{\phi_s},$$

where ϕ_s is surface potential and V_{TH0} is threshold voltage at zero bias voltages. From the both previous equations, minimal capacitor value for charge pump is defined at bias voltage $V_{GS} = V_{TH}$:

$$\boxed{C_{min}|_{V=V_{TH0}} = \frac{W_{eff} L_{eff} C_{oxe}}{\sqrt{1 + \frac{4(\phi_s + K_1\sqrt{\phi_s})}{K_{1ox}^2}}}.} \tag{6.44}$$

6.5 Summary

Design of the pump functional blocks was discussed in this chapter. The main criterion of the design process is maximal pump voltage gain, the static efficiency, respectively. Description of these blocks was beased on equations, which were declared in the previous chapter. All the formulae were verified in ELDO Spice. Important results and consequences will be summarized.

Inverter draft is based on the low cross current during the transition between logic high and logic low levels. The sensitivity analysis of the switching point to the sizing of the transistors shows that it is possible to find the optimal ratio $R = \frac{W_n}{L_n}\frac{L_p}{W_p}$, while keeping a relatively big ratio W/L of the NMOS and PMOS transistors. It is very favorable from a time response perspective. It is recomended to select solution satysfying relationship $W_n \gg W_p$ because the pump losses caused by the reverse current through the switch transistor are also minimized. Average value of the cross current is the linear function of the strength of the inverter MOSFETs.
Other important implications of the design process can be summarized in the following items:

- Asymmetric DC characteristics; switching point is not equal to the half supply voltage. It is not an appropriate configuration in a digital circuit (rise time versus fall time, noise margine for high versus low logic level,...), while these properties are not meaningful in analog circuits.

- Propagation delays between logic levels should be short because of the possibility of setting small effective switching resistances (large width) of the NMOS and PMOS. Propagation delays are not the same. Propagation delays of the inverter must be very short in comparision to the pulse width of the CLK.

- The cross current is very small if the operating point of the inverter is set to the linear region of the voltage transfer characteristics.

- Static and dynamic properties are insensitive to the dimensional tolerance of the transistors. It follows from the principle of the design process.

All proposals were validated by real circuit simulations.

The width of the switch and "diode" transistor were determined based on the analytical expression of the time response characteristics of the pump stage as an analog block. The switching ressistance of the M_S transistor cannot be very small because increasing the ratio W/L, the reverse switch current decreases pump efficiency. This fact emerged from the study of basic properties of the pump topology. Design process was based on the reverse switch current minimization during a period of the clock signal. The found relationship $W_{Ms_{opt}}$, see Eq. 6.28, (6.29), can be applied for N-stage charge pump, providing the adequate bias voltages (power supply, source-bulk voltages). This ratio can be smaller than one at the extreme input parameters (power supply, clock frequency). Exceeding the critical value of the reverse current, the pump output voltage is discontinously decreased because the basic condition (5.12) is not valid. Thus, the width (equivalent MOSFET resistance) cannot be excessively large.

The pump properties (static and dynamic) are near not dependent on the width of the "diode" transistor, as is prooved by the simulation results. An estimation of the minimal width W_D, see Eq. (6.33), is possible to determine from the requirements of the output load current and the output ripple voltage.

Main capacitor value in charge pump was found, so that the static efficiency (maximal voltage gain - low equivalent internal impedance at defined load current) and dynamic properties (rise time after connecting power supply voltage) were secured. Under given conditions, capacitor sizing is connected with the diode transistor sizing. Both the parameters W_{MD} and C were found as intersection of time response characteristics in first stage (Fig. 6.14) with zero initial condition (Eq. 6.35) and the last pump stage (Fig. 6.15) in steady state (Eq. 6.36), so that the energy transport would be maximal in half of the period of CLK. As a result of this, the load capacitor is discharged only in the passive interval. Thence, the minimal load capacity value was derived from the peak value of the output ripple voltage (Eq. 6.41). Determination of these parameters was shown in the practical example with simulation results in N-stage circuit topology (Fig. 6.18). The solution was designed for the minimal number of stages, as it is evidenced in Tab. 6.9. But in general terms, this task is not unambiguous (N vs. C, etc.), as it was explained. If the nonlinear MOS capacitor is used, then the minimal capacity value (Fig. 6.19) should be respected (Eq. 6.44).

Chapter 7

Estimation of the pump properties

Estimation of the static and dynamic properties of the cross-coupled charge pump (Fig. 3.1) through the mathematical description is a comprehensive task. Many reasons have been mentioned and demonstrated by the simulation results. Simulations are the usual way of the optimal quasi-analog circuits design. Digital model is not an option due to its low

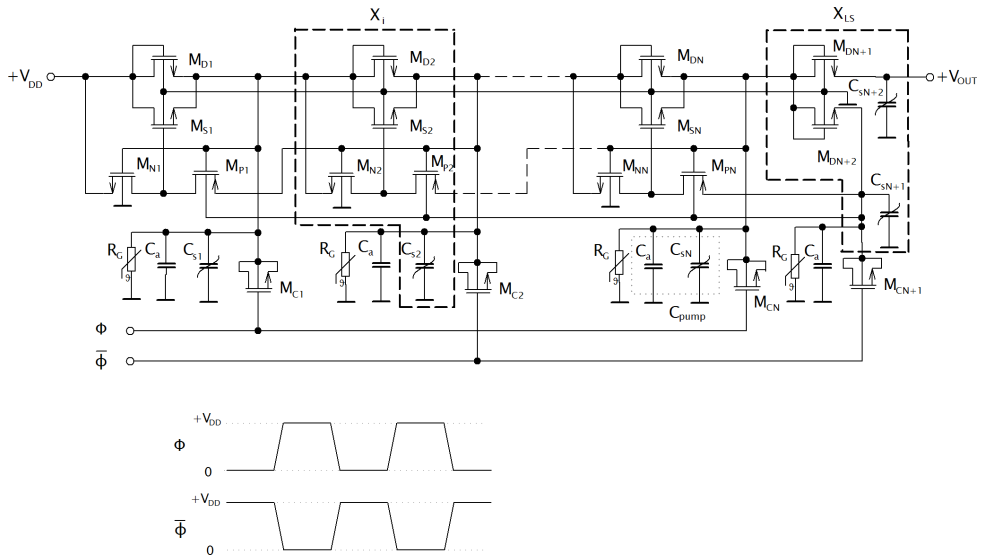


Figure 7.1: Cross-coupled charge pump diagram implemented with MOS capacitors and parasitic impedances

accuracy, as it was outlined in the previous chapters. In this chapter, the attention will be focused on the **program procedure**, which allow *to estimate the charge pump properties.* Firstly, the strategy of the solution through the state description of the system will be explained. The main part deals with principle of the computational algorithm which core is operating with previously derived analytic formulae of the analog blocks, i.e. *complex model of the pump stage blocks from Fig. 5.9 is applied.* Moreover, MOSFET nonlinear main capacitors and the higher-level effects–added parasitic capacitances C_{mont} and leakage resistors R_l are included into description, see Fig. 7.1. Algorithm is implemented in Maple SW and achieve results are compared with the full transistor-level properties of the charge pump, which are simulated in professional design environment ELDO. *The main*

benefit is the development of step-by step synthesis procedure by using known relationships without the necessity to use computationally demanding iteration processes.

7.1 State model of the system

Generally, the classical control theory and methods that are used to simple input-output description of the plant can not be applied in this case. The reasons are based on the non-linear nature of the circuit, which handles discrete values–discontinuity of the inner states in time. But considering the selected time interval defined by the valid logic levels of the clock signals, the circuit may be described as *multidimensional continuous nonlinear dynamic system* [45]. The internal description leads to the state model of the system [46], block diagram is shown in Fig. 7.2. Each of the i-pump stage represents

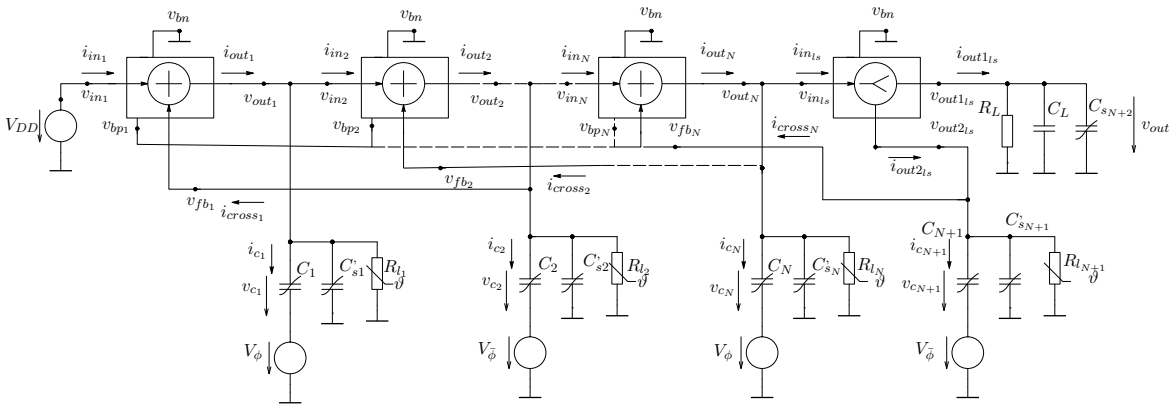


Figure 7.2: Block diagram of the N-stage cross-coupled charge pump

block, where the output current i_{out_i} is given by the sum of the input and cross inverter current, $i_{out_i} = i_{in_i} + i_{cross_i}$, and the block of the last stage splits the input current $i_{in_{ls}}$ into load current and current, whose part charges the last main capacitor C_{N+1}, then $i_{in_{ls}} = i_{out1_{ls}} + i_{out2_{ls}}$.Capacitors C'_{s1}, $C'_{s2} \ldots C'_{sN+2}$ represent total substrate capacitances of the i-pump stage. Each of them is given by the part of the its pump strange capacitance (dynamic part of the model) and added strange capacitance (linear) C_{mont}. After that,

$$C'_{si} = C_{si} + C_{mont}. \tag{7.1}$$

The dynamics of the *state-space* system refers to *state variables represent by the voltage on the capacitors*, that fully describe the system at time $\langle 0, T_{clk}/2\rangle$ and its response to any given set of inputs. Asuming the constant clock signal amplitude, the number of state variables with knowledge of those variables at initial time $t_0 \in \langle 0, T_{clk}/2\rangle$ is equal to number of main capacitors because the time-varying component of the voltage v_{C_i} is the only one on the parasitic capacitor. In the other words $\dot{v}_{C_s} = \dot{v}_{C_i} + \dot{v}_{clk} = \dot{v}_{C_i}$ for valid logic levels. In the standard form, the mathematical description expressed as a set of N+2

(including load capacitance C_L) coupled first-order ordinary differential equations,

$$\begin{aligned}
\dot{v}_{C_1} =& \frac{1}{C_1 + C_{s_1}^{'}} \left[i_{in_1} - i_{in_2} + i_{cross_1} - \frac{v_{C_1} + V_{clk}}{R_{l_1}} \right] \\
\dot{v}_{C_2} =& \frac{1}{C_2 + C_{s_2}^{'}} \left[i_{in_2} - i_{in_3} + i_{cross_2} - \frac{v_{C_2} + V_{clk}}{R_{l_2}} \right] \\
& \vdots \\
\dot{v}_{C_i} =& \frac{1}{C_i + C_{s_i}^{'}} \left[i_{in_i} - i_{in_{i+1}} + i_{cross_i} - \frac{v_{C_i} + V_{clk}}{R_{l_i}} \right] \\
& \vdots \\
\dot{v}_{C_N} =& \frac{1}{C_N + C_{s_N}^{'}} \left[i_{in_N} - i_{in_{ls}} + i_{cross_N} \right] - \frac{1}{C_N + C_{s_N}^{'}} \frac{v_{C_N} + V_{clk}}{R_{l_N}} \\
\dot{v}_{C_{N+1}} =& \frac{1}{C_N + C_{s_{N+1}}^{'}} \left[i_{out2_{ls}} - i_{cross_N} \right] - \frac{1}{C_N + C_{s_{N+1}}^{'}} \frac{v_{C_{N+1}} + V_{clk}}{R_{l_{N+1}}} \\
\dot{v}_{out} =& \frac{1}{C_L} \left[i_{out1_{ls}} - \frac{v_{out}}{R_L} \right]
\end{aligned} \tag{7.2}$$

where $\dot{v} = \mathrm{d}v/\mathrm{d}t$. and each of the functions i_{in_i}, i_{cross_i}, $i_{out1_{ls}}$, $i_{out2_{ls}}$ is nonlinear time-varying function of the nodes voltages v_{C_i}, the system inputs (transistos sizing, power supply, etc.) and time.

7.2 The basic principle of the algorithm

The state model is the core of the analysis algorithm despite its limitations that is mentioned in the previous text. The philosophy of the following approach that allow to estimate static a dynamic charge pump parameters is based on idea of the *quasi-analog system*. Block structure of the N-stage charge pump (Fig. 7.2), is described as analog circuit in each phase of the clock signal, while the transition into next phase is characterized by the discrete changes of some input variables (clock signal). The influence of the rising and falling edges of the clock signal is not considered. The new state is dependent on the new input variable but also on the previous state, i.e. recurrent expression. Algorithm diagram is shown in Fig. 7.3. Reffering to the input parameters (number of stages,clock frequency,...), program procedure automatically generates set of the paremetric *state equations* according to (7.2) for the actual cycle, labeled $k+1$, where $k = \{1,2,...,n\}$. A set of initial conditions and parameters are determined by the *end values* of state variables from the k-cycle and the amplitude of the clock signal:

$$V_\phi = \begin{cases} 0, & \text{for odd } k \\ V_{DD} & \text{for even } k. \end{cases} \tag{7.3}$$

Zero intial conditions are set in the first cycle that corresponds to the half of the period of the clock signal. It is very important point due to solution convergence. After

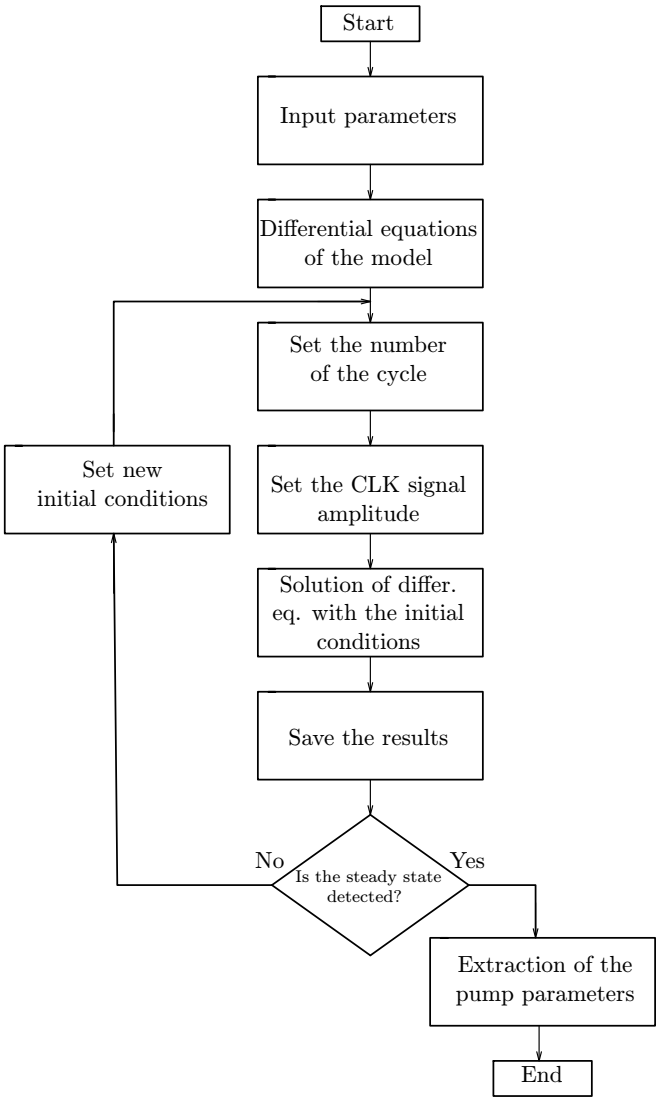


Figure 7.3: Charge pump analysis algorithm

initialization, the time response characteristics $v_{C_i}(t)$ and $v_{out}(t)$ are computed at time interval

$$t \in \left\langle (k-1)\frac{T_{clk}}{2}, k\frac{T_{clk}}{2} \right\rangle .$$

In general form, the inital condition of each of the state variables, labeled $v_{C_{i_0}}^{(k+1)}$,$v_{out_0}^{(k+1)}$, in the next cycle is determined as

$$v_{C_{i_0}}^{(k+1)} = \mathrm{sgn}_{V_{DD}} V_{DD} \cdot \frac{C_{si}^{\prime(k+1)}(v)}{C^{(k+1)}(v) + C_{si}^{\prime(k+1)}(v)} + v_{C_i}^{(k)}|_{t=k\cdot T_{clk}/2}, \tag{7.4}$$

$$v_{out_0}^{(k+1)} = v_{out}^{(k)}|_{t=k\cdot T_{clk}/2}, \tag{7.5}$$

where $t \in \left\langle k\frac{T_{clk}}{2}, (k+1)\frac{T_{clk}}{2}\right\rangle$, factor $\mathrm{sgn}_{V_{DD}}$ provides sign of the clock signal amplitude:

$$\mathrm{sgn}_{V_{DD}} = \begin{cases} +1, & \text{for the passive interval of CLK} \\ -1, & \text{for the active interval of CLK.} \end{cases}$$

If the nonlinear-capacitors are used, then its capacitance will be jump changed at the beginning of the next phase. $C_{(s)i}^{,(k+1)}(v)$ labels instante capacitance value at bias voltages, which correspond to the voltage values from k-cycle and this state variable value at the time $kT_{clk}/2$ increased by the clock voltage level V_ϕ, $V_{\bar{\phi}}$ of the actual voltage level,

$$C_{(s)i}^{,(k+1)}(v) = \begin{cases} C_{(s)i}^{,(k)}\big|_{v,\, v_{ci}^{(k)}+\max\{V_\phi, V_{\bar{\phi}}\}}, & \text{for active interval} \\ C_{(s)i}^{,(k)}\big|_{v,\, v_{ci}^{(k)}+\min\{V_\phi, V_{\bar{\phi}}\}}, & \text{for passive interval.} \end{cases} \tag{7.6}$$

When one of the M_d transistors becomes from strong inversion region to subthreshold region (considering $I_D = 0$ in the model) during the active interval of CLK while the switch transistor is OFF, then the end value at $kT_{clk}/2$ is corrected according to equation

$$v_{C_{i_0}}^{(k+1)\prime} = v_{C_{i_0}}^{(k+1)} + |V_{OFF}|\,, \tag{7.7}$$

where V_{OFF} is cut-off voltage. The same correction is applied, if the bias voltage of the switch transistor $v_{DS} = v_{GS}$.

After the compution of the new state variables, all the mentioned steps are repeated. As a result, dynamic behavior of the system within the interval $t \in \langle 0, k \cdot T_{clk}/2\rangle$ is obtained by composing partial response characteristics in the appropriate scale. Computional procedure runs until the the output voltage $v_{out}(t)$ achieves the steady state. It means that average value of the output voltage is practically constant over time. Steady

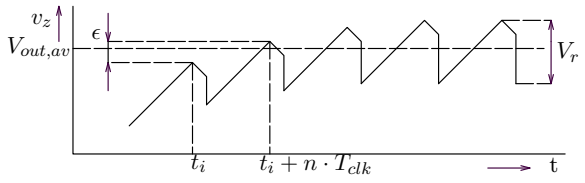


Figure 7.4: Time response characteristics of the pump output voltage

state is simply indicated by comparing two arbitrary values that are temporarily shifted by just one period of the clock signal (see Fig. 7.4). Consequently,

$$v_{out}(t_i + T_{clk}) - v_{out}(t_i) < \epsilon, \tag{7.8}$$

where parameter ϵ should be chosen with regard to the numerical calculation accuracy, for example $\epsilon = 1\,\mathrm{mV}$.

7.3 Experimental part

The computational algorithm has been programmed in Maple SW according to the structure that is shown in Fig. 7.2. The influence of the parasitic capacitances C_{s_i} and shunt resistances R_{l_i} is taken into account. All the simulations parameters are given in Tab. 7.1.

Table 7.1: Simulation parameters

Parameter		**Value**
Temperature	ϑ	24° C
Supply voltage	V_{DD}	1V
Clock frequency	f_c	10 MHz
Main capacitance	C_i	5 pF
Parasitic capacitance	C_{mont}	0.6 pF
Shunt resistance	R_l	$10^7\,\Omega$
Load ressistance	R_L	100 k
Load capacitance	C_L	10 pF
Threshold voltage of	V_{TH0_N}	0.35 V
NMOS and PMOS at V=0	$\lvert V_{TH0_P}\rvert$	0.33 V
Channel length of N(P)MOS	L	1μm
Channel width of the M_{Si}	W_s	$2\,\mu$m
M_{Pi}	W_p	$20\,\mu$m
M_{Ni}	W_n	$9\,\mu$m
M_{Di}	W_d	$10\,\mu$m

Under condition (7.8), the values of the system state variables can be used used to calculate other significant parameters, as power consumption, etc. In addition, procedure checks correct function of the circuit (open loop of feedback is a typical problem for this topology), operation mode of each of the transistors and exceeding the limit parameters ($V_{DS_{max}}$, $V_{GS_{max}}$, etc.).

Total number of cycles, labeled n, when the output voltage v_{out} starts from the initial value to the final value in steady state is approximately equal to *Rise time* T_r,

$$T_r \approx \frac{n}{2} T_{clk}|_{k=n}. \tag{7.9}$$

The voltage trend over time $v_{out}(t)$ is actually difficult to describe, because it is influenced by many dynamic effects in circuit, as capacitive couplings between stages and charge injection. An example of time response characteristic is shown in the Fig. 8.5.

Average value $V_{out,av}$ of the output voltage is estimated as the average value of the minimum and maximum values instead of the numerical integration of $v_{out}(t)$ in steady state,

$$V_{out,av} \doteq \frac{v|_{t=k\cdot T_{clk}/2} + v|_{t=(k+1)\cdot T_{clk}/2}}{2}, \tag{7.10}$$

where k is close to n. The output ripple voltage, labeled V_r, is given by the difference of

the maximal and minimal values,

$$V_r = |v_i - v_{ii}| \text{ for } k \to n, \tag{7.11}$$

where $v_i = v|_{t=k\cdot T_{clk}/2}$ and $v_{ii} = v|_{t=(k+1)\cdot T_{clk}/2}$. Static and dynamic characteristics were compared with values that have been analyzed by the professional simulator ELDO including SPICE-level models of the components (library MGC Design Kit). Some results are summarized in the following table, including relative average output voltage error $\epsilon_{V_{out}}$. Naturally, the computional time increases with the number of circuit nodes, which

Table 7.2: Simulation results

$\epsilon = 1\,\mathrm{mV}$	Calculation	ELDO	
N [-]	n [-]	$V_{out,av}$ [V]	$V_{out,av}$ [V]	$\epsilon_{V_{out}}$ [%]
1	33	1.12	1.10	1.8
2	59	1.61	1.53	5.2
3	87	2.02	1.93	4.6
4	109	2.16	2.18	0.91
5	163	2.53	2.48	2
6	202	2.61	2.67	2.2
7	207	2.57	2.47	4

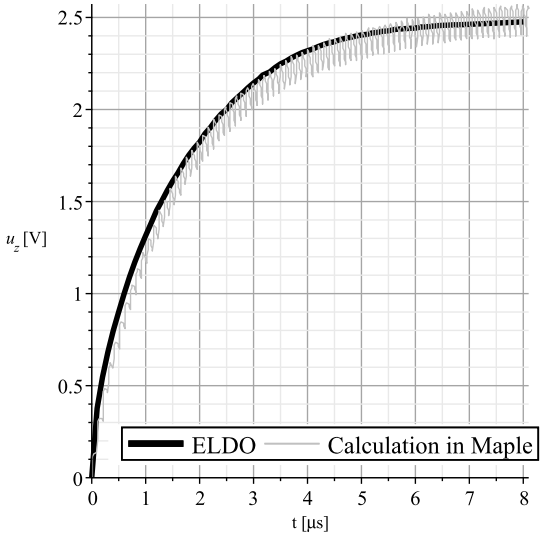


Figure 7.5: Time response characteristic of the five-stage pump output voltage

is associated with the number of pump stages. However, total cycle count is a crucial indicator of computational difficulty. The growth trend, as it is shown in Fig. 7.6, is limited by the *pump efficiency*.

7.4 Summary

The analysis algorithm for estimation of static and dynamic parameters of the cross-coupled charge pump was discussed in this chapter. The principle is based on the state model analyzing circuit behavior at each phase of the clock signal. The block structure was built from the subcircuits, which include dominant effects via the BSIM model equations. N-stage charge pump structure is described by the N+2 first-order differential equations.

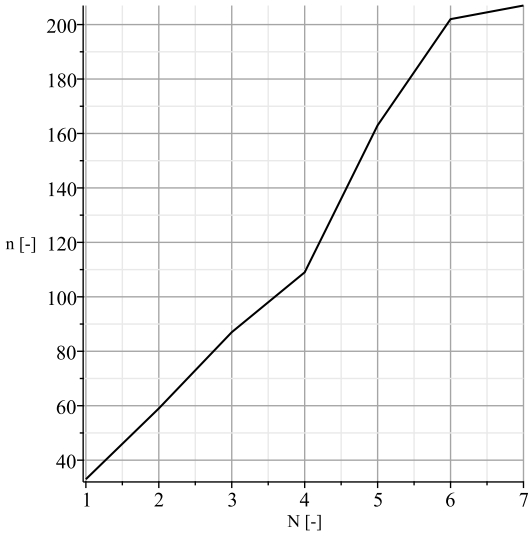


Figure 7.6: Number of cycles vs number of stages

Total response characteristics of the output voltage is obtained through the composition of partial responses for each phase of CLK with initial conditions. This method is very accurate because the transistor-level properties can be arbitrarily included in the sub-blocks description, unlike the "digital circuit perception". Furthermore, the knowledge of the state variables allows to estimate many other parameters, for example, static efficiency. On the contrary, the disadvantage is the need to use a recurrent description associated with the total number of cycles. Computational difficulty is derived from the complexity of the circuit topology and pumping efficiency (voltage increase) in time, see Fig. 7.6.

Chapter 8

Charge pump design on the circuit-level HW realization

Design utility for the cross-coupled charge pump is presented in this chapter. Synthesis process includes the design of the pump functional blocks and application of the pump stage complex model for estimation of the number of pump stages via state-space model description. in algorithm. One of the main reason for its use is still an unknown relationship between number of stages and pump output voltage [35, 38], $V_{out,av} = \mathrm{f}(N)$, which would consist properties of the real structure. Access is designed to stress the maximum pump voltage efficiency. The whole procedure is summarized in practical example with the evaluation of the achieved results and comparision with simulation results of the real structure in professional simulator. The solution is shown both in terms of *maximal voltage efficiency* and the *optimal pump area* on chip.

8.1 Synthesis process

The charge pump draft is divided into two basic steps, as the outcome of the current research on the issue: *Design of the partial pump blocks* and *finding number of the pump stages* at the input requirements. As in other circuits, the procedude also start by evaluating of the input requirements to the circuit and setting the limit values for given technology process. This includes, in particular, maximal bias voltage and current values $\{V_{DS_max}, V_{GS_{max}}\}$ and permissible range of the technolgy parameters and their dispersion $(L(W)_{min}\, L(W)_{max}$, etc.). Sizing of the components (MOSFETs sizing, main capacitor value, etc.) is interrelated and consequences of these settings was evidenced in Chapter 6. Recommended sequence of individual blocks design is shown in Fig. 8.1. The algorithm that finds the pump number of stages N represents the computationally the most demanding part of the complete procedure, see Fig. 8.2. It consists of three basic steps:

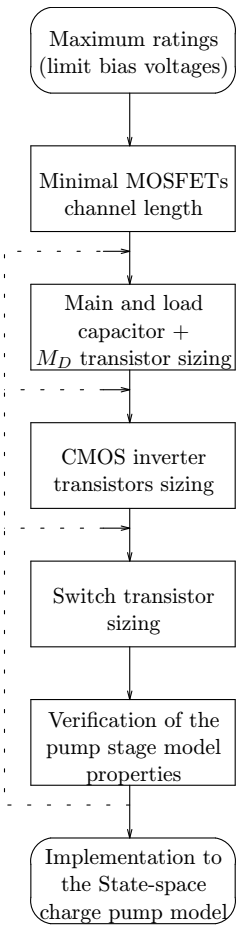


Figure 8.1: The hierarchy of the pump functional blocks design procedure

- generating of the state equations of charge pump model having $\hat{N}$ stages,
- calculation of the time response characteristics $v_{out}(t)$,
- evaluation of the results and estimation of the new pump stages $\hat{N}_{i+1}$.

The initial number of stages is set based on the input parameter values–*output voltage and load current, ripple voltage and clock signal frequency* for analysis algorithm via to **state-space model**. The following equation comes from the theoretical relationship 3.2, which is modified for the BSIM model:

$$\hat{N}_{i_0} = \text{round}\left(\frac{R_L C f_{clk} \chi \varphi \rho}{2C^2 R_L V_{DD} f_{clk} - 2V_{out,av}\left(C + C_{mont}\right)}\right), \quad \text{for } C_{si} \gg C_{mont}, \tag{8.1}$$

where

$$\chi = \left(C + C_{mont}\right)\left(K_{1ox}\sqrt{4\phi_s + 2V_{rmax}} - 2K_1\sqrt{\phi_s}\right),$$
$$\varphi = C\left(K_{2ox}V_{rmax} + 2V_{out,av} - 2V_{DD} + 2V_{TH0}\right),$$
$$\rho = C_{mont}\left(K_{2ox}V_{rmax} + 2V_{out,av} + 2V_{TH0}\right),$$

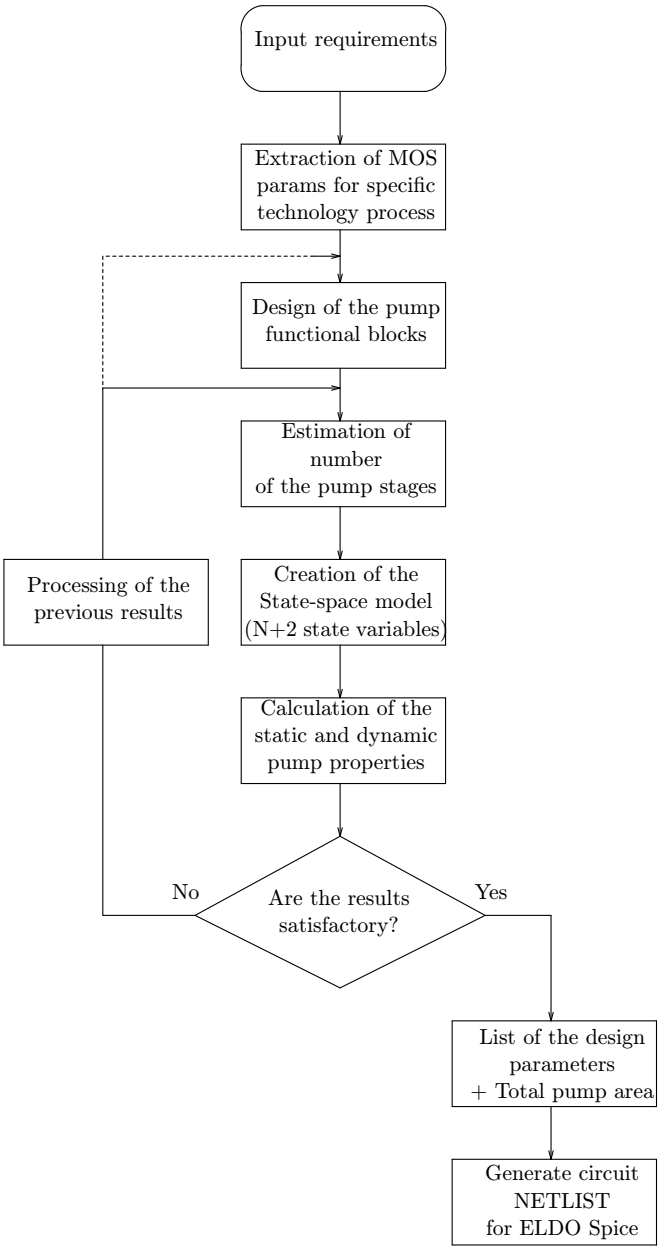


Figure 8.2: Basic principle of the charge pump synthesis algorithm

where R_L is load resistance, C is main capacitor and C_{mont} is added strange capacitor value (see Fig. 7.1), f_{clk} is clock signal, V_{DD} is power supply voltage, $V_{out,av}$ is average value of the output voltage, V_{rmax} is ripple of the output voltage and V_{TH0} is threshold voltage of NMOS at zero bias voltages, ϕ_s is surface potential and K_1, K_{1ox}, K_{2ox} are body effect coefficients [27].

Equation 8.1 does not provide the correct result in the vast majority of cases, the reasons of this are explained in detail in [35, 36, 38], thus in real $N > \hat{N}_{i_0}$. In the next step, the procedure automatically generate set of the first order differential equations with initial conditions, which describe the behaviour of the N_i-pump stage model for each phase (ϕ,$\bar{\phi}$) of the clock signal (analogue domain). Philosophy of the analysis part including an estimation of some static and dynamic characteristics is listed in Chapter 7. Calculation

of the state variables, which also include output voltage, is similar to the principle of *state machine*. The process is ended in the steady state, this is detected mainly based on:

- trend of the pump voltage gain in time, see Chapter 7, $G_v = f(t)$,
- evaluating of the previous time response characteristics v_{out}^j (if they have already been implemented), where j labels the rank of the calculated time response char.,
- trend of the calculated average output voltage V_{out}^j, $V_{out}^{j-1} \ldots$, V_{out}^1, with N,

Providing the output voltage V_{out_i} does not reach the required level $V_{out,av}$, the number of the stage for next iteration, labelled $\hat{N}_{i+1}$, is estimated from *Lagrange´s polynomial function* and the procedure is repeated.

Example:
Considering the set of the parameters N and output voltage $V_{out}(< V_{out,av})$ after two N-iterations $[N_i,V_{out_i}]$, $\left[N_{i+1},V_{out_{i+1}}\right]$. The number of stages N_{i+2} for next cycle is calculated from:

$$N_{i+2} = \text{round}\left[\frac{N_i(V_{out_{i+1}} - V_{out,av}) - N_{i+1}(V_{out_i} - V_{out,av})}{V_{out_{i+1}} - V_{out_i}}\right]. \tag{8.2}$$

The first order polynom is sufficient for monotone functions $V_{out,av} = \text{f}(N)$, however with more iterations is better to use the interpolation of the multiple points for effective computional process.

8.2 Other properties of the design environment

Program procedure offers the user in the additional design features. Among other things, these include:

- **Monitoring of the correct function.** Algorithm checks the state of all the transistors during computing and reports that correct functionality of the circuit is not guaranteed. This can occur, for example, if the maximum number of the pump stages is exceeded (the task has no solution) or the output voltage decreases with the number of stages, etc.. Example is mentioned bellow.

  ```
  "N>20!  Solution was not found, try to change the input parameters."
  ```

- **Fast analysis.** Time response characteristic $v_{out}(t)$ is not computed until a steady state is detected but the cycle is ended, when the instantaneous value at the end of the passive interval exceeds the required voltage level.Moreover, the numerical

accuracy is reduced, so that the calculation is accelerated. This configuration does not allow to estimate all the pump parameters.

- **Selection of the circuit and parasitic elements.** The user can set the value of strange capacitances, labeled C_{mont}, and leakage resistances R_l in the pump stages. In addition, it is possible to select linear or MOSFET capacitors. Other types of the capacitors have not been implemented yet. For a big enough main capacitance values, programme automatically or manually by user deactivates the dynamic part of the model.

- **Netlist and pump area estimation.** When the synthesis process is ended, the list of design parameters is displayed and system generates a circuit netlist with calculated elements values for ELDO Spice. This will make it easier for designers. Total pump area on the chip is estimated from the sum of the partial components area and area, which is reserved for routing (from practical design, it is about 30% of the total circuit area),

$$\boxed{S_{pump} = 1.3\left[N(W_nL_n + W_pL_p + W_sL_s)\right] + 1.3\left[(N+2)(W_dL_d) + (N+1)W_cL_c\right],} \tag{8.3}$$

where W_c, L_c are MOS capacitor sizes.

8.3 Experimental part

The following application of voltage converter can be used as a secondary power block which increases the clock signal amplitude of the main charge pump. It greatly improves the voltage efficiency of the main pump that operates at the low supply voltage. Input requirements are listed in Tab. 8.1. The topology consists of MOS capacitors, added

Table 8.1: List of the input pump requirements.

Output voltage	$V_{out,av}$	$\geq 3.3\,\mathrm{V}$
Output load current (max.)	I_{Lmax}	$\leq 0.6\,\mu\mathrm{A}$
Maximal outptut ripple voltage	$V_{r_{max}}$	$\leq 2\,\mathrm{mV}$
Power supply voltage	V_{DD}	$0.8\,\mathrm{V}$
Clock signal amplitude	V_ϕ	$0.8\,\mathrm{V}$
Clock signal frequency	f_{clk}	$10\,\mathrm{MHz}$

parasitic impedance in the nodes are not considered. The step involving the pump block design in according to hierarchy from Fig. 8.2 will be skipped through the Chapter 6. Initial value of N in according to Eq. 8.1 is set to $N_{i0} = 3$, this corresponds to the calculated output voltage of $2.44\,\mathrm{V}$ in steady state. Figure 8.4 shows that to achieve voltage level $3.3\,\mathrm{V}$ three iterations of N are performed

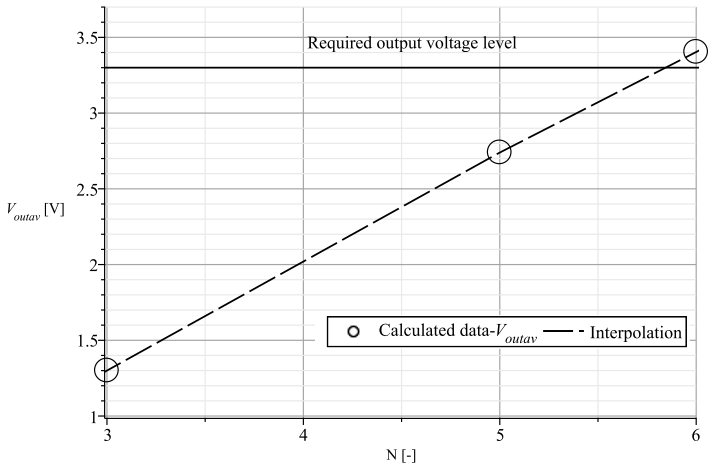


Figure 8.3: Interpolation of the calculated output voltages with the number of stages

Output voltage function of N is described by the following equation:

$$\hat{V}_{out,av}(N) \approx \begin{cases} 0.15N + 1.99, & \text{for } 3 \leq N \leq 5, \\ 0.56N, & \text{for } N \geq 6, \end{cases} \tag{8.4}$$

where N is the integer. An illustration of the programme report is listed below. Finally,

```
Number of N iterations: 3
Total number of stages is N=6.
Average value of the pump output voltage: Voutav=3.4039 V.
Ripple value of the pump output voltage: 1.8 mV.
Relative error of the output voltage: 3.15 percent.
Rise time of the output voltage: Tr = 7.15 us.
```

Figure 8.4: Report if the results in Maple software

statement of the draft results is shown in Tab. 8.2

Calculated time response characteristics of the six-stage charge pump output voltage compared to simulation results in ELDO is shown in Fig. 8.5.

Production cost minimization is an important part of the proposal in practice. It means the voltage gain may not be decisive from an economic point of view. The charge pump final version is most often designed to *minimize the area on a chip* (layout topology, the circuit parameters). The main capacitor C always represents the circuit element with the largest area in comparison with others elements in the pump stage, as it follows from Tab. 8.2,. Decreasing the main capacitor means that the pump must have more stages to achieve the same output voltage level. However, increasing of the number of the pump stages does not always mean that output voltage will grow to the desired value (task does not have a solution in extreme case). The algorithm in Fig. 8.6 is designed to find a relationship between the number of stages and main capacitor value so that the pump state area is minimal and the pump losses (switch reverse current and inverter cross current) in each of the pump stages were at the lower limit. Procedure in Fig. 8.6 starts

Table 8.2: List of the charge pump parameters.

Conditions		
Temperature	ϑ	22 °C
Model of MOSFETs M_d, M_s, M_n: *nmos_hvt*		
Model of MOSFETs M_p: *pmos_hvt*		
Model of MOSFETs M_c: *nmos_nat*		
MOS corner analysis: *Typical*		
Design parameters		
Number of stages	N	6
Main capacitor value	C	6.5 pF
MOSFETs sizing		
Channel length of M_D,M_s, M_p, M_n	L	1 µm
Width of M_d: nmos_ hvt	W_{Md}	31.5 µm
Width of M_s: nmos_ hvt	W_{Ms}	0.6 µm
Width of M_p: pmos_ hvt	W_{Mp}	1 µm
Width of M_n: nmos_ hvt	W_{Mn}	11 µm
MOS capacitor sizing - nmos_ nat		
Channel length	L_c	14 µm
Channel width	W_c	137 µm
Pump stage area	S_{stage}	1963.1 µm^2
Total pump area on layout (est.)	S_{pump}	0.018 mm^2
Estimation of static and dynamic parameters		
Output voltage (avg.)	$\hat{V}_{out,av}$	3.199 V
Output ripple peak voltage	$\hat{V}_r$	1.8 mV
Rise time [1]	$\hat{T}_r$	7.15 µs
Static voltage efficiency	$\hat{\eta}_v$	57 %

from solution for optimization of the pump voltage gain. Pump consists N_g number of stages and main capacitors value C_g. The procedure firstly selects pair W_i and $C_i < C_g$

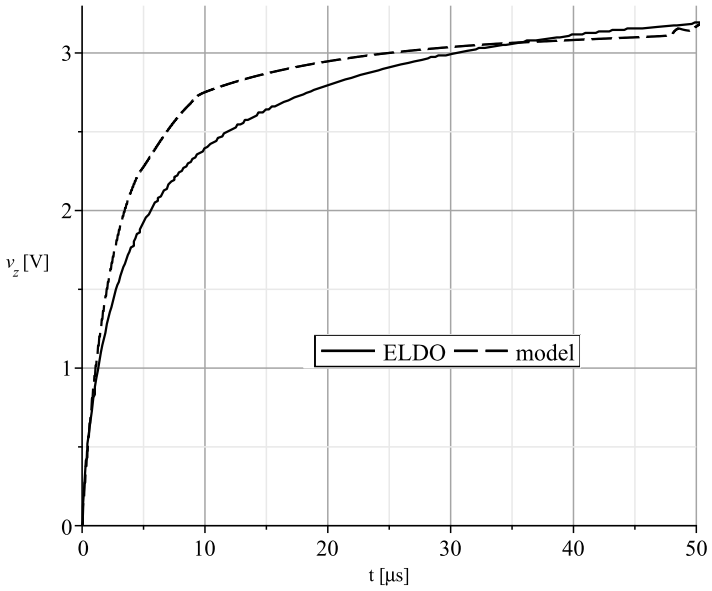


Figure 8.5: Time response characteristic of the six-stage pump output voltage

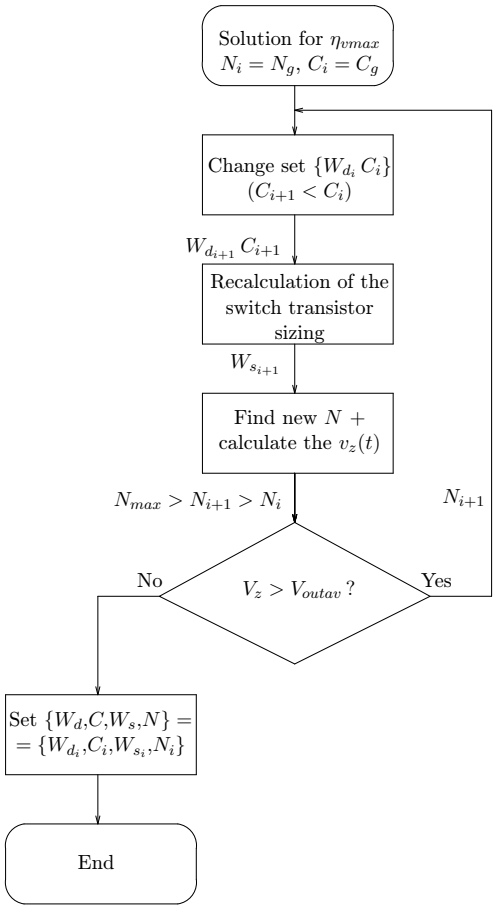


Figure 8.6: Algorithm for pump area optimization

from the solutions set of equations from chapter 6

$$v_c|_{t=T_{clk}/2} = \alpha_D \cdot v_{c_\infty}|_{V_\phi=0}, \tag{8.5}$$

$$v_{out}(W_{MD},C)|_{t=nT_{clk}/2} \geq V_{out,av} + V_r/2, \tag{8.6}$$

where the meaning of the symbols is explained in section 6.3 and subsequently recalculates the switch transistor sizing. After that, the analysis algorithm tries to find the new number of stages, labelled $N_i(> N_g)$, according to the procedure in section 8.6. If the solution exists, the new pair $\{W_{di+1},C_{i+1}\}$ is selected and the process is repeated until the output voltage $\bar{V}_z$ is less than $V_{out,av}$. The number of stages is the critical parameter in this case. Considering the set of the input parameters from Tab. 8.1, possible pairs of solution Eq. 8.6–transistor width in μm and main capacitor value in pF are: $[W_d,C] = \{[1, 0.5], [4.5, 1.5], [10, 2.5], [15.5, 3.5], [21, 4.5], \dots\}$. The result in according to algorithm from Fig. 8.6 satysfying the conditions $\bar{V}_z > V_{out,av}$, $N < N_{max} = 20$ and minimal capacitance value is $\{W_{sopt,a} = 0.5, \mu m, W_{opt,a}\, C_{opt,a}\} = \{10, 2.5\,\text{pF}\}$ for $N = 14$. MOS capacitor sizing is $W_c = 72.1\,\mu m$ and $L_c = 10\,\mu m$. Sizing of the other components is the same, see Tab. 8.2.

Total charge pump area calculated from (8.3) is $0.0145\,mm^2$ *is about* **20** % *less than in*

the previous case, see Tab. 8.2. The pump voltage efficiency is only about **27** %.

8.4 Summary

The utility for the design of the cross-coupled charge pump was discussed in this section. Synthesis process, which is the result of the current research in the field of two-phase charge pumps, significantly facilitates designer's work. The algorithm is based on the pump elementary blocks modelling through the symbolic description by using the BSIM model description. Sizing of the pump components is derived from both the static (CMOS inverter) and state equations (switch transistor, main capacitor sizing, etc.) from and solving of the state equations, which meet the prerequisites following from continuous pump character during the phase of the clock signal. Subblocks were designed, so that the pump voltage static efficiency is maximal, see (3.3). Complex model is used for calculating the number of pump stages in the synthesis process through the state-space description, as it is shown in Fig. 8.2. The number of stages for computing cycle is estimated by using the *Lagrange´s* interpolation polynomial function, initial N was calculated from (8.1). The full mentioned process was shown in the practical example, in which the pump design was done based on both the maximal static efficiency and minimal total pump area. The procedure allows, among other functions, to generate *netlist for ELDO* and estimate the total pump area, see Eq. 8.3. Description approach is complicated and allows to observe a number of static and dynamic parameters with acceptable accuracy. On the other hand, some dynamic properties, as power dissipation cannot be calculated because of the neglecting of the transition between phases of CLK and other effects cited in [36,38]. Comparision between the calculated and analysis results in ELDO shows Fig. 8.5.

Chapter 9

Conclusion

9.1 Summary of thesis

Synthesis process of the cross-coupled charge pump is discussed in the thesis.

General systems theory defines the main properties and aspects associated with the proposal and problematic solution of the partial steps of the design algorithm. Conventional description methods fail to capture the real circuit behaviour, whose analogue character brings another dimension of the complexity. The non-traditional approach to an analysis of the discrete-time analogue circuit was offered to readers.

Attention was focused on the **cross-coupled charge pump**, that is used is used to the power of the low-current-consumption peripherals on the chip, as flash or EEPROM memories.

The modern topology of the two-phase charge pump is constructed primarily based on two conceptions, namely the Dickson charge pump and static charge pump (CTS-1), which were given in overview. Analysis results confirmed the discrepancy between the theory relationships and simulated data thus an alternative way was found for the successful draft. This topology partially eliminates the reverse charge transport through the switches but the problem remains– voltage gain is strongly dependent on the switch transistor sizing. Other dominant effects on the pump characteristics are *threshold voltage and body effect, inverter cross current, substrate capacitances, leakage current.*

The main pump properties were included in the pump stage model. Each of the pump functional blocks was described as an analogue block based on the BSIM model equations for long channel process and respecting to the various operating modes of the transistors. Only the subthreshold region of the MOSFETs is not included because the high-voltage application is provided. The main pump properties were included in the pump stage model. The resulting model is significantly closer to the real circuit behaviour, as it is shown in simulation results. The model allows both the design pump circuit elements and to carry out the synthesis of the N-stage charge pump. The pump functional blocks were designed so that the *pump voltage gain is maximal.* The process is based on previous

experience gained from analyzes in the simulator. The principle applies the calculation of the time response characteristics and finding the extrema points. The switch and diode transistor and main capacitor sizing are set in accordance with the guidelines. Because the system is nonlinear, the finding point must be defined in the worst case of the bias voltages to satisfy the solution over all the pump stages. The CMOS inverter transistor width was set in a different way then the other circuit elements. The simple principle was based on the static power minimization so that the inverter switching point was shifted to the cut-off border of the NMOS. As a consequence, the switch reverse current is also decreased. All the properties were verified by the simulation of the N-stage charge pump in Mentor Graphics SW.

Estimation of the pump static and some dynamic properties were done through the *state-space model*. The partial time response characteristics for each phase of the clock signal was calculated and transition into the next phase respects the end values of the state variables from the previous phase. Total time response characteristic from zero to time, in which the steady state is detected, is given by the composition of the partial time responses.

On the basis of a comprehensive description of each charge pump block, an algorithm for the design of cross-coupled charge pumps was developed. Synthesis process includes the pump block design through the *semi-symbolic equations* according to the recommended hierarchy. The core is the mentioned analysis procedure, which calculates the output voltage. Number of the pump stages is predicted using the *Lagrange´s interpolation function*. Complete procedure was demonstrated on the practical example, including the comparison to simulation results. Utility provides two significant solutions considering two design criteria: *maximal pump voltage efficiency* and *minimal pump area on a chip. The approach may be applicated for other technology MOS process, as PSP or EKV models.*

9.2 Fulfilments of targets

The thesis clarifies many real effects in the cross-coupled charge pump and their interrelations, which are described by the symbolic equations derivated from the elementary circuit models and their characteristics. The results solve the issue of the circuit design, which is time effective. The practical benefit of the thesis is the synthesis of the high-efficiency/ area-efficiency charge pump on the circuit-level. The design utility is complemented by additional functions. Firstly, the circuit netlist generation for ELDO at the end of the synthesis process. By this way the designer can easily check the results, make the further modifications, etc.. Secondly, the pump model allows to include the high-level parasitic effects: added strange capacitances and leakage currents in each pump stage.

9.3 Further extensibility and recommendations

The future research will be focused on the activities in the field of the design utility including these innovations: derivation of the refined equation for the initial pump stages, i.e. shortening the calculation time, implementation of the corner synthesis (FF, SS) and other technology process and graphical interface (guide, maplet). It would be appropriate to compare utility results with the results of the optimization algorithm in the simulator. The steps leading to the production of the functional samples highlight knowledge in the branch of the charge pumps.

Appendix A

Design utility–illustration

```
# Illustration of the settings in Maple SW
# The initial settings
Simulation settings:
Fast analysis:  NO
CAPMOD = 1            # MOS capacitor will be used
Minimal capacity value:  0.6pF            # Capacitance value at V = V_TH0
WARMOD = 1            # Ward's model will be activated
Initial number of stages:  3
- - - - - - - - - - - - - - - - - - - - - - - - - - -
Power supply voltage:  1V
Clock signal amplitude:  1V
Clock signal frequency:  10MHz
Load impedance:  10Mohms || 10pF
Added strange capacitance value:  0.001pF
Leakage resistance value:  10Mohms
Nominal output voltage value:  3V
Minimal value of the output voltage:  2.85V           # tolerance

# Computional process
N = 3           # Initial value of N
Computing, please wait...
3.6535 10e-13, 1.8087 10e-13, 3.5051 10e-13, 1.1231e-14, 10e-15 Strange Cs
-0.37911, 0.23261, -0.36942, 0.0035260, 0 # initial conditions
-0.37911, 0.23261, -0.62272, 0.074483, 0.015639 # end state variable values
1, 5.0000.10e-7, 0.015639 # cycle, time, output voltage
# next cycle
9.8971.10e-14, 1.0587 10e-13, 1.2278 10e-13, -7.58 10e-17, -0
-0.2367, 0.08143, -0.4516, 0.07294 0.015638617
```

```
0.52778, -0.62346, 0.37544, 0.072944, 0.015414
2, 1.0000e-7 , 0.015414
⋮
# Programme continous...
# List of the results
# Approximation of the output voltage
```

$$\begin{aligned} \mathrm{V}_{out} = & \texttt{piecewise}(0 <= t \texttt{ and } t <= 3, 0.87363 * t, 0) + \\ & + \texttt{piecewise}(3 <= t \texttt{ and } t <= 5, 0.2424 * t + 1.8936, 0) + \\ & + \texttt{piecewise}(5 <= t, 0.23132 * t + 1.9489, 0) \end{aligned}$$

```
Number of N iterations:  3
Total number is N=6
Average value of the output voltage:  Voutav=3.33V
Ripple value of the pump output voltage:  1.8 mV
Relative error of the output voltage:  0.9 %
Rise time of the output voltage:  Tr=5.4 us
Transistor Md:  NMOS HVT
W=20um
L=1um
 Switch transistor Ms:  NMOS HVT
W=2um
L=1um
 CMOS inverter
Transistor Mn:  NMOS HVT
W=9um
L=1um
 Transistor Mp:  PMOS HVT
W=10um
L=1um
 Capacitor Mc:  NMOS HVT
=80um
L=10um
 Component area:  6608 um^ 2.
Total pump area on layout (estimation):  8591 um^ 2.
```

Appendix B

Netlist for ELDO

Netlist is generated by the design utility for ELDO
Netlist(N); # call the procedure
1-stage charge pump. Very long netlist, isn´t that?

```
"* .CONNECT statements
*
.CONNECT GROUND 0
*ELDO netlist generated with ICnet
*
*GLOBALS
*
.global GROUND
*
*MAIN CELL: 1-stage Cross-coupled charge pump
*
V1 1 GROUND dc 1
Vclka clka GROUND PULSE (0 1 0 .10e-8 .10e-8 .50000e-7 .10000e-6)
Vclkb clkb GROUND PULSE (0 1 .49000e-7 .10e-8 .10e-8 .50000e-7 .10000e-6)
M1 1 1 2 GROUND nmos_ hvt w=.5e-5 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.5e-5*2.6e-07+(1-2)/2*(.5e-5*2.3e-07))/1):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((.5e-5*2.3e-07)/2):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.5e-5+2.6e-07)+(1-2)*(.5e-5+2.3e-07))/1):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1 ))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.5e-5+2.3e-07):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
M2 1 3 2 GROUND nmos_ hvt w=.2e-5 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.2e-5*2.6e-07+(1-2)/2*(.2e-5*2.3e-07))/1):
((.2e-5*2.6e-07+((1-1)*.2e-5*2.3e-07)/2)/1))}
```

```
+ ad={eval(((1/2-trunc(1/2))==0)?((.2e-5*2.3e-07)/2):
((.2e-5*2.6e-07+((1-1)*.2e-5*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.2e-5+2.6e-07)+(1-2)*(.2e-5+2.3e-07))/1):
((2*(.2e-5+2.6e-07)+(1-1)*(.2e-5+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.2e-5+2.3e-07):
((2*(.2e-5+26e-07)+(1-1)*(.2e-5+2.3e-07))/1))}
M3 3 2 1 GROUND nmos_ hvt w=.16e-4 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.16e-4*2.6e-07+(1-2)/2*(.16e-4*2.3e-07))/1):
((.16e-4*2.6e-07+((1-1)*.16e-4*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((.16e-4*2.3e-07)/2):
((.16e-4*2.6e-07+((1-1)*.16e-4*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.16e-4+2.6e-07)+(1-2)*(.16e-4+2.3e-07))/1):
((2*(.16e-4+2.6e-07)+(1-1)*(.16e-4+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.16e-4+2.3e-07):
((2*(.16e-4+2.6e-07)+(1-1)*(.16e-4+2.3e-07))/1))}
Mc1 2 clka 2 2 nmos_ hvt w=Wc l=Lc m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*Wc*2.6e-07+(1-2)/2*(Wc*2.3e-07))/1):
((Wc*2.6e-07+((1-1)*Wc*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((Wc*2.3e-07)/2):
((Wc*2.6e-07+((1-1)*Wc*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(Wc+2.6e-07)+(1-2)*(Wc+2.3e-07))/1):
((2*(Wc+2.6e-07)+(1-1)*(Wc+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(Wc+2.3e-07):
((2*(Wc+2.6e-07)+(1-1)*(Wc+2.3e-07))/1))}
Cs1 2 GROUND .1e-14
Rl1 2 GROUND .1e11
M4 3 2 vb vb pmos_ hvt w=.5e-5 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.5e-5*2.6e-07+(1-2)/2*(.5e-5*2.3e-07))/1):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((.5e-5*2.3e-07)/2):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.5e-5+2.6e-07)+(1-2)*(.5e-5+2.3e-07))/1):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.5e-5+2.3e-07):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
M5 2 2 out GROUND nmos_ hvt w=.5e-5 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.5e-5*2.6e-07+(1-2)/2*(.5e-5*2.3e-07))/1):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((.5e-5*2.3e-07)/2):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.5e-5+2.6e-07)+(1-2)*(.5e-5+2.3e-07))/1):
```

```
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.5e-5+2.3e-07):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
M6 2 2 vb GROUND nmos_ hvt w=.5e-5 l=.1e-5 m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*.5e-5*2.6e-07+(1-2)/2*(.5e-5*2.3e-07))/1):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((.5e-5*2.3e-07)/2):
((.5e-5*2.6e-07+((1-1)*.5e-5*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(.5e-5+2.6e-07)+(1-2)*(.5e-5+2.3e-07))/1):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(.5e-5+2.3e-07):
((2*(.5e-5+2.6e-07)+(1-1)*(.5e-5+2.3e-07))/1))}
Mc2 vb clkb vb vb nmos_ hvt w=Wc l=Lc m=1
+ as={eval(((1/2-trunc(1/2))==0)?((2*Wc*2.6e-07+(1-2)/2*(Wc*2.3e-07))/1):
((Wc*2.6e-07+((1-1)*Wc*2.3e-07)/2)/1))}
+ ad={eval(((1/2-trunc(1/2))==0)?((Wc*2.3e-07)/2):
((Wc*2.6e-07+((1-1)*Wc*2.3e-07)/2)/1))}
+ ps={eval(((1/2-trunc(1/2))==0)?((4*(Wc+2.6e-07)+(1-2)*(Wc+2.3e-07))/1):
((2*(Wc+2.6e-07)+(1-1)*(Wc+2.3e-07))/1))}
+ pd={eval(((1/2-trunc(1/2))==0)?(Wc+2.3e-07):
((2*(Wc+2.6e-07)+(1-1)*(Wc+2.3e-07))/1))}
Cs2 vb GROUND .1e-14
Rl2 vb GROUND .1e11
RL out GROUND .1e8
CL out GROUND .10e-10
.end"
```

Appendix C

Charge pump–logo

The design problem and the interconnection of the pump parameters is illustrated by the spider net. Optimal design is indicated by the regularity of its shape.

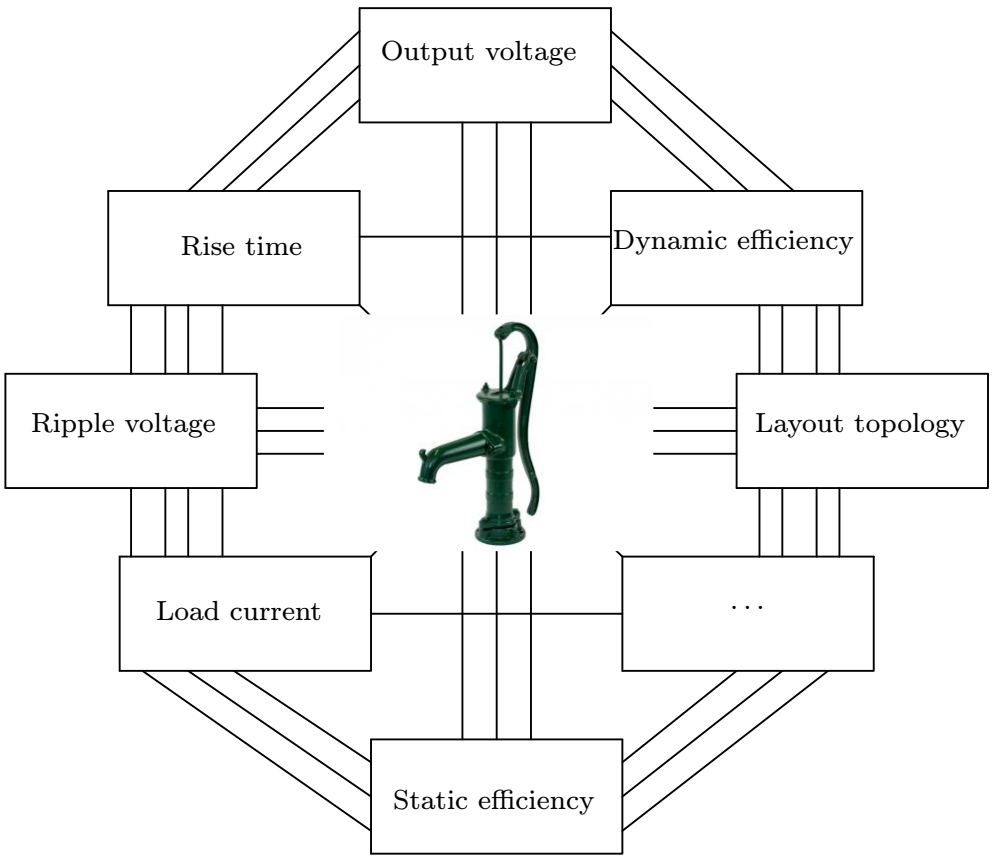
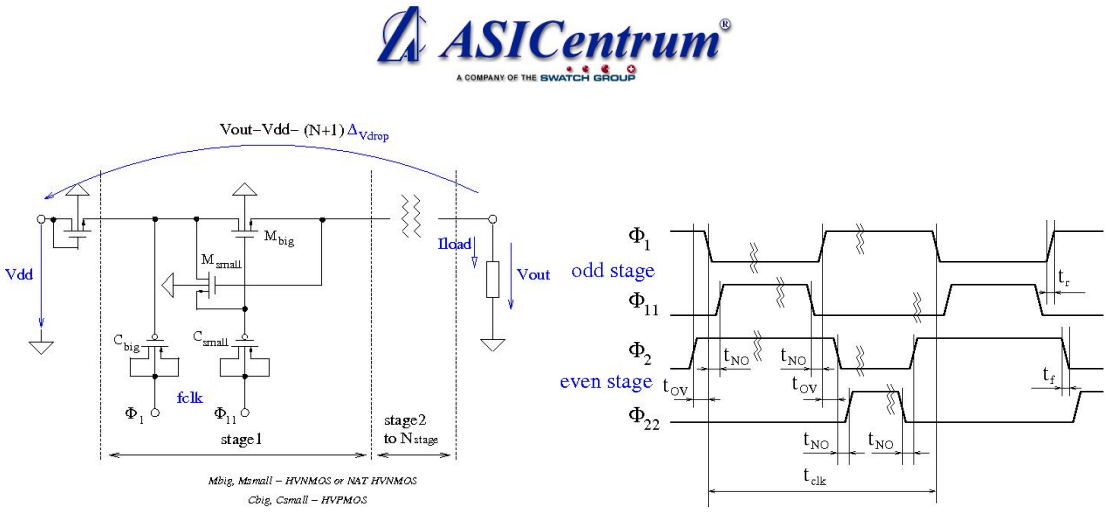


Figure C.1: Charge pump in spider net

Appendix D

Design maplet for 4-phase charge pump

The synthesis procedure for 4-phase charge pump draft had been programmed before the procedure for cross-coupled charge pump. The interactive application was created by **Ondřej Šubrt** for the needs of ASICentrum company, where he works as Senior IC Designer engineer. The synthesis algorithm is based on the on a simpler principle, than it is specified in the thesis. Nevertheless, the author applies practical knowledge from measurement of the real structure. Excerpts from the design environment *chpump_ interactive_ school_ 1.0*, programmed in Maple SW, are listed below.



(a) (b)

Figure D.1: 4-phase charge pump: diagram (a) and timming of the CLK (b)

Bibliography

[1] TANZAWA, T. A.. Behavior model of a Dickson charge pump circuit for designing a multiple charge pump system distributed in LSIs. *IEEE Circuits and Systems II: Express Briefs*. 2010, Vol. 57, iss. 7 pp. 527-530. ISSN 1549-7747. DOI 10.1109/TCSII.2010.2048482.

[2] TANZAWA, T. and T. TANAKA. A dynamic analysis of the Dickson charge pump circuit. *IEEE Journal of solid-state circuits*. 1997, vol. 32, iss. 8, pp. 1231-1240. ISSN 0018-9200. DOI 10.1109/4.604079

[3] WONG, Yan Ch. and et al. An evaluation of 2-phase charge pump topologies with charge transfer switches for green mobile technology. *IEEE Industrial Electronics*. 2011, vol. 32, pp. 136-140. ISBN 978-1-4244-9312-8. DOI 10.1109/ISIE.2011.5984146.

[4] ZHANG, M. and N. LLASER. A dynamic analysis of the Dickson charge pump circuits with a resistive load. *IEEE Electronics, Circuits and Systems*. 2003, vol. 2, iss. 8, pp. 431–434. ISBN 0-7803-8163-7. DOI 10.1109/ICECS.2003.1301814.

[5] ZHANG, M. and N. LLASER. Optimization design of the Dickson charge pump circuit with a resistive load. *IEEE Circuits and Systems*. 2004, vol. 5, pp. 840–843. ISBN 0-7803-8251-X. DOI 10.1109/ISCAS.2004.1329939.

[6] KURTH, C. F., MOSCHYTZ, G.S. Nodal analysis of switched-capacitor networks. *IEEE Transaction on Circuits and Systems*. 1979, vol. CAS/26, No. 2, pp. 93-104. ISSN 0098-4094. DOI 10.1109/TCS.1979.1084613.

[7] BAKER, R. *CMOS: mixed signal circuit design*. 2nd ed. Hoboken, N.J.: Wiley, c2009. ISBN 0470290269.

[8] MOHAN ANANDA, P. V. , V. RAMACHANDRAN, M. N. S. SWAMY. *Switched capacitor lters–theory, analysis and design*. Prentice Hall International, 1995, ISBN 0-13-879818-4.

[9] TOUMAZOU, C., J.B. HUGHES and N.C. BATTERSBY. *Switched-currents an analogue technique for digital technology*. Stevenage: IEE, 1993. ISBN 0-86341-294-7.

[10] CHEEK, B. J., N. STUTZKE et al.. Investigation of circuit-level oxide degradation and its effect on CMOS inverter operation and MOSFET characteristics. *Reliability Physics Symposium Proceedings*. 2004, pp. 110-116. ISBN 0-7803-8315-X. DOI 10.1109/RELPHY.2004.1315309.

[11] HAFED, M., M. OULMANEO and N. C. RUMIN. Delay and current estimation in a CMOS inverter with an RC load. *Computer-Aided Design of Integrated Circuits and Systems*. 2001, vol. 20, iss. 1, 2001, pp. 80-89. ISSN 0278-0070. DOI 10.1109/43.905677.

[12] MARRANGHELLO, F.S., A.I. REIS and R.P. RIBAS. CMOS inverter delay model based on DC transfer curve for slow input. *Quality Electronic Design (ISQED)*. 2013, pp. 651-657. ISBN 978-1-4673-4953-6. DOI 10.1109/ISQED.2013.6523679.

[13] MATSUMOTO, K., T. HIROSE et al..Switching-voltage detection and compensation circuits for ultra-low-voltage CMOS inverters. *Circuits and Systems. MWSCAS '09. 52nd IEEE International Midwest Symposium on.* 2009, pp. 483-486. ISBN 978-1-4244-4479-3. DOI 10.1109/MWSCAS.2009.5236051.

[14] CHAKRABORTY, A.S., M. CHANDA and C.K. SARKAR. Analysis of noise margin of CMOS inverter in sub-threshold regime. *Engineering and Systems (SCES).* 2013, p. 1–5. ISBN 978-1-4673-5630-5. DOI 10.1109/SCES.2013.6547499.

[15] CHOURANI, P., I. MESSARIS, N. FASARAKIS et al..An analytical model for the CMOS inverter. *Power and Timing Modeling, Optimization and Simulation (PATMOS).* 2014, p. 1-6. 978-1-4799-5412-4. DOI 10.1109/PATMOS.2014.6951894.

[16] HAMOUI, A.A., N.C. RUMIN. An analytical current, delay, and power model for the submicron CMOS inverter. *Electronics, Circuits and Systems.* 1999, p. 1547-1551. ISBN 0-7803-5682-9. DOI 10.1109/ICECS.1999.814466.

[17] PENG, X. and P. ABSHIRE. Stochastic Behavior of a CMOS Inverter. *Electronics, Circuits and Systems.* 2007, p. 94-97. ISBN 978-1-4244-1377-5. DOI 10.1109/ICECS.2007.4510939

[18] RUANGPHANIT, A., K. KIDEE et al.. The effects of temperature and device demension of MOSFETs on the DC characteristics of CMOS inverter. *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON).* 2012, p. 1-4. ISBN 978-1-4673-2025-2. DOI 10.1109/ECTICon.2012.6254337

[19] BISDOUNIS, L., S. Nikolaidis and O. LOUFOPAVLOU. Propagation delay and short-circuit power dissipation modeling of the CMOS inverter. *Circuits and Systems I: Fundamental Theory and Applications.* 1998, vol. 45, iss. 3, p. 259–270. ISSN 1057-7122. DOI 10.1109/81.662699.

[20] MARRANGHELLO, F. S., A. I. REIS and R. P. RIBAS. CMOS inverter analytical delay model considering all operating regions. *2014 IEEE International Symposium on Circuits and Systems (ISCAS).* 2014, pp. 1452-1455. ISSN 0271-4302. DOI 10.1109/ISCAS.2014.6865419.

[21] IOANNIDIS, E. G., S. HAENDLER et al. Impact of dynamic variability on the operation of CMOS inverter. *Electronics Letters.* 2013, vol. 49, iss. 19, pp. 1214-1216. ISSN 0271-4302. DOI 10.1049/el.2013.1343.

[22] JAEGER, R. C., N. TRAVIS.*Microelectronic circuit design.* 3rd ed. Boston: Mcgraw-Hill, 2008. ISBN 9780073309484.

[23] BAKER, R.. *CMOS: circuit design, layout, and simulation.* 3rd ed. Hoboken, NJ: Wiley, c2010, xxxiii, 1173 p. ISBN 9780470881323. DOI 10.1002/9780470891179.

[24] TSIVIDIS, Y., C. McANDREW. *Operation and modeling of the MOS transistor.* 3rd ed. New York: Oxford University Press, 2011, ISBN 0195170156.

[25] DOBEŠ, J., V. ŽALUD, *Moderní radiotechnika.* 1. vyd. Praha: BEN - technická literatura, 2006, 767 p. ISBN 80-7300-132-2.

[26] LIU, W., J. XIADONG et al.. *BSIM3v3.2.2 MOSFET Model. User´s Manual.* 1999. Department of Electrical Engineerong and Computer Sciences. University of California, Berkeley, CA 947220, url: http://iecon02.us.es/ASIGN/DCSE_4T/Doc/bsim3.pdf.

[27] HU, C., A. M. NIKENJAD et al..*BSIM4.6.4 MOSFET Model: User´s Manual.* 2009, Department of Electrical Engineerong and Computer Sciences. University of California, Berkeley, CA 947220.

[28] NIKENJAD C. Hu, W. YANG et al.. *BSIM4v4.8.0 MOSFET Model: Userś Manual*. 2009, Department of Electrical Engineerong and Computer Sciences. University of California, Berkeley, CA 947220. Available on www.device.eecs.berkeley.edu/bsim/?page=BSIM4.

[29] STEFANOVIĆ, D., M. KAYL. *Structured analog CMOS design*. Dordrecht: Springer, 2008. ISBN 9781402085727.

[30] BREWS, J. R.. MOSFET hand analysis using BSIM. *IEEE Circuits and Devices Magazine*. 2006, vol. 22, no. 1, pp. 28-36. ISSN 8755-3996. DOI 10.1109/MCD.2006.1598077.

[31] *ELDO User´s manual*. 2005. Mentor Graphics Corporation. url: http://web.engr.uky.edu/∼elias/tutorials/Eldo/eldo_ ur.pdf.

[32] CHANG, K.–L. and J.–T. WU. *Charge pumping circuit having cascaded stages receiving two clock signals*. US. 5734290. Granted March 31, 1998.

[33] WANG, Y.–R., Z.-G. YU. A High-Efficiency Cross-Coupled Charge Pump for Flash Memories. *2010 2nd International Conference on Advanced Computer Control, IEEE*. 2010, vol. 3, p. 130-133. ISBN 978-1-5090-0629-8. ISBN 978-1-4244-5848-6. DOI10.1109/ICACC.2010.5486757.

[34] MINAMI, Y., K. IGARASHI. Area-efficient cross-coupled charge pump for on-chip solar cell. *2016 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*. 2016, pp 1-6, ISBN 978-1-5090-0629-8. DOI 10.1109/ISPACS.2016.7824716.

[35] MAJD H. E. and E. RODRIGEUZ–VILLEGAS. *Analysis and design of cross-coupled charge pump for low power on chip applications. Microelectronics Journal*. 2017, vol. 66, pp. 9-17. ISSN 0026-2692.

[36] F, PAN. *Charge Pump IC Design*. McGraw-Hill, 2015. ISBN 9780071836777.

[37] HUI, Z., H. MENGSHU, Z. YIMENG, T. YOSHIKARA. A 4-phase cross-coupled charge pump with charge sharing clock scheme. *Electronic Devices, Systems and Applications (ICEDSA)*. 2011, p. 73-76. ISBN 978-1-61284-389-6. DOI 10.1109/ICEDSA.2011.5959067.

[38] PAN, F. and T. SAMADDAR. *Charge pump circuit design*. McGraw-Hill, c2006, xv, 247 p. ISBN 978-007-1470-452.

[39] WANG, Y.–R., Z.-G. YU, A High-Efficiency Cross-Coupled Charge Pump for Flash Memories. *IEEE Transaction on Circuits and Systems*, 2010, vol. 3. ISBN 978-1-4244-5848-6. DOI 10.1109/ICACC.2010.5486757.

[40] *Maple User Manual–Maplesoft*. 2014 Maplesoft, a division of Waterloo, Maple Inc..

[41] MAREK, J..Modelování a návrh nízkopříkonové nábojové pumpy. *Diploma thesis*. 2014, CTU in Prague-FEE, Department of Microelectronics.

[42] SHIAU, M.–S., Z.–H. HSIEH et al..A novel static CTS charge pump with voltage level controller for DC-DC C=converters. *2007 IEEE Conference on Electron Devices and Solid-State Circuits*. 2007, p. 481-484. ISBN 978-1-4244-0636-4. DOI 10.1109/EDSSC.2007.4450167.

[43] NEW, L.F., Z.A.bin ABDUL, M.F. LEONG, *A low ripple CMOS charge pump for low-voltage application. Intelligent and Advanced Systems (ICIAS)*.2012, vol. 2. ISBN 978-1-4577-1967-7. DOI 10.1109/ICIAS.2012.6306120.

[44] G. PALUMBO and D.PAPPALARDO. Charge pump circuits with only capacitive loads: optimized design. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2006, vol. 53, iss. 2. ISSN 1549-7747. DOI 10.1109/TCSII.2005.855732.

[45] HONKELA, A., *Nonlinear switching state-space models.* Master´s thesis. 2001. Helsinki university of technology.

[46] ARROWSMITH D. K. and C. M. PLACE, *An introduction to dynamical systems.* 1990. Cambridge University Press, Cambridge.

List of candidate´s work related to the thesis

The percentage is even for all listed authors at each publication[1].

Journals (Impact)

- MAREK, J., J. HOSPODKA and O. ŠUBRT, Guidelines on the switch transistors sizing using the symbolic description for the cross-coupled charge Pump. *Radioengineering*, vol. 26, iss. 3, 2017. ISSN 1805-960. [85%]

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Complex model description and main capacitor sizing for the cross-coupled charge pump synthesis process. *Journal of Electrical Engineering.* 2018, ISSN 1339-309X. Available on: http://iris.elf.stuba.sk/JEEEC *(ACCEPTED FOR PUBLICATION.)* [85%]

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Synthesis of the cross-Coupled charge pump on circuit-Level hardware realization.*Advances in Electrical and Electronic Engineering. (UNDER REVIEW PROCESS.)*

Conferences indexed in WoS

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Design aspects of the SC circuits and analysis of the cross-coupled charge pump. *2016 International Conference on Applied Electronics (AE).* 2016, pp. 165-168. ISBN 978-80-261-0602-9 . DOI: 10.1109/AE.2016.7577265. (IN THE BEST PAPERS CATEGORY.) [90%]

- MAREK, J., J. HOSPODKA and O. ŠUBRT Description of the functional blocks for the cross-coupled charge pump design algorithm. *2017 International Conference on Applied Electronics (AE), Pilsen, Czech Republic.* 2017, pp. 1-4. ISBN 978-8-0261-0642-5. DOI: 10.23919/AE.2017.8053594. [85%]

- MAREK, J., J. HOSPODKA and O. ŠUBRT. A program procedure for estimation of the cross-coupled charge pump properties. *2018 International Conference on Applied Electronics (AE), Pilsen, Czech Republic.* 2018. ISBN 978-80-261-0722-4. [85%]

Journals (Reviewed)

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Design rules of the CMOS inverter for voltage converters. *2018 International Journal of Engineering and Innovative Technology (IJEIT).* 2016, vol. 5, iss. 11, pp. 7-12. ISSN 2277-3754. DOI: 10.13164/re.2017.0781. [90%]

Other publications related to thesis

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Analýza nábojová pumpy CTS-2. *In: V. Letní doktorandské dny 2015.* Praha: ČVUT FEL, Katedra teorie obvodů, 2015. pp. 17-22. ISBN 978-80-01-05749-0. [33.3%]

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Modelovaní funkčních bloků křížově vázané nábojové pumpy. *In: VI. Letní doktorandské dny 2016.* Praha: ČVUT FEL, Katedra teorie obvodů, 2016. pp. 18-23. ISBN 978-80-01-05959-3. [85%]

[1] The supervisor and the supervisor-specialist are the only co-authors of all the mentioned publications. Their percantage are not counted in according with *Rules of Doctoral Study at the CTU in Prague.*

- MAREK, J., J. HOSPODKA and O. ŠUBRT. Analýza přechodových dějů v křížově vázané nábojové pumpě. *In: VII Letní doktorandské dny 2017*. Praha: ČVUT FEL, Katedra teorie obvodů, 2017. pp. 25-30. ISBN 978-80-01-06161-9. [85%]

List of other candidate´s publications

- MAREK, J., J. HOSPODKA. *Analýza neohraničených kolejových obvodů ve volném, šuntovém a havarijním stavu*. Interní výzkumná zpráva. Praha: ČVUT FEL, Katedra teorie obvodů, 2016.