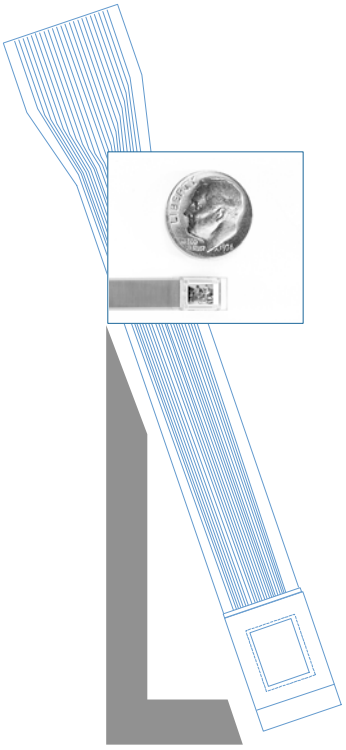
CyberDisplay™



A230 Display Driver

Rev 2.0
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KOPIN CONFIDENTIAL

PS-0305 Rev 2.0

1. Overview

A230 driver IC supports low voltage CyberDisplay®. It designed to accept BT.656 or similar digital video source and generate analog RGB for the CyberDisplay®. It supports internal frame buffer for up to 432x240 or smaller windows of video which can be alpha blend into BT656 video input. It includes three 8-bit DACs and three video amplifiers, one charge pump for -6 V power supply voltage to the display and two PWM current sinks for backlight LED. It supports two types of serial interface and one processor interface, which are I2C, 3-wire serial interfaces and Intel 80 bus.

Features

- Low-voltage CyberDisplay® 113K/152K or 230K/308K
- Support NTSC and PAL
- Up to 40MHz video input clock
- Digital video input formats
    - BT.656 standard digital video (YCBCR 422 8-bit interlaced video input).
    - Square-pixel variants of BT.656
    - Any of the above format with separate HS and VS input instead of embedded sync (SAV/EAV)
    - Supports also interlaced formats using RGB 888(8bit serialized) , RGB 565(16bit) and YCBCR 422 16 -bit
    - Color space conversion when using YCBCR mode.
    - Native QVGA, WQVGA progressive format
- Internal frame buffer
    - 103680 x 16 bits SRAM
    - Resolution up to 432x240
    - Supports up to 4 windows with programmable position and size with respect to display frame
    - Supports following storage formats:
        - 16 bit RGB 565
        - 16 bit RGB Alpha 4444 or 5551
        - 8 bit RGB332
        - 3 bit 8 color video RGB 111
- Video overlay
    - Overlay video from frame buffer on to external video input
    - Supports Alpha blending of frame buffer video with external video

- Supports fade-in and fade-out using global alpha control , Windows Alpha control or local pixel level alpha blending data

- Horizontal and vertical scaling
- Programmable dual-string gamma correction with two individual look up tables per each color
- Programmable video enhancement on YCbCr
  - Contrast, brightness and sharpness control on Y signal
  - Gain control on Cb,Cr signal
- Support line buffer base horizontal inversion.
- Programmable timing control for CyberDisplay®s
- I2C, 3-wire serial interface and Intel 80 bus
- RGB 8-bit DACs and video amplifiers
- A charge pump to provide -6 V power to CyberDisplay®s
- Two current sink for backlight
- Independent drive strength control for display interface signals
- An LDO regulator to generate 1.8V from the IO supply voltage
- Power saving function
  - Clock gating
  - Power down control for all individual blocks
  - Video amplifier power control register
    - Power VS Performance
  - Use CMOS switches for 3 bit video mode
  - Can be operated as only external video or only frame buffer mode to save power
- 1.8V core/1.8~3.3V IO/3.3~5V Display IO and Analog Power
- 121 FBGA

2. Block Diagram

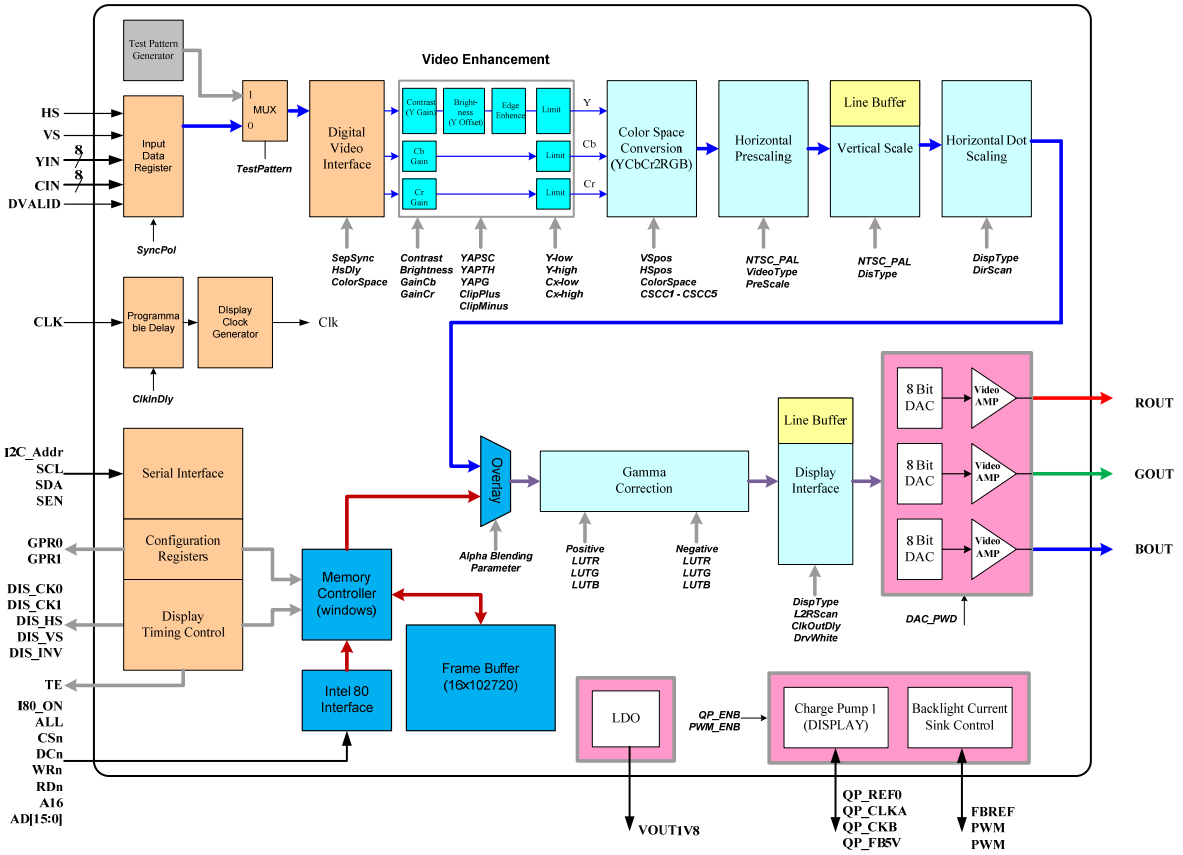


Figure 1. A230 block diagram

Part Number

KCD-A230-BC (Commercial grade 0º C to 70º C, ROHS, 121 FBGA)

3. Functional Description

3-1. Digital Video Interface

The digital video interface accepts 8 or 16 bit data and clock for video input. The interface supports up to 40MHz video input clock. Additional horizontal and vertical sync inputs are needed in some formats. It also converts the 4:2:2 YCbCr format to 4:4:4 format before feed the video data to color matrix. The supported input formats for video path are;

- BT.656 standard digital video (422 YCBCR 8 or 16 bit interlaced) , both 525-line/60Hz and 625-line/50Hz (NTSC or PAL)
- Square-pixel variants of BT.656 for both NTSC and PAL
- Any of above with separate HS and VS inputs instead of embedded sync (SAV/EAV)
- Native QVGA/WQVGA progressive with HS and VS input
- Formats using 8-bit serialized RGB 888 or 16-bit RGB 565 color spaces instead of YCbCr
- 8 bit formats uses YIN [7:0] as the data input.
- The mapping for 16-bit RGB565 is as follows:

```
B[4:0] = CIN[4:0]
G[2:0] = CIN[7:5]
G[5:3] = YIN[2:0]
R[4:0] = YIN[7:3]
```

Table 1 summarizes the timing and resolution of NTSC/PAL formats.

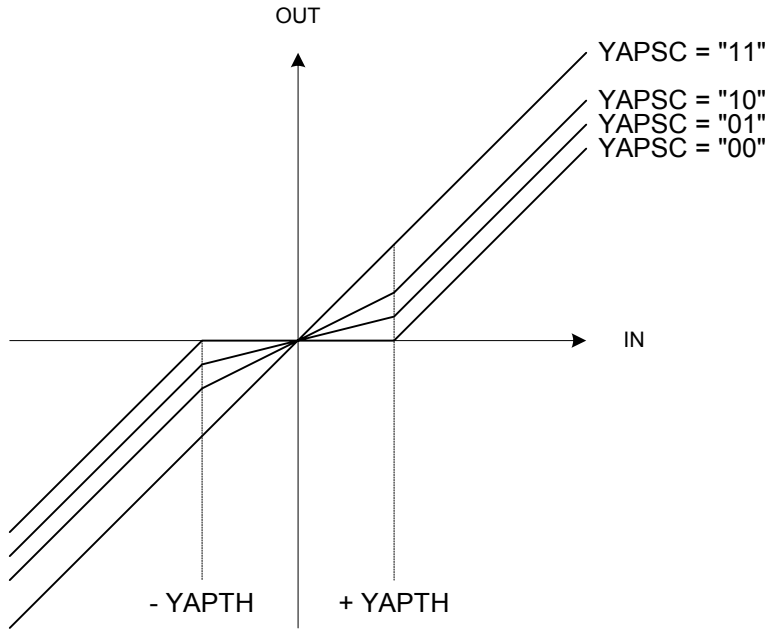
Format	Mode	Clock (MHz)	Total Y Samples/Row	Active Y Samples/Row	Active CbCr or RGB Samples/Row
16:9 Standard	NTSC	36.00/18.00	1144	960	480
	PAL	36.00/18.00	1152	960	480
16:9 Square	NTSC	32.72/16.36	1020	856-864	428-432
	PAL	39.3/19.7	1258-1260	1024	512
Standard	NTSC	27.00/13.5	858	720	360
	PAL	27.00/13.5	864	720	360
Square Pixel	NTSC	24.54/12.27	780	640	320
	PAL	29.5/14.75	944	768	384
Native	QVGA	6.75	429	320	320
	WQVGA	9	572	428	428

Table 1. Digital input format

3-2. Digital Video Enhancement

The digital video enhancement block enhances YCbCr video source by Contrast, Brightness, Sharpness on Y signal and Gain on Cb, Cr signals. Enhanced data are limited to BT.656 data range as default (Y : 16 ~ 235, Cb & Cr : 16 ~ 240)

- Contrast control : 0X to 1.99X
- Brightness control : -128 to 127
- Sharpness control block enhance picture sharpness. Sharpness control block generate horizontal sharpness filter from Y video input. Sharpness filter can be noise slice, gain control and clipping by configuration registers.
- Cb, Cr Gain : 0X to 1.99X
- Y_low, Y_high : Y signal low and high limits.
- Cx_low, Cx_high : Cb, Cr signals low and high limits.



* YAPSC: Sharpness Noise Slice Control
YAPTH: Sharpness Noise Slice TH Value

Figure 2. Edge enhancement filter

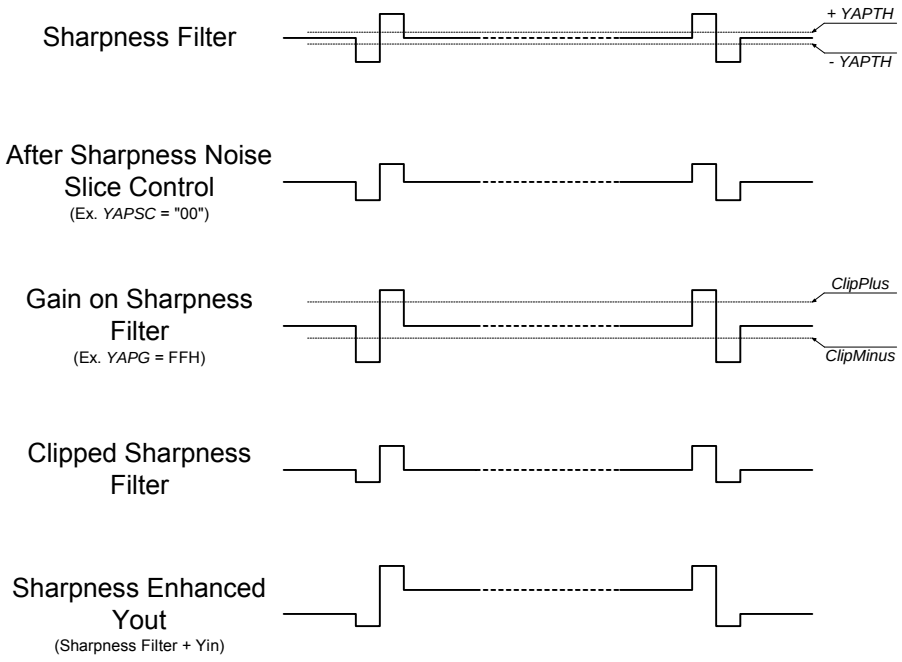


Figure 3. Edge enhancement process

3-3. Color Space Conversion

The color space conversion block converts color space from YCbCr to RGB by following equations.

- R = CSCC1 * (Y – 16) + CSCC2 * (Cr – 128)
- G = CSCC1 * (Y – 16) – CSCC3 * (Cr – 128) – CSCC4 * (Cb – 128)
- B = CSCC1 * (Y – 16) + CSCC5 * (Cb – 128)

The default values of the constants are;
CSCC1 = 1.164
CSCC2 = 1.596
CSCC3 = 0.813
CSCC4 = 0.392
CSCC5 = 2.017

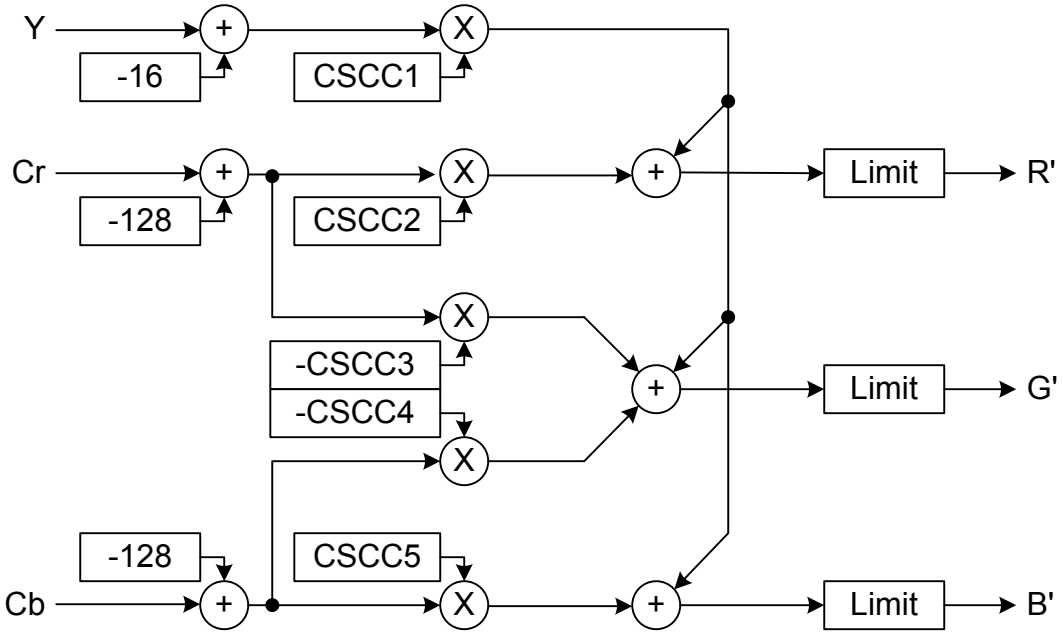


Figure 4. Color Space Conversion

3-4. Horizontal Pre-scaling

The horizontal pre-scaling stage makes 640 samples per line video data, independent of the input format. All scaling is linear interpolated and pre-scaling ratios can be selected by internal mode registers 0x00 and 0x05 as follows:

VideoType[0]	NTSC/PAL	PreScale	Pre-scale ratio	Modes
0	0	0	11:10	Standard NTSC/PAL
0	0	1	9:8	Standard NTSC/PAL
1	1	X	6:5	Square pixel PAL
All others			1:1	Square Pixel NTSC

The pre scale ration can be overridden by PreOVRD bits in register 0x05

3-5. Vertical Scaling

PAL input data will be vertically 6:5 scaled by linear interpolation.

3-6. Horizontal Dot Scaling

The second phase of horizontal scaling produces output samples matching the display's dot layout. The dot scaling consists of three fixed ratios which are selected by DisType bits in register 0x10 as follows:

DispType[1]	DispType[0]	Dot-scale ratio	Display Modes
0	0	2:1	CyberDisplay® 230K/308K
0	1	3:2	CyberDisplay® 230K/308K
1	0	5:9	CyberDisplay® 113K/152K
1	1	5:12	CyberDisplay® 113K/152K

For CyberDisplay® 113K display, the 61 samples are discarded from 640 pre-scaled samples before 5:9 horizontal dot scaling.

The dot scale ratio can be overridden by the DotOVRD bits in register 0x05.

The VideoType[1] and DispType[1] bits also used to select the clock for display drive block. The automatic display clock selection can be overridden by the DclkOVRD bits in register 0x09.

Figure 5 to Figure 11 show the optimal scaling ratios for various input and output combination.

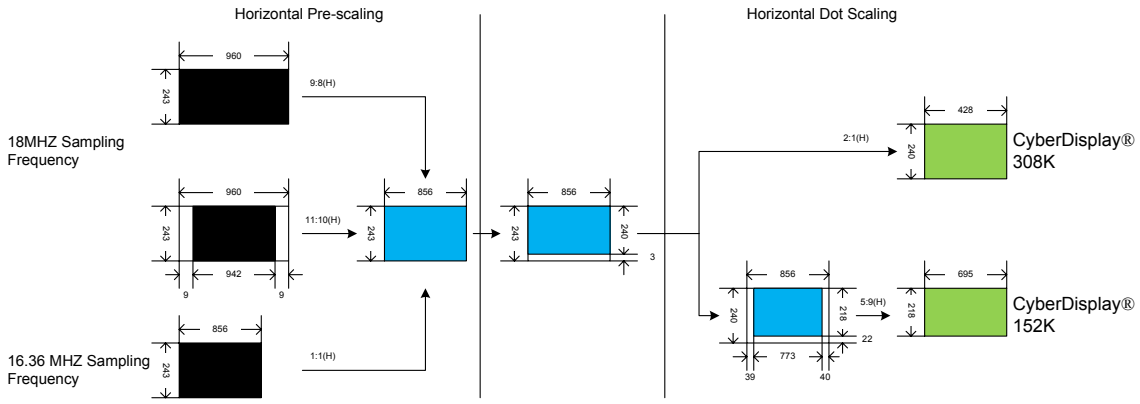


Figure 5. Scaling: NTSC wide input to 308K, 152K

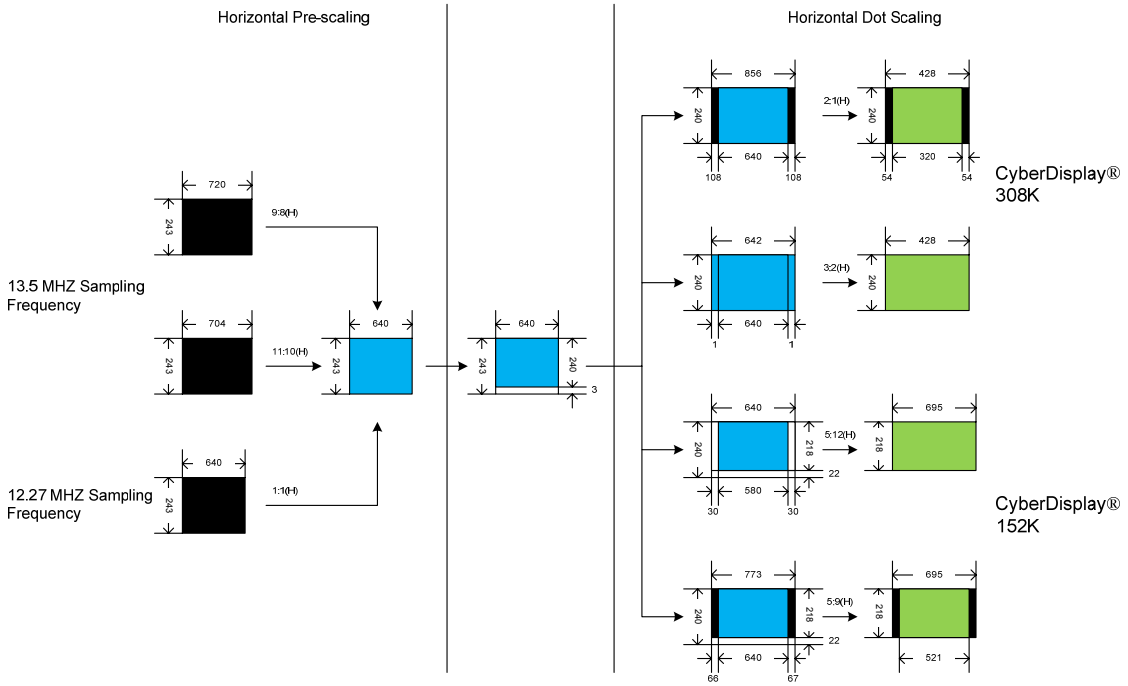


Figure 6. Scaling: NTSC input to 308K, 152K

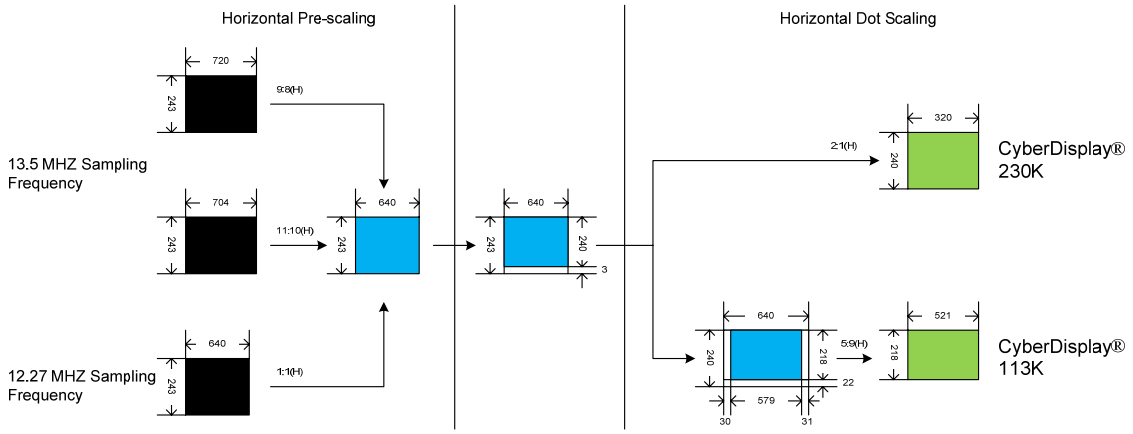


Figure 7. Scaling: NTSC input to 230K, 113K

]

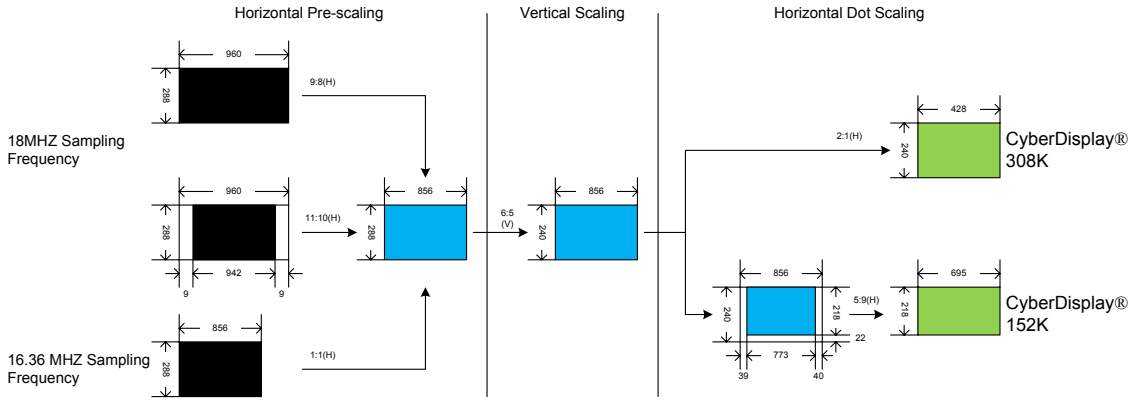


Figure 8. Scaling: PAL wide input to 308K, 152K

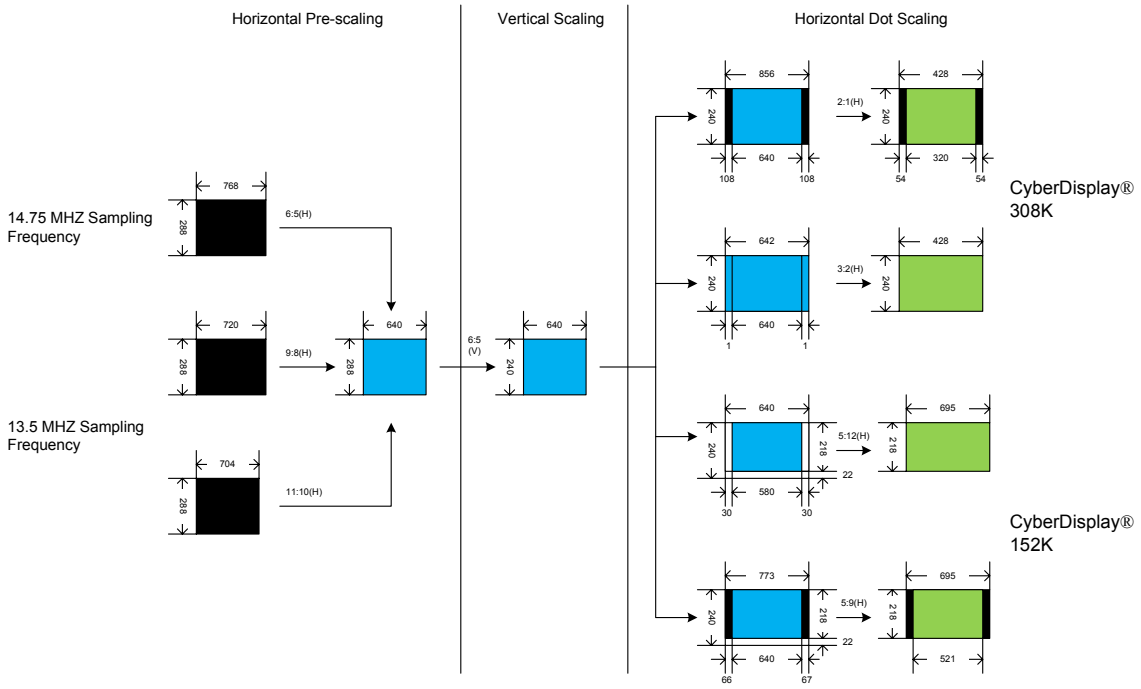


Figure 9. Scaling: PAL input to 308K, 152K

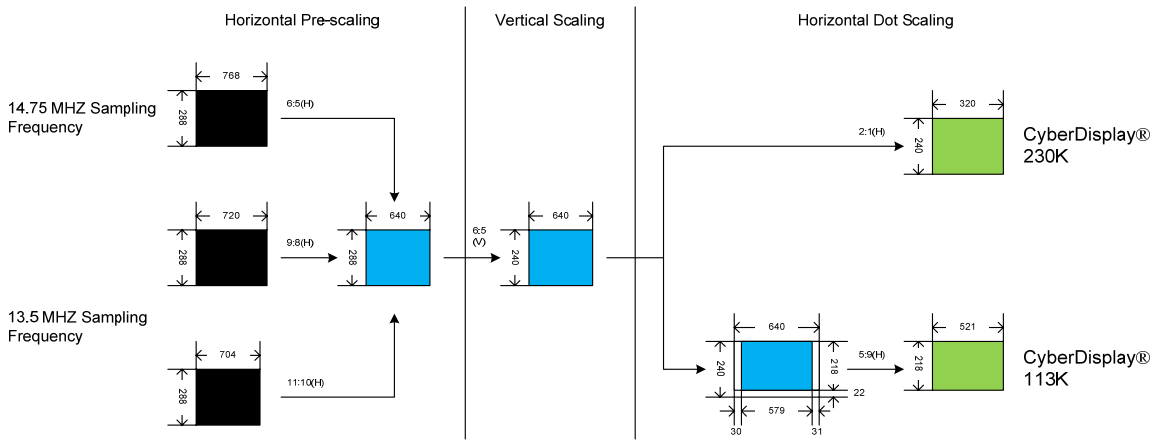


Figure 10. Scaling: PAL input to 230K, 113K

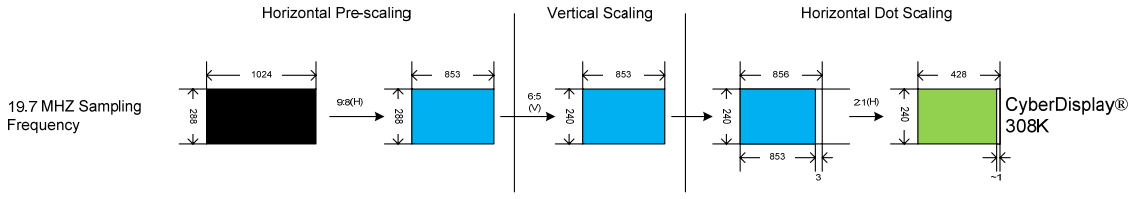


Figure 11. Scaling: PAL wide input to 308K

3-7. Frame Buffer

A230 implements 103680x16 bits SRAM frame buffer which can support video resolution up to 432x240. Each word in the frame buffer is 16-bit wide. The video from frame buffer is displayed in the form of window. In the case of external video the window from the frame buffer is overlaid on to the external video. In case of no external video the window is overlaid on a black background. The window may fill the full display frame or part of the frame. There are a maximum of 4 windows at time. The numbers of windows are also limited by the amount of storage available in the frame buffer. A host may write to the frame buffer memory via serial interface(I2C or 3-wire) or via Intel80 type parallel interface. The frame buffer data can also be read via I2C or Intel80 bus. The frame buffer support following video formats:

- 16 bit RGB 565
- 16 bit RGB Alpha 4444 or 5551
- 8 bit RGB 332
- 3 bit 8 color video RGB 111

Figure 12 to Figure 14 show relationship between width of the data in the frame buffer and the pixel on the display with a window configuration parameters.

For 16bit data format, each 16bit data allocated to single pixel. For 8bit data format, each 16bit data allocated to two pixels. For 3bit data format, each 16bit data allocated to four pixels.

Each of the 4 windows occupies a contiguous space in the frame buffer and staring address is pointed to by a register in the configuration register map. The location and size of each window are programmable.

The definitions of the parameters of a window in Figure 12 to Figure 14 are as follows:

S= Start address of a window
W= Window width
H= Window height
X= Horizontal position of the window with respect to display frame
Y= Vertical position of the window with respect to display frame

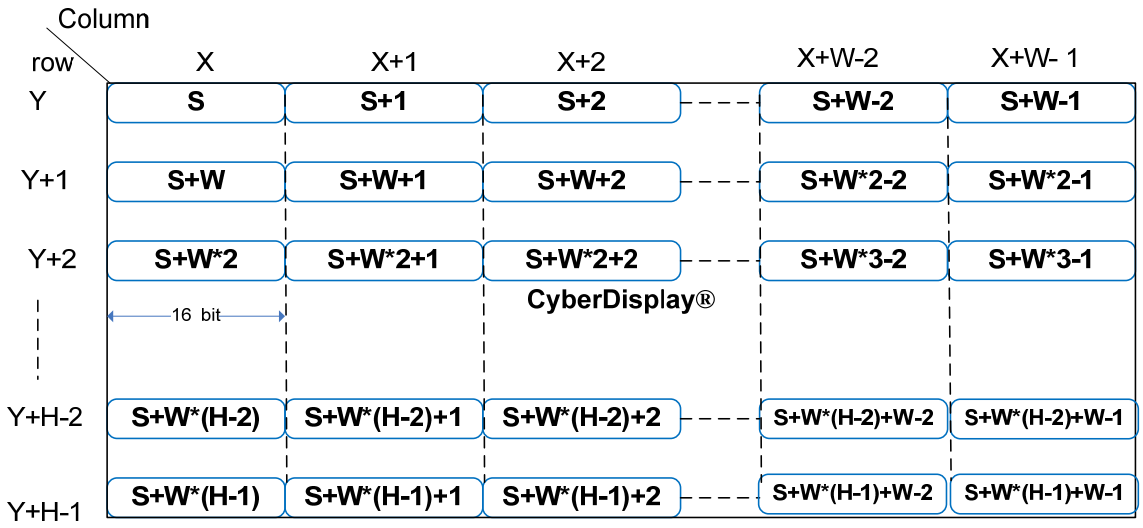


Figure 12. The frame buffer data allocated in 16bit data format

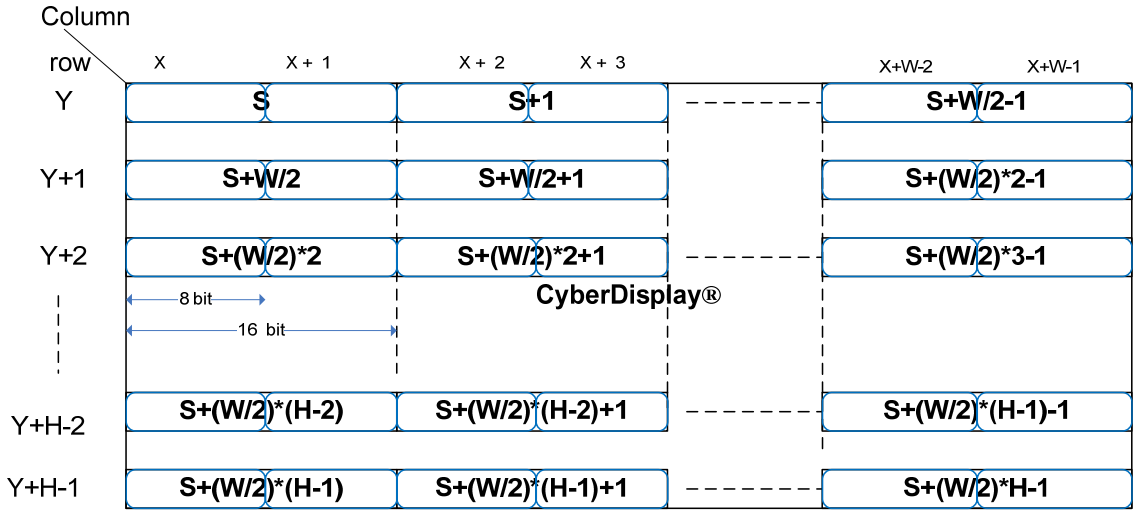


Figure 13. The frame buffer data allocated in 8bit data format

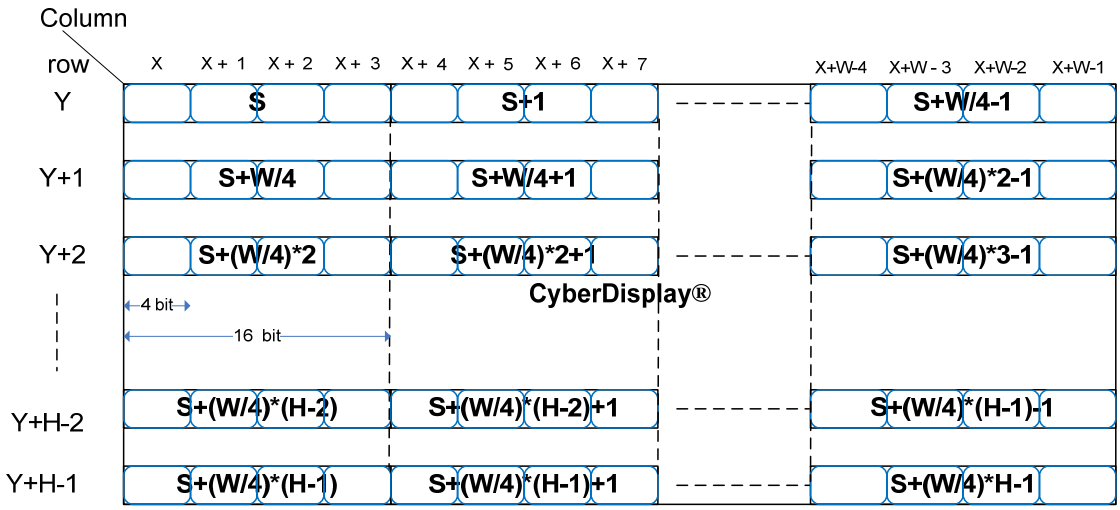


Figure 14. The frame buffer data allocated to CyberDisplay® (3bit data)

The FBVideoType bits in register 0x4C control the allocation of video data bits in a word to the R, G, B colors. It also controls the allocation of data to pixels in 8 bit and 3-bit modes. For 8bit data format, each 16bit data allocated to two pixels. For 3bit data format, each 16bit data allocated to four pixels.
Figure 15 shows the relationship between frame buffer data to RGB colors and pixel ordering for 8-bit and 3-bit modes.

In order to enable power saving in 3-bit RGB111 mode, the following bits must be set high:

1. HIGH_LOW_EN: bit 7 of register 4CH
2. INVINV : bit 7 of register 35H
3. DAC_DWN : bit 5 of register 13H

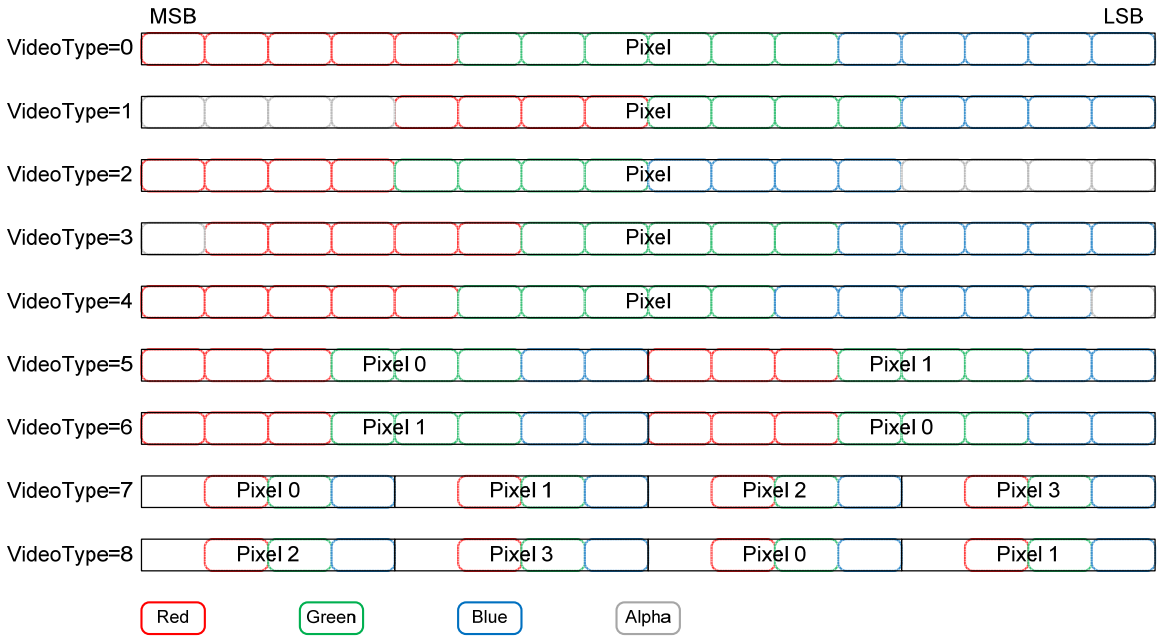


Figure 15. The frame buffer data allocation to RGB and pixel ordering

3-7-1. Frame Buffer Access

A host may access the frame buffer memory via serial interface (I2C or 3-wire) or via Intel80 type parallel interface. There are two types of access to the frame buffer direct and indirect. In direct address mode the frame buffer is addressed directly by frame buffer address and data. Only Intel80 interface supports this type of transaction. In the indirect mode the frame buffer is accessed via the address register (0xB9-0xBB) and data register (0xBC-0xBD). Both Intel80 and serial interface supports indirect access. Serial interface can only do 8-bit indirect access. Refer to Figure 16 for 8-bit and Figure 17 for 16-bit indirect access to the frame buffer.

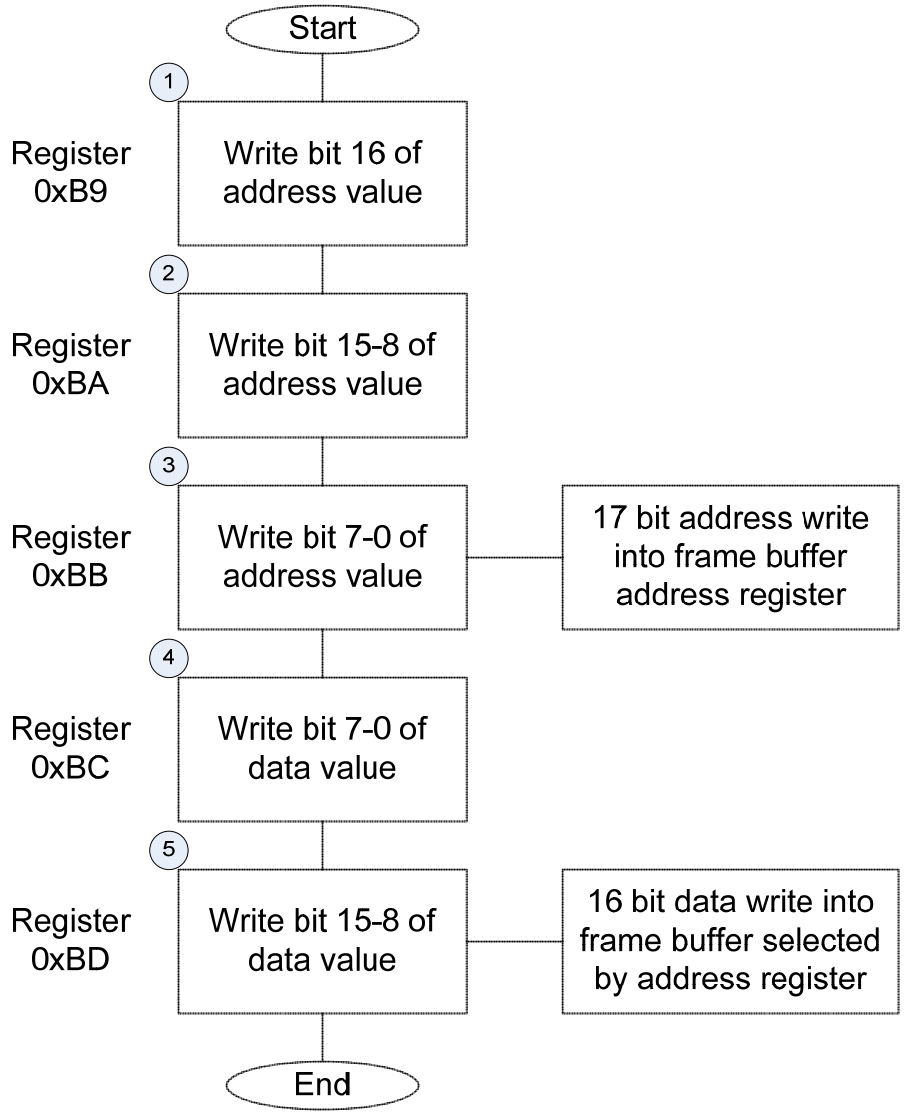


Figure 16. 8bit interface indirect data write to the frame buffer

In case of burst mode step 4 and 5 in Figure 16 are repeated continuously. After completion of step 5 the data is written to the frame buffer and the internal fame buffer address is incremented automatically.

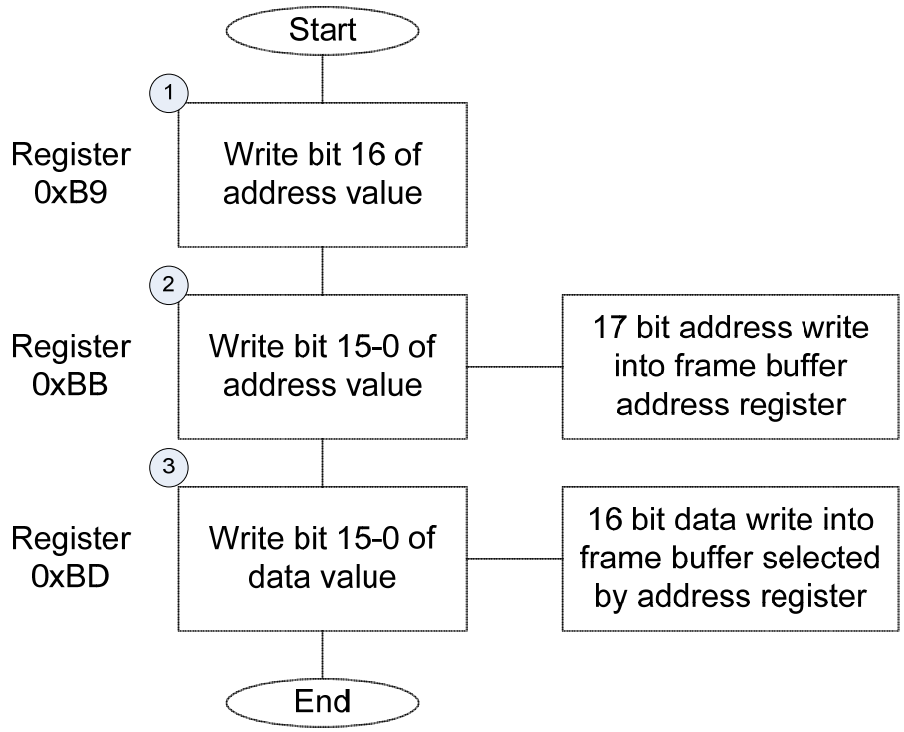


Figure 17. I80 16bit interface indirect data write to the frame buffer

In case of burst mode step 3 in Figure 17 is repeated continuously. After completion of step 3 the data is written to the frame buffer and the internal fame buffer address is incremented automatically.

I case of direct address mode the data phase of the Intel80 transaction is repeated continuously and internal address is incremented automatically at the end of the data phase.

3-7-2. Windows Control

There are a maximum of 4 windows at time. Each of the 4 windows occupies a contiguous space in the frame buffer and staring address is pointed to by a register in the configuration register map. The location and size of each window are programmable. Each window has its global Alpha Blend parameter. The registers 0x80 to 0x9E control the windows location, alpha blend and size. The registers 0xA0 to 0xAE points to the start address of window data in the frame buffer.

When the two or more windows overlap each other than the highest priority window is displayed and others are ignored. The priority of windows is Window0 > Window1 > Window2 > Window3

Refer to Figure 18 for windows control and priority scheme.

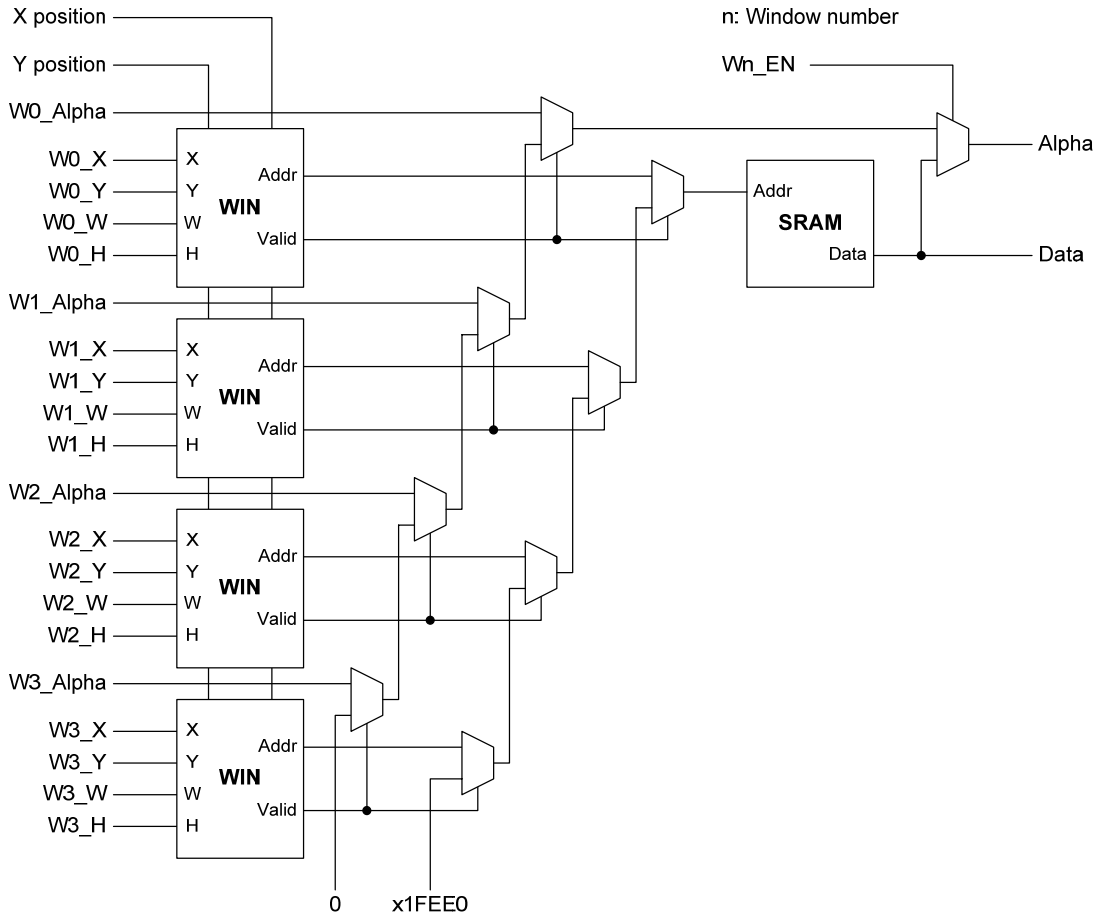


Figure 18. Windows control

Video Overlay

A230 can display video either from external source or from the frame buffer. It can also blend these videos to make an overlay video. The video overlay feature supports alpha blending controlled by a global AlphaBlend (Register 0x4D) parameter. The global alpha blend applies to all windows. It also support pixel based alpha blending when the stored data is one of the four alpha blend video data types (FBVideoType 1, 2, 3, 4). In the case of alpha blend data types the local pixel based alpha is selected instead windows alpha.

When the two or more windows overlap each other than the highest priority window is displayed and others are ignored. The priority of windows is Window0 > Window1 > Window2 > Window3. Refer to Figure 18 for windows priority scheme.

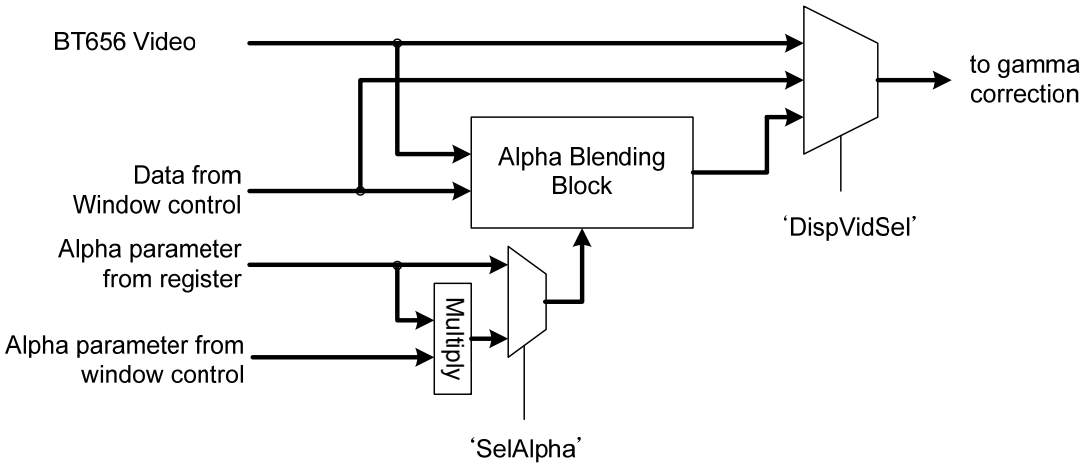


Figure 19. Alpha blending control for video overlay

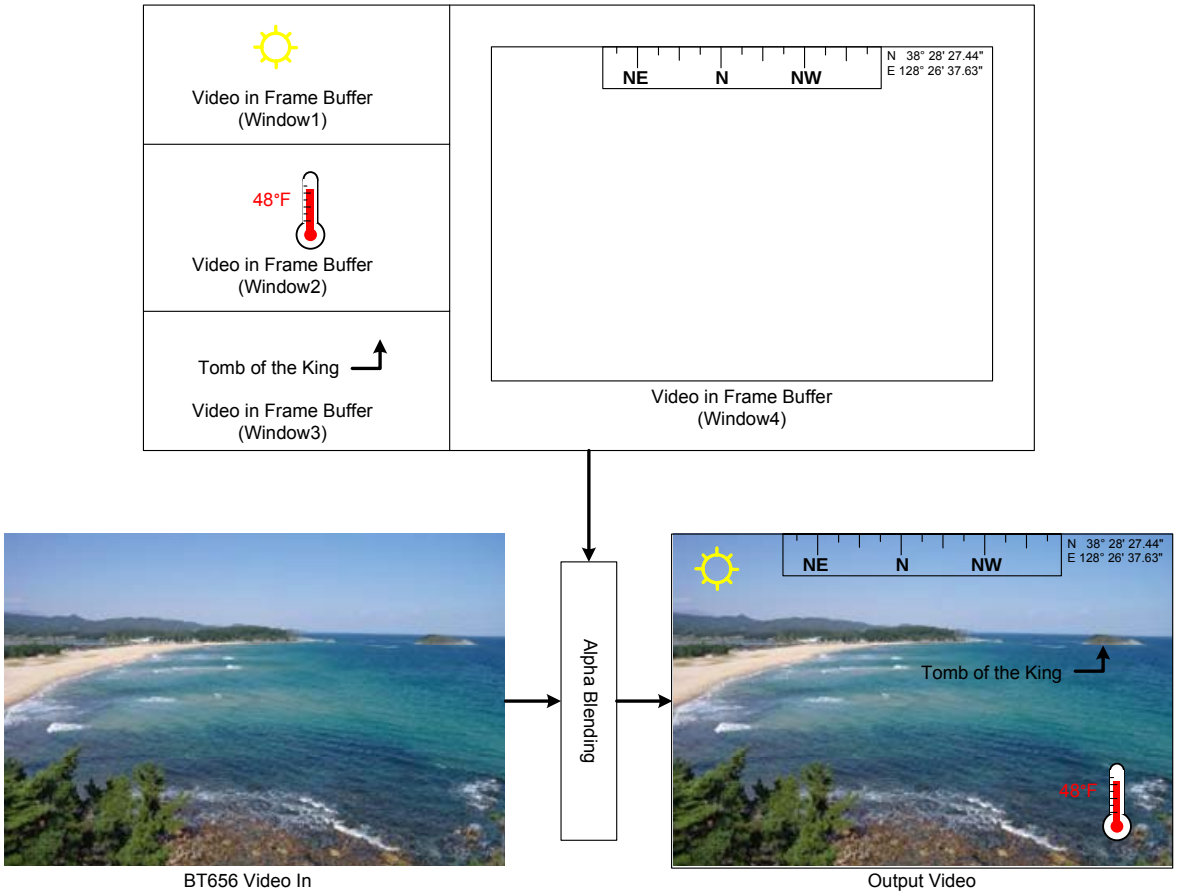


Figure 20. Example of overlay with 4 windows

Refer to Figure 20 for an example with 4 non overlapping windows. Refer to Figure 21 for an example with 2 overlapping windows.

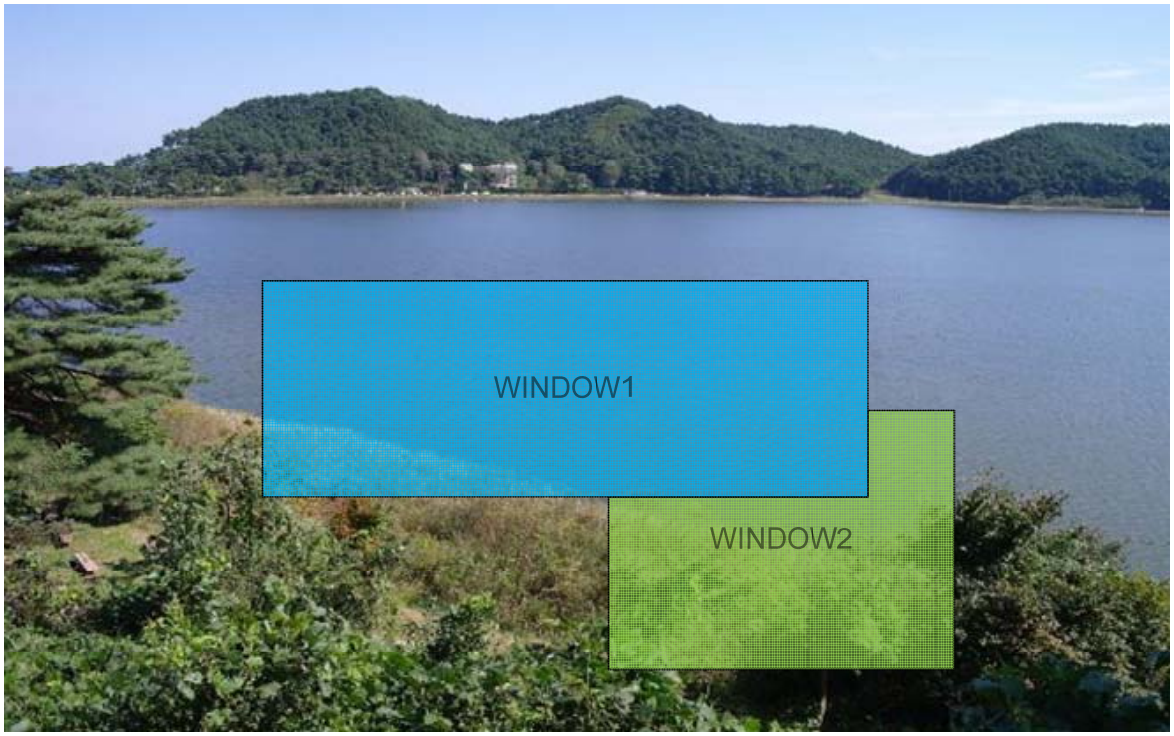


Figure 21. Example of overlapped windows

3-8. Dual-String Gamma Correction

A230 supports gamma correction on the input video signal. A230 drives high and low input of the display in alternative row period. The Dual-String Gamma Correction implements separate lookup table for high and low video output. The gamma correction is performed using piecewise linear interpolation function with programmable 17 look up table for each positive and negative channel. The following figure shows the typical shape of a gamma lookup table where the horizontal side is 8 bit input video points with step size of 16 and the vertical side is the corresponding output values in the LUT. The intermediate gamma corrected output value is calculated by interpolating between 2 points of the table. The process of interpolation is called linear interpolation.

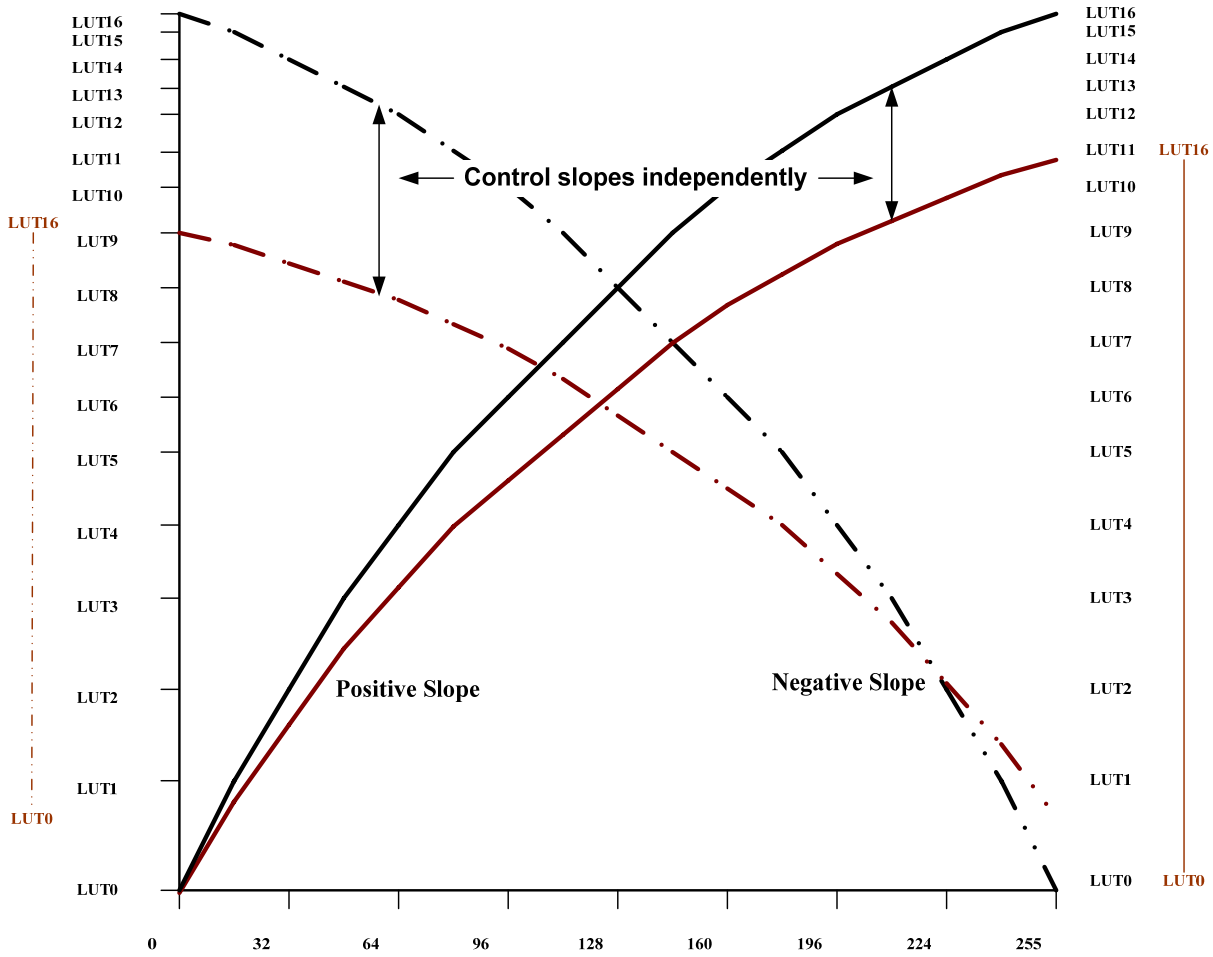


Figure 22. Dual-String Gamma

The calculation of linear interpolation is:

Gamma_x = LUT[x/4] + (((Lut[x/4+1] - Lut[x/4]) / 4) * (x%4)) ;

Where x is the 8 bit input video level.

For example, input data is 0x65 then the output value is in between LUT[6] and LUT[7].

Loading gamma table

The positive and negative channel LUT has separate set of registers to load the LUT values. The registers 50H-60H are LUT for negative and the registers 62H-72H are LUT for positive. The default values in the gamma LUTs are set to linear.

3-9. I²C Serial Interface

The A230 supports I²C serial interfaces. The I²C sub-address can be changed by I2C_ADDR pins. Table 2 shows sub-address configuration for I²C interface.

I²C_Addr	Sub-Address
00	68H
01	6AH
10	6CH
11	6EH

Table 2. I2C Address

3-10. 3-wire Serial Interface

The A230 also supports write only 3-wire serial interface to host. The 3-wire uses 16 bit transaction which composed by 8 bit address (A7 - A0) and 8 bit data (D7 - D0). Refer to next figure for format of 3-wire write transaction.

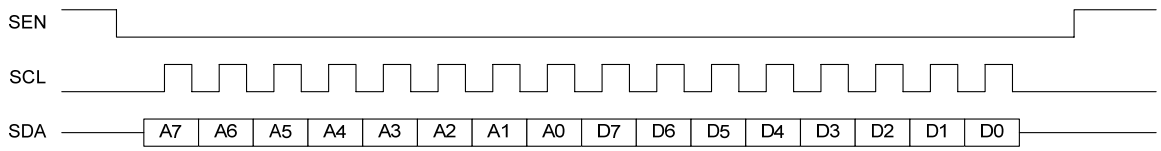


Figure 23. 3-wire Format

A high on SI_SEL pin selects I2C interface and a low selects 3-wire interface.

3-11. Intel 80 Bus Interface

The A230 supports Intel80 bus interfaces for external host processor. The bus supports read and write access to configuration registers and frame buffer memory. The signals for Intel80 bus are as follows:

Signal name	Description
A16	MSB of the 17 bit address
AD[15:0]	16-bit address/data
CSn	Chip select
DCn	Address indicator or address latch strobe
WRn	Write strobe
RDn	Read strobe

There are two modes of Intel80 timing based on DCn input signal. The ALEEN IO input selects the behavior of DCn. The input DCn work as address indicator when ALEEN is 'Low' and works as address latch strobe when ALEEN is 'High'. Figure 24 and Figure 25 show the timing when DCn behaves as address indicator.

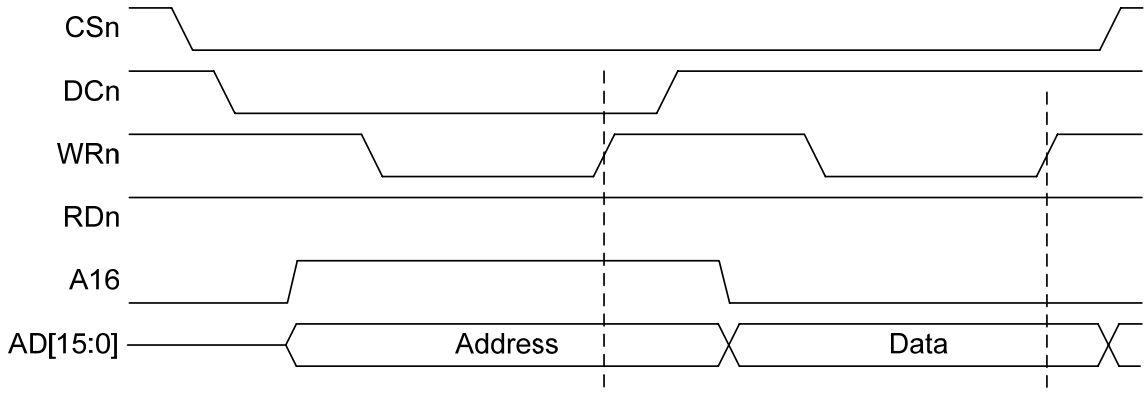


Figure 24. Intel 80 bus write (ALEEN=0)

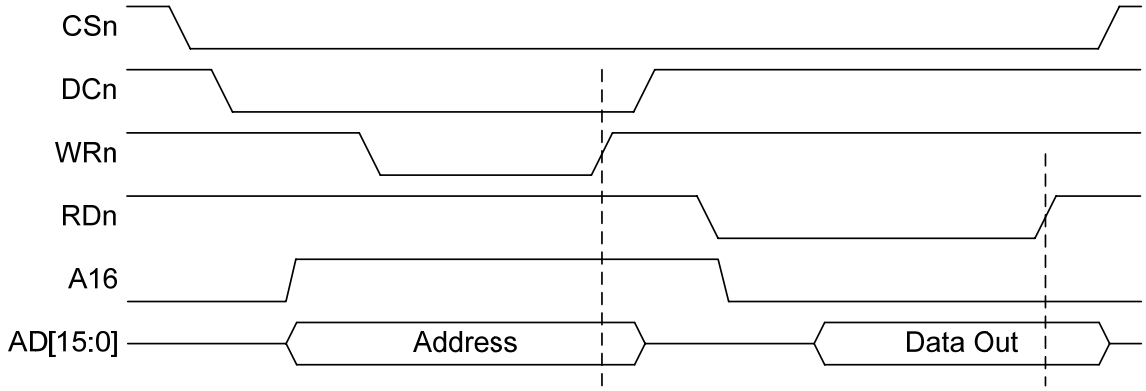


Figure 25. Intel 80 bus read (ALEEN=0)

Figure 26 and Figure 27 show the timing when DCn behaves as address latch strobe.

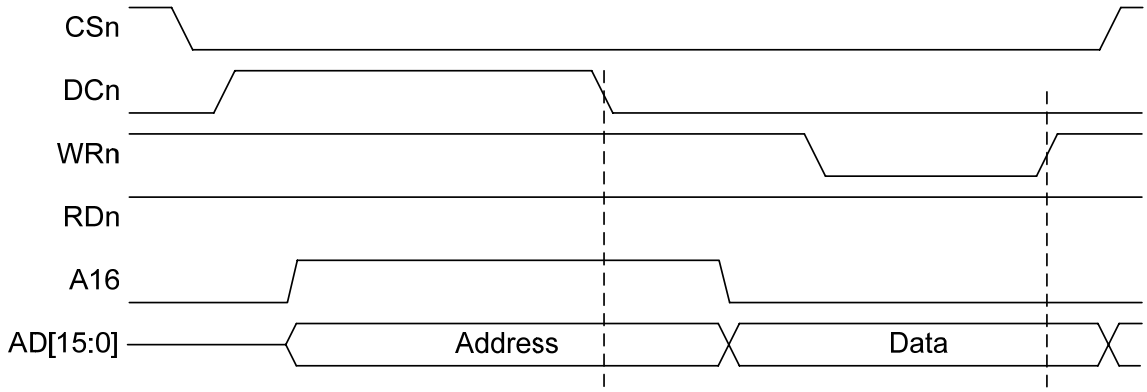


Figure 26. Intel 80 bus write (ALEEN=1)

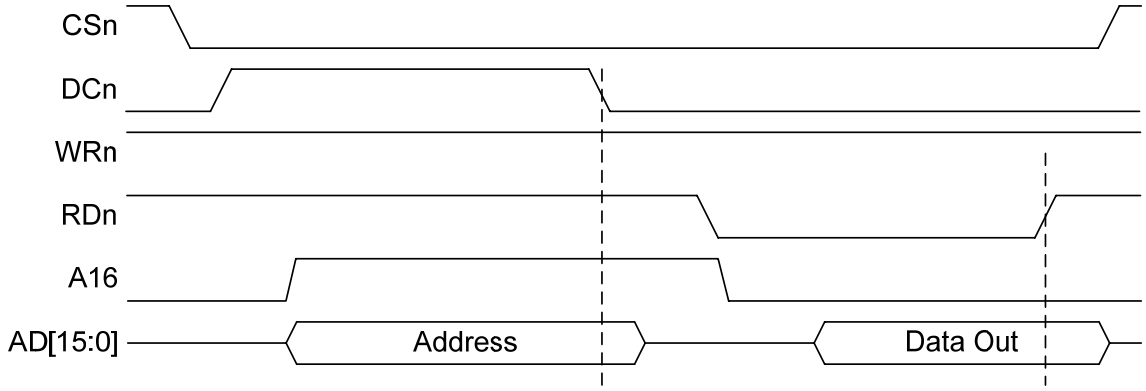


Figure 27. Intel 80 bus read (ALEEN=1)

The AC characteristics and detailed of Intel80 bus is shown in Figure 38 ~ Figure 3941.

An IO pin I80_CAEN (low selects serial and high selects Intel80) selects which interface serial or Intel80 has access to configuration register. In direct access mode the address 0 of configuration register is mapped to address 0x1FF00.

4. Analog Block

The A230 has three 8bit digital to analog converters. The A230 also has 3 video amplifiers which can be support one CyberDisplay®. There is one charge pump for generating negative power to the display. Also, there are two backlight current sink for drive backlight LED.

4-1. Analog Video Path

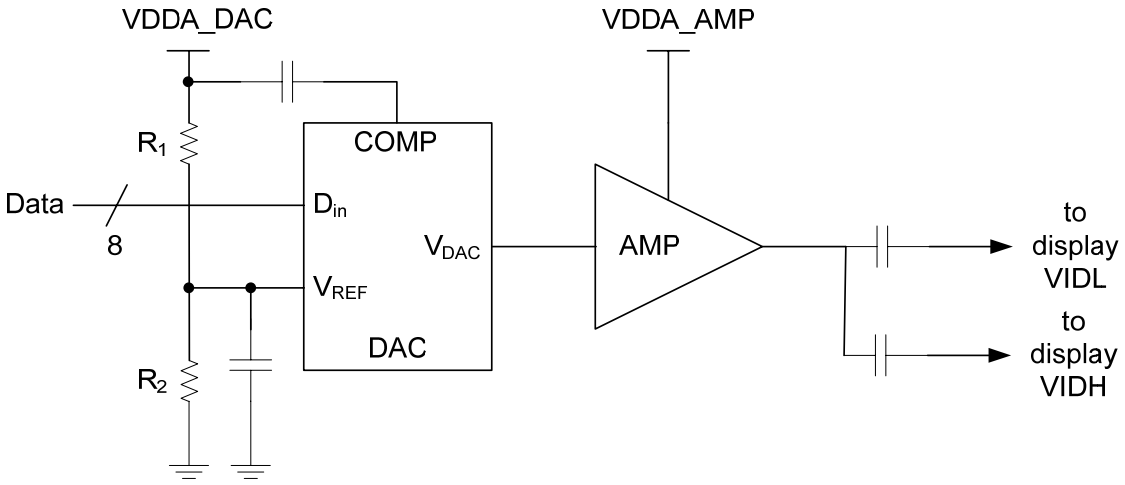


Figure 28. Digital to display video path

4-2. Digital to Analog Converter (DAC)

The A230 has three digital to analog converters. The included DAC has following features.

- 8 bit parallel input
- Maximum conversion rate - 6 MSPS
- One external voltage reference (DAC_VREF)
- One external compensation input
- Supports power down mode
- Maximum ±0.5 LSB integral linearity error

The DAC output voltage can calculate by following formula.

V_{REF} = VDDA_DAC x $[R_2/(R_1+R_2)]$ – – – – – – (1)

$V_{DAC} = V_{REF} / 256 \times D_{IN}$ (D_{IN}=0,1, ⋯,254,255) ------(2)

4-3. Video Amplifier

The A230 has 3 video amplifiers, the Figure 29 shows data path from the DAC to the display. The amplifier has 5 times gain, so the output voltage of the video amplifier is

$V_{AMP} = V_{DAC} * 5$

4-4. Charge Pump

A230 has a charge pump for supplying negative voltage to display. Figure 30is a charge pump reference circuit with 4 diodes which is suitable for VDDA_QP up to 3.3V. Figure 31 is a charge pump reference circuit with 3 diodes which is suitable for VDDA_QP over 3.3V. Refer to Table 3 for parts used in charge pump reference circuit. All the diodes in circuit are schottky type.

The output voltage of charge pump (VSS) determined by following formula.

$VSS = V_{FB5}^{*} - (R0/R1) \cdot (V_{REFO}^{*} - V_{FB5}^{*})$
$\approx 0.8 - (R0/R1) \cdot (1.2 - 0.8)$
*V_{FB5} = 0.8V @ typical
*V_{REFO} = 1.2V @ typical

For example, if R0 = 95KΩ, R1 = 5.6 KΩ then charge pump output voltage in typical condition is:
0.8 – (95K/5.6 K) · (1.2-0.8) = - 5.98 V

A Schottky diode should be used for the diode string.
They have a low equivalent resistance, a low forward voltage drop and a breakdown voltage more than 20V for reducing the power loss.MBR0530, 1N5817 or equivalent can be used.
For applications that are cost driven, the 1N4818 or equivalent can be used but the power efficiency will be reduced.

Low ESR capacitors should be used to minimize the switching output ripple voltage.

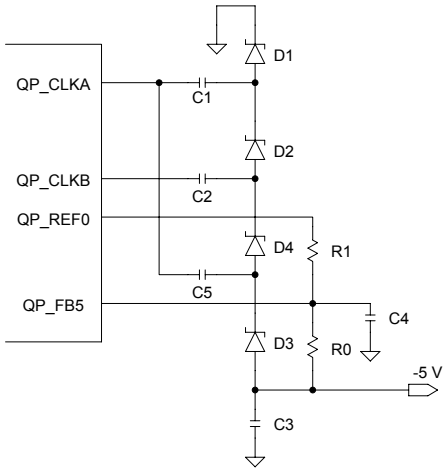


Figure 30: Charge pump application circuit for VDDA_QP up to 3.3V

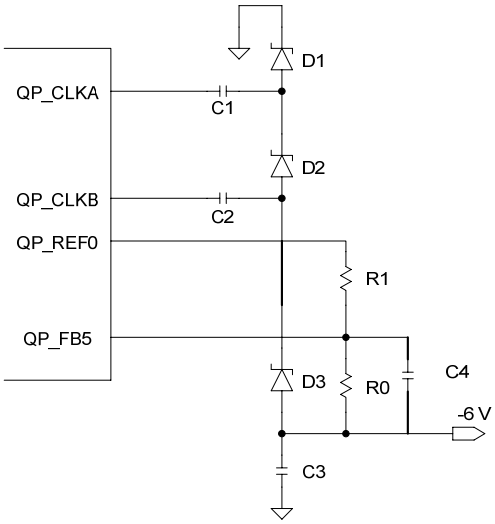


Figure 31: Charge pump application circuit for VDDA_QP over 3.3V

Name	Value	Unit
C1	0.1	µF
C2	0.1	µF
C3	10	µF
C4	10	nF
R0	95	KΩ
R1	5.6	KΩ

Table 3: Charge pump part list

4-5. Backlight Driver

The A230 has two current sink based backlight driver for driving led backlight. Refer to Figure 32 for backlight driver reference circuit.
The driving current for full on condition can be calculated by the following formula:

$I_{BLD\_OUT} = 1.25(V_{BANDGAP})/R0 * 200$

For example, set to backlight driver drives 10mA current for backlight, use 25 KΩ register for R0.
1.25 / 25K * 200 = 0.01 = 10mA

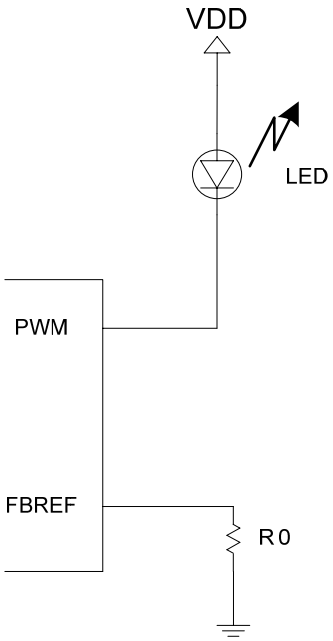


Figure 33. Backlight current sink reference circuit

5. Register Description

Address	Bit	Name	Default	Description
00H	7:6	SepSync	0	"00" – All embedded Sync. "10" – Separate V-Sync. "01" – Separate H-Sync. "11" – All Separate Sync.
	5:4	ColorSpace	0	"0X" – YCbCr "10" – RGB(8,8,8) "11" – RGB(5,6,5)
	3	Vid16	0	"0" – 8bit video, "1" – 16bit video
	2:1	VideoType	0	"00" – 13.5MHz Sampling Video (4:3/16:9) "01" – 12.27MHz Sampling Video (4:3/16:9, Square) "10" – 18MHz Sampling Video (16:9) "11" – 16.36MHz Sampling Video (16:9, Square)
	0	NTSC/PAL	0	"0" – NTSC "1" – PAL
01H	2	VSyncPol	0	External Sync. Polarity
	1	HSyncPol	0	"0" – Active High
	0	DvalidPol	0	"1' – Active Low
02H	3:0	ClkInDly	0H	Video clk delay
03H	1:0	HSdly	1	HS Input delay adjustment (Separate H-Sync. Mode)
04H	0	TestPatt	0	"0" – External Video Input Select "1" – Internal Video Pattern Gen. Select (Color Bar)
05H	6:4	DotOVRD	000	Dot-scaling override "0XX" – use automatic dot-scaling, same as A221 "100" – 2:1 dot-scaling "101" – 2:3 dot-scaling "110" – 5:9 dot-scaling "111" – 5:12 dot-scaling
	3:1	PreOVRD	000	Pre-scaling override "0XX" – use automatic pre-scaling, same as A221 "100" – 11:10 pre-scaling "101" – 9:8 pre-scaling "110" – 6:5 pre-scaling "111" – No pre-scaling
	0	PreScale	0	Std. NTSC/PAL Video Pre-scaling select "0" – Scaling "1" – 9:8 Scaling
06H	7:0	HSpos	1EH	Horizontal position (Number of blinking Pixels) (Value range from 0 to 254)
07H	7:0	VSpos0	0DH	Vertical position – Number of "Field 0" blinking lines (Value range from 0 to 254)
08H	7:0	VSpos1	0DH	Vertical position – Number of "Field 1" blinking lines (Value range from 0 to 254)
09H	7	IntOVRD	0	"0" – Use external sync signals for access frame buffer "1" – Use generated signals for access frame buffer
	6	native	0	'0' – don't select native mode '1' – native mode enable
	5:2			Reserved
	1:0	DclkOVRD	00	"00" – use automatic clock selection, same as A221 "01" – select 2:1 clock for display panel interface "10" – select 3:2 clock for display panel interface

				“11” – select 1:1 clock for display panel interface
0AH-0EH				Reserved
0FH	7:2			Reserved
	1	GPR1	1	General Purpose Output 1
	0	GPR0	1	General Purpose Output 0
10H	5	Disp43	0	“0” – 152K, 308K Display Select “1’ – 113K, 230K Display Select
	4	BlueScr	1	“0” – Video Screen “1” – Blue Screen
	3	T2Bscan	0	“0” – Top to Bottom Scan “1” – Bottom to Top Scan
	2	L2Rscan	0	“0” – Left to Right Scan “1” – Right to Left Scan
	1:0	DispType	11	“00” – 3:2 scaling for CyberDisplay® 230K, 308K “01” – 2:1 scaling for CyberDisplay® 230K, 308K “10” – 5:9 scaling for CyberDisplay® 113K, 152K “11” – 5:12 scaling for CyberDisplay® 113K, 152K
11H	2:0	DACCC	100	DAC Current Control
12H	1	DIG_DWN	0	Digital Power Down (except I2C block) when “1”
	0	PAD_DWN	0	PAD Power Down when “1”
13H	7			Reserved
	6	DAC_TST	0	DAC Test Mode
	5	DAC_DWN	0	DAC/AMP Power Down: “0”:Enable, “1”:Power Down
	4	QP_DWN	0	Q-Pump Power Down: “0”: Enable, “1”: Power Down
	3:2			Reserved
	1	PWM_ENB	0	PWM Enable: “0”: Enable, “1”: Power Down
	0			Reserved
14H	7:0	Contrast	80H	Y contrast value (0x ~ 1.99x)
15H	7:0	Brightness	00H	Y brightness value (-128 ~ 127)
16H	1:0	YAPSC	0	Sharpness Noise Slice Control “00” – x 0 , “01” – x ¼ “10” – x ½ , “11” – x 1
17H	7:0	YAPTH	FFH	Sharpness Noise Slice TH Value
18H	7:0	YAPG	80H	Sharpness filter gain (0x ~ 1.99x)
19H	7:0	ClipPlus	00H	Sharpness Noise Slice TH Value
1AH	7:0	ClipMinus	00H	Sharpness Filter Minus Level Clip : 00H(0) ~ FFH(255)
1BH	7:0	GainCb	80H	Cb Gain (0x ~ 1.99x)
1CH	7:0	GainCr	80H	Cr Gain (0x ~ 1.99x)
1DH	7:0	PWM0[11:4]	80H	Higher 8 bit of PWM0
1EH	7:0	PWM1[11:4]	80H	Higher 8 bit of PWM1
1FH	7:4	PWM1[3:0]	1	Lower 4 bit of PWM1
	3:0	PWM0[3:0]	1	Lower 4 bit of PWM0
20H	4	GainSel	0	R, ,G, B Gain range select “0” – 0X ~ 1.99X range select “1” – 0X ~ 3.99X range select
	3	VegSel	0	V-sync. Active Edge Select “0” – Falling edge select when Active High V-sync. Polarity Mode “1” – Rising edge select when Active High V-sync. Polarity Mode

	2	DrvWhite	0	Drive-to-White Select
	1:0	DAC_Dly	1	DAC Delay (No of DAC clocks)
21H				Reserved
22H	7:0	Y_low	10H	Y Signal Low Limit
23H	7:0	Y_high	EBH	Y Signal High Limit
24H	7:0	Cx_low	10H	Cb, Cr Signal Low Limit
25H	7:0	Cx_high	F0H	Cb, Cr Signal High Limit
26H	7:0	CSCC1[7:0]	2AH	Lower 8 bit of Color Space Conversion Coefficient 1 1.164 (1.164*256=297.984 -> 12AH)
27H	1:0	CSCC1[9:8]	1H	Higher 2 bit of Color Space Conversion Coefficient 1
28H	7:0	CSCC2[7:0]	98H	Lower 8 bit of Color Space Conversion Coefficient 2 1.596 (1.596*256=408.576 -> 198H)
29H	1:0	CSCC2[9:8]	1H	Higher 2 bit of Color Space Conversion Coefficient 2
2AH	7:0	CSCC3[7:0]	D0H	Lower 8 bit of Color Space Conversion Coefficient 3 – 0.813 (0.813*256=208.128 -> 0D0H)
2BH	1:0	CSCC3[9:8]	0H	Higher 2 bit of Color Space Conversion Coefficient 3
2CH	7:0	CSCC4[7:0]	64H	Lower 8 bit of Color Space Conversion Coefficient 4 0.392 (0.392*256=100.352 -> 064H)
2DH	1:0	CSCC4[9:8]	0H	Higher 2 bit of Color Space Conversion Coefficient 4
2EH	7:0	CSCC5[7:0]	04H	Lower 8 bit of Color Space Conversion Coefficient 5 2.017 (2.017*256=516.352 -> 204H)
2FH	1:0	CSCC5[9:8]	2H	Higher 2 bit of Color Space Conversion Coefficient 5
30H	7:0	CTRL_HIGH[7:0]	21H	Extra control signal set to high when internal counter reached this point. Lower 8 bit of extra control bit turn on value
31H	1:0	CTRL_HIGH[9:8]	0H	Higher 2 bit of extra control bit turn on value
32H	7:0	CTRL_LOW[7:0]	40H	Extra control signal set to low when internal counter reached this point. Lower 8 bit of extra control bit turn off value
33H	1:0	CTRL_LOW[9:8]	0H	Higher 2 bit of extra control bit turn off value
34H	7	FlipEn	0	“0” – use display base horizontal flip “1” – use line buffer base horizontal flip
	6:1			Reserved
	1:0	INST	00	Control INV bit “00” – INV1 set to ‘0’ “01” – INV1 set to ‘1’ “10” – INV1 same as polarity “11” – INV1 is inverted polarity
35H	7	INVINV	0	0: Disables inversion mode for RGB111 mode 1: Enables inversion mode for RGB111 mode
	6:0			Reserved
36H	7:0	BkUpStartL[7:0]		Forward read start address while using line buffer base horizontal flip. Lower 8 bit of forward start address
37H	1:0	BkUpStartL[1:0]		Higher 2 bit of forward stat address
38H	7:0	BkDnStartL[7:0]		Reverse read start address while using line buffer base horizontal flip. Lower 8 bit of reverse start address
39H	1:0	BkDnStartL[1:0]		Higher 2 bit of reverse start address
3AH-3EH				Reserved

3FH	7:4	DrvStrCK	8H	The output strength for the display clock VID_CK0 and VID_CK1, '0' - no drive, '15' - strongest
	3:0	DrvStrET	8H	The output strength for other display control signal VID*, same strength control as DrvStrCk.
40H	3:0	dclkSkip	2H	Display clock skip mode register used for control internal data transfer. For example, every third data is skipped if the register value is 2.
41H	7:0	WHS	1DH	DIS_HS Width
42H	7:0	WSP	25H	CK0 Start Position
43H				Reserved
44H	7:0	DispPixel[7:0]	0EFH	Lower 8 bit of Number of Display Pixel – 1
45H	1:0	DispPixel[9:8]	0EFH	Higher 2 bit of Number of Display Pixel – 1
46H	7:0	VidStartP[7:0]	005H	Lower 8 bit of Display Data Start Point (CKx number)
47H	1:0	VidStartP[9:8]	005H	Higher 2 bit of Display Data Start Point
48H	7:0	VidEndP[7:0]	0EEH	Lower 8 bit of Display Data End Point (CKx number)
49H	1:0	VidEndP[9:8]	0EEH	Higher 2 bit of Display Data End Point
4AH	7	InvMem	0	Invert frame buffer clock when high
	6:0			Reserved
4BH				Reserved
4CH	7	HIGH_LOW_EN	0	0: Disables 1 bit mode of DAC/AMP 1: Enables 1 bit mode of DAC/AMP
	6		0	Reserved
	5:2	FBVideoType	0	Video type in frame buffer memory "0000" – RGB565 "0001" – ARGB4444 "0010" – RGBA4444 "0011" –ARGB1555 "0100" –RGBA5551 "0101" – RGB332 (01 pixel order) "0110" – RGB332 (10 pixel order) "0111" – RGB111 (0123 pixel order) "1000" – RGB111 (2301 pixel order)
	1:0	DispVidSel	00	"00" – Display BT656 video "01" – Display frame buffer video "10" – Display blended video "11" – Reserved
4DH	7:4	AlphaBlend	0H	Alpha blending level
	3:1			Reserved
	0	SelAlpha	0	Alpha blending parameter selector "0" – Control alpha blending by 'AlphaBlend' register "1" – Control alpha blending by the frame buffer memory data or the alpha parameter in window control register
4EH				Reserved
4FH	1:0	SelColor	00	Gamma LUT color selection "00" – all three color "01" – red "10" – green "11" – blue
50H	7:0	LUT_H_00	FFH	Gamma correction positive channel Look Up Table 1
51H	7:0	LUT_H_01	EFH	Gamma correction positive channel Look Up Table 1
52H	7:0	LUT_H_02	DFH	Gamma correction positive channel Look Up Table 2
53H	7:0	LUT_H_03	CFH	Gamma correction positive channel Look Up Table 3
54H	7:0	LUT_H_04	BFH	Gamma correction positive channel Look Up Table 4

55H	7:0	LUT_H_05	AFH	Gamma correction positive channel Look Up Table 5
56H	7:0	LUT_H_06	9FH	Gamma correction positive channel Look Up Table 6
57H	7:0	LUT_H_07	8FH	Gamma correction positive channel Look Up Table 7
58H	7:0	LUT_H_08	7FH	Gamma correction positive channel Look Up Table 8
59H	7:0	LUT_H_09	6FH	Gamma correction positive channel Look Up Table 9
5AH	7:0	LUT_H_10	5FH	Gamma correction positive channel Look Up Table 10
5BH	7:0	LUT_H_11	4FH	Gamma correction positive channel Look Up Table 11
5CH	7:0	LUT_H_12	3FH	Gamma correction positive channel Look Up Table 12
5DH	7:0	LUT_H_13	2FH	Gamma correction positive channel Look Up Table 13
5EH	7:0	LUT_H_14	1FH	Gamma correction positive channel Look Up Table 14
5FH	7:0	LUT_H_15	0FH	Gamma correction positive channel Look Up Table 15
60H	7:0	LUT_H_16	00H	Gamma correction positive channel Look Up Table 16
61H				Reserved
62H	7:0	LUT_L_00	00H	Gamma correction negative channel Look Up Table 0
63H	7:0	LUT_L_01	0FH	Gamma correction negative channel Look Up Table 1
64H	7:0	LUT_L_02	1FH	Gamma correction negative channel Look Up Table 2
65H	7:0	LUT_L_03	2FH	Gamma correction negative channel Look Up Table 3
66H	7:0	LUT_L_04	3FH	Gamma correction negative channel Look Up Table 4
67H	7:0	LUT_L_05	4FH	Gamma correction negative channel Look Up Table 5
68H	7:0	LUT_L_06	5FH	Gamma correction negative channel Look Up Table 6
69H	7:00	LUT_L_07	6FH	Gamma correction negative channel Look Up Table 7
6AH	7:0	LUT_L_08	7FH	Gamma correction negative channel Look Up Table 8
6BH	7:0	LUT_L_09	8FH	Gamma correction negative channel Look Up Table 9
6CH	7:0	LUT_L_10	9FH	Gamma correction negative channel Look Up Table 10
6DH	7:0	LUT_L_11	AFH	Gamma correction negative channel Look Up Table 11
6EH	7:0	LUT_L_12	BFH	Gamma correction negative channel Look Up Table 12
6FH	7:0	LUT_L_13	CFH	Gamma correction negative channel Look Up Table 13
70H	7:0	LUT_L_14	DFH	Gamma correction negative channel Look Up Table 14
71H	7:0	LUT_L_15	EFH	Gamma correction negative channel Look Up Table 15
72H	7:0	LUT_L_16	FFH	Gamma correction negative channel Look Up Table 16
73H-7FH				Reserved
80H	7	W1_EN	1	Window 1 enable
	3:0	W1_Alpha	8H	Window 1 alpha value
81H	7:0	W1_X[7:0]	00H	Lower 8 bit of X position for window 1
82H	6:0			Reserved
	0	W1_X[8]	0	MSB of X position for window 1
83H	7:0	W1_Y	0	Y position for window 1
84H	7:0	W1_W[7:0]	40H	Lower 8 bit of window 1 width
85H	6:0			Reserved
	0	W1_W[8]	1	MSB of windows 1 width
86H	7:0	W1_H	F0H	Window 1 height
87H				Reserved
88H	7	W2_EN	0	Window 2 enable
	3:0	W2_Alpha	0H	Window 2 alpha value
89H	7:0	W2_X[7:0]	00H	Lower 8 bit of X position for window 2
8AH	6:0			Reserved
	0	W2_X[8]	0	MSB of X position for window 2

8BH	7:0	W2_Y	0	Y position for window 2
8CH	7:0	W2_W[7:0]	00H	Lower 8 bit of window 2 width
8DH	6:0			Reserved
	0	W2_W[8]	0	MSB of windows2 width
8EH	7:0	W2_H	00H	Window 2 height
8FH				Reserved
90H	7	W3_EN	0	Window 3 enable
	3:0	W3_Alpha	0H	Window 3 alpha value
91H	7:0	W3_X[7:0]	00H	Lower 8 bit of X position for window 3
92H	6:0			Reserved
	0	W3_X[8]	0	MSB of X position for window 3
93H	7:0	W3_Y	0	Y position for window 3
94H	7:0	W3_W[7:0]	00H	Lower 8 bit of window 3 width
95H	6:0			Reserved
	0	W3_W[8]	0	MSB of window 3 width
96H	7:0	W3_H	00H	Window 3 height
97H				Reserved
98H	7	W4_EN	0	Window 4 enable
	3:0	W4_Alpha	0H	Window 4 alpha value
99H	7:0	W4_X[7:0]	00H	Lower 8 bit of X position for window 4
9AH	6:0			Reserved
	0	W4_X[8]	0	MSB of X position for window 4
9BH	7:0	W4_Y	0	Y position for window 4
9CH	7:0	W4_W[7:0]	00H	Lower 8 bit of window 4 width
9DH	6:0			Reserved
	0	W4_W[8]	0	MSB of windows 4 width
9EH	7:0	W4_H	00H	Window 4 height
9FH				Reserved
A0H	7:0	W1_START[7:0]	00H	Lower 8 bit of window 1 buffer start address
A1H	7:0	W1_START[15:8]	00H	Middle 8 bit of window 1 buffer start address
A2H	7:1			Reserved
	0	W1_START[16]	0	MSB of window 1 buffer start address
A3H				Reserved
A4H	7:0	W2_START[7:0]	00H	Lower 8 bit of window 2 buffer start address
A5H	7:0	W2_START[15:8]	00H	Middle 8 bit of window 2 buffer start address
A6H	7:1			Reserved
	0	W2_START[16]	0	MSB of window 2 buffer start address
A7H				Reserved
A8H	7:0	W3_START[7:0]	00H	Lower 8 bit of window 3 buffer start address
A9H	7:0	W3_START[15:8]	00H	Middle 8 bit of window 3 buffer start address
AAH	7:1			Reserved
	0	W3_START[16]	0	MSB of window 3 buffer start address
ABH				Reserved
ACH	7:0	W4_START[7:0]	00H	Lower 8 bit of window 4 buffer start address
ADH	7:0	W4_START[15:8]	00H	Middle 8 bit of window 4 buffer start address
AEH	7:1			Reserved
	0	W4_START[16]	0	MSB of window 4 buffer start address

AFH				Reserved
B0H	7:0	MemInitVal[7:0]	00H	Lower 8 bit of memory initialize value
B1H	7:0	MemInitVal[15:8]	00H	Higher 8 bit of memory initialize value
B2H	7:1			Reserved
	0	InitStart	0	Write '1' to initiate memory initialize process
B3H	7:2			Reserved
	1	I80_16bit	0	Intel 80 bus width selection "0" – 8bit "1" – 16 bit
	0	DirectFB	0	Intel 80 bus addressing mode selection "0" – Indirect Addressing "1" – Direct Addressing
B4H-B8H				Reserved
B9H	0	FB_Address[16]	0	MSB of Frame buffer write start address
BAH	7:0	FB_Address[15:8]	00H	Middle 8 bit of Frame buffer write start address
BBH	7:0	FB_Address[7:0]	00H	Lower 8 bit of Frame buffer write start address
BCH	7:0	FB_Data[7:0]	00H	Lower 8 bit of Frame buffer write data
BDH	7:0	FB_Data[15:8]	00H	Higher 8 bit of Frame buffer write data
BEH-CEH				Reserved
CFH	7:0	FB_DATA2	00H	The data for frame buffer (burst mode alternate)

Table 4. Configuration registers

Pin Description

Name	Type	# of pins	IO Supply	Description
SEN	IN	1	VDD_SC	Enable signal for 3-wire (tied high for I2C mode)
SDA	IN/OUT	1	VDD_SC	Serial data input/output for I2C/3-wire
SCL	IN	1	VDD_SC	Serial clock input for I2C/3-wire
SI_SEL	IN	1	VDD_SC	Serial interface mode selection ('Low' - 3-wire, 'High' - I2C)
I2C_Addr	IN	2	VDD_SC	I2C Sub-address selection
TESTMODE	IN	1	VDD_SC	Test mode select. Connect to 'Low' for normal operation
ResetB	IN	1	VDD_SC	System reset in low active
I80_CAEN	IN	1	VDD_IO80	Configuration register access selection ('Low' - serial bus, 'High' - I80 bus)
A16	IN	1	VDD_IO80	Intel 80 bus address MSB(bit 16)
AD	IN/OUT	16	VDD_IO80	Intel80 bus address/data bus
ALEEN	IN	1	VDD_IO80	Intel 80 bus address latch type selection ('Low' – DCn work as indicator, 'High' – DCn work as high active strobe)
DCn	IN	1	VDD_IO80	Intel80 bus address latch strobe / indicator
WRn	IN	1	VDD_IO80	Intel80 bus write strobe
RDn	IN	1	VDD_IO80	Intel80 bus read strobe
CSn	IN	1	VDD_IO80	Intel 80 bus enable
TE	Out	1	VDD_IO80	Indicator for tear-effect
CLK	IN	1	VDD_IO	Video clock
YIN	IN	8	VDD_IO	Digital video YiInput
CIN	IN	8	VDD_IO	Digital video CbCr input
VS	IN	1	VDD_IO	Vertical sync
HS	IN	1	VDD_IO	Horizontal sync (Should be tied to high for frame buffer only mode)
DVALID	IN	1	VDD_IO	Data valid
DIS_CK0	OUT	1	VDD_DIS	Pixel clock output to display
DIS_CK1	OUT	1	VDD_DIS	Pixel clock output to display
DIS_HS	OUT	1	VDD_DIS	Horizontal sync output to display
DIS_VS	OUT	1	VDD_DIS	Vertical sync output to display
DIS_INV	OUT	1	VDD_DIS	White level indicator / instruction signal
DIS_I2	OUT	1	VDD_DIS	Extra instruction signal to display
DIS_SLEEP	OUT	1	VDD_DIS	Sleep control to display. If DIG_DWN, PAD_DWN or DAC_DWN bits are set that makes the DIS_SLEEP output to go low
DIS_RGT	OUT	1	VDD_DIS	Horizontal scan direction control to display
DIS_DWN	OUT	1	VDD_DIS	Vertical scan direction control to display

GPR1	OUT	1	VDD_DIS	General purpose register 1 output
GPR0	OUT	1	VDD_DIS	General purpose register 0 output
VOUT_R	OUT	1	VDDA_AMP	Red video signal output
VOUT_G	OUT	1	VDDA_AMP	Green video signal output
VOUT_B	OUT	1	VDDA_AMP	Blue video signal output
DAC_VREF	Analog	1	VDDA_DAC	Voltage reference for DAC
COMP	Analog	1	VDDA_DAC	connect 0.1u Cap. to VDDA_DAC
QP_CLKA	Analog	1	VDDA_QP	Charge pump pulse output A
QP_CLKB	Analog	1	VDDA_QP	Charge pump pulse output B
QP_REFO	Analog	1	VDDA_QP	Charge pump reference voltage output
QP_FB5	Analog	1	VDDA_QP	Charge pump voltage feedback
FBREF	Analog	1	VDDA_BLD	Tie to the resistor for sink current setting
PWM1	Analog	1	VDDA_BLD	Open drain output, tie to the cathod of LED
PWM0	Analog	1	VDDA_BLD	Open drain output, tie to the cathod of LED
VSS_CORE	GND	6		Digital GND for core logic
VDD_CORE	Power	6		Digital power for core logic
VSS_IO	GND	1		Digital GND for video interface
VDD_IO	Power	1		Digital power for video interface
VSS_IO80	GND	2		Digital GND for Intel80 bus
VDD_IO80	Power	2		Digital power for Intel80 bus
VSS_DIS	GND	2		Digital GND for display IO
VDD_DIS	Power	2		Digital power for display IO
VSS_SC	GND	1		Digital GND serial interface
VDD_SC	Power	1		Digital power for serial interface
VSSA_AMP	GND	1		Analog ground for DAC/AMP
VDDA_AMP	Power	1		Analog power for DAC/AMP
VSSA_DAC	GND	1		Analog ground for DAC/AMP
VDDA_DAC	Power	1		Analog power for DAC/AMP
VSSA_LDO	GND	1		Analog ground for LDO
VDDA_LDO	Power	1		Analog power for LDO
VSSA_QP	GND	1		Analog ground for charge pump
VDDA_QP	Power	1		Analog power for charge pump
VSSA_BLD	GND	1		Analog ground for backlight current sink
VDDA_BLD	Power	1		Analog power for backlight current sink
VSSA_REF	GND	1		Analog ground for reference generator
VDDA_REF	Power	1		Analog power for reference generator
VOUT1V8	Power Out	1		1.8V power output from LDO

Table 5. Pin summary

Pin Allocation

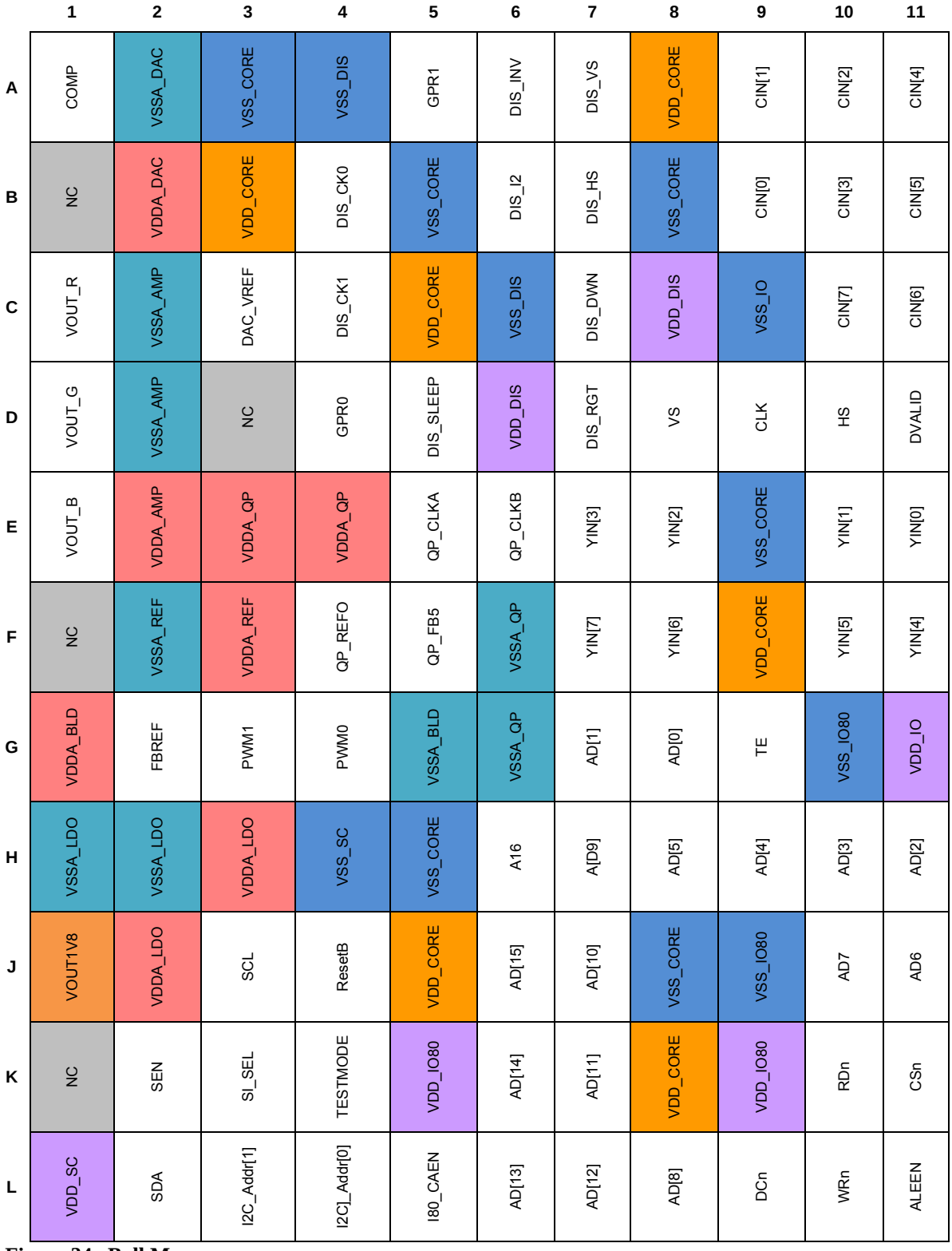
PIN No.	Ball No.	Pin Name	Type	Description
1	D2,C2	VSSA_AMP	Ground	Ground for AMP
2	C1	VOUT_R		RED Signal Output
3	D1	VOUT_G		GREEN Signal Output
4	E1	VOUT_B		BLUE Signal Output
5	E2	VDDA_AMP	Power	Power for AMP
6	E3,E4	VDDA_QP	Power	Power for charge pump
7	E5	QP_CLKA		Charge Pump Pulse Output
8	E6	QP_CLKB		Charge Pump Pulse Output
9	F6,G6	VSSA_QP	Ground	Ground for charge pump
10	F5	QP_FB5		Charge Pump Voltage Feedback
11	F4	QP_REFO		Charge Pump Ref. Vlotage Output
12	F3	VDDA_REF	Power	Power for reference voltage generator
13	F2	VSSA_REF	Ground	Ground for reference voltage generator
14	G1	VDDA_BLD	Power	Power for backlight current sink
15	G2	FBREF		Tie to the resistor for sink current setting
16	G3	PWM1		Open Drain output,Tie to the chthod of LED
17	G4	PWM0		Open Drain output,Tie to the chthod of LED
18	G5	VSSA_BLD	Ground	Ground for backlight current sink
19	H1,H2	VSSA_LDO	Ground	Ground for LDO
20	J2,H3	VDDA_LDO	Power	Power for LDO
21	J1	VOUT1V8	Power Out	1.8V Out
22	L1	VDD_SC	Power	Digital Power for serial interface
23	K2	SEN	IN	Enable signal for 3-Wire (Tied high for I2C mode)
24	L2	SDA	IN/OUT	Serial Data Input/Output for I2C/3-Wire
25	J3	SCL	IN	Serial Clock Input for I2C/3_Wire
26	K3	SI_SEL	IN	Serial Interface Mode Selection (‘Low’ - 3-Wire, ‘High’ - I2C)
27	L3	I2C_Addr[1]	IN	I2C Sub-Address Selection
28	L4	I2C_Addr[0]	IN	I2C Sub-Address Selection
29	K4	TESTMODE	IN	Test mode select. Connect to ‘Low’ for normal operation
30	J4	ResetB	IN	System Reset in Low Active
31	H4	VSS_SC	Ground	Digital Ground
32	H5	VSS_CORE	Ground	Digital Ground
33	J5	VDD_CORE	Power	Power for core logic
34	K5	VDD_IO80	Power	Digital Power for Intel 80 bus
35	L5	I80_CAEN	IN	Configuration register access (‘Low’ - Serial, ‘High’ - I80)
36	H6	A16	IN	Intel 80 bus address MSB(bit 16) input
37	J6	AD[15]	IN/OUT	Intel80 bus address/data
38	K6	AD[14]	IN/OUT	Intel80 bus address/data
39	L6	AD[13]	IN/OUT	Intel80 bus address/data
40	L7	AD[12]	IN/OUT	Intel80 bus address/data
41	K7	AD[11]	IN/OUT	Intel80 bus address/data
42	J7	AD[10]	IN/OUT	Intel80 bus address/data
43	H7	AD[9]	IN/OUT	Intel80 bus address/data

44	J8	VSS_CORE	Ground	Digital Ground
45	K8	VDD_CORE	Power	Power for core logic
46	L8	AD[8]	IN/OUT	Intel80 bus address/data
47	J9	VSS_IO80	Ground	Digital Ground
48	K9	VDD_IO80	Power	Digital Power for Intel 80 bus
49	L9	DCn	IN	Intel80 bus address latch / indicator
50	L10	WRn	IN	Intel80 bus write strobe
51	L11	ALEEN	IN	Intel80 bus address latch selector
52	K10	RDn	IN	Intel80 bus read strobe
53	K11	CSn	IN	Intel 80 bus enable
54	J10	AD[7]	IN/OUT	Intel80 bus address/data
55	J11	AD[6]	IN/OUT	Intel80 bus address/data
56	H8	AD[5]	IN/OUT	Intel80 bus address/data
57	H9	AD[4]	IN/OUT	Intel80 bus address/data
58	H10	AD[3]	IN/OUT	Intel80 bus address/data
59	H11	AD[2]	IN/OUT	Intel80 bus address/data
60	G7	AD[1]	IN/OUT	Intel80 bus address/data
61	G8	AD[0]	IN/OUT	Intel80 bus address/data
62	G9	TE	Out	Indicator for tear-effect
63	G10	VSS_IO80	Ground	Digital Ground
64	G11	VDD_IO	Power	Digital Power for IO
65	F7	YIN[7]	IN	Digital Video Y Input
66	F8	YIN[6]	IN	Digital Video Y Input
67	F9	VDD_CORE	Power	Power for core logic
68	F10	YIN[5]	IN	Digital Video Y Input
69	F11	YIN[4]	IN	Digital Video Y Input
70	E7	YIN[3]	IN	Digital Video Y Input
71	E8	YIN[2]	IN	Digital Video Y Input
72	E9	VSS_CORE	Ground	Digital Ground
73	E10	YIN[1]	IN	Digital Video Y Input
74	E11	YIN[0]	IN	Digital Video Y Input
75	D8	VS	IN	Verical Sync
76	D9	CLK	IN	Video Clock Input
77	D10	HS	IN	Horizontal Sync
78	D11	DVALID	IN	Data Valid
79	C10	CIN[7]	IN	Digital Video CbCr Input
80	C11	CIN[6]	IN	Digital Video CbCr Input
81	B11	CIN[5]	IN	Digital Video CbCr Input
82	A11	CIN[4]	IN	Digital Video CbCr Input
83	B10	CIN[3]	IN	Digital Video CbCr Input
84	A10	CIN[2]	IN	Digital Video CbCr Input
85	A9	CIN[1]	IN	Digital Video CbCr Input
86	B9	CIN[0]	IN	Digital Video CbCr Input
87	C9	VSS_IO	Ground	Digital Ground
88	A8	VDD_CORE	Power	Power for core logic
89	B8	VSS_CORE	Ground	Digital Ground
90	C8	VDD_DIS	Power	Power for Display Interface IO
91	D7	DIS_RGT	OUT	Horizontal Scan Direction Control to Display
92	C7	DIS_DWN	OUT	Vertical Scan Direction Control to Display

93	B7	DIS_HS	OUT	Horizontal Sync Output to Display
94	A7	DIS_VS	OUT	Vertical Sync Output to Display
95	A6	DIS_INV	OUT	White Level Indicator / Instruction signal
96	B6	DIS_I2	OUT	Extra Instruction Signal to Display
97	A4	VSS_DIS	Ground	Digital Ground
98	D6	VDD_DIS	Power	Power for Display Interface IO
99	D5	DIS_SLEEP	OUT	Sleep control to display. If any of the power down bits are set that makes the DIS_SLEEP output to go low
100	C5	VDD_CORE	Power	Power for core logic
101	B5	VSS_CORE	Ground	Digital Ground
102	A5	GPR1	OUT	General Purpose Register1 Output
103	D4	GPR0	OUT	General Purpose Register0 Output
104	C4	DIS_CK1	OUT	Pixel Clock Output to Display
105	B4	DIS_CK0	OUT	Pixel Clock Output to Display
106	C6	VSS_DIS	Ground	Digital Ground
107	A3	VSS_CORE	Ground	Digital Ground
108	B3	VDD_CORE	Power	Power for core logic
109	C3	DAC_VREF		Vref for DAC
110	A2	VSSA_DAC	Ground	Ground for DAC
111	B2	VDDA_DAC	Power	Power for DAC
112	A1	COMP		need 0.1u Cap. To VDDA_DAC

Table 6. Pin allocation

6. Ball Map



	1	2	3	4	5	6	7	8	9	10	11
A	COMP	VSSA_DAC	VSS_CORE	VSS_DIS	GPR1	DIS_INV	DIS_VS	VDD_CORE	CIN[1]	CIN[2]	CIN[4]
B	NC	VDDA_DAC	VDD_CORE	DIS_CK0	VSS_CORE	DIS_I2	DIS_HS	VSS_CORE	CIN[0]	CIN[3]	CIN[5]
C	VOUT_R	VSSA_AMP	DAC_VREF	DIS_CK1	VDD_CORE	VSS_DIS	DIS_DWN	VDD_DIS	VSS_IO	CIN[7]	CIN[6]
D	VOUT_G	VSSA_AMP	NC	GPR0	DIS_SLEEP	VDD_DIS	DIS_RGT	VS	CLK	HS	DVALID
E	VOUT_B	VDDA_AMP	VDDA_QP	VDDA_QP	QP_CLKA	QP_CLKB	YIN[3]	YIN[2]	VSS_CORE	YIN[1]	YIN[0]
F	NC	VSSA_REF	VDDA_REF	QP_REFO	QP_FB5	VSSA_QP	YIN[7]	YIN[6]	VDD_CORE	YIN[5]	YIN[4]
G	VDDA_BLD	FBREF	PWM1	PWM0	VSSA_BLD	VSSA_QP	AD[1]	AD[0]	TE	VSS_IO80	VDD_IO
H	VSSA_LDO	VSSA_LDO	VDDA_LDO	VSS_SC	VSS_CORE	A16	A[D9]	AD[5]	AD[4]	AD[3]	AD[2]
J	VOUT1V8	VDDA_LDO	SCL	ResetB	VDD_CORE	AD[15]	AD[10]	VSS_CORE	VSS_IO80	AD7	AD6
K	NC	SEN	SI_SEL	TESTMODE	VDD_IO80	AD[14]	AD[11]	VDD_CORE	VDD_IO80	RDn	CSn
L	VDD_SC	SDA	I2C_Addr[1]	I2C_Addr[0]	I80_CAEN	AD[13]	AD[12]	AD[8]	DCn	WRn	ALEEN

Figure 34. Ball Map

7. Recommended Operating Conditions

Power Supply

Type	Name	Min	Typ	Max	Unit	Remark
Analog Power	VDDA_DAC	1.6	1.8	2	V	
	VDDA_AMP	3	4.0	4.8	V	Cannot swing rail to rail over 4.2V
	VDDA_QP	3	4.0	5	V	
	VDDA_BLD	3	4.0	5	V	
	VDDA_REF	3	4.0	5	V	
	VDDA_LDO	2.4	3.3	3.6	V	If 1.8V supply is available then VDDA_LDO may remain unconnected
Digital Power	VDD_CORE	1.6	1.8	2	V	
	VDD_IO	1.6	1.8	3.6	V	
	VDD_IO80	1.6	1.8	3.6	V	Power supply for intel80 bus
	VDD_SC	1.6	1.8	3.6	V	Power supply for serial interface (I2C/SPI)
	VDD_DIS	1.6	4.0	5	V	
Input Level	VIL			0.2*VDD_IO	V	
	VIH	0.8*VDD_IO			V	
Temperature		0		70	°C	

Table 7. Operation conditions

8. Analog block characteristics

DAC

Parameter	Conditions	MIN	TYP	MAX	UNIT
Resolution				8	Bits
Differential Linearity Error			±0.5	±1	LSB
Integral Linearity Error			±1	±2	LSB
Gain Error	D[7:0]=all high			1	%
Maximum Output Voltage	D[7:0]=all high	0.6	0.66	1.0	V
LSB Size	V_{LSB}=VOUT/255		2.59		mV
Channel Variation among R, G, B			0.2	0.5	%

Table 8. DAC characteristics

Charge Pump

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage		3.0	4.0	5.5	V
Output Voltage		-6.5	-6		V
Output Current			1	3	mA
Ripple Voltage			16		mV
Shutdown Current				1	μA
Line regulation				21	mV
Load regulation				21	mV

Table 9. Charge pump characteristics

Backlight Driver

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage			4.0		V
Output Voltage			4.0		V
Output Current				30	mA
Shutdown Current				1	μA

Table 10. Backlight current sink characteristics

LDO

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage		2.4	3.3	3.6	V
Output Voltage			1.8		V
Output Current			25		mA
Line regulation	Power drain = 5 mA ~ 30mA			35	mV
Load regulation	Power drain = 5 mA ~ 30mA			35	mV

Table 11. LDO characteristics

9. DC characteristics

	Power		Condition	Current (Min)	Current (Typ)	Current (Max)	Unit	Remark
Analog	DAC/AMP (VDDA_AMP)		4 V		2.6		mA	Not include loading power
	VDDA_REF		4V		0.2		mA	
	DAC/AMP(VDDA_DAC)		1.8 V		0.7		mA	
	Charge Pump (VDDA_QP)		4 V		2.6		mA	0.7 mA loading
	BLD (VDDA_BLD)		4 V		0.9		mA	15 mA current sink
	LDO (VDDA_LDO)		2.5 V		0.1		mA	0.1mA + power drained. May remain unconnected if not used
Digital	BT656 Video	VDD_CORE	1.8 V		10		mA	No frame buffer video. No activity on Intel 80 bus and serial bus
		VDD_SC	1.8V		0.02		mA	
		VDD_IO	1.8 V		0.01		mA	
		VDD_DIS	4 V		1.8		mA	
		VDD_IO80	1.8 V		0.01		mA	
	Blended	VDD_CORE	1.8 V		11		mA	BT656 + frame buffer video. No activity on serial bus
		VDD_SC	1.8V		0.02		mA	
		VDD_IO	1.8 V		0.01		mA	
		VDD_DIS	4 V		1.8		mA	
		VDD_IO80	1.8 V		0.03		mA	
	Frame Buffer Video	VDD_CORE	1.8V		7		mA	Only frame buffer video, no BT656 video input, No activity on serial bus
		VDD_SC	1.8V		0.02		mA	
		VDD_IO	1.8V		0.01		mA	
		VDD_DIS	4 V		1.8		mA	
		VDD_IO80	1.8V		0.03		mA	

Table 12. DC characteristics

10. AC characteristics

Video Input

The timing parameter for video input

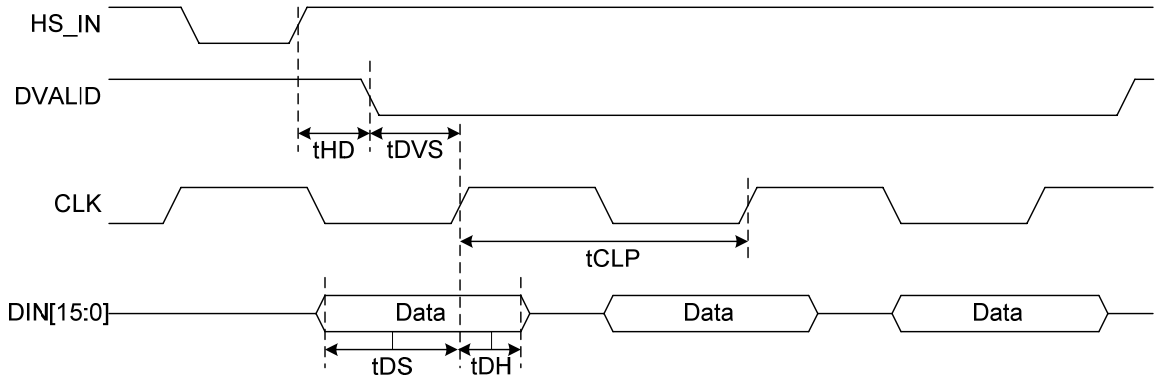


Figure 35. Video input timing

Parameter	Symbol	Min	Typ	Max	Unit
HS to DVALID hold timing	tHD	100			ns
Clock Period	tCLP	25			ns
DVALID setup timing	tDVS	10			ns
DIN setup timing	tDS	5			ns
DIN hold timing	tDH	10			ns

Table 13. Video input timing parameter

3-wire

The timing parameter for 3-wire are as dollows:.

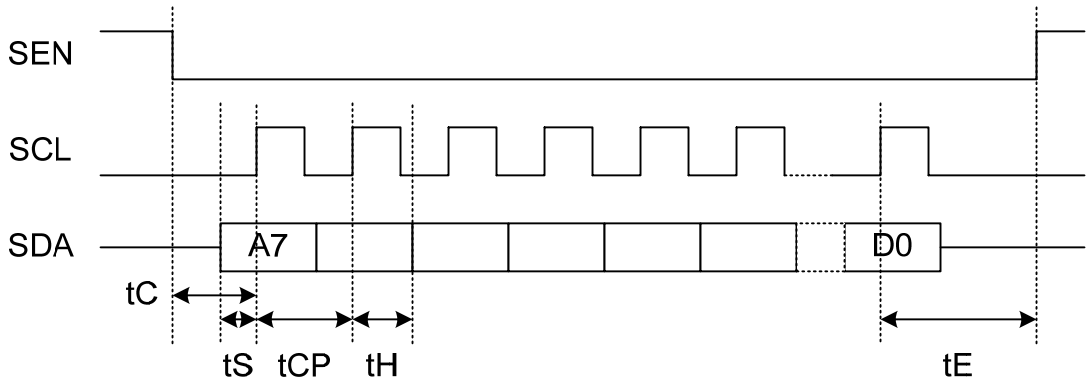


Figure 36. 3-wire timing

Parameter	Symbol	Min	Typ	Max	Unit
SPI Data setup and hold timing	tS	20			ns
	tH	20			
Clock Period	tCP	500			ns
SEN falling edge to first clock rising edge	tC	500			ns
Last clock falling edge to SEN rising edge	tE	2			us

Table 14. 3-wire timing parameters

I2C

The timing parameters for I2C are as follows:

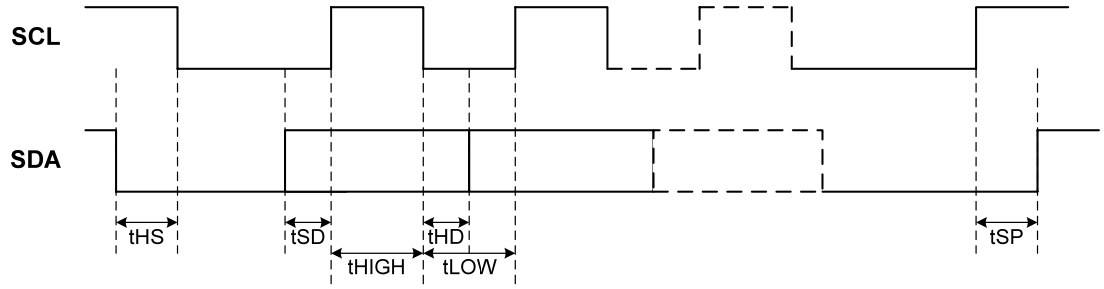


Figure 37. I2C Timing

Parameter	Symbol	Min	Typ	Max	Unit
Setup time for SDA input	tSD	200			ns
Hold time for SDA input	tHD	200			ns
Setup time for SDA output	tSD(o)	100			ns
Hold time for SDA output	tHD(o)	3			ns
High period of SCL	tHIGH	500			ns
Low period of SCL	tLow	500			ns
Hold time for START	tHS	500			ns
Setup time for STOP	tSP	500			ns

Table 15. I2C timing parameters

Intel 80 bus

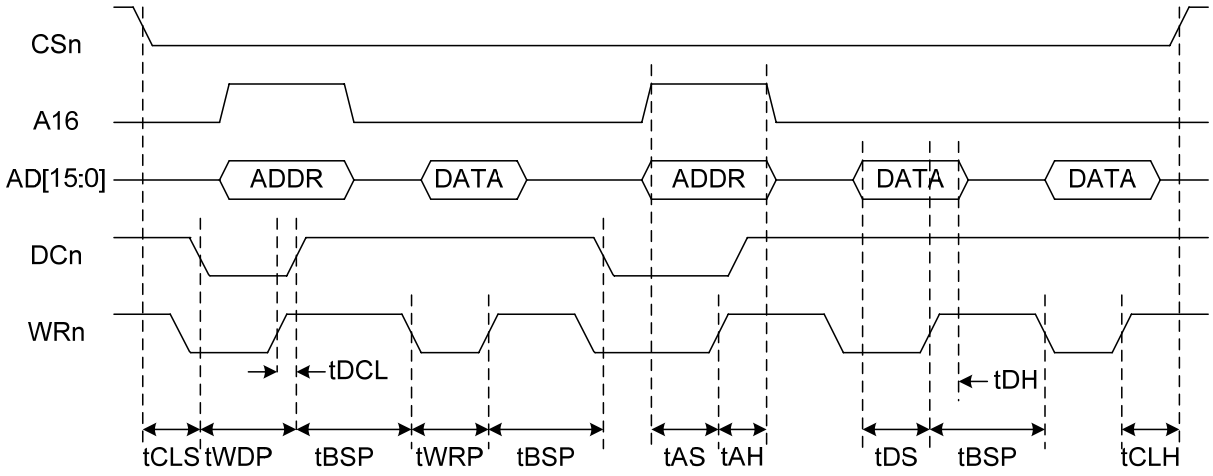


Figure 38. Intel 80 write timing (ALEEN = 0)

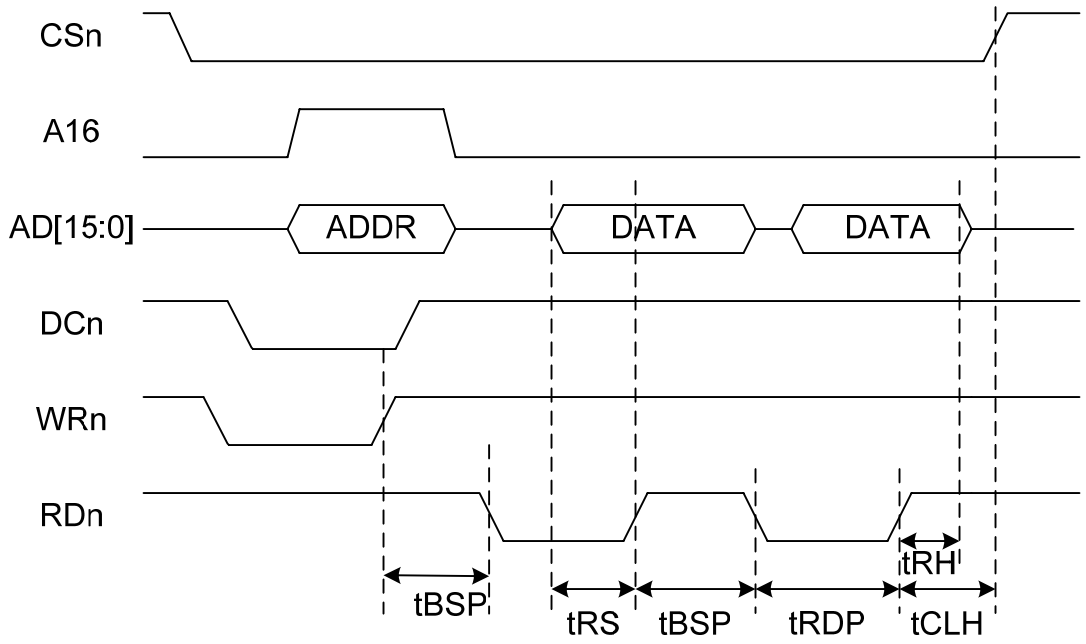


Figure 39. Intel 80 read timing (ALEEN = 0)

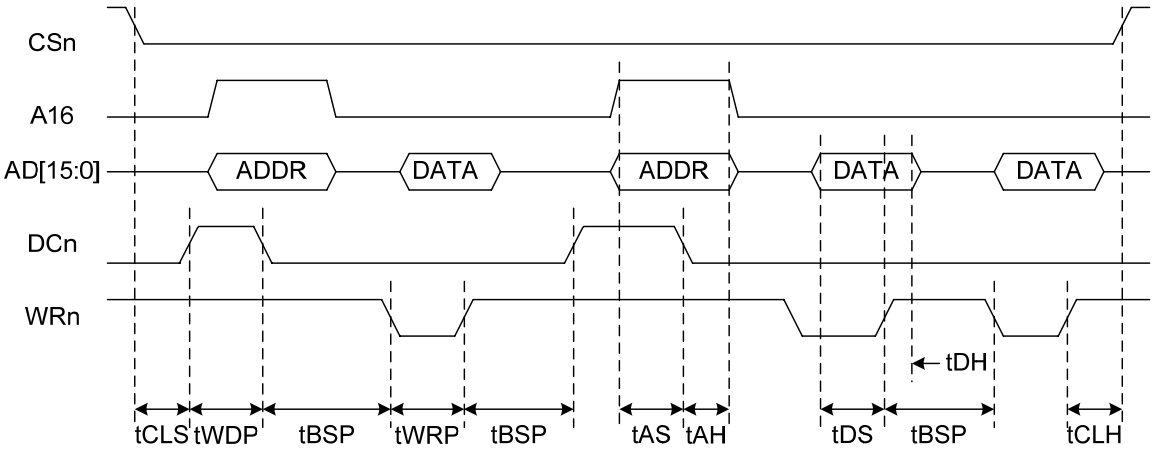


Figure 40. Intel 80 write timing (ALEEN = 1)

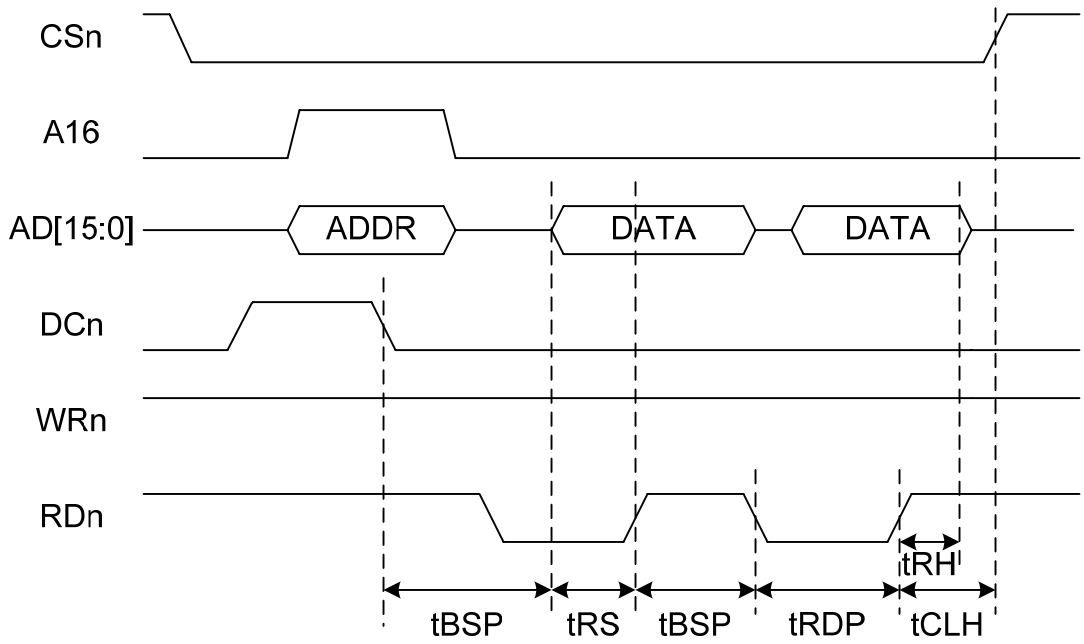


Figure 41. Intel 80 read timing (ALEEN = 1)

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Address input data setup time	tAS	1.5			Mclk*	
Address data input hold time	tAH	9			ns	
Address latch active time	tWDP	2			Mclk*	DCn and WRn is low while ALEEN = 'Low'. DCn is high while ALEEN = 'High'
Write strobe low period	tWRP	2			Mclk*	
Minimum period between two active signals	tBSP	2			Mclk*	
Address latch indicator hold time	tDCL	9			ns	Not applicable while ALEEN = 'High'
Data in setup time	tDS	1.5			Mclk*	
Data in hold time	tDH	9			ns	
Data out setup time	tRS	20			ns	
Data out hold time	tRH	10			ns	
Read strobe low period	tRDP	6			Mclk*	
Chip select setup time	tCLS	2			Mclk*	
Chip select hold time	tCLH	2			Mclk*	

*****Mclk : one period of memory clock . Mclk equals video clock (CLK) in 8 bit video input mode and 2 times the video clock in 16 bit video input mode

Table 16. Intel 80 timing parameters

11. Application Note

Power Up Sequence

The following sequence is recommended for proper working at power up. Wait 1ms between each step in power up sequence if not specified.

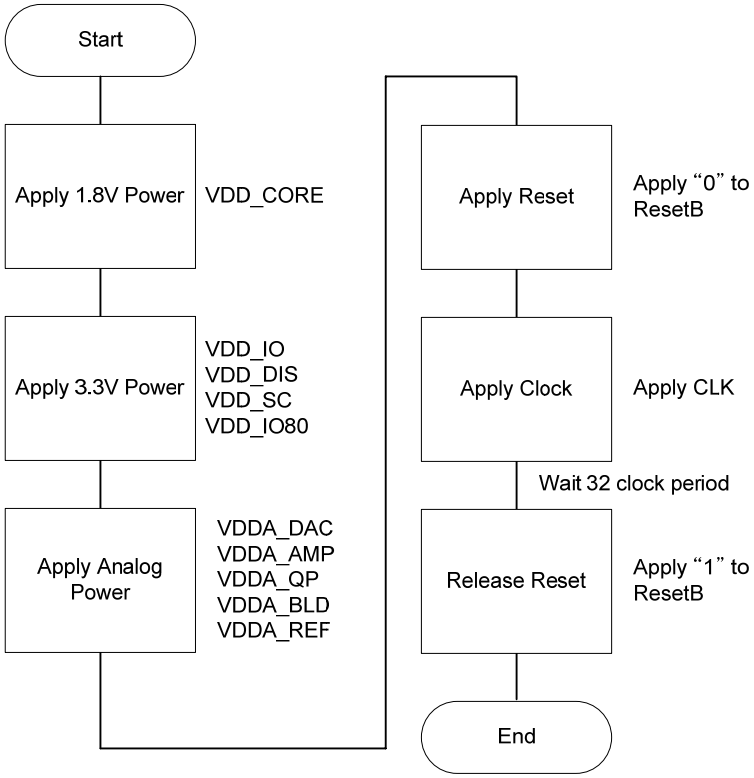


Figure 42. Power Up sequence (1.8V power supplied)

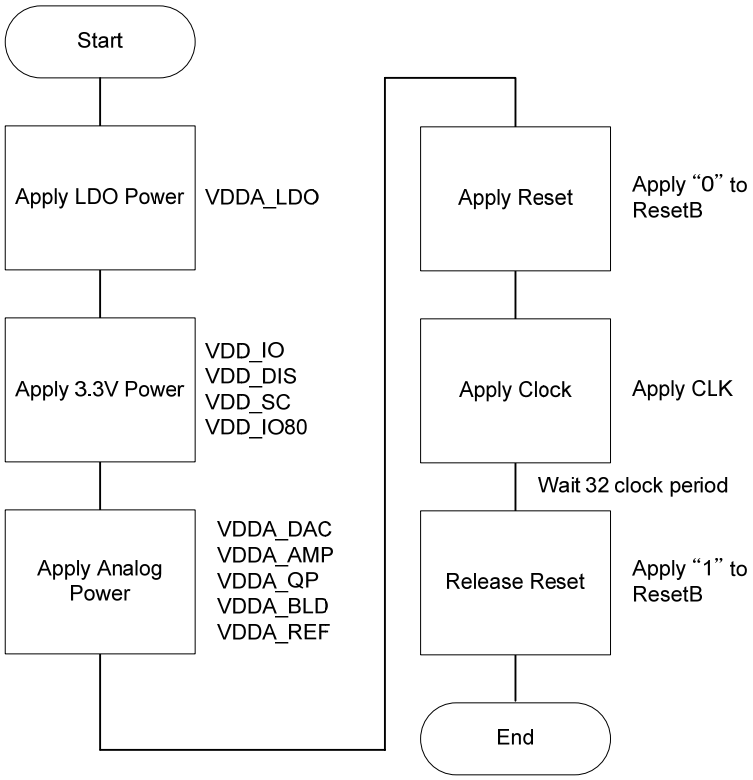


Figure 43. Power Up sequence (1.8V power not supplied and LDO is used)

Power down and restore

A230 can be powered down to save power by writing to Power down bits (DIG_DWN, PAD_DWN, DAC_DWN) in the configuration registers 0x12 and 0x13. The setting of bits DIG_DWN, PAD_DWN and DAC_DWN power down the digital, IO pads and DAC/AMPLIFIER block respectively. The driver IC can be brought back to full operation by writing 0 to the same configuration register bit. The recommended power down and restore sequences are shown below. If any of the DIG_DWN, PAD_DWN or DAC_DWN bits are set that makes the DIS_SLEEP output to go low

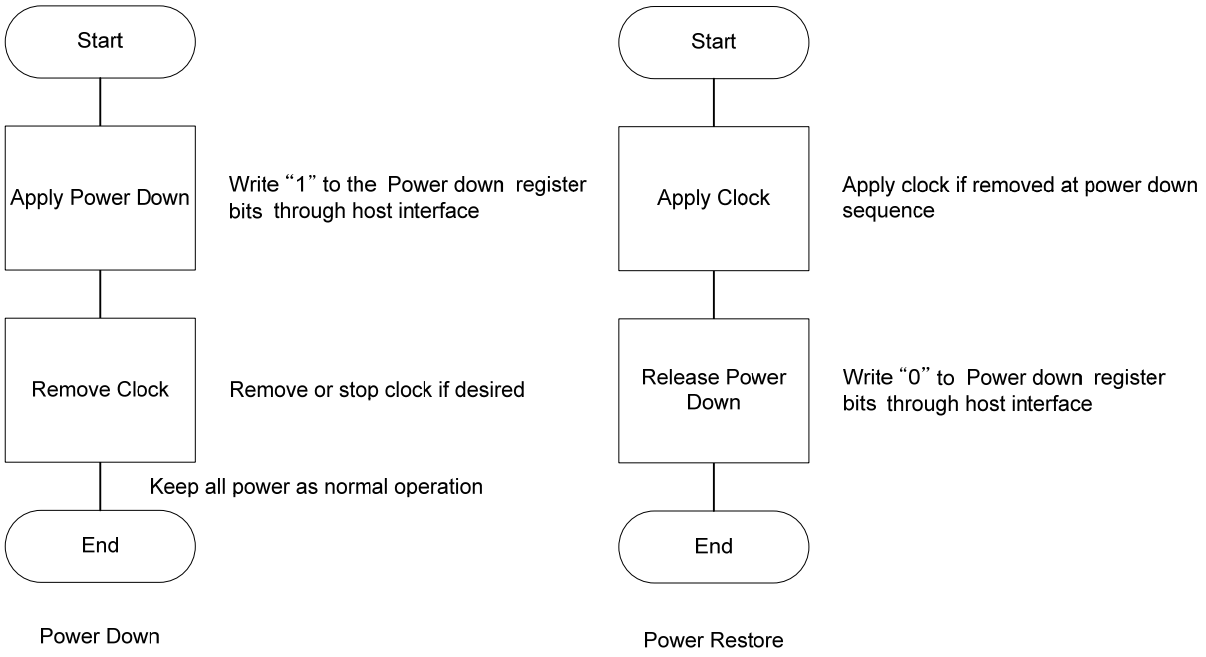
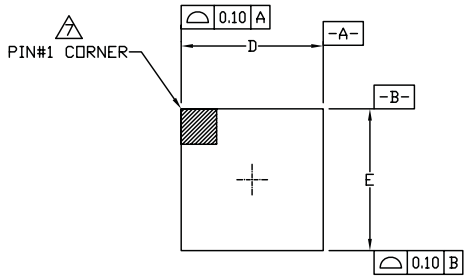


Figure 44. Power down and restore

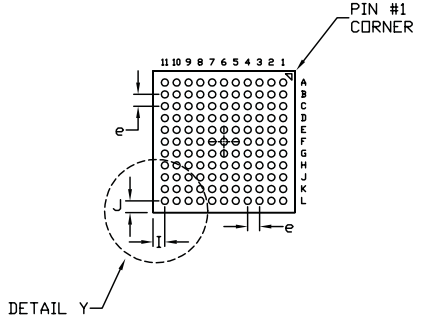
12. Package Information

Package Dimension: 6 mm x 6 mm, Ball Pitch: 0.5 mm, Ball Count: 121

REV.	DESCRIPTION	DATE	ENG	APPROVAL
–	GENERATE	12/16/'09	JH BAE	



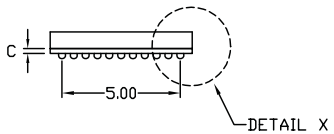
TOP VIEW



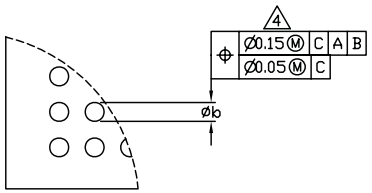
BOTTOM VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.

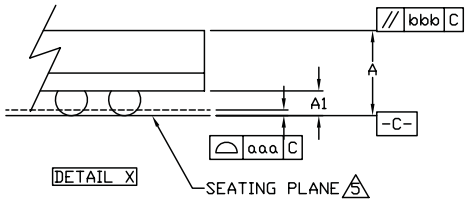


SIDE VIEW



DETAIL Y

SYMBOL	MIN.	NOM.	MAX.
A	0.99	1.13	1.25
A1	0.17	0.22	0.27
D	5.90	6.00	6.10
E	5.90	6.00	6.10
I	0.5 REF.		
J	0.5 REF.		
M	11x11 <FULL>		
aaa			0.08
bbb			0.10
b	0.25	0.30	0.35
e	0.50 TYP.		
c	0.21 REF.		



LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: N/S	DATE: 12/16/'09	DRAWN: JH BAE	TITLE: FBGA 6X6 mm, 121BALL 0.50MM BALL PITCH PACKAGE OUTLINE (MAX 1.25MM THICKNESS)
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH BAE	
PROJECTION UNLESS SPECIFIED	FRAC: .X ±0.10, .XX ±0.05, .XXX ±0.03, ANGLE ±1°	CHECKED: JJ SHIN	
		APPROVED: YS KIM	
Signetics		CAD NAME: EEV-OLB-06007	DRAWING NUMBER: EEV-OLB-06007 / REV. – / SHEET: 1 OF 1

Revision Control

Date	Person	Version	Reason
4/1/2012		0.1	Original draft version
6/14/2012		0.2	Revision after tape out, includes pin out , I80 timing, frame buffer modes and storage format
7/23/2012		0.3	Change the charge pump reference circuit to 3-diode configuration, Added pin mapping for RGB 565 mode, Change the Video AMP circuit to show connection to both VIDH and VIDL, Added the definition for IO drive strength control register (0x3F)
7/26/2012		0.4	Updated the DC characteristics table after board measurement. Added current for VDDA_VREF and VDD_SC
8/03/2012		0.5	Updated the charge pump reference circuit. Added controlling IO supply voltage at IO description table
8/15/2012		0.6	Updated the DC characteristics table
3/12/2013		1.0	Released datasheet for A230-BB version
4/26/2014		2.0	Added the definition for registers for enabling power savings in RGB111 mode. Released datasheet for A230-BC version