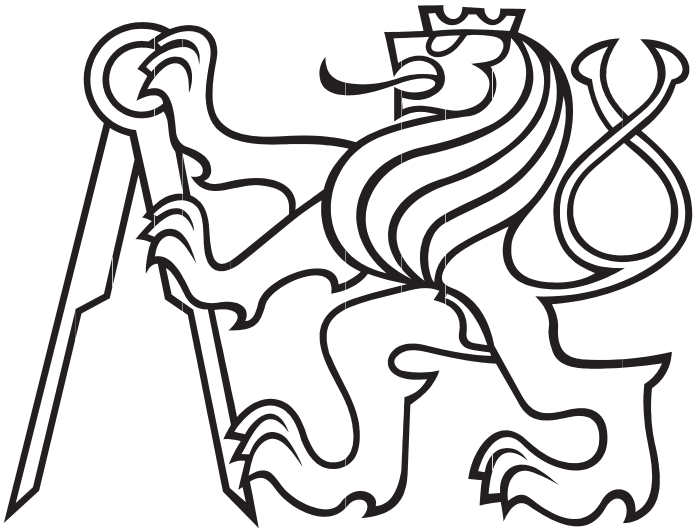
ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ

Fakulta elektrotechnická
Katedra mikroelektroniky



Diplomová práce

Teplotní senzor s dvojím oscilátorem

Intelligent temperature sensor based on dual oscillators

Autor: Bc. Václav Grim

Vedoucí práce: Ing. Vladimír Janíček, PhD.

2018

Čestné prohlášení autora práce

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

V Praze dne ....

Podpis autora práce

ČVUT
ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

ZADÁNÍ DIPLOMOVÉ PRÁCE

I. OSOBNÍ A STUDIJNÍ ÚDAJE

Příjmení: **Grim** Jméno: **Václav** Osobní číslo: **382887**

Fakulta/ústav: **Fakulta elektrotechnická**

Zadávající katedra/ústav: **Katedra mikroelektroniky**

Studijní program: **Komunikace, multimédia a elektronika**

Studijní obor: **Elektronika**

II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

Teplotní senzor s dvojím oscilátorem

Název diplomové práce anglicky:

Intelligent temperature sensor based on dual oscillators

Pokyny pro vypracování:

1) Prostudujte problematiku měření teploty pomocí polovodičových struktur.
2) Navrhněte zapojení teplotního senzoru bez použití AD převodníků.
3) Zapojení realizujte v Cadence SW a proveďte potřebné simulace.
4) Vytvořte layout obvodu.
5) Proveďte post-layoutové simulace.
6) Zhodnoťte výsledky a porovnejte se stávajícími řešeními.

Seznam doporučené literatury:

1) Pertijs M.A.P. - Precision Temperature Sensors in CMOS Technology (Analog Circuits and Signal Processing) ISBN-13: 978-1402052576
2) Cadence tutorials, online

Jméno a pracoviště vedoucí(ho) diplomové práce:

Ing. Vladimír Janíček Ph.D., katedra mikroelektroniky FEL

Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) diplomové práce:

Datum zadání diplomové práce: **26.09.2017** Termín odevzdání diplomové práce: _____

Platnost zadání diplomové práce: **28.02.2019**

Podpis vedoucí(ho) práce	Podpis vedoucí(ho) ústavu/katedry	Podpis dekana(ky)

III. PŘEVZETÍ ZADÁNÍ

Diplomant bere na vědomí, že je povinen vypracovat diplomovou práci samostatně, bez cizí pomoci, s výjimkou poskytnutých konzultací. Seznam použité literatury, jiných pramenů a jmen konzultantů je třeba uvést v diplomové práci.

Datum převzetí zadání	Podpis studenta

Abstract

This thesis is dealing with design procedures needed for successful design of semiconductor temperature sensor with digital output. Among several approached discussed and evaluated, dual relaxation oscillator proved to be the most robust solution. Although in theory only single-point calibration is needed, it does not provide enough accuracy due to device mismatch.

The key idea of this design lies in moving the trimming circuitry from the analog sensor core to the digital processing portion. Although the total number of transistors is increased, it allows for large trimming range with good linearity.

Design steps are described using TSMC 180 nm mixed-signal technology. A complete IC layout with I/O pads is presented.

Keywords: *CMOS, Analog IC Design, PTAT source, temperature sensor*

Anotace

Tématem diplomové práce byl návrh polovodičového integrovaného obvodu pro měření teploty, jenž dodává naměřené hodnoty v digitálním tvaru. Z několika možných principů byl pro svoji robustnost zvolen senzor se dvěma relaxačními oscilátory. Přestože v principu postačuje pouze jednobodová kalibrace, z důvodu nepřesných poměrů parametrů jednotlivých tranzistorů bylo nutné použít dvojbodovou kalibraci.

Hlavní myšlenka tohoto návrhu spočívá v použití nekalibrovaných analogových bloků, jež jsou použity pro výpočet teploty v digitální části. Přestože se tím navýší celkový počet tranzistorů, lze dosáhnout velkého kalibračního rozsahu s dobrou linearitou.

Návrh byl proveden v technologii TSMC 180 nm, včetně layoutu a umístění kontaktovacích plošek.

Klíčová slova: *CMOS, Návrh analogových IO, proudový zdroj PTAT, integrovaný snímač teploty*

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Chapter 1
Introduction

Temperature sensors are present in all imaginable electronic devices, where they serve many different purposes. Each field of application prioritizes different aspects of temperature measurement – e.g. medical sensors require precision in narrow range, for industry the key parameter is reliability, commercial devices need to be as cheap as possible, etc.

Typical application of integrated temperature sensors is to provide feedback to closed-loop temperature control systems, such as HVAC or thermally stabilized instrumentation (caesium clocks etc.). Other important area is overtemperature protection, either for monitoring ambient temperature, temperature of components on a PCB, or for on-die measurement inside a larger IC. Using integrated sensors instead of discrete RTDs or thermistors has the advantage of increased reliability, easy automated assembly, and reduction in size and cost.

Because integrated circuits cannot be manufactured with tolerances tight enough to ensure good initial accuracy, trimming is always necessary. For high volume production, chip-by-chip calibration is too expensive, so the usual design goal is to achieve the required accuracy with batch trimming, during which only several samples from each wafer are measured and results are extrapolated to all remaining dice.

1.1 Motivation

Initial motivation for this thesis was to continue with work started by previous students of my advisor at NTUST. The original idea was to modify existing temperature compensated oscillator into a temperature sensor by rearrangement and adjustment of device dimensions. After much effort was expended to no avail, a new design based on bandgap reference was created. However it needed a reliable trimming method capable of adjustment for any process corner, and more importantly regardless of any device mismatch.

Trimming by adjustable increment counter was selected because a counter would be present in the circuit in any case, and also because this way the analog digital portions of the circuit can be designed and verified separately. Lengthy iterative calibration during Monte Carlo simulations is avoided.

1.2 Thesis organization

At first in chapter 2 several published designs of temperature sensors are reviewed and compared. Chapter 3 deals with system design and determines key sensor parameters based on initial requirements. In 4 and 5, detailed steps of analog and digital circuit design are explained. Chapter 6 is dealing with layout procedures. Conclusion (8) summarizes the outcomes and provides comparison between initial

requirements and actually achieved performance.

1.3 Relation to previous theses

This thesis is a continuation of my previous master thesis *Intelligent temperature sensor based on dual oscillator*, done at NTUST Taipei. Although the main principle remains the same, the circuit was completely redesigned using a different process (TSMC 180 nm instead of TSMC 250 nm). Previous thesis used HSPICE as the main simulation engine, current version uses Spectre. Trimming method is also reworked from adjustable resistors to adjustable digital accumulator.

Chapter 2
Literature Review

2.1 Temperature-insensitive relaxation oscillator

Design [1] was used to provide the basic operation principle. Although this circuit is not directly related to temperature measurement, it was taken as a reference for creating a simple oscillator with controllable temperature coefficient. Originally the thesis' objective was to modify it into a complete temperature measurement circuit, however it was not successful due to the inherent nonlinearity of regular polysilicon resistors.

It is a robust industrial design, already used for several years in Freescale microcontrollers. It provides a low-precision low-power clock signal to auto-wakeup IP. By adjusting sizes of resistors R1 and R2, it is possible to achieve reasonable stability of frequency across temperature. However it suffers from poor PSRR, which means that for any precision application it would have to be complemented by a voltage regulator, increasing complexity of the whole system. Not shown in the figure is a mandatory startup circuit, because it is possible that after power-on, currents in both MS1 and R1 stay at zero.

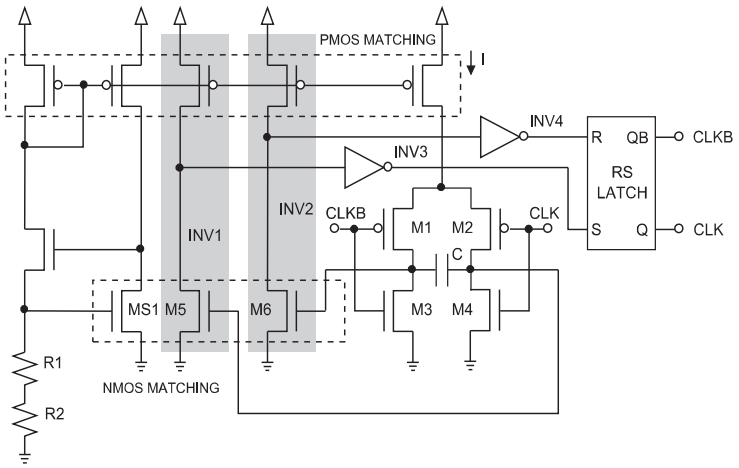


Figure 2.1: Schematic of simple relaxation oscillator (from [1])

Principle of operation is simple: a transistor H-bridge is used to alternately charge capacitor C with constant current through either M1 or M2. Instead of using traditional voltage comparators with differential pair at input, simple current-starved inverters INV1 and INV2 are used. This introduces additional temperature dependence to the circuit, because the comparator tripping point is determined not only by threshold voltage of M5 and M6, but also by the biasing current.

The effects of variable capacitor current and variable voltage threshold are set to cancel each other, keeping product $V_{th}/I(T)$ constant. In case the temperature coefficient of $I(T)$ could be reversed, the oscillator would produce frequency strongly

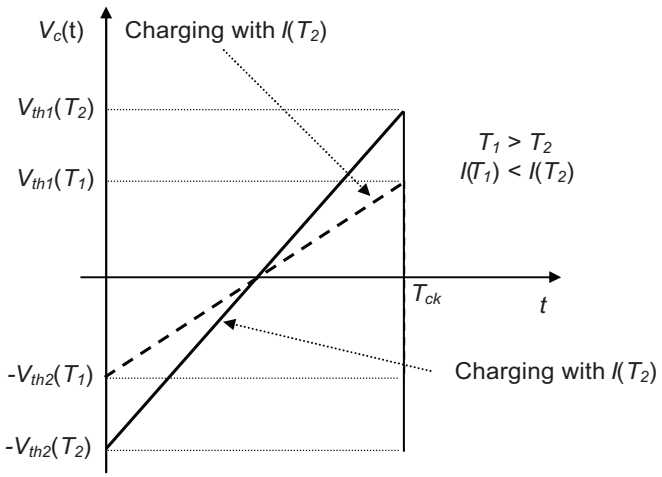


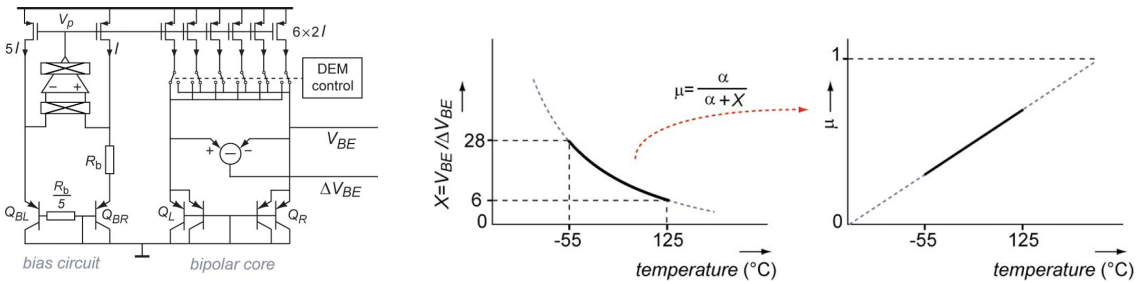
Figure 2.2: Principle of period stabilisation (from [1])

dependent on temperature. Pairing such temperature sensitive oscillator with the already existing compensated oscillator would allow for extraction of absolute temperature information. The problem with such arrangement was high sensitivity to process variation and non-linearity, therefore a different approach was eventually chosen.

2.2 BJT-based sensor with ADC and digital post-processing

Design presented in [2] shows exceptional performance, especially in terms of initial accuracy before trimming. It exploits bipolar transistor's exponential characteristic in a way similar to bandgap voltage reference, but in this case V_{BE} from two identical transistors is used to compute the temperature.

2.2.1 Sensor core



(a) Schematic (b) Voltage ratios before and after linearization

Figure 2.3: Chopped BJT sensor core (from [2])

Sensor core is biased by a PTAT current generator, formed by transistors Q_{BL}, Q_{BR} and a chopped operational amplifier. Voltage across these two BJTs is not used for measurement. Instead the PTAT current is copied into second pair of BJTs, Q_L

and Q_R. The left-to-right current ratio is maintained at 5:1, but the current is chopped by switching six analog multiplexers between Q_L and Q_R. This way the biasing P-MOSFETs become dynamically matched to each other. Temperature information is extracted from ratio $V_{BE}/\Delta V_{BE}$ by integrating amplifier and a two-step ADC. Although this ratio provides high precision, it is not a linear function of temperature. Linearisation is done as the last step in digital post-processing circuit, which in this implementation is not included in the IC itself.

2.2.2 Zoom ADC

Zoom Analog-to-digital converter is a circuit combining two different techniques to achieve high resolution and low power. It is especially suited for slow signals such as ambient temperature. In this case the ratio $V_{BE}/\Delta V_{BE}$ is known to always be between 5 and 25. At first a 5-bit successive approximation converter is used to find a coarse "integer" value. After V_{BE} is located between $n \times \Delta V_{BE}$ and $(n+1) \times \Delta V_{BE}$, conversion mode is switched to $\Delta\Sigma$. The two voltages are used as positive and negative references, between which lies the precise value of V_{BE}. Delta-sigma bitstream needs to go through a decimating filter to remove unwanted spectral portions. This digital post-processing is implemented in a separate logic controller outside the sensor IC. To further improve this circuit, first order $\Delta\Sigma$ modulator

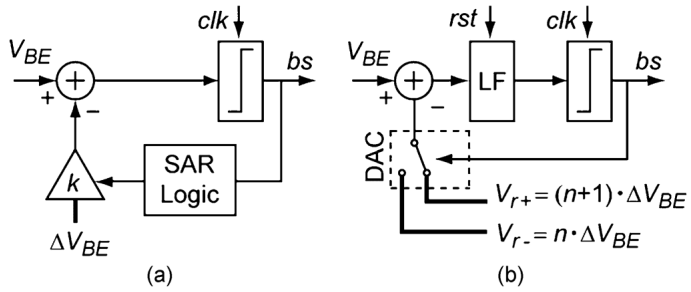


Figure 2.4: Zoom ADC, SAR phase (a) and $\Delta\Sigma$ phase (b), from [2]

can be replaced by second order. This relaxes the need for high dynamic range in amplifier k, enabling 13-bit resolution to be achieved with low power consumption.

Chapter 3
System Design

3.1 Initial requirements of sensor parameters

The first step in the design process of every integrated circuit is defining the required key parameters, such as required temperature range or accuracy. Some parameters given by the manufacturer's technology are fixed, such as supply voltage, which is 1.8 V for core devices and 2.5 V for I/O devices.

Temperature range of PTAT-based sensor core is unlimited in theory, in practice there will be limits imposed by other parts of the sensor. This applies most prominently to the bias current generator, which has to ensure correct operating region throughout the temperature range. A tradeoff between power consumption, complexity and temperature range has to be selected. Devices with broad industrial or military temperature range will waste more power for biasing, because they need to take larger temperature drifts into account. Another important thing to consider is the validity of models used for simulations. Design kit provided by TSMC is intended for commercial purposes and is based on characterisation done between 0 °C and 100 °C. Although there will be no problem with simulating lower or higher temperatures, the results are less likely to match the actual performance after fabrication. The design procedures will start with temperature range of −55 °C to 125 °C. These values are commonly used for military applications. In case of problems with reliability or accuracy the range may be narrowed to stay within the characterisation bounds, e.g. to commercial range of 0 °C to 70 °C.

When designing a temperature sensor with digital output, it is important to know the required output data rate. Different applications have different needs for readout speed. In order to efficiently use a sensor in a temperature feedback loop, it is necessary to keep sampling period shorter than the plant's time constant τ. Some special application work with very short time constant, for example [3] uses on-die temperature sensor together with miniature thin-film heater to produce thermal 'carrier wave' with 300 K swing and frequency over 1 MHz, to be used for thermography and absorption spectroscopy. The silicon die is very small and has high thermal conductivity ($\approx$150 W m^{-1} K^{-1}). Thus the time constant in this case is in the order of microseconds. In systems with off-chip heaters and coolers, such as [4] used for maintaining constant temperature of semiconductor lasers for optical spectroscopy measurements, significantly longer time constants are present in the system, in the order of tens or hundreds of milliseconds. The sensor discussed in this thesis is intended for ambient air temperature measurement and therefore its dynamic properties are of little concern. One sample per second is more than enough for applications with stationary or slow-moving air. For this design a slightly higher sample rate of 32 SPS was chosen to allow for possible oversampling.

Resolution of an absolute temperature sensor has to matched to its effective number of bits, otherwise it will produce unnecessarily long results, wasting supply current

for no increase in accuracy. Effective number of bits is defined as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{3.1}$$

The concept of ENOB is meant for evaluating ADCs and DACs, but it may be applied also to sensors. Errors caused by non-linearity are difficult to predict, but for simplicity static errors in frequency ratio may be used. When the ideal transfer function is

$$H_{ideal}(T) = \frac{f_1(T)}{f_2(T)} = 0.0025 \cdot T - 0.25 \tag{3.2}$$

and lowest possible temperature error is approximately 0.1 °C, which in relative terms is 0.05 % or -66 dB. Using equation (3.1), the resulting ENOB is 10.7 bits. To keep design compact and also because some dynamic range can be saved in subsequent digital processing, only 10-bit resolution is used.

Oscillator frequency may be determined from the output data rate and its resolution. Data is assumed to be shifted out through a SPI-like interface, with output clock at ½ of reference oscillator. For the aforementioned resolution of 10 bit and data rate 32 SPS, minimum possible frequency is

$$f_{min} = f_S \cdot 2^N = 32 * 1024 = 32\,768\,\text{Hz} \tag{3.3}$$

In reality the oscillator needs to run faster, because in this implementation data readout phase has to be interleaved with data acquisition phase, with 1:1 (or possibly 3:1) ratio. Another disadvantage of such low frequency is the required size of timing capacitors. Because the reference oscillator frequency will not be subject to trimming, it is necessary to leave some margin for temperature coefficient and chip-to-chip variation in order to achieve 32 SPS in worst case scenario. Therefore design will proceed with target f_{ref} at 100 kHz.

At this point all important high-level parameters are formulated, and more specific design procedures may commence. Following table summarizes their values.

Supply voltage	1.8 V
Temperature range	−55 °C to 125 °C
Output data rate	32 SPS
Resolution	10 bits
Reference f_{osc}	100 kHz

Table 3.1: Targeted system parameters

3.2 Principle of operation

The presented sensor is based on two oscillators with different thermal coefficients; one ZTC or zero temperature coefficient and one NTC or negative temperature coefficient. Absolute temperature is determined from the frequency ratio of these oscillators. It is important that it does not rely on the NTC frequency itself, because it is necessary to reject non-constant bias current.

Digital temperature is extracted by a counter, clocked by the NTC clock and periodically reset by the ZTC clock. This way at each counter reset a value corresponding to f_{NTC}/f_{ZTC} is available at output. This basic structure needs several refinements

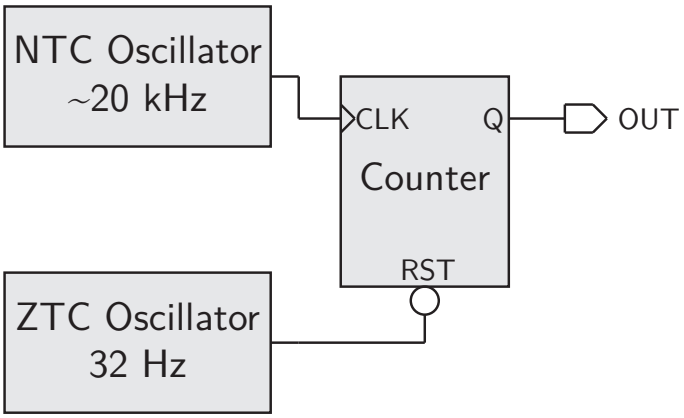


Figure 3.1: Basic system diagram

in order to make it a usable integrated circuit. All semiconductor temperature sensors need a trimming circuit to cope with finite manufacturing accuracy. In this case also a serializer is needed, to reduce the number of I/O pads, which would otherwise take up a lot of chip area [5].

3.3 Trimming

Trimming is usually done by changing W/L of biasing transistors by switching appropriate number of parallel instances on and off. It can also be done by shorting out segments of a resistor string. These traditional methods require many additional device instances, and since transistors in analog circuits are much larger than minimum node size, it can lead to significant area being occupied by the trimming circuit, such as in [6]. That particular paper uses an array of polysilicon resistors, with laser-cut metal connections. Athough such technique is not used for mass production anymore, some kind of trimming circuit is necessary in any case.

The design presented in this thesis attempts to get around analog trimming by using trimming only in digital on-chip processing. Sensors based on PTAT current lend themselves to easy calibration due their inherent linearity. Although the slope of P-N junction forward voltage is constant in theory, in practice it is impossible due to mismatch in current mirrors. Therefore a means to adjust both slope and offset is necessary. A digital circuit with transfer function

$$N_{out} = K_{offs} + \frac{f_{TEMP}}{f_{REF}} \cdot K_{gain} \tag{3.4}$$

has to be implemented. Bandgap curvature compensation or other higher-order effects are not implemented, because that would require much more complex circuitry. Figure 3.2 shows the concept of digital trimming: an accumulator with adjustable reset value (offset K_{offs}) and adjustable increment (gain K_{gain}). Repeated addition of constant K_{GAIN} is equivalent to multiplication. To make this concept work, register size has to be increased by the number of bits in K_{GAIN}. If 10-bit counter

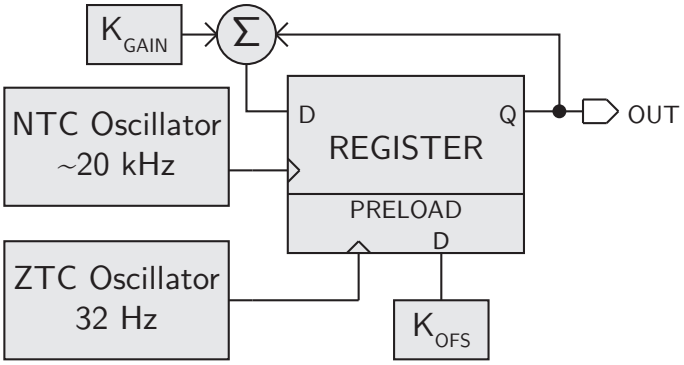


Figure 3.2: Block diagram with accumulator

was previously assumed and 6-bit multiplication constant is used, in total 16-bit register is needed. Not all bits need to be supplied to output during readout phase, only the 10-bit integer portion is relevant. It would be more correct to keep the remaining fractional part and add it to next conversion cycle, but it would require more adders in the circuit and overall size and complexity would increase.

Following figures show preliminary results from a statistical analysis of the analog block. Two-point measurement is assumed, at 25 °C and 65 °C. Slope is calculated as a linear fit between these two points. It should be noted that there is correlation

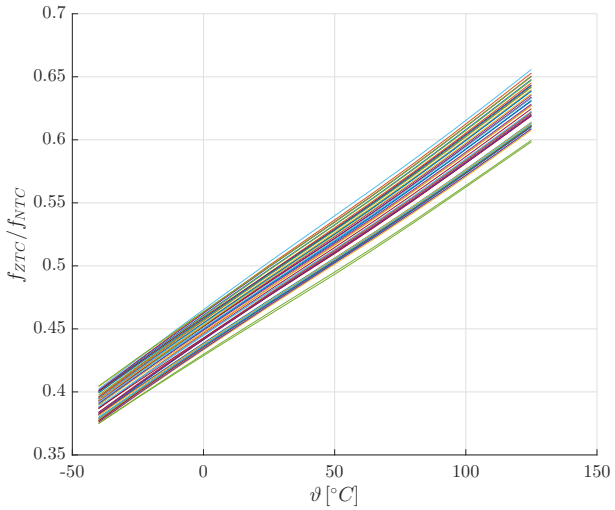
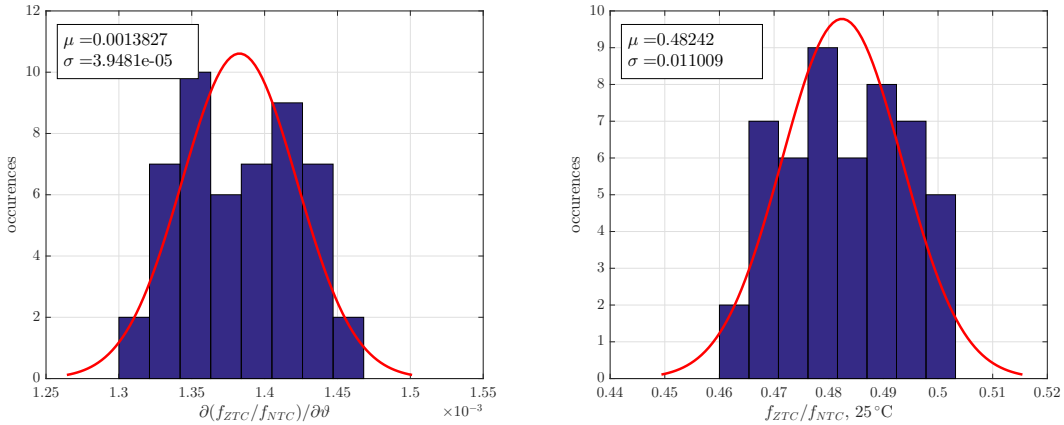


Figure 3.3: Statistical variations in transfer function

between these two histograms, because in theory all lines intersect at 0 K. In practice both offset and slope has to be controlled, as curves deviate from PTAT behaviour.

The design itent is to allow correction for any gain and offset errors from within $\pm 3\sigma$ intervals, which would provide soft yield of 99%. Without comparison with actual manufactured samples, it is difficult to make any assumptions about confidence intervals, because actual yield depends on many parameters not included in the simulation models.

At first average value of slope is observed. Its value $a = 1.38\,\mathrm{m°C^{-1}}$ is taken as the calibration target. Three-sigma interval lies between $1.26\,\mathrm{m°C^{-1}}$ and $1.50\,\mathrm{m°C^{-1}}$. If error caused by incorrect slope has to stay within ±0.5 °C across whole temperature



(a) Slope of frequency ratio

(b) Frequency ratio at 25 °C

Figure 3.4: Histograms of statistical analysis

range, maximum permissible error is computed as

$$a \cdot \frac{\vartheta_{max} - \vartheta_{min}}{2} = (a + \Delta a) \cdot \left(\frac{\vartheta_{max} - \vartheta_{min}}{2} + \Delta\vartheta \right) \tag{3.5}$$

$$\Delta a = a \cdot \frac{2\Delta\vartheta}{\vartheta_{max} - \vartheta_{min} + 2\Delta\vartheta} \tag{3.6}$$

$$\Delta a = 1.38 \times 10^{-3} \cdot \frac{2 \cdot 0.5}{125 - (-55) + 2 \cdot 0.5} \tag{3.7}$$

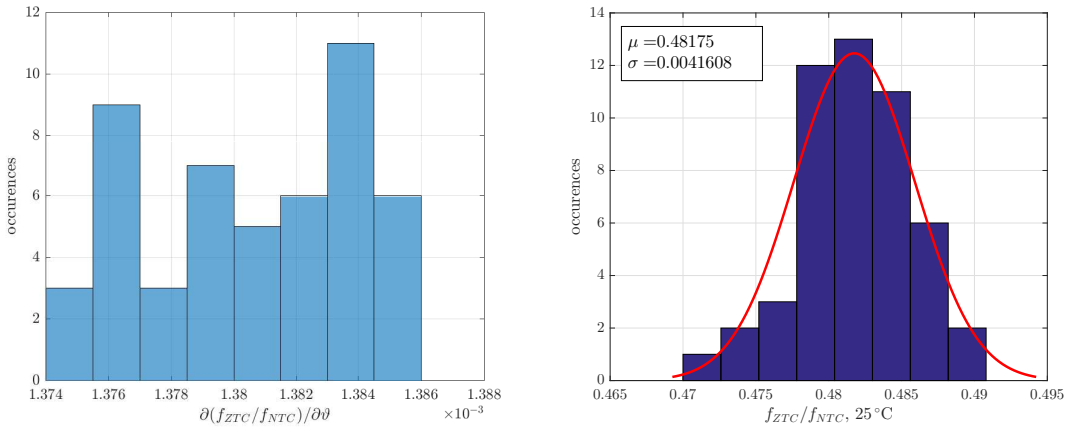
$$\Delta a = 7.6 \times 10^{-6}\,^{\circ}\mathrm{C}^{-1} \tag{3.8}$$

This value corresponds to $0.19\,\sigma$. In order to encompass $\pm 3\sigma$ interval, 32 steps (5-bit word) are needed. The slope correction term Δa needs to be combined with its much bigger base value a. Binary numbers in this case are best treated as 1.n fixed-point values. Centre of calibration interval is 1_d or $1.000..._b$. Maximum increment has to end with 01111_b (largest 5-bit signed number) and its value has to be ≥ 1.086 $((\mu + 3\sigma)/\mu)$. Closest value is 1.117_d or 1.0001111_b. Minimum increment is derived in the same way, except for additional sign extension. It is 0.875_d or 0.1110000_b.

To verify previously defined calibration interval, slope correction is performed on curves from 3.3. Raw data is divided by corrected slope constant $a + \Delta a$ to match targeted slope of 1.38×10^{-3} between 25 °C and 65 °C. Histograms 3.5 confirm the expected outcome. Slope error is narrowed down to Δa previously defined in equation 3.8. Its distribution is no longer normal, therefore it is not possible to define its standard deviation. Offset at 25 °C retained its normal distribution, but because gain and offset were correlated, its standard deviation was reduced from 0.011 to 0.004.

The last step is to perform offset calibration. It is done at 25 °C. This temperature was selected, because the sensor is likely to work at room temperature, and because it is near the centre of the temperature range. It is not practical to make trimming granularity too fine, because even with precise trimming the results will drift with supply voltage. Steps equivalent to 0.25 °C are assumed. Trimming target is $b = 0.48$. To determine required Δb resolution, step size is calculated as

$$\Delta b = a \cdot \Delta\vartheta = 1.38 \times 10^{-3} \cdot 0.25 = 3.45 \times 10^{-4} \tag{3.9}$$



(a) Slope of frequency ratio (b) Frequency ratio at 25 °C

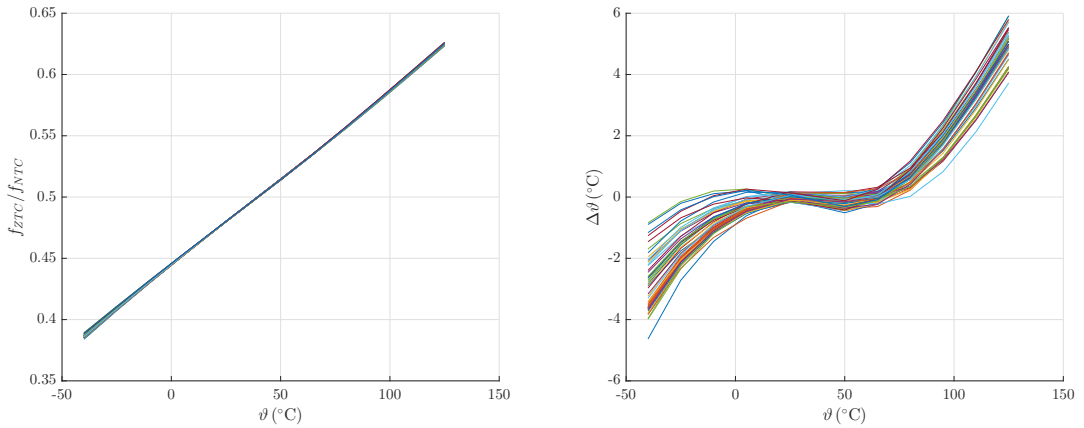
Figure 3.5: Histograms after slope correction

To cover $\pm 3\sigma$ interval from 0.469 to 0.494, 72 steps are needed. This is rounded to 64 steps or 6-bit word. Chapter 3.1 stated that accumulator with 10-bit integer part is to be used. Its preload value for -3σ is

$$N_0 = 2^{10} \cdot 3\sigma = 1024 \cdot 3 \cdot 4.16 \times 10^{-3} = 12.8 \tag{3.10}$$

This number is rounded to 16, the nearest power of two. Required step size is smaller than 1 LSB, so a portion of accumulator fractional part is also used for preloading. Highest preload value is therefore $00\,0000\,1111.1000\,000_b = 15.5_d$ and the lowest is $11\,1110\,0000.0000\,000_b = -16_d$.

Following picture shows all 50 transfer curves after both slope and offset calibration, together with deviations from targeted linear function $1.38 \times 10^{-3} \cdot \vartheta + 0.4455$. Be-



(a) Calibrated transfer functions (b) Deviation from target linear function

Figure 3.6: Results of calibration

tween 10 °C and 80 °C, the calibration outcome is satisfactory – temperature errors stay within ±1 °C from ideal linear transfer characteristic. However at both ends of temperature range the errors are significant, almost an order of magnitude higher than expected. It is caused by inherent nonlinearity not only in the PTAT voltage

reference, but also in the rest of the circuit, which suffers from temperature drift of threshold voltages. More careful design can reduce spread of these curves, but it is difficult to get rid of the S-shaped curvature. It could be compensated by additional digital processing, but it would lead to impractically large number of logic gates. Design will continue with the outlined principle, and in case of unfavourable results the working temperature range shall be reduced.

Chapter 4
Analog Circuit Design

4.1 Sensor core

The sensor core is the central part of the IC, on whose quality depends most of its accuracy. It is based on classical principle of creating a difference in forward voltage between two transistors with identical collector currents. In ideal case, a BJT current follows the exponential equation

$$I_C = I_S e^{\left(\frac{qV_{BE}}{nkT} - 1\right)} \tag{4.1}$$

where $k = 1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}}$ is the Boltzmann constant, $q = 1.602 \times 10^{-19}\,\mathrm{C}$ is the elementary charge, I_S is the saturation current and n is the non-ideality factor or emission coefficient. When two transistors with different emitter areas are arranged to have the same V_{BE}, (as in figure 4.1), equations may be combined as follows:

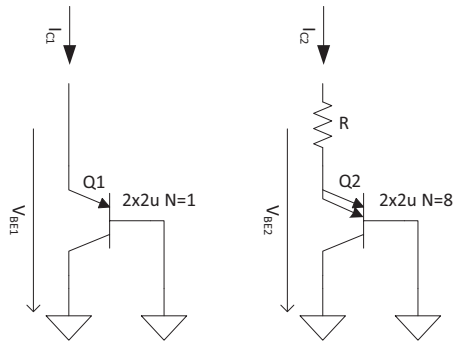


Figure 4.1: Principle of bandgap circuit

$$I_{C1} = I_S e^{\left(\frac{qV_{BE1}}{nkT} - 1\right)} \qquad I_{C2} = A I_S e^{\left(\frac{qV_{BE2}}{nkT} - 1\right)} \tag{4.2}$$

$$e^{\frac{qV_{BE1}}{nkT}} = A e^{\frac{qV_{BE2}}{nkT}} \tag{4.3}$$

$$\frac{qV_{BE1}}{nkT} = \ln(A) + \frac{qV_{BE2}}{nkT} \tag{4.4}$$

$$\Delta V_{BE} = V_{BE1} - V_B E2 = \ln(A) \cdot \frac{nkT}{q} \tag{4.5}$$

Ratio of areas A was selected as 8, because it provides a good common-centroid layout pattern. The aforementioned derivation assumes that both transistors have the same saturation current. This depends a lot on quality of layout. Models predict $0.05\,\%(1\sigma)$ mismatch in I_S and $2\,\%$ in β_f, the only way to verify these numbers is to measure manufactured samples. The overall core schematic is provided in figure 4.2.

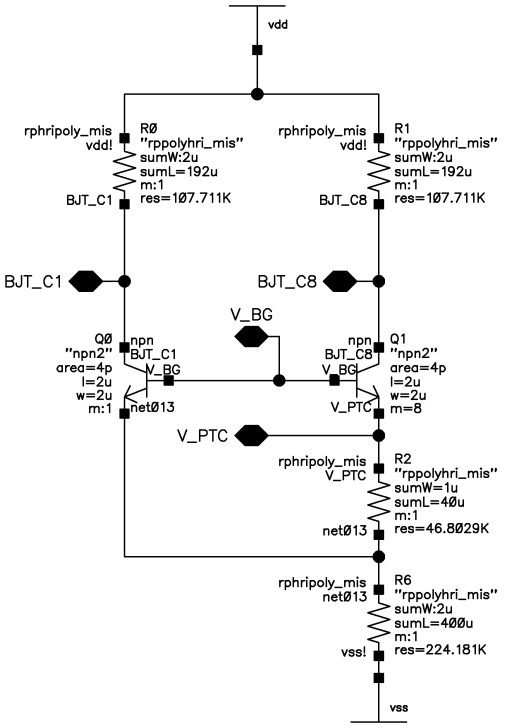


Figure 4.2: Sensor core schematic

4.2 Operational amplifier

This amplifier is used for establishing the bandgap voltage V_{BG} by keeping voltage at nodes BJT_{C1} and BJT_{C8} equal at around 150 mV below V_{DD}. It is a standard 2-stage amplifier. Because its input levels are very close to power supply voltage, it uses N-type differential pair at input. Input offset voltage of this amplifier has significant influence on quality of 1:1 current distribution between left and right BJT and therefore on the value of V_{BG}.

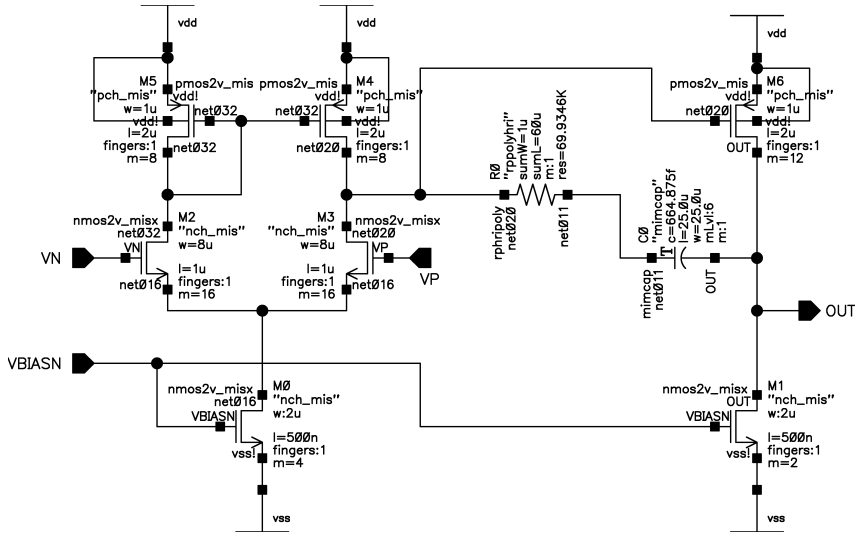


Figure 4.3: Operational amplifier schematic

4.3 Startup circuit

Startup circuit is necessary to ensure that the sensor core does not get stuck in an undesirable state in case it has more than one possible operating points. In this case it is possible that V_{BG} remains at 0 V and both BJT_{C1} and BJT_{C8} close to V_{DD}. MOSFETs M0,M1,M2,M15 are constantly drawing a small current to create

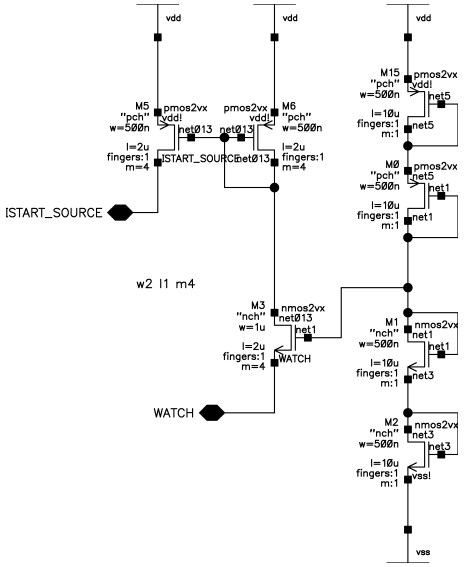


Figure 4.4: Schematic of startup circuit

bias voltage for gate of M3, approximately $V_{dd}/2$. During normal operation, input terminal `WATCH` is at around 800 mV, keeping M4 closed. During fault condition voltage at `WATCH` drops to zero and current starts to flow, through M3 and also through M5.

4.4 Comparator

Comparators in general have the same structure as operational amplifiers, but they have no frequency compensation. This is because they always work with large signals, where AC parameters are not defined. Both polarities of input stage would work here, because reference voltage is near neither positive nor negative rail.

Chapter 5
Digital Circuit Design

5.1 Standard design flow

The design of oscillator-based temperature sensor may successfully be split between analog and digital portions, each of which may be conducted separately using appropriate tools and verification methods. Digital design starts with behavioural description of the required functionality in the form of a Verilog RTL code. This code is tested to ensure the code conveys the designer's intent. Verilog by itself provides means for functional testing with *testbenches*. In case of more complicated tests scripting languages are used to automate the process. For example Modelsim, a popular simulator and IDE for HDL languages, comes with a built in TCL interpreter. However any editor and any script interpreter can be used with Modelsim simulation engine.

After behavioural code is finished, design has to be synthesised. Synthesis tool takes behavioural code together with timing constraints and recreates the design as a new source file with identical functionality, but different internal structure. Synthesised netlist is a valid Verilog source as well, and it consists entirely of instances of logic elements. Synthesis is dependent on the available chip manufacturing technology. Design library (CBDK or cell-based design kit) may be provided either by the IC foundry (TSMC, ON Semi, etc.) or a third-party company (e.g. Faraday).

Synthesised netlist is then used to perform place and route, commonly abbreviated as P&R. In this step instances of logic cells are arranged into a rectangular area representing the surface of a silicon die. Auto-routing algorithm then iteratively tries to connect logic cells together using connections in metallization layers. It has to follow design constraints regarding propagation delays – this is especially important for clock nets. Clock signals typically drive a large clock domain, in which all nodes have to receive exactly the same signal, regardless of its physical distance from clock source. Advanced techniques such as buffer insertion or matched interconnect length are therefore used.

Post-layout simulation is conducted, in order to reveal any setup time or hold time violations introduced by wire propagation delay and parasitic capacitances and resistances. Physical extraction tools can complement the original cell netlist with accurate information about interconnect properties.

The last step is export of finished digital core layout, typically in GDS format. It may then be imported into IC layout editor and merged with analog subcircuits to form a complete integrated circuit. At this stage bonding pads with ESD protection devices are also added.

The actual inner structure of logic cells is not always included in the CBDK, because of licensing conditions and information security. This is the case e.g. with Faraday's UMC180 library. Users of such library have to perform tapeout with empty placeholder rectangles, which are substituted during postprocessing at IC foundry.

5.2 Review of available resources

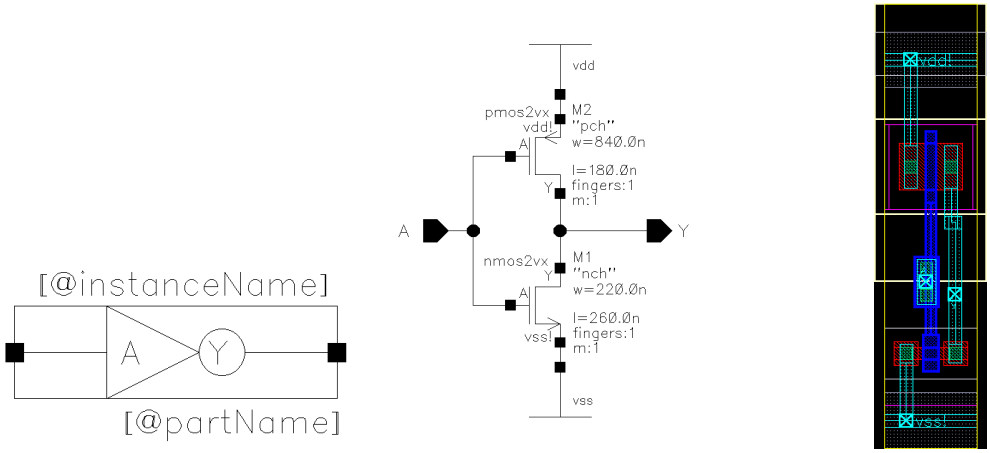
For the design of the sensor's digital circuit I did not have access to any suitable standard cell library. Therefore everything had to be assembled from individual transistors. Synthesis was done manually, assuming a small set of elementary logic components: transfer gates, D-type flip-flops, inverters, NANDs, NORs and XORs. Because of the digital circuit's rudimentary functionality, it is not impossible to perform synthesis and place&route without any automated tool. Any timing parameters cannot be taken into account with such primitive approach, but it should not be a problem when all clock frequencies are no higher than 100 kHz (as specified in section 3.1).

5.3 Digital subcircuits design

5.3.1 Elementary gates

Inverter

Inverter is the simplest logic gate with one P-type and one N-type MOSFET. Both devices are as short as possible, TSMC180 allows sizes down to 180 nm. N-channel M1 is slightly longer, 260 nm, to achieve symmetric transfer characteristic without making M2 too wide. Output of an inverter has to toggle when input voltage crosses $Vdd/2$, this is to ensure good noise immunity. In typical CBDKs there are multiple variants of buffers and inverters with varying transistor sizes to provide appropriate fanout. For simplicity only minimum size is designed here, in case of need for high drive strength multiple instances may be placed in parallel.



(a) Symbol view (b) Schematic view (c) Layout view

Figure 5.1: Inverter

Transfer gate

Transfer gate is a component realizable only with unipolar transistors. It allows for using fewer transistors than former bipolar circuits, i.e. when building multiplexers

or SRAM cells. One P-type and one N-type transistor of minimum length are connected in parallel. Their widths are adjusted to provide approximately equal resistance in conducting state.

NAND and NOR

Primitive arithmetic gates use the same transistor size as inverter mentioned earlier. Two-input and three-input variants are prepared for further integration into logic circuits. There is no XOR gate, even though it is usually needed for adders. Here it is omitted, because it requires a at least 12 transistors. With 18 adder stages it would take a significant amount of chip area. Different types of adders without XOR gates are used instead.

5.3.2 Building blocks

D-type flip-flop

Compared to its bipolar implementation with NAND gates, Dff with TGs is more power and area efficient. It comprises of two SRAM loops of back-to-back inverters. These two loops (master and slave) are alternately opened and closed by the clock signal CLK.

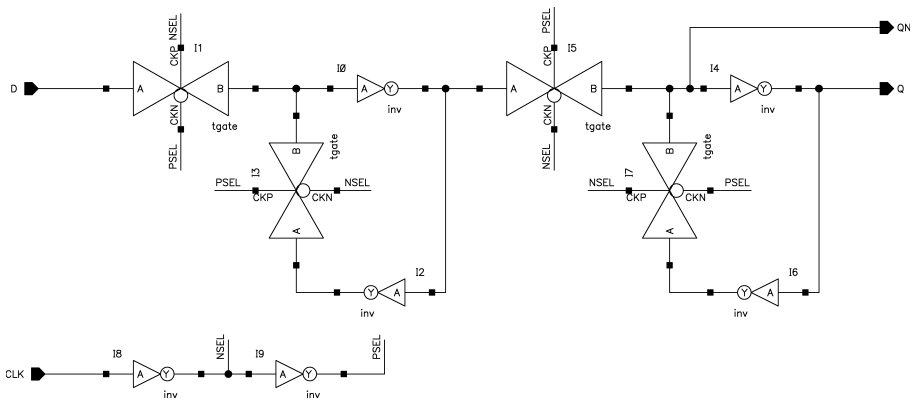


Figure 5.2: Schematic diagram of D-type flip-flop

Adders

Both a half adder and a full adder are needed in this design. Half adder takes two inputs (a and b) and produces two outputs (sum and carry-out). Full adder takes three inputs (a, b and carry-in) and produces two outputs (sum and carry-out). Most obvious implementation is with XOR gates, but in this case less usual type from [7] is used. Although its schematic is more complex, in terms of transistor count it provides significant saving.

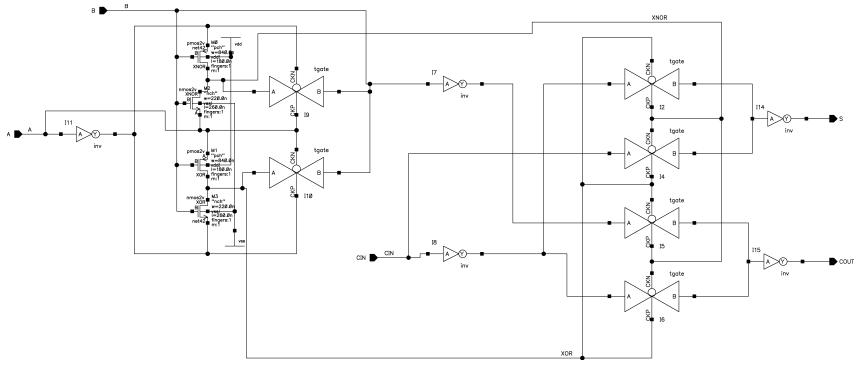


Figure 5.3: Transmission gate full adder schematic

5.4 Serial data interface

Because reading the output data in plain binary form would take too many I/O pads, a simple serial interface is needed to provide practical means of communication. Although a single wire interface is possible in the form of a UART, it will not be used because the sensor's reference clock is not constant and clock synchronisation would have to take place at regular intervals. Instead a two-wire serial interface similar to SPI will be used. SPI standard allows four timing modes, referred to as *mode 0*, *mode 1*, etc. Mode 0 will be assumed here – output is sampled at falling edge, input at rising edge starting at first edge after `nSS` is enabled. Waveforms are shown in figure 5.4. Its operating principle is very simple – it merely consists of a

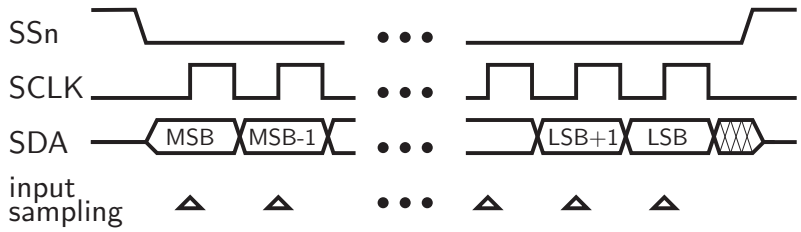


Figure 5.4: Waveform of SPI transaction

shift register with output from MSB tapped out as SDA. Reference clock divided by two is provided as SCK alongside the data for easy processing on receiver's side. Source code be written for example as in listing 1. This source code is equivalent to circuit diagram in figure 5.5. It is not a good design practice to place unregistered

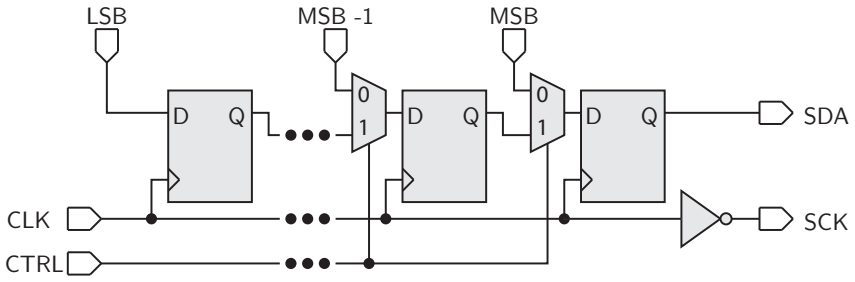


Figure 5.5: Schematic of data serializer

```
module shiftout(clk,ctrl,data_in,sck,sda);
        in clk;
        in [WIDTH-1:0] data_in;
        out sck,sda;
        reg [WIDTH-1:0] stored_value;
        assign sda=reg[WIDTH-1];
        assign scl=~clk;
        always@(posedge clk) begin
                counter<=counter+2'b01;
                if(ctrl==0) begin
                        stored_value<=data_in;
                end else begin
                        stored_value<={stored_value[WIDTH-2:0],1'b0};
                end
        end
endmodule
```

Listing 1: Serializer source code

logic elements before I/O pins, such as `assign sck=~clk` which is synthesised into an inverter between these two nets. In this particular case it is unlikely to cause any problems, because signal `sck` is used only for clocking flip-flops in shift register on receiving side. A minuscule propagation delay of the inverter has no effect, because inverting the clock relaxes setup time and hold time requirements. Relative skew between `sck` and `sda` up to almost $f_{sck}/2$ does not affect the ability of an off-chip receiver to reconstruct the register content.

Not shown in the code and schematic is the generation of control signal `ctrl`. It should be synchronous to `clk` and its on-time equal to or larger than $\tau_{clk} \cdot N_{bits}$. In its simplest form it is a plain clock divider. For 10-bit shift register division by 32 results in 16 clock edges for loading and 16 for shifting.

In this work two SPI-like interfaces are present – one input for setting numeric correction coefficients, and one output for reading out the final value.

5.5 Digital block top level

The purpose of the whole digital circuit is to provide a numeric value equivalent to ratio of its two input clock frequencies: reference clock $\texttt{clk}_{\texttt{ref}}$ and variable clock $\texttt{clk}_{\texttt{var}}$. When a counter clocked by $\texttt{clk}_{\texttt{var}}$ is gated by $\texttt{clk}_{\texttt{ref}}$, the counted value is equal to $\frac{f_{var}}{f_{ref}}$. Reference clock has to be much slower than $\texttt{clk}_{\texttt{var}}$ to provide reasonably large counter value. Counter can be implemented either as a ripple counter,

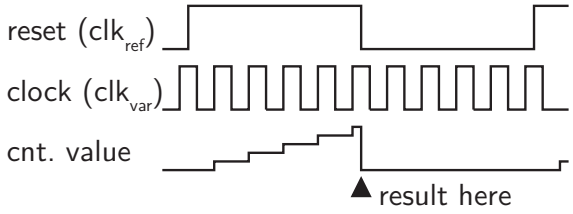


Figure 5.6: Principle of frequency measurement with gated counter

or more elaborately as a register with adder in feedback path. For n-bit counter, n D-type flip-flops and n half adders are needed. To reset the register after each counting period, asynchronous clear input could be used. However it is more area-efficient to use synchronous reset by placing a multiplexer before D input. With

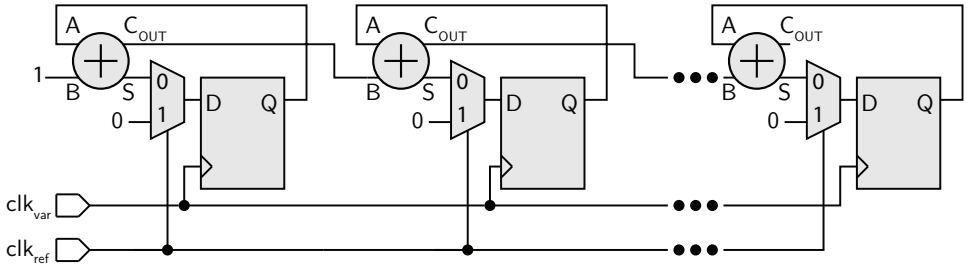
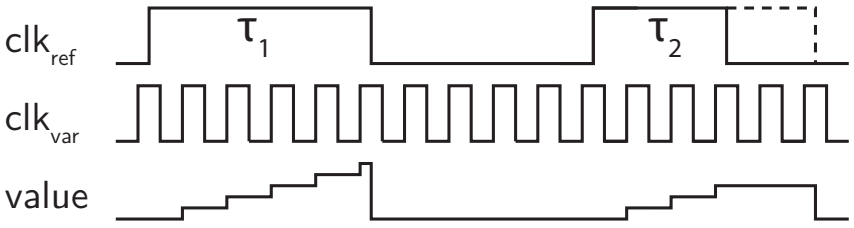
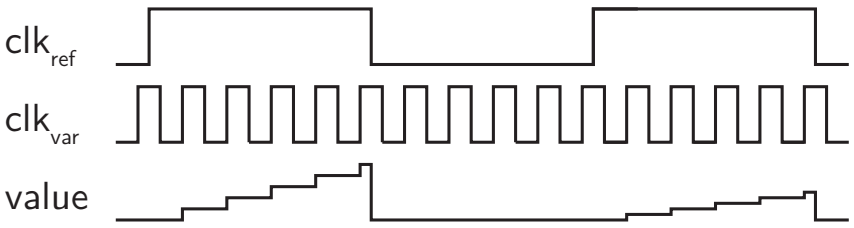


Figure 5.7: synchronous gated counter

this configuration counting always starts at zero. When a different initial value is needed, zero from multiplexer input is replaced with a suitable constant. For successful two-point digital trimming a circuit with transfer function $y = ax + b$ is needed. Additive constant b is provided by adjustable counter preload. Multiplicative constant a can be implemented in two ways: by changing the gating period or by changing the counter increment.



(a) Counter with variable gate period



(b) Counter with variable increment

Figure 5.8: Two possible implementations of adjustable digital gain

The latter approach was used Using variable increment requires extending the accumulating register with a fractional part. As derived in 3.3, 8 additional binary digits are necessary for adequate step size.

It is obvious that structures in figures 5.5 and 5.7 are very similar. They can be merged together by increasing the number of inputs at multiplexer feeding the D terminal of Dff. It is possible because counting and shifting do not occur at the same time. A clock multiplexer is used to switch accumulator clock between $\texttt{clk}_{\texttt{var}}$ for counting the frequency ratio, and $\texttt{clk}_{\texttt{ref}}$ for data readout.

Figure 5.9 shows the relative position of increment and preload registers to the main accumulator. Only the top 11 integer bits from accumulator are used for shifting

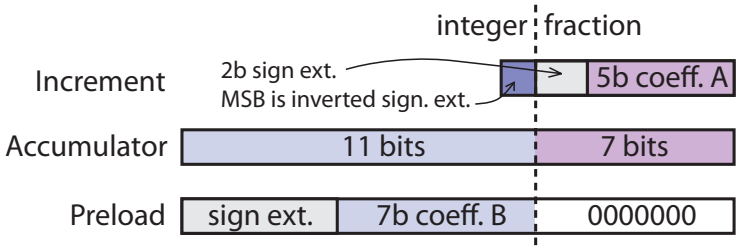


Figure 5.9: Register alignment

out the final value. The MSB of increment is formed by inverting MSB of coefficient A, which centers the available increment range around 1.

5.6 Behavioral description

Although it was not possible to use automated synthesis and placement tools, a behavioral code of the digital block was composed to serve as a reference for manual synthesis. Behavioral (listing 2) and gate-level (listing 3) versions were simulated side-by-side on a common testbench to ensure correctness of synthesised code. Not included in these source files is the input shift register for numeric coefficients. It is a simple chain of D-type flip-flops as described in section 5.4. Simple digital subcircuits described in 5.3.2 were used for synthesis. The finished circuit is not an exact 1:1 implementation, but it replicates the required behaviour with sufficient accuracy, results differ by 2 LSBs at most. Component `carry_adjust` mentioned in code is a chain of half adders (it sums upper part of accumulator with one carry bit).

5.7 Digital verification

Accuracy verification was started by running Monte Carlo analysis of the analog subcircuit. Transient analysis of approx. 10 periods was used. A simple MATLAB script was used to determine the required correction coefficients. These coefficients were fed into Modelsim together with the oscillation frequencies, to perform gate-level simulation. Output on serial interface was reconstructed into an integer to get the final results.

Simulation models assume every run is from different wafer, and chip-by-chip calibration is needed. However in real-world application, only a few samples from a wafer need to be measured. All remaining dice can then be calibrated by interpolation of the measured parameters.

5.7.1 Transistor-level simulation

A short simulation of all logic gates comprising the digital block was done in order to get more realistic estimation of the digital circuit behaviour. Because it takes a very long time to complete such simulation, only one case was conducted. Reference

```
module toplevel(clk_master,clk_var,multiply_const,add_const,clk_out,data_out);
        parameter INCREMENT_WIDTH=6;
        parameter ACC_WIDTH=8;
        parameter COUNTER_WIDTH=7;

        input clk_master,clk_var;
        input[INCREMENT_WIDTH-1:0] multiply_const;
        input[ACC_WIDTH-1:0] add_const;
        reg [COUNTER_WIDTH-1:0] count;
        reg[ACC_WIDTH-1:0] accumulator;
        output clk_out,data_out

        wire[1:0] state;
        parameter COUNTING_A = 2'b10,COUNTING_B = 2'b11,
                  SHIFTING=2'b00,RESTART=2'b01 ;
        assign state=count[COUNTER_WIDTH-1:COUNTER_WIDTH-2];
        assign clk_out=(state==SHIFTING)?(count[COUNTER_WIDTH-7]):1'b0;
        assign data_out=(state==SHIFTING)?accumulator[ACC_WIDTH-1]:1'b0;

        initial begin
                count=0;
                accumulator=0;
        end
        always@(posedge clk_master)begin
                count<=count+1'b1;
        end
        always@(negedge clk_out)begin
                accumulator<={accumulator[ACC_WIDTH-2:INCREMENT_WIDTH-1],
                                1'b0,{INCREMENT_WIDTH-1{1'b0}}};
        end
        always@(posedge clk_var)begin
                if(state==COUNTING_A || state==COUNTING_B)begin
                        accumulator<=accumulator+multiply_const;
                end else if (state==RESTART)begin
                        accumulator<=add_const;
                end
        end
endmodule
```

Listing 2: Source code of digital block

frequency was set to 93.36 kHz, variable frequency to 71.36 kHz. Precomputed correction coefficients were $a = 2$ and $b = -20$. A Verilog-A auxiliary loading circuit was assembled to load these numbers into the main circuit's registers. During simulation an output word of $01100010001_b = 785_d$ was received. This is in agreement with previous Verilog simulation, which for the same input yielded also 785_d.

5.8 Final schematic

Figure 5.11 contains the full schematic of the digital core, this schematic was used to generate layout instances of individual subcircuits.

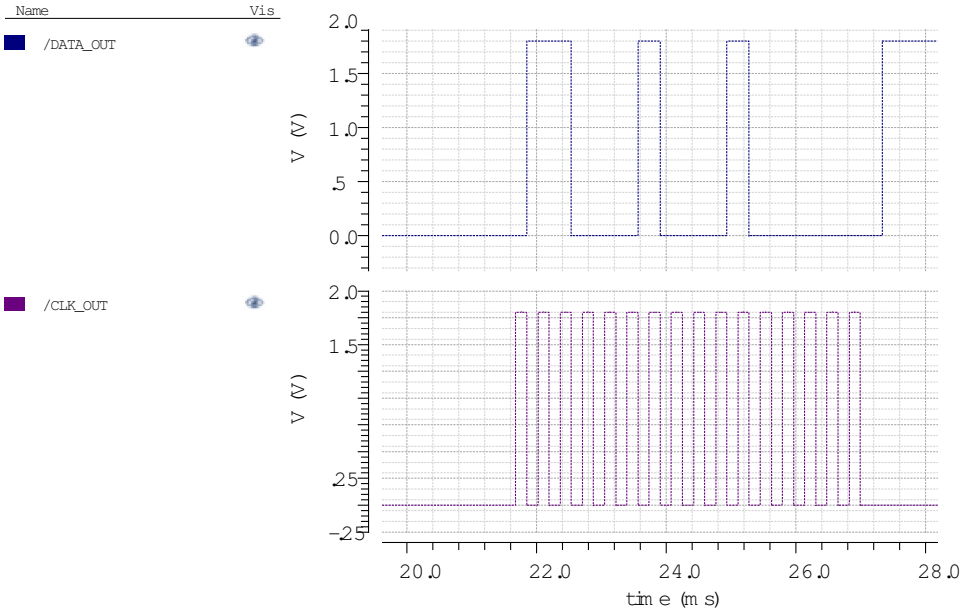


Figure 5.10: Transistor-level digital simulation

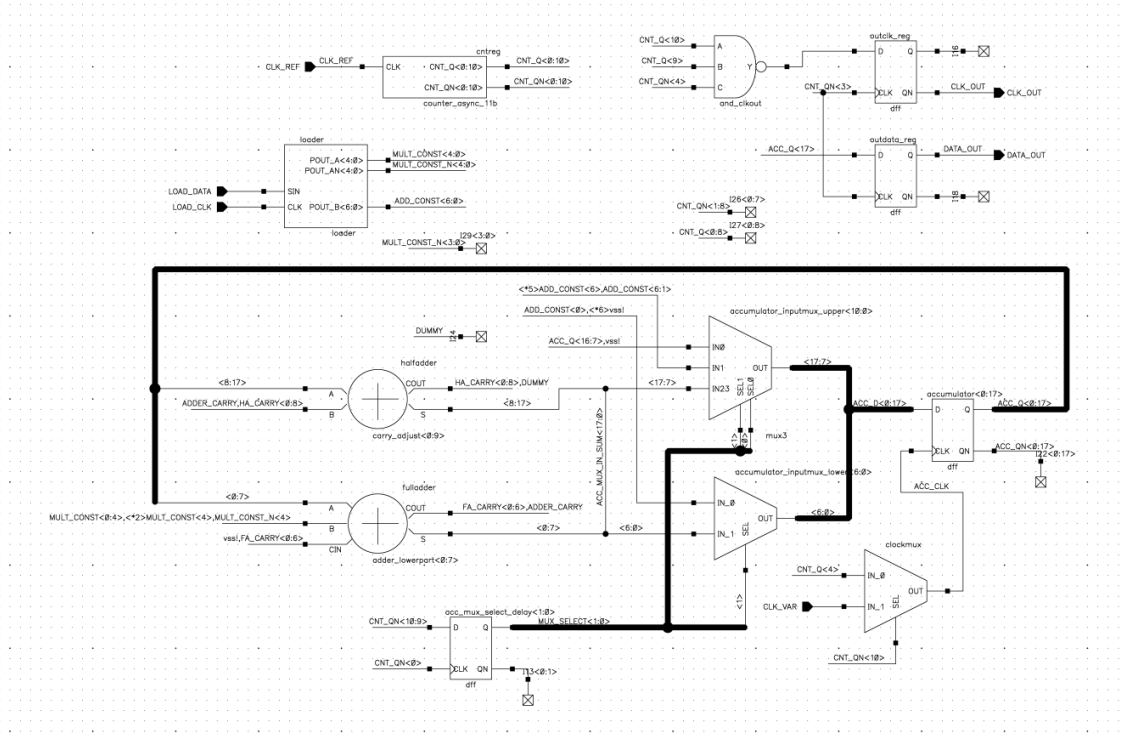


Figure 5.11: Full schematic of digital block

```
module toplevel_synth(clk_master,clk_var,multiply_const,add_const,clk_out,data_out);
        parameter INCREMENT_WIDTH=6,COUNTER_WIDTH=7,ACC_WIDTH=10;
        input clk_master,clk_var;
        input[INCREMENT_WIDTH-1:0] multiply_const;
        input[ACC_WIDTH-1:0] add_const;
        output clk_out,data_out;

        wire clk_master_neg;
        wire [COUNTER_WIDTH-1:0] cnt_qn_async,cnt_q_async;
        wire adder_carry;
        wire [1:0] mux_select;
        wire [ACC_WIDTH-1:0] acc_mux_in_sum,acc_d,acc_q,acc_qn;
        wire acc_clk,clkout_n_unreg,clk_out_n;

        genvar i;
        generate
        for(i=0;i<COUNTER_WIDTH;i=i+1)begin
                dff cntreg_0(.clk(i==0?clk_master:cnt_q_async[i-1]),
                             .d(cnt_qn_async[i]),.q(cnt_q_async[i]),.qn(cnt_qn_async[i]));
        end
        endgenerate
        mux_2 clockmux(.in_0(cnt_q_async[COUNTER_WIDTH-7]),.in_1(clk_var),.out(acc_clk),
                       .sel(cnt_qn_async[COUNTER_WIDTH-1]));
        inv clk_inverter(.a(clk_master),.y(clk_master_neg));
        dff #(.WIDTH(ACC_WIDTH)) accumulator(.clk(acc_clk),.d(acc_d),.q(acc_q),.qn(acc_qn));
        fulladder #(.WIDTH(INCREMENT_WIDTH)) adder_lowerpart(
                .a(acc_q[INCREMENT_WIDTH-1:0]),.b(multiply_const),
                .s(acc_mux_in_sum[INCREMENT_WIDTH-1:0]),.cin(1'b0),.cout(adder_carry));
        carry_adjust #(.WIDTH(ACC_WIDTH-INCREMENT_WIDTH)) adder_upperpart(
                .a(acc_q[ACC_WIDTH-1:INCREMENT_WIDTH]),.cin(adder_carry),
                .s(acc_mux_in_sum[ACC_WIDTH-1:INCREMENT_WIDTH]));
        dff #(.WIDTH(2)) acc_mux_select_delay(
                .d(cnt_qn_async[COUNTER_WIDTH-1:COUNTER_WIDTH-2]),
                .q(mux_select),.qn(),.clk(cnt_qn_async[0]));
        mux_3 #(.WIDTH(ACC_WIDTH-INCREMENT_WIDTH+1)) accumulator_inputmux_upper(
                .in_1x(acc_mux_in_sum[ACC_WIDTH-1:INCREMENT_WIDTH-1]),
                .in_01(add_const[ACC_WIDTH-1:INCREMENT_WIDTH-1]),
                .in_00({acc_q[ACC_WIDTH-2:INCREMENT_WIDTH-1],1'd0}),
                .out(acc_d[ACC_WIDTH-1:INCREMENT_WIDTH-1]),
                .sel (mux_select));
        mux_2 #(.WIDTH(INCREMENT_WIDTH-1)) accumulator_inputmux_lower(
                .in_1(acc_mux_in_sum[INCREMENT_WIDTH-2:0]),
                .in_0(add_const[INCREMENT_WIDTH-2:0]),
                .out(acc_d[INCREMENT_WIDTH-2:0]),
                .sel (mux_select[1]));
        nand3 and_clkout(.a(cnt_qn_async[COUNTER_WIDTH-7]),.b(cnt_q_async[COUNTER_WIDTH-1]),
                         .c(cnt_q_async[COUNTER_WIDTH-2]),.y(clkout_n_unreg));
        dff outclk_reg(.clk(cnt_qn_async[COUNTER_WIDTH-8]),.d(clkout_n_unreg),
                       .q(clk_out_n),.qn(clk_out));
        dff outdata_reg(.clk(cnt_qn_async[COUNTER_WIDTH-8]),.d(acc_q[ACC_WIDTH-1]),
                        .q(data_out),.qn());
endmodule
```

Listing 3: Synthesised code of digital block

Chapter 6
Chip Layout

The PDK used for layout contains 6 metal layers by default, which is very convenient for analog circuit layout. Metal layers 1 to 3 are used for routing almost all signals. Metal 4 is used primarily for global power and ground connections. Layers 5 and 6 are reserved for MIM capacitors. This way they may be placed on top of other circuitry and interconnect. It saves a lot of chip area, e.g. op-amp compensation capacitor occupies its entire boundary above transistors and resistors, effectively saving 50% in layout size.

6.1 Digital subcircuit

All digital components have uniform height of 8 µm. Transistors occupy only a small portion of the cell boundary, because a lot of space has to be reserved for metal connections. The chosen size proved as a good compromise, all connections could eventually be successfuly placed with not too much empty space remaining.

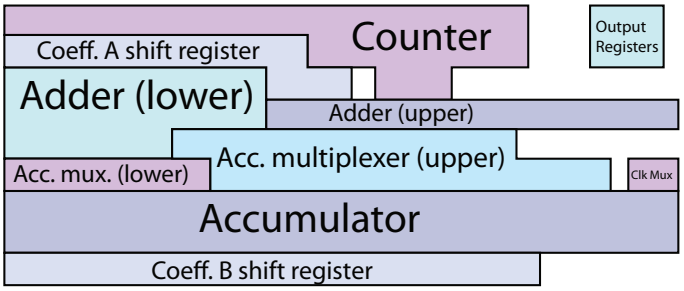


Figure 6.1: Digital block floorplan

6.2 I/O pads

Bonding pads are used for connecting silicon die to its package either by wires (wire-bond packaging) or by solder balls (flip-chip packaging). Shape and size of bonding pad depends on available bonding machinery, therefore it has to be adjusted to match the requirement of the packaging company. This design was not meant for actual manufacturing, and no recommended pad design was available for 180nm technology. The only feasible reference was bonding pad for 250nm, issued by Chip Implementation Center (CIC). These pads were reused with minor changes to pass DRC check.

6.2.1 supply pads

Supply pads make a direct connection with the IC's power rings. Because the chip has very low pin count, there is only one pad for Vcc and one for Vss. In larger

designs, more ESD-tolerant approach is typically used, such as one Vdd/Vss pair for feeding the power rings and another Vdd/Vss pair powering the internal circuitry, with protection diodes against the rings.

6.2.2 input pads

Input pads require the most attention, because CMOS gates are only several nanometers thick and are vulnerable to dielectric breakdown [8]. A simple means of protection is a gate-grounded NMOS (commonly referred to as ggNMOS), which works as a diode to absorb harmful voltage spikes. Such ggNMOS and ggPMOS transistors usually use non-silicided gates with high resistivity for increased robustness in terms of $I \cdot t^2$ product [9].

6.2.3 output pads

Output pads provide drive strength to off-chip signals, which have to travel through bonding wires, package leadframe and PCB traces. High drive strength enables signals to propagate at higher speeds, but also causes more electromagnetic interference. Since this IC works with external clock rates below 100 kHz, only a low-power IO driver is necessary. The presented buffer was designed to succesfully feed a common logic load (1kΩ||50pF) with rise and fall time around 20 ns.

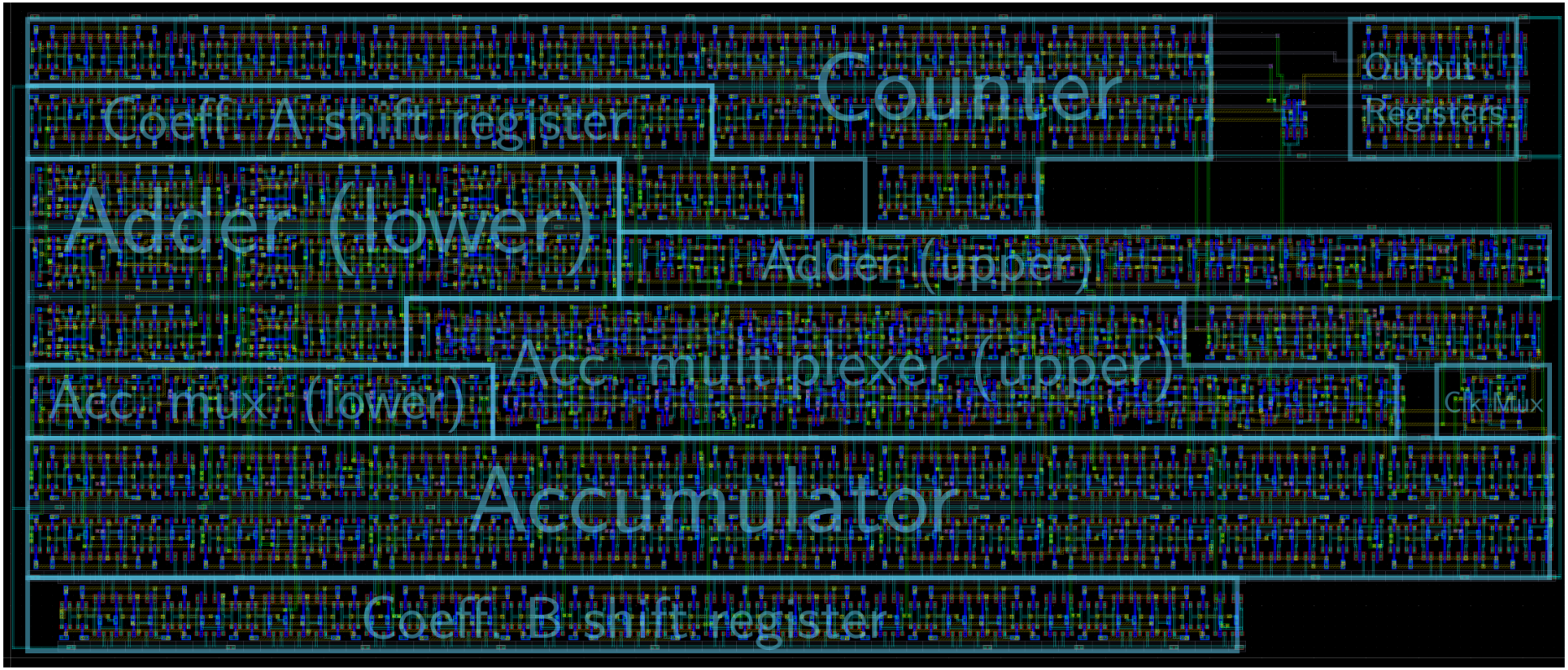


Figure 6.2: Full layout of digital block

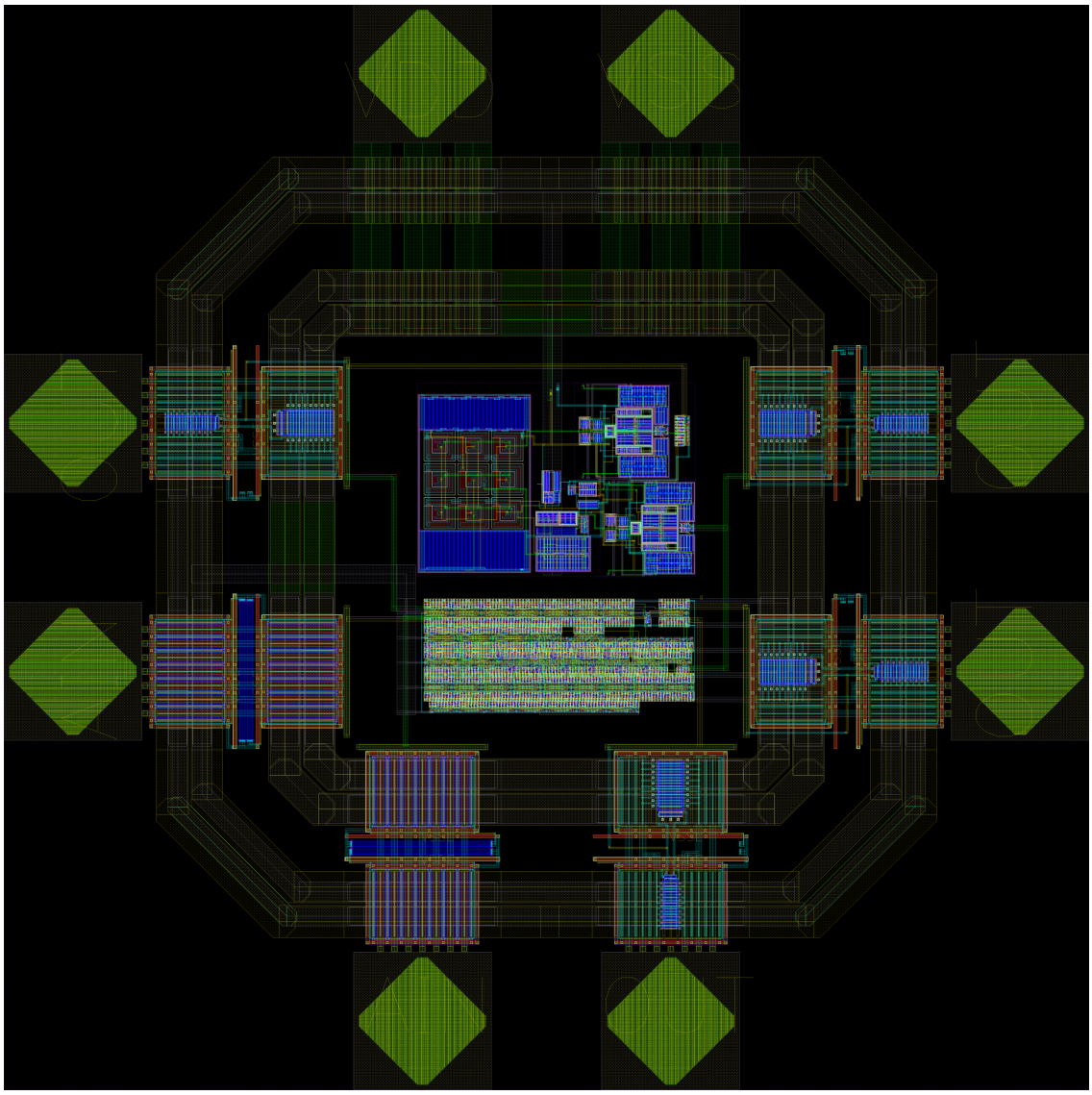


Figure 6.3: Full chip layout, including IO pins

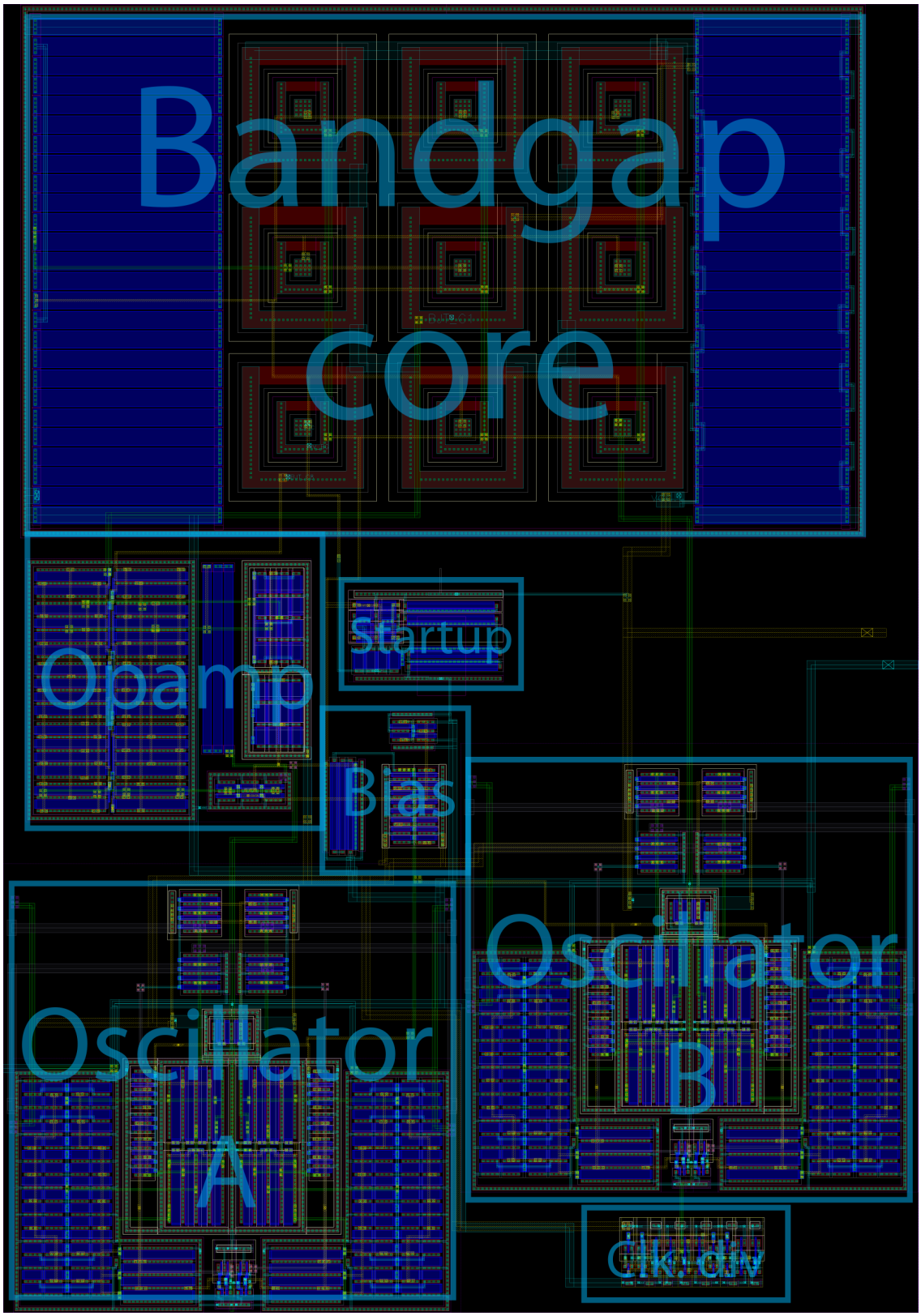


Figure 6.4: Analog circuits layout

Chapter 7
Discussion of Results

7.1 Simulation of post-layout netlist

After layout was completed, Calibre PEX tool was used to extract parasitic resistances and capacitances resulting from finite interconnect conductivity and proximity of devices. Although the results seem promising, they are incorrect. This is because extraction algorhithm does not take mismatch information into account.

Figure 7.1 shows 20 runs of Monte Carlo simulation. Contrary to previously seen significant variations (fig. 3.3), now all curves lie atop each other. Therefore it does not make sense to perform any trimming.

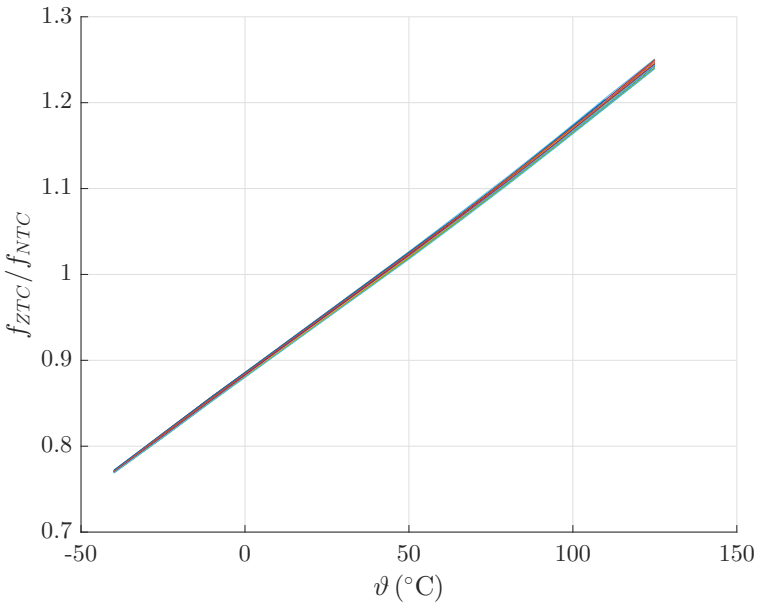


Figure 7.1: Post-layout simulation result

Parameter	This work	[2]	[10]	[11]	[12]	[13]
Node size	0.18 µm	0.16 µm	65 nm	0.18 µm	90 nm	0.16 µm
Sensor Type	BJT	BJT	MOSFET	MOSFET	Resistor	BJT
Accuracy (°C)	???	$\pm 0.15 (3\sigma)$	± 1.5	-1.4 $+1.5$	-0.6 $+0.8$	$\pm 0.1 (3\sigma)$
Supply Voltage (V)	1.8	1.5 to 2.0	1.0	1.2	0.8 to 1.2	2.5 to 5.5
Temperature range (°C)	-40 to $+125$	-55 to $+125$	0 to $+110$	0 to $+100$	-40 to $+125$	-55 to $+125$
Resolution (°C)	≈ 1	0.02	0.18	0.3	0.36	0.025
Conversion rate (SPS)	32	188	469k	30M	5k	10
Charge per conv. (J)	???	27.5n	1n	2.2n	2.36n	6.25u
IC core area (mm^2)	0.03	0.08	0.008	0.09	0.18	4.5
Calibration	2-point	Voltage	1-point	2-point	2-point	1-point
Architecture	Time-domain	Voltage-domain	Time-domain	Time-domain	Time-domain	Voltage domain

Table 7.1: Performance summary

Chapter 8
Conclusion

Temperature sensor IC with digital calibration was designed and simulated during the course of this thesis. A layout of the IC was finished, but it was never manufactured due to time limitations. Comparison with existing publication is difficult to make, because estimated accuracy is strongly dependent on mismatch models. In any case a useful feature of this design is the inclusion of serial data input and output, saving a lot of bonding pads and therefore also chip area.

Although initially the goal was to use only single-point calibration, it turned out to be extremely challenging because of device mismatch. Without actual samples it is hard to evaluate the effect of mismatch-cancelling layout techniques. Two-point calibration was eventually used, at the expense of making the digital portion more complex.

There is still room for improvement, especially in terms of working temperature range. Currently a reasonable accuracy is achieved between 10 °C and 100 °C. To make it usable for industrial applications, low temperature performance down to −40 °C has to be improved.

Occupied chip area is 0.348 mm^2. Most space is taken up by I/O pads and power rings. IC core measures $150 \times 150\,\mu\mathrm{m}^2$. approximately 40 % of this area is digital processing section. It could be made much smaller in case libraries for automated synthesis and placement were available. Using a different technology with smaller feature size would allow for some additional savings. However the overall IC size is dictated mostly by packaging constraints, which are independent of lithography process.

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