Czech Technical University in Prague

Faculty of Electrical Engineering

Doctoral Thesis

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Department of Electric Power Engineering

HVDC circuit breakers modeling in multiterminal grids

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Declaration

Hereby I declare that the thesis is the result of my own work done independently and all the references in the work are appropriately cited and listed in the list of references.

In Prague, 31.5.2017

Alexander Yanushkevich

Abstract

Transition towards sustainable energy systems lead to transformation of the existing electrical power grids. One of the key enabling technologies for this transformation is high voltage direct current (HVDC) technology that has range of advantages comparing to today's AC systems. One of the main obstacles for HVDC grids implementation is lack of robust and reliable protection systems for DC fault clearing. HVDC circuit breaker is a crucial component for DC fault clearing, however, performance of this new technology in multiterminal HVDC grids is not fully understood. Discussed nowadays innovative hybrid circuit breaker solution, that combines mechanical switches and power electronic components, is very different from AC circuit breaker technology. Application of power electronic components for DC fault clearing puts higher requirements on protection system where approach used in AC systems may not be optimal. Alternative multifeeder protection solution is proposed and investigated in the thesis. This solution brings benefitofthe protection system cost reduction and high speed fault clearing capability. In this thesis methods for HVDC components, including converter and circuit breakers, modelling are explained. Developed models are crucial for further protection systems development and optimisation. These models are used for performance investigation of the HVDC circuit breakers in multiterminal HVDC grids, radial and meshed. Results of the simulations performed in the thesis conclude into requirements for protection system and HVDC circuit breakers design.

Anotace

Přechod směrem k udržitelným energetickým systémům vede k transformaci stávajících elektrických rozvodných sítí. Jednou z klíčových technologií pro tuto transformaci je stejnosměrný přenos vysokého napětí (HVDC). Tato technologie má řadu výhod v porovnání s dnešními AC systémy. Jednou z hlavních překážek při realizaci HVDC sítí je neexistencedostatečně robustního a spolehlivého systémuchráněníproti DC poruchám. Jedním ze základních prvků ochrany proti DC poruchám je HVDC vypínač. Chování této nové technologie však není v sítích s více terminály (Multiterminal) dosud plně objasněno.V dnešní době často diskutované inovativní hybridní řešení HVDC vypínačů, které kombinuje mechanické spínače a výkonové elektronické součástky, je velmi odlišné od technologií AC vypínačů. Aplikace výkonových elektronických součástek pro odstranění DC poruch klade vyšší nároky na systém ochrany, kde nemusí být přístup používaný v AC systémech optimální. V rámci této práce bylo navrženo a prozkoumáno alternativní řešení vícevodičové ochrany. Toto řešení přináší výhodu v podobě snížení nákladů na systém chránění proti DC poruchámpři zachovánívysoké rychlostijejich odstranění. V práci jsou vysvětlenymetodymodelováníHVDC komponent, včetně měničů a vypínačů.Vyvinuté modely jsou rozhodující pro další vývoj a optimalizaci systémů chránění. Vypracované modely jsou použitypři vyšetřováníchování HVDC vypínačův radiálních a mřížových víceterminálových sítích. Na základě výsledků provedených simulací jsou doporučeny požadavky použitelné pro návrh systému chránění a HVDC vypínačů.

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1. Introduction

Transmission of bulk power over long and inter country lines has been seriously limited by system stability. Moreover, due to deregulated power market and large amount of decentralized generation in a meshed AC grid, an existing power system is becoming more complex. These limitations are triggering all sorts of problems and reliability issues in power systems. However, the recent advancement in power electronics has been pushing the boundary limit. As a result, the use of FACTS and HVDC devices has become growing in recent years. High voltage direct current (HVDC) technology has been considered as a viable alternative to AC systems for long distance power transmission and interconnection of power systems with different frequencies or networks which may not be synchronized. Besides, using fast DC power modulation implemented in a HVDC link's control system, the power oscillation in related AC power grids can be restrained timely, which is helpful to enhance the transient stability of the power system.

Moreover, the penetration of variable renewable energy sources in power systems around the globe has been increasing at an impressive rate in recent years. The EU aims at the 20-20-20 goals according to Energy and Climate Package one of which is the 20% share of renewable generations in the EU total consumption by 2020 and up to 30% in 2030. To deliver this energy to European consumers, it will require the development of a high capacity transmission system capable of delivering this energy to Europe's load centres.

The German transmission system, where implementation of renewable generation has been growing at the fastest rate, is facing challenges to maintain operation of the grid. At the same time as European grid is interconnected, problems in the German system affect grids in the neighbouring countries, like Czech Republic, Poland and the Netherlands, due to uncontrolled power flows.Implementation of the HVDC systems that have higher than HVAC transmission capacity in the same corridors and full power controllability can help to solve many problems existing today and upcoming in the future.

Plans for HVDC grids have been discussed in Europe and around the globe. Even first steps have been taken already by implementing small multiterminal systems. However, protection of an HVDC grid is considered as one of the main technical challenges for big system deployment. Protection system algorithms and prototypes of HVDC circuit breakers have been proposed. Effects of circuit breakers operation on the grid as well as methods for modelling of these devices are under investigation still.

1.1 Drivers towards HVDC grid

There are several drivers and challenges that need to be looked into while discussing the implantation of HVDC grids. The high-voltage high-power grid today is based on high-voltage alternating current (HVAC) technology. The large conventional generators connected to this grid are responsible for supplying power, keeping the frequency within the limits, and maintaining the voltage balanced throughout the nodes in the grid. The power flow has been predominantly unidirectional, i.e. from the generators to the consumers through the transmission and distribution systems. The power flow and voltage control in these grids has been relatively simple mainly because of the availability and predictability of the generators. In addition, transmission systems have been monopolies where the system security has been the main objective for control purposes. This has, however, changed in the recent past and the need for fast power flow control has emerged. Highvoltage direct current (HVDC) transmission system, whether it is conventional line-commutated converter (LCC) based or the modern voltage source converter (VSC) based, offers this functionality in addition to other benefits, such as lower losses and smaller transmission line corridor needed to transmit the same amount of power.

The past two decades have seen tremendous growth in renewable technologies such as wind and solar. The introduction of the renewables promises to mitigate the climate change and pollution problems through the replacement of fossil fuel powered electricity generating plants.The intermittency and unpredictability associated with renewables is proven to be a challenge for the transmission system operators (TSOs). Frequency is a measure of the balance between demand and supply of energy and has shown greater excursions around the nominal value. HVDC is an excellent solution for fast frequency control due to its characteristic fast power control functionality. In addition, offshore wind power plants (OWPP) are being built further offshore and AC transmission is technically not viable due to high charging currents that take up the entire thermal capacity of the cable connecting the OWPP to the grid system onshore. HVDC transmission does not produce steady-state charging currents and hence can be utilized for power flow over large distances.

Until recently, the electricity consumption was predicted in advance with a fairly degree of accuracy that enabled the amount of conventional generation to be adjusted to match this. As renewable generation cannot be changed easily (dispatched) due to its intermittent nature, the load has to be matched to maintain the power balance. The growth of the renewable share creates more, bigger and faster fluctuations of generation and leads to a paradigm shift from “generation matches load” to “load matches generation”. Variable generation from wind farms or solar installations have a rate of change much faster than the ramp rate of conventional generating

units and the present system for voltage control. This implies new challenges for power system operations, as well as the need for accurate forecasting.

The transmission grids are not evolving as quickly as the generation and consumption. The generation has become more dispersed and diversified and in the case of renewables, needs support from the grid rather than providing it. The growth in transmission capacity has not been in line with the growth of value and direction of power flows. This means the factors of safety are being encroached into and available stability margins are thin. The consumers are now more active and the trend is that of more active consumers as the smart grid technologies and business models are rolled out. In order for the grids to facilitate the power flows associated with these changes, grids have to be adequately equipped with fast power-flow control capability and voltage control functions.

CAVE-thinking (Citizens Against Virtually Everything) leads to public pressure to put more of the transmission system lines underground in the form of cables. This undergrounding trend will increase the investment level, as high voltage cable systems are more expensive than overhead lines. This trend might also speed up the development of an HVDC grids as HVDC cable systems become an attractive alternative to high voltage AC cables.

The liberalization and deregulation of electricity markets is resulting into increased transactions between neighbouring countries. Firstly, it is easier to control the flow of power over HVDC lines, which is ideal for power trade from one country to the other. Secondly, transmission grids of countries do not operate in synchronism in general and may have different grid control strategies. The only way to transfer power between such grids is through HVDC lines. That is why a vast number of country interconnectors have been built using HVDC.

In terms of capital expenditure, the substation costs for HVAC transmission is lesser than that of HVDC converter station; the reason being the elaborate AC/DC converter equipment and allied accessories for HVDC against a simple configuration of transformers and switchgear for HVAC operation. On the other hand, the cost of transmission line for HVDC is lower than that for HVAC. The reason is the need for smaller transmission towers and smaller number of conductors for HVDC transmission than HVAC technology. Therefore, above a certain length HVDC becomes the cheaper option. The cost summary is illustrated in Figure 1.1. The variable costs include the costs of losses which are lower for HVDC. The break-even distance is between 600 and 800 km for overhead lines (OHL) and between 80 and 100 km for cable transmission due to even higher AC losses and the need for reactive compensation along the transmission route[1].

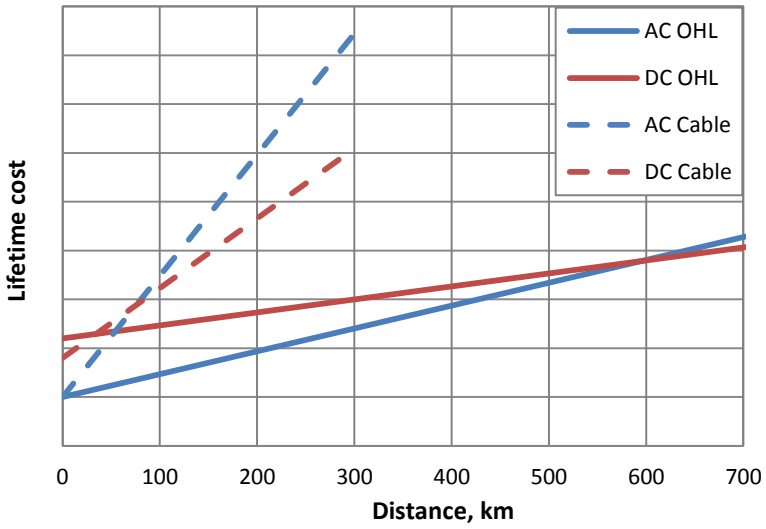


Figure 1.1: Comparison system lifetime costs as a function of transmission distance

Wind resource, even onshore, may be located further from the load centre. In the case of offshore wind, HVDC becomes the preferred option at very short distances as mentioned in the preceding section. The presence of an HVDC link between a wind farm and a grid system prevents the faults in one network from disrupting safe operation in the other. The fast power controllability associated with HVDC is another plus when integrating intermittent wind resource. In brief, HVDC makes integration of wind power with reduced costs, reduced losses, and higher security.

Offshore oil & gas production facilities have to employ fully-redundant gas turbines for their power demand. These take up valuable space on the platform that could otherwise be used for other purposes adding to the capacity of the facility. This solution entails high cost of production due to full-throttle operation of the standby generating unit. The CO_2 produced during use of these turbines is another cause for concern in certain countries. Norwegian authorities,for example, may ask offshore field developers to provide an economic comparison between offshore power production and powering from the shore solutions and employ the latter if it is comparatively economical. Due to this, few offshore oil & gas facilities on the Norwegian continental shelf have been powered from the shore; the first one being the Troll platform operated by Statoil [2].

In Europe the evolution of the HVDC Grid will be taken in steps. During next 10 years more than 60 HVDC projects are planned to be built. The first main development step foreseen to take place, in parallel to a few first regional multiterminal projects, is that the authorities planning a grid will require gridenabled pointtopoint systems that should be prepared for a future extension to a threeor more multiterminal system.

Until recently, majority of HVDC systems worldwide were point to point connection type. Point to point connections are very vulnerable to failure. Breakdown of any component can cause the failure of the complete HVDC connection leading to, generally, lower reliability of the system comparing to AC grids. In the past attempts were made to benefit from the same transmission corridor building radial multiterminal systems. Nevertheless, conventional LCC technology did not allow flexibility of the system operation and multiterminal systems were no developed further till recent years. Introduction of new flexible VSC based HVDC technology allows relatively easy implement multiterminal systems opening opportunity to increase reliability of the systems.

Development of multiterminal systems is seen to be crucial for wind energy integration and small island grids connection where is difficult to apply AC transmission. Offshore wind energy integration is strong component of EU targets towards low carbon future. While offshore wind share is becoming more significant in the European energy demand reliability of supply is getting more essential leading towards utilization of multiterminal HVDC systems.

Combining activities in offshore and onshore HVDC systems could lead towards overlaying continental SuperGrid [3], as shown in Figure 1.2, allowing integration of renewable resources and free energy trading. Long term plans for development of Continental SuperGrids have been discussed in Europe, Asia and North America. Nevertheless, it could take tens of years, same way it took 100 years to build European continental AC grid. On the way towards SuperGrid many challenges have to be overcome, as such as technical, economical and not the least political since it will involve international cooperation.

Figure 1.2: Concept of the future HVDC SuperGrid

1.2 HVDC converter technology

Line commutated converter (LCC) is a thyristor based technology that has been in operation for more than 40 years and used both for overhead and submarine transmission lines. In the past ten years, there have been a boom of development and deployment of LCC HVDC systems, mainly caused by construction growth in China. There HVDC is used for bulk power transmission from west part of the country, rich of hydro and wind resources, to the east part where the demand is mainly concentrated. Existing technology allows to transmit up to 6400 MW of power for bipolar line using voltage of ±800 kV. In the near future, upcoming technology for 7200 MW using ±1000 kV is expected. Development is going further to ±1200 kV HVDC transmission lines with 10000 MW of power rating. Due to use of thyristors application of LCC is possible only in strong AC systems with high short-circuit power. Except for China and India, development of LCC technology that has been going rapidly during last 15 years reached technical and feasible limits. Further increase in voltage level and transmitting power is limited byvulnerability of the power system due to loss of the HVDC line. Development of this technology in the range of 400-500 kV will be connected with decreasing costs and losses as well as compact design. LCC technology is not considered for multiterminal systems nowadays, mainly due to need of polarity reversal for power flow change and difficult control in a parallel multiterminal configuration [4]. However, two 3-terminal systems exist nowadays, in Canada [5] and Italy [6].

Voltage source converter (VSC) is an IGBT based converter technology. First VSC commercial application was presented in 1999 in Sweden [7]. VSC has an advantage over LCC due ability to connect systems with low short-circuit power like wind parks, offshore platforms or isolated power islands. Compared to LCC VSC technology has the following additional advantages [8,9]:

1) Simultaneous control of both active and reactive power. The AC voltage can be controlled at both stations.
2) Does not require any support from the AC grid it is connected to, and it can even be used for energizing an AC grid (black start capability).
3) VSC converters can operate without communication between the stations. It does not experience commutation failures and can support the AC grid by fast voltage control, thus minimizing the risk of commutation failures on nearby LCC links in case of a voltage drop.
4) In a LCC link the DC current always flows in the same direction, and the DC voltage polarity must change depending on the direction of power flow. A VSC converter always has the same voltage polarity but different current direction depending on the power

direction. VSC converters therefore can control the power flow continuously, which makes it easier to build multiterminal schemes.

5) VSC technology is more suitable for connecting decentralized onshore or offshore wind farms where robust and economical extruded cables could be used.

6) Smaller converter stations that reduce the space requirements.

However, VSC suffers from higher power losses and supplementary control complexity. Due to lower power capacity of IGBT compared to thyristor, the highest ratings of VSC are much lower than that of LCC systems. Nowadays, bipolar systems technology for power transmission up to 1200 MW using ±500 kV overhead lines or XLPE cables for land or submarine connections are available. Up to now, main applications of VSC systems are offshore wind park connection to the land and submarine cables interconnections. Since the technology is relatively immature, comparing to LCC, the high potential in development is expected, especially application of new semiconducting materials like SiC or GaN. These new materials have better electrical characteristics, less power losses and higher working temperatures. In the next 20 years rating of ±800kV and 4000MW for bipolar system could be available. Technology costs are expected to decrease in the future and that could lead to the move from LCC to VSC in high power transmission applications.

In Figure 1.3 ratings of LCC and VSC systems are presented, including systems proposed until 2025. It clearly can be observed that increase of the ratings for both LCC and VSC systems in upcoming years is expected.

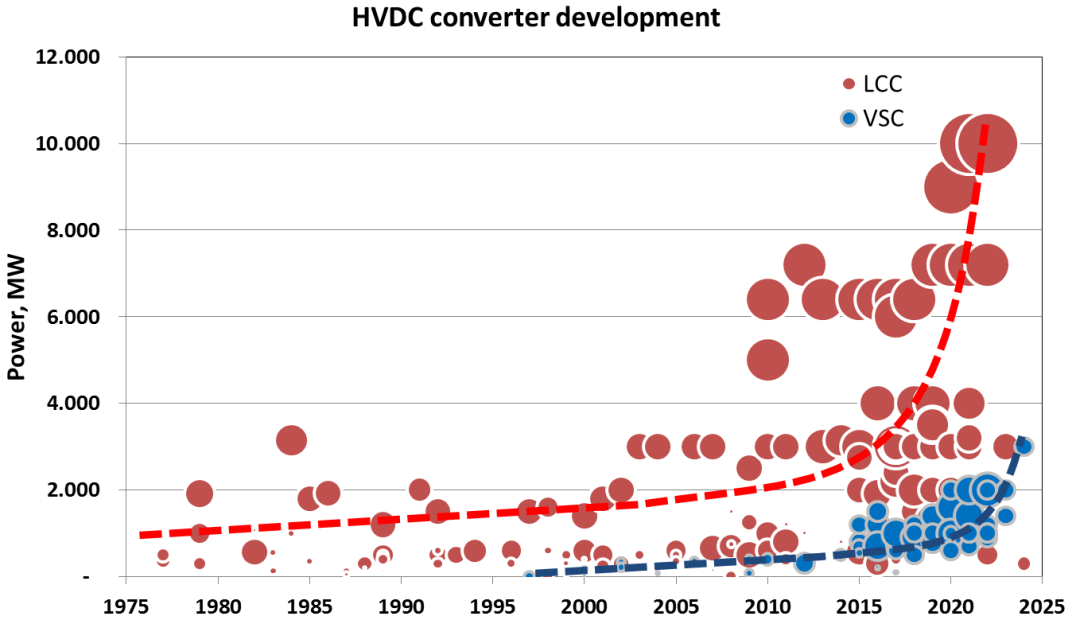


Figure 1.3: HVDC system ratings for LCC (red) and VSC (blue), size of bubble represents operational voltage, dash lines are trends

1.2.1 VSC system design

Further discussion is limited to VSC technologies, as itrepresents the best potential solution for multi-terminal HVDC transmission systems. The major components of a point-to-point HVDC connection are shown in Figure 1.4. The converter stations at ends of the DC line provide the interface between the AC and DC systems where power is extracted from the AC system (rectifier mode) or transfer power to it (inverter mode). As it is possible to transmit power both ways over a transmission corridor, these converter stations have the ability to switch from rectifier to inverter mode. Converter stations are equipped with AC/DC converter valves made up of power electronic modules, switchgear, converter transformers, and AC & DC filters (if required). The other major component is the transmission medium that can be either an overhead line or a cable. The materials employed are similar to those used in AC lines. The major difference is that HVDC lines can operate with two conducting paths in the line compared to three for AC transmission. In certain cases a metallic return is used to enable monopolar operation in case of a fault on one of the poles. In that case, 50% of the rated power can be transmitted.

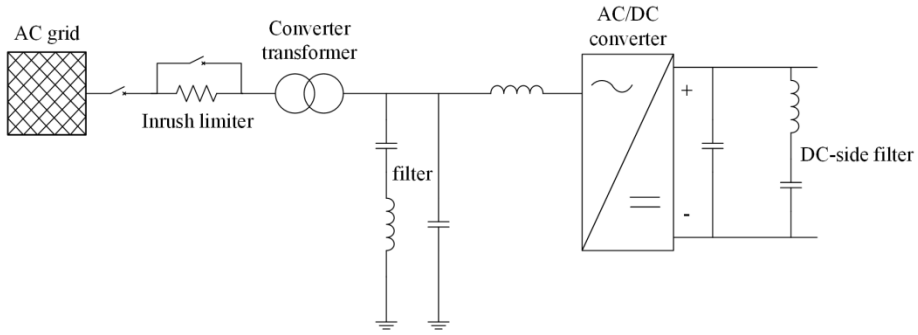


Figure 1.4: Schematic arrangement of major components in a VSC HVDC converter station

1.2.2 VSC modules design

For VSC two main approaches are used: pulse width modulation (PWM), often presented by 2 or 3 level converters, and modular multilevel converter (MMC). The pulse width modulated voltage source converter employs line of modules, depicted in Figure 1.5, in the valves for AC/DC conversion where the main components are:

1. A single self-commutating switch IGBT with antiparallel diode (ID)
2. The associated gate electronics (GE)
3. The snubber circuit (SC)
4. The antiparallel thyristor for protecting the anti-parallel diodes in case of AC fault (T)
5. The bypass switch (BS)

6. Busbars for connection to adjacent modules
7. Casing and cooling (surrounds the module)

The modules may be connected in series and/or parallel to enhance the voltage and/or current ratings respectively. The modules in this topology switch simultaneously requiring a single gate pulse. As the switches are self-commutating, they have to interrupt the rated current and high rate-of-change of current can produce high voltages across the modules due to their inherent inductances. Therefore, the snubber circuit has to be designed to protect the power electronics from voltage surges. This is the main reason which limits the voltage scalability of this technology.

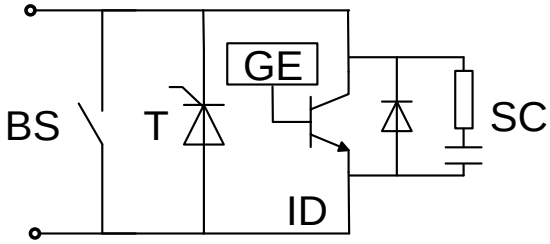
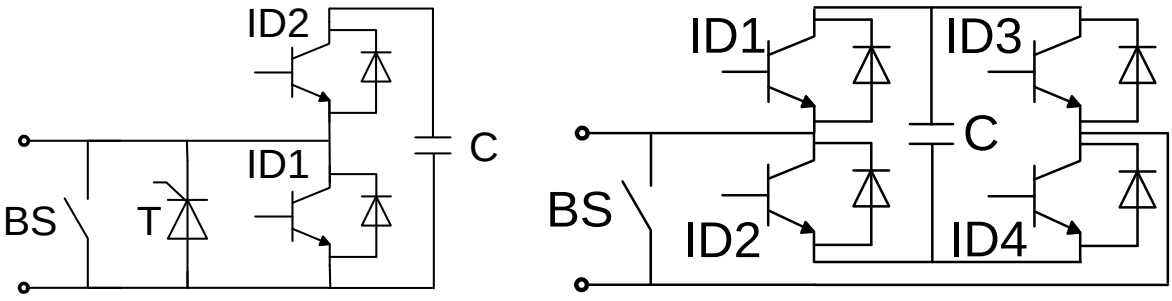


Figure 1.5: Schematic layout of the PWM VSC module

Inmodular multilevel converter (MMC) based VSC modules have similar design but arranged in a different configuration, half or full bridge, presented in Figure 1.6. When in PWD solution capacitor is connected in parallel to entire converter, in MMC each module has its own capacitor that allows achieving required operational voltage. The modules may be connected in series and/or parallel to enhance the voltage and/or current ratings respectively. The modules do not switch simultaneously and the control system for generation of firing pulses is fairly complex. Due to its design, this technology is more scalable in terms of voltage rating than the PWM VSC technology.



(a) (b)

Figure 1.6: An example schematic layout of a half bridge (a) and full-bridge (b)MMC modules

1.2.3 VSC converter design

Switching modules (SM) are collected into a valve connecting the AC line with one of the DC electrodes. All valves are housed in enclosures that perform the tasks of insulation and connection to other valves and equipment in the HVDC converter terminal. The valve cooling system is an auxiliary system that keeps the powerelectronic modules within specified temperature limits, and must be considered a critical sub-system for the operation of the HVDC station.A representation of a valve is given in Figure 1.7. The inductance L_s is often present to reduce the *di/dt* stresses on the power-electronic switches. The first subscript in the module numbering represents module number in the valve. The second signifies the position of the valve in the phase leg, "*u*" for upper and "*l*" for lower. The third subscript identifies the phase to which the specific phase leg is connected (*a*, *b*, or *c*). Finally, the last subscript refers to the shunt path for additional current capacity. The shunt connection of modules is possible in the PWM VSC converters only. In a three-phase system, three phase legs, each containing two valves, connect to three AC lines to form a three-phase AC/DC conversion system.

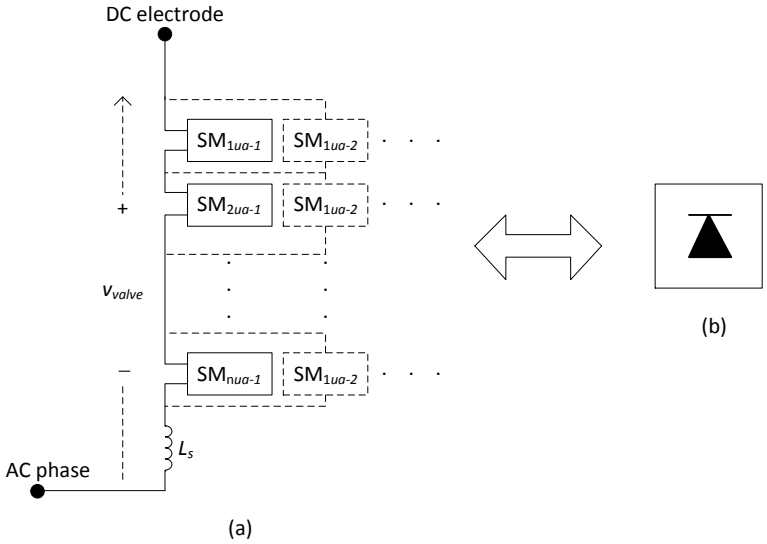


Figure 1.7: Multilevel converter valve arrangement (a) Schematically (b) Symbol.

The individual valves discussed above are connected to form a complete converter. The converter topology to be used in further discussion is the MMC VSC based solution, since this topology:

- offers modularity,
- lower losses as compared to other VSC topologies due to lower switching frequencies,
- lower harmonics distortion, no filters required, and
- is being supported more and more by the manufacturers and utilities.

The construction of a converter is shown in Figure 1.8, where six valves are configured in three phase legs to form a three-phase converter. The arm connecting a specific phase to the positive DC bus is known as the upper arm (indicated by the subscript ‘u’) and the one connecting the negative DC bus to a specific phase is called the lower arm (indicated by the subscript ‘l’). Each valve has a series inductor between the AC connection and the DC electrode.

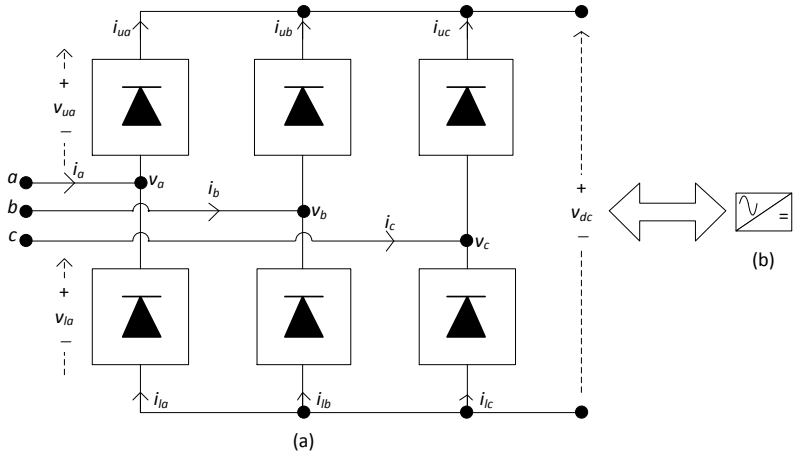


Figure 1.8: The three-phase MMC VSC (a) Schematic (b) Symbol.

1.2.4 VSCcontrol

The converter is supposed to behave like a synchronous generator, which controls its AC voltage magnitude and phase in response to certain control commands. The active and reactivepower exchange between the converter and the AC system follows the same set of rules and equations as in the case of exchange between a generator and an infinite bus.

The control of the converters is divided into the outer and inner control loops as shown in Figure 1.9. The first of the two outer control loops compares the active power and the converter DC-link voltage to their respective reference values and fed into a proportional-integral (PI) controller. The output of the PI controller is the reference d-axis current (I_d^*). Similarly another PI controller outputs the *q*-axis reference current (I_q^*) by processing the error between the reference and actual reactive power and AC voltage. These reference currents are then processed to form reference voltages for the converter. The switch-modulation control (not shown here) takes care of individual switching in the modules in the converter arms. The switch modulation in PWM VSC is simple in the sense that all the switches in a valve change their state simultaneously on a single gate command. The output voltage is, therefore, a train of high-frequency rectangular pulses, which has to be filtered by the switching-harmonic filter in order to get a sinusoidal voltage. In contrast, the switches in MMC VSC valve are given individual firing commands at different points in the cycle to synthesize a nearperfect sinusoid without the help of switching harmonic filters.

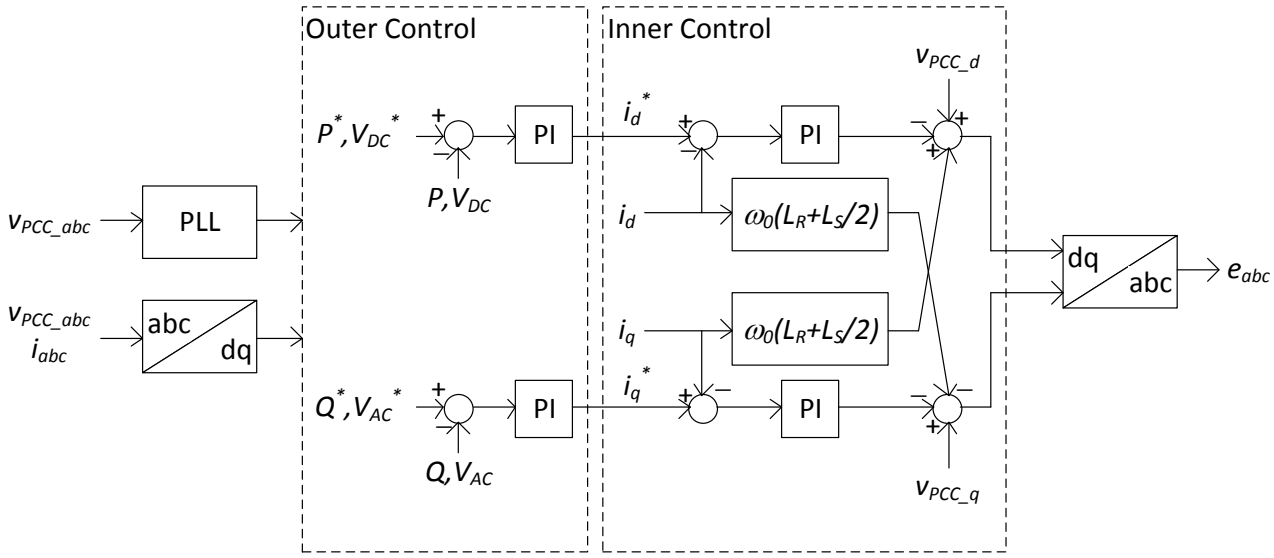
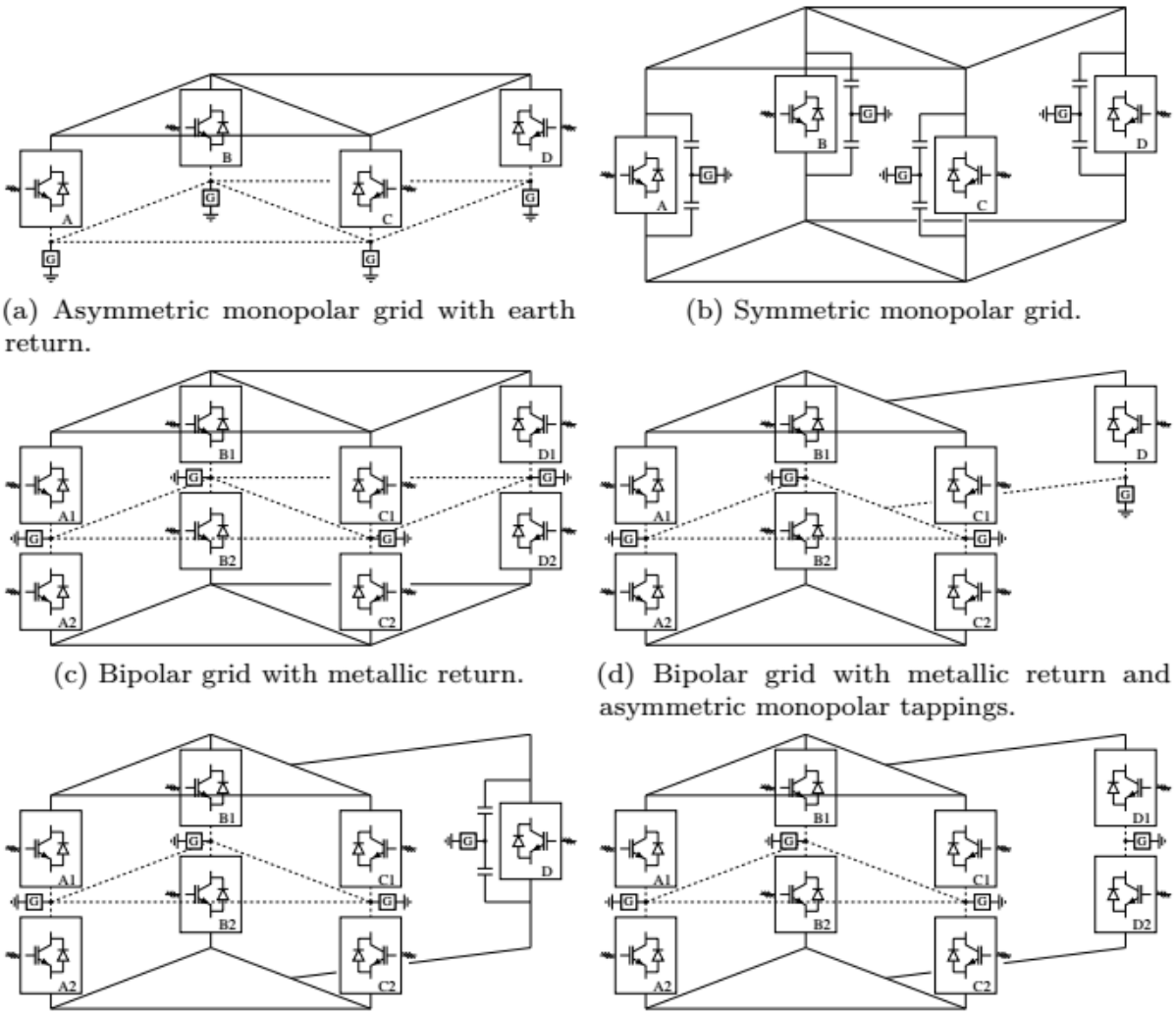


Figure 1.9: Major loops in the converter control system

1.2.5 Configurations of HVDC systems

In general, a point-to-point HVDC transmission system consists of a rectifier station, inverter station and a transmission line. There are mainly five kinds of point-to-point HVDC transmission schemes: monopolar earth return system, monopolar metallic return system, bipolar system with neutral point of one terminal earthing, bipolar system with neutral point of both terminals earthing and bipolar system with neutral line earthing. For earth return system, electric corrosion of DC earthing electrode and influence of DC currents on DC magnetic bias of neutral earthing transformers should be taken into consideration. Therefore, a monopolar earth return system is usually adopted by cross-sea power transmission projects or instalment-constructed bipolar system with one pole operating first.Topologies of multiterminal systems can have different configurations of monopolar, bipolar or combined type with metallic return or without. Examples of possible configurations are presented in Figure 1.10.



(a) Asymmetric monopolar grid with earth return.

(b) Symmetric monopolar grid.

(c) Bipolar grid with metallic return.

(d) Bipolar grid with metallic return and asymmetric monopolar tappings.

(e) Bipolar grid with metallic return and symmetric monopolar tappings.

(f) Bipolar grid with metallic return and bipolar tappings with earth return.

Figure 1.10: Possible HVDC grid configurations

2. Current status and aims of the thesis

Deployment of HVDC grids is limited by several areas such as components development, converter and DC system controls and grid protection against DC faults.HVDC components and system control have been developing in the past 20 years from the beginning of VSC technology. Protection of the grid, on the other side, is a relatively new topic as there are only few multiterminal systems deployed so far. In order to boost implementation of multiterminal HVDC grids, robust and reliable protection system against DC faults should be developed. A range of fault detection methods and HVDC circuit breakers designs have been proposed and studied. Number of developed prototypes has been studied in laboratory environment. Further chapters explain the state of the art in DC fault transient studies, fault detection methods and circuit breaker technologies.

2.1 DC fault transients in HVDC systems

The aim of this section is to introduce the transient behaviour of HVDC networks under DC fault conditions. Understanding of a short circuit phenomenon in HVDC systems is essential for development of protection systems and circuit breakers in particular. Due to relatively low impedance in HVDC systems rate of rise of short circuit current is much higher than in AC systems [10]. Resulting high short circuit current could damage components of the system leading to prolong outages. This chapter describes the method for calculation of short circuit phenomenon in VSC HVDC systems. Moreover, the influence of the main parameters of the HVDC and associated AC systems on the short-circuit conditions are discussed.

Simplified HVDC systems could be represented by a number of component blocks and parameters, see Figure 2.1. The HVDC converter divides a system into its AC and DC parts. The AC part is represented by AC source and AC system parameters, transformer and line inductance. The DC part, for point to point and multiterminal systems, includes DC system parameters, namely line resistance, inductance and capacitance. In case of a multiterminal system, potential circuit breaker current I_{fault} consists of two components: AC side current contribution $I_{AC}$from the nearest terminal and other terminals contribution I_{line} that consists of system capacitance discharge current and other terminal AC side contribution.

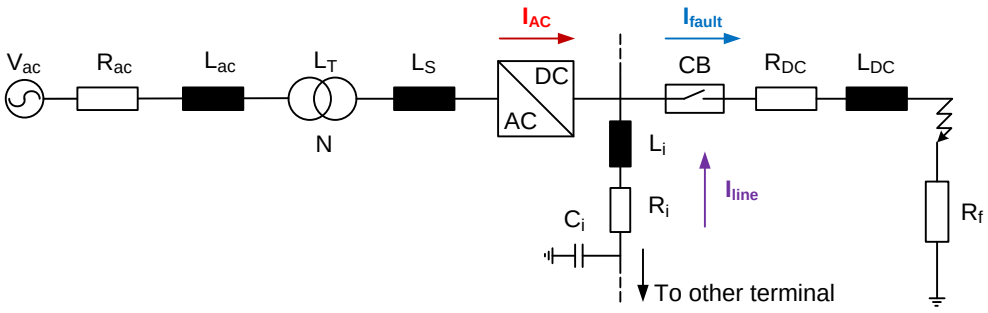


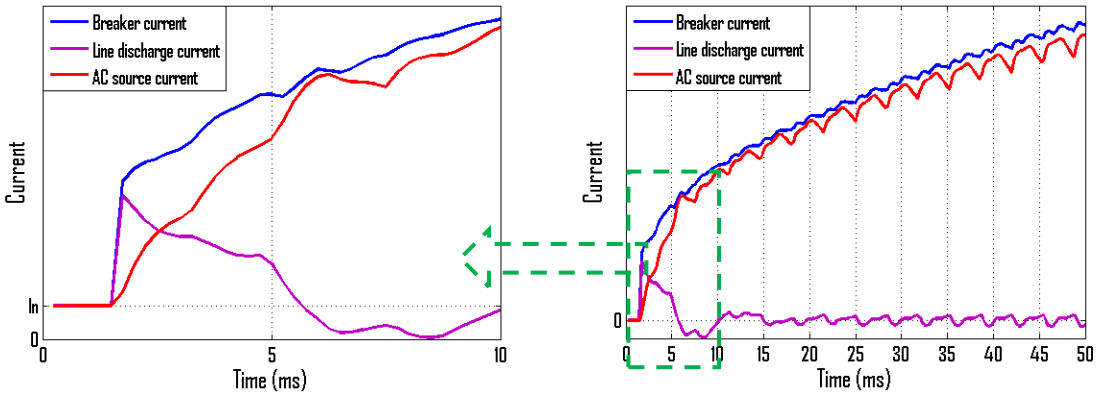
Figure 2.1: Single line diagram of HVDC system in case of DC fault

Generally DC fault current can be defined as follows:

$$i(t) = \frac{U}{R}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) + I_0 \exp\left(-\frac{t}{\tau}\right) \tag{2.1}$$

where $\tau = L/R$ is the time constant of the system, U is DC system voltage and I_0 is current prior the fault. From the equation (1) can be observed that if the current is not interrupted it reaches the value of U/R.

The detailed transient development of the short circuit current in HVDC systems is a complex phenomenon and depends on the value of many system and fault parameters. A representative example of the DC fault current development is shown in Figure 2.2.



Transient phase Short circuit development

Figure 2.2: Example of the representative fault current development

During the initial transient phase of the short circuit current development (i.e. typically within the first 5-10ms after occurrence of the fault), the following parameters are most important since they influence the discharging of associated capacitances:

a) The size of the capacitance in concentrated filter elements [11] or cables (solid insulated cables or overhead power lines) [12],
b) The length of the faulted line between the fault location and the circuit breaker [13],
c) The length and number of lines connected to the same busbar as the faulted line [14],

d) The size of a DC inductor (if used) [11] or the distributed line inductance (cable or overhead power line) [12],
e) The resistance of the fault [15] and the method of the system earthing [16],
f) The topology of the system and location of the fault [14].

The detailed quantitative influence of all these parameters has to be calculated for each and every situation individually, but a qualitative influence can be described and is universally valid. The amplitude of the initial transient capacitive discharge current increases with increasing capacitance such as that of DC filter elements or a number of lines connected. The larger the resistance in the short-circuit loop, the lower the amplitude of this transient peak. The resistance is slightly influenced by the length of the line between the fault location and the breaker, but mainly by the earthing scheme selected and the fault arc resistance. Any inductance introduced in a short circuit current loop decreases the rate-of-rise of short-circuit current but not the peak value. Thus, the rate-of-rise for overhead power line systems is lower than for cable systems since inductances are an effective means to reduce the short-circuit current.

The fault current waveform just after the fault occurrence is strongly dependent on the value of any fault limiting reactor installed in the system. This is because the main current component contribution comes from the discharge of the DC line capacitance and capacitors inside the converter flowing through the current limiting reactor. Consequently, a larger current limiting reactor value can limit the fault current rate-of-rise. This effectively reduces the DCCB interruption current requirement, assuming that it can operate fast enough, i.e. during the initial transient phase where the fault current has still not reached its steady state value. In order to reduce fault current rate of rise the use of fuses and superconductive coils was proposed and studied as well [17, 18].

The transient discharge of the DC-side capacitances results in a voltage drop in the DC system. This leads to an overcurrent through the converter valves, which are consequently blocked by theinternal protection system. In half-bridge VSC converters (PWM and MMC) when IGBTs are blocked, the bypass diodes or thyristors, protecting the IGBTs, bring the converter into an uncontrolled rectifier state providing a path for the fault current from the AC-side being injected into the fault. This leads to a further increase in the short-circuit current. If no measures to achieve interruption are taken, the short circuit current reaches a steady-state level within 10-100ms. In this steady-state phase the main parameters influencing the amplitude of the short circuit current are:

a) Topology of the system and location of the fault [14,19],
b) Converter technology [20-22],
c) SCR of AC systems [11],

d) Method of earthing [16, 20],
e) Fault clearing options such as partial system disconnection and circuit breakers action [20, 23, 24].

Again, an increase of the total resistance in the system between the converters and earth decreases the amplitude of the steady-state short-circuit current. The fault resistance, the earthing of the system and also the topology (weakly or densely meshed) all contribute to the total resistance. For symmetric monopoles in particular, there is no current loop established during a pole-to-earth fault and no steady-state contribution from the AC can occur. Obviously, weak AC systems (with a low SCR) contribute less to the fault-current amplitude than strong AC systems connected to the DC network.

2.2 DC fault protection systems

Due to lower impedance compared to AC in HVDC systems a DC fault propagates extremely fast and in few milliseconds it causes voltage drop in all the terminals leading to converters control capability loss [25]. Additionally, growing fault current increases the risk of damaging sensitive power electronics components.

Several methods of DC fault detection and protection have been investigated and implemented [26]. Nowadays, frequently used method is opening of AC circuit breakers on the AC side and, when DC system is disconnected, identifying the faulted feeder and isolating it from the rest of the DC system. After that DC system can restart its operation. This solution is very time consuming and may require more than 100 ms for full system restoration. This approach is acceptable in cable systems where DC faults are mostly permanent and no reclosing operation is required. Another option could be, in case if full bridge converters are used, to block converters and isolate faulted feeder by disconnecting it from the rest of the DC system [27, 28]. This solution is faster than the first one since there is no time delay caused by AC breakers opening and system restoration can be done in tens of milliseconds. However, it requires significant increase of IGBTs in the VSC converters, up to doubling comparing to half bridge solution, and therefore, increases cost of the system. The fastest solution is to apply DC circuit breakers that can isolate the faulted feeder in several milliseconds. Several concepts of HVDC circuit breakers have been proposed [29]. However, the optimal solution that allows fast fault clearing capability with acceptable losses during steady-state operation is the hybrid circuit breaker concept [30].

Reliable protection system for HVDC meshed grids is still under development and no universal approach has been proposed so far. Due to fast fault propagation and information processing and communication delay central fault protection is very challenging [31, 32]. Thus

local measurement is a preferable solution in order to identify the faulted feeder and trigger the circuit breaker in the shortest period of time [33, 34]. Detection of the fault based on the threshold values of voltage or current are not fast enough and do not provide high level of selectivity [35-37]. Another option could be measurement of the rate of change of voltage [38]. However, it should be taken into account that voltage fluctuations are very sensitive to changes in the system as well as external effects and, therefore, achieving reliable protection based on this approach could be very challenging. In certain cases when the fault is far away from the circuit breaker it can be difficult to distinguish if the fault is within the protected feeder. In this case higher level protection system based on more advanced algorithms and measurements may be applied to accurately identify the affected feeder.

2.3 HVDC circuit breakers

One of the key components limiting the deployment of multiterminal HVDC grid is absence of suitable DC breakers capable of interrupting DC fault current. This is due to strict practical challenges that these devices are required to satisfy. One of these challenges is the requirement that the DC switchgear must isolate the faulty section of the network in a very short time before the fault current reaches dangerous levels.

The breaking of DC current is technically demanding and consequently true DC breakers are considerably larger and more expensive than their AC counterparts. DC circuit breakers which exist today, mainly in medium voltage applications, normally consist of an AC circuit breaker plus an auxiliary circuit which creates a high frequency oscillatory current, allowing the arc to be interrupted when the current passes through zero. Alternatively DC breakers can be made out of semiconductor devices such as IGBT's, for example one half phase or the full-bridge circuit, is the equivalent of a single pole breaker whilst much faster than their mechanical counterparts, they would be considerably larger and more expensive, which will add to the costs of operating the DC breaker.

Development of HVDC circuit breakers has been started recently. The main reason is multiterminal systems construction planning. Nowadays, there is no standard design for HVDC breakers and, therefore, a lot of development is going on and opportunities for different design are available. Most of development is focused on research of breakers for VSC technology. One of the reasons for that is development of multiterminal systems using VSC technology where breakers are necessary. Another is lower ratings of VSC systems comparing with LCC.

Several technological areas where research and development is needed in order to improve or enable HVDC circuit breakers were identified and discussedin [29]. These areas are summarized in the list below:

- Optimization of existing HVDC circuit breaker scheme by optimizing the size of elements like capacitors, inductors, varistors, or charging units. Main goal is a reduction in size, interruption time, and costs.
- Optimization of switching arcs with respect to growth of oscillation and capability to interrupt by detailed investigation of arc characteristics under many different conditions for gas and vacuum circuit breakers. Derivation and verification of the parameters in mathematical arc models.
- Multi-physics simulation of HVDC arcs for high current (growing current oscillation) and interruption phase.
- Extension of medium voltage circuit breakers to higher voltage levels. Either by improving the technology, by series connection, or by applying breakers across medium voltage levels in multilevel converter topologies.
- Fast mechanical switches or disconnectors with high recovery voltage withstand and low on-state-losses. Ideally, these switches have sufficient arcing voltage for fast commutation. Use of such a switch in a hybrid circuit breaker.
- Pure semiconductor switch with minimal on-state-losses. Use of new wide band-gap power semiconductor devices, e.g. SiC or GaN.
- Fault current limiters for medium and high voltage applications.
- Combined optimization of the whole system: breaker-control-protection.
- New testing methods for HVDC circuit breakers or its individual components. Due to the strong breaker-network interaction, power hardware in the loop techniques would be advantageous.
- Standards and norms for multiterminal HVDC.

In common with AC transmission systems, a breaker failure scenario would need to be considered. This could be another series connected DC breaker, the converter itself, if it were of the full-bridge design, or the AC circuit breaker.

There are four main topologies for HVDC circuit breakers considered nowadays presented in Figure 2.3. Two topologies are based on breaking of the current in the mechanical switch and therefore they are called a mechanical type. In another topology fault current is interrupted by power electronic branch and it is called electronic type circuit breaker. The last one is a combination of both where fault current is commutated into power electronic branch by which is interrupted. Hybrid type has an advantage of lower on-state losses than an electronic type and faster fault blocking capability than a mechanical type. All topologies utilise surge arresters (SA) to dissipate inductive energy stored in the system when the fault current is interrupted. Often

circuit breakers have a current limiting reactor L_{cl} to reduce rate of rise of current and disconnector (D) to isolate the circuit breaker from the rest of the grid and eliminate leakage losses through the surge arresters. More detailed explanation of the operating principle can be found in Chapter 3.

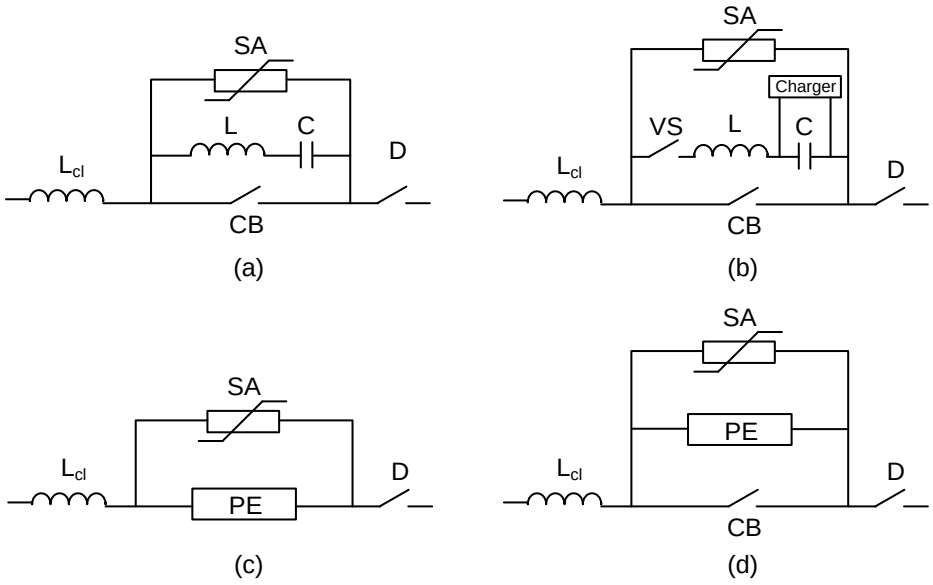


Figure 2.3: Example of HVDC circuit breaker topologies: (a) passive oscillation, (b) active oscillation, (c) electronic, (d) hybrid types

Depending on the demands and topologies of the multiterminal HVDC grids, converters and connected AC systems it may be appropriate to implement a variety of HVDC circuit breaker topologies. The parameters specified in the Table 2.1 represent proposed and hardware demonstrated results that are the state of the art at the time of writing. Regarding maturity of technology, whilst in some cases there may be significant work required to bring a topology to the full scale application, majority of the discussed designs have been proven in a laboratory environment and none are thought to be beyond a full scale prototype.

Several prototypes of HVDC circuit breaker have been discussed for future applications in multiterminal HVDC transmission systems. The choice of the breaker topology is likely to depend heavily on numerous network parameters; therefore, the decision is highly system dependent. With regards to the selection of specific circuit breaker topologies, extensive project specific investigation is likely to occur for each planned system, however some general observations based upon apparent trends can be discussed. It is expected that, besides current and voltage capabilities, the on-state losses and the current interruption time would be the critical factors. Based on this consideration further investigation is focused on modelling and analysis of performance of active oscillation type and several topologies of hybrid type circuit breakers.

Table 2.1: Summary of HVDC circuit breaker prototypes

Type	*Breaking branch*	*Current breakingtime (ms)*	*Breaking current (kA)*	*Voltage (kV)*	*On-state Losses*	*di/dt (A/μs)*	*Installation Costs*	*References*
Passive oscillation	Air Blast	12	4.0	500	Negligible	-	lower	[39]
	SF6 CB	14	2.2	500		-		[40]
Active oscillation	VI	< 5	2.0	400	Negligible	-	lower	[41]
	SF6 CB	20	1.2	250		-		[42]
	SF6 CB	30 -40	8.0	250		-		[43]
	VI	5	10.0	80		2.0		[44]
	VI	< 8	16.0	72		1.7		[45]
Electronic	PE	0.4	19.1	13.5	higher	47.8	higher	[46]
Hybrid	PE	2.4	16.0	80	lower	6.7	higher	[47]
	PE	2	7.5	120		2.9		[48]
	PE	3	15.0	200		5.0		[49]
	VI	2	15.0	450		-		[50]

Note: VI – vacuum interrupter, PE – power electronics

2.4 Aims of the thesis

In order to further implement HVDC grid, protection system against DC faults should be developed. To deliver reliable DC protection system future research should be focused on interoperability investigation of the protection algorithms and circuit breakers as well as how DC fault clearing effects operation of the HVDC grid. As discussed earlier a range of DC fault detection methods and HVDC circuit breakers designs been proposed and studied. Performance of HVDC circuit breakers in multiterminal system has not been studied extensively so far. This thesis is aiming to fill this gap and investigate operation of different circuit breakers topologies in multiterminal HVDC grids.

The work is divided in several steps:

- Create a model of HVDC converter that can be used for DC fault studies
- Create models of HVDC circuit breaker topologies
- Investigate DC fault conditions and influence ofthe grid parameters such as transmission media, converter type andtopology
- Investigate performance of different types of circuit breakers in multiterminal systems: radial and meshed topologies
- Conclude requirements for HVDC circuit breakers based on the results of simulations
- Propose cost effective solution for multiterminal grid protection

3. Working methods

In this chapter methods to design models for DC fault transient studies are described. The developed models are compiled to develop a database that is presented in Annex A. The database allows designing required topology of the grid with implemented HVDC circuit breakers to investigate performance of the HVDC grid and its elements during DC faults.

3.1 HVDC systems modelling

In this chapter, a replacement model for acomplex converter station modelshown inFigure 1.4in Chapter 1.2.1 is explained. This replacement model is developed in order to decrease the computation time of the simulation and eliminate the complex control parameters of the system. With a decreased computation time and no active control in the model, simulations of multiterminal systems become more feasible. Furthermore, the model only has to be valid during fault conditions as the behaviour of the circuit breakers during DC faults is investigated.

3.1.1 Converter model for DC fault studies

The proposed simplified model for an AC system and the converter is shown in Figure 3.1.

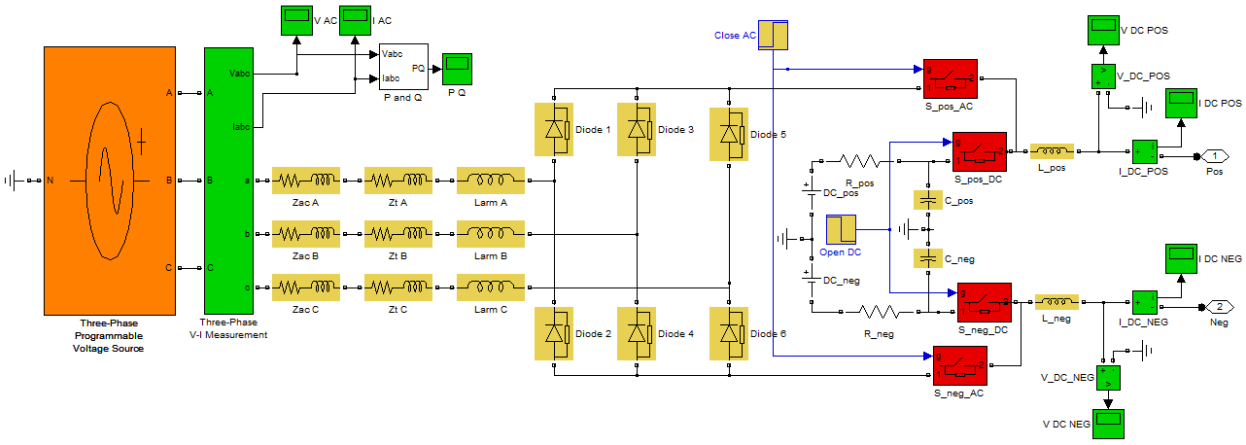


Figure 3.1: Simplified model converter station and AC system

The AC system showed in Figure 3.1contained a three-phase AC voltage source, output impedances of AC system that defined by AC system short circuit power (S_{AC}) and reactance to resistance ratio:

$$L_{AC} = \frac{U_{AC}^2}{S_{AC}} \cdot \sin\left(\arctan\left(\frac{X_{AC}}{R_{AC}}\right)\right) \cdot \frac{1}{2\pi f} \tag{3.1}$$

$$R_{AC} = \frac{U_{AC}^2}{S_{AC}} \cdot \cos\left(\arctan\left(\frac{X_{AC}}{R_{AC}}\right)\right) \tag{3.2}$$

The transformer modelled by the impedance of the transformer that is defined by short circuit impedance, nominal power and active losses.

$$R_t = \frac{\Delta P_k}{S_T} \cdot \frac{U_{AC}^2}{S_T} \tag{3.3}$$

$$L_t = \sqrt{(\frac{u_k}{100})^2 - (\frac{\Delta P_k}{S_T})^2} \cdot \frac{U_{AC}^2}{S_T} \cdot \frac{1}{2\pi f} \tag{3.4}$$

The controlled MMC IGBT bridge has been replaced by an uncontrolled three-phase diode rectifier. This diode rectifier simulates the blocking mode of the IGBTs during fault conditions. Parameters of the diodes and capacitance of the converter are derived from the topology of the converter and depend on the number of modules/levels in the arm and resistance of the single diode/thyristor.

$$R_{armdiode} = N_{arm} \cdot R_{diode} \tag{3.5}$$

$$C_{pos} = C_{neg} = \frac{3 \cdot C_{module}}{N_{arm}} \tag{3.6}$$

Inductance of the arm reactor can be defined using

$$L_{arm} = L_{pu} \cdot \frac{U_{AC}^2}{S_T} \cdot \frac{1}{2\pi f} \tag{3.7}$$

Inductance of the current limiting reactors L_pos and L_neg, that limit the rise of current from converter, is defined by the system design. Value of the inductance is limited by the effect on HVDC system stability as affect rate of current control [51]. Values between 50 and 100 mH could be considered acceptable.

Finally, the model is designed to set the initial conditions of the system and to connect the rectified voltage of the AC system when the fault is detected. Prior the fault is initiated, two DC sources (DC_pos and DC_neg) are connected to the output circuit to set the initial conditions and represent steady state operation of the converter. When the fault is detected, the switches S_pos_DC and S_neg_DCare opened to disconnect the DC sources and converter capacitors;at the same instance the switches S_pos_AC and S_neg_ACare closed. Changing of the converter state is done with consideration of the converter protection system delay.

3.1.2 Model verification

To verify that the simplified model is working correctly, three different simulations are compared: simulations of the complex model, simulations of the simplified model with and without setting initial conditions. In all three cases symmetrical monopole point to point system is considered; a fault at the rectifier side is simulated. Different system configurations and faults at other locations give comparable results, but those are not explained here. The hybrid circuit

breaker is implemented at the rectifier end in order to investigate stresses on the device. The results of the simulations are shown in Figure 3.2-3.5.

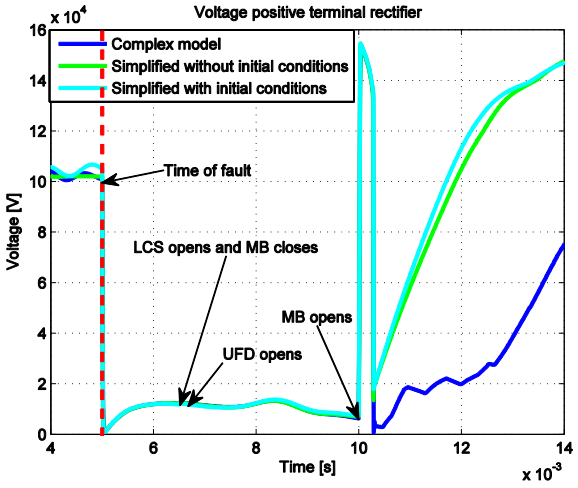


Figure 3.2: Rectifier positive terminal voltage

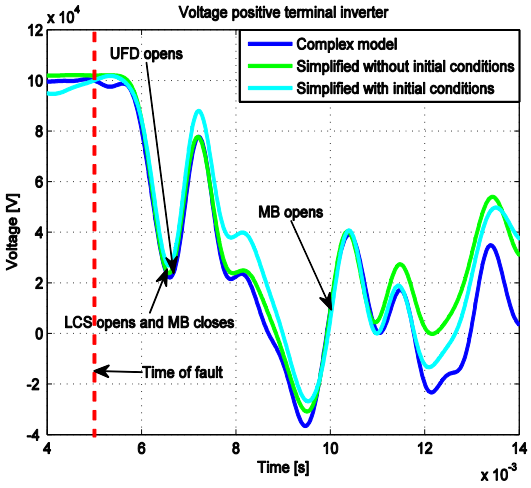


Figure 3.3: Inverter positive terminal voltage

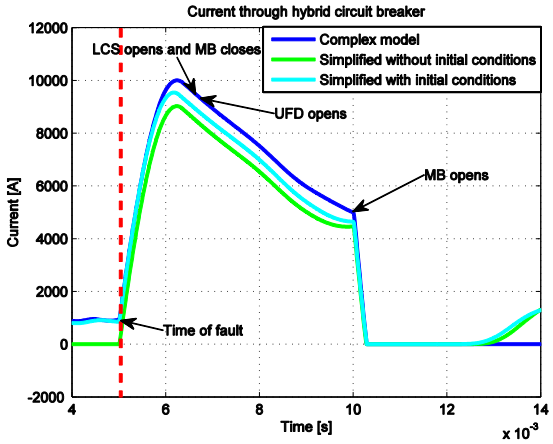


Figure 3.4: Current through hybrid circuit breaker

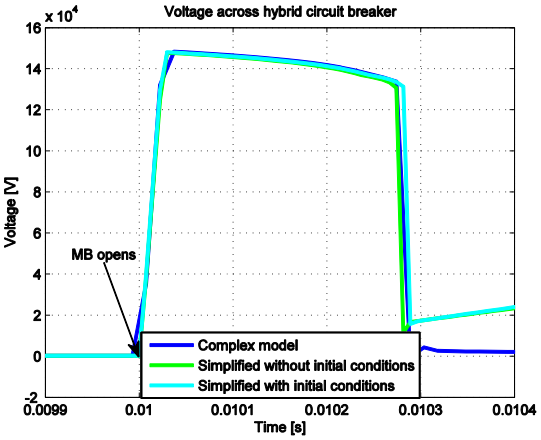


Figure 3.5: Voltage across hybrid circuit breaker

The simulation with the complex model takes almost two minutes, while the calculation time for the simplified circuit is below 10 seconds. This is a speedup of more than ten times which has even higher effect in a multiterminal system.Additionally, it avoids risk of control systems interaction between converters that can have negative effect on the results if not considered fully.Figure 3.2shows that the voltage at the positive terminal of the rectifier is almost the same for all three simulations, only the voltage recovery after fault clearance is different due to action of the control system inside the converters. Although it plays a role when continues grid operation is studied, in this work, where just circuit breaker operation is considered, these discrepancies are acceptable.

Figure 3.3shows that the voltage at the positive terminal of the inverter is almost the same for the complex model and the simplified model without initial conditions, whereas the

simplifiedmodel with initial conditions differs slightly. Figure 3.4shows that the current for all three simulations has the same behaviour, only some small differences in the values can be seen. Next**,** Figure 3.5 shows that the voltage across the breaker is almost identical during the fault. Because the results show little variations between the complex and simplified model, it has been concluded that the replacement model is working with acceptable accuracy for further investigations.

3.2 HVDC circuit breaker modelling

One of the key components limiting the deployment of a multiterminal HVDC grid is absence of suitable HVDC circuit breakers capable of interrupting DC fault current. This is due to strict practical challenges that these devices are required to satisfy. One of these challenges is the requirement that the DC switchgear must isolate the faulty section of the network in a very short time before the fault current can damage components of the network. It is also equivalently important to verify whether, upon their integration into HVDC grids, these HVDC circuit breakers meet the requirements demanded by multiterminal HVDC networks. There are two important aspects worth considering prior implementation of theHVDC breakers. The first is a clear understanding of the transient phenomena that the breakers are subjected to during switching operations, for instance, at time of fault clearing. The other is proper knowledge of the design and working principle of the circuit breakers themselves.

For these reasons in this further section a mechanical and four hybrid type circuit breakers are investigated in details and modelling principles are explained. Investigated circuit breakers contain several components that are similar and in the following sections these general elements and phenomena are described. Models of the investigated circuit breakers have been verified by comparison with results of the tested prototypes presented in the literature.

3.2.1 Hybrid circuit breaker

A hybrid circuit breaker generally consists of several branches: nominal current, current blocking and energy absorbing branches as presented in Figure 3.6. Nominal current branch has low steady-state power losses and consists of a mechanical switch and, in some topologies, additional power electronic devices for current commutation. Current blocking branch consists of power electronic devices and passive components in order to block the fault current. Speed and process of current blocking depends on the design of the nominal current branch due to mechanical switch opening delay. Energy absorbing branch is required in order to dissipate inductive energy stored in the system when fault current is blocked. Generally, metal oxide

varistor (MOV) is applied as energy absorbing element. It has similar design to a surge arrester used for overvoltage protection.

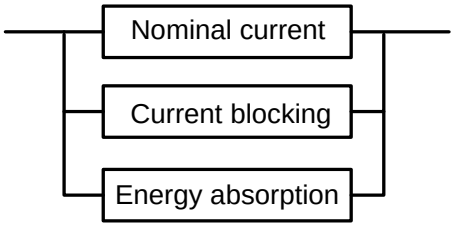


Figure 3.6: General design of a hybrid DC breaker

3.2.2 Current commutation

In order to divert fault current from the nominal current branch to the current blocking branch commutation circuit should be designed. In Figure 3.7 simplified electrical circuit for commutation during a pole to ground fault is presented, where L is inductance and R is resistance of the path between the voltage source and the fault location. Parameters L and R include AC system and AC transformer impedance, DC transmission line (OHL or cable) impedance and fault resistance. Nominal current branch consists of impedance L_1 and resistance R_1 that represent arc voltage in the mechanical switch or resistance of power electronic components installed. Current blocking branch consists of impedance L_2 and resistance R_2 of power electronic components.

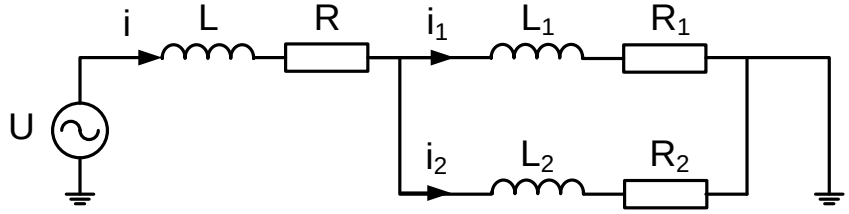


Figure 3.7: Electric equivalent of the hybrid DC breaker commutation circuit

In HVDC systems $R>>R_1$ and $L>>L_1$, hence solution for the fault current is

$$i(t) = \frac{U}{R}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) + I_0 \exp\left(-\frac{t}{\tau}\right) \tag{3.8}$$

where $\tau = L/R$ is the time constant of the system and I_0 is current prior the fault. From the equation (3.8) can be observed that if the current is not interrupted it reaches the value of U/R.

Current commutation process could be described by solving equations (3.9) and (3.10) for currents in nominal current and current blocking branches as defined in Figure 3.7.

$$L_2 \frac{di}{dt} + R_2 i = (L_1 + L_2)\frac{di_1}{dt} + (R_1 + R_2) i_1 \tag{3.9}$$

$$L_1 \frac{di}{dt} + R_1 i = (L_1 + L_2)\frac{di_2}{dt} + (R_1 + R_2) i_2 \tag{3.10}$$

In Figure 3.8 current commutation process is presented where t_{fault} is the time of the fault inception and t_1 is the time of the commutation process beginning that can be triggered by the action of the protection relay, and t_2 is the end of the commutation process when the current is fully commutated into the current blocking branch. Current I_0 is the steady-state current prior the fault and I_{NC} is the maximum current in the nominal current branch. Maximum value of I_{NC} can be limited by the capabilities of the power electronic components, installed in the nominal current branch, as they are dimensioned for current commutation only and not for the fault current blocking.

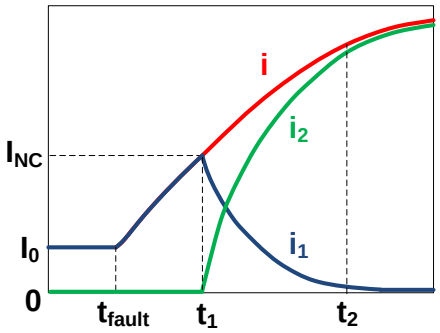


Figure 3.8: Illustration of the current commutation process

In order to commutate significant part of the current, resistance of the nominal current branch should be much higher than resistance of the current blocking branch in the end of the commutation process. For this reason switches with high arc voltage can be used in the nominal current branch. High pressure gas filled type switches have high arc voltage, however, they have lower contacts moving speed due to gas resistance. As alternative to reach high contact separation speed vacuum switch could be used [52], however, vacuum arc has relatively low resistance and thus could be supported by the power electronic switch [53].

3.2.3 Energy absorption

Energy absorption branch consists of surge arresters [54]. Number and parameters of surge arresters depend on the amount of energy that should be dissipated and limiting voltage. Limiting voltage is defined by the system design and voltage withstand capability of the protected devices [55]. Generally, considering typical surge arrester *U=f(I)* characteristics, the counter voltage amplitude must be set significantly higher than the maximum system voltage to prevent high leakage current through the breaker once the bulk of the energy has been dissipated. At the same time, the recommendation for basic insulation level for long term voltage exposure for DC equipment defines the upper limit for the DC breaker counter voltage. Considering that in hybrid breaker designs arrester's protection voltage value is set between 1.5 and 1.6 of the system

voltage. In the proposed circuit breaker design the surge arresters are disconnected from the grid during steady-state operation leaving more room for defining the surge arrester protective voltage in order to reduce stress on the components.

Development of the current through surge arrester can be defined using (3.11), where U_{sa} is limiting voltage of the surge arrester, U is nominal voltage of the system and I_{peak} is the fault current at the moment of current blocking, and $\tau = L/R$ from the circuit in Figure 3.7.

$$i_{sa} = I_{peak}\, exp^{-\frac{t}{\tau}} + \frac{U_{sa}-U}{R}\,(\, exp^{-\frac{t}{\tau}} - 1) \tag{3.11}$$

The duration of the current flow in the surge arrester t_{sa}, can be deduced by equalling to 0 the equation (3.11) and solving it for t. Energy dissipation time is important for concluding the fault clearing process preceding opening of the auxiliary switches.

$$t_{sa} = \tau \ln(1 + \frac{RI_{peak}}{U_{sa}-U}) \tag{3.12}$$

If the surge arrester voltage characteristics $U_{sa}=f(I)$ is replaced by the real characteristics it comes that the steady state current is never really interrupted. A "small" current flows through the surge arrester as long as a voltage difference appears across the circuit breaker. An expression for the energy that is dissipated in the surge arrester E_{sa} is now derived using equation (3.11) and (3.12) as follows:

$$E_{sa} = U_{sa} \int_0^{t_{sa}} i_{sa}(t)dt = U_{sa}(I_{peak}\, \tau - \frac{U_{sa}-U}{R}\, t_{sa}) \tag{3.13}$$

Characteristics of a surge arrester are unstable after reaching maximum operational temperature, generally 120^{o}C, and energy absorption capabilities are limited by thermal stability limit that is between 190°C and 220°C [56, 57]. The cool-down time typically lies between 45 and 60 minutes depending on the arrester type and the ambient conditions.

To define number of surge arresters required for the breaker equation (9) can be used, where k is a safety coefficient and $n_{op}$is the number of operations during cool down time. Number n_{op} can include reclosing operation as well as probability of the fault occurrence in the protected feeders during cooling time. During reclosing operation E_{sa} could be lower since only activation of the current blocking branch is required in order to define if fault was temporary. Energy absorption of a single surge arrester E' is limited by thermal stability limit of a MOV element in the surge arrester and defined in a datasheet as an energy value per kV of limiting voltage level.

$$N_{sa} = \frac{\sum^{n_{op}} E_{sa}}{E' U_{sa}}\, k \tag{3.14}$$

3.3 Hybrid Power Electronic HVDC Circuit Breaker type I

The electrical model of type I hybrid power electronic (HPE I) HVDC breaker based on the concept proposed in [47, 58] is shown in Figure 3.9. It can be seen from the model that this scheme consists of four parallel paths.

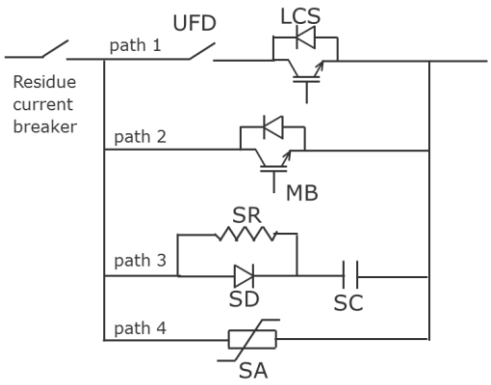


Figure 3.9:Electrical diagram of the HPE I HVDC circuit breaker

Under normal load operation, current flows through the branch consisting of the load commutation switch (LCS) and ultrafast disconnector (UFD). The load commutation switch is a power electronic switch that is able to carry the load current with low losses and it contains only a few modules of IGBTs required to commutate the current into the main breaker when ordered to interrupt.

When a fault is detected, the load commutation switch turns into blocking state while at the same time the main breaker switches on. The main breaker has several modules of IGBTs that can withstand higher voltage stresses compared to the load commutation switch. However, this branch has higher on-state losses and hence, this is the reason why it is used only during switching operations. The fault current is now commutated to the main breaker (path2). After the fault is fully commutated to the main breaker, the ultra-fast disconnector is opened to protect the load commutation switch against transient recovery overvoltage (TRV) at later stage. By the time the contacts of ultra-fast disconnector reach the position where it can withstand the TRV, the main breaker is switched off. The rise of TRV immediately follows the opening of the main breaker and soon it reaches the surge arrester protection level. By this time the surge arrester will be turned into conducting mode (path 4) and finally this branch will dissipate the magnetic energy in the system. Consequently, the fault current is interrupted. The snubber circuit (path 3) is included to control the rate of rise of TRV (du/dt) after the main breaker is switched off.

A disconnecting circuit breaker (residual current DC breaker) interrupts the residual current and isolates the faulty line from the HVDC grid to protect the arrester banks of the hybrid HVDC breaker from thermal overload.

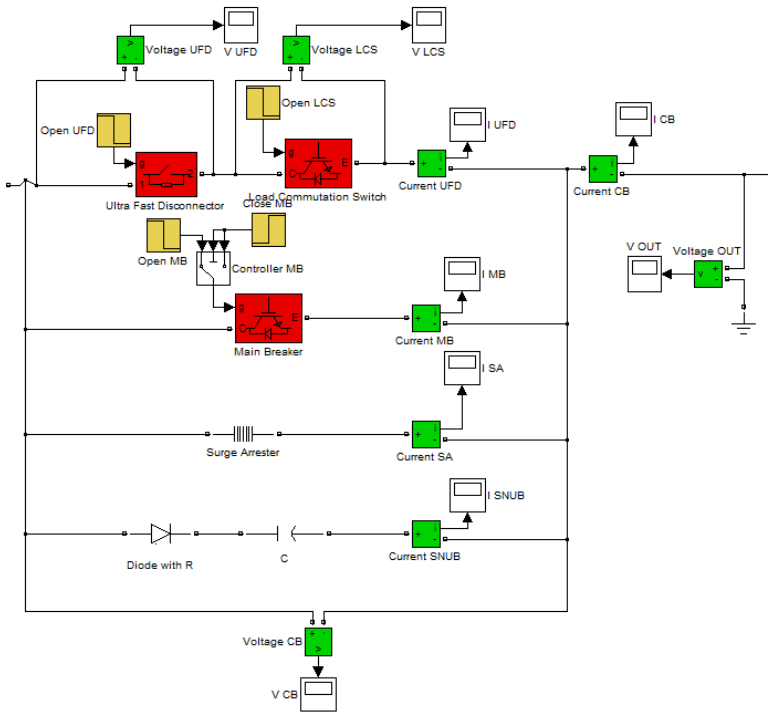


Figure 3.10:MatLab model of the HPE I HVDC circuit breaker

The MatLab model of the HPE I circuit breaker is presented in Figure 3.10. Dimensioning of the components are explained as following.

Ultra-Fast Disconnector (UFD). UFD isolates the LCS from the voltage stress built up across the main breaker during current blocking. It is modelled as an ideal switch that can operate only at zero current.

Load Commutation Switch (LCS). The IGBTs used in the simulation are designed considering the specifications of commercially available IGBTs. The number of IGBTs in this branch is mainly determined by the maximum expected current$I_{\mathrm{LCS,max}}$ that it has to commutate to the main breaker branch. The maximum voltage stress on this branch is low and is only dependent on stray inductance between LCS branch and main breaker branch. In this model a stray inductance between these branches is neglected. However, it has been shown in [59] that the maximum stress on this branch is well below the forward break over voltage of a single IGBT. Hence the equivalent resistance of the LCS can be obtained from the expression:

$$R_{\mathrm{LCS}} = \frac{I_{\mathrm{LCS,max}} * R_{\mathrm{IGBT}}}{I_{\mathrm{IGBT}}} \tag{3.15}$$

The above calculation results in the necessary number of IGBTs required while practically redundancy is introduced in order to avoid a stresses on healthy IGBTs when one of the IGBTs fails. Moreover, different topologies that result in lower power loss and higher reliability have been proposed in [59].

Main Breaker. The main breaker consistsof similar family of IGBTs used for load commutation switch. However, large number of series and parallel connected IGBTs are used in this branch in order to carry large currents and withstand higher voltages. The equivalent internal resistance of this branch can be calculated using the following formula:

$$R_{\mathrm{MB}} = \frac{I_{\mathrm{IGBT}} * R_{\mathrm{IGBT}}}{V_{\mathrm{IGBT}}} * \frac{V_{\mathrm{breaker}}}{I_{\mathrm{breaker}}} \tag{3.16}$$

As in the case of LCS, the above calculation results in the necessary number of IGBTs required to withstand the voltage and current stresses designated as V_{breaker} and I_{breaker}. In reality redundancy is included in order to enhance the reliability of operation. Recently, it has been suggested that in hybrid Power electronic HVDC breaker of this type, BIGT (Bi-mode Insulated Gate Transistor)is utilized because of its higher current carrying and voltage withstand capability.

Surge Arrester. This component serves two purposes; limiting transient recovery voltage and dissipating energy stored in the system after current is interrupted. The optimum surge arrester protection level is 1.5 times the operation voltage. The standard MatLab surge arrester I/V characteristic is modified and the design used in breaker model is shown in Appendix B.

Snubber Circuit. In order to reduce the du/dt stress during switching, each IGBT is equipped with resistor, capacitor-diode (RCD) snubber circuit. The typical HV IGBTs have a snubber circuits that limit du/dt to 300 v/μs. The series and parallel arrangement of the IGBTs in the main breaker will have an equivalent snubber capacitance calculated as follows;

$$C_{\mathrm{snubber}} = \frac{I_{max,IGBT}}{du/dt} * \frac{I_{Breaker}}{I_{max,IGBT}} * \frac{V_{max,IGBT}}{V_{breaker}} \tag{3.17}$$

Note that, the equivalent capacitance calculated above is based on the necessary number of IGBTs in the main breaker.

3.4 Hybrid Power Electronic HVDC Circuit Breaker type II

The model of the hybrid power electronic type II (HPE II) circuit breaker adapted from [48] is illustrated in Figure 3.11. It may consist of several parallel paths that are shown in the figure. The first branch designated as path 1 is a low impedance branch for carrying nominal current. It consists of UFD in series with power electronic switch (IGBTs) for bypassing short circuit current into the first auxiliary branch. The auxiliary paths consist of thyristors in series with capacitors which, during the commutation process, charge sequentially to a voltage proportional to the parting contacts of mechanical disconnector in low impedance path. In order to limit further increase of the voltage, the capacitors in first and second auxiliary paths, path 2a and 2b, have surge arresters in parallel. Besides, in these paths, relatively larger capacitors are

chosen to keep rate rise of voltage lower. When the UFD reaches sufficient separation, the auxiliary branch in path 3 starts conducting and, charges the capacitor C3. When voltage across C3 reaches protective level of surge arrester SA3 in path 4, current commutates to this path and magnetic energy stored in the system is dissipated.

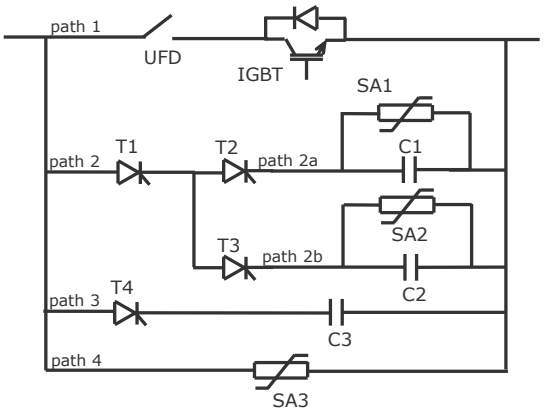


Figure 3.11: Electrical diagram of the HPE II HVDC circuit breaker

It is important to note that the UFD opens by the time current is fully commutated to path 2a. After current commutates to path3, the voltage across the breaker starts to build up to a protection level of surge arrester designated by SA2. This makes the current to commute to path 4 and finally cease to flow as the energy is absorbed by the surge arrester SA3. The commutation in several paths of the auxiliary branch is, therefore, important so that the breaker can handle the fault current until the TIV builds to a required level in controlled manner. It is important to note that, the protection level of surge arresters (and also the voltage across capacitors) at each branch is designed to exceed the protection level in previous branch.

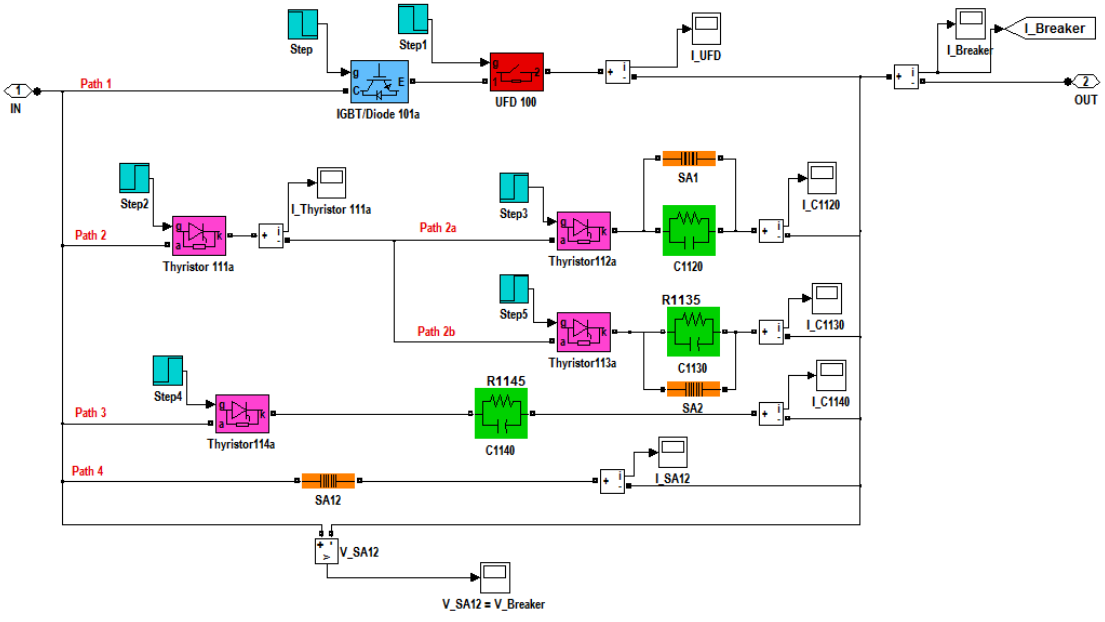


Figure 3.12:MatLab model of the HPE II HVDC circuit breaker

The MatLab model of the HPE II circuit breaker is presented in Figure 3.12. Dimensioning of the components are explained as following.

Ultra-Fast Disconnector (UFD). This isolates the IGBTs in the low impedance branch from TRV across the breaker. It is modelled as an ideal switch that can operate only at zero current. In MatLab, this is a single phase breaker set for breaking only zero current.

IGBTs. This are modelled based on standard high power IGBTs available from different manufacturers. These IGBTs have maximum steady state current $I_{max}$and internal resistance R_{IGBT}. Due to the parallel surge arrester and series UFD, the IGBTs in this branch do not have a burden of withstanding high voltage stress. Hence, the number of IGBTs to be used in this branch is mainly determined by the maximum expected current that it commutates to the auxiliary branch. Thus, the equivalent internal resistance of the necessary IGBTs in this branch can be calculated as follows,

$$R_{equivalent} = \frac{I_{\text{path1,max}} * R_{\text{IGBT}}}{I_{\text{IGBT}}} \tag{3.18}$$

For lower power dissipation and higher reliability, various series and parallel topologies can be utilized.

Thyristors. These are high voltage thyristors which are modelled based on commercially available ratings. Typical high power thyristor has forward blocking voltage $V_{max,thy}$, on-state voltage $V_{on,thy}$ and rated current$I_{max,thy}$. Thus, in order to handle larger voltage and current, these can be arranged in parallel and series. The total on state voltage drop and equivalent internal resistance are calculated, respectively, as follows.

$$V_{on,module} = \frac{V_{on,thy}}{V_{max,thy}} * V_{breaker} \tag{3.19}$$

$$R_{equivalent} = \frac{V_{on,module}}{I_{breaker}} \tag{3.20}$$

Note that thyristors 111a and 114a are the ones subject to full voltage across the breaker. Thyristors 112a and 113a are subjected to reverse voltage stresses from surge arresters SA1 and SA2 respectively. These can be designed based on protection voltages of the respective surge arresters. These thyristors have parasitic inductances which are approximated to be $1\mu H$.

Capacitors. The capacitors are the main reason of current commutation inside the auxiliary branches. The three capacitors in this branch can be determined based on the desired rate of change voltage across the breaker (TRV) and the current to be commutated at each step. Hence, in general it can be determined using the following expression.

$$C = \frac{I_{Breaker}}{dv/dt} \tag{3.21}$$

The capacitors in auxiliary branch are each protected by surge arresters as described in the previous section.

Surge Arrester. This component serves two purposes; limiting transient recovery voltage and dissipating energy stored in the system after current is interrupted. The optimum surge arrester protection level is 1,5 times the operation voltage. The standard MatLab surge arrester I/V characteristic is modified and the design used in breaker model is shown in Appendix B.

3.5 Hybrid Power Electronic HVDC Circuit Breaker type III

The electrical diagram of type III hybrid power electronic (HPE III) HVDC circuit breaker adapted from [60] is shown in Figure 3.13. This circuit breaker employs 4 current paths for interrupting fault current. During normal operation, current flows through the mechanical interrupter(s) in path 1. For mechanical breakers, vacuum interrupters are preferable due to higher arc voltage characteristics than in SF_6. When a fault is detected, the IGBTs in the main breaker (path 2) are turned on and the mechanical interrupters are opened. This results in the formation of an arc between the mechanical contacts. By the time the arc voltage exceeds the on state voltage of the IGBTs in path 2, current fully commutates to the latter, thus extinguishing the arc across the mechanical interrupter contacts. The speed of current commutation from path 1 to path 2 is dependent on the difference between the arc voltage and the on state voltage of the IGBTs as well as the stray inductance that exist between path 1 and path 2. The thyristors can be fired to allow reverse current to flow easily without overheating the reverse diodes of the main breaker in case if the fault current has opposite direction.

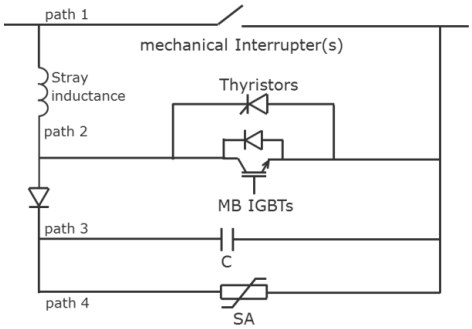


Figure 3.13: Electrical diagram of the HPE III HVDC circuit breaker

Once the vacuum breaker contacts reach sufficient separation to withstand the TIV, the IGBTs in the main breaker are turned off. This is instantly followed by rise of voltage across the breaker. The rate of rise of this voltage is restricted by the snubber capacitor (C) in path 3. In the same way as for the other HVDC circuit breaker schemes, the snubber capacitor charges up to

the protection level of the surge arrester in path 4, after which the energy stored in the system is dissipated in the latter.

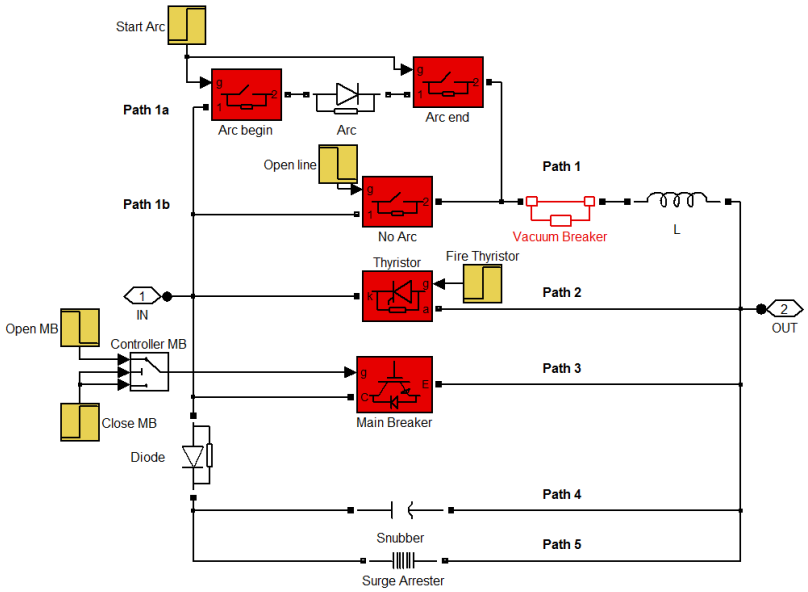


Figure 3.14: MatLabmodel of the HPE III HVDC circuit breaker

The MatLab model of the HPE III circuit breaker is presented in Figure 3.14. Dimensioning of the components are explained as following.

Vacuum Breaker. In HPE III a vacuum breaker is chosen because of its higher contact separation speed than in SF6. The typical arc voltage of a vacuum interrupter is in the range of 30 to 50V [61]. Depending on the voltage level of the breaker one or multiple vacuum interrupters can be used. In MatLab this breaker is modelled as a simple single phase breaker in parallel with a diode and another single phase breaker as shown in path 1a and b. The on state voltage across the diode represents the arc voltage. The single phase breaker in series with diode (path1b) can only be operated at current zero in order to ensure the arc is extinguished when current is fully commutated to path2.

Main Breaker (Power Electronic Switch). The main breaker consists of IGBTs which have on-state voltage of $V_{on,IGBT}$ at rated voltage $V_{max,IGBT}$current$I_{max,IGBT}$. These are modelled in MatLab as ideal IGBTs with mentioned ratings. In order to withstand higher voltage and conduct larger current several IGBTs, in a real application, are connected in series and parallel. The equivalent resistance of such an arrangement can be computed using expression:

$$R_{MB} = \frac{V_{on,IGBT}}{V_{max,IGBT}} * \frac{V_{Breaker}}{I_{Breaker}} \tag{3.22}$$

The expression for equivalent resistance shown above is obtained assuming only the necessary number of IGBTs required for a breaker rating. In real situation redundancy can be introduced for higher breaker reliability.

Snubber Capacitor.The snubber capacitor is required to restrict the rate of rise of TRV as well as to avoid any voltage surges that could result from stray inductance of the breaker during commutation. The voltage across this capacitor appears across the vacuum interrupter and the IGBTs. Therefore, the capacitance of this capacitor is set in such a way that the rate of rise of the voltage across its terminals is kept lower than the rate of rise voltage withstand capability of separating vacuum interrupter contacts. Mathematically, the capacitor value is obtained as:

$$C_{snubber} = \frac{I_{Breaker}}{dV_c/dt} \tag{3.23}$$

Surge Arrester. This component serves two purposes; limiting transient recovery voltage and dissipating energy stored in the system after current is interrupted. The optimum surge arrester protection level is 1,5 times the operation voltage. The standard MatLab surge arrester I/V characteristic is modified and the design used in breaker model is shown in Appendix B.

Stray Inductance. This is a parasitic inductance that exists in the conduction path from vacuum interrupter to IGBTs path. It determines the rate at which current is commutated from path1 to path2 shown in Figure 3.14. Accordingly, the stray inductance can be calculated using the following expression.

$$L_{stray} = \frac{V_{arc} - V_{IGBT}}{di/dt} \tag{3.24}$$

In the HPE III model, this inductance is assumed to be 1μH. Hence the rate of commutation can be calculated by rearranging the above expression.

Thyristor. This component exists only in a unidirectional model of this breaker. The main function of this thyristor(s) is to protect the anti-parallel diodes of each IGBTs from over current and damage during transient fault currents in the reverse direction. Typical high power thyristor has forward blocking voltage V_{Thyr}, on-state voltage $V_{on,Thyr}$and rated current $I_{max,Thyr}$. For higher current, a number of these thyristors can be arranged in parallel. The equivalent on state resistance of such an arrangement can be obtained as follows:

$$R_{on,Thyr} = \frac{V_{on,Thyr}}{V_{Thyr}} \cdot \frac{V_{Breaker}}{I_{Breaker}} \tag{3.25}$$

3.6 Hybrid Power Electronic HVDC Circuit Breaker type IV

Electrical diagram of thehybrid power electronic type IV (HPE IV) circuit breaker, based on the concept proposed in [50], is illustrated in Figure 3.15. This circuit breaker topology cannot be fully called hybrid as fault current is interrupted inside the vacuum switch and not by the power electronic components. However, as power electronic elements play a significant role in the operation of this circuit breaker, here it is considered of a hybrid type.

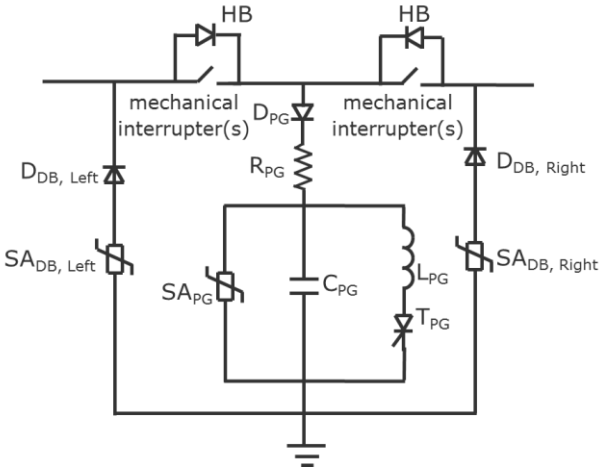


Figure3.15: Electrical diagram of the HPE IV HVDC circuit breaker

During normal operation, current flows through the mechanical interrupter(s), preferably medium voltage vacuum interrupters connected in series, in case of bidirectional operation. When a fault is detected, the vacuum interrupter(s) open establishing an arc between its contacts. In following step, the thyristor T_{PG} is fired and the pre-charged capacitor C_{PG} discharges through the inductor L_{PG} resulting in an oscillating output voltage. Because of the low impedance of the mechanical breakers, the voltage at the output terminal also oscillates. As soon as the output voltage of the circuit breaker becomes negative, the protection voltage of surge arresters in the damping branches, SA_{DB}, is reached and current flows through diode D_{PG} towards the mechanical interrupters. The opposite current creates a zero crossing of the fault current and results in extinguishing of the arc.

After the arc is cleared, the thyristor T_{PG} is turned-off at the next zero crossing. The capacitor C_{PG} is quickly charged to the protection level of surge arrester in the pulse generator branch designated as SA_{PG}. Once, the surge arrester starts conduction, it will dissipate magnetic energy of all the inductances in the system and as a result a fault is cleared. The voltage across this surge arrester counter acts the system voltage and finally, the remaining magnetic energy of the network is dissipated in this branch. Diode D_{PG} prevents capacitor from discharging and R_{PG} represents internal resistance of the components. It is important to note that the pulse generator capacitor does not require additional components for charging; it is charged to a nominal system voltage during normal operation.

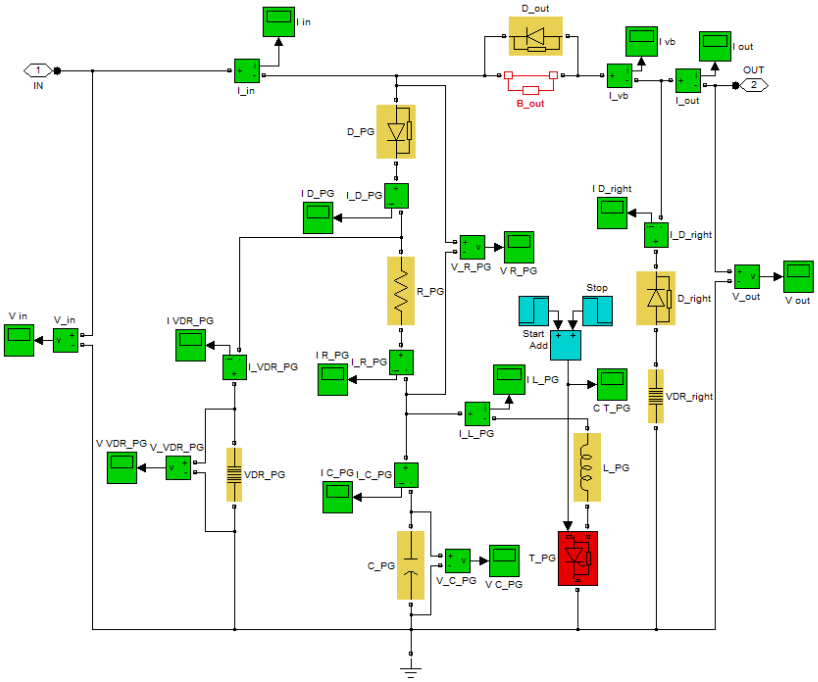


Figure 3.16:MatLab model of the HPE IV HVDC circuit breaker

The MatLab model of the HPE IVcircuit breaker (in this case unidirectional) is presented in Figure 3.16. Dimensioning of the components are explained as following.

Hybrid breaking unit (HB). The hybrid breaking units of this breaker employ very fast vacuum interrupters. A number of medium voltage vacuum tubes are used in series to cope up with the maximum voltage across the breaker. In MatLab, this branch is modelled as a simple single phase breaker that can be operated only at current zero. The diodes in parallel to the vacuum interrupters ensure current flow in reverse direction.

Damping Branch. The damping branches consist of surge arresters that limit negative overvoltage that could happen during breaking operation. The protection level of these surge arresters is very small and could be up to 15% of the nominal voltage. The series diodes in these branches avoid current flow in surge arresters during normal operation.

Pulse generator Capacitor. The capacitor in the pulse generator stays fully charged to the maximum line voltage at all times. The size of this capacitor must be chosen in such a way that (with properly sized inductor) it will generate the necessary pulse of required magnitude to create a current zero in the vacuum interrupters. It is also important to keep in mind that this capacitor determines the rate of rise of TRV after the arc has been extinguished. Thus, the choice of this capacitor is based on optimization process which includes current commutation speed, probability of current interruption at zero crossing (di/dt) and the level of stress (du/dt) on the system. Discharge current can be defined by:

$$i_c(t) = \frac{U_c}{\sqrt{L/C}} \sin\left(\frac{1}{\sqrt{LC}} \cdot t\right) \tag{3.26}$$

The magnitude of initial charge has to be chosen so that the largest expected fault current can be interrupted. Indeed, keeping this capacitor fully charged in practice is the main challenge of this circuit breaker.

Pulse generator Inductor. The value of this inductor is also chosen with reference to the amplitude of the pulse that is required to break the maximum fault current that can happen in the system. Hence, the optimum values of the capacitor and inductor are dependent on system in which the breaker is going to be employed.

Surge Arrester. This component serves two purposes; limiting transient recovery voltage and dissipating energy stored in the system after current is interrupted. The optimum surge arrester protection level is 1,5 times the operation voltage. The standard MatLab surge arrester I/V characteristic is modified and the design used in breaker model is shown in Appendix B.

3.7 Active Oscillation HVDC Circuit Breaker model

An electrical diagram of a generic active oscillation type HVDC circuit breaker is shown in Figure 3.17and is based on the solution proposed in [45].

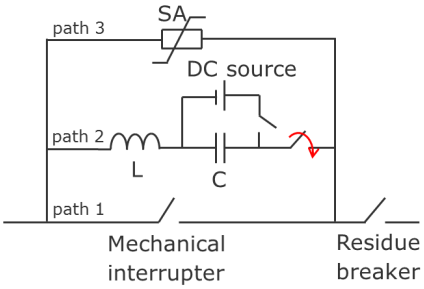


Figure 3.17: Electrical diagram of the active oscillation type mechanical HVDC circuit breaker

Under normal operation, current flows through the mechanical interrupter, (could be fast AC breaker), in path 1. When a fault is detected the mechanical interrupter is opened at full current, resulting in an arc. The entire fault current still flows through arc path. After the contacts of the mechanical interrupter are fully opened, the making switch in auxiliary path (LC branch in path 2) closes resulting in discharge of the pre-charged capacitor. Due to inductance in this path, an AC resonant current is superimposed onto the arcing fault current through the mechanical interrupter, thus creating a zero crossing for extinguishing the arc. After arc is extinguished, current commutates to LC branch and re-charges the capacitor again. As a result TRV builds up ultimately reaching the protective voltage of the surge arrester. At this moment the fault current commutates to the surge arrester branch (path 3). Finally, the surge arrester absorbs magnetic energy stored in the system as a consequence of which the fault current decays to zero.

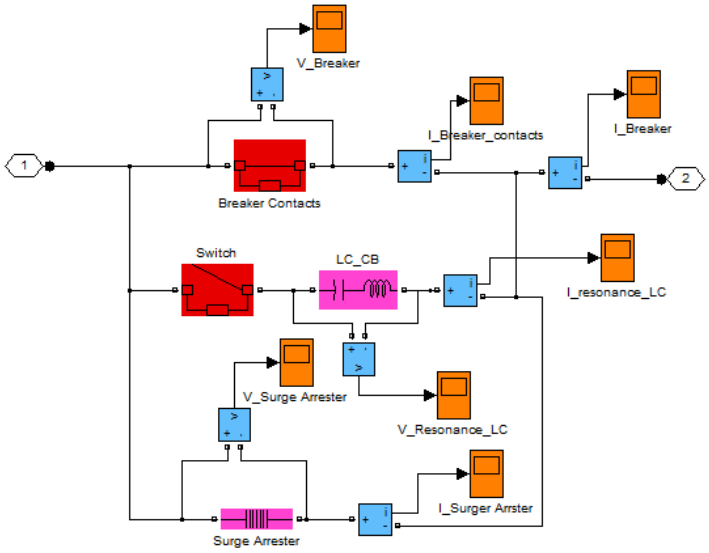


Figure 3.18:MatLab model of the active oscillation mechanical HVDC circuit breaker

The MatLab model of the active oscillation circuit breaker is presented in Figure 3.18. Dimensioning of the components are explained as following.

Breaker contacts. Practically this can be a standard SF_6 AC breaker or number of serious connected vacuum interrupters. In the model this is presented as a standard single phase breaker which can interrupt current only at zero crossing.

Resonant circuit. The resonant circuit consists of the pre-charged capacitor and an inductor. An inductor is very small and is usually a stray inductance. When stray inductance is insufficient to create a necessary oscillation a small inductor can be used in this branch. The most important component of the resonant branch is the capacitor. The size of this capacitor is determined by the speed of commutation required. Reducing the size of this capacitor will reduce the commutation time. However, as commutation speed is increased the probability that the AC breaker will interrupt current at zero crossing is reduced. Moreover, in ideal situation, the size of this capacitor determines the rate of rise of transient recovery voltage. Thus, the choice of this capacitor is based on optimization process which includes current commutation speed, probability of current interruption at zero crossing (di/dt) and the level of stress (du/dt) on the system. Discharge current can be defined by:

$$i_c(t) = \frac{U_c}{\sqrt{L/C}} \sin\left(\frac{1}{\sqrt{LC}} t\right) \tag{3.27}$$

The magnitude of the initial charge has to be chosen so that the largest expected fault current can be interrupted. Indeed, keeping this capacitor fully charged in practice is the main challenge of this breaker.

LC circuit switch. The switch is used to start discharge of the capacitor and modelled as ideal switch. In practice fast AC circuit breaker [44] or thyristor based switch [62] can be used.

Surge arrester. This component serves two purposes; limiting transient recovery voltage and dissipating energy stored in the system after current is interrupted. The optimum surge arrester protection level is 1.5 times the operation voltage. The standard MatLab surge arrester I/V characteristic is modified and the design used in breaker model is shown in Appendix B.

3.8 Multifeeder circuit breaker

In a meshed HVDC system a converter would have more than one feeder of the same polarity connected to other terminals of the DC grid. Installation of hybrid circuit breakers at each feeder of the system would lead to protection system costs increase due to high number of power electronic components required. High cost reduces advantage of the DC system over AC, where cost of the breakers is much lower. Although several concepts for hybrid circuit breaker have been investigated [30], it has not been proposed to utilise hybrid circuit breaker solution for multifeeder protection.

Probability of simultaneous faults on several feeders at the same time is close to zero. This gives an opportunity to utilize the same current blocking branch, where majority of costly power electronic components is concentrated, in more than one feeder. The current blocking branch in this case should be isolated from the nominal current branch by auxiliary switches that would connect it under the fault condition to the affected feeder as illustrated in Figure 3.19. In case of same polarity feeders protection nominal current path can be separated by one auxiliary switch and in case of two polarities feeders protection by pair of switches as current breaking and energy absorption branches should be isolated from another feeder during fault current clearing.

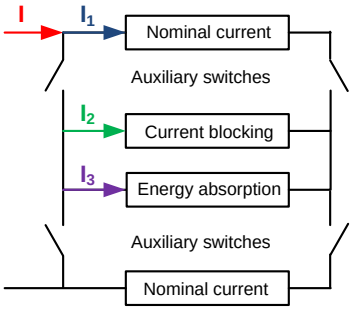


Figure 3.19: Multifeeder hybrid circuit breaker concept

The process of circuit breaker action and control signals for elements are presented in Figure 3.20. When a fault is detected at t_1 the control signal to close is sent to auxiliary switches (AS) and fault current is commutated into the current blocking (CB) branch at t_2. After current commutation process mechanical switch in the nominal current (NC) branch can be open. When the switch in the NC is open the current is forced to zero by CB branch at t_3. Blocking of the fault current leads to transient recovery voltage rise that causes conduction of the surge arrester

in the energy absorption branch. When current through the arrester is reduced to low level at t_4 auxiliary switches are open and the circuit breaker is ready for next interruption at t_5. The opening and closing delay of the switches is marked in grey.

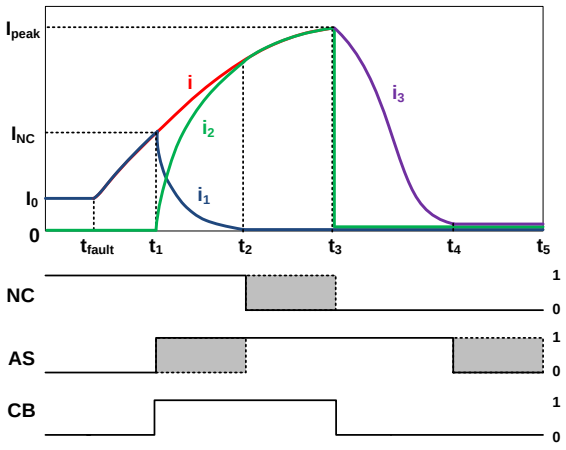


Figure 3.20: Currents in the multifeeder circuit breaker and control signals.

If multiple feeders of the same voltage are connected to a terminal it is possible to use only one CB and EA branches as shown in Figure 3.21. These branches are isolated from the NC branch by pairs of auxiliary switches. The price of power electronic components required for the CB branch of the same current and voltage capabilities as the vacuum based auxiliary switch can be three to five times higher than auxiliary switch price. Proposed arrangement would allow reduction of the protection equipment costs and potentially space requirements. Comparing to a hybrid circuit breaker approach the proposed multifeeder breaker operation is delayed by closing of the auxiliary switches. As discussed further the closing time of 1 ms could be achieved by utilising MV vacuum switches with Thompson actuator. Delay of the current blocking leads to higher fault current and therefore require higher CB branch capabilities that depend on the rate of rise of fault current. Considering that hybrid circuit breakers proposed have fault breaking speed around three millisecond CB branch capabilities for multifeeder circuit breaker should be increased up to by twenty five per cent.

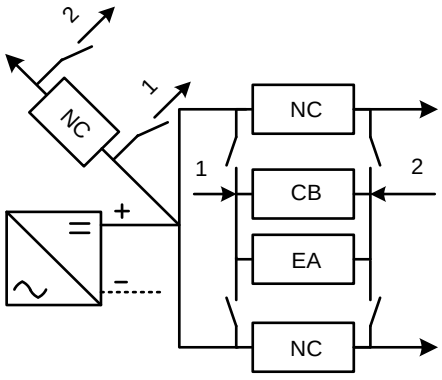


Figure 3.21: Multifeeder protection topology

For secondary protection of the terminal station to clear the fault, when the circuit breaker in one of the feeders fails, additional circuit breaker can be installed as shown in Figure 3.22. In case of a pole to ground fault primary breaker makes an attempt to clear the fault and if it fails secondary protection designed for higher fault current isolates the terminal from the fault. Positive and negative poles are isolated from each other by the auxiliary switches and thus faults in positive and negative parts of the system can be cleared independently. In case of a pole to pole fault primary breakers in positive and negative poles make an attempt to cleat the fault. If one of the breakers fails to clear the fault secondary breaker can isolate the terminal by disconnecting affected pole. Other feeders should be isolated by operation of the breaker at remote terminals.

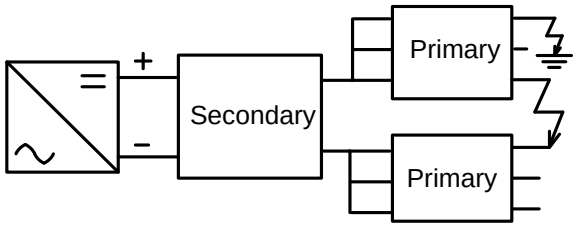


Figure 3.22: Multifeeder primary and secondary protection topology

3.8.1 Auxiliary switch

In order to reduce current commutation time maximum speed of the contacts movement in auxiliary switches should be reached. The best candidate in this case is a vacuum based switch that has very high breakdown voltage at short contacts separation distance, in the range of 20 kV per mm. Typical application of the vacuum switch is interruption of the current thus all the efforts in the design are given to opening of the switch and current interruption capability [63]. Nowadays, vacuum circuit breakers of up to 80 kV are commercially available [64]. In the proposed architecture of the multifeeder circuit breaker vacuum switch should close as fast as possible and conduct the fault current until it is interrupted in the current blocking branch and the current caused by transient recovery voltage is reduced to almost zero in the energy absorption branch. Summarizing, the design of the switch should be focused on the closing speed and current conducting capabilities. In order to reach HV application series arrangement of switches should be applied as proposed in [65]. Diagram of the vacuum switch with actuator circuit based on Thompson coil drive is presented in Figure 3.23. As auxiliary switch does not have burning arc, design of the contacts and vacuum chamber can be optimised to reduce weight of moving contact increasing speed of closing. Thompson coil drive is applied to achieve high speed of the contacts movement [66], as described in [67] maximum contact speed of 15 mm/ms can be

reached. Considering that contacts separation of 10 mm, that corresponds to 80 kV operational voltage, could be reached within less than a millisecond.

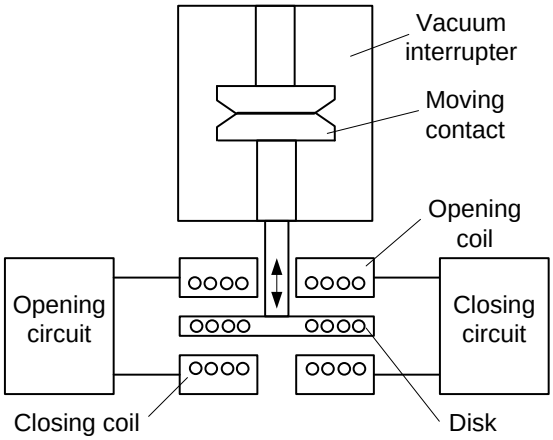


Figure 3.23: Diagram of the auxiliary switch

Thompson coil drive consists of two coils and a disk that is moved by the magnetic force created between the coil and the disk. In the multifeeder circuit breaker actions of closing and opening follow in a short period of time and thus separated circuits are proposed here. At high travelling speed re-bouncing of the contacts can occur. This effect is not considered in modern vacuum interrupters as they are designed for fast contacts opening and speed is reduced by spring mechanism. To eliminate re-bouncing effect speed of the contacts movement should be close to zero at the moment of contacts connection. In order to reach that closing operation should be divided into two time intervals accelerating and decelerating of the contacts. The circuit for actuator mechanism is presented in the Figure 3.24.

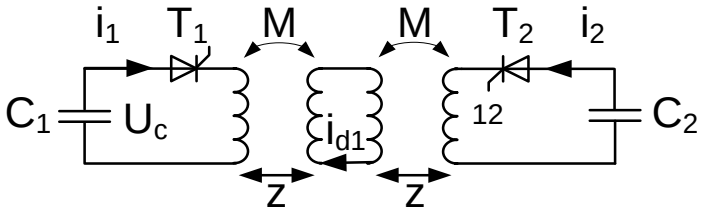


Figure 3.24: Equivalent circuit for Thompson coil actuator

The circuit consists of two separated circuits. The accelerating part consists of capacitor C_1 connected to the closing coil through a thyristor T_1. When thyristor is fired capacitor starts discharging and eddy current I_{d1} is induced in the disk. The force between coil and the disk causes acceleration of the movable contact. When current I_1 reaches zero thyristor T_2in the decelerating branch is fired and discharging current I_2 causes deceleration of the movable contact.

The process of the contact acceleration and deceleration can be described by the equation (3.28) from [68], where m is the mass and a is acceleration of the moving mechanism (contact

and disk), C and U_c are capacitance and voltage of the capacitor, i_d is the eddy current in the disk, M is mutual inductance and z is distance between coil and the disk.

$$ma = C\frac{dU_c}{dt}i_d\frac{dM}{dz} \tag{3.28}$$

Mutual inductance between coil and disk can be defined using (5), where dl is an element of the coil or disk length andμ is permeability of the coil.

$$M_n = \frac{\mu}{4\pi}\oint_{coil} dl_{coil}\oint_{disk} dl_{disk}\int_d^0 \frac{1}{z}dz \tag{3.29}$$

As can be seen due to movement of the disk it is very difficult to obtain parameters of the actuator circuit using an analytical approach [67]. Parameters of the circuit could be defined by using FEM approach [70-72]. Development of the contact speed, current, force and distance between the contacts during opening phase are shown in Figure3.25, where t_r is time until deceleration beginning and t_c is time until complete contacts closing.

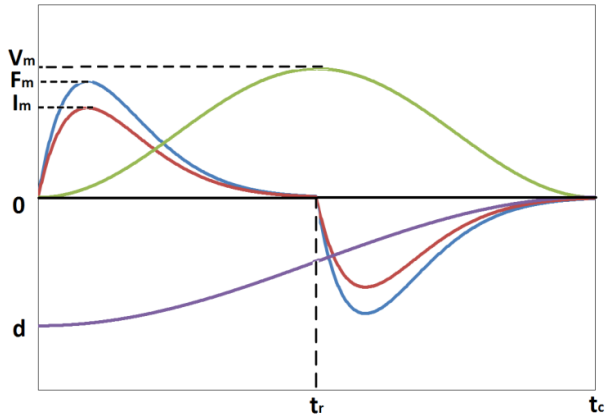


Figure 3.25:Waveforms of the actuator current (red), force (blue), speed (green) and contacts displacement (purple)

3.8.2 Protection system

Reliable protection system for HVDC meshed grids is still under development and no universal approach has been proposed so far. For the multifeeder topology fast detection of the affected feeder is important. When affected feeder is detected auxiliary switches start connecting the current blocking branch. In certain cases when the fault is far away from the circuit breaker it can be difficult to distinguish if the fault is within the protected feeder. In this case higher level protection system based on more advanced algorithms and measurements can accurately identify the affected feeder.

Due to fast fault propagation and information processing and communication delay central fault protection is very challenging. Thus local measurement is a preferable solution in order to

identify the faulted feeder and trigger the circuit breaker in the shortest period of time. Detection of the fault based on the threshold values of voltage or current are not fast enough and do not provide high level of selectivity. Another option could be measurement of the rate of change of voltage. However, it should be taken into account that voltage fluctuations are very sensitive to changes in the system as well as external effects and, therefore, achieving reliable protection based on this approach could be very challenging.

For the proposed multifeeder circuit breaker protection based on the measurement of the rate of rise of current is considered, that has been implemented in railway systems already [73]. Rate of rise of current is defined by inductance in the path between the converter and the fault. Inductance of the path is mainly defined by the inductance of the transmission media (cable or overhead line). If path from the terminal, where the breaker is installed, is shorter than from other terminals the faulted feeder can be distinguished based on the *di/dt* measurement. In Figure3.26 the waveforms of the rate of rise of current are presented in three protected feeders during pole to ground fault. It can be clearly observed that the rate of rise of current in the faulted feeder (green line) is higher than in the others. Thus this method provides a reliable condition for faulted feeder detection.

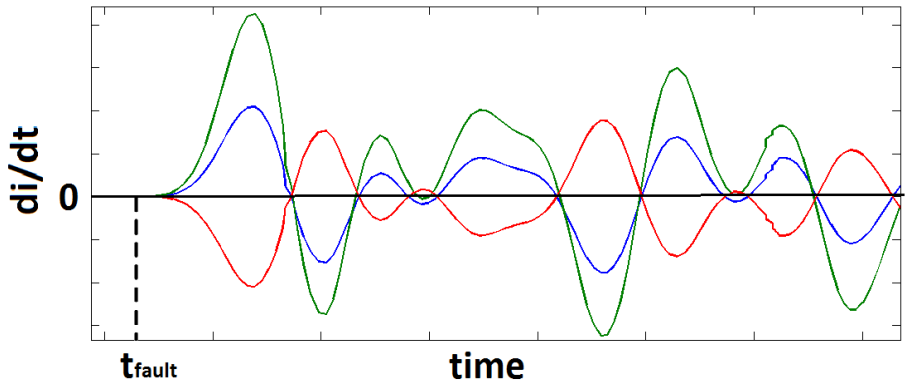


Figure 3.26: Waveforms of rate of rise of current for three feeders

For the proposed topology fast detection of the affected feeder is important. When affected feeder is detected auxiliary switches start connecting the current blocking branch. In certain cases when the fault is far away from the terminal can be difficult to distinguish if the fault is within the protected feeder. In this case higher level protection system based on more advanced algorithms and measurements can accurately identify the affected feeder.

In order to measure the rate of rise of current in the protected feeders DC current transformers (DCCT) are used. To suppress noise caused by the environment between the DCCT and the protection cubicle, an analog filter is installed. The cut-off frequency of this analog filter is chosen to be 10 kHz, which is matching the bandwidth of commercially available DC measurement devices. The filtered analog signal is then converted to a digital signal by using an

analog to digital converter (ADC) with a sampling frequency of 50 kHz that would allow high resolution for fault detection. Digital signal is used to continuously calculate an absolute value of the rate of rise of current. As the protection system should be able to compare the measured signals multiple times to avoid incorrect tripping, a digital moving averaging filter is installed as well. The final average value is used to detect the fault and evaluate the faulted feeder by comparing it with the values from other protected feeders. A schematic representation of the proposed protection system is shown in Figure 3.27.

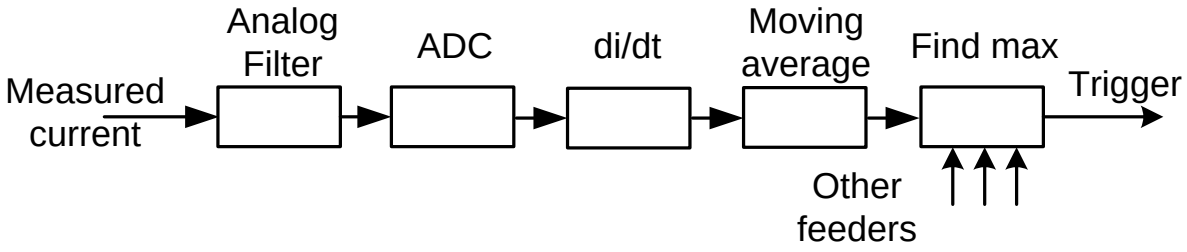


Figure 3.27: Protection system design

Simulations show that, even if it is hard to accurately identify the location of the remote faults, proposed method reliably identifies the feeder with shortest distance to the fault. The circuit breaker can later be used to disconnect the feeder during secondary protection system action.

4. Results

4.1 DC fault conditions

A three terminal radial network adopted from [12] is shown in Figure 4.1. Since the main objective is to understand the transient current contributions of various network components during fault, to which the HVDC circuit breaker is subjected, the radial system layout is replicated here. Moreover, detailed system information is available for this network. The system consists of three converters connected to AC systems and a fault is applied 100 km away from terminal 1 towards terminal 2. Terminal 3 is located 300 km away from terminal 1 and it is connected to terminal 2 via terminal 1.

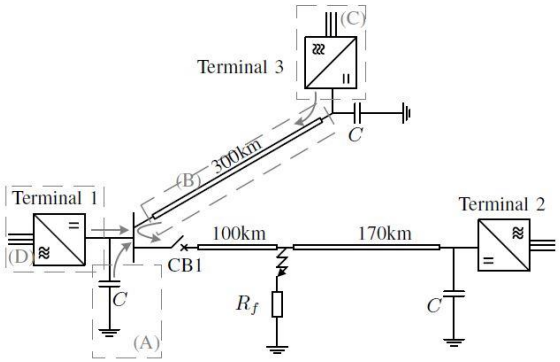


Figure 4.1:Three terminal radial HVDC network

This network consists of VSC converter stations where monopole and bi-pole converter configurations are investigated separately. The system modelled by equivalent converter models as explained in chapter 3.1. The detailed system parameters are shown in Table 4.1.

Table 4.1 - System parameters

Parameter name	Symbol	Value
Rated Converter Power	S_C	800 MW
DC Voltage	U_{DC}	±320
AC Voltage (L-L, RMS)	U_{AC}	400kV
Short circuit power of AC system	S_{AC}	10 GVA
X/R of AC Network	X_{AC}/R_{AC}	10
Transformer power	S_T	1000 MVA
Transformer leakage Reactance	u_k	0.1 pu
Transformer power losses	ΔP_k	650 kW
Number of modules per arm	N_{arm}	400
Capacitance per module	C_{module}	10mF
Resistance of diode	R_{diode}	0.5 mΩ
Converter Phase Reactor	L_{pu}	0.05 pu

In case of a DC fault, the IGBTs in the converter are blocked within a first half a millisecond after the fault is detected in order to protect them from overcurrent. Then uncontrolled short circuit current continues to flow through freewheeling diodes connected in parallel to the IGBTs. In order to simplify the model and speed up design and simulation, most of the control systems of the converters are neglected in the simulations. Converter is presented as a three arm diode converter with parallel connected capacitor banks.A cable and overhead linesarerepresented by adistributed parameters model inMatLab.

4.1.1 Effect of VSC type

For investigating the impacts of various VSC converter topologies on DC fault current behaviour, terminal capacitance is adjusted accordingly. Since the fault current contributions of various components, except for monopole pole-to-ground fault, have the similar (dominant) characteristics, only a bi-pole pole-to-ground is illustrated here. For a 2-level converter 200 µF capacitor is implemented in order to simulate its influence in a 2-level converter during fault.

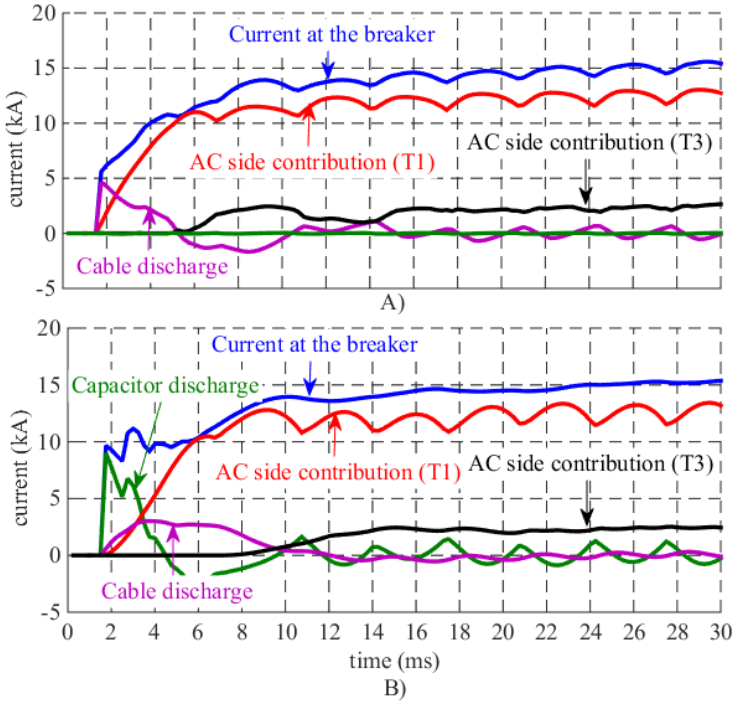


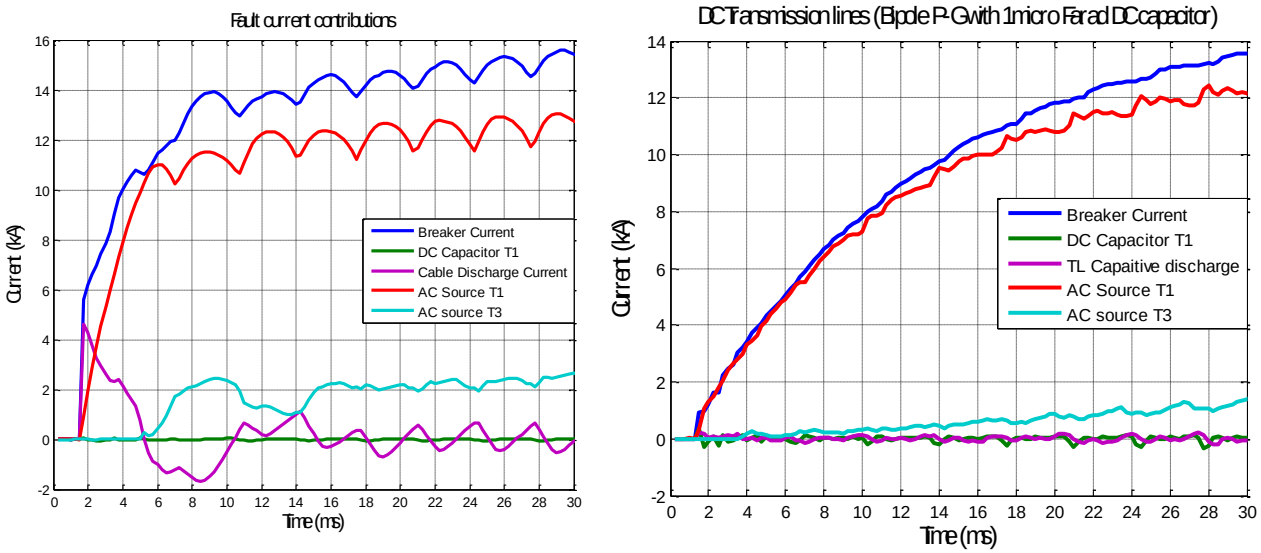
Figure 4.2: Fault current contributions of various components in bipole pole-to-ground fault. A) MMC, B) 2-level converter with 200 µF DC capacitors

In modular multilevel converter (MMC), the blocking of the IGBTs during fault limits the discharge of module capacitors. Simulation results of these two technologies are put side by side in order to observe the impact of the converter capacitance as shown in Figure 4.2. Moreover, detailed contribution of fault current from various components is presented. From this figure, it can be seen that immediate discharge of converter capacitance and cable is followed by

contribution of AC sides at terminal 1 (T1) and several milliseconds later at terminal 3 (T3) due to traveling wave delay.

4.1.2 Effect of the transmission media

In order to clearly observe the impact of capacitive nature of cables, a simulation is performed by replacing all cables in the system with overhead transmission lines (OHL) for a bipolar system described above and pole-to-ground fault is applied.



(A) (B)

Figure4.3: Fault current contributions of various components in bipole system during pole-to-ground fault in(A) cable,(B) overhead line system

Compared to cable interconnected system, absence of abrupt spikes in fault current during the first few milliseconds after fault can be seen in Figure 4.3(B). In addition, the fault current in the system interconnected with OHL grows steadily compared to the system interconnected with cables. Relatively steady growth in fault current is partly due to inductive nature of OHLs. Nevertheless, both systems (cable and OHL) have nearly the same steady state value of the fault current, except in this case the system with OHL has slightly lower value. This is due to higher resistance of the OHL resulting from smaller conductor cross-section used in the model.

4.1.3 Effect of the system configuration

In order to investigate the fault current behaviour and identify the most severe conditions for circuit breaker operation, several studies have been performed using monopole and bipole configurations.

Symmetrical monopole system

A single, low impedance line to earth fault will cause the DC voltage of the faulted line to collapse. The propagation of this throughout the network is, again, related to the characteristics of the line. The effect on the converters will depend on the system earthing. In MMC VSC symmetrical monopole systems where the converter voltage floats on the DC side, with no earthing on the converter side of the transformer the voltage on each line should be balanced prior to the fault. The current from AC side is only drawn through the converter while the DC voltage is lower than the rectified AC voltage. Soon the non-affected DC feeder is quickly charged and the total DC voltage recovered. Therefore, the current surge is transient and will end when the voltage on the positive and negative poles have stabilised. Thus current stress on the converter and cables is temporary in pole to earth faults.

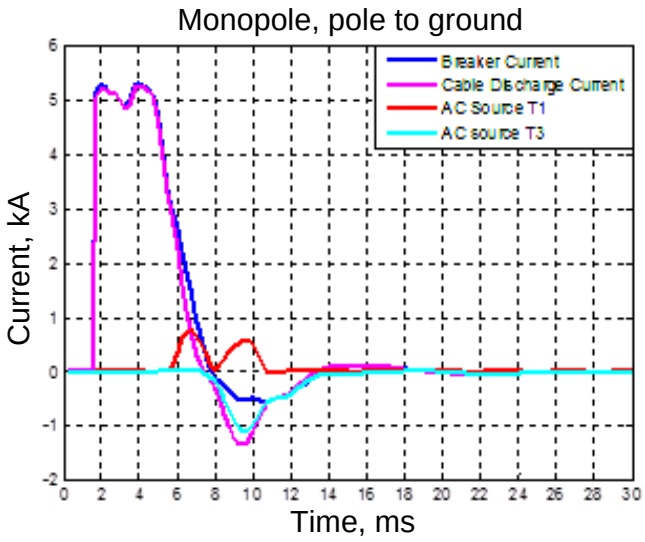


Figure 4.4: Current during pole to ground fault in the monopolar VSC HVDC system

Figure 4.4 shows an example of simulation results for a pole to ground fault placed on the positive DC pole of a symmetric monopole system. The fault current is mainly dominated by discharge of the system capacitance. The affected pole voltage collapses to almost zero, only a voltage drop caused by line resistance remains. The unaffected pole, on the other side, suffers increase of voltage to the double of nominal value.

Fault current contributions of various network components in symmetric monopole configuration during pole-to-pole fault are shown in Figure 4.5. The fault current through CB is nominated from the discharge of the cable during first 5 ms similar to pole to ground situation. However, in pole-to-pole fault, the fault current is much larger and continues to grow to a steady state value of over 25 kA. It is sufficiently high to damage power system component, if not cleared in time.

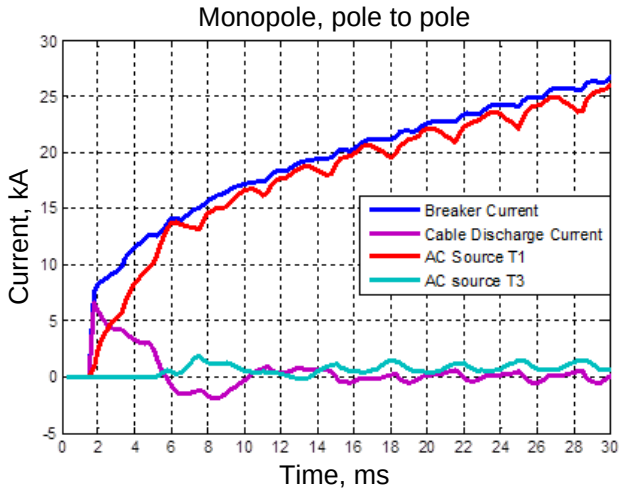
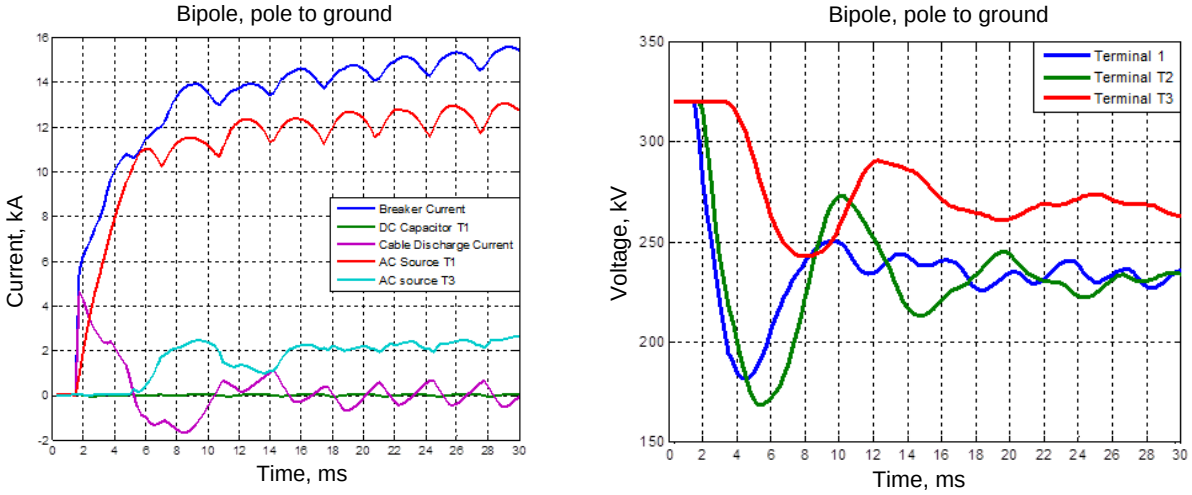


Figure 4.5: Current during pole to pole fault in the monopolar VSC HVDC system

Bipole system

In order to compare monopole and bipole configuration during DC fault, the above situation is investigated for bipole converter stations. Figure 4.6 (A) presents the fault current through the CB when a pole-to-ground fault is applied to bipole system. From this figure we can observe quite similar behaviour as pole-to-pole fault in a monopole system.

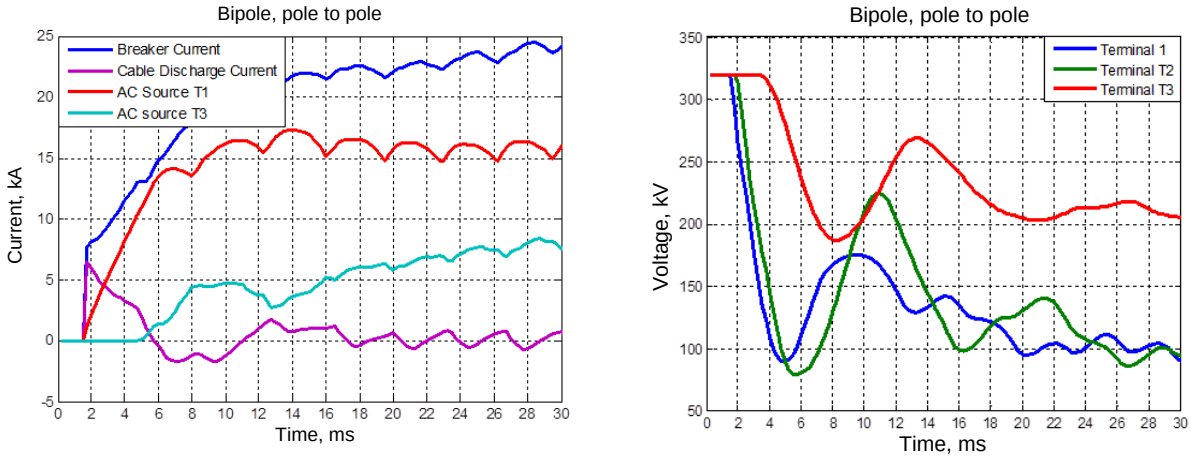


(A) (B)

Figure 4.6: Fault current (A)and terminals voltage (B) during poletoground fault in bipole converter configuration

The negative and positive pole voltages at each terminal during a poletoground fault in bipole system are depicted in Figure 4.6 (B). The voltage dip at each terminal is proportional to the distance of the terminal from fault location. Hence, the voltage at terminals 1 and 2 falls to a lower value compared to the voltage at terminal 3 due to the relative proximity of these terminals to the fault location. The most important point to note here is that these voltages do not drop to zero due to the impedance of the cable and the fault resistance.

A more severe condition is observed when a pole-to-pole fault occurs in multiterminal DC networks with bipole converter configuration. Simulation results during such a situation are shown in Figure 4.7.Figure



(A) (B)

Figure 4.7:Fault current (A) and terminals voltage (B) during pole-to-pole fault in bipole converter configuration

Figure 4.7 (A) displays fault current contributions from different sources during a pole-to-pole fault in a bipole system. As would be expected the fault current in this case is quite large and grows to a steady state value of more than $25\ kA$. The fault behavior in this case is quite similar to the fault behavior in monopole, pole-to-pole fault except the contribution from AC source at terminal 3 in this case is higher. It has been observed that the pole to pole fault affects the two poles equally. The voltage dips (in magnitude) for both poles are significant.

Comparison

If identical fault conditions are applied for a radial grid utilising different topology fault current development can be compared. Figure 4.8 shows the fault current during the transient phase for four cases. Except for the monopolar pole to earth fault case, fault current is similar because of dominant capacitance discharge current. At latter stages pole to pole faults are more severe for both bipolar and monopolar topologies, mainly due to lower resistance in the current path. Pole to pole faults cause a collapse in DC voltage and, depending on converter technology, can lead to an increase in current flowing through the converter. Pole to pole fault in symmetrical monopole HVDC systems is similar to pole to pole faults in a bipolar system. Pole to earth faults in a monopolar system does not lead to such severe current stress and more voltage stress is placed on the converter and system, relating to insulation coordination.

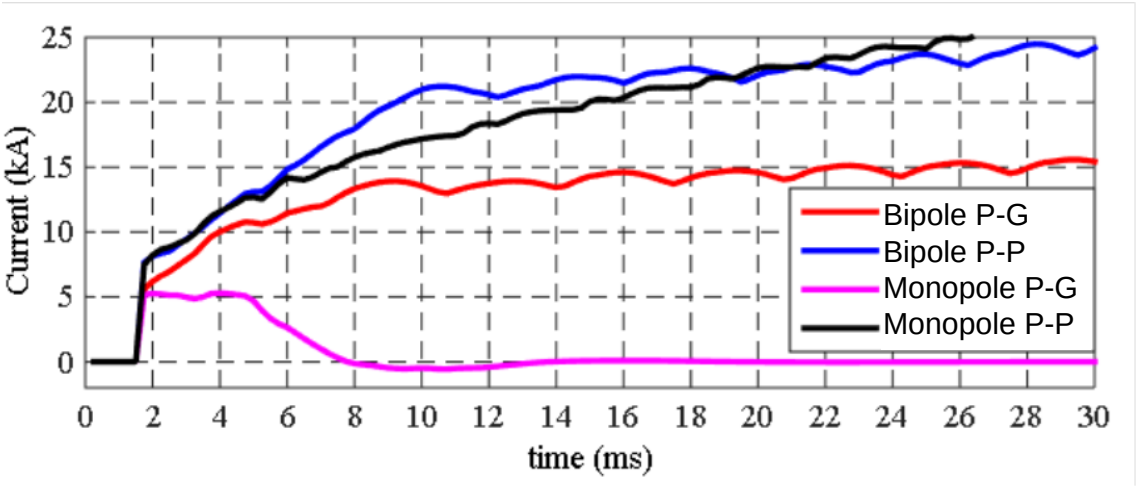


Figure 4.8: Comparison of the fault current behaviour in different system configurations

4.2 Circuit breaker performance in a radial grid

In Chapter4.1 fault current contributions of various components as well as the total current that is measured at breaker location (without circuit breakers tripping) is briefly discussed. In this chapter HVDC circuit breaker models are integrated at breaker location as shown in Figure 4.1. The main purpose in this case is to investigate the transient stresses (current and voltage) that appear across the breaker as a whole and its internal components, as well as in the system, while clearing a fault using different HVDC circuit breaker technologies. In all cases, modular multilevel converter with bipole configuration during the fault condition is assumed. In order to study the worst case scenario, a fault location is brought to the vicinity of terminal T1 (1km away towards T2). Also a fault resistance is changed to 0.1 Ω in order to further worsen the situation. However, in order to restrict the rate of rise of fault current, DC smoothing reactors of 30 mH are put at the ends of each cable. With these system parameters, simulation results show that a pole-to-ground fault, with 0.1 Ω fault resistance, have sufficiently similar characteristics with a pole-to-pole fault in the same system. Moreover, since the rate of rise of current (di/dt) is slightly higher in the pole-to-ground fault (with system parameters just mentioned), this system is chosen as a worst case for simulation with breakers embedded in the system. For all the cases the triggering signal sent to the circuit breaker 1ms after the fault wave reaches the circuit breaker. This time is allocated to detection and processing of the fault by protection system.

4.2.1 Hybrid Power Electronic Type I (HPE I)

In this section simulation results during fault clearing by HPE I are explained. An electrical diagram of HPE I HVDC circuit breaker is shown in Figure 4.9. Operational principle and model of the circuit breaker is explained in Chapter 3.3. Load commutation switch (LCS) is

blocked1ms after the fault wave reaches the circuit breaker. At the same time the IGBTs in the main breaker are turned on in order to commutate current to this path. In reality, the IGBTs in the main breaker are switched on sequentially in such a way that the large in rush current that could, otherwise, overstress the IGBTs is avoided.

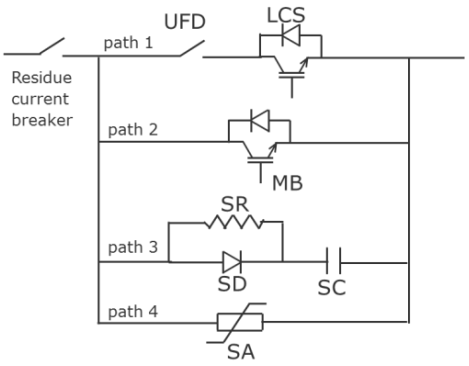


Figure 4.9: Electrical diagram of theHPE I HVDC circuit breaker

Although current commutation time from LCS to main breaker is determined by the stray inductance that exist between these branches, in the ideal situation it takes about 10μs to complete the commutation. By this time the ultrafast disconnector (UFD) opens its contacts. The main breaker continues to conduct full fault current until the UFD reaches sufficient separation to withstand the TRV. This time is assumed to 2ms in the simulation study after which the main breaker is turned off. The switching off the main breaker is followed by rise of TRV with rate of rise determined by the snubber circuit of the main breaker.

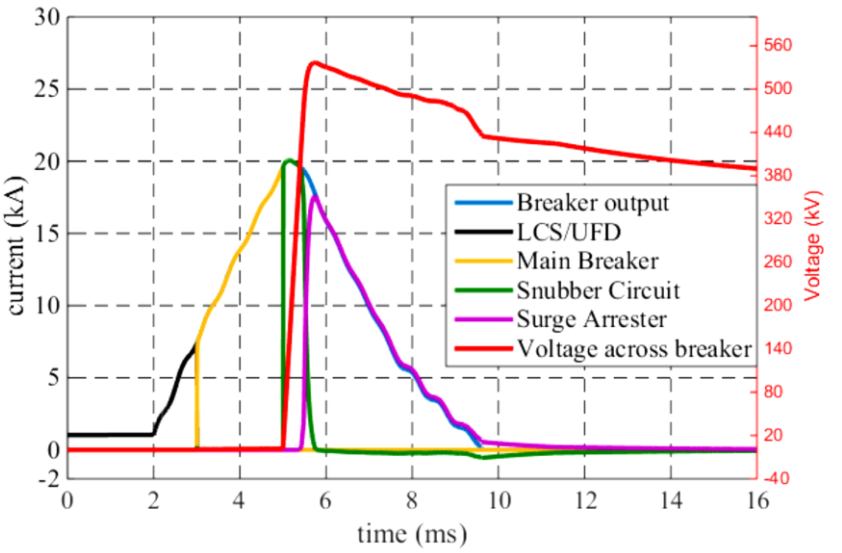


Figure 4.10:Current through commutation branches and voltage the HPE I

Figure 4.10 shows current commutation through various branches of the HPE1. Rate of rise of current is defined by the inductance in the current flow path and in this case resulted in 6.21 kA/ms and it lead to the peak current of 20 kA. The time till peak or time until the current is

blocked by main breaker is 3.32 ms with a total fault clearing time 6.61 ms when the surge arrester dissipates the inductive energy resulted in 17.4 MJ. From this graph it can be observed that the snubber circuit conducts fault current for about 700μs, while during this time the TRV rises to full protection level of surge arrester. Hence, simulation studies show that the rate of rise of TRV is determined by the value of the snubber capacitor along with the snubber resistance in parallel with the diode. It is determined from this plot that the rate of rise of TRV is about 975,5 kV/ms. Besides, it can be seen from this graph that the TRV grows to a slightly higher value (about 536kV) than the protection level of surge arrester. This is indeed determined by the number of parallel surge arresters chosen in the model. Simulation study indicates that the larger number of parallel surge arresters reduce the peak value of TRV; however, this is achieved at the cost of longer energy dissipation time and hence longer fault clearing.

As can be observed in Figure 4.11 during fault clearing, current through the breaker rises to the peak value of 20 kA in about 3.1 ms after occurrence T1 is significantly overstressed since it reaches 16 kA, compared to T3 which is subjected to a much lower stress. It can be observed that the terminal voltages dip is significant and converters cannot maintain voltage control anymore. Voltage at T1 falls to a value of about 100 kV, whereas the voltage at T3 dips to zero when the cable is discharged. When fault is cleared, the terminal voltages recover immediately to a slightly higher value than nominal despite small transient oscillation remaining in the system. This is due to absence of the converter control thatleaves voltage to a higher value (about 460kV) after the fault current is cleared.

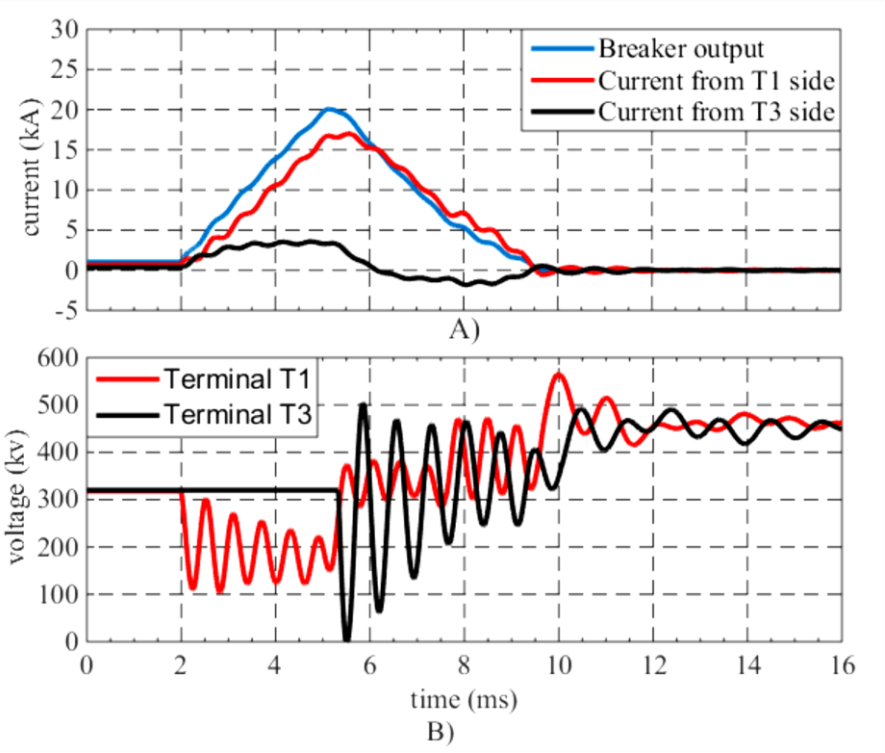


Figure 4.11: Current and voltage in the system during fault clearing by HPE I

4.2.2 Hybrid Power Electronic Type II (HPE II)

In this chapter simulation results during fault clearing by HPE II are explained. An electrical diagram of the HPE II HVDC circuit breaker is shown in Figure 4.12. Operational principle and model of the circuit breaker is explained in Chapter 3.4. A point worth mentioning here is that the fault current is commutated from low impedance branch to the first path in auxiliary branch within 10μs after which the UFD starts opening its contacts. In reality the commutation time depends on stray inductance between these paths as well as the parasitic resistance associated with the capacitor in the auxiliary path. The opening of the UFD at this moment is critical because it avoids the fault current from retracting back to the low impedance branch (through the surge arrester in this branch). This happens because the protection level of the surge arrester in the first path of the auxiliary branch is lower than the protection level of the surge arrester in the low impedance branch.

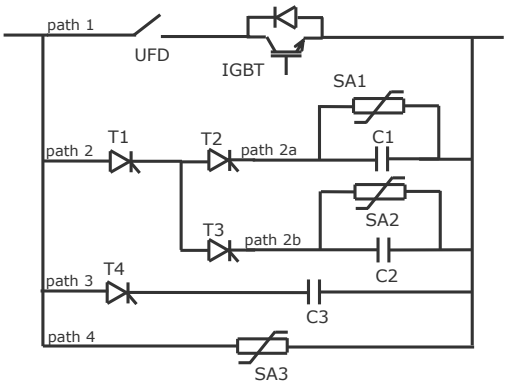


Figure 4.12: Electrical diagram of the HPEII HVDC circuit breaker

In Figure 4.13 the current commutation process through different branches of HPE II as well as the voltage across this breaker is illustrated. Rate of rise of current is mainly defined by the inductance in the current flow path and in this case resulted in 6.15 kA/ms and it lead to the peak current of 16.2 kA. The time till peak or time until the current is blocked by main breaker is 2.81 ms with a total fault clearing time 6.08 ms when the surge arrester dissipates the inductive energy resulted in 11.6 MJ. It is obtained that the rate of rise of the TRV is 606.3kv/ms.

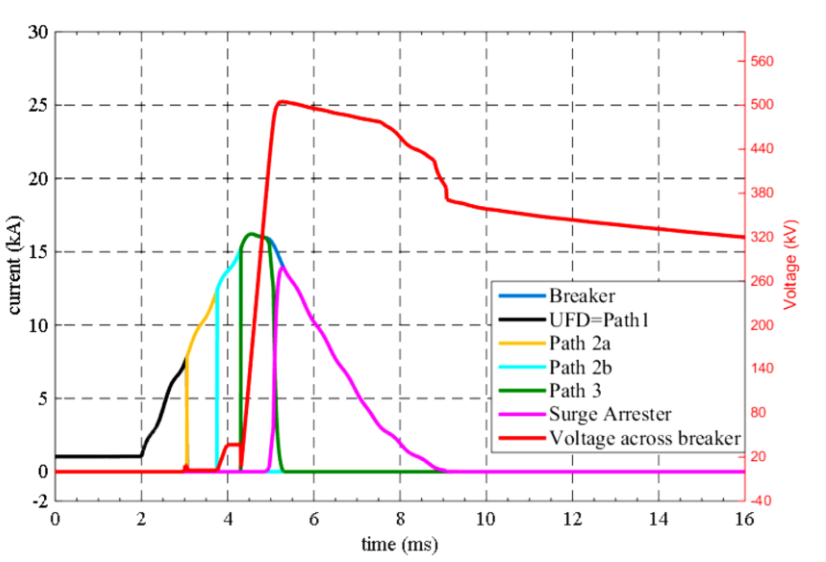


Figure 4.13:Current through commutation branches and voltage across the HPE II

Although not shown on this graph (for the purpose of clarity), current through each path of the auxiliary branch flow first through the capacitor and then through the surge arresters parallel to the corresponding capacitor. This can be seen from the voltage plot. A small pulse at about 3 ms that can be seen on the voltage curve graph in Figure 4.13 caused by current flow through surge arrester in parallel to the IGBTs in low impedance branch. This pulse only exists until current is fully commutated to the first path of the auxiliary branch (about 60μs). After this, current commutates to the first path of the auxiliary branch; thus charging the capacitor in this path. In order to give relatively longer time for the UFD, this capacitor can be chosen to be high so that the charging time (time constant) is longer. However, it should be noted that the surge arrester in parallel to this capacitor is set to lower protection level (about 8kV in this case); thus current through this path mostly flow through this surge arrester as the capacitor is quickly charged. This is the reason why the voltage is flat for about 0.65ms after the first pulse. After this time, a thyristor in the second path of the auxiliary branch is turned on. The same procedure happens as in the first path. However, the protection level of the surge arrester is higher in this path (about 37kV). This is indicated by the rising voltage after the first pulse (capacitor conducts during rise time). The plateau after the small rise in voltage is the time when the surge arrester parallel to the capacitor is conducting. The process in this path takes about 0.7ms.

After this time the thyristor in the final path of the auxiliary branch latches on. As a result, current commutates to this path in a similar way as for the other paths. This is indicated by the dip in the voltage just before it rises to the protection level of the main surge arrester. Voltage starts rising as the capacitor is charged. Therefore, this capacitor and its associated parasitic components determine the rate of rise of the voltage across the main surge arrester and hence, across the whole breaker system.

Figure 4.14 presents simulation results obtained by integrating this breaker into the HVDC system. The first observation is that the peak value of the fault current is 16.2 kA which is lower than in case of HPE I due to faster switching sequence. Energy dissipation time is lower as well due to the presence of relatively larger capacitors in the auxiliary paths that absorbs energy flowing through the circuit breaker. The other observation is that the converter terminal voltages recover faster with smaller oscillations.

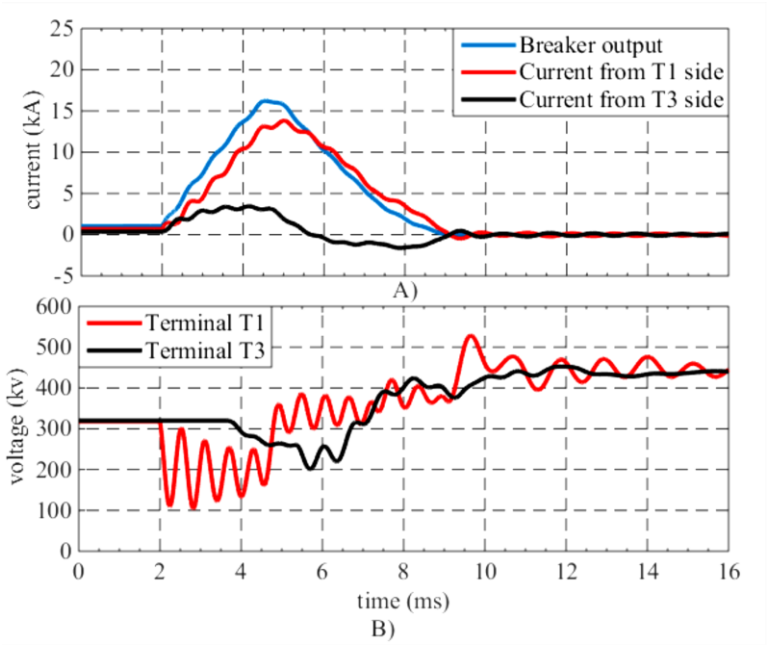


Figure 4.14: Current and voltage in the system during fault clearing by HPE II

4.2.3 Hybrid Power Electronic Type III (HPE III)

In this chapter simulation results during fault clearing by HPE III are explained. An electrical diagram of the HPE III HVDC circuit breaker is shown in Figure 4.15. Operational principle and model of the circuit breaker is explained in Chapter 3.5. The vacuum breaker opens its contacts triggering signal is given as a result of which an arc is formed. At the same time the IGBTs in the main breaker are turned on. As a result of a voltage drop across the arc, current is commutated to the main breaker. This is an important design issue in this breaker as the voltage across the vacuum breaker arc has to be larger than the voltage drop across the total resistance of the IGBTs in the main breaker.

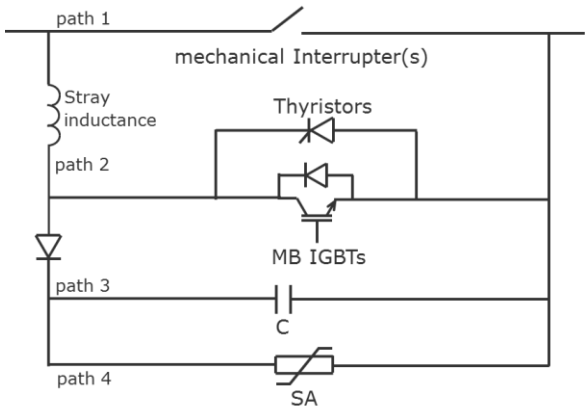


Figure 4.15: Electrical diagram of the HPE III HVDC circuit breaker

Several medium voltage vacuum interrupters are arranged in series in order to obtain the necessary voltage drop for commutation. Although the accurate design is dependent not only on the exact current to be commutated, but also on the value of the stray inductance that exists between this path, number of vacuum interrupters required for commutation considering the worst case scenario can be computed using the following expression:

$$n \geq \frac{R_{MB} \cdot I_{breaker}}{V_{arc}} \tag{4.1}$$

Where, R_{MB} is the equivalent resistance of the IGBTs in the main breaker, V_{arc} is the voltage across the arc of a single vacuum breaker and $I_{breaker}$ is the maximum fault current across the breaker. Using the expression for R_{MB} from chapter 3.5 and the above expression can be reduced to a more simplified expression as shown below

$$n \geq \frac{V_{on,IGBT}}{V_{max,IGBT}} \cdot \frac{V_{breaker}}{V_{arc}} \tag{4.2}$$

For system voltage of 320kV this results in at least 6 vacuum interrupters of 80 kV with arc voltage of 40 V.

The arc is extinguished within 200μs during the commutation process. The main breaker continues to conduct fault current until the contacts of the vacuum breaker attain sufficient separation to with stand TRV. Hence, the IGBTs in the main breaker are turned off 2ms after circuit breaker triggering. As soon as the IGBTs in the main breaker block, the TRV starts to rise quickly to the protection level of the surge arrester. This can be observed from the voltage plot of Figure 4.16. The rate of rise of the voltage across the breaker (TRV) is determined by the size of the snubber capacitance of the IGBTs in the main breaker. Hence, using only ideal capacitor in the snubber circuit, the rate of rise of TRV is about $880kv/ms$.

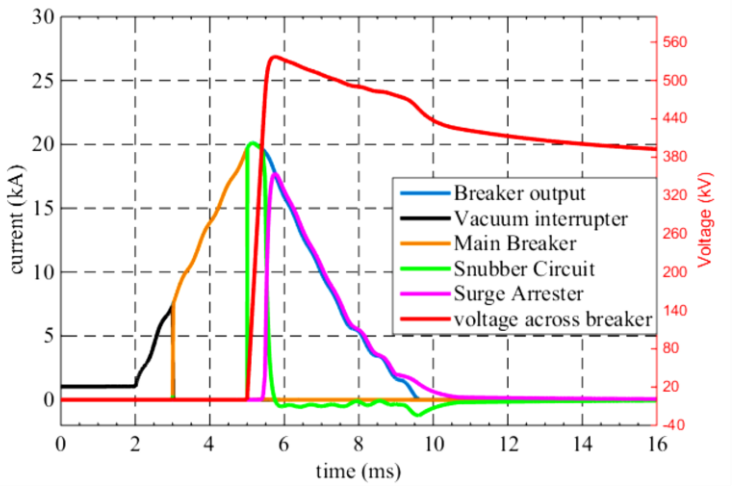


Figure 4.16:Current through commutation branches and voltage across the HPE III

The Figure 4.16 shows current through various branches of HPE III. Rate of rise of current is mainly defined by the inductance in the current flow path and in this case resulted in 6.21 kA/ms and it leads to the peak current of 20.1 kA. The time till peak or time until the current is blocked by the main breaker is 2.32 ms with a total fault clearing time 6.62 ms when the surge arrester dissipates the inductive energy resulted in 17.9 MJ. From this figure it can be observed the snubber circuit of this breaker conducts current for about 0.75ms, after which the surge arrester takes over to dissipate magnetic energy stored in the system and consequently clearing the fault.

From the plots of fault current in Figure 4.17can be observed that the fault current rises to a peak value of 20.1kA. In this situation the performance of this breaker is similar to HPE I in many respects. This can be easily observed by comparing Figure 4.17 and Figure 4.11.

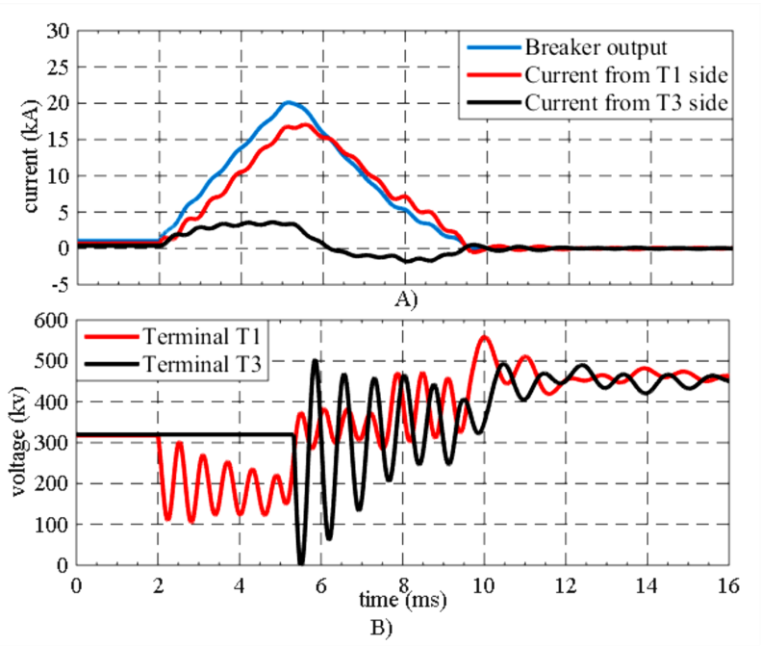


Figure 4.17: Current and voltage in the system during fault clearing by HPE III

4.2.4 Hybrid Power Electronic Type IV (HPE IV)

In this chapter simulation results during fault clearing by HPE IV are explained. An electrical diagram of the HPE IV HVDC circuit breaker is shown in Figure 4.15. Operational principle and model of the circuit breaker is explained in Chapter 3.6.

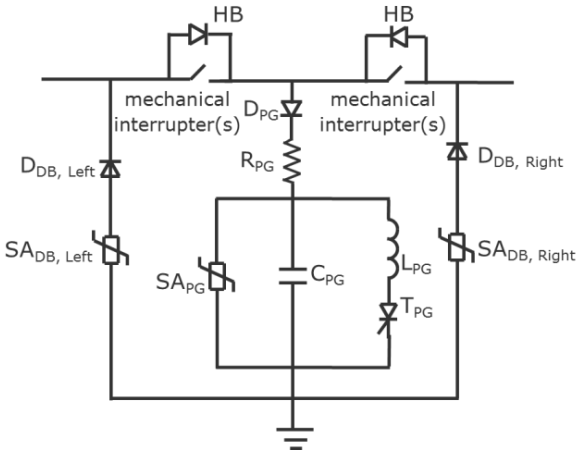


Figure 4.18:Electrical diagram of the HPE IV HVDC circuit breaker

Figure 4.19illustrates current through various branches as well as voltage build up by this breaker during fault current interruption process. The pulses that can be observed right after fault inception is a result of current flowing through the surge arrester in the damping branches of the breaker. The surge arresters in the damping branches are required to protect the breaker against negative overvoltage during fault clearing. As a result of travelling waves between the DC smoothing reactors and the fault location, the transient voltage oscillates between negative and positive values. This can be observed from the voltage plot on the same figure; hence, conducting current in the damping branches during the negative cycles of the oscillation.

From Figure 4.19 we can also see that the pulse generator injects a pulse current as high as 30 kA, depending on the values of L and C in the pulse generator branch. For this simulation, 10 μH and 10 μF are chosen for L_{PG} and C_{PG}, respectively. Further simulation studies show that the amplitude and duration of the pulse current is determined by the inductor and capacitor in the pulse generator branch. The capacitor also determines rate of rise of the TRV that is calculated to be 1636 kV/ms which is higher than in other circuit breakers investigated here.

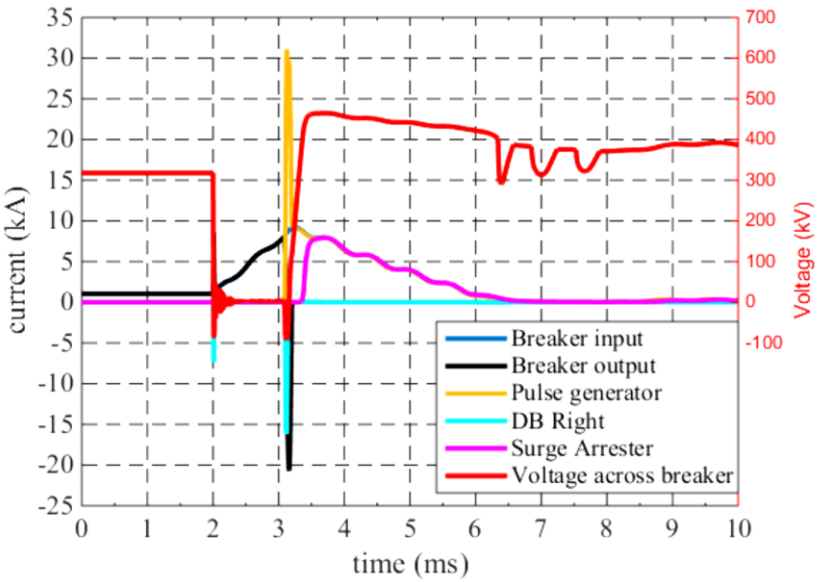


Figure 4.19: Current through commutation branches and voltage across the HPE IV

The Figure 4.19 shows current through various branches of HPE IV. Rate of rise of current is mainly defined by the inductance in the current flow path and in this case resulted in 6.75 kA/ms and it lead to the peak current of 9.2 kA. The time till peak or time until the current is interrupted in the mechanical interrupter is 1.31 ms with a total fault clearing time 3.34 ms when the surge arrester dissipates the inductive energy resulted in 9.5 MJ. Charging of the pulse generator capacitor partly reduce requirements for serge arrester as part of the energy is consumed during charging.

Simulation results by integrating HPE IV circuit breaker into the three terminal radial HVDC network is shown in Figure 4.20, we can easily see that the peak fault current through this breaker is limited to a value of 9.2 kA. In this breaker scheme the mechanical interrupters are assumed to reach sufficient separation to withstand TIV in less than 1 ms, which could be possible by employing several vacuum interrupters in series. As a result, the converter terminal voltages recover faster in about 2 ms during the interruption process. From the simulations performed it can be considered that this topology of the circuit breaker is more effective than other topologies. However, it should be taken in account that there is no prototype of this solution that has been tested. The operation principle and parameters are estimated from the publications and could be updated as test results are provided.

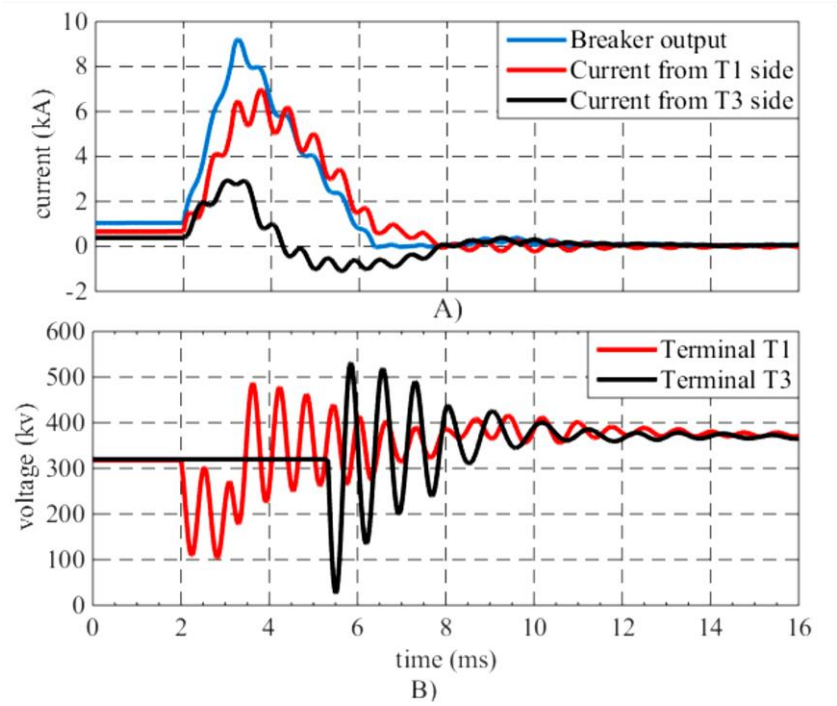


Figure 4.20: Current and voltage in the system during fault clearing by the HPE IV

4.2.5 Active Oscillation HVDC Circuit Breaker

An electrical diagram of a generic active oscillation type HVDC circuit breaker is shown in Figure 4.21. Operational principle and model of the circuit breaker is explained in chapter 3.7. The selected value of the capacitor and inductor are 30μF and 0.5mH respectively. The counter current, from the pre-charged capacitor, is injected 2 ms after triggering assuming the fact that, by this time, the mechanical breaker contacts will reach sufficient separation to withstand TIV. Another assumption is that the arc is extinguished during the first zero crossing.

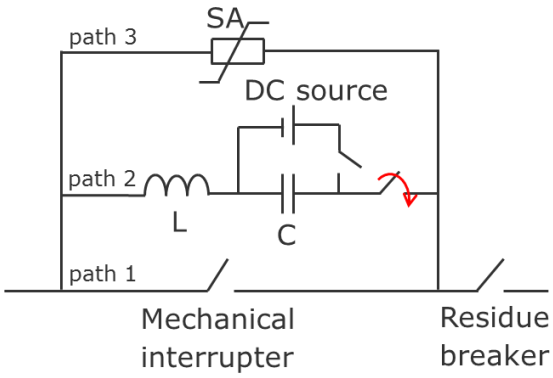


Figure 4.21: Electrical diagram of the active oscillation type mechanical HVDC circuit breaker

Figure 4.22 illustrates the process of current commutation between various branches of active oscillation breaker as well as the voltage across the circuit breaker. The arc between mechanical contacts is immediately cleared (within about 20μs) after current injection from LC

branch. By this time the capacitor is fully discharged and a current commutates to the LC branch recharging the capacitor in the meantime. The capacitor is recharged to a value determined by the surge arrester protection level. The negative voltage seen on the voltage plot is due to the charge remaining on the capacitor at exactly current zero across the mechanical interrupter. The rate of rise of voltage across the circuit breaker (TRV), in this ideal model, is determined by the capacitor. However, in reality the rate of discharge and/or recharge can be affected by the parasitic resistance. With the selected value of the capacitor and inductor the simulation results show that the rate of rise of TRV is $701.5 kV/ms$. Rate of rise of current is defined by the inductance in the current flow path and in this case resulted in 6.21 kA/ms and it lead to the peak current of 21.5 kA. The time till peak or time until the current is interrupted in the AC breaker is 3.61 ms with a total fault clearing time 11.43ms when the surge arrester dissipates the inductive energy resulted in 22.9 MJ.

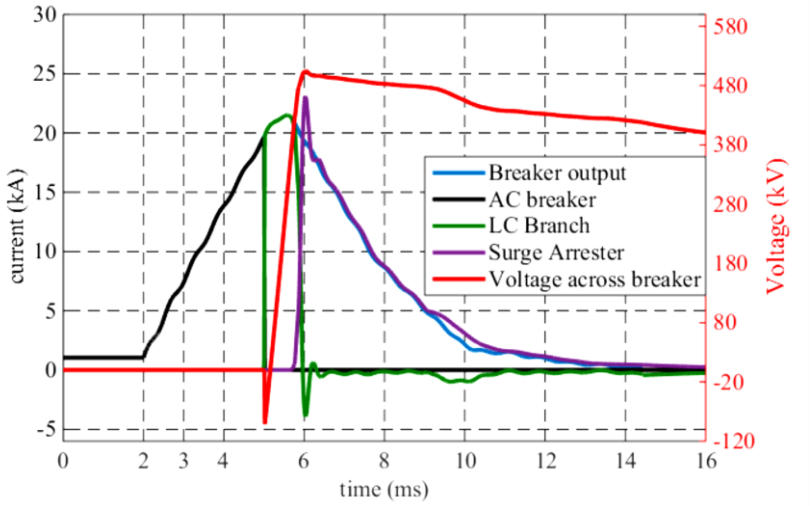


Figure 4.22:Current through commutation branches and voltage across the circuit breaker

Figure 4.23 A) presents the fault current through the breaker and current contributions from terminals T1 and T3. The contribution from T3 is mainly due to discharge of the cable interconnecting T1 and T3, since the contribution from AC side at T3 arrives after several milliseconds delay. Figure 4.23 B) displays the voltage measured at converter terminals (T1 and T3) during the fault clearing by active oscillation mechanical breaker. Although, there is considerable oscillation due to reflections of travelling waves between DC reactors and the fault location during breaking process, we can see that the terminal voltages are restored quickly to a value slightly higher than nominal due to offset caused by the AC voltage source.

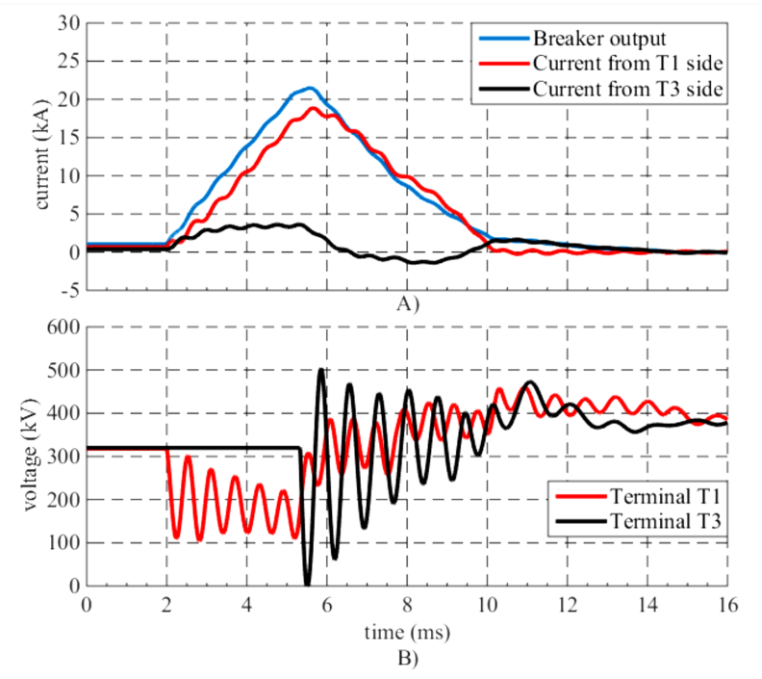


Figure 4.23:Current and voltage in the system during fault clearing by active oscillation circuit breaker

4.2.6 Results of performance

Performance investigation of the HVDC CB and systems behaviour are important to identify requirements for future multiterminal grids. Based on the analysis and simulation results explained in this chapter, current and voltage stresses across the breaker and its internal components are summarized in Table 4.2.

Table 4.2 - Summary of the HVDC circuit breakers performance

Type	Criteria						
	Fault current		TIV		Time to peak current, (ms)	Fault clearing time, (ms)	Energy dissipated (MJ)
	Rate of rise (kA/ms)	Peak value (kA)	Rate of rise (kV/ms)	Peak value (kV)			
HPE I	6.21	20.0	975	536	3.32	6.61	17.4
HPE II	6.15	16.2	606	505	2.81	6.08	11.6
HPE III	6.21	20.1	880	537	2.32	6.62	17.9
HPE IV	6.75	9.2	1636	465	1.31	3.34	9.5
Active res.	6.21	21.5	701	505	3.61	11.43	22.9

The rate of rise of fault current (di/dt) is mainly determined by the system parameters such as nominal voltage and the size system inductance (converter, transmission line and DC reactors). Besides, the distance to the fault location from the converter stations as well as the impedances of commutation paths of the breaker models influence the rate of rise of fault current. Since identical system conditions and fault location is considered for all breakers, the difference in commutation path impedances of each breaker is the main reason for the slight differences seen in di/dt. In addition to system parameters and circuit breakers commutation

path impedance, the time required by mechanical breakers to reach sufficient distance to withstand TIV, has direct impact on the time to peak of the fault current.

The rate of rise and the maximum value of TRV are exclusively dependent on the circuit breaker parameters. Time to peak current, which is the time from fault detection till system recovers its voltage, is dependent on internal switching operations as well as the size of internal components such as snubber capacitors, stray inductances and resistances of the breaker. The total fault clearing time, the time from fault detection till fault current ceases to flow, is therefore, dependent not only on the breaker parameters, but as well on system parameters and configuration. Nevertheless, the main difference in the total fault clearing duration among various breaker schemes is dueto difference in operation and component parameters.

The energy dissipated in the system is dependent, to a considerable extent, on the system parameters such as DC reactors and DC line inductances as well as the maximum fault current. The speed of operation and impedances of DC breakers also have an influence on the energy to be absorbed.

4.3 Multifeeder circuit breaker performance

To demonstrate multifeeder protection system, described in Chapter 3.8, simulations were performed in MatLab/Simulink on a part of 400 kV CIGRE B4 DC Grid Test System [74] presented in Figure 4.24, system parameters can be found in Annex C. All the feeders are overhead lines. The multifeeder circuit breaker is installed at busbar B4 to which three feeders are connected. It can be considered that here proposed solution would have the biggest advantage due to three feeders connected to the busbar.

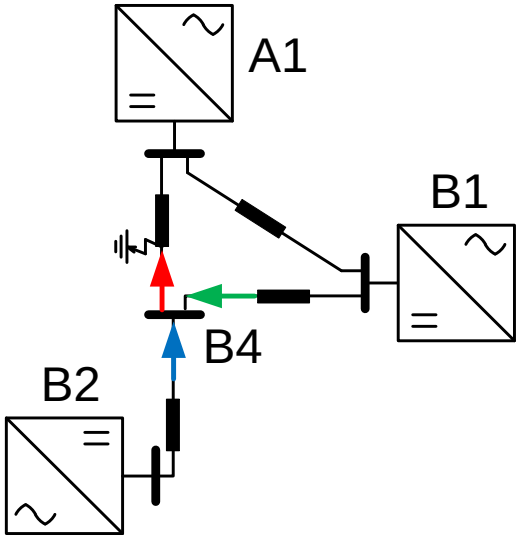


Figure 4.24: Multiterminal HVDC system

4.3.1 Fault current

To define protection system design criteria pole to ground fault distant 10 km from B4 in line A1B4 at time 2 ms was simulated. This location has been defined as the most severe due to shortest distance to terminals B1 and B2. Contribution of the currents from lines B2B4 (blue) and B1B4 (green) to the fault current (red) are presented in Figure4.25. Small oscillations are caused by interaction between PI sections of the line. It can be observed that fault current soon reaches magnitude that is dangerous for power electronic devices in the converters. Clearance of such high value of current by a hybrid circuit breaker is challenging thus fast fault detection and clearing is essential.

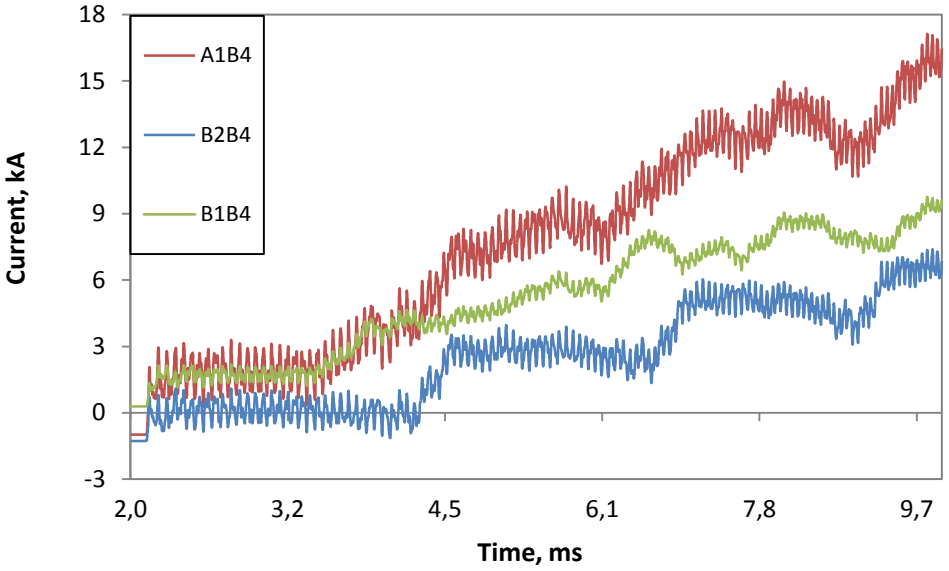


Figure 4.25: Current during pole to ground fault

Considering faulted feeder detection time up to 0,5 ms and period until current blocking of 4÷4,5 ms the circuit breaker should be capable of clearing fault current of 11 kA within 5 ms from the fault inception.

4.3.2 Protection system

Protection system design is described in Chapter 3.8.2. Anticipated time for the fault detection and affected feeder selection is around 300 μs. Limiting factors for faulted feeder detection speed are moving average period, data processing speed and communication between protection cubicle and circuit breaker delays. Data processing speed and communication delay is not discussed here, however, time of 100-200 μs could be considered feasible. In order to define time period length of the moving average block simulations were performed for different

distance to the fault from terminal B4. Accuracy of the method depends on the difference between values measured in the feeder I' and a affected one I'_{af}, it can be defined by:

$$N = \frac{I'}{I'_{af}} \tag{4.3}$$

Results for the average di/dt difference are presented in Figure 4.26 for the moving average period length of 100 μs (in blue) and 200 μs (in red) after the fault inception. Comparison is given based on the difference between average di/dt measured in the affected line A1B4 and healthy lines B1B4 and B2B4. It can be seen that time length of 200 μs has no advantage over 100 μs period. Identical simulations have been performed for faults in other feeders where similar results have been observed. It is a positive conclusion that allows reduction of the faulted feeder detection time to 300 μs.

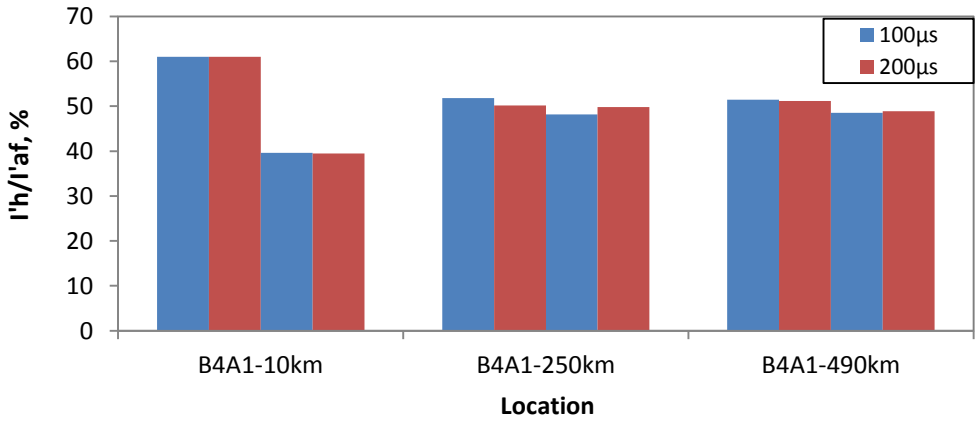


Figure 4.26: Effect of the moving average period on the faulted feeder detection

Simulations have been performed to verify robustness of the method for faults in protected feeder at different distances: close to B4, half distance and remote. Results for the moving average difference after the fault detection between affected and healthy feeders for every case are presented in Figure 4.27. It can be observed that affected feeder can be easily detected based on the comparison of average rate of rise of current.

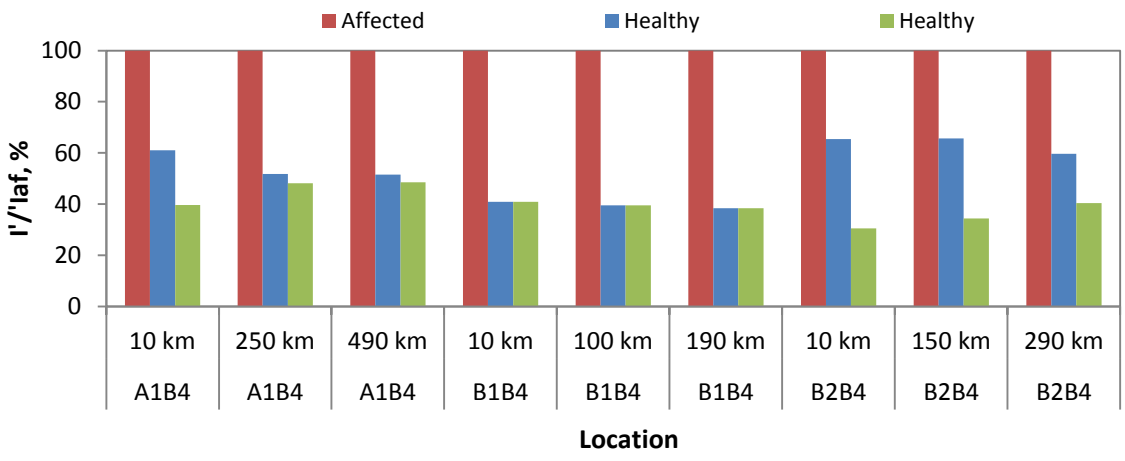


Figure 4.27: Effect of the fault location on the faulted feeder detection

Effect of the fault resistance on detection accuracy has been also investigated. Results for the moving average difference after the fault detection between affected and healthy feeders are presented in Figure 4.28. Higher fault resistance has negative effect on the selectivity function, however, not as significant to prevent faulted feeder detection.

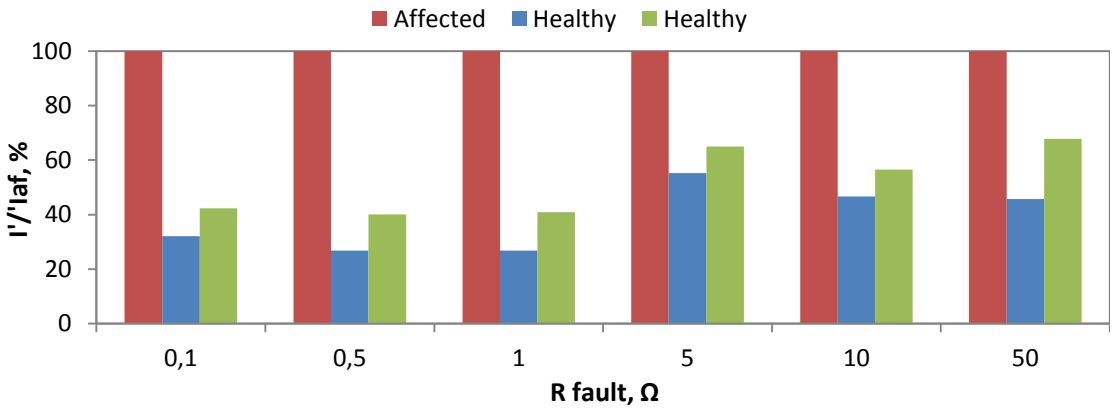


Figure 4.28: Effect of the fault resistance on the faulted feeder detection

4.3.3 Circuit breaker design

Hybrid circuit breaker topology of HPE I was used as a basis for multifeeder circuit breaker demonstration. Design of the multifeeder circuit breaker is shown in Figure 4.29, as the circuit breaker protects the feeders of the same polarity nominal current branch is separated by one auxiliary switch per feeder. Each nominal current (NC) branch is compiled of the Load Commutating Switch (LCS) that consists of two stacks of 3x3 4.5 kV/1200 A IGBT modules [75] with snubber circuit elements for fast current commutation; Ultra Fast Disconnector (UFD) that has fast opening capability and protects LCS from transient recovery voltage, UFD has similar design to the auxiliary switch. Current blocking branch consists of two stacks of IGBT that allow bidirectional current blocking. Each stack consists of 10x30 IGBTs with snubber circuit elements for blocking 12 kA current and has 612 kV withstand voltage. Maximum energy that should be absorbed by the surge arresters is 7600 kJ. Safety coefficient of 1.2 is considered here. Energy absorbing branch consists of 4 parallel surge arresters [76]. Each surge arrester has energy absorption capability of 15.4 kJ/kV and current conduction of 2,2 kA during 2 ms. Protective voltage of 560 kV is chosen that is under voltage withstand capability of IGBTs in the main breaker branch and fifty per cent above nominal voltage to prevent conductive current during auxiliary switch opening.

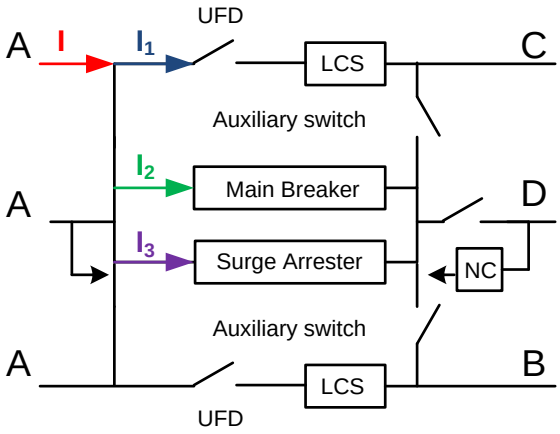


Figure 4.29: Multifeeder hybrid circuit breaker model

Auxiliary switch consists of 5 units with 80 kV operational voltage and 15 kA conducting current, each unit equipped with a Thompson drive. Parameters for Thompson drive used in the auxiliary switches can be anticipated from [77] where parameters of Thompson drive based on measurement are provided. Parameters of the Thompson drive circuit chosen: voltage of accelerating and decelerating parts is 1000 V and *C1 = 11 mF, C2 = 7 mF*.

Fault current interruption by the circuit breaker is presented in Figure 4.29; currents are illustrated in Figure 4.30. Faulted feeder is identified in 0,3 ms after the fault is detected and auxiliary switches are closed followed by commutation of IGBTs in the main breaker. After the current is fully commutated into the main breaker, LCS opens. In 2 ms, when UFD is fully opened, IGBTs in the main breaker are blocked and current flows through surge arresters and at 11,5 ms reduced to zero as inductive energy is dissipated. Auxiliary switches are fully opened at 13,5 ms and the circuit breaker is ready for the next operation.

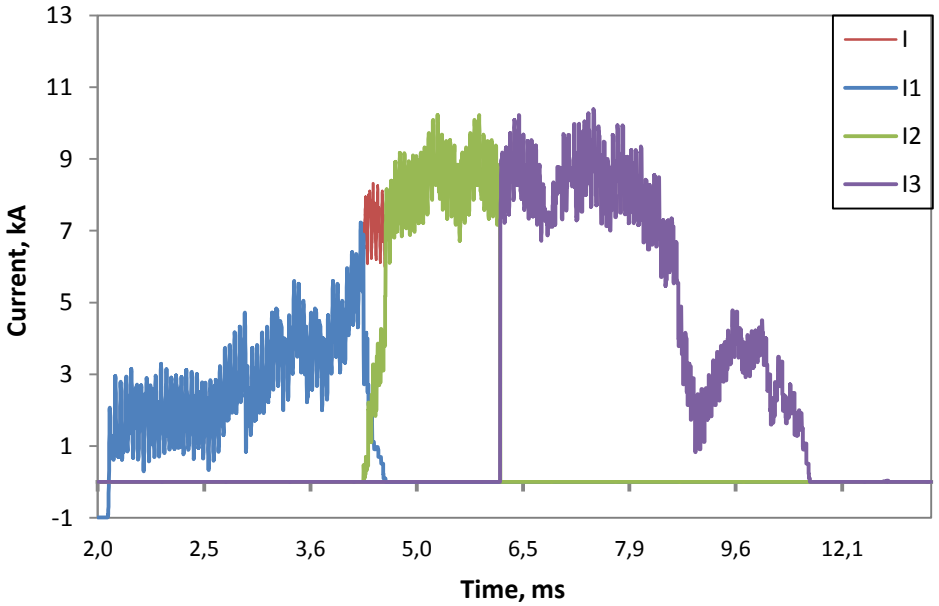


Figure 4.30: Fault current interruption by multifeeder circuit breaker

4.4 Circuit breaker performance in CIGRE Benchmark grid

Hybrid power electronic circuit breakers of 3 typesare investigated in this chapter by implementing developed models into the CIGRE Benchmark grid model shown in Figure 4.31, system parameters can be found in Annex C. A pole-to-ground fault is created in the middle of a 200 km long line that is protected by two circuit breakers on both sides. Current and voltage stresses on both circuit breakers are investigated. Next, the voltages of two converter stations are observed: one close to the fault (100km) and one far from the fault (500km). For all simulations detection time of 1 ms is considered.

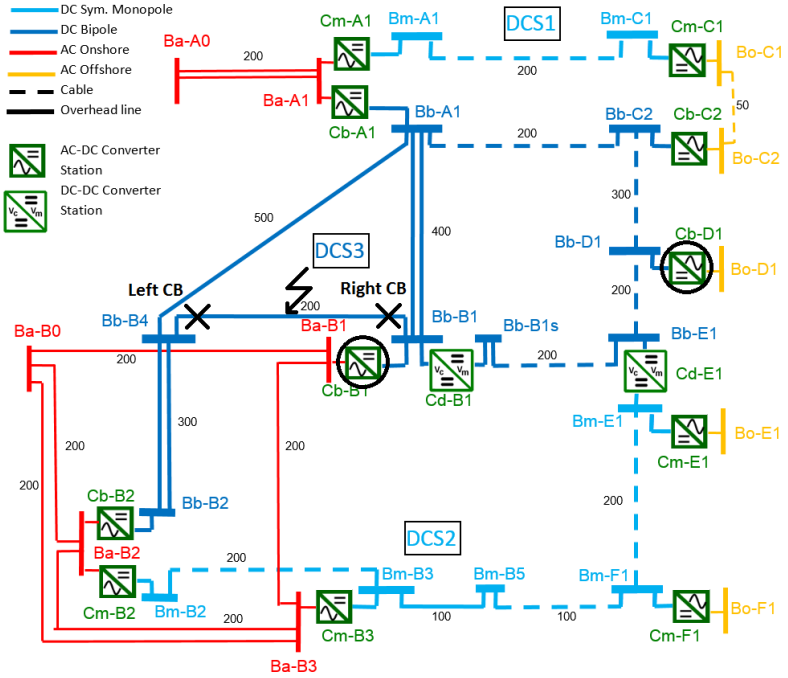
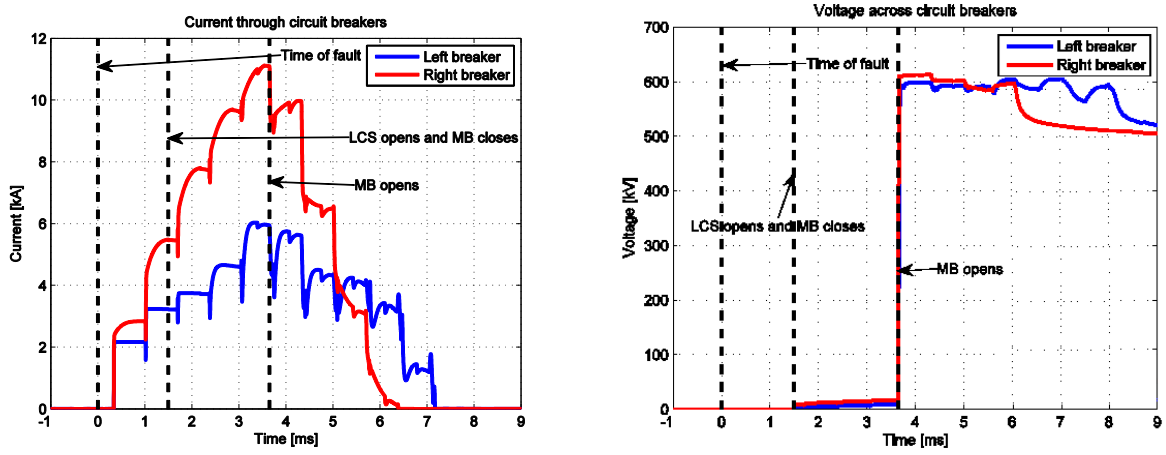


Figure 4.31: CIGRE grid model with location of the circuit breakers and the fault

4.4.1 Hybrid Power Electronic Type I (HPE I)

The results of the stresses onHPE I circuit breakers are shown in Figure 4.32. It can be observedin Figure 4.32(A) that the maximum current is flowing through the right circuit breaker. This can be expected, as the line is directly connected to a converter station on the right side. Also, the right side is connected to other converter stations by relatively short lines. Because of the short connections to other converter stations, line discharging currents will be much higher than for the left breaker. Furthermore, a strong AC network is connected to converter station Cd-B1 by a short line. This results in a low impedance path for AC network current through the right circuit breaker. Finally, the influence of current reflections can be observed as current oscillates.

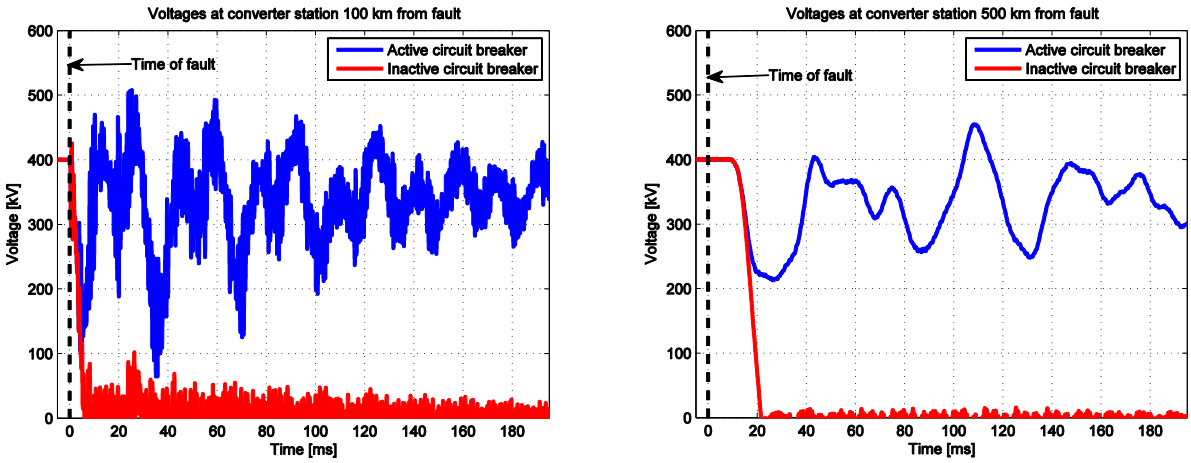


(A) (B)

Figure 4.32: Current and voltage stress on circuit breakers during fault clearing by HPE I

Figure 4.32(B)illustrates the voltage across the circuit breakers. In this figure is shown that the protection value of 600 kV is reached very quickly after the IGBTs of the main breaker are blocked. The voltage is then slowly decreasing until the current through the breaker is reduced to zero. Furthermore, it is shown that the voltage across the single IGBT of the load commutation switch is relatively low.

Figure 4.33 show the voltages of two converter stations: one near the fault and one far from the fault. Figure 4.33(A) shows that the voltage of terminal station Cd-B1 is almost immediately dropping to zero after the fault occurs in case if a circuit breaker is not installed. If the breaker is activated, this voltage drop is reduced significantly and the voltage immediately starts to recover once the circuit breakers have isolated the cable. Finally, also high frequency reflections and oscillations can be seen due to traveling waves across the grid. This effect can be reduced if converter station control is activated.



(A) (B)

Figure 4.33: Voltage at converter station 100 km (A) and 500 km (B) from the fault

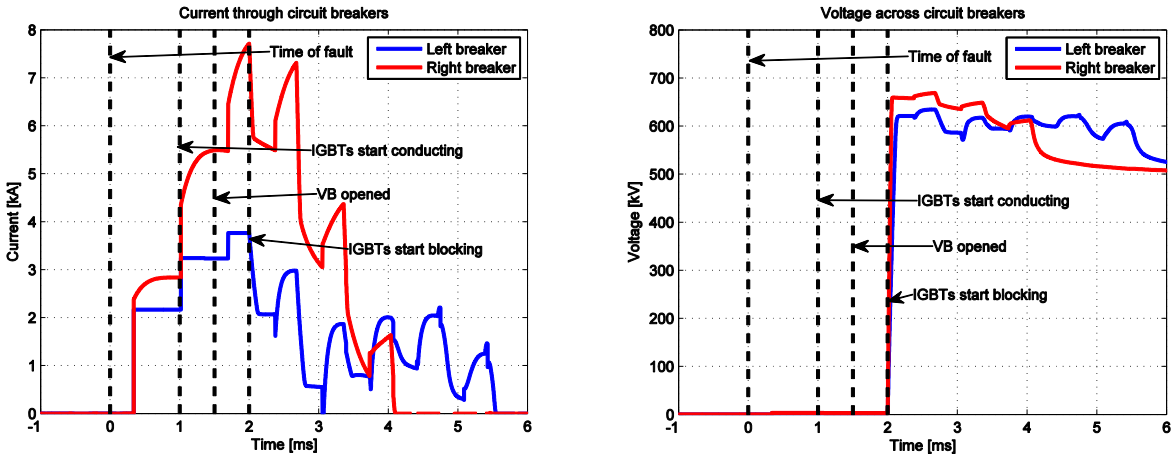
Figure 4.33 (B) shows the voltage of terminal station Cb-D1. In this figure can be seen that the voltage start to drop after a delay caused by wave traveling speed through the lines. Also, the

drop of voltage is less severe as the higher impedance to the fault increases damping. This line damping also prevents high frequency reflections to reach the far converter station. Therefore, the figures show that faults far from the converter station have reduced effects, however, still can have negative on the converter performance.

4.4.2 Hybrid Power Electronic Type II (HPE II)

The results of the stresses on HPE II circuit breakers are shown in Figure 4.34. Figure 4.34(A) shows that the highest current is again flowing through the right circuit breaker. Also, reflections have very high influence on the current behaviour. Furthermore, the figure shows how the commutation process within the breaker works, as the current is directly decreasing after the IGBTs are blocked.

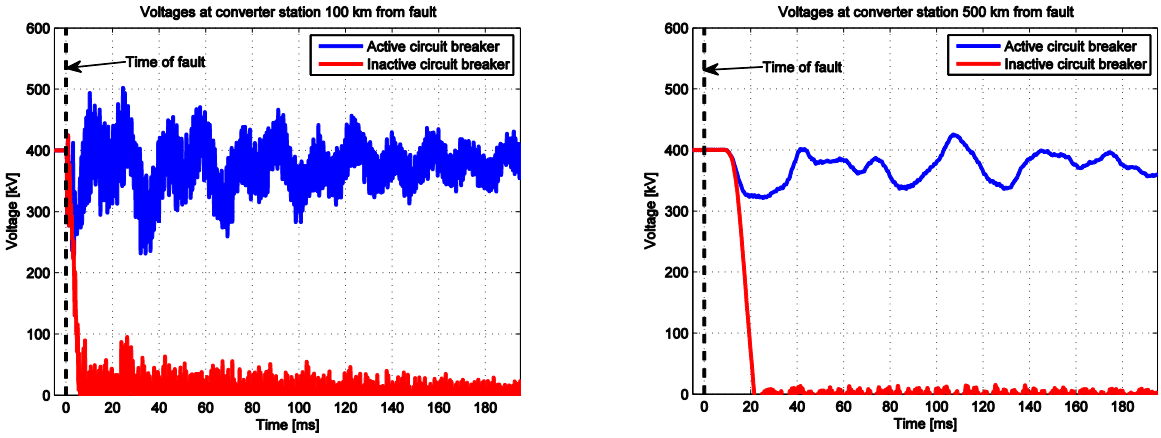
Figure 4.34 (B)shows the voltage across the left and right breaker has a similar behaviour. The figure shows that the protection voltage of the surge arrester is reached almost immediately after blocking the IGBTs. Due to traveling waves across the grid voltage does not get back to nominal level still. It takes tens of milliseconds longer for voltage to stabilize.



(A) (B)

Figure 4.34: Current and voltage stress on circuit breakers during fault clearing by HPE II

Figure 4.35illustrates that the voltage at the converter stations is only dropping slightly and also recovers relatively fast due to faster action of the HPE II than HPE I circuit breaker. The voltage at the closest converter station shows a lot of oscillations/reflections, while the voltage at the converter station far away is affected much less. Furthermore, it is shown that the voltage is only decreasing after a certain amount of time because of the wave propagation delay.

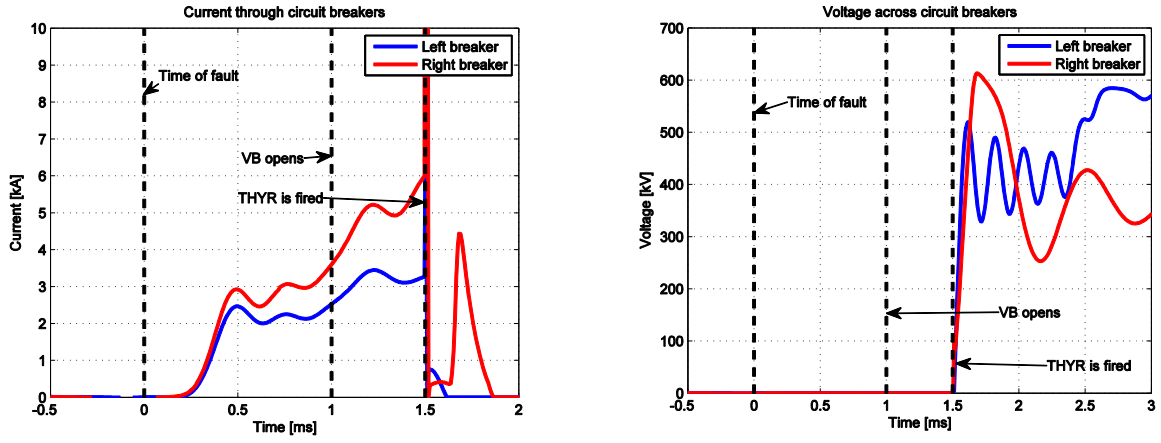


(A) (B)

Figure 4.35: Voltage at converter station 100 km (A) and 500 km (B) from the fault

4.4.3 Hybrid Power Electronic Type IV (HPE IV)

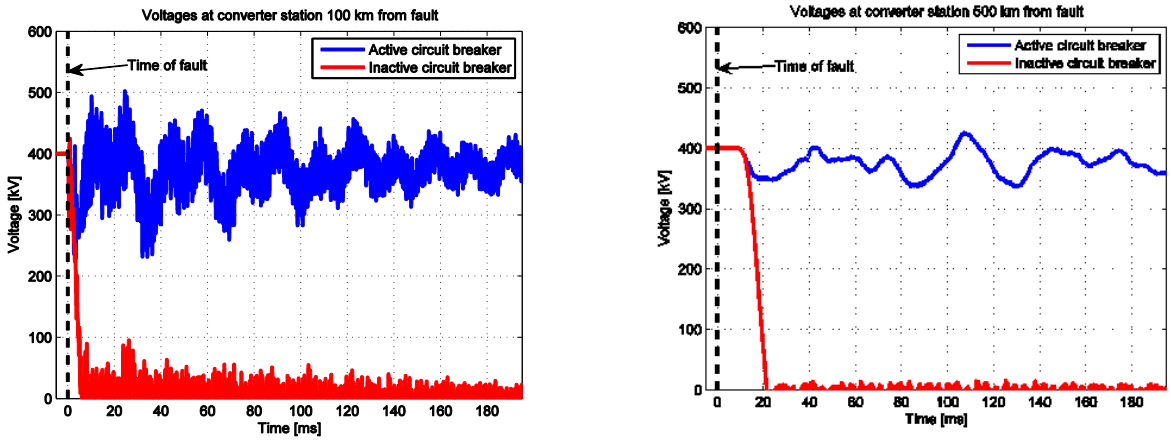
Figure 4.36 shows the current through the HPE IV circuit breaker and the voltages across the circuit breaker. For this simulation, the value of the pulse-generator capacitor C_{pg} is chosen to be 0,1 µF. Furthermore, the value of the pulse-generator inductor L_{pg} is chosen to be 40 nH. The influence of the circuit breaker on system voltage is not shown, as simulations take too much time. Figure 4.36 (A) shows that the circuit breaker is 'opened' 1,5 ms after the fault. In this figure, also a large current pulse is shown at the moment of 'opening' the circuit breaker. This current pulse has a maximum value of 10,7 kA and only lasts for several microseconds. Finally, the figure shows that the Siemens circuit breaker clears the fault current almost immediately after 'opening' the circuit breaker. After this operation, the pulse-generator capacitor C_{pg} is recharged and this fast recharging of the capacitor enables reclosing capabilities. Figure 4.36(B) shows the TRV stresses on the breaker. The maximum voltage of the right breaker is reaching the protection voltage of the surge arrester in the PG branch. Next, the stored magnetic energy is dissipated in a relatively short time and the voltage immediately drops again.



(A) (B)

Figure 4.36: Current and voltage stress on circuit breakers during fault clearing by HPE IV

Figure 4.37 illustrates that the voltage at the converter stations is only dropping slightly and also recovers relatively fast due to fast action of the HPE IV circuit breaker. The voltage at the closest converter station shows a lot of oscillations/reflections, while the voltage at the converter station far away is affected much less. Voltage behaviour is very similar to the case of HPE II circuit breaker. Although HPE IV acts even faster than HPE II voltage fluctuation caused by the fault still affects the remote terminal.

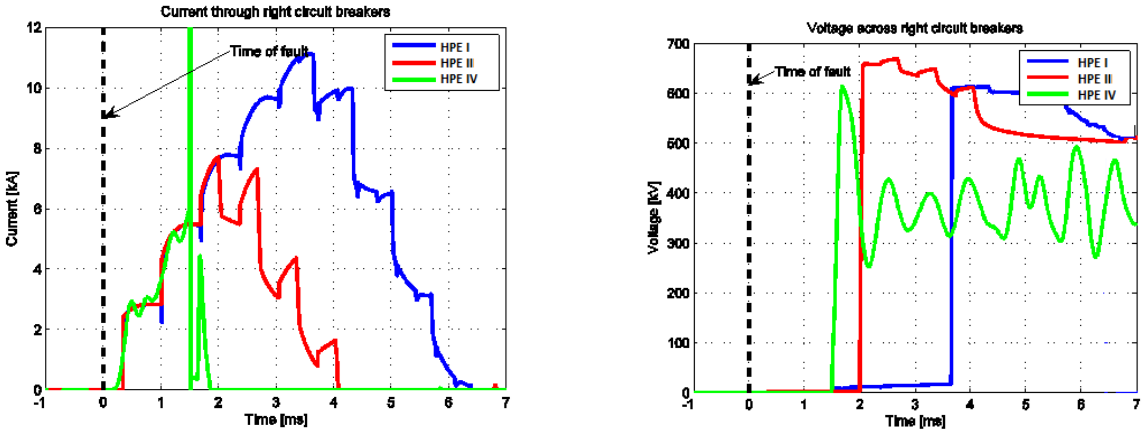


A) B)

Figure 4.37: Voltage at converter station 100 km (A) and 500 km (B) from the fault

4.4.4 Comparison Performance of Different Circuit Breakers

A comparison between the three circuit breaker technologies is shown in Figure 4.38. It is clearly shown that the HPE IV breaker clears the fault much faster than the other two breakers. The figure shows that the fault current before interruption, is not influences by the different breaker types. From TRV behaviour for different circuit breaker technologies it is clearly seen that the HPE II circuit breaker has the highest TRV stresses. Furthermore, the figure shows that the voltage across the HPE IV drops to line voltage within milliseconds due lower fault current and energy absorption by the capacitor.



(A) (B)

Figure 4.38: Comparison of current and voltage stress on hybrid circuit breakers

The performance of the different circuit breaker is shown inTable 4.3. The first column in Table 4.3 indicates the type of the investigated circuit breaker. The second column indicates the average rate-of-rise of the current from the beginning of the fault to the maximum value. The third column indicates the average rate-of-rise of the voltage when the circuit breaker interrupts the current. The maximum fault clearance time is indicated in the fourth column, and the maximum current through the breakers is shown in the fifth column. The minimum system voltage, which is measured at the nearest converter station, is shown in the sixth column. The seventh column then indicates the maximum energy that is dissipated in the surge arresters.

Table 4.3 - Comparison of performance for the circuit breaker at Cb-B1

Type	d*i*/d*t* (kA/ms)	d*v*/d*t* (MV/ms)	t_{clear} (ms)	I_{max} (kA)	$V_{sys,min}$ (pu)	$E_{sa,diss}$ (MJ)
HPE I	3.35	27.0	7.17	11.1	0.16	8.70
HPE II	4.63	10.9	5.44	7.69	0.58	5.07
HPE IV	4.27	3.39	1.86	6.00	0.65	0.31

4.5 Requirements for HVDC circuit breakers

Based on simulations performed in the previous chapters general requirements are derived that are important for designing or choosing a HVDC circuit breaker.

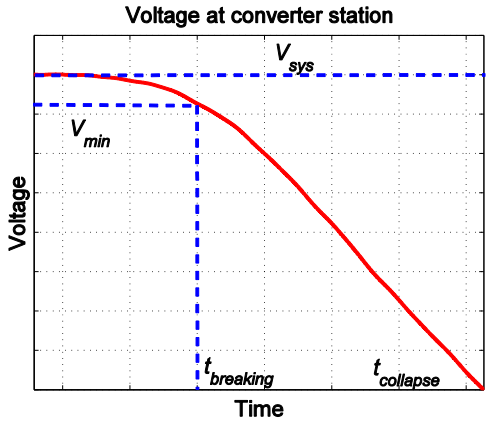


Figure 4.39: Voltage at converter station

Figure 4.39 shows the voltage at the converter station. In this figure, the nominal voltage level is indicated with V_{sys}. When a fault occurs, the voltage starts to drop towards zero. In order to prevent a collapse of the system, the circuit breaker has to interrupt the fault current before the voltage drops below the minimum system value V_{min} which is defined by the converter control system parameters. This point is called the maximum breaking time, indicated as $t_{breaking}$ in the figure. To increase this maximum breaking time, the inductance in the network should be

increased. The inductance of the network mainly consist of inductance in the line (L_{sys}) and inductance in the breaker ($L_{breaker}$). The inductance in the breaker ($L_{breaker}$) can be increased by adding a current limiting reactor. The whole breaker should then be designed in such a way that it is fast enough to clear a fault within this time.

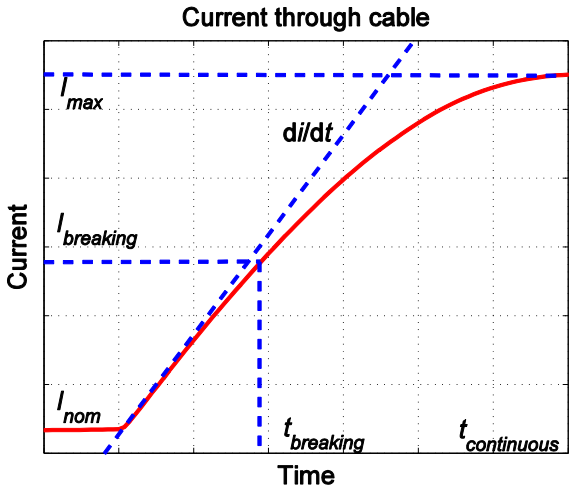


Figure 4.40: Current through the circuit breaker

Figure 4.40 shows the current through the circuit breaker. In this figure, the maximum current is indicated by I_{max}. When a fault occurs, the current starts to rise with a specific di/dt towards the maximum current. The circuit breaker then needs to interrupt the current at $t_{breaking}$. The di/dt is depended on the total inductance in the network (L_{sys}+$L_{breaker}$). To decrease $I_{breaking}$, a current limiting reactor can be placed inside the breaker to increase $L_{breaker}$ and therefore limit di/dt. The time when the maximum current is reached is called $t_{continous}$. The breaker should be designed to withstand the current at this point for a certain amount of time to prevent damage to the breaker when it cannot operate.

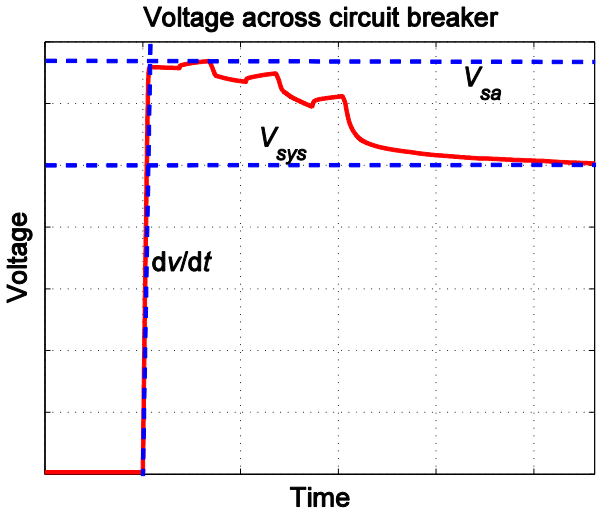


Figure 4.41: Voltage across the circuit breaker

Figure 4.41shows the voltage across the circuit breaker. In this figure the nominal voltage level is again indicated asV_{sys}. When the circuit breaker interrupts the fault current, a transient recovery voltage will appear across the terminals. This voltage will rise with a constant dv/dt, limited by the parallel capacitance of the circuit breaker. At the protection voltage of the surge arrester V_{sa}, the surge arrester dissipates the energy stored in the system. Therefore, to protect the circuit breaker, a correct snubber capacitance and protection voltage should be chosen.

The HVDC circuit breaker can be designed for interrupting nominal current (I_{nom}) or short-circuit current (I_{max}). Furthermore, different HVDC breaker technologies have different reclosing capabilities. Reclosing operation is limited by different factors, such as: thermal properties of components and recharging of capacitors etc. Finally, also the reliability of component should be taken into account. Due to the fact that faults must be switched off within several milliseconds, there could be limited room for backup protection and therefore, HVDC breakers should be very reliable.

Conclusion and future work

One of the key components required for deployment of HVDC grids similar to existing AC systems is need of DC fault protection systems. Nowadays, there is no standardised solution for DC fault detection and fault clearing equipment. In order to develop robust and efficient protection systems for future HVDC grids modelling of components is necessary that would allow investigating operation of the grid under DC fault conditions. Behaviour of the HVDC grid under DC fault conditions depends on many parameters of the grid itself such as grid topology, converter technology and protection system action.

Models of the HVDC converter developed in this thesis allow studying operation of the system under DC fault condition and investigate influence of the system parameters on its operation. The proposed converter model has no control system implemented but maintains close approximation of the converter behaviour under DC fault conditions. This model allows increasing of the system simulation speed more than ten times for point to point system and even further for a multiterminal topology.

Based on the proposed model simulations have been performed in order to investigate how HVDC system parameters, such as converter type and topology as well as transmission media, affect development of DC fault current and terminal voltage which is very important for converter operation stability. Both these parameters play an important role in understanding of requirements for HVDC circuit breakers.

HVDC circuit breakers are much different from broadly used HVAC breakers and performance of different circuit breaker designs is not fully understood. In this thesis methods for HVDC circuit breakers modelling are described. These models are later used to investigate the stresses that are applied on the components of these circuit breakers as well as HVDC system behaviour. Based on the simulations performed requirements for HVDC circuit breakers are derived. The understanding of HVDC circuit breakers performance as well as requirements is crucial for protection system development.

Hybrid HVDC circuit breakers that are considered as the optimal solution for DC fault clearance have costs much higher than AC circuit breaker due to use of power electronic components. High price of these devices increase the cost of the HVDC grid as a whole and that might limit or postpone implementation of the grid. To resolve this problem multifeeder circuit breaker topology is proposed and studied. As in multiterminal systems busbars at converters stations might have more than one feeder, use of the multifeeder circuit breaker topology allows significant reduction of the costs for feeders protection.

Protection of an HVDC grid is complex problem and has been divided into several areas such as voltage and current measurement, fault detection algorithms, fault clearance technics, circuit breaker technology and grid restoration process. The work performed in this thesis is one of the crucial steps towards development of full scale DC fault protection system that includes fault detection and isolation by circuit breakers. Developed models can be used to verify performance of protection algorithms in combination with circuit breakers and converters. Next step that should be taken is investigation of cooperation between protection algorithms and circuit breaker technologies to identify the most efficient combined solution. Another important step is to develop secondary protection methods that have not been fully addressed so far. Some ideas proposed in this thesis could help in further research.

In this work converter approximation model has been used that shows good performance for circuit breaker operation studies. However, it puts limitation on investigation of the grid restoration process as converters can help to stabilise voltage in the grid. Full scale converter modelwould help to define converter control system parameters how to behave during different fault scenarios. To simulate multiterminal system with full converter models high computation capacity would be required.

Right now local protection is considered to be an advantageous solution due to no communication delay. However, fault clearing action in one part of the grid creates traveling waves that can be wrongly interpreted by the protection system in the other side of the grid. It can lead to the wrong action and potentially dangerous state for the grid. To fully understand parameters for the protection system and converter control complex models with implemented fault detection algorithms, including measurement uncertainties, circuit breaker models and other elements of the grid should be developed and investigated. In such complex model protection methods can be tested and verified prior being implemented into a real HVDC grid.

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List of publications

Publications in WOS journals related to the thesis

1. Yanushkevich A., Švec J., "Multifeeder protection system with hybrid circuit breakers for MVDC grids", Electric Power Components and Systems, Approved for publication, ISSN: 1532-5016, 50%

Publications in peer reviewed journals related to the thesis

2. Yanushkevich A., Tlustý J., "Protection System for a Multifeeder Busbar Using an HVDC Circuit Breaker", Energetika, 2/2017, page 120, ISSN 0375-8842, 50%

Other publication related to the thesis

3. Yanushkevich A., Scharrenberg R., Kell M., Smeets R.P.P., "Switching phenomena of HVDC circuit breaker in multi-terminal system," ACDC2015, UK, February 2015, 25%
4. Yanushkevich A., Belda N.A., Scharrenberg R., Smeets R.P.P., "Transient system behaviour under DC fault conditions in meshed HVDC systems," IPST2015, Cavtat, Croatia, June 2015, 25%
5. Belda N.A., Yanushkevich A., Scharrenberg R., Gibescu M., " Investigation of Circuit Breaker Fault Clearing Performance in Radial Multiterminal HVDC Grid", HVDC2015, Korea, Oct. 2015, 25%
6. Smeets R.P.P., Kertész V., Yanushkevich A., "Modelling and Experimental Verification of DC Current Interruption Phenomena and Associated Test-Circuits", CIGRE Session, August 2014, 33%

Other publications not related to the thesis

7. Yanushkevich, A., "Using STATCOM for Active Power Compensation: Power Quality Improvement in Distribution Systems", Poster 2011, Prague, May 2011, 100%
8. Yanushkevich A., Sýkora T., Tlustý J., Švec J., "Voltage stabilisation in industrial applications using Statcom with active power compensation", ČK CIRED 2011, Tabor, October 2011, 25%
9. Yanushkevich A., "Statcom with Active Power Storage: Wind Power Park Compensation", Poster 2012, Prague, 100%
10. Yanushkevich A., Tlustý J., "Analysis of photovoltaic systems influence on low voltage distribution grid", Electric Power Engineering 2012, Brno, Czech Republic, May 2012, 50%
11. Yanushkevich A., Mareček P.,"Electromobility: distribution grid challenge. Impact of electrical vehicles on distribution grid. Electric Power Engineering 2012., Czech Republic, May 2012, 50%
12. Yanushkevich A., Tlustý J., " Active Power Compensation in Industrial Applications Using Statcom with Supercapacitors", PMAPS 2012, Istanbul, June 2012, 50%
13. Yanushkevich A., Mareček P., Tlustý J. "Using Statcom with active power compensation for voltage flicker mitigation", CIGRE B4 HVDC colloquium 2013, Brasilia, October 2013, 33%
14. Jafar M., Yang Y., Yanushkevich A., "Low frequency AC transmission for grid integration of offshore wind power", 13th Wind Integration Workshop 2014, Berlin, October 2014, 33%
15. Tourgoutian B., Yanushkevich A., Marshall R., "Reliability and availability model of offshore and onshore VSC-HVDC transmission systems", ACDC2015, UK, February 2015, 33%
16. Chowdhury N.U.A., Yanushkevich A., "Power Flow Analysis of Meshed AC-DC Super Grid", PowerTech 2015, Eindhoven, July 2015, 50%

Annex A – Models database

Models described in Chapter 3 are compiled into a database shown in Figure A.1. Models from the database can be used to study different topologies and configurations of a multiterminal HVDC grid during DC faults. Models of the circuit breakers mechanical or hybrid can be implemented into the gird to investigate performance of the circuit breakers and the system. Combination of different types of circuit breakers can be considered as well to maximise the effectiveness off the protection system.

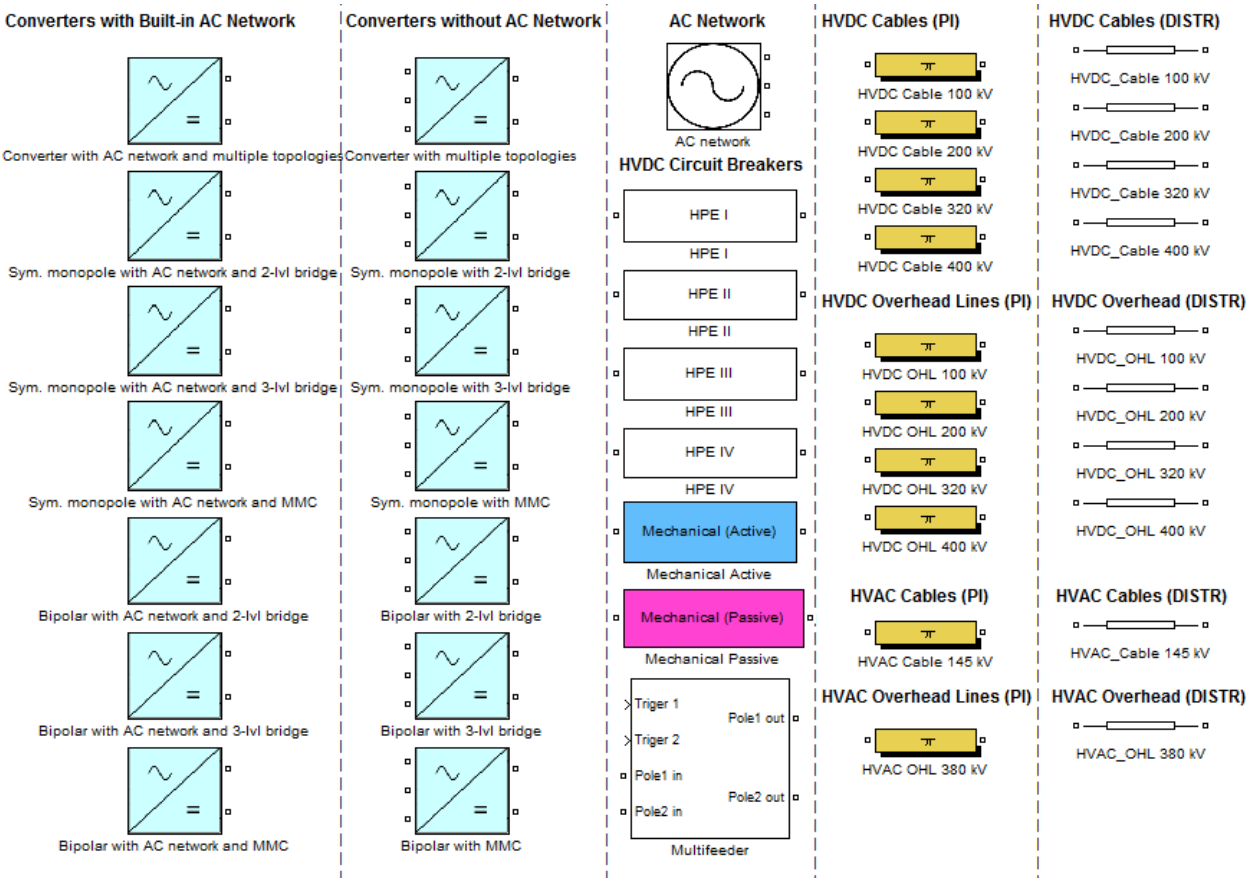

Figure A.1 – Database of models for DC fault studies

Annex B – Arrester model

The model of the surge arrester used in simulations is based on the I-V characteristic summarized in Table B.1 and presented in Figure B.1.

Table B.1 Surge arrester I-V data

Points	Voltage (p.u)	Current (A)
1	0.4	10^{-5}
2	0.8	10^{-4}
3	1	10^{-3}
4	1.15	10^{-2}
5	1.19	10^{-1}
6	1.22	1
7	1.275	10
8	1.415	10^{2}
9	1.59	10^{3}
10	1.82	10^{4}
11	2.2	10^{5}

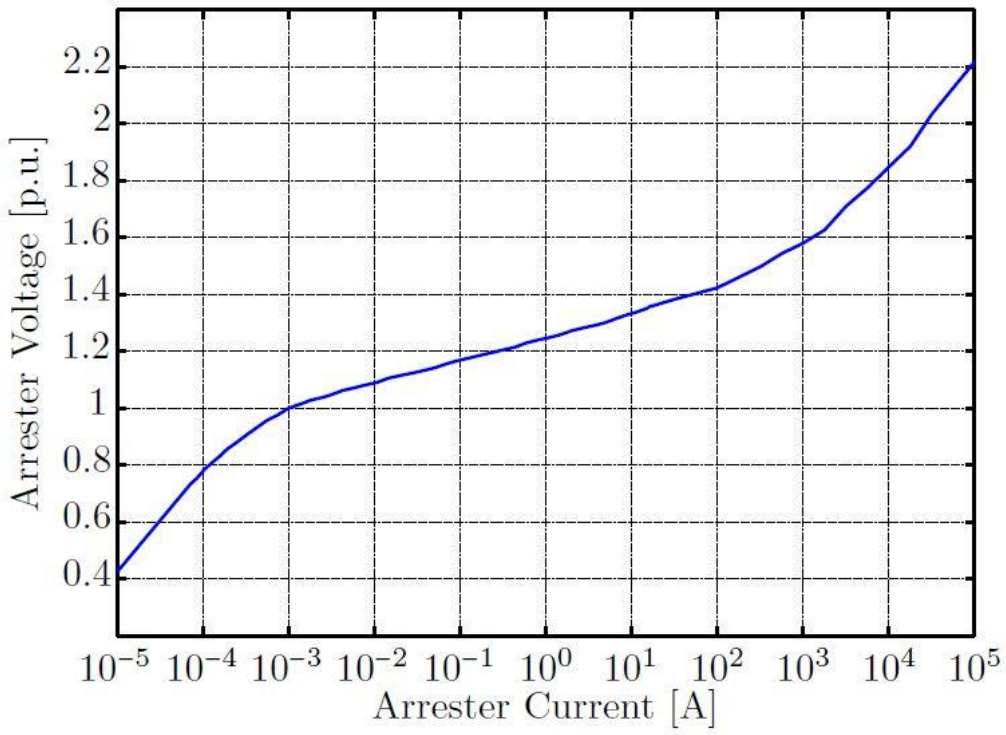

Figure B.1:Arrester I-V characteristic

Annex C – Cigre benchmark HVDC grid

Cigre B4 working group developed a VSC based DC grid test system with AC and DC parts of a very general nature with all input data [74]. It can be used as a general grid by engineering community as it has been done with the CIGRE LCC benchmark, so that the results of various DC grid studies can be compared on the same basis.

Converter model

All converters operate on 400kV DC voltage and 220kV AC voltage. The AC voltage at the Point of Common Coupling (PCC) can be either 380kV (onshore) or 145kV (offshore), but this only influences the ratio of the ideal transformer while it does not influence the rest of the converter pole model.

The model has been selected for easy implementation in average value model simulation software. All given values in pu are referring to a local converter pu system and are based on real projects. The values for converters are given in two different pu systems, one for each side. The equivalent capacitance value is based on a 1000 MVA project with the following approximate data: V_{dc} = +/-320 kV, submodule capacitance C_{SM}=10mF, number of submodules per arm: 400.

Inductance values proposed in Table C.1are composed of converter transformer inductance (18%) plus half the converter arm inductance (15%/2). The following formulae are used to calculate the physical values:

$$L = L_{pu} \cdot \frac{Z_{AC,ref}}{\omega_{ref}} \qquad R = R_{pu} \cdot Z_{AC,ref} \qquad G = G_{pu} \cdot \frac{1}{Z_{DC,ref}} \qquad C = C_{pu} \cdot \frac{1}{Z_{DC,ref}}$$

Table C.1 – Converter parameters

	pu	E1	C2	A1, B2, C1, D1, F1	A1, B1, B2, B3
S	1.0	200MVA	400MVA	800MVA	1200MVA
L	25.5%	196mH	98mH	49mH	33mH
R	1.00%	2.420Ω	1.210Ω	0.605Ω	0.403Ω
G	0.10%	1.25µS	2.50µS	5.00µS	7.50µS
C	60ms	75µF	150µF	300µF	450µF

DC-DC converter station

The offshore DC-DC converter at E1 operates at 800kV on the V_m-side and at 400kV on the V_c-side. The onshore DC-DC converter at B1 operates at 800kV on both sides. Table C.2 summarises the DC-DC converter data.

Table C.2 - General DC-DC converter station data

	pu	E1	B1
S	1.0	1000MW	2000MW
L	5ms	800mH	1600mH
R	1,200%	1,92Ω	3,84Ω
G	0,025%	0,390625µS	0,78125µS
C	5ms	7,8125µF	15,625µF

Lines and cables

The test systems contain AC and DC cables and overhead lines. The R-L-G-C parameters needed for average value simulation are given in Table C.3Table . AC lines are represented by 50Hz data and DC lines by DC data.

Table C.3 - Line data for average value model simulation

Line Data	R [Ω/km]	L [mH/km]	C [μF/km]	G [μS/km]	Max. current [A]
DC OHL +/- 400kV	0.0114	0.9356	0.0123	-	3500
DC OHL +/- 200kV	0.0133	0.8273	0.0139	-	3000
DC cable +/-400kV	0.0095	2.1120	0.1906	0.048	2265
DC cable +/-200kV	0.0095	2.1110	0.2104	0.062	1962
AC cable 145kV	0.0843	0.2526	0.1837	0.041	715
AC OHL 380kV	0.0200	0.8532	0.0135	-	3555