České vysoké učení technické v Praze
Fakulta elektrotechnická

katedra mikroelektroniky

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: **Bc. GEČNUK Josef**

Studijní program: Komunikace, multimédia a elektronika
Obor: Elektronika

Název tématu: **Návrh koncového stupně pro řízení sestupné hrany I2C**

Pokyny pro vypracování:

1. Proveďte podrobnou rešerši současných obvodových koncepcí koncových stupňů pro řízení sestupné hrany I2C.
2. Porovnejte jednotlivé obvodové implementace z hlediska rozsahu napájecího napětí, kapacitní zátěže a rychlosti.
3. Vyberte nejvhodnější řešení pro splnění následujících parametrů:
   - rozsah napájecího napětí: 1,2 V-3,6 V,
   - kapacitní zátěž Cload: 10 pF - 400 pF,
   teplotní rozsah: -50 °C až 95 °C,
4. Navržené řešení implementujte v technologii CMOS 180 nm nebo CMOS 90 nm (GPDK180 respektive GPDK090).
5. Navrhněte obvodová řešení vedoucí k zlepšení jednotlivých parametrů.
6. Navrhněte koncovou topologii (layout) čipu s důrazem na co nejmenší plochu.

Seznam odborné literatury:

[1] Gray, Hurst, Lewis, Meyer: ?Analysis and Design of Analog Integrated Circuits?, John Wiley and Sons, 2000.
[2] B. Razavi: ?Design of Analog CMOS Integrated Circuits?, McGraw Hill, 2001.
[3] NXP. I2C-bus specication and user manual Rev. 6 [online]. [cit. 2014-04-04]. Available from: http://www:nxp:com/documents/user manual/UM10204:pdf
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[5] Anderson, A.; Rutkowski, J.; Oehler, D. Edge rate control for i2c bus applications. Mar. 12, 2009, US Patent App. 11/816,710

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Master's thesis

Slope-controlled output stage of I^2C

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Supervisor: Doc. Ing., Jiří Jakovenko Ph.D.

16th February 2017

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Declaration

I hereby declare that the presented thesis is my own work and that I have cited all sources of information in accordance with the Guideline for adhering to ethical principles when elaborating an academic final thesis.

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Czech Technical University in Prague
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Abstrakt

Tato diplomová práce řeší problém řízení sestupné hrany pro velký rozsah napájecího napětí a kapacitní zátěže. Téma je návrh CMOS koncového členu sběrnice I^2C s řízením sestupné hrany v 180nm technologii. Cílem textu je shromáždit používané techniky, porovnat obvody pro řízení sestupné hrany a následně navrhnout vlastní topologii a rozmístění.

Obvody na principu řízení proudu jsou implementovány a vzájemně porovnány. Zpětná vazba a techniky využívající snímání napětí a kapacity sběrnice jsou popsány. Dostupné řešení spotřebou, plochou nebo rozsahem napájecího napětí však neodpovídají představě pro použití jako univerzální koncového členu pro sběrnici I^2C. Navržený buffer jde jiným směrem a využívá zpožďovací členy spolu s několika vybíjecími cestami.

Statická spotřeba prezentovaného řešení je více než 5,3 krát menší, než u běžně používaného obvodu. Tento buffer je vhodný pro realizaci v přenosných zařízeních komunikujících po sběrnici I^2C v High-speed módu.

Tato práce ukazuje alternativu v přístupu k řešení koncového členu pro I^2C sběrnice pracujícího v High-speed módu.

Klíčová slova koncový stupeň, řízení, sestupná hrana, i2c, návrh,otevřený kolektor, koncová topologie, 180 nm

Abstract

This master thesis deals with the problem of controlling the slope for large range of capacitive load and voltage. The central topic of the thesis is a design of CMOS Slope-controlled output stage of I^2C bus in 180 technology. The text aims at collecting the technique in use, comparing the circuits for slope control and subsequently suggests an own topology and a layout.

Circuits that handle current control are implemented and compared reciprocally. The feedback as well as technologies utilizing sensing of the voltage and capacitance are described. Available solutions that would be in compliance with the concept that would be suitable for use as a universal output stage for I^2C bus fail in consumption, surface or range of supply voltage. The buffer proposed is heading another direction and uses delay elements with several sinking paths.

Static power consumption of proposed solution is more than 5.3 times smaller than it would be if compared to a commonly used circuit. The buffer is suitable for use in portable devices that use I^2C bus in a high-speed mode.

What the thesis presents is an alternative approach to solving the output stage of I^2C buffer in a high speed mode.

Keywords output stage, i2c, slope-controlled, slew rate, fall time, cmos, pvt, variations, buffer, open drain, layout, high speed

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Introduction

Nowadays most electronic systems are using logical one and zero to store, compute and transfer informations. Mainly due to their immunity to noise. These systems are called digital systems. In digital systems one and zeros can be represented as 0 voltage and a high level of voltage and nothing in between. In case of data transfer, ideally it is expected that changes between 1's and 0's are happening infinitely fast, thus when observing the signal in an oscilloscope it should look as perfect shaped squares.

Taking the real world into account some arising complications had to be bear in mind. Change between 0 and 1 cannot happen infinitely fast, because for that it would be needed an infinite amount of energy. But at the same time, communications must be as fast as possible. Without losing any information, without disturbing other communication lines and making the information readable for receiver device. For this, the transitions need to have suitable shapes. Therefore compromises must be established.

This thesis aims at interface between the chip and communication line (bus). A closer look at communication between two or more devices on printed circuit board through a bus line will be taken. I^2C is Inter-Integrated circuit bus, which is used for communication between chips and components.

Every transmission medium have certain characteristics and comes with limitations. Transmission line can be modeled in different ways for particular purposes and with several levels of model precision. I^2C is used for short distances between devices. Data can be transmitted through wire or PCB. Transmission line and receiver for I^2C is modeled as capacitor, which can acquire big range of capacitance. To overcome the loses caused by metal connections and the transceiver input circuits the need for an output buffer emerges.

It is possible to fulfill, or at least get close the ideal digital communication, but with several consequences. For quick change of voltage from rail to rail, high current is unavoidable. The amount of current is dependent on load capacitance. To sustain same slope with higher load capacitance more current

is necessary. Sink or source big amount of currents demands large output components. Large output transistor will result in using tremendous area of the chip. This will lead to higher cost of the device. Cost is an important factor, therefore using big chip area should be avoided if it is possible.

Also high current flow in the circuit would increase the volume of heat losses. Thus reduction of resistance of the switching components has to be done and relocation of the heat to cool down the device would be necessary. Last but not least, having fast changes of current implies that strong electromagnetic fields are created, those can be received by another line and disturb the communication.

In one sentence, nice squares like from digital theory can be made, nevertheless it is challenging for since it is redeemed by area, power consumption and noise. These are exactly things which should be minimize, hence can be observed that this is not a good manner. Therefore another approach would be desirable. Agreement on certain transition time and shape can be made, which would be suitable to sustain the same speed of communication. And also that would be easily readable in a same way as previous case. Thus by the alternation of the output signal shape, the price and power consumption can be minimized.

Topology for I^2C high speed mode with a controlled slew rate will be proposed, but the principle can be used easily for any other communication protocol.

Motivation

An interesting task is set, when there is a need for output buffer that would be capable of working in a wide range of supply voltage, temperature and drive capacitive load, which can be small or big, in a similar way.

It is not so simple to create such a solution, because with the changes of voltage and capacitance the ultimate answer can vary. Usually it is solved by using programmable driver, which is digitally set up to work under certain conditions. Other things that have to be taken into account are process variations. Process variations can greatly affect the final function of circuit depending on technology and on capability of manufacturing the chip of a good quality. So even if simpler solution is found, there is frequently a need for trimming if produced circuits are not in compliance with requirements.

Both of these solutions are impractical. For programmable driver numerous controlling lines are necessary, and even if those are minimized, the whole circuit is massive, because it contains a lot of components, which are connected or disconnected according to the working conditions. As a result of this, the circuit will cover a big area of the chip, which is unwanted because it will increase the manufacturing price. Trimming every produced chip is also un-

wanted, because it increase the manufacturing time, complexity of production and costs.

Therefore there is a need to precisely crafted solution, which can be simple and at the same time would use small amount of components as possible, cover small area and fulfill requirements in wide range of working conditions.

Objectives

Goal of this Thesis is to design a slope-controlled output buffer for I^2C bus, in high speed mode, in 180 nm process using the design kit provided by Cadence® (GPDK180). Buffer should be capable of operating for supply voltages between 1.2 V and 3.6 V. Temperature can change from -50°C to 95° C. Buffer will load capacitance according to specification which can varies from 10 pF to 400 pF. Buffer should sink charge from capacitor fast enough to enable communication of 3.4 Mbits, but also slow enough to not cause peaks, which can disturb another communication. Slope of the output should be regulated in such way that fall time for load capacitance between 10 pF and 100 pF should go from 10 ns to 40 ns and for 400 pF load capacitance between 20 to 80 ns. Low level output voltage should not exceed 0.4 V for supply voltage higher than 2 V. For supply voltage lower than 2 V low level of output voltage should be smaller that 0.2 V_{DD}. Power consumption is mostly defined by the sink current during the logical low on output. The layout should be small as possible.

Several existing topologies will be examined and modified in a way to fulfill the specification for I^2C. Compare them and try to find right one for this application. In case that none of the circuits will be satisfying, new design will be proposed

Chapter 1

I²C bus

1.1 Generally

I²C stands for internal bidirectional two-wire bus. A serial data line (SDA) and a serial clock line (SCL). Each device is software addressable by a unique address. Bus includes collision detection, arbitration for preventing the data from corruption in case of using more masters and it has open collector/drain. Standby state is defined by logical one by pull up resistor connected to V_{DD} or current source. The bus is working for load capacitance smaller than 400 pF. For capacitance higher than 100 pF there is a need to add current source to secure that bus will be in logical 0 in defined rise time. Data are changing when clock signal is in logical zero (SCL=0). In standard settings, the data are send in 8bit chunks and they are followed by Acknowledge bit. Addressing is made by following sequence: Start condition, 7 bit address, 0 read/1 write. The input levels of the logical 0 and 1 are not fixed and depend on V_{DD}. Vlow = $0.3V_{DD}$ and Vhigh = $0.7V_{DD}$.

Table 1.1: Bi-directional modes of I²C

Name of Mode	Bus speed
Low speed mode	10 kbps
Standard mode	100 kbps
Fast mode	4000 kbps
Fast mode+	1 Mbps
High speed mode	3.4 Mbps

Originally the I²C bus was limited to 1000 kbps operation. Over time there have been several additions to the specification. Now, it is divided into five operating speed categories. Standard-mode, Fast-mode (Fm), Fast-mode Plus (Fm+), and High-speed mode (Hs-mode). Devices are downward-compatible, any device may be operated at a lower bus speed. Ultra Fast-mode devices

are not compatible with previous versions, since the bus is unidirectional. Complete list of bus speed and following modes is shown in Table 1.1. [1]

1.2 Transmission line

The need of such devices as a buffer is caused by non-ideal environment. Every transmission line has certain resistance, capacitance and inductance depending on its type and environment. With every of this characteristics differing from ideal, losses appear. Model of a transmission line and losses can be simple or very complicated depending on the requested precision, which is usually bond with working on higher frequencies. I²C implies usage as internal bus, therefore use on long distances is not expected. According to specifications, the bus is modeled by ideal capacitance which can vary from 10pF to 400pF. Taking in account the maximum frequency of High speed mode and hinted usage of the bus, capacitance models the transmission line satisfyingly.

These characteristics are unwanted, because they are causing distortion of the emitted signal. To overcome this, signal has to be modified in a certain way, to ensure that the signal will be readable by a receiver. As can be observed the extreme states can appear. In case of high capacitance, discharging of such a capacitance will take longer time if to assure readability, communication speed has to be lowered. That is not acceptable, therefore current has to be sank faster. For small capacitance the discharge will happen quickly, thus this is not a problem, output will be well readable. For such a short transition, another complication arise. Quick change of current can cause distortion on surrounding lines around bus, which has to be taken into account. Current peaks also should be eliminated by regulating the current.

To eliminate influence of the transmission line in this concrete case, the problem is reduced to regulate current during the transitions.

1.3 Buffer

For communication on lower speed, nxp proposed slope-controlled output stage which is shown in Figure 1.1. Basic principle is to form a low pass filter, which is modulating a slope responsible for is controlling the output transistor N2.

1.4 High speed mode

To achieve desirable speed of 3.4 Mbits, few changes were made from regular I²C specifications:

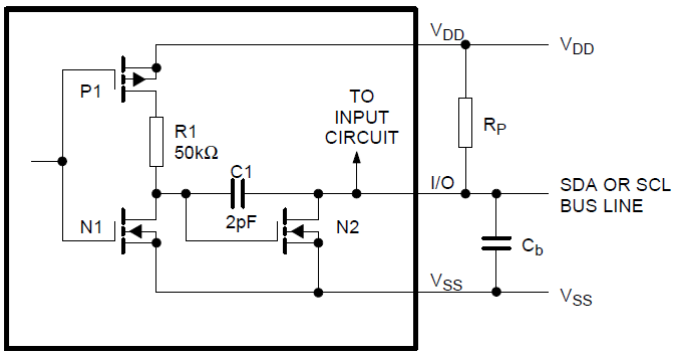


Figure 1.1: Slope-controlled output stage in CMOS technology [1]

- Master device for SCLH output has open-drain pull-down and current-source pull-up circuit, which shortens the rise time of SCLH signal. Only one current-source is enabled at one time.

- There is no arbitration neither clock synchronization during HS-mode transfer that allows higher speed.

- Master device generates SCL signal with a HIGH to LOW ratio of 1 to 2.

- It is possible to include a built-in bridge into HS master device, which separate SDAH and SCLH from SDA and SCL and helps to reduce capacitive load of the HS bus.

- Optional pull-down transistors on the SCLH pin can be used to stretch the LOW level of the SCLH signal. This is only possible after acknowledgment but in HS mode.

- Input has spike suppression and a Schmitt trigger.

- An output buffer has a slope control of the falling edge.

Short version of most crucial specification for I^2C high speed bus buffer in shown in the following Table 1.2

Bus configuration in High speed mode can be seen in 1.2

When the bus is free, the pull-up resistor maintains the SDAH and SCLH lines at HIGH level. For capacitive loads higher that 100pF, resistor can be replaced by external current source pull-up, to meet rise time specifications. Before acknowledge bit, SCLH in HS transfer is shortened by current-source pull-up circuit of the active master.

Table 1.2: Specification of I²C High speed mode

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	LOW-level output voltage	$V_{DD} \leq 2$ V	0	$0.2V_{DD}$	V
		$V_{DD} > 2$ V	0	0.4	V
t_{fSCLH}	fall time of SCLH signal	load 10 pF - 100 pF	10	40	ns
		load of 400 pF	20	80	ns
t_{fSDAH}	fall time of SDAH signal	load 10 pF - 100 pF	10	80	ns
		load of 400 pF	20	160	ns
t_{sp}	pulse width of spikes	SDAH and SCLH	0	10	ns

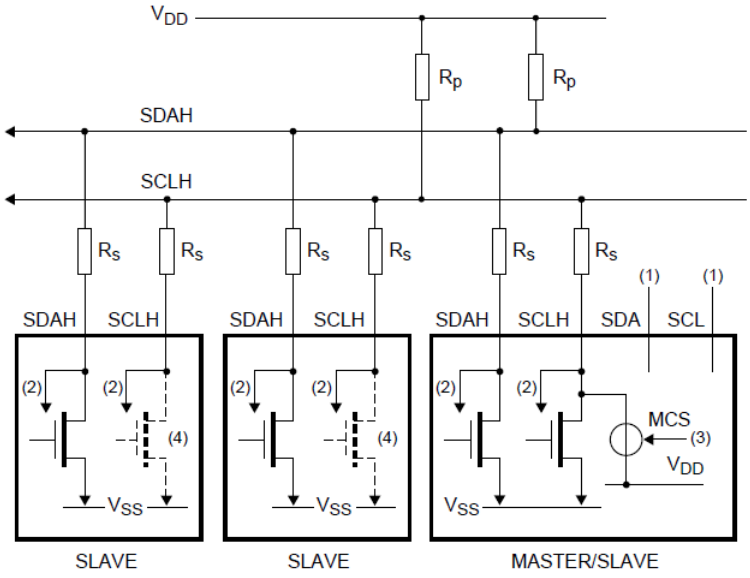


Figure 1.2: I²C-bus configuration with HS-mode devices only [1]

1.5 Open drain

I²C is an open drain bus. Output buffer can pull the bus down to the ground or release the bus. When the bus is released, level of the bus is defined by Pull-up resistor R_P, which is pulling the bus to Supply voltage. This is useful for bidirectional communication because no device can force a line into a high state. In case of multi-master communication, when master is transmitting logical high and observe that bus is in a logical low (another master is pulling the bus down), master will bring the communication to a halt.

Pull-up is usually realized by external resistor. Value of resistor depends on supply voltage, load capacitance and maximum communication speed.

Strong pull-up (small resistor) is sourcing maximum allowable current.

Minimum value of resistor can be calculated from

$$R_P(min) = \frac{V_{DD} \cdot V_{OL}(max)}{I_{OL}} \tag{1.1}$$

where V_{DD} is supply voltage, $V_{OL}(max)$ is maximum voltage during logical LOW and I_{OL} is maximum pull up current. Value of $V_{OL}(max)$depends on supply voltage and can be seen in Table 1.2. Taking corner values of operational voltage, $R_P(min)$ is shown in Table 1.3.

Table 1.3: Minimum pull-up resistor

$V_{DD}[V]$	1.2	2.4	3.6
$R_P(min)[\Omega]$	**320**	**666.6**	**1066.7**

On contrary week pull up (maximum pull-up resistance) is determined by bus load capacitance and rise time requirements. Because it has to be secured that the line will rise to the logical HIGH state, before it will be pulled down. Maximum pull-up resistor can be calculated from maximum rise time

$$R_P(max) = \frac{t_r}{0.8473 \cdot C_B} \tag{1.2}$$

where t_r is rise time from 0.3 V_{DD} to 0.7 V_{DD} and C_B load capacitance. Taking values from specification. Maximum value of pull-up resistor is shown in Table 1.4

Table 1.4: Maximum pull-up resistor

$C_B[pF]$	10	100	400
$R_P(max)[\Omega]$	**1180**	**472**	**236**

Chapter 2

MOSFET

Metal-oxide-semiconductor field effect transistor have become dominant in the area of digital integrated circuits thanks to high density and low power dissipation. For analog application bipolar transistors are more widely used because of their better performance, for example transconductance per unit of bias current. But all-MOS processes are cheaper then combined solutions. So it is understandable that if economic considerations are taken into account, circuit manufacturers prefer to use all-MOS processes.

Digital chips have to embody analog circuits, like in the case of output buffer, there is a need to study characteristics of mosfets, which influence analog design. [2]

2.1 Structure

N-channel MOS consists of heavily doped n-type source and n-type drain made on top of p-substrate. Between the channel and gate contact, there is a thin layer of silicon dioxide. A cross section of NMOS transistor is shown in Figure 2.1

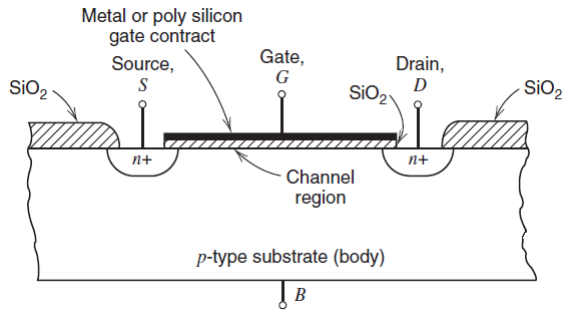


Figure 2.1: NMOS structure cross section[2]

When positive voltage is applied at gate contact, conductive channel under gate is formed (considering enhancement-mode NMOS).

2.2 Model

Usually in analog design the transistor is biased to certain operation point and by small changes of V_{GS} are driven big changes of current Ids. Therefore small signal model is widely used in analog design. In the case when V_{GS} will be swept in the whole range from 0 to 3.6 V, large signal model will be more useful. A transistor will go gradually through all states, from closed through a triode region to a saturation region. This heavily simplified model is just showing that according to V_{GS} the current source between D and S is changing and neglect any parasitic influences as is shown in Figure 2.2

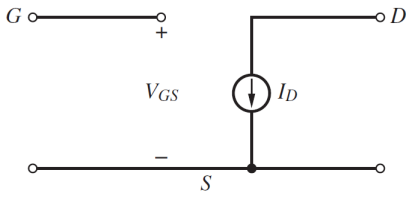


Figure 2.2: NMOS large-signal model[2]

2.3 Operational regions

Depending on V_{GS} and V_{DS} , the transistor work in different operation regions, which is shown in Figure 2.3.

As designers, voltages can be adjusted to make transistor operate as it is desirable. It is also dependent on threshold voltage. V_{TH} cannot be moved so easily and usually this voltage is considered as constant. Of course threshold voltage is not constant at all and it is changing depending on temperature apart from other variables. Dependence of temperature on V_{TH} is more closely studied in section 3.3.3.

Difference between V_{GS} and V_{TH} is called "overdrive voltage". If overdrive voltage is smaller than Vds than transistor work in triode region. If this overdrive voltage is bigger the transistor is in saturation regions, sometimes also called active region.

Distribution of operation regions is better understandable from following equations.

$$V_{DS} < V_{GS} - V_{TH} \quad Triode\ region$$
$$V_{DS} > V_{GS} - V_{TH} \quad Saturation\ region$$

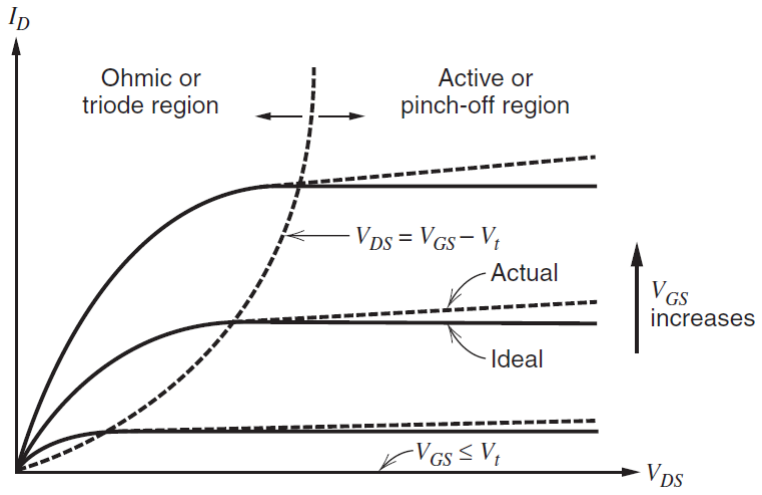


Figure 2.3: NMOS device characteristics[2]

2.3.1 Triode region

As can be seen for V_{GS} smaller than V_{DS} - V_{TH} , transistor operates in triode region. Where drain current can be written as

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{TH})\, V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.1}$$

where

- μ_n - Mobility of carriers
- C_{ox} - Capacitance of oxide
- W/L - Width and length of a transistor
- V_{GS} - Voltage between gate and source electrodes
- V_{TH} - Threshold voltage of a transistor

2.3.2 Saturation region

When voltage V_{GS} is higher than V_{DS} - V_{TH} , the drain stop following parabolic behavior for triode region and the I_D stays almost constant. This region is called saturation. Saturation phenomenon is caused because the conducting channel does not reach all the way to the drain. The channel is "pinched-off". The difference of local potential under gate is not sufficient to sustain

an inversion level and this point is moving closer to the source with higher voltage. Dependence of drain current in saturation can be written as [3]

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2 \tag{2.2}$$

As Figure 2.3 shows the Ids is slightly changing with a rising V_{DS} , this is caused by channel-length modulation. Because the effective length of channel is getting smaller. This behavior can be suppressed by using transistor with longer channel. The dependence of drain current in saturation with channel-length modulation can be written as [3]

$$I_D \approx \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2 (1 - \lambda V_{DS}) \tag{2.3}$$

Chapter 3

CMOS Process gpdk180

General process design kit 180nm by Cadence® will be used for design and simulations. Process design kit contains the process technology and all information, which is necessary for device-level design. GPDK180 consists of these types of components: resistors, capacitors, mosfets, bipolar transistors and inductor. CMOS process is used mostly for digital circuits. Precision of passive components is in CMOS process is usually lower than for processes used for analogue circuits. Library also contains information about process variations.

3.1 Process variations

Semiconductor chips are usually made in a huge series. Depending on technology, devices fabricated on the chip can differ. They can vary from lot to lot, from wafer to wafer, from die to die. For example oxide thickness or diffusion depths are the few of parameters which can vary. It is result of non uniform deposition or diffusion. As a consequence of this the electrical parameters can differ from one transistor to another. Same is applied for resistors or capacitors. Example of such parameters are sheet resistance and threshold voltage.

Manufacturer provide us device models. The process corners for CMOS technology are:

- FF Fast NMOS, Fast PMOS
- FS Fast NMOS, Slow PMOS
- TT Typical NMOS, Typical PMOS
- SF Slow NMOS, Fast PMOS
- SS Slow NMOS, Slow PMOS

Fast means, that the corner have higher carrier mobilities for one type of transistor. Contrary to that, slow means lower carrier mobilities. Typical is not really a corner. Corners can be divided on even (SS, FF) and skewed (SF, FS). Nowadays the skewed corners should concern us more, because they causes non even switching in circuit.

3.2 Passive components

In library two types of resistors can be found, diffused and insulated. Diffused resistors are formed from n+ dopped area, which is normally used for forming source and drain. Insulated resistors are poly resistors isolated from silicon by oxide. Thus options for resistors with different square resistivity are:

- nplusres have square resistivity 50 Ω/sq
- pplusres 158 Ω/sq
- polyres 7.5 Ω/sq
- polyhres 352 Ω/sq
- nwellres 415 Ω/sq

High polysilicon resistor will be used for this design. Model of the high polysilicon resistor has temperature dependency $2.9125 \cdot 10^{-3}/°C$.

Model of resistor only obtain information about typical fabrication, corners for fast and slow were added. Value change of +/- 30 with process and temperature was implemented. This should sufficiently describe the process and ensure that the design will be robust.

For a capacitor in gpdk180 are three option:

- mimcap
- pmoscap
- nmoscap

Pmoscap is formed from pmos transistor connnected as capacitor, where the capacitor is the capacitance of the gate. Pmoscap would be preferable option because it is available in every library. Mimcaps do not have to be available in every real technology. The reason for using mimcap, can be that it exhibits different characteristics than pmoscap, which are more close to an ideal transistor.

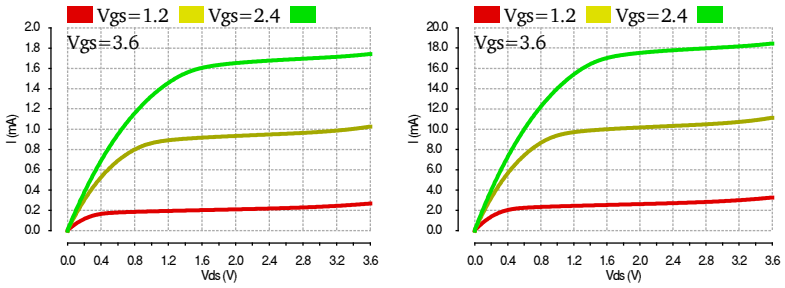
Unfortunately, GPDK180 does not contains 3V transistors. The closest transistors are transistors for nominal voltage 2.5 V (mos25), but it needs to be verified the model is valid for voltage 3.6 because our device should operate from 1.2 V to 3.6 V. The GPDK180 is based on BSIM3v3

3.3 Model of the transistor - nmos25

Transistor models nmos25 and pmos25 will be used for this circuit. Verification of the function over the full voltage range, has to be made. To verify this, drain current will be measured for changing drain-source and gate-source voltage.

3.3.1 Verification of I_{DS} vs V_{DS}

What becomes a prime interest is if the transistor is defined from 0 to 3.6 V or if the characteristics after 2.5 V, which is nominal voltage of this transistor, go straight up. Simple circuit measuring was made in Cadence® tool kit. DC analysis where V_{DS} was swept in the voltage range and V_{GS} was used as parameter. Characteristics for I_{DS} vs V_{DS} for W=2 μm, L=350 nm and W=20 μm, L=350 nm are shown are Figure 3.1. It can be observed that model works properly in the selected voltage range.

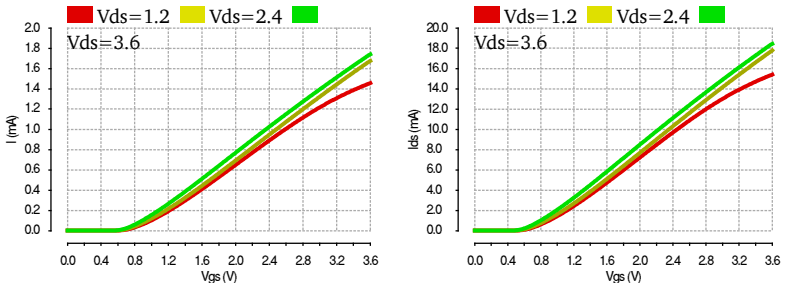


(a) W=2u, L=350 nm (b) W=20u, L=350 nm

Figure 3.1: I_{DS} vs V_{DS} of NMOS

3.3.2 I_{DS} vs V_{GS}

Simulations for sweeping V_{GS} are shown in Figure 3.2.



(a) W=2u, L=350 nm (b) W=20u, L=350 nm

Figure 3.2: I_{DS} vs V_{GS} of NMOS

It can be seen that the transistor has nice linear dependence on V_{GS} after it exceeds the threshold voltage. According to V_{GS}, transistors are in different operation regions.This allows second verification that is working correctly in selected conditions.

3.3.3 V_{TH} vs temperature

With changing temperature occur significant change of the threshold voltage. This dependency is crucial if the transistor has to be set to a certain operation point. For example in Patent US 6670822, when the transistor is set to provide current for closing the output transistor. Temperature dependency is show in Figure 3.3

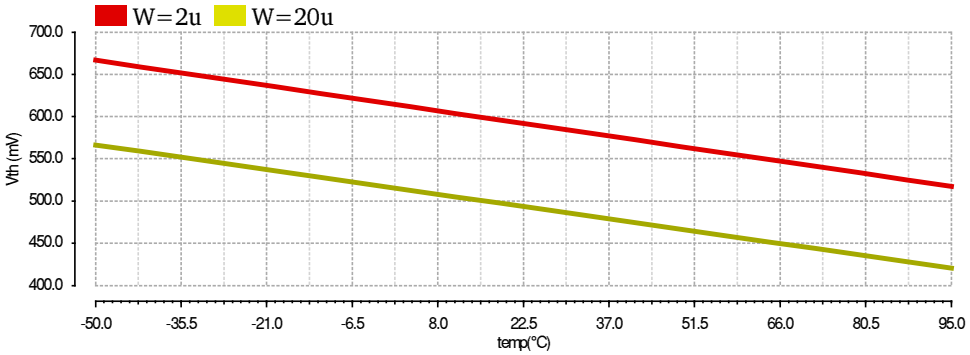


Figure 3.3: V_{TH} vs temperature for NMOS

Chapter 4

PVT variations

A closer look at the at the topology design, from the perspective of the Process, Voltage and Temperature variations, will be taken.

Although nowadays is tendency to use statistical methods, because simulating through PVT corners are giving us too pessimistic results and therefore the circuit is over-designed. Which can cost us power consumption or area to maintain the same functionality even for worst case, which would statistically most likely never happen. [4]

Reason for using approach of PVT variation can be an insufficient accuracy of statistical process variations for selected technology. Which is exactly our case. For process design kit 180 nm is crucial to use PVT variations, because there are no satisfying models available for statistic approach. Also proposed circuit has to work under different supply voltage and has to fulfill the specification for every load, thus it is necessary to go through corners of these different operating conditions. Again it is underlaying approach if intention is a robust circuit.

From combination of process, voltage and temperature variations, PVT corners are obtained. Under the normal circumstances huge amount of corners is obtained, that introduce enormous time consumption necessary for simulations.

Analysis through PVT corners aims to find worst case for every output. If the worst case is found, design can be optimize for the best performance and guarantee that circuit will work under all circumstances. With older technology was acceptable smaller amount of corners, usually FF, SS and minimal and maximal voltage end temperature. Therefore was enough to run simulations through 8 corners. Nowadays this path would be inadequate, at least brackets has to be found for every specification. Specially taking into account multiple supply voltage levels and different value of load colossal amount of simulations is obtained. All of them has to be simulated to affirm functionality of the circuit.

Simulating every corner can last few seconds, minutes or hours. This

can be time consuming. With experience with certain circuits, designer can guess the worst case corner, but that can be risky and in case of wrong guess it another time spend on simulations. Result of worst corner can be with great profit used for design loop of changing design variable, let say width of transistor to obtain best performance or smallest area. Taking this to account asks for the use of this discovery to a greatest extent.

This can be done with brightly selecting approach to simulating PVT variations [5]

4.1 PVT variation flow approaches

First obvious one is to start with topology, size it and do the full PVT corners simulations, and with every adjustment of circuit do the full PVT simulations again. This is futil from perspective of time, in case of complex circuit it can took about weeks spend just on simulations.

Second approach which was already voiced is guess. With enough experiences in field and with similar topologies nature of the circuit can be more or less foresee. This technique is fast, but in case of wrong assumption can lead to circuit, which will not behave correctly or more simulations. Commonly this access is improved by full PVT verification.

PVT variation oriented approach is for a such design fundamental. To guarantee that circuit will work under all conditions and his parameters will not change much in a wide spectrum. Compensation for this is robust design is slightly bigger power consumption and area. Time spend on simulations can be abbreviated by wisely selecting flow for PVT simulations.

Chapter 5

Problems that need to be addressed

In this chapter a short glimpse will be taken on some aspects, which have to be kept in mind during whole process of design a buffer. Load capacitance will be charged and discharged. Load capacitance is modeled as ideal capacitor persistent with specification of the I^2C. It is mandatory to stay in time specification and assure that shape of the transition will happen in a well defined way. Next, area of the design should stay small as possible, this can be done by using bold layout technique and crafty topology. Last but not least, the design should not exceed power consumption, which would prevented circuit from using in low power devices and power peaks should not jam other communication on or outside of chip.

5.1 Discharging capacity

Proposed buffers circuits should be capable of driving relatively big capacitive load Cl = 400 pF. Because buffer is open-drain, the transition from LOW to HIGH is secured by chosen resistor or current source by customer. This will have minimal effect on HIGH to LOW transition.

Design of buffer has to obey specification, thus HIGH to LOW transition (fall time) should fall in certain range. Therefore the charge stored from capacitor have to be sink through NMOS to the ground in defined time.

Size of this current can be taken from capacitor equation

$$I_{Dn} = -C_{load}\frac{dV_{out}}{dt} \tag{5.1}$$

Initial conditions will be Vout=Vdd, therefore when the capacitor started discharging the transistor will be in saturation region and discharging will be fast. After the voltage on capacitor drops down to Vds = Vdd - Vtn, transistor will enter the triode region. Thus resistivity of the channel will rise, therefore

current will be smaller and discharging will slow down. Transition is shown in Figure 5.1

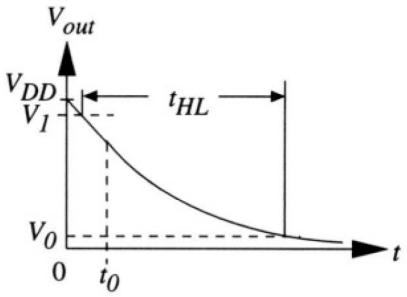


Figure 5.1: Output voltage on capacitor during fall time [6]

Time t_0 when this transition will happen can be found using equation

$$t_0 = \frac{2 \cdot C_{load} \cdot V_{Tn}}{K_P \cdot \frac{W}{L} (V_{DD} - V_{TN})} \tag{5.2}$$

The fall time can be calculated as

$$t_{HL} = s_n \cdot \tau_n \tag{5.3}$$

where time constant is.

$$\tau_n = \frac{C_{load}}{K_p \cdot \frac{W}{L} (V_{DD} - V_{Tn})} \tag{5.4}$$

s_n is scaling multiplier which consist from two parts, first represents time when NMOS is saturated and second when NMOS is in triode region

$$s_n = \frac{2 (V_{Tn} - V_0)}{V_{DD} - V_{Tn}} + ln \left(\frac{2 (V_{DD} - V_{Tn})}{V_0} - 1 \right) \tag{5.5}$$

Also thanks to defining the time constant, it can be written that $\tau_n = R_n C_{load}$ where

$$R_n = \frac{1}{K_p \cdot \frac{W}{L} (V_{DD} - V_{Tn})} \tag{5.6}$$

And use R_n which expect that transistor behaves as linear resistor through all control voltage. This is useful for hand calculations and approximation. It is necessary to kept in mind that mosfet is non-linear device and approximation have to be verified with simulations.

The whole procedure how to derive these equations can be found in [6]

5.2 Area

Although certain variables in our circuit cannot be modified, for example with size of output transistor, because it is pretty much selected with amount of output current and maximum output level of LOW voltage. But still there is some space left for optimization on our shoulders. Circuit can be modified in such a manner to aim for minimization of other part of topology. Therefore minimize amount of components, their size and try to select simple and straight forward solution. Ideally with small amount of passive components, which are covering a lot of area and also for CMOS process don't have very precise value. Also this aspect have to be kept in mind, while designing structures helping to bring PVT robustness of the circuit.

5.3 Power consumption and current peaks

This kind of circuit is meant without exception for mobile devices. Therefore aspect of power consumption cannot be omit. Which will dramatically influence the size of the battery or prolong the life on one charge. Consumption is mostly defined by type of bus. For I^2C bus the buffer is open drain. Thus in Logic HIGH, the bus in connected through resistor or current source to the V_{DD}. But in case of logical zero there is constant current going through output transistor or current pull down source.

Therefore main power consumption saving is done by usage of bus, in case of I^2C. When the bus is idle, it is in logical HIGH. So only when transmitting data the power is consumed. But also the amount of consumed power can be changed by sizing output transistor by minimizing the size, so the V_{OL} will be small as possible. Another option is minimize consumption of complementary circuits.

Consumed power is heavy related to the switching moment, when the output transistor change the state from close to open. Today transistors are for this bus even to fast. In the moment of switch, the amount of current going through the component would cause interruption on other buses or wire on the chip. Therefore it has to be ensured that maximum value of current was lowered and execution of this transition is as slow as possible to achieve nicely shape current curve.

All these aspect have to be taken in a count, few years ago was crucial for us to go as fast as possible, now the problem is opposite. The circuit has to be slowed down to obey specification, but still be able to charge big capacitive load. This all should be done with minimal area and small power consumption, so today portable devices will last longer. To not interfere with another communication, which can run simultaneously with us. Current function going through our circuit have to be shaped, because with today transistors the transitions can happen even to fast for us and with large current magnitude.

Chapter 6

Analysis and comparison of existing solutions

Several patented solutions that are suitable for application of adjusting the signal slope for the bus communication, have been presented. These circuits were usually made with different technology and were supposed to solve slightly different problems. Patents consist of a topology, short function description and simulations. Thus changes have to be made, to execute same function in 180 nm process technology GPDK180. Mainly because circuits are designed for different currents and delays, therefore a new sizing of components is needed.

Main complication is that in older processes the transistors are switching slower, while to abide same function with new technologies there was a need to slow down function of the circuit to fulfill the specifications. Second issue which had to be addressed was the wide range of operating conditions. Most of the topologies were formed to charge and discharge much smaller capacitance and also possible capacitance range was smaller. The nominal voltage of circuits were usually greater than 2.4V. Most of the topologies were expected to work under fluctuating voltage, but weren't designed to work under several different supply voltages (in this case from 1.2 V to 3.6 V).

6.1 Different approaches of controlling slew rate

There are numerous solutions for controlling a slew rate out there through patents and scientific papers. A closer look shows that it can be reduced to several approaches. However, each of them are solving the same problem from a different perspective. Problem is solved with more or less success depending on the aim of the topology. One solution can work well with a large spectrum of load, another with high changes of voltage and last one with process and temperature changes. It is not usual to have a circuit which incorporates robustness from all of this at the same time. Most common approaches will

be mentioned in next paragraphs.

6.1.1 Low pass filter

Low pass filter formed in front of output transistor is the most straight forward approach.[7] Simplified scheme can be seen in Figure 6.1. Low pass filter is modeled with a capacitor and a resistor. Depending on required values of components, it can lead to big area. As a compensation for this, better robustness from process and temperature variation is obtained. In this case, slope of controlling signal will stay the same for every voltage and capacitance. With precisely selected value of the filter as well as the slope, such a buffer can control wide spectrum of capacitance. Problem can arise with a change of the voltage. Higher voltage can be advantage for some applications, because transitions happen much faster in such a case. The output transistor will conduct more current, therefore the capacitor will discharge faster with high supply voltage. For operation, where minimum and maximum time of the transition is defined, this it is unfortunately unacceptable. To meet the specification with this method, it is fundamental to sens supply voltage and to implement a feedback mechanism.

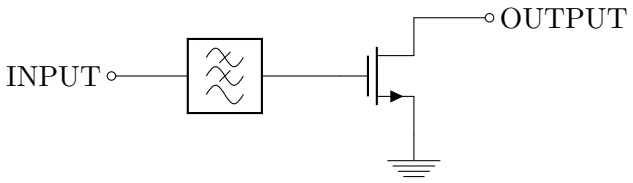


Figure 6.1: Low pass filter

6.1.2 Delay elements

Another approach is to use delay elements. The input signal can be delayed and used as a control signal. Delay elements can be realized in a different manner, for example as transfer gates[8], skewed inverters[9], Schmitt triggers and so on and so forth. Delaying itself does not give us any advantage. The output would have same slope, only shifted in confer to the delay. Using branching of input signal give us a bigger area for maneuvers. More output transistors can be implemented. These transistors can be controlled by several controlling signals in different time. Branching is shown in Figure 6.2. Output slope can be changed by adding more output transistors of various sizes controlled by different control signals. Sadly, attaining necessary time delay for this purpose is hardly reachable in 180nm technology. Lets take a transfer gate. Delay rely upon a propagation delay through PMOS and NMOS. The propagation delay through the transfer gate depends on width and length of used transistors. Therefore to obtain a high delay, the channel length have

to be enormous. Long transistors and branching is area expensive. Another problem is generated delay. In case of using transistors, delay cannot reach big values. Lastly, this topology is hardly load independent.

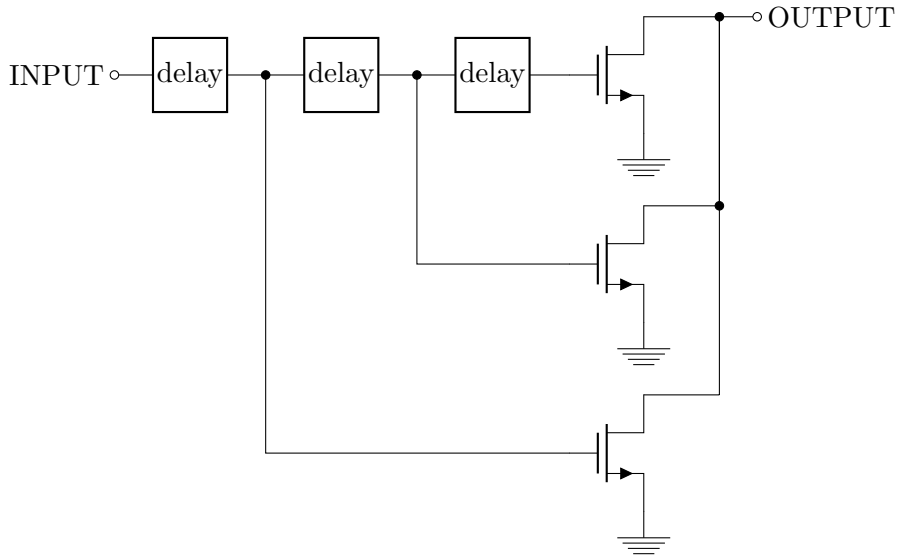


Figure 6.2: Delay elements

6.1.3 Limiting current

A gate of the output transistor form a capacitor. The capacitance of the gate depends on a silicon oxid and a size of the gate. In a case of the output transistor, capacitance can be in the order of hundreds of femto Farads. This transistor can be driven by limiting the current that is loading the gate capacitance[10], [11]. Simplified scheme can be seen in Figure 6.3.

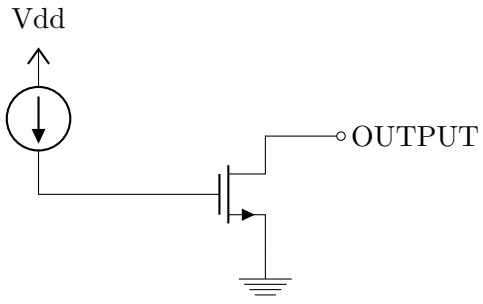


Figure 6.3: Limiting current

When mentioned example is taken in a consideration (C_L= 100 fF) it leads to a current around 1μA. Generating this current is inconvenient.First, it is not possible to achieve this value by simple circuit, if current should stay constant

over changing voltage. Second, generating current will cause an enlargement of a power consumption. Even in a case of current 1μA this can be central, specially when taking into account that a leakage caused by a transistor can be in order of nano ampers or even pico ampers. To lower power consumption the current source has to be switched on only during part of the period. Current sources need time to settle, thus this is not also recommended option.

6.1.4 Voltage biasing

A drain current of the mosfet transistor is set by gm and V_{GS}. The only possible path how a current from the capacitor can be sunk to the ground is through the output transistor. Thus by tuning V_{GS}, maximum sinking current can be chosen. This is shown in Figure 6.4. Problem is how to set the voltage to constant value with changing supply voltage. Using resistor divider will result in the different bias voltage with the different supply voltage. Reliable solution can be to derive this voltage from the transistor threshold voltage. Required voltage can be also clamped from different part of the circuit. [12] Another option could be setting this voltage with on resistance of transistor like in [13]. With relatively stable biasing, reliable current can be obtained and so the slew rate. Disadvantage of this approach can probably be observed already. When lowering the supply voltage drain source voltage will also go down. Operation on voltage close to threshold voltage current will be much smaller. Thus this approach can be used only for voltages higher that 2V, depending on settings.

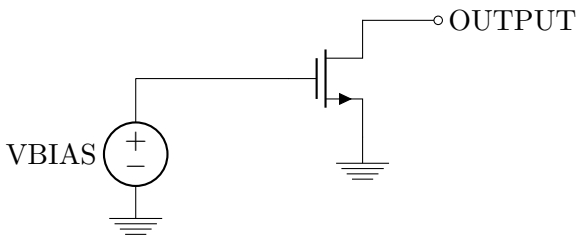


Figure 6.4: Voltage biasing

As can be observed, these techniques can be used for adjusting slope rate. Depending on requirements, each technique can be satisfactory to some degree. Working in a wider range of voltage and capacitive load is a problem. Setting the slope with a low pass filter can fulfill the criteria for a wide range of capacitive load. Depending on a good sizing, the range of capacitance can be quite tremendous. A complication can arise with a change of voltage. When the voltage is reduced, the output current will change and so the slope. This calls for a feedback mechanism. As it was already mentioned above, the heaviest influence on the slope has the supply voltage and the capacitive load. To eliminate this, a feedback path can be added to the circuit. The

feedback mechanism can introduce a big complexity into the circuit. Hence it is important to use the simplest mechanism.

6.2 Sensing conditions and feedback

All previously mentioned approaches have a certain dependency. Working with voltage which can thrice in a value and capacitance that can change in two orders, it is almost inevitable to adjust the function with compliance of working conditions. Art of sensing capacitance and voltage will be presented in next paragraphs.

6.2.1 Sensing voltage

With the higher supply voltage, currents in the circuits are higher, and so the control signals are faster. Therefore a fall time is faster. On contrary when the voltage is reduced, currents are smaller, transitions slower and fall time slower. Hence a voltage sensing is desirable.

First, the fall time is set for one corner. For example for the lowest voltage 1.2V. Now a component with inverse function to the voltage have to be found, which will compensate an influence of the voltage change. Components with a negative resistivity are not usually part of CMOS technology. The negative resistance can be implemented by the circuit but this, again, introduces a complexity into a buffer design. It is also possible to use with advantage components or circuits with positive dependency on voltage. Using two paths with different functions, subtraction can results in another function, that can acquire high values for a small voltage and small values for a high voltage. Depending on a principle and how strong is the feedback, it is possible to make a fall time only slightly dependent or almost independent on a supply voltage.

A good example of a voltage feedback is shown in [7]. According to the voltage, the current through voltage divider is set. Dependency of the current is linear. At the same time the current can be sunk through PMOS shunt, which sinks more of the current with rising the higher voltage. This simple and nice mechanism is very effective.

6.2.2 Sensing capacitive load

When a slew rate is mentioned it is usual to mention at which loading capacitance. The reason is simple. An influence is enormous. With a higher capacitance more current have to be provided. Thus sensing and adding a feedback is convenient. One of the simplest ways is sensing a voltage function on the output. With a higher capacitance the output voltage will fall in a slower manner, and oppositely with a small capacitance the output will fall very fast. This solution is also shown in [7]. The output voltage is brought

on the gate of NMOS. When transition from HIGH to LOW is happening the NMOS is open. How long is the transistor open depends how long will be voltage on output higher than V_{TH}. When value of the capacitor will rise, transistor will be open longer, thus this transistor can sink more current from the control line.

Another option is to use a simple switch current cell [12]. Slew depends on the current and the capacitor. The load independence is obtained with controlling the output transistor with constant current generator. By sizing the internal capacitance and current source, the slew rate can be set independently on load capacitance. It is done by setting the gate voltage of output transistor. The gate is clamped to voltage which depends on a load capacitance. It works for feedback capacitance higher than capacitance of the output transistor. The output falls at the same rate as the feedback capacitor is charged. Limitation of this is that clamped gate voltage is always higher than V_{TH}. That is unfortunate because it is not possible to operate on lower voltages.

The last example also sens transition on output but does it in a more sophisticated way. The circuit is formed by a differential amplifier[14]. Where on positive output is connected internal capacitance, which is charged during logical HIGH on input. When circuit switch, the current from this capacitance is discharged through current sink. At the same time the output node is also discharging. Nodes are connected to the input of the differential amplifier. Therefore these two transitions, discharging output capacitance with high current and discharging small internal capacitance with small current are compared. When the output transition is faster, control current of output transistor is sinked to the ground, therefore the slope will adjust to the same discharging rate of the internal capacitor.

Approaches to control slew rate were mentioned. Low pass filtering, current limiting and multiple control paths are used most often. Main factors which can entail change of set slope were shown. Principles of sensing voltage, capacitance and ways of changing control signals taking them in account were demonstrated. In next the section concrete patents and papers will be taken and adjusted to fulfill the task.

6.3 Edge rate control for I²C bus applications

The patent US 2009/0066381 A1 should be usable for I²C bus and working in wide range of voltage. Method used in this patent is limiting the charging current with a resistor. Such a method should have a small static current dissipation. To be clear, this topology is just improvement of recommended circuit by NXP/Philips. It uses RC low pass filter, which shape the input signal before it reaches the output transistor. Only difference is that the characteristics of RC low pass filter is changing with a supply voltage. For higher supply voltage the part which is forming resistance in the low pass filter, behaves as resistor with higher resistance. Hence the cut off frequency is lower and the input signal is more adjusted. Oppositely, if the supply voltage is lower, resistance which is formed is lower, thus cut off frequency is higher and input signal is shaped only slightly. This signal is used to control output NMOS transistor. The result is that low pass filter work in a different manner for small and higher voltage. This function can be achieved with proper sizing of components.

The solution presented in the patent is working with a supply voltage in range between 2.3V and 5.5V. For loading capacitance 10 pF it exhibits fall time around 100 ns, which is calculated between supply voltage and zero voltage.

6.3.1 Schematic, components

As can be seen from Figure 6.5 this patented solutions use a voltage divider and two transistors to sink a current instead of one resistor, that is used in recommended solution for Fast mode by NXP.

Value of components used in this circuit are written in Table 6.1

Table 6.1: Components of Patent1

Component	Value
M1	20.8/0.35 μm
M2	8/0.35 μm
M3	2.6/0.35 μm
M4	1/0.35 μm
M5	80/0.35 μm
R1	3870 Ω
R2	11610 Ω
C1	1 pF

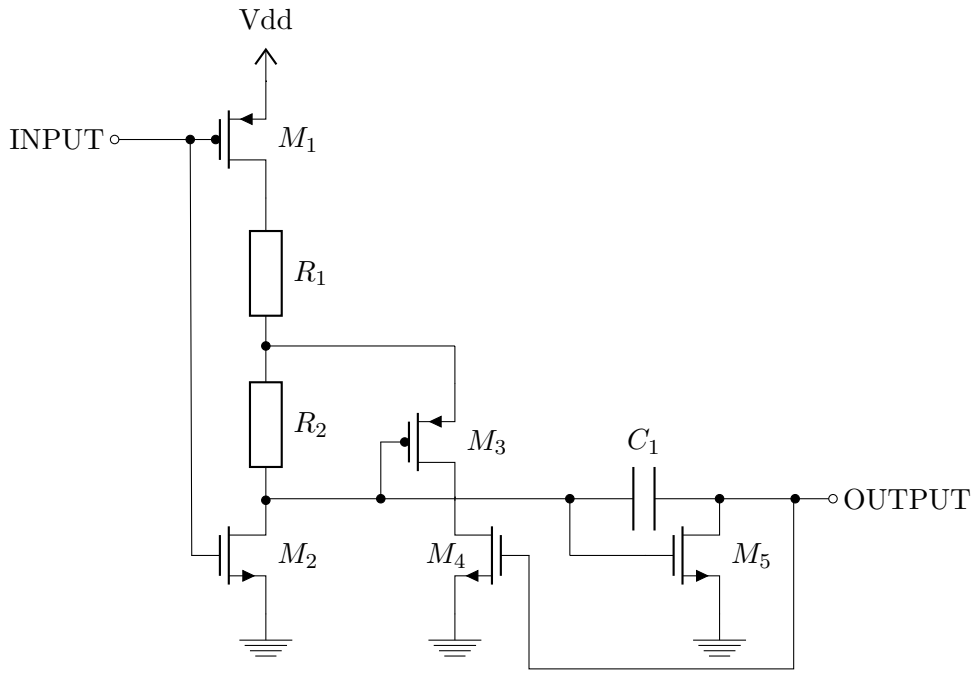


Figure 6.5: Patent US 2009/0066381 schematic [7]

6.3.2 Principle of function

During the transition from logical HIGH to LOW on the input, the transistor M4 is still open because of logical HIGH sensed from the output. This allows current go through transistors M3 and M4 to the ground through minimal resistance R_{on} of transistors M3 and M4. Amount of current going through the transistor M4 depends on ratio of width and length.

Maximum current that goes through resistors R1 and R2 can be adjusted. In case of total resistance R = 15480 Ω, current I_{max} is 232.5 μA for 3.6 V and I_{max} is 77.5 μA for 1.2 V. Now, when size of the transistor M4 is precisely set, it can be achieved that current of certain amount can be sinked to the ground. At high supply voltage V_{DD}= 3.6 V current I_D is 232.5 μA, oppositely at supply voltage V_{DD}= 1.2 V current I_D is 20.05 μA. This results in a current subtraction. For a higher voltage, the current is going only through the transistor and the voltage divider is virtually cutoff. On contrary at a low voltage, there is still small current going through resistor, I_r is 57.45 μA.

Briefly, the input part of the circuit is behaves like a variable resistor which is changes value of resistance from low to high with changing supply voltage. Resistance with capacitor C1 this circuits creates a low pass filter. C1 as Miller capacitance have value $C = (1 + A) \cdot C_0$. This low pass filter changes the cut off frequency with supply voltage. For higher voltage the low pass

filter will have cutoff frequency at lower frequencies that results in a smoother controlling of the output transistor M5.When voltage at output node is lower than the threshold voltage of M4, transistor will shut down, resulting that all current is going through R1, therefore the circuit is functioning as low pass filter with cutoff frequency $ft = 1/2\pi RC$.Thus for controlling slew rate it is desirable to open the transistor M4 for as long as possible.

6.3.3 Corner analysis

Corner analysis of this circuit was made. Minimum fall time of 11.2 ns occurred for skewed corner FS at temperature 95 °C, supply voltage 3.6V and 10 pF capacitor. Maximum fall time of 41.63 ns occurred for process SS at temperature 95 °C, supply voltage 1.2 V and 400 pF capacitor. Maximum values are for medium and high capacitor for each condition in the same corner. This is most likely caused by bigger regulation, which occurs with higher value of capacitor. The regulation circuit works when the transistor M4 is open. Time when the transistor M4 is open, depends on how long is on the output node voltage bigger that V_{TH}. Bigger capacitors take longer to discharge, hence with bigger capacitors the regulation circuit is connected for longer time period. It is interesting to see that at small supply voltage of 1.2V and medium size or big capacitor, extreme values are located even corners, such as SS and FF. On contrary, at high supply voltage of 3.6 V and medium size and big capacitor, extremes are in skewed corners.

Table 6.2: Corner simulations of US 2009/0066381

Process		FF	FS	SF	SS	FF	FS	SF	SS
Temp[°C]		-50	-50	-50	-50	95	95	95	95
V_{DD}[V]	C[pF]	C1	C2	C3	C4	C5	C6	C7	C8
1.2	10	12.77	12.79	18.44	**18.6**	12.76	**12.43**	17.62	17.71
1.2	100	**15.26**	15.33	23.03	23.28	15.95	16.06	23.59	**23.99**
1.2	400	**22.45**	22.56	35.57	35.74	26.08	26.14	41.53	**41.63**
3.6	10	12.22	11.26	**12.79**	11.9	12.03	**11.2**	12.64	11.91
3.6	100	13.13	**12.18**	14.05	13.06	13.52	12.65	**14.75**	13.84
3.6	400	16.5	**15.61**	18.07	17.17	18.86	18.07	**21.43**	20.57

Explanation of this could be that at small voltages, on-resistance of the transistor M1 have significant influence on amount of the current going to the voltage divider. Change of the total current with process is more significant that impact on subtraction caused by the transistor M3. That is why extreme values for bigger capacitor are in corners SS and FF for the small supply voltage. On contrary to that, at the highest voltage, on-resistance of

the transistor M1 is many times smaller than in previous case, thus changes doesn't have a big impact. Now, when regulation circuit is on and PMOS M3 is SLOW, more current is going to the resistor R2 and control the gate of the output transistor, thus fall time is faster. Same for the slowest case at the highest voltage. When PMOS M3 is FAST it sink more current to the ground and the output transistor is opened more slowly. This is the reason why extreme values of fall time for bigger capacitor are in skewed corners SF and FS for the highest supply voltage. Results of corner analysis are shown in Table 6.2. Green color indicates the shortest fall time under certain operating conditions. Red color indicates the slowest fall time.

6.3.4 Area

The only draw back is that this topology is using relatively big values of components and as a result it covers a big area on a chip. Area of this circuit can be seen in Table 6.3

Table 6.3: Area of Patent1

Components	Area$[\mu m^2]$
Transistors	39.34
Capacitors	125.00
Resistors	26.33
Total	**190.67**

6.4 Transceiver driver with programmable edge rate control independent of fabrication process, supply voltage, and temperature

The patent US 6670822 B2 should be usable as a general driver which should work despite of change of a supply voltage and a temperature. Here the capacitors are used to provide turn-off potential of output transistor. This can be done in a highly programmable way. Also certain value of a gate voltage is brought to transistor, which limits the current going to gate of output the transistor.

6.4.1 Schematic, components

The circuit consist of series of three inverters which are gradually bigger. Capacitors coupled to transistors regulate the maximum control current. The

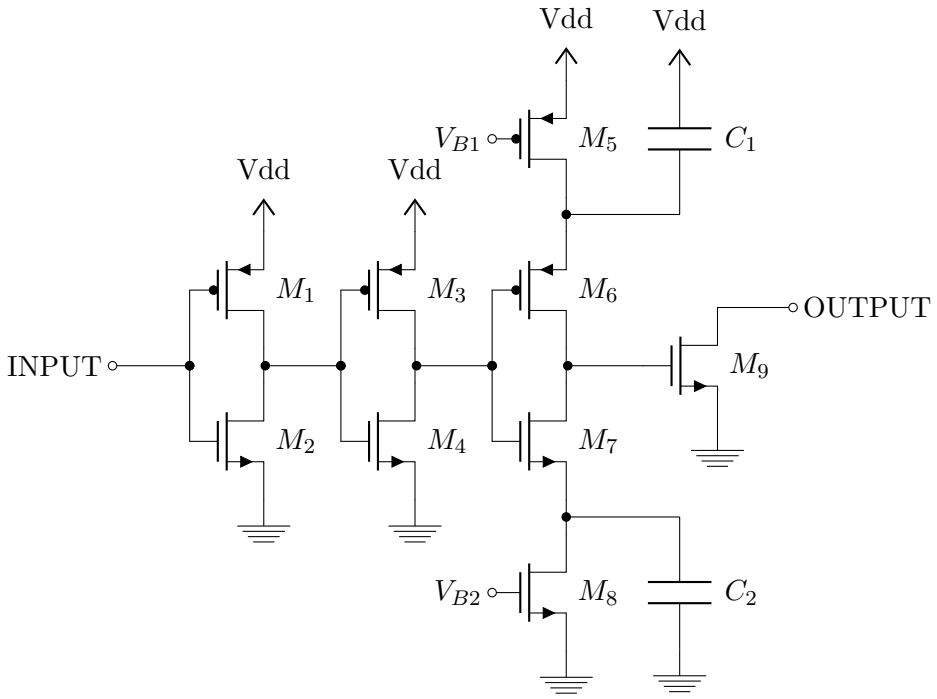


Figure 6.6: Patent US 6670822 schematic [15]

final stage is formed from one output transistor. Schematic is shown in Figure 6.6

Value of components used in this circuit are written in Table 6.4

Table 6.4: Components of Patent2

Component	Value
M1	1.1/0.35 μm
M2	0.42/0.35 μm
M3	5.2/0.35 μm
M4	2/0.35 μm
M5	1.1/0.35 μm
M6	14.3/0.35 μm
M7	5.5/0.35 μm
M8	0.42/0.35 μm
M9	45/0.35 μm
C1, C2	50 fF

6.4.2 Principle of function

During a transition from logical HIGH to LOW, the capacitor C1 charge gate of output transistor M9. By selecting good value of capacitance amount of stored electric charge can be regulated.

Second important thing for this topology is to apply the right gate voltage to the transistor M5, so it will work at triode region. It is necessary to secure that bias voltage (V_{B1}) will be a few millivolts bigger than threshold voltage.

This is very difficult to secure, because threshold voltage is highly dependent on a temperature. It can be done by connection another PMOS as diode. After current is specify by diode connected transistor. Defined voltage between drain and source will be obtained and therefore defined voltage on gate of M5 will be also set. This generated bias is dependent on temperature in a same manner as threshold voltage of PM5.

Now the problem is to generate current of precise value. To fulfill the specification of fall time between 10 ns and 80 ns, current sink have to be 1 μA. Current sink has to generate current with a small variation between 0.997 μA and 1.153 μA. Therefore it has to be decided, if current sink with defined amount of current and in this precision can be secured.

With this topology it is possible to change the rise time with the same approach. Only difference is that for regulating rise time, the biasing voltage has to be brought to the node V_{B2}.

6.4.3 Corner analysis

After sweeping through all process corners, temperature, supply voltage and supply capacitance it can be observed, that minimum and maximum values of fall time are equally distributed between even and skewed corners. Following circuit fulfills the specification, which is shown in Table 6.5. Green color indicates the shortest fall time under certain operating conditions. Red color indicates the slowest fall time.

The most interesting is that this buffer exhibits different voltage dependency than rest of tested buffers. For example, in corner SS at 95°C with load capacitor 400 pF, it would be normal to expect that with the higher voltage, fall time will be shorter. Result is exact opposite, fall time = 65.55 ns and at 1.2 V and 79.83 at 3.6 V. Reason for this is the ideal current source, control current is generated without any dependency on the supply voltage. Thus output slope does not change with a voltage a lot. When the gradient of the transition is the same, fall time depends on the starting point(supply voltage). The shortest fall time of this buffer is 10.67 ns and the slowest fall time is 79.83 ns.

Table 6.5: Corner simulations of Patent US 6670822

Process		FF	FS	SF	SS	FF	FS	SF	SS
Temp[°C]		-50	-50	-50	-50	95	95	95	95
V_{DD}[V]	C[pF]	C1	C2	C3	C4	C5	C6	C7	C8
1.2	10	**17.71**	18.01	26	24.45	24.6	21.9	**33.91**	33.29
1.2	100	26.32	**23.74**	32.84	32.92	35.08	31.67	42.33	**42.77**
1.2	400	42.5	**40.45**	50.3	51.51	55.44	54.26	64.28	**65.55**
3.6	10	16.27	17.53	24.6	**26.56**	**10.67**	11.3	22.55	22.05
3.6	100	**27.81**	29.06	35.94	34.36	32.13	31.14	**45.5**	43.56
3.6	400	51.29	**50.13**	61.99	61.52	65.19	63.98	79.82	**79.83**

6.4.4 Area

The complexity of supply current is counterbalance with small area of this topology, as you can see in Table 6.6. The purpose was to show the principle not to design a current source. Most likely with a circuit for generation current or bias voltage, the final area would be much bigger.

Table 6.6: Area of Patent2

Components	Area[μm^2]
Transistors	**25.6**
Capacitors	**12.5**
Resistors	**0**
Total	**38.1**

6.5 Output buffer circuit

The patent US 6559676 B1 is suitable for an integrated circuit application, mainly because of a wide operation conditions. The output driver eliminates ringing due to overdrive and also power noise due to switching. This buffer incorporates a capacitance feedback to control the output slew rate and also to reduce the power noise. In a following section principle of function and a realization of such a driver in 180nm technology will be shown.

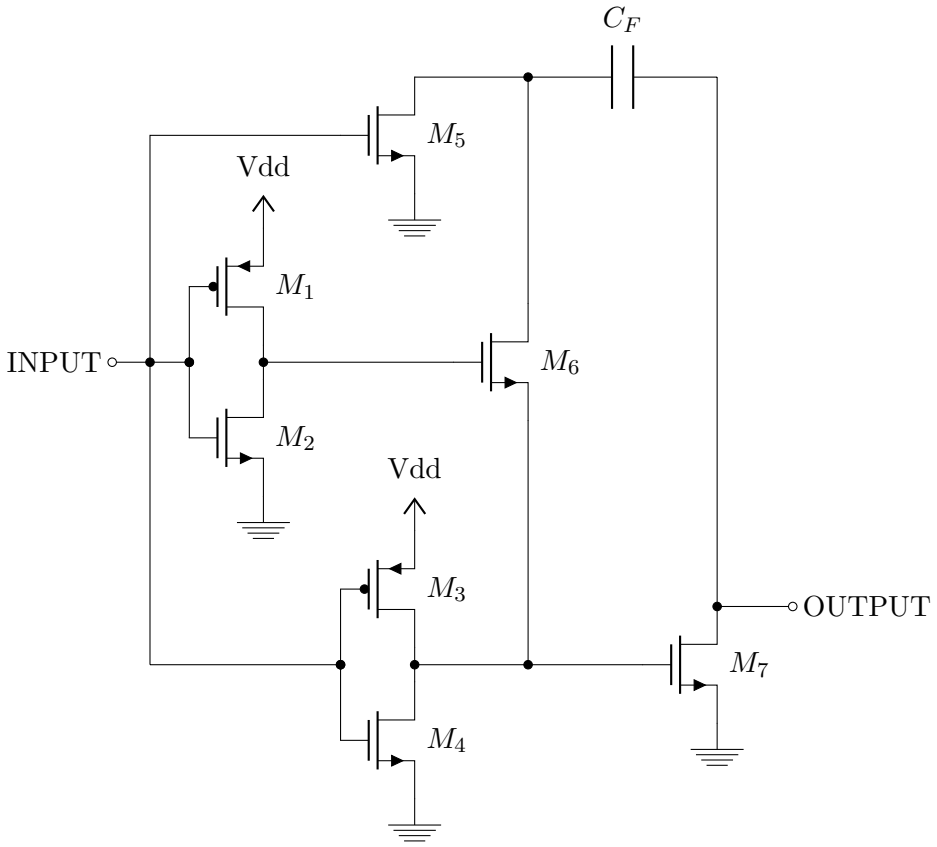


Figure 6.7: Patent US 6559676 schematic [12]

6.5.1 Schematic, components

The circuit consists of two inverters, two transistors used as a switch, capacitor and output stage is realized by one transistor. Full schematic is shown in Figure 6.7

Value of components used in this circuit are written in Table 6.7

6.5.2 Principle of function

As it was mentioned before, this circuit uses a capacitive feedback. This allows to work with a wide range of loading capacitance. A feedback circuit consists of the feedback capacitor C_F and PMOS M3. The output voltage decreases in a same manner as the feedback capacitor is charged. Taking the following equation

$$SR = \frac{dV_{out}}{dt} = \frac{I_D}{C_F} \tag{6.1}$$

Table 6.7: Components of Patent3

Component	Value
M1	0.84/0.35 μm
M2	0.42/0.35 μm
M3	1.6/0.35 μm
M4	0.42/0.35 μm
M5	0.42/0.35 μm
M6	0.42/0.35 μm
M7	57/0.35 μm
C1	1 pF

slope can be set by selecting C_F and I_D. A current I_D is the current sourced by PMOS M3. By doing this, the slope should be constant in a wide range of loading conditions, because initial biasing of output transistor is changing with dependency on capacitive load. For small load, for example 10 pF, step voltage is around threshold voltage of the transistor. This voltage is changing only slightly during a transition. This way, the transistor is limiting current that is sinked. On a contrary with a capacitive load around 400 pF the step voltage is bigger, output transistor is more open and sink current faster.

There are several criterias which have to be obeyed. First the C_F should be bigger than the gate capacitance of the output transistor, to obtain a correct step voltage. Inverters and switching transistor should be sized wider to limit short a circuit current. And lastly the C_F should be much smaller than capacitive load.

Unfortunately, problem lies in the threshold voltage. Even when this circuit is suitable for a wide range of capacitive load when it comes to voltage, problems with a low supply voltage will occur. For typical case, circuit is working till 1.2V, but taking the worst corner into account, minimum operating voltage is 1.5V. Problem lies in biasing. When step voltage is set to threshold and big capacitance is sensed at output node, step voltage doesn't have big room for change, because it is limited by supply voltage. By that output transistor sink less current and fall time rapidly rise.

At steady state this topology consumes only by leakage currents, I_{static}= 75.64 pA.

6.5.3 Corner analysis

Sweeping through all process corners, temperature, supply voltage and supply capacitance, corner simulation is obtained. Almost inclusively, all extreme values are located in even corners (SS and FF). Fall time is the slowest for every

condition in SS corner at 95 °C and the fastest for almost every condition in FF at -50 °C. This was expected, because with a rising temperature, the mobility of carriers in the channel are reduced. Thus amount of current through the channel is decreasing with a rising temperature. The shortest fall time of this buffer is 11.6 ns and the slowest fall time is 112.2 ns. Following circuit didn't fulfill the specification for the low voltage V_{DD}=1.2V and C_L > 100 pF, which is shown in Table 6.8. Green color indicates the shortest fall time under certain operating conditions. Red color indicates the slowest fall time.

Table 6.8: Corner simulations of Patent US 6559676

Process		FF	FS	SF	SS	FF	FS	SF	SS
Temp[°C]		-50	-50	-50	-50	95	95	95	95
V_{DD}[V]	C[pF]	C1	C2	C3	C4	C5	C6	C7	C8
1.2	10	**44.49**	52.12	56.27	67.26	51.47	59.33	62.58	**77.91**
1.2	100	**46.65**	54.39	60.59	71.84	52.93	63.06	69.24	**83.92**
1.2	400	**54.76**	63.4	81.29	92.44	66.74	75.85	96.23	**112.2**
3.6	10	**11.6**	11.63	12.28	12.62	13.45	14.36	14.29	**15.2**
3.6	100	11.37	**11.29**	11.72	11.7	13.7	14.42	14.68	**15.44**
3.6	400	**13.52**	13.87	15.59	16.06	19.27	20.13	22.53	**23.61**

6.5.4 Area

As can be seen in Table 6.9 main area is covered by a capacitor. On other hand no resistor was used , that save some chip area.

Table 6.9: Area of Patent3

Components	Area[μm^2]
Transistors	**23.1**
Capacitors	**125.9**
Resistors	**0**
Total	**148.1**

6.6 Comparison

First two topologies were most suitable for this application. Both of them fulfill the specification and they can work in a wide range of voltage end temperature.

The patent US 2009/0066381 A1 works well in the whole voltage range. The drawback of this circuit is use of capacitors and resistors, that covers big chip area 190.67 μm^2.

The patent US 6670822 uses smaller amount of passive components but it needs a current sink of specific amount, which has to be between 0.997 μA and 1.153 μA. This enlarge static a current dissipation drastically.

Last patent in comparison (US 6559676) used interesting technique of regulation of an output slope. The gate voltage of the output transistor was set to a certain value according to an output capacitance. To proper function, this regulation mechanism need a certain operating voltage. At lower voltages, a feedback mechanism isn't effective and control of an output slope is lost. This circuit fulfills specification only for the supply voltage > 1.5 V. Thus this circuit is not suitable for operation under the supply voltage, which can vary from 1.2 V to 3.6V.

To compare from point of view of static power consumption, static current was measured. The simulation was made at V_{DD} = 3.6V, T = 27°C and a typical process. Comparison of circuits is shown in Table 6.10. The area and the static current dissipation are written down for each circuit to get an overview.

Table 6.10: Comparison of Existing solutions

	Publication number	$Area[\mu m^2]$	I_{static}
P1	US 2009/0066381 A1	190.67	669 pA
P2	US 6670822 B2	37.7	1.0004 μA
P3	US 6559676 B1	148.1	75.64 pA

Chapter 7

Buffer design

Solution will be proposed build on knowledge gained from studying existing buffers. In following chapter the principle of the proposed buffer will be shown and described in detail. After principle, calculations and sizing of components will be explained. Characteristics of the final design will be displayed and commented. Finally, at the end of the chapter, results of corner analysis will be shown

7.1 Main principle

Seeing next to each other different approaches lead to better understanding advantages and down parts of all previous approaches. Getting acquainted in detail with the subject helped to propose the right way of solving this problem.

Solutions that is chosen is based on principle of delay elements and different propagation paths of control signal. Similarly as was mention in chapter 6.1.2

But there is a big difference in terms of application this principle in circuit. Circuit will be composed from three sinking paths. Three sinking paths, each realized by one NMOS transistor, with three different control signals. Two of them delayed and one input signal. First part should ensure that none of HIGH to LOW transition on output will not happen faster than 10 ns. Fall time 10 ns is limit of minimum fall time for minimal load capacitance from specification. Second part will be activated after approximately 10 ns and sink the leftover charge from the capacitor, that will happen in a such way that no transition will last longer than 80 ns and also minimize the LOW-level output voltage. Last but not least, third part will shape the transition in such a manner that function will be fluent, specially between first and last phase. This solution will be area-wise bigger or comparable to patent one. In terms of power consumption it should greatly suitable for portable devices. Schematic of the proposed buffer is shown in 7.1

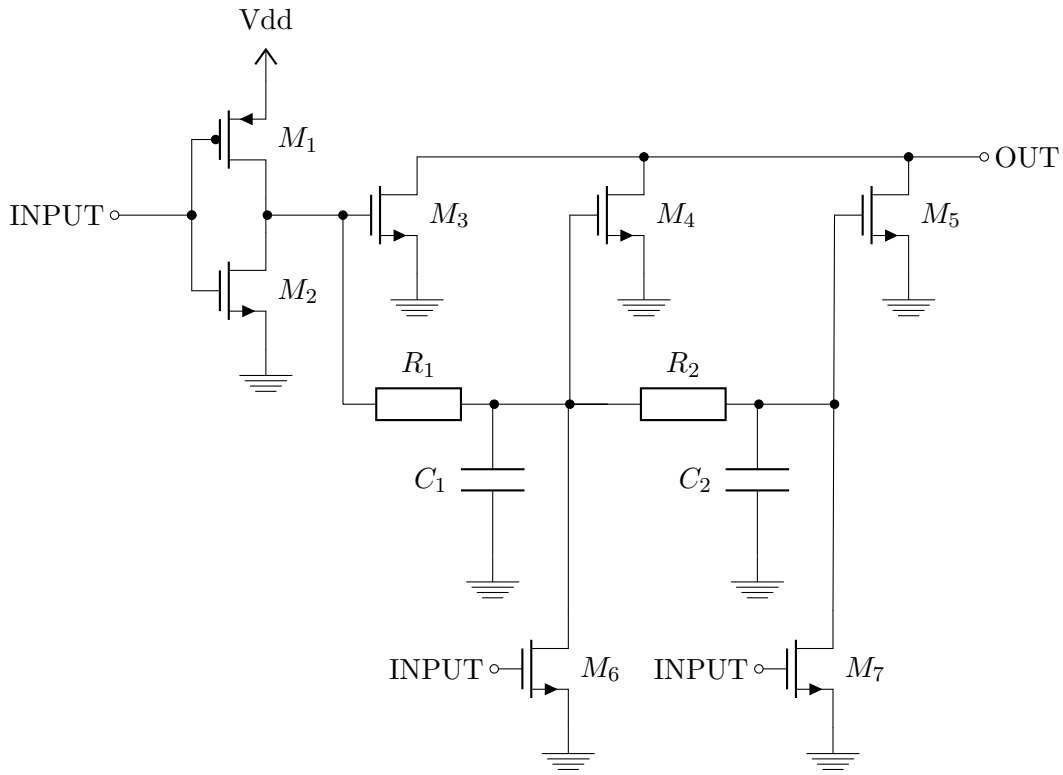


Figure 7.1: Schematic of the proposed buffer

7.2 Sizing the first transistor - A (M3)

Before entering any delay element control signal will be brought directly to the gate of A transistor. Transistor A will begin to open. Therefore through this transistor will start the current sinking to the ground from the capacitive load. This is the essential part. To limit current sinking in a way that the time of the transition will not overcome the minimum time from specification. And do so even for the fastest state. The fastest state will occur for the highest supply voltage (V_{DD} = 3.6V) and the lowest possible load capacitance (C_L = 10pF). Transition from 70% to 30% of supply voltage should not happen faster than in 10 ns. Corresponding current for these conditions can be found from following equation.

$$I_A = -C_{load}\frac{dV_{out}}{dt} \tag{7.1}$$

After putting values in equation, current of $I_A = 1.44mA$ is obtained.

$$I_A = 10 \cdot 10^{-12}.\frac{0.7 \cdot V_{DD} - 0.3 \cdot V_{DD}}{10 \cdot 10^{-9}} = \underline{\underline{1.44mA}} \tag{7.2}$$

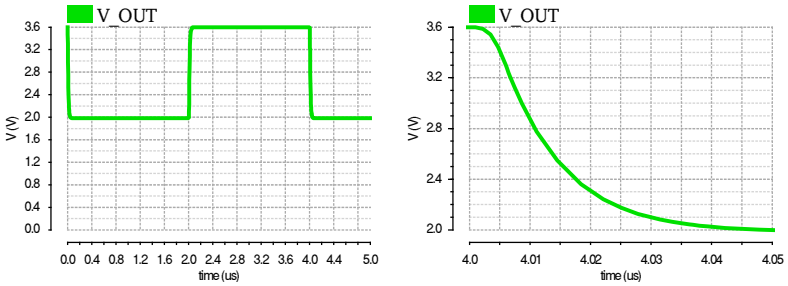
To acquire width of the transistor A for maximum current of 1.44 mA, equation for the drain current in saturation region can be modify.

$$I_A = \frac{k^{'}}{2}\left(\frac{W_A}{L_A}\right)(V_{GS} - V_{TH})^2 \tag{7.3}$$

Modify to the following form. After putting the with correct values in equation the width of transistor resulted in $0.54\mu m$.

$$W_A = \frac{2 \cdot I_A \cdot L_A}{k^{'}\left(V_{GS} - V_{TH}\right)^2} = \frac{2 \cdot 1.44 \cdot 350 \cdot 10^{-12}}{207.2 \cdot 10^{-6} \cdot 9} = \underline{\underline{0.54\mu m}} \tag{7.4}$$

Afterwards verification from simulation it can be seen calculated value is too small. Because transistor width of 0.54 μm leads to smaller maximum drain current, which is not sufficient. Thus correction is made according to gpdk180 models. Required drain current is obtained with width 1.72 μm, which can be rounded to 1.8 μm. Unfortunately because of the small drain current, transistor will have big channel resistance. The channel resistance together with pull-up resistor model a resistor divider, which allows the transistor to sink computed current from 3.6 V to 2.02 V. Output voltage limitation and detail of the HIGH to LOW transition can be observed in Figure 7.2



(a) $W_A = 1.8\mu m, L = 350nm$ (b) Detail of the transition

Figure 7.2: LOW-level output voltage for transistor A

Range of possible drain current in different corners can be seen in Table 7.1

Table 7.1: Sinking current through transistor A, corner simulations

Model Group, NMOS	S	F		T	F	S	F	S
Temperature [°C]	95	-50		27	-50	-50	95	95
	Min	Max						
$I_A[mA]$	**1.132**	**1.945**		1.484	1.945	1.602	1.410	1.132

7.3 Sizing the main output transistor - C (M5)

First, without worrying about fall time, it is necessary to set boundaries for size of an output transistor. To fulfill specification of High speed mode, V_{OL} has to be in accordance with Table 1.2. Therefore LOW- level output voltage should be always smaller that certain value to sustain readable output.

Because the bus is open drain, pull-up resistor is connected to the V_{DD}. During the discharging, output transistor is fully open and it is sinking all the current through conductive channel, that is form underneath the gate. Resistivity of this channel is not zero, it depends on physical dimensions of transistor, technological constants and V_{DD}. Thus this channel resistance form together with a pull-up resistor a voltage divider. Voltage drop across the channel depends on the ratio between value of resistor and value of channel resistance. To obtain small voltage drop, the pull-up resistor should have big value and resistance of the channel should be minimal.

The worst case occurs at minimum value of pull-ups for each supply voltage. From specification of LOW-level output voltage, maximum channel resistance can be calculated. Maximum resistance determined from divider equation. Results are shown in Table 7.2.

Table 7.2: Maximum channel resistivity(R_{ON}) of an output transistor

$V_{DD}[V]$	1.2	3.6
$R_P(min)[\Omega]$	320	1066.7
$V_{OL}[V]$	0.24	0.4
$R_{ON}(min)[\Omega]$	**80**	**133.3**

Keeping this value of resistance in mind, estimation of size of transistor can be made. Although the MOSFET is not a linear device, equivalent resistance can be define as [6]

$$R_{ON} = \frac{1}{k' \frac{W}{L} (V_{DD} - V_{TH})} \tag{7.5}$$

But only in case, that this equation will be taken just for estimation. It is crucial to validate results with simulations. From equation can be seen dependence between channel on resistance and width of transistor.

$$R_{ON} \propto \frac{1}{W} \tag{7.6}$$

Therefore can be observed that for lowering channel resistance width of transistor have to be bigger. Width can be obtained simply from modifying equa-

tion for equivalent resistance, that was mentioned before.

$$W = \frac{1}{k' \frac{R_{ON}}{L} (V_{DD} - V_{TH})} \tag{7.7}$$

For $V_{DD} = 1.2$V calculated width of the output transistor is $22.3\mu m$. For $V_{DD} = 3.6$ V calculated width of the output transistor is $2.6\mu m$. Thus it is obvious that value for the lowest voltage will be limiting in this case. Still these are expected values and they have to be verified with simulations, specially for sub-micron technologies. Calculated widths and results from simulations at nominal temperature of 27°C are compared in Table 7.3.

Table 7.3: Minimum width of an output transistor - C, Comparison between calculated and measured values

$V_{DD}[V]$	1.2	3.6
$W_{Calc}[\mu m]$	22.3	2.6
$W_{Meas}[\mu m]$	38.7	8.3

As can be observed, results from calculation are more optimistic. Measured and calculated widths are exactly on voltage limit, also the simulations were made for typical process and nominal temperature. It would be desirable to set the value bigger, to have adequate margin. Values of the transistor on resistance gathered from simulations at nominal temperature and typical corners can be seen in Table 7.4 and graph 7.3.

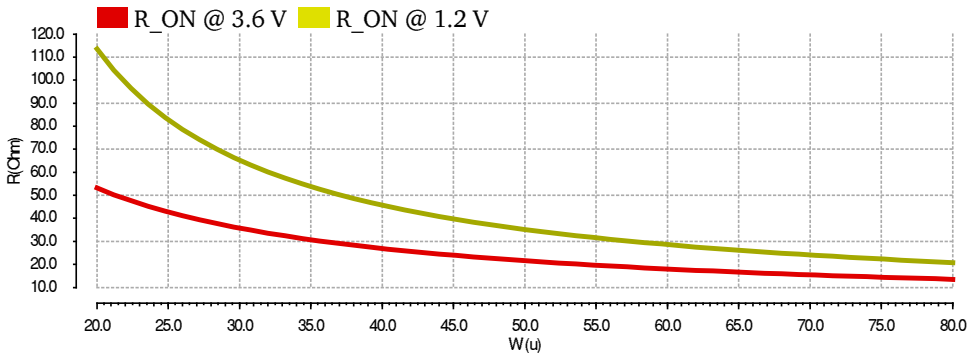


Figure 7.3: On channel resistance dependency on width of the transistor, L= 350nm

To be absolutely sure that V_{OL} will be in accordance with specification in every corner and no less important that power consumption will be minimized. Width of output transistor was determined W = 75 μm. This value according

Table 7.4: On channel resistance, L = 350nm, Temp = nom, Process= T

$W[\mu m]$	40	50	60	70	**75**	80
$R_{ON}[\Omega]$ @ Vdd = 1.2V	76.64	57.08	45.48	37.78	**34.84**	32.32
$R_{ON}[\Omega]$ @ Vdd = 3.6V	23.91	18.98	15.74	13.44	**12.53**	11.73

to simulations fulfill the specification for every corner with reasonable tolerance margin. Results for worst corner are V_{OL} = 177.7 mV for 1.2V and V_{OL} = 59.68 mV for 3.6V, both measured for highest temperature and SS corner. Value of V_{OL} through temperature and process corners is shown in Table 7.5 and Table 7.6

Table 7.5: LOW-level output voltage, corner simulation, V_{DD} = 1.2V, Rp= 320 Ω

Model Group NMOS	F	S		T	F	S	F	S
Temperature [°C]	-50	95		27	-50	-50	95	95
	Min	Max						
$V_{OL}[V]$	**70.92**	**177.7**		117.8	70.92	117.9	112.4	177.7

Table 7.6: LOW-level output voltage, corner simulation, V_{DD} = 3.6V, Rp= 1066 Ω

Model Group NMOS	F	S		T	F	S	F	S
Temperature [°C]	-50	95		27	-50	-50	95	95
	Min	Max						
$V_{OL}[V]$	**27.4**	**59.68**		41.82	27.4	31.56	50.06	59.68

7.4 Delay element

Idea behind proposed buffer is switching different sinking paths in different time. To create several controlling signals from one, the easiest option seems like delaying signal from input.

To gain desired delay, it is possible to incorporate CMOS delay elements. For example transfer gates, chain of inverters or some combination like transfer gate with Schmitt trigger. CMOS delay elements are suitable for small delays and they are generating delay with a straight edge. Two main requirements are expected from delay element for following use. First, delay of 10 ns and second, slow fluent voltage change (For fluent driving of the output transistor). As can be seen CMOS delay elements are not suitable, for this case. Much more usable is simple RC delay element. Down part is that for such a delay it can lead to a big area of components.

Value of components can be calculated from modification of the equation for voltage in the circuit.

$$V_{out} = V_{in} \cdot \left(1 - e^{\frac{-t_d}{R \cdot C}}\right) \tag{7.8}$$

$$\frac{V_{out}}{V_{in}} - 1 = e^{\frac{-t_d}{R \cdot C}} \tag{7.9}$$

Where V_{out} is required voltage on output. V_{in} is maximum voltage on input, t_d is delay and R is value of resistor and C is value of capacitor.

$$ln\left(-\frac{V_{out} - V_{in}}{V_{in}}\right) = \frac{-t_d}{R \cdot C} \tag{7.10}$$

$$t_d = -R \cdot C \cdot ln\left(-\frac{V_{out} - V_{in}}{V_{in}}\right) \tag{7.11}$$

When capacitor C is chosen, corresponding R for required delay can be calculated from:

$$R = \frac{t_d}{-C \cdot ln\left(-\frac{V_{out} - V_{in}}{V_{in}}\right)} \tag{7.12}$$

To cover all cases is important to keep in mind that value of resistor can change +/- 30 % with process and temperature. Thus to realize delay for the smallest temperature and the worst process corner. Time of delay has to be more than 70 % bigger than intended 10 ns.

Usually the delay is calculated as time between start time and time when output signal reaches half of the input voltage. Transistor used in this circuit have threshold voltage 0.6 V. Therefore transistors are starting to conduct current around this gate voltage. Thus in this case the delay is calculated as time difference between unity jump on input and 0.6 V on output. This leads to bigger component values but gives us an actual time of opening transistor.

It is important to mention that total capacitance forming the RC element does not consist only from one component. Because the RC delay element is connected do the gate of the output transistor C. Capacitance of the gate will also influence delay. In this particular case heavily. Output transistor C have huge size therefore big capacitance. This capacitance is parallel to capacitor in RC element. Total capacitance is sum of these two. Gate oxide capacitance Cox = 8.62 $fF/\mu m^2$, length L= 350nm and width W = 75 μm. Hence total area is 26.25 μm^2 and capacitance = 226.28 fF.

$$R = \frac{t_d}{-C \cdot ln\left(-\frac{V_{out}-V_{in}}{V_{in}}\right)} = \frac{10 \cdot 10^{-9}}{-C \cdot ln\left(-\frac{0.6-3.6}{3.6}\right)} = \frac{10 \cdot 10^{-9}}{-C \cdot ln\left(0.83\bar{3}\right)} = \frac{10 \cdot 10^{-9}}{C \cdot 0.1823} \tag{7.13}$$

To calculate value of resistor for 17 ns delay, capacitor of certain value can be chosen C = 403.2 pF(which is capacitance of 28μm x 14μm mimcap). $C_{total} = C + C_{nmos} = 403.2 + 226.275 = 629.48fF$ and put the values in the equation.

$$R = \frac{17 \cdot 10^{-9}}{629.48 \cdot 10^{-15} \cdot 0.1823} = 148.2k\Omega \tag{7.14}$$

Resistor value can be rounded to 150 kΩ

Original intention was to use capacitors that are formed from pmos by connecting source and drain together. Pmos is used because smaller speed of carriers. Capacitor created using pmos gate capacitance is called pmoscap. Value of such capacitor depends on width and length of the pmos transistor.

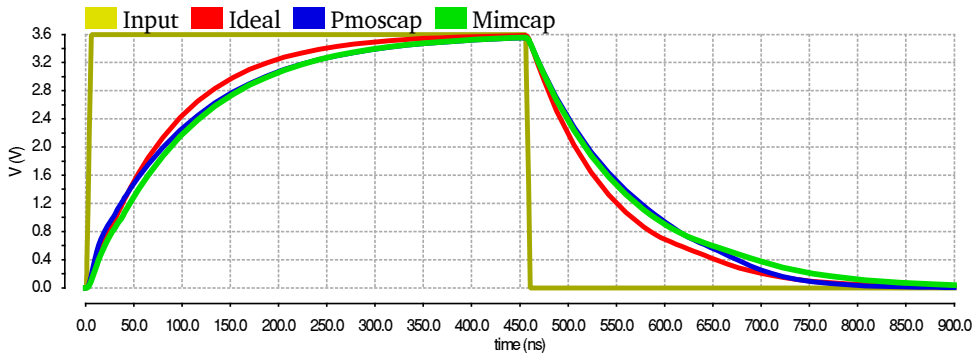


Figure 7.4: RC delay, R= 150 $k\Omega$, C= 403.2 fF, Temp = nom, Process= T

Studying behavior of pmos transistor it is obvious it is not suitable for such a use in RC delay elements. Especially when delay is calculated for small voltage. Here, around threshold voltage, capacitance of pmos is changing and by that also the characteristics of RC element. When voltage between pmos electrodes reaches threshold voltage, capacitance is getting smaller, hence the

delay is also smaller. Ensure the right value of delay on output, value of the capacitor have to be much bigger. That is not desirable.

In this case mimcapacitor is preferred, because around threshold voltage exhibits bigger capacitance than pmoscap and so the delay is bigger for smaller value of capacitor. Characteristics can be seen in Figure 7.4. Detail for small voltage is shown in Figure 7.5.

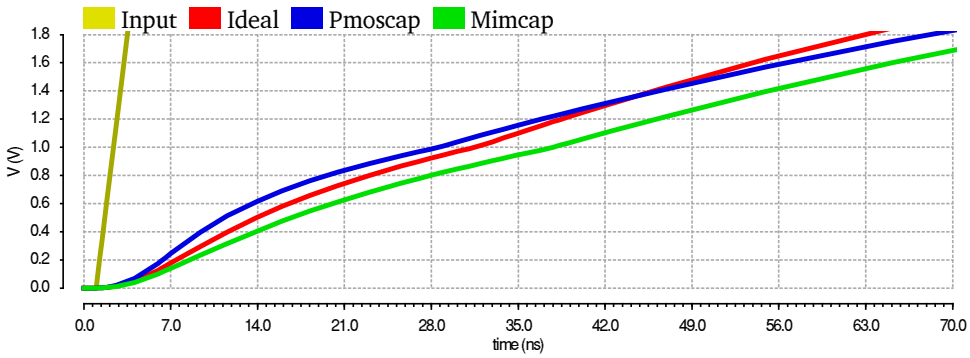


Figure 7.5: Detail of RC delay

Comparison of delay between unity jump on the input and 0.6V on the output can be seen in Table 7.7

Table 7.7: RC delay, R= 150 $k\Omega$, C= 403.2 fF, Temp = nom, Process= T

	delay [ns]		
Type of capacitor	cap	pmoscap	**mimcap**
$t_d[ns]$ @ Vdd = 1.2V	67,49	43,19	**54,28**
$t_d[ns]$ @ Vdd = 3.6V	20,05	13,58	**16,56**

7.5 Sizing the shaping output transistor - B (M4)

Building output buffer only from parts mentioned in previous sections would work well from two points of view. Fall time and LOW- level output voltage. Problem arise when closer look is taken on shape of the fall transition. There is a big differences between sizes of transistor A and C and so in the amount of current that each transistor can sink.

Thus in the fastest case ($V_{DD} = 3.6$, $C_L = 10$ pF) the current is sinked to the ground through transistor A with current approximately around 1.5 mA till delayed control signal reaches the gate of transistor C. When transistor C is fully open it can possibly sink 60 mA, which means it would sink the rest of the charged stored on load capacitor almost instantly. Thanks to continuous driving from RC element, this will not happen. The transistor does not open in one moment, but instead it is slowly opening, with slowly arising voltage on the gate. This is helpful and make the transition between sinking through transistor A and through combination of transistors A and C smother, but still when worst case occurs (process FF, temperature +95° C). The transistor A will be sinking current longer, but it reaches the limitation of an output voltage set by external pull-up and channel on-resistance. On-resistance will also rise, thus there can be time when current is not longer sinking and waiting for transistors C to open. Opening of the transistor C will take longer time in this case. Now can be observed that there is possibility that of emerging state when the gradient will be zero in one moment after it change to big value, right after transistor C will start sinking the current. This can create jumps on the slope.

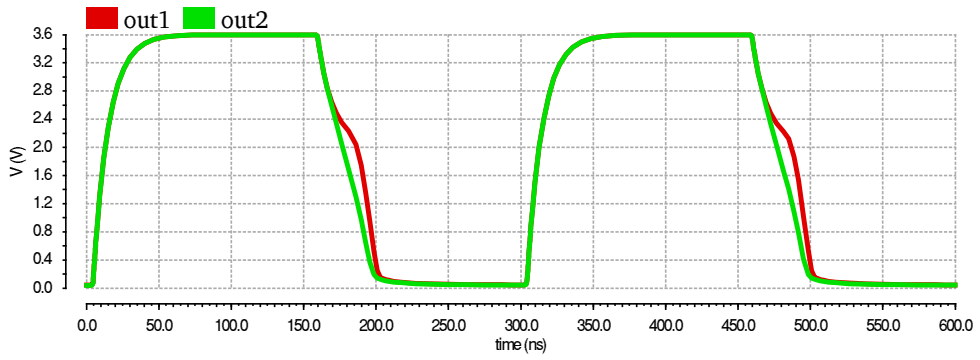


Figure 7.6: Shaping of an output signal with transistor B

To prevent this behavior from occurring. Another sinking part can be added to the circuit to bridge the difference between the previous two. And make both the slope and current function smoother for the fastest case. In different conditions, with rising capacitance and diminishing voltage will this improvement will not be almost noticeable. Of course it depends on the size

of the transistor and when the transistor B will be switch on in terms of delay between transistor A and transistor C.

Best results were archived with W = 6 μm. Transistor of this size is big enough to shape the transition. Delay element is split to two equal parts, thus transistor B is switch on after 8.5 ns. The transistor B will also speed up a little bit the whole transition, but thanks to the choosing delay components with a big margin, fall time will not go out from the specification.

Improvement of the output buffer signal can be seen in Figure 7.6. Where out1 is output from buffer which consist only transistors A and C. Opposite to that, out2 is output from buffer consisting transistors A, B and C. Simulation was made for T = 300 ns, V_{DD}, C= 10 pF.

7.6 Support structures

Previous in this chapter, main principle and necessary parts for proper function were mentioned. There are several additional circuits to improve functionality of the buffer.

Buffer consist of an inverter on the input. Width of PMOS and NMOS is 2 times bigger that minimal. This inverter is incorporated for several reasons. First to separate rest of the circuit. This way the RC elements is driven from the inverter and not from the input signal itself. Second, because inverter is bigger than minimal size it adjust signal to for big capacitive load. Because of this it causes smaller delay comparable in comparison with minimum size inverter. [16]

Maximum operating speed of I^2C bus in high speed mode is 3.4 Mbits. That correspond to T= 294 ns. RC element can be observed also as low pass filter. Low pass filter have certain cutoff frequency, at which the input signal is attenuate by half. In case of total R = 150 kΩ and C = 644 fF cutoff frequency can be calculated from following equation.

$$f_c = \frac{1}{2\pi RC} \tag{7.15}$$

In these settings it leads to $f_c = 1.65MHz$. At this point the control signals would never discharge all the way to the zero voltage. Also it is not necessary to regulate the control signal during logical one on input. Output transistors A, B, C are driven by control signal only during logical zero on input. Thus all the RC elements can be disconnected during logical one. This is realized by the two NMOS transistors. NMOS transistors are connected to the gate node of transistors B and C. They are controlled by the input signal. Immediately when input signal rise over threshold voltage, these transistors will open and sink all the charge stored on gates of the transistors, capacitors and do so by shorting the gates of the transistors B and C to the ground. Now transistors B and C are fully closed, thus output voltage can rise to the logical one. Both

transistors are identical, (width = 2 μm). During logical zero on input the transistor have big resistance and they don't influence rest of the circuit.

Final sizes of transistors of the proposed buffer are written in Table 7.8.

Table 7.8: Sizes of the circuit devices

Component	W [μm]	L [μm]
M1	2	0.35
M2	0.84	0.35
M3	1.8	0.35
M4	6	0.35
M5	75	0.35
M6	2	0.35
M7	2	0.35

Values and sizes of all passive components are written in Table 7.9.

Table 7.9: Sizes of the circuit passive components

Component	W [μm]	L [μm]	value
R1, R2	0.6	127.85	75kΩ
C1, C2	14	14	201pF

Total area of all components is shown in Table 7.10. As expected the biggest part of area is covered by capacitors.

Table 7.10: Area of components of the proposed buffer

Component	Area[μm^2]
Transistors	**31.37**
Capacitor	**392**
Resistors	**153.42**
Total	**576.79**

Layout of the buffer is shown in the appendix A.2. 4 times bigger width of metal was used for the output line ($W_{m1}1.6\mu m$). Each resistor was realized from 9 segments of polyhres connected together. This caused enlargement of the area because of the minimum distance between each segment. Capacitors were split for better area arrangement. Final layout has dimension 53.51μm x 22.8 μm and total area 1220 μm^2.

7.7 Characteristics of the proposed buffer

In this section, all important characteristics of the proposed buffer will be written down. Behavior under different conditions, such as supply voltage and loading capacitance, will be explained. Subsequently corner simulations will be shown.

7.7.1 Power consumption

Purpose of this buffer is an application in portable devices, hence power consumption is an important factor in decision. With smaller and smaller technology, static power dissipation starts to be as important as dynamic power consumption. In this circuit static power depends on transistor leakage current. I_{static} = 125.9 pA. During normal temperature and typical process. For temperature 95C, SLOW SLOW process corner and supply voltage 3.6V is static power dissipation ten times bigger than at nominal temperature. I_{static} = 1.1439 nA.

7.7.2 Fall time

In following section it will be shown how buffer fulfill fall time specification for different voltages and changing capacitance. Buffer aims for use in high speed mode, hence first will be shown the characteristics for fastest communication. As mention before, this was the main challenge. That because at the highest supply voltages and small capacitor values, transitions are happening much faster and need to be slow down.

Maximum operation speed of high speed buffer is 3.4 Mbits. Function of an output signal for V_{DD}=3.6 V and C_{load} = 10 pF is show in Figure 7.7

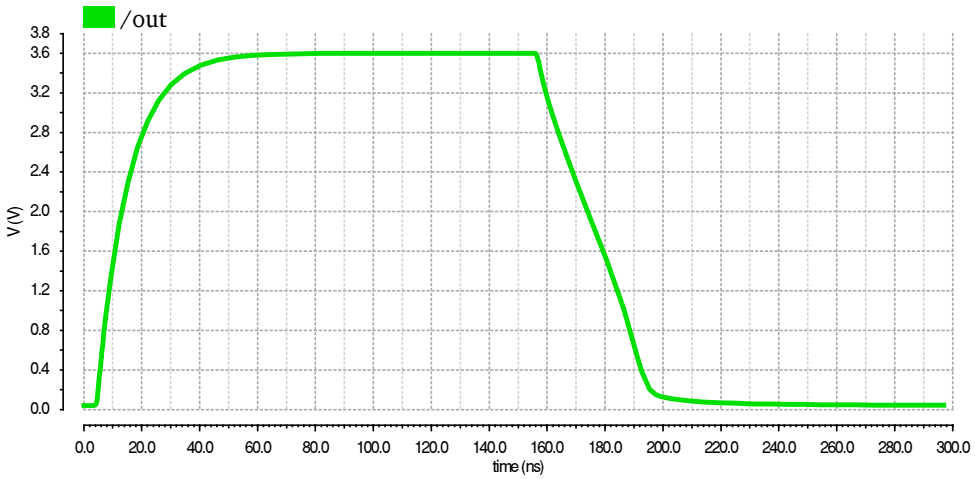
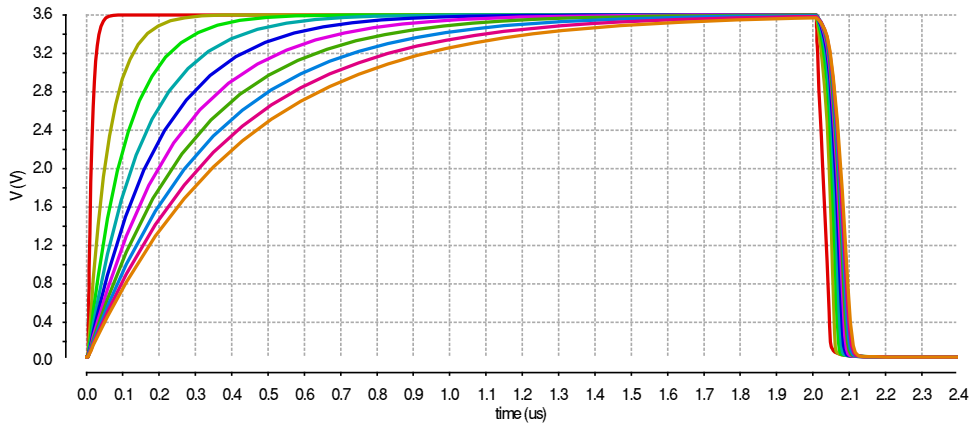


Figure 7.7: Output signal, Maximum frequency

The fastest fall time for V_{DD}=3.6 V and C_{load} = 10pF is t_{fall}= 18.36 ns. This value is in the range from specification. It is not possible to bring value more down. Even minimum of fall time from specification for this conditions is t_{fall}= 10 ns. Mainly because with process variation and operation under different temperature fall time would go out of specification. With this settings the buffer will function through all corners. That will be shown later in corner analysis.

For measuring fall time through all the possible values of load capacitor, the period was changed to 4 μs. That is because with shorter time the circuit would not charge all the way to the supply rail voltage. Especially with bigger value of load capacitor. Rise time is not limited by buffer. It depends on pull-up resistor or current source, thus it can be change by user, by connecting stronger power source.

How the fall time is changing with different value of load capacitor can be seen in the figure 7.8.



Because of big number of outputs, labels are not shown for clarity. Value of capacitor is changing from 10 pF to 400pF in 10 linear steps. Where red color represent the smallest capacitor (C_{load} = 10pF) and orange represents the biggest capacitor (C_{load} = 400pF).

Figure 7.8: Output signal with changing load capacitor, V_{DD}=3.6 V

Function of fall time in the whole range of possible load capacitance for V_{DD}=3.6 V can be seen in Figure 7.9.

Requirement from specification is that fall time between 100 pF and 400 pF have to be linearly interpolated. As can be observed from the figure, this criteria is fulfilled.

To see how different load capacitor influence the fall time and shape of the transition, detail of falling edge for selected values is shown in figure 7.10.

From graph can be observed that with rising load capacitor output signal exhibits rising delay, but the gradient of the transition change slowly. Values

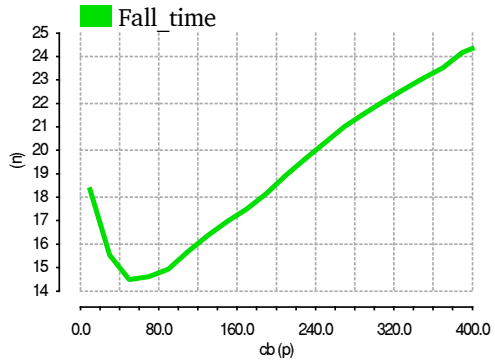


Figure 7.9: Function of fall time, V_{DD}=3.6 V

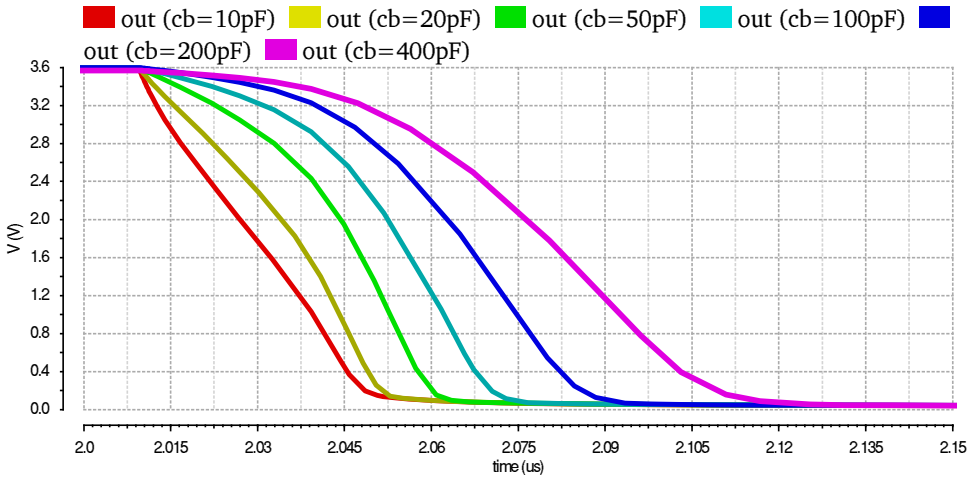


Figure 7.10: Detail of falling edge, V_{DD}=3.6 V

of the fall time for selected values are written in Table 7.11

To observe the influence of the supply voltage, results will be presented for 1.2V and 2.4V. Detail of falling edge is shown in Figure 7.11.

Again, for better overview, simulation is made for 6 selected value of capacitance. Dash line signals are for V_{DD}=2.4 V and solid line for V_{DD}=1.2 V. With smaller voltage the delay is rising and also it is noticeable that gradient of falling edge is more dependent on capacitance at the smallest supply voltage. But still it is in range from specification.

Function of the fall time can be seen in Figure 7.12. As can be noticed. For the smallest supply voltage, function of fall time is linear in the whole range. Also fall time at V_{DD}=1.2 V is more dependent on capacitance, compared to the fall time at V_{DD}=2.4 V.

Overview of fall time under different operating voltage and different capacitive load is shown in Table 7.12. Fall time for capacitive load in range from

Table 7.11: Fall time, V_{DD}=3.6 V

$C_{load}[pF]$	Fall time [ns]
10	18.32
20	16.90
50	14.48
100	15.27
200	18.59
400	24.34

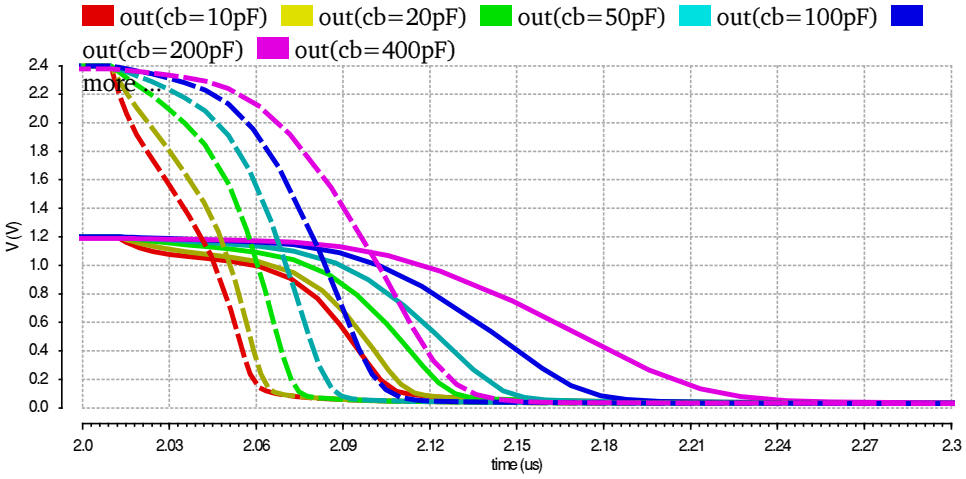


Figure 7.11: Detail of falling edge, V_{DD}=1.2 V, V_{DD}=2.4 V

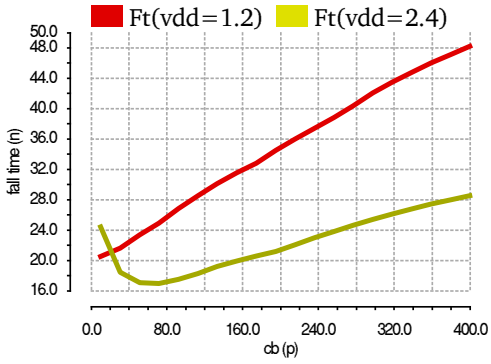


Figure 7.12: Function of fall time, V_{DD}=1.2 V, V_{DD}=2.4 V

10 pF and 100 pF is for all supply voltage in range between 14.48 ns and 27.48 ns. For the biggest capacitive load of 400 pF, fall time is between 24.34 ns

and 48.23 ns. Fall time is in accordance with specification.

Table 7.12: Fall time overview

$C_{load}[pF]$	Ft[ns], V_{DD}=1.2 V	Ft[ns], V_{DD}=2.4 V	Ft[ns], V_{DD}=3.6 V
10	20.54	24.41	18.32
20	20.92	20.75	16.90
50	23.28	17.14	14.48
100	27.49	17.66	15.27
200	34.87	21.37	18.59
400	48.23	28.53	24.34

To test if the buffer will function under any circumstances, corner analysis have to be made. Corners and values for corner simulation are written in Table 7.13.

Table 7.13: Corner parameters

Parameter	min	max
Supply voltage	1.2 V	3.6 V
Temperature	-50°C	95°C
Capacitance	10pF	400pF
Process	SS SF FS FF	
Resistor process	71k	83.4k

From corner analysis it is easy to observe that the fastest states occurs for a minimum temperature, a minimum resistor value and almost inclusively for an even process corner FF. Oppositely the slowest fall time occurs for a maximum temperature, maximum resistor value and process corner SS. Reason for this is the crucial influence on the fall time caused by delay elements. Thus at maximum temperature and maximum process corner of the resistor, value of the resistor will enlarge in total +30% from the nominal value. This will cause longer delay in the circuit and a different slope of the control signal. Response to that will be that output transistors B and C will start opening later in comparison to the nominal value of resistors and they will open at a slow pace. On the contrary, with a low temperature and a minimum process corner of resistor, the value of the resistor will drop by -30% from the nominal value. This will result in shortening the delay and faster opening of the output transistors. The only one PMOS is used in this circuit, as part of the input inverter, hence the uneven switching in the skewed corners have almost no

effect on the fall time. Specially when compared with impact of the resistor value change.

Results of full corner analysis are shown in Table 7.14. Green color indicates the shortest fall time under certain operating conditions. Red color indicates the slowest fall time.

Table 7.14: Corner analysis of the proposed buffer

C_b	P	T	V_{DD}	ft [ns]	R	C_b	P	T	V_{DD}	ft [ns]	R
10	FF	-50	1.2	14.89	min	10	FF	-50	1.2	18.82	max
10	FS	-50	1.2	14.15	min	10	FS	-50	1.2	16.94	max
10	SF	-50	1.2	14.69	min	10	SF	-50	1.2	17.71	max
10	SS	-50	1.2	15.01	min	10	SS	-50	1.2	17.78	max
10	FF	-50	3.6	10.08	min	10	FF	-50	3.6	12.04	max
10	FS	-50	3.6	10.66	min	10	FS	-50	3.6	12.9	max
10	SF	-50	3.6	12.28	min	10	SF	-50	3.6	15.29	max
10	SS	-50	3.6	12.75	min	10	SS	-50	3.6	15.78	max
400	FF	-50	1.2	30.94	min	400	FF	-50	1.2	34.86	max
400	FS	-50	1.2	33.89	min	400	FS	-50	1.2	37.33	max
400	SF	-50	1.2	41.91	min	400	SF	-50	1.2	45.72	max
400	SS	-50	1.2	45.82	min	400	SS	-50	1.2	49.94	max
400	FF	-50	3.6	16.81	min	400	FF	-50	3.6	18.93	max
400	FS	-50	3.6	17.46	min	400	FS	-50	3.6	19.65	max
400	SF	-50	3.6	18.45	min	400	SF	-50	3.6	20.55	max
400	SS	-50	3.6	19.08	min	400	SS	-50	3.6	21.12	max
10	FF	95	1.2	24.73	min	10	FF	95	1.2	30.05	max
10	FS	95	1.2	22.76	min	10	FS	95	1.2	28.69	max
10	SF	95	1.2	24.97	min	10	SF	95	1.2	29.44	max
10	SS	95	1.2	25.3	min	10	SS	95	1.2	30.62	max
10	FF	95	3.6	19.49	min	10	FF	95	3.6	24.79	max
10	FS	95	3.6	19.93	min	10	FS	95	3.6	25.38	max
10	SF	95	3.6	22.96	min	10	SF	95	3.6	29.38	max
10	SS	95	3.6	22.99	min	10	SS	95	3.6	29.53	max
400	FF	95	1.2	45.25	min	400	FF	95	1.2	51.4	max
400	FS	95	1.2	49.65	min	400	FS	95	1.2	55.2	max
400	SF	95	1.2	59.96	min	400	SF	95	1.2	65.65	max
400	SS	95	1.2	64.68	min	400	SS	95	1.2	70.93	max
400	FF	95	3.6	27.13	min	400	FF	95	3.6	30.23	max
400	FS	95	3.6	28.16	min	400	FS	95	3.6	31.35	max
400	SF	95	3.6	29.64	min	400	SF	95	3.6	33.13	max
400	SS	95	3.6	30.8	min	400	SS	95	3.6	34.38	max

Conclusion

Goal of this thesis was fulfilled. The new design of CMOS I^2C bus buffer for High speed mode in 180nm process has been presented and simulated in Cadence® Virtuoso. Slope control was archived with several controlling signals and multiple sinking paths.

Theoretical part consists of chapters about I^2C bus, high-speed mode, MOSFET, GPDK180 and process variations. Wide range of output buffers topologies were studied from patents and scientific papers. Different approaches and interesting techniques used for the slope control were explained and presented. Three most suitable circuits for this purpose were implemented in 180 nm process.

Circuits were compared in between in terms of a static power dissipation and an area. First circuit[7] fulfill the specification and it exhibits static current dissipation, $I_{static} = 669pA$. Second circuit from comparison[15] is area wise smaller 37.7 μm^2, but it needs an additional circuitry for the generating a stable current over a large operating range. Last compared circuit[12] is suitable only for $V_{DD} > 1.5V$.

The proposed buffer works for the wide supply voltage range from 1.2 V to 3.6 V and for the capacitive load between 10 pF and 400 pF. The circuit exhibits small static current dissipation, $I_{static} = 125.9pA$. The static current dissipation of this circuit is more than 5.3 times smaller in comparison to Edge rate control for I^2C bus application [7]. Fall time is in range between 18.23 ns and 48.23 ns for the nominal case and 10.08 ns and 70.93 ns for the worts case. Final layout has dimension 53.51μm x 22.8 μm and total area 1220 μm^2.

For future work, it could be interesting to find a mechanism to reduce delay at the low supply voltage by bypassing the delay element or by adjusting its characteristics.

This work shows an alternative approach of design of the output buffer. The buffer can be use with a great advantage in applications where power consumption is crucial and demands on area are not so strict.

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Appendix A

Schematic and layout of the proposed buffer

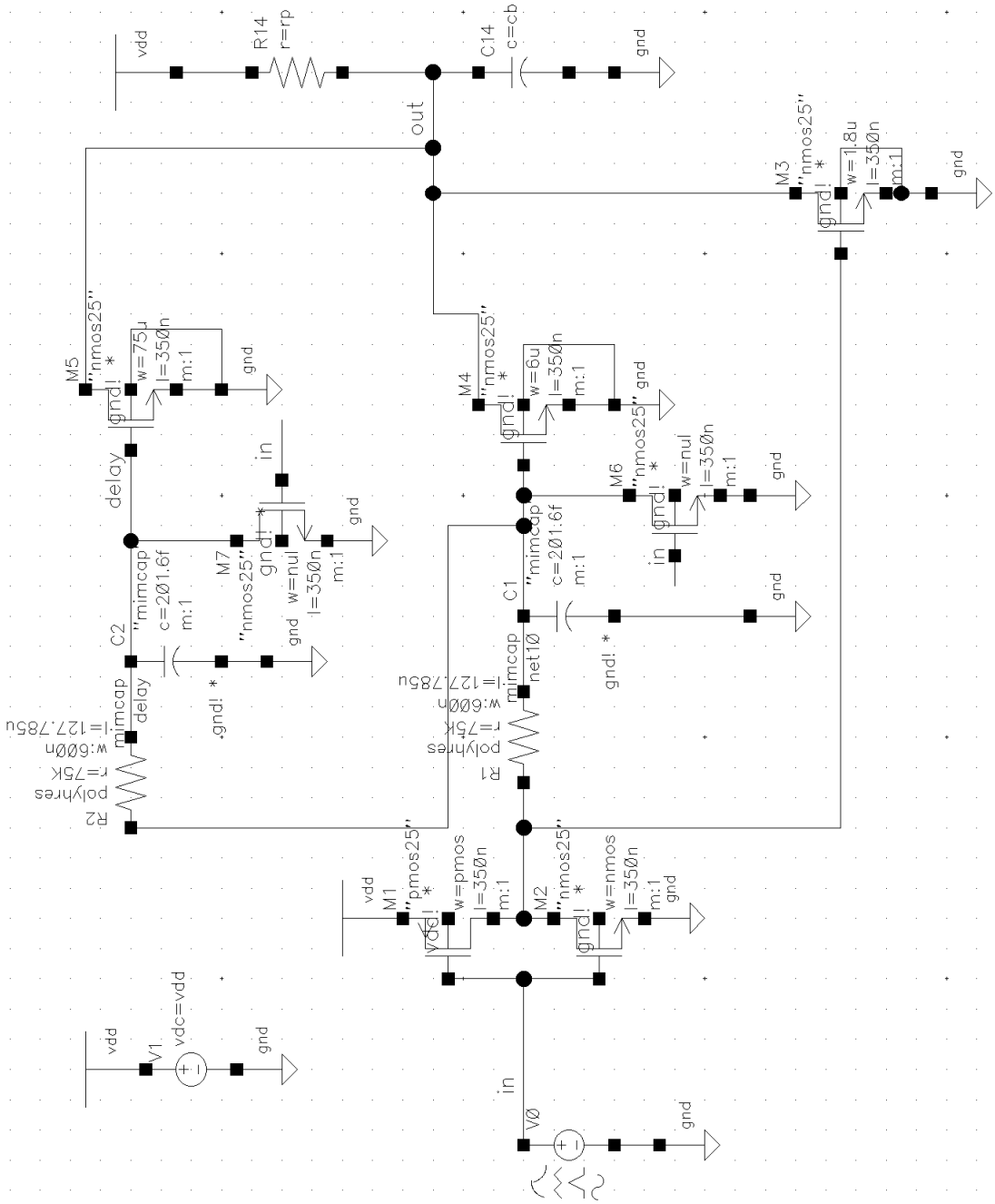

Figure A.1: Schematic of the proposed buffer

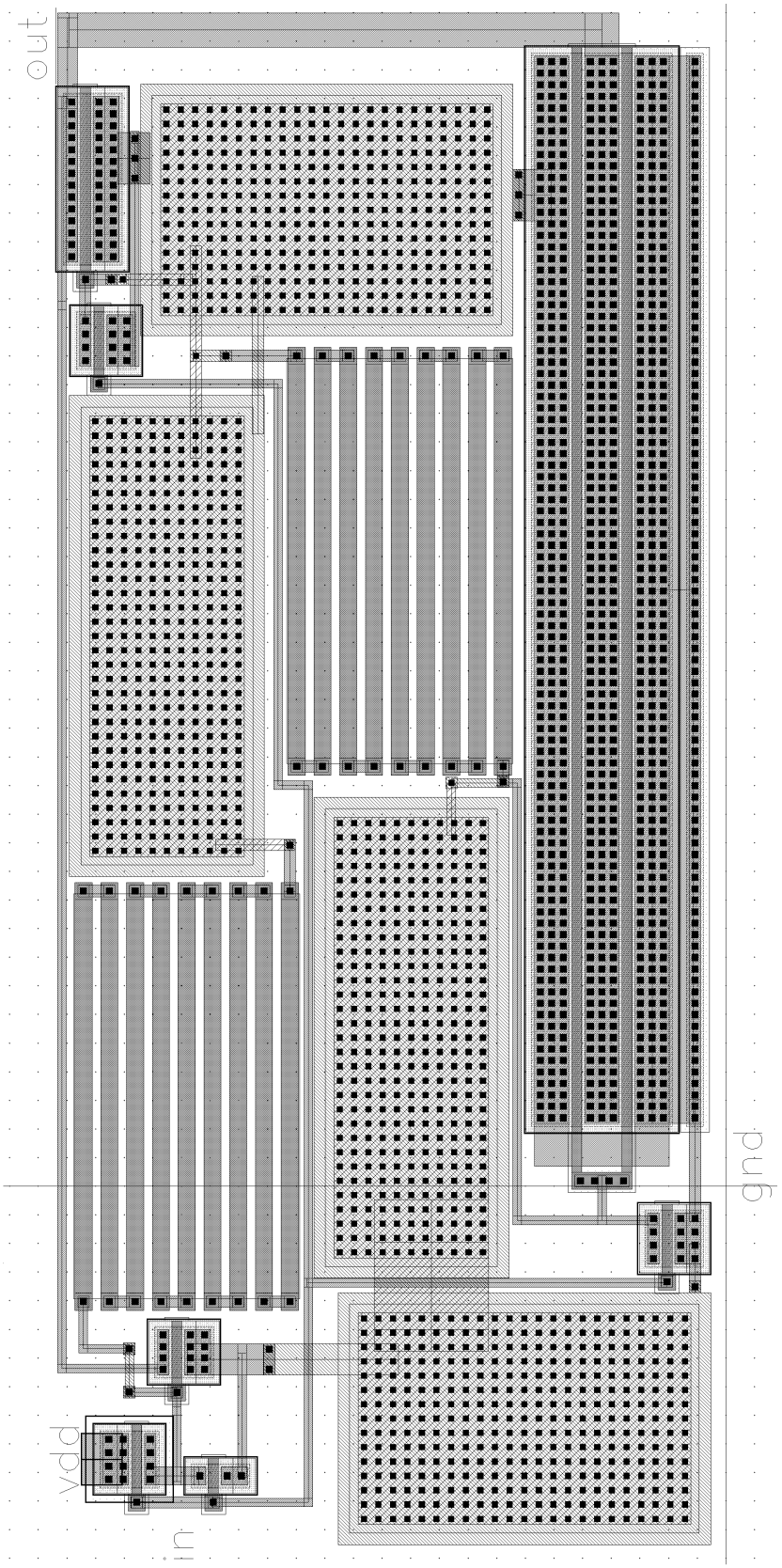

Figure A.2: Layout of the proposed buffer

Appendix B

Acronyms

BSIM Berkeley Short-channel IGFET Model

CMOS Complementary Metal-Oxide-Semiconductor

GPDK Generic Process Design Kit

HS High Speed

I^2C Inter-Integrated Circuit

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NMOS N-type Metal-Oxide-Semiconductor

PMOS P-type Metal-Oxide-Semiconductor

PVT Process- Voltage-Temperature

SCL Serial Clock Line

SCLH High-Speed Serial Clock

SDA Serial Data Line

SDAH High-Speed Data