Czech Technical University in Prague
Faculty of Electrical Engineering
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Design and Classification of IC Layout Mached Structures

Master's thesis

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Field of study: Electronics
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Prague, 2017

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Declaration

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In Prague, 2017

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Pavel Vančura

ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

ZADÁNÍ DIPLOMOVÉ PRÁCE

I. OSOBNÍ A STUDIJNÍ ÚDAJE

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Studijní program: **Komunikace, multimédia a elektronika**

Studijní obor: **Elektronika**

II. ÚDAJE K DIPLOMOVÉ PRÁCI

Název diplomové práce:

Návrh a klasifikace generování párových struktur topologie IO

Název diplomové práce anglicky:

Design and Classification of IC Layout Mached Structures

Pokyny pro vypracování:

Popište, jak vznikají náhodné a systematické neshody v procesu IO a metody, kterými tyto neshody můžeme minimalizovat. Navrhněte matematický model systematické neshody v procesu IO, ke které dochází v průběhu navrhování topologie IO. Na základě matematického popisu navrhněte a optimalizujte metodu pro klasifikaci topologie symetrických a nesymetrických párových struktur v IO.
Při sestavování matematického popisu zvažte neznámou pozici topologie párové struktury na křemíkové desce, zdali se jedná o aktivní či pasivní integrované součástky, různý počet elektronických součástek, jejich rozdělení na více částí včetně "dummy" struktur a nastavení poměru W / L součástky.

Seznam doporučené literatury:

[1] H. Elzinga,On the impact of spatial parametric variations on MOS transistor mismatch, Microelectronic Test Structures. 1996 IEEE International Conference on. IEEE, pp. 173-177, 1996.
[2] M. J. M Pelgrom, A. C. J Duinmaijer, A. P. G. Welbers, Matching properties of MOS transistors, IEEE J. Solid-State Circuits, vol. SC-24 pp. 1433-1439, 1989.
[3] Michael, Christopher, and Mohammed Ismail. Statistical modeling of device mismatch for analog MOS integrated circuits, IEEE Journal of Solid-State Circuits 27.2, pp. 154-166, 1992.
[4] Okada, Kenichi, Hidetoshi Onodera, and Keikichi Tamaru. Layout dependent matching analysis of CMOS circuits, Analog integrated circuits and signal processing 25.3, pp. 309-318, 2000.

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Jméno a pracoviště druhé(ho) vedoucí(ho) nebo konzultanta(ky) diplomové práce:

Datum zadání diplomové práce: **03.02.2017** Termín odevzdání diplomové práce: _____

Platnost zadání diplomové práce: **10.09.2018**

Podpis vedoucí(ho) práce	Podpis vedoucí(ho) ústavu/katedry	Podpis děkana(ky)

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Abstract

The systematic mismatch arising during the manufacturing process for integrated circuits can be effectively reduced by a proper layout technique. The new method for matched structures classification introduced in this work is able to compare different layout patterns, resulting in increasing efficacy during the design process. The most robust pattern suppressing systematic mismatch can be detected. Active or passive microelectronic device matched structures are classified by estimating parameter gradient function up to the fifth order. Due to unknown position of a device pattern on a wafer, matched structures are evaluated in eight different directions. The worst case of matching is used as representative result. An input layout pattern can contain an arbitrary amount of subdevices including dummy devices. The result is then summed up into one evaluation vector which improves orientation in results and facilitates the right pattern decision. This innovative method helps to save time and increase yield and effectivity of design process.

Keywords: pattern, mismatch, gradient, layout, classification, method

V jednotlivých krocích výroby integrovaných obvodů vznikají systematické neshody v parameterech aktivních i pasivních mikroelekronických součástek. Tyto systematické neshody lze snížit vhodným rozmístěním součástek u kterých je požadována shoda v parameterech do symetrických topologií, čímž dochází k eliminaci systematické neshody v určitém parametru, nebo u aktivních součástek i ve více parameterech. V této práci je navržena nová metoda která je schopna porovnat předem navržené topologie a vybrat tu s nejmenší odchylkou v parametru mezi dvěmi a dokonce i více součástkami. Metoda je založena na matematickém modelu gradientu parametru až do pátého řádu a je vhodná pro aktivní i pasivní součástky. Směr působení gradientu na parametr je počítán v osmi ortogonálních směrech kvůli neznámé orientaci topologie na křemíkové desce. Směr kde metoda vyhodnotí nejhorší nesoulad v parametru je potom použit jako representativní výsledek. Testované topologie mohou obsahovat velký počet součátek včetně dummy součástek. Pokud je v určité topologie použit počet součástek větší jak tři, je možné nastavit váhu testované součátky k referenční součástce a sjednotit všechny vysledky do pouhých pěti čísel. Tím se velmi zjednodušší orientace ve výsledcích a výběr vhodné topologie. Tato metoda je inovativní a umožnuje zkrátit čas při výběru topologií, zvýšit výtěžnost a efektivitu při návrhu mikroelektronických struktur.

Klíčová slova: topologie, neshoda, nesoulad, parametr, gradient, metoda

Acknowledgements

I would like to express my gratitude to Vlastimil Kotě, Patrik Vacula and Adam Kubačák from STMicroelectronics for hours spent by constructive consultations, useful comments throughout creation of this thesis and opportunity to present this work on CDNLive conference in Munich, Germany. Also, I would like to thank to doc. Jiří Jakovenko for master thesis leading and for providing support from SGS grant SGS17/188/OHK3/3T/13 to settle CDNLive conference charges. Last but not least, I thank to my wife how patient she has been during arising this thesis.

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List of Acronyms

Analog to Digital Converter (ADC)
Capacitive Analog to Digital Converter (CDAC)
Complementary Metal–Oxide–Semiconductor (CMOS)
Central Limit Theorem (CLT)
Chemical Vapor Deposition (CVD)
Digital to Analog Converter (DAC)
Graphical User Interface (GUI)
Metal Insulator Metal (MIM)
Metal–Oxide–Semiconductor (MOS)
N-chanel Metal–Oxide–Semiconductor (NMOS)
Successive Aproximation Register (SAR)
System on Chip (SoC)

Contents

Introduction

The main limitation of the precise analog integrated circuits is established by noise and mismatch. There are variations in component parameters in each step of the manufacturing process for microelectronic analogue circuits. More recent deep submicron analog devices are even more sensitive to a parameter variability than older technologies. These variabilities in manufacturing steps lead to a mismatch of parameters for identically designed microelectronic active and passive devices. Deviation in undividual manufacturing step are usually divided into two main categories, stochastic and systematic mismatch. Stochastic errors are also called random errors. Random effects caused by an ion implantation for example, the number of dopant variations resulting in a local difference between a parameter value for two or more identically designed devices. The stochastic mismatch is, in the designing process, defined by a variance measured and provided by a manufacturer of particular technology for each device and their parameters. Variance is used as an estimation of random mismatch using hand calculation or Monte Carlo simulation in design software. The first part of this thesis is dedicated to random mismatch and two examples of stochastic errors in hand calculation are shown.

The random mismatch is usually well handled in a designing process. On the other hand in a design software no common tools exist to handle systematic mismatch. The typical source of systematic error is an oxide thickness variation. Individual technological causes of systematic mismatch are summarized and justified as a parameter gradient which is a function of a distance. The random mismatch and their physical causes are also summarized into a variance. The systematic mismatch is minimized by a proper layout technique described in the second part of the first chapter. For example two devices where good matching is required, they are usually divided into a number of subdevices and placed symmetrically into a pattern in order to eliminate a parameter gradient. While the case of a pattern containing only two devices and a few subdevices is a proper structure readily found, in cases of more than three devices and a numerous subdevices it is not easy to find a proper layout structure. The main goal of this thesis is to create a method that will be able to classify different matched structures containing the same number of devices and subdevices with different layout topology and select the most robust layout pattern resistant to the systematic mismatch.

The most important step in this thesis is finding a mathematical description which will characterize the physical causes of the systematic mismatch. The mathematical description in the second chapter is derived. The main idea behind the mathematical description is to model

the systematic mismatch as a two-dimesional function from linear up to the fifth order. The two-dimesional function represents a parameter gradient that is physically caused by systematic mismatch, for example an oxide thickness variation etc. Variations in z-axis are neglected. Individual devices in a pattern is placed to vertical and horizontal coordinates and a parameter value from modeled two-dimensional function is calculated. As the position of a pattern on the wafer is unknown, devices are placed into the mesh grid in eight orthogonal directions. A worse case direction is then used as a representative result in the mismatch calculation. The proposed matched structures algorithm also allows one to insert dummy devices, set width, length ratio of a device. This proposed method is applicable to both active and passive devices The algorithm is implemented in the Matlab software with a graphical user interface for input, output data and settings, or without the graphical user interface where an input data and settings can be loaded by a text file with defined structure and output data written into another text file. These two options are described at the end of the second chapter.

The third chapter is dedicated to figuring out how the proposed method is used for the design and classification of matched structures used in design of 10-bit analog to digital converter with charge redistribution in CMOS 180 nm process.

The proposed method is new, innovative and currently is used in the STMicroelectronics. With reference to available literature, at the present time a similar method that is able to classify matched structures is not available.

Chapter 1

Mismatch Theory

Studies of design analog integrated circuits mostly assumes that circuits are perfectly symmetrical, i.e. a circuit of current mirrors assumes that the same current flows through both transistors. In practice, theoretically symmetric devices exhibit inaccuracies in each step of the manufacturing process. For example, uncertainties in the length and width of channel of an MOS transistor or different doping levels cause mismatch properties of these devices. The study of mismatch involves two steps. The first, identify and formulate the mechanisms that lead to mismatch between devices. The second, analyze the effect of device mismatches upon the performance of circuits [1].

Relative mismatch between two identically designed devices is ideally zero and can be calculated according to following equation

$$\Omega = 2\left|\frac{P_A - P_B}{P_A + P_B}\right| 100 \tag{1.1}$$

where Ω is mismatch between device A and B, P_A and P_B are parameters of the same magnitude. Of course, these compared parameters have to be the same magnitude. Relative mismatch is holds for example for resistance, current, capacitance and β factor. On the other hand, for absolute magnitudes as difference of the threshold voltage V_{TH} of MOS transistor mismatch is defined according equation 1.2

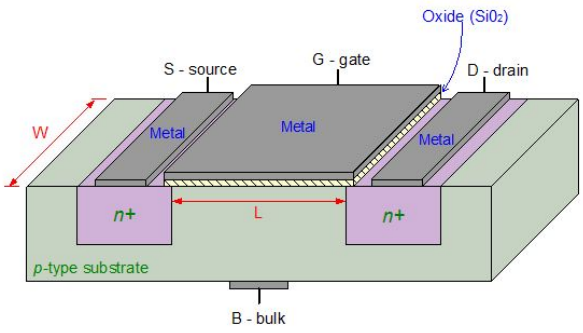

Figure 1.1: MOS transistor [2]

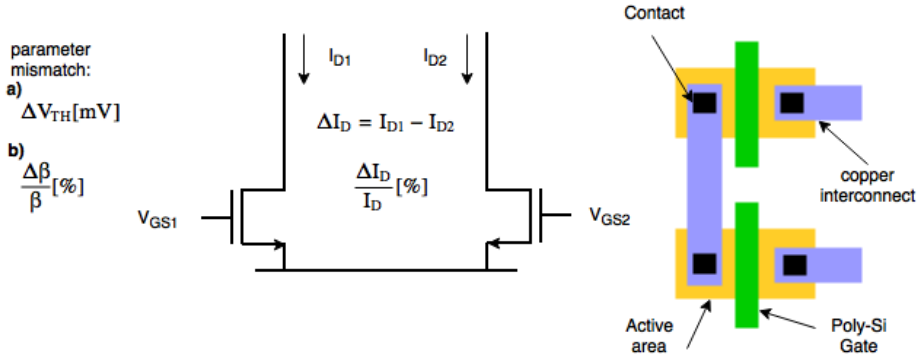

Figure 1.2: Mismatch of MOS transistor

$$\Delta V_{TH} = V_{TH1} - V_{TH2} \tag{1.2}$$

Mismatch is zero when values of parameters of devices A and B are identical. In the design of precision analog circuits left out matching very strongly degrade performance of a circuit. Good examples are current mirror and differential pair circuits, two of most significant circuits used in analog design almost in all more complex circuits. Mismatch between transistors in the differential pair causes undesirable voltage offset and in case of current mirrors causes nonidentical ratio current mirroring. The equation 1.3 describes behavior of the N-channel MOS transistor in the strong inversion

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.3}$$

where μ_n is mobility of electrons, C_{ox} is oxide capacitance, W and L are physical dimensions, V_{GS} is voltage gate to source and V_{TH} is threshold voltage. Apart from MOS transistor, capacitors and resistors are in analog design frequently used as well. Of course, the above stated equation 1.1 can be used for resistors or capacitors as well. These variations in a parameter of identically designed devices are caused by variations in manufacturing process, for example different doping levels, irregular thickness of oxide, lithography inaccuracy and others. It is out of scope of this thesis to describe manufacturing process variations in great detail. The main purpose of this thesis is focused to finding method how to face mismatch especially by layout techniques. Mismatch can be categorized to two main categories, the random mismatch characterized as stochastic process and the systematic mismatch which can be effectively minimized by a proper layout technique. Random and systematic mismatch are describes in the following section.

1.1 Difference between Random and Systematic Mismatch

First attempts to model mismatch behavior in integrated circuit manufacturing have been focused to MOS transistors devices. One of first models based on MOS transistor physics was Lakshmikumar model [3] in 1986. Another, more popular was Pelgrom's model [4] published

in 1989. Pelgrom derived his MOS transistor mismatch model from spectral analysis resulting in very simple model which is used today's designers and manufactures. Manufactures provides so called Pelgrom coefficient in their design rule specifications and this coefficient is used by all analog design engineers for random mismatch calculations around the world. Pelgrom's model is used for any rectangular device including capacitors and resistors. This model will be discuss in more detail in the following section. Some statistical models can be found between articles as well, for example [5], but these models are usually very complicated for using in practice. Examples of physical causes for differences between identically designed devices shows the table 1.1.

Stochastics effects	Systematic effects
ion implantation	electrical errors
dopant fluctuations	photo-mask differences
edge roughness	photo-resist thickness variations
poly-Si grain effects	CVD[1] layers variations

Table 1.1: Examples physical causes for differences

Matching is defined as random variation between two identically designed devices after fabrication. Pelgrom's model [4] is most widely used in the matching terminology

$$\sigma^2_{\Delta P} = \frac{A_P}{WL} + S_P^2 D^2. \tag{1.4}$$

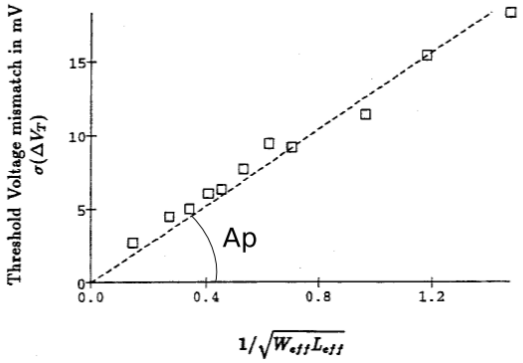

Figure 1.3: Pelgrom's Random Model [4]

The first term $\frac{A_P}{WL}$ is the random part of a mismatch. This term simply says that in order to improve matching two times, we need to increase an area of device four times. The coefficient A_P is the Pelgrom coefficient and can be obtained from a manufacture in design rule (DR) specification of particular process or by measurement. Random mismatch part can be improved by larger size of a device. The second part of Pelgrom's equation $S_P^2 D^2$ is called the systematic

[1]Chemical Vapor Deposition (CVD) is process to produce a thin layers is semiconductor industry

mismatch. Second physical cause in Pelgrom's equation 1.4 is parameter S_P produced by the fact that physical device parameter gradient is presented along the die. Systematic mismatch is function of distance between devices and constant S_P which can be also obtained from statistics of manufacturing process. However, constant S_P is not commonly provided by a manufacture but can be modeled by gradient modeling method which is introduced in following chapter. The systematic part of mismatch can be improved by a proper layout.

This master thesis is focused to matched structures clasification, in other words how two or more different layout patterns are resistant against a change of parameter gradient as a function of a distance. This work starting from second chapter is thus especially focused to systematic part of mismatch. Random part of mismatch may be affected by increasing area of a device or decreasing W/L ratio. Systematic part only by a proper layout pattern.

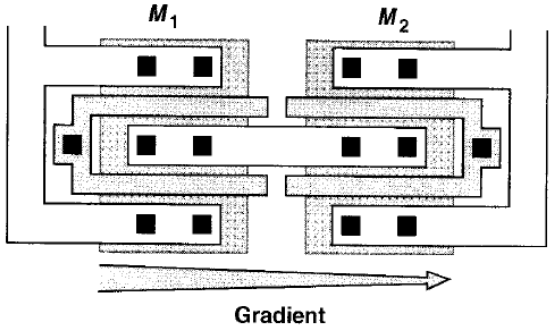

Figure 1.4: Example of systematic mismatch in the Layout [1]

1.2 Random Mismatch

Generally, methods of statistics for describing stochastical effects in electronic components are used. We can learn from analysis of limited numbers of samples that are affected by random mismatch fluctuations. The purpose is determination of the statistical distribution of electrical differences between closely spaced identical components. Fluctuations of a parameter[2] $\frac{\Delta P}{P}$ for a statistically significant number of matched pairs or circuits are measured. The mean value and variance of limited number of samples are calculated by following equations [6]

$$\mu = E[x] = \sum_{i=1}^{n} p_i x_i \tag{1.5}$$

where p_i is probability, $p_i = P[x = x_i]$.

$$\sigma^2 = E[x^2] - E[x]^2 = E[(x - E[x])^2] = \sum_{i=1}^{n} p_i (x_i - E[x])^2 \tag{1.6}$$

The central limit theorem (CLT) have huge physical impact in electrical measurement. CLT states that under certain general conditions, the distribution $F(x)$ of x approaches a normal

[2]difference of parameter P againts to nominal value of parameter P

distribution with the same mean and variance as n increases

$$F(x) = G\left(\frac{x-\mu}{\sigma}\right). \tag{1.7}$$

Furthermore, if random variables x_i are of continuous type, the density $f(x)$ of x approaches a normal density [6]

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{1.8}$$

where μ is the mean value and σ is variance.

Many times are two parameters in a random function correlated. In this case holds following formula 1.9 [6].

$$\rho(y_1, y_2) = \frac{E[(y_1 - \mu_{y1})(y_2 - \mu_{y2})]}{\sigma_{y1}\sigma_{y2}} = \frac{cov(x,y)}{\sigma_{y1}\sigma_{y2}} \tag{1.9}$$

where $\rho(y_1, y_2)$ is correlation coefficient and $cov(x, y)$ is covariance. If $\rho(y_1, y_2) = 0$ then variables are called uncorrelated. The covariance is implemented in order to calculate the variance of a random vector[3], because mean value and variance of a random vector not provide sufficient information if random variables are correlated.

Above stated equations allows calculate the variance of a component. When variance of a magnitude in a circuit is calculated, the transformation of random variables is often used [6]

$$\sigma^2(y) = \sum_{i=1}^{n} \left(\frac{\partial y}{\partial x_i}\right)^2 \sigma^2(x_i) \tag{1.10}$$

where x_i are mutually independent random variables. The application of equation 1.10 is shown on the following example.

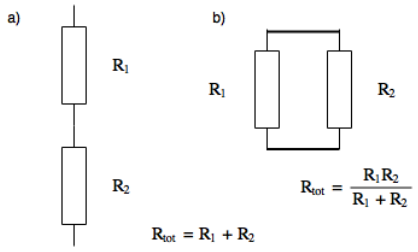

Figure 1.5: Example of calculation random error of serial and paralel resistance

Calculation of total resistance error of serial resistance on the figure 1.5 [7]

$$\sigma^2(R_{tot}) = \left(\frac{\partial R_{tot}}{\partial R_1}\right)^2 \sigma^2(R_1) + \left(\frac{\partial R_{tot}}{\partial R_2}\right)^2 \sigma^2(R_2) = \sigma^2(R_1) + \sigma^2(R_2). \tag{1.11}$$

[3]random vector is composed of more random variables $\vec{X} = (X_1, X_2, .., X_n)$

Calculation of total resistance deviation of parallel connected resistors of figure 1.5:

$$\sigma^2(R_{tot}) = \left(\frac{\partial R_{tot}}{\partial R_1}\right)^2 \sigma^2(R_1) + \left(\frac{\partial R_{tot}}{\partial R_2}\right)^2 \sigma^2(R_2) \tag{1.12}$$

$$\sigma^2(R_{tot}) = \frac{R_2^2}{(R_1+R_2)^2}\sigma^2(R_1) + \frac{R_1^2}{(R_1+R_2)^2}\sigma^2(R_2) \tag{1.13}$$

Another example [7] of calculation of variance as function of random variable is shown on the integrator circuit depicted on the figure 1.6.

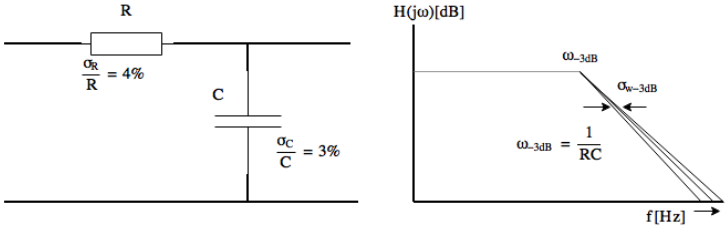

Figure 1.6: Example of calculation random error of cutoff frequency of the integrator circuit

The cut-off frequency ω for -3 dB is equal to $\frac{1}{\tau}$ where time constant $\tau = RC$. Then the variance of the cut-off frequency is calculated as follows [7].

$$\sigma^2_{\omega_{-3dB}} = \left(\frac{\partial \omega_{-3dB}}{\partial R}\right)^2 \sigma_R^2 + \left(\frac{\partial \omega_{-3dB}}{\partial C}\right)^2 \sigma_C^2 = \left(\frac{-1}{R^2C}\right)^2 \sigma_R^2 + \left(\frac{-1}{RC^2}\right)^2 \sigma_C^2 \tag{1.14}$$

Then the relative error of cutoff frequency is

$$\frac{\sigma_{\omega_{-3dB}}}{\omega_{-3dB}} = \sqrt{\frac{(\frac{-1}{R^2C})^2\sigma_R^2 + (\frac{-1}{RC^2})^2\sigma_C^2}{(\frac{1}{RC})^2}} = \sqrt{\frac{\sigma_R^2}{R^2} + \frac{\sigma_C^2}{C^2}} = \sqrt{4^2+3^2} = 5\%. \tag{1.15}$$

For calculation of random mismatch of transistors is the first term of Pelgrom's model 1.4 widely used. Suppose that the variance of threshold voltage is investigated. The Pelgrom's constant obtained from a fab documentation is $A_{VT} = 10mV\mu m$. Consider four common transistors topologies as on the following figure 1.7 [7].
For standard differential pair on 1.7 a) is mismatch $\sigma_{V_1-V_2}$ equal to

$$\sigma_{V_1-V_2} = \frac{10mV\mu m}{\sqrt{5\mu m * 20\mu m}} = 1mV \tag{1.16}$$

If a double diffrential pair 1.7 b) is used then will be mathing between threshold voltages about 29 % better.

$$\sigma_{V_1-V_2} = \frac{10mV\mu m}{\sqrt{5\mu m * 40\mu m}} = 0.71mV \tag{1.17}$$

In case of calculation threshold voltage variation for one single transistor 1.7 c) is variance

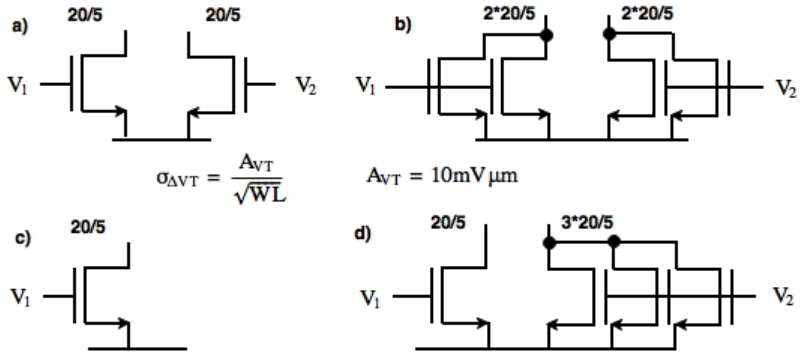

Figure 1.7: Example of calculation random error of threshold voltage four different transistor's topologies [7]

divided by square root of two.

$$\sigma_{V_1-V_2} = \frac{10mV\mu m}{\sqrt{2}\sqrt{5\mu m * 20\mu m}} = 0.71mV \tag{1.18}$$

Finally for calculation current mirror threshold voltage variance 1.7 d), the result 1.18 can be used.

$$\sigma_{V_1-V_2} = \sqrt{0.71^2 + \frac{0.71}{3}} = 0.82mV \tag{1.19}$$

1.2.1 MOS transistor mismatch origins

This section describes basics MOS transistor physics and associated mismatch between two MOS devices. Consider NMOS transistor with the source electrode connected to the ground, drain to +0.1V. What happens as gate voltage V_G increases from zero? As V_G becomes more positive, the holes in p-substrate are pushed away from gate area, a depletion region is created. When V_G reaches sufficiently positive value, electrons starts flow from source to drain electrode. Gate electrode has two capacitance. First is capacitance between gate and oxide C_{ox} and the depletion region capacitor C_{dep}. The value of V_G when current starts flow is called the threshold voltage V_{TH}. According to [1], threshold voltage is function proved following equation

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}} \tag{1.20}$$

where Φ_{MS} is difference between the work functions of the polysilicon gate and the silicon substrate, $\Phi_F = \frac{kT}{q} ln(\frac{N_{sub}}{n_i})$, k is Boltzmann's constant, T is temperature, q is electron charge, N_{sub} is doping concentration of the substrate. Q_{dep} is the charge in depletion region and C_{ox} is the gate oxide capacitance per unit area.

MOSFET drain current I_d in the saturation region ($V_{DS} \geq V_{GS} - V_{TH}$) is approximately

$$I_d \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.21}$$

where μ_n is the mobility of electrons, W and L are width, length respectively, V_{GS} is voltage gate

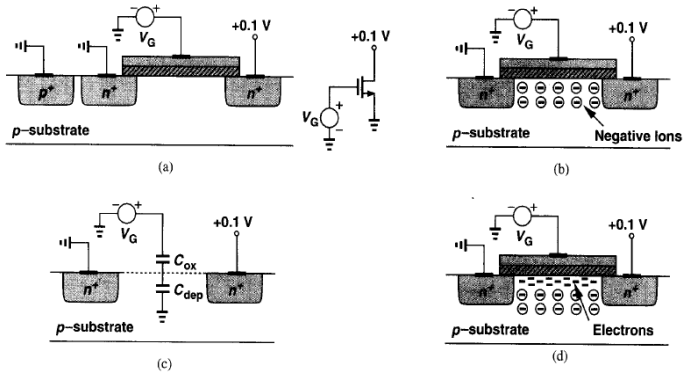

Figure 1.8: (a) A MOS transistor driven by a gate voltage, (b) formation of depletion region, (c) onset of inversion, (d) formation of inversion layer [1]

to source and V_{TH} is threshold voltage. For the triode region ($V_{DS} < V_{GS} - V_{TH}$) is equation for drain current approximately

$$I_d \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS}. \tag{1.22}$$

When we look to above metioned equations, we can observe mismatches between μ, C_{ox}, W, L and V_{TH} affecting each individual MOS transistor on the substrate. Changes of these parameters are caused by technological processes uncertainties. An important observation is that mismatch decreases as the area of the transistor increases [1], [8]. Assume the NMOS transistor with the channel width W and channel length L. When we slice up width of this transistor to n slices of a new width W_0, we get n slightly different channel lengths [1]

$$\Delta L_{eq} \approx \frac{\Delta L_1^2 + \Delta L_2^2 + ... + \Delta L_n^2}{n} = \frac{(n\Delta L_0^2)^{1/2}}{n} = \frac{\Delta L_0}{\sqrt{n}}. \tag{1.23}$$

where ΔL_0 is the statistical variation of the length the channel for a transistor with width W_0. The equation 1.23 discovers very the important fact that when n increases, the variation ΔL_{eq} decreases. This invention can be extended to other parameters μC_{ox} and V_{TH}. Each individual transistor with W_0 and L_0 will have $(\mu C_{ox})_j$ and V_{THj}. If number of unit transistors increases, μC_{ox} and V_{TH} exhibit greater averaging, thus smaller mismatch between two large transistors [1]. The $\Delta(\mu C_{ox}\frac{W}{L})$ and ΔV_{TH} can be mathematically expressed according to Pelgrom's model [4] discussed in the previous section 1.2:

$$\Delta(\mu C_{ox}\frac{W}{L}) = \frac{A_k}{\sqrt{WL}} \tag{1.24}$$

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{1.25}$$

For better using of equation 1.25, the A_{VTH} can be according to [1] expressed with oxide thickness t_{ox}. $A_{VTH} \approx 10mV$ for $t_{ox} \approx 100\mathring{A}$. Two transistors in 0.6 μm technology exhibit V_{TH} mismatch 1.4 mV. These devices have size 100 μm / 0.6 μm. Therefore, we can modify the

equation 1.25 to

$$\Delta V_{TH} = \frac{0.1 t_{ox}}{\sqrt{WL}}. \tag{1.26}$$

The simplification in the equation 1.26 may be used for a rough estimation, on other hand the Pelgrom's coefficient always should be present in a design rule specification of a particular manufacturing process.

MOS transistors with higher W/L rate typically have poorer random part of matching. This section explains this preposition mathematically according to [8].

1.2.2 Threshold Voltage Mismatch

The work done in the reference [8] is concerned to changing $\frac{W}{L}$ ratios while the area WL remains the same.

Effective dimensions are defined as follows

$$W_{ef} = W_{drawn} - DW \tag{1.27}$$

$$L_{ef} = L_{drawn} - DL \tag{1.28}$$

where DL a DW are channel length and width reduction parameters.

Equation 1.4 is restated below with the difference that the effective dimensions for V_T mismatch are now used instead of drawn dimensions

$$\sigma(\Delta V_T) = \frac{A_{VT0}}{\sqrt{W_{ef} L_{ef}}}. \tag{1.29}$$

According with [8] following observations can be made.

- For equal drawn layout area devices, those with greater effective areas have better mismatch in accordance with [8].
- For equal drawn layout area devices, as channel length becomes shorter and channel width is relatively wide, the effective layout area is greatly reduced and matching is poor as predicated by [8].
- For equal drawn area devices, if channel length is relatively long and width is narrow, the effective area is larger and matching is better [8].

1.2.3 β Mismatch

The current factor β is a combination of following parameters

$$\beta = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \tag{1.30}$$

where μ is the channel mobility and C_{ox} is the gate oxide capacitance. Gate oxide capacitance will be virtually constant for adjacent devices. Research suggests that mobility variations are likely to be dominant source of β parameter mismatch. By considering β as a function of four variables and derivation, following expression is obtained [8]

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A^2_{W^2}}{W^2L} + \frac{A^2_{L^2}}{L^2W} + \frac{A^2_{\beta^2}}{WL} \tag{1.31}$$

where W and L refer to the drawn channel dimensions and A_W, A_L, A_β are constants. The effective dimensions arrived at for V_T mismatch no longer apply since they were derived with the assumption that substrate doping was dominant source of mismatch, this cannot be assumed in the case of β mismatch. For short channel device, the term $\frac{A^2_{L^2}}{L^2W}$ becomes significant and inflates the β mismatch. The β mismatch is consistent with the theoretical predictions described above, where devices with short channels show greater measured mismatch. It is apparent that in the case of β mismatch for equal drawn area devices, as was the case for V_T mismatch, a wide channel device with short channel length (large W/L ratio) has poorer matching than an equal area narrow channel transistor with relatively long channel (small W/L ratio). This difference in matching can be much as 300 % [8].

1.2.4 Drain Current Mismatch

The relationship between drain current mismatch and mismatches in V_T and β shows following formula [8]. This formula 1.32 is derivative of MOS drain current in strong inversion 1.3 according the transformation of independent random variables 1.10.

$$\frac{\sigma^2(\Delta I_d)}{I_d^2} = \frac{\sigma^2(\Delta\beta)}{\beta^2} + 4\frac{\sigma^2(\Delta V_{TH})}{(V_{GS} - V_{TH})^2} \tag{1.32}$$

where $\sigma^2(\Delta V_{TH})$ and $\sigma^2(\Delta\beta)$ are the measured mismatches in V_{TH} and β. The variations in mismatch between equal area devices which have been observed in V_{TH} and β are transferred to I_d mismatch through the relationship shown in 1.32 above. A comparison between the I_{DS} matching performance of the equal area devices reveals that the same trends are present for drain current mismatch as were observed for V_T and β mismatch, namely that devices with a small W/L ratio have better matching then equal area transistors with a large W/L ratio. Drain current mismatch shows very dramatic improvements in matching for equal area devices of up to 500 % obtained simply by selecting a smaller W/L ratio and without increasing layout area. It is also interesting to note that device with the best matching performance is not largest drawn area device. More information about different area device matching can be found in [8]. Drain current mismatch are same for both saturation and linear region.

1.3 Layout Techniques for Minimum Mismatch

The systematic mismatch described in the section 1.1 is effectively eliminated by proper layout techniques. Proper layout techniques are important for the yield of digital IC's and in analog systems can a proper layout significantly decrease mismatch, crosstalk and noise [1]. Differences in electrical parameters between identically designed devices in a layout are caused mainly by a poor layout, parameter gradient, lithography effects (proximity effect), incorrect reference distribution, temperature gradients and the package stress. A parameter gradient, or in other words the systematic mismatch, the second term in the Pelgrom's model 1.3, is effectively eliminated by symmetric (common centroid) structures. Sometimes in a layout design is not easy to determine what matched structure is better if contains a large number of subdevices. Classification of these symmetrical structures for elimination of systematic mismatch is the main focus of this work starting by the second chapter. Matched devices must be of the same type, size and shape. Other above mentioned sources of mismatch, temperature gradients, reference distribution, proximity effects and the package stress are briefly described in this section.

1.3.1 Multifinger Transistors

To help reduce source, drain junction area and the gate resistance, wide transistors are usually folded. According to [1], the width of each finger is chosen such that the resistance of the finger is less than the inverse transconductance associated with the finger. In low-noise applications, the gate resistance must be one-fifth to one-tenth of $1/g_m$[4]. On other hand, the negative effect more parallel fingers is that the capacitance with the perimeter of the source/drain is increased. Thus, the number of fingers must be much less than width of transistors to minimize the source, drain perimeter capacitance contribution.

1.3.2 Symmetry

An asymmetry in the layout can have stronger effect on the circuit behavior then inevitable mismatch caused by technological processes. It is important in agreement with [1] to note that steps in lithography and wafer processing must behave equally along different axes to devices of interest and their surrounding environment. Another thing in considering the layout topology is effect called gate shadowing. This effect arises when the source/drain implantation because the implant (or wafer) is tilted by 7 degrees to avoid channeling. As a result, the small region behind the gate area is shadowed and obtains less implantation, creating a small asymmetry. Therefore, is important to take in account the shadowing effect when choosing between topologies. Also, the asymmetry of structures can be sometimes improved by "dummy" devices to suitable place in the layout. The symmetry should be applied to metals as well even though the replica may remain floating. The another aspect of symmetry which is needed to take in account is the gradient along x-axis of the wafer. For large devices is gradient more significant. Therefore,

[4] $1/g_m = R_{DS}$ where R_{DS} is drain to source resistance of a channel

to reduce the error, a "common-centroid" configuration may be used such that the effect of first-order gradients along both axes is canceled in agreement with [1]. Consider in instance two large transistors forming the differential pair, they can be splited into four transistors and place them diagonally opposite of each other and connected in parallel to reduce gradient effect as in figure 1.9.

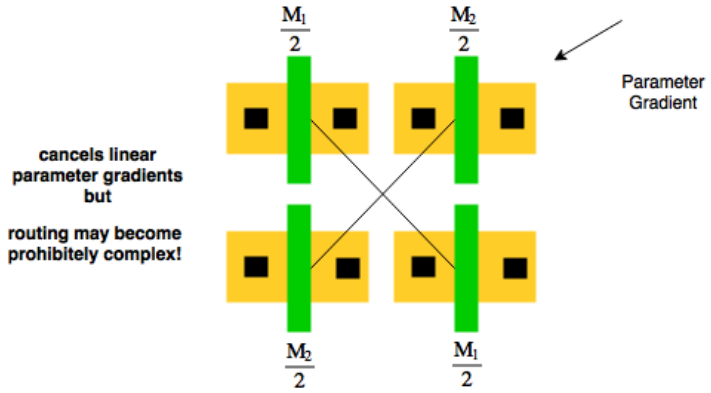

Figure 1.9: Common centroid structure for canceling the linear parameter gradient [1]

The routing of interconnects sliced transistor can be difficult in the layout, often leading to systematic asymmetries or in the capacitances from the wires to ground and between the wires. The effect of linear gradient can be also reduce in one-dimension as in figure 1.10.

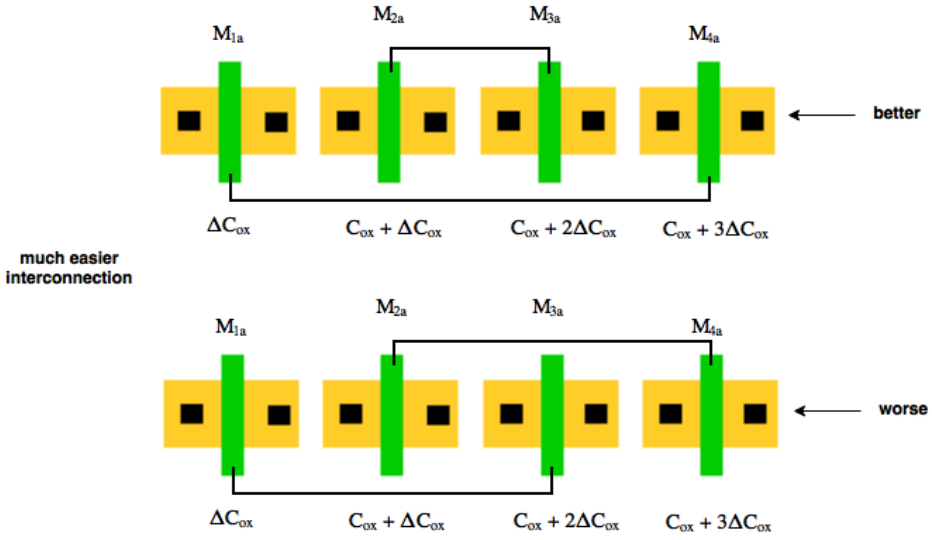

Figure 1.10: One-dimensional common centroid structure for canceling the linear parameter gradient [1]

Assuming four transistors M_1, M_2, M_3 and M_4 ordered in the one row along x-axis and signed from the left. M_{1a} can be connected with M_{4a} and M_{2a} with M_{3a}. If we consider that the gate oxide capacitance varies by ΔC_{ox} then we have in accordance with [1]

$$I_{d1a} + I_{d4a} \approx \frac{1}{2}\mu(C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.33}$$

and for M_{2a} and M_{3a}:

$$I_{d2a} + I_{d3a} \approx \frac{1}{2}\mu(C_{ox} + \Delta C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.34}$$

The second option is connect M_{1b} with M_{3b} and M_{2b} with M_{4b}, then we obtain

$$I_{d1b} + I_{d3b} \approx \frac{1}{2}\mu(C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.35}$$

$$I_{d2b} + I_{d4b} \approx \frac{1}{2}\mu(C_{ox} + \Delta C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.36}$$

According to [1], equation 1.35 and 1.36 removes the error to a lesser extent.

To solve an issue with difficult interconnection in "rectangle" common centroid stuctures as in the figure 1.9, the interdigitated type of structures are often used. These structures are possible to use as common centroid in order to cancel the linear parameter gradient as well. However, they are arranged in one line rather than into two dimensional matrix. Therefore, the interconnection between matched devices is much more uniform excluding asymmetry arising when two dimensional interconnection as in case of the pattern in the figure 1.9. An asymmetry in a layout causes lithography errors called the proximity effect. Example of interdigitated structure is shown in the figure 1.11.

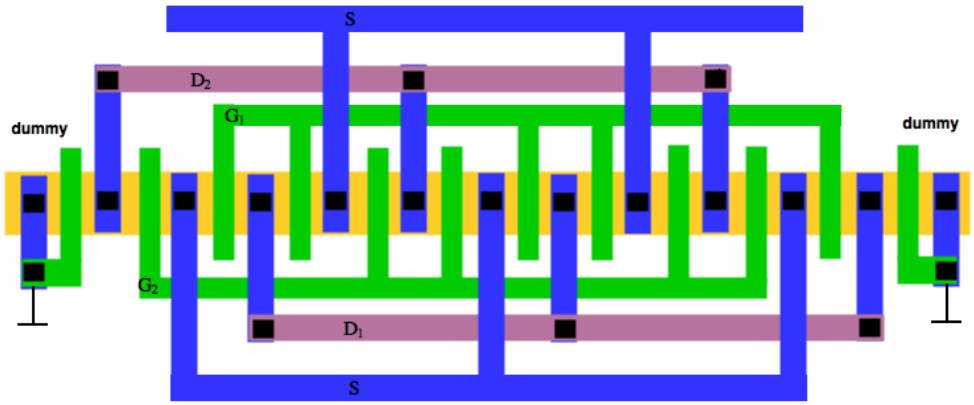

Figure 1.11: Interdigitated structure for canceling the linear parameter gradient [7]

1.3.3 Micro Loading Effect

Designed line width is different from manufactured line width depending on the size of line width (size effect, figure 1.12) and distance to its adjacent pattern (proximity effect, figure 1.14). These issues are called Micro-loading effect [9].

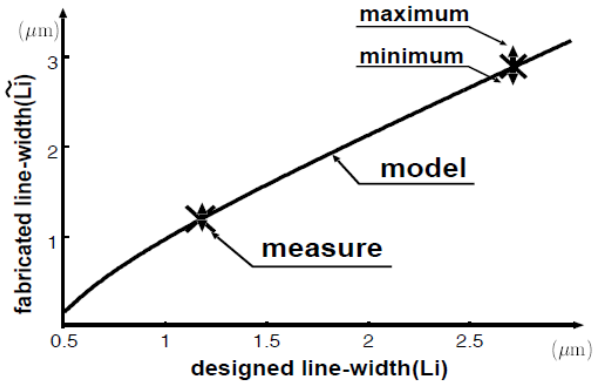

Figure 1.12: Size effect [9]

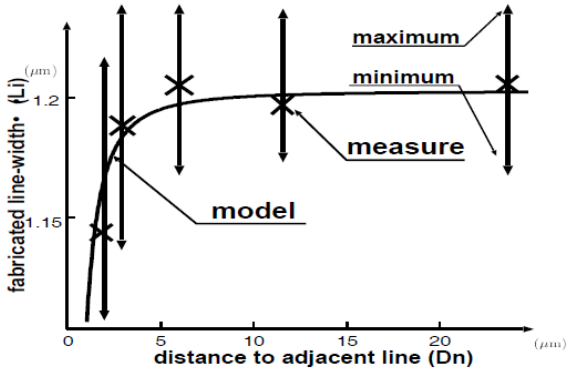

Figure 1.13: Proximity effect [9]

Micro loading deteriorates matching between devices in matched structures because of influence interconnection and symmetry as described in the previous chapter 1.3.2. Size and proximity effects are also the reason why dummy devices are added around a pattern as illustrated in the figure 1.14.

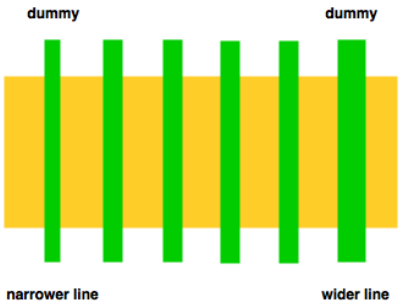

Figure 1.14: Illustration of purpose dummy devices in a layout

1.3.4 Reference Distribution

The distribution of voltage and bias references across large chip introduces important issues. Consider the circuit depicted in the figure 1.15 [1].

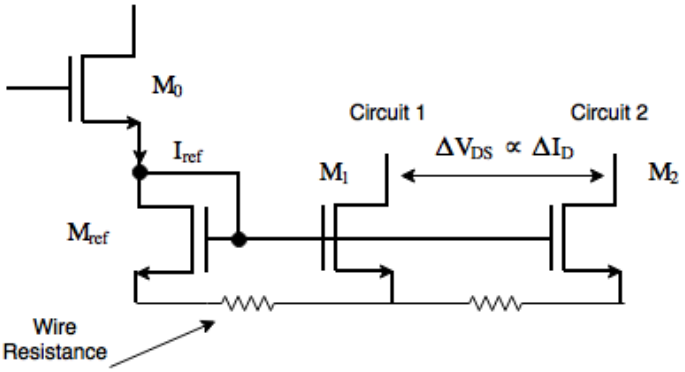

Figure 1.15: Example of influence a metal resistance to reference current [1]

If are current mirrors far away on the chip each other than the voltage drop along the ground line must be taken into account. In fact, in accordance with [1], if large number of circuits are connected to the same ground line, mismatch between current sources may be unacceptable. To improve voltage drop difficulty is better variant to distribute the reference in current domain instead in the voltage domain as is depicted on figure 1.16 [1].

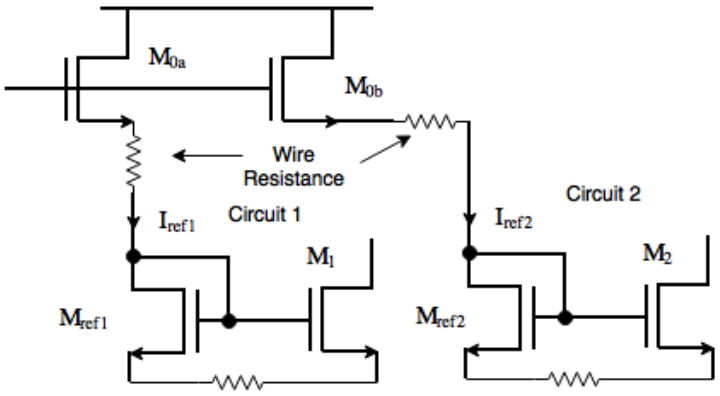

Figure 1.16: Reducing the effect of interconnect resistance [1]

Anyway, in large systems may be advantageous to use local reference sources instead leading current references across the chip. The another important issue in accordance with [1], the orientation of transistors in the layout described in the previous section must be the same otherwise the substantial mismatches arises. Moreover, the appropriate selection of dimensions W/L requires careful choice if scaling of currents is needed. As is depicted on figure 1.17 [1], the circuit requires $I_{d1} = 0.5I_{ref}$ and $I_{d2} = 2I_{ref}$.

To avoid large mismatches is the useful solution to design $W_1 = 0.5W_{ref}$ and $W_2 = 2W_{ref}$. Different widths may be performed by proper connection of the same W/L transistors as is depicted on 1.17 [1].

Similar problem is with connecting power supply lines and timing signals. Design rule says that we ever use the star-connected wiring for power and timing as on the figure 1.18.

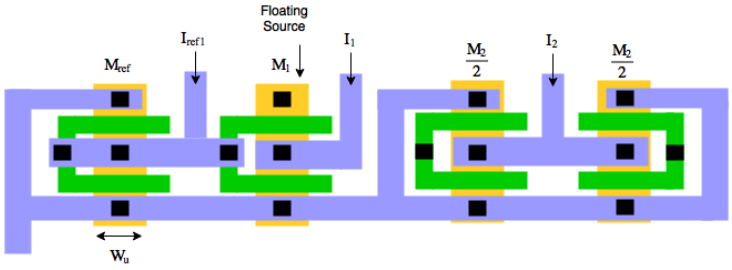

Figure 1.17: Proper scaling of device dimensions for better mathing [1]

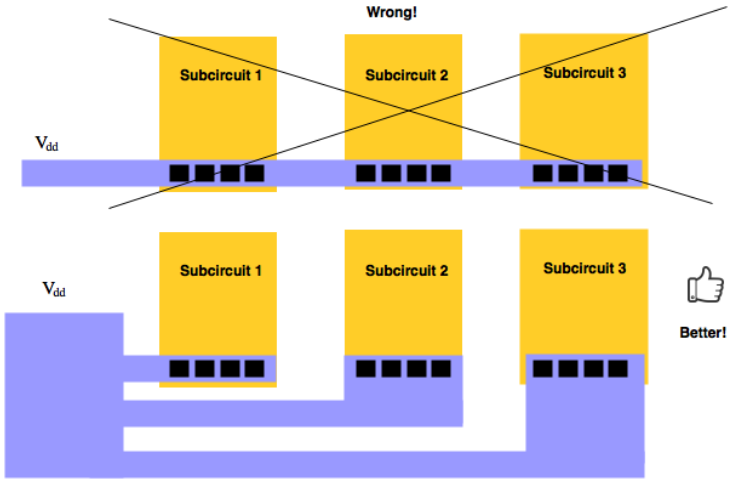

Figure 1.18: Star-connected power supply line [7]

1.3.5 Temperature Gradients

Nowadays system on chip (SoC) solutions integrates power devices and sensitive devices, for example ADC, DAC, bandgaps, at the same substrate. Typically, the temperature coefficient for threshold voltage, $\Delta V_T/\Delta T$ is -1 up to -3 mV/°C and current factor $(\Delta\beta/\beta)/\Delta T$ approximately 0.5 %/°C [7]. Therefore, for good matching is needed place sensitive circuit blocks as far as possible from heating devices and high power blocks should be placed symmetrically with respect to analog blocks. Matched structures should be placed in direction to equivalent temperature lines.

1.3.6 Resistors

Polysilicon resistors in accordance with [1] using a silicide block exhibit high linearity (length dependent), low capacitance to the substrate and relatively small mismatches. For example, resistors having a length of 5 μm and width of 3 μm display typical mismatches about 0.2 %. The symmetry described in the section 1.3.2 is applicable to polysilicon resistors as well. For example, a resistance may be consisted from small indentical units placed in parallel or in series (with the same orientation) such as illustrated example in the figure 1.19.

Sometimes from the viewpoint of matching may be preferable "serpentine" topology instead the serial connection, where corners contribute significant resistance. The sheet resistance, $R_{\square}$,

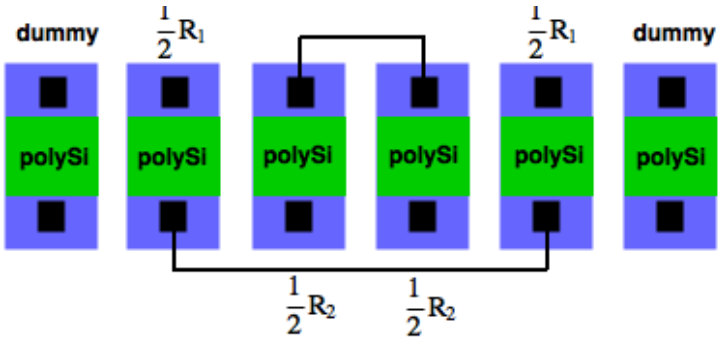

Figure 1.19: Example of matched Poly-Si resistors

of polysilicon varies with temperature and processes. Typical values in accordance with [1] are +0.1 %/°C and -0.1 %/°C for p^+ and n^+ doping. The another option how to create a resistor is using n-well, source/drain p^+ or n^+ or metal with a sheet resistance $R_\square$. $R_\square$ is function of width of the resistor. In case of n-well type of resistors, there is the strong dependency on n-well-substrate voltage difference. These resistors suffers from large mismatches. The p^+ and n^+ source/drain regions can also be used as resistors with $R_\square$ 3-5 Ohms, thus these resistors are suited only for small values. Furthermore, their values changes with process as high as 50 %. The metal layers can also provide low resistor values. However, if the width is small, mismatch becomes high. The temperature coefficient is about 0.3 %/°C.

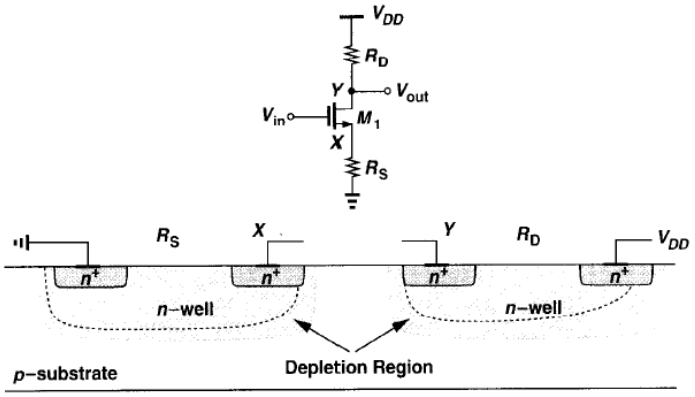

Figure 1.20: Common-source stage using n-well resistors [1]

1.3.7 Capacitors

High-density linear capacitors can be fabricated using polysilicon over diffusion, polysilicon over polysilicon, or metal over polysilicon, with relatively thin layer of oxide grown between the two plates [1]. The first structure exhibits more linear characteristics then do the other two, therefore is commonly used in today's analog processes. In absence of the above structures must be capacitors designed using sandwiches of the available conductive layers. In typical technologies, the parasitic capacitance between consecutive metal layers are on the order of

40 $aF/\mu m$. Typical values of ratio C_p/C are around 0.2.

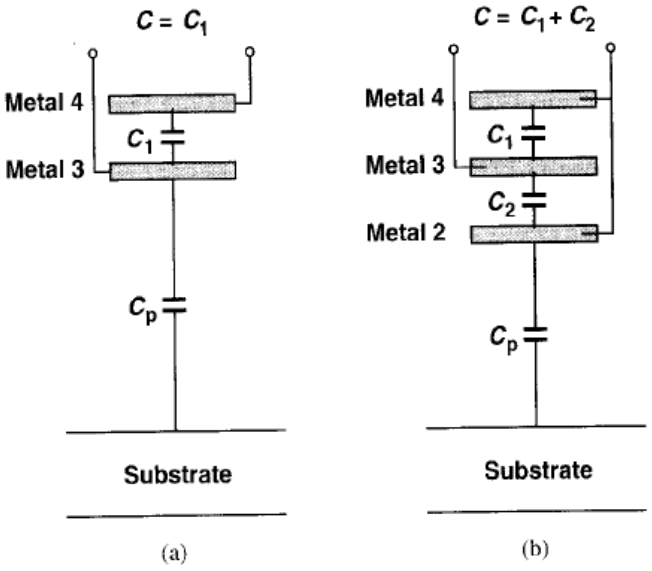

Figure 1.21: Capacitor structures using conductive layers [1]

In a real design, the fringe capacitances depicted in the figure 1.22 not have to be neglected. The fringe capacitance can be calculated using equation 1.37 or from tabulated values from a process design manual.

$$C_{fringe} \approx \frac{W}{h} + 0.77 + 1.06\left(\frac{W}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5} \tag{1.37}$$

where w is width and t is thickness of a conductive layer, h is height of a conductive layout over the substrate.

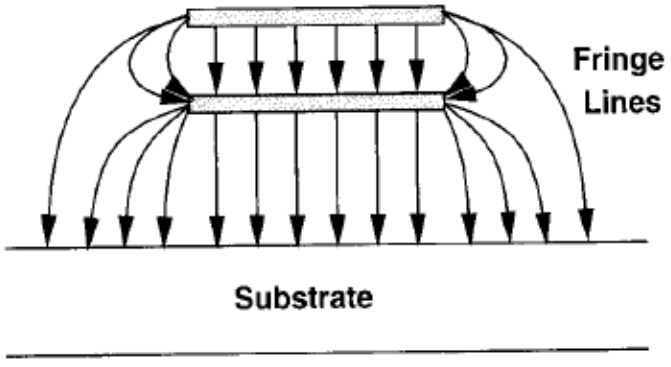

Figure 1.22: Capacitor structures using conductive layers [1]

A MOS capacitor are often also used but voltage dependence limits using of this structure. Also, capacitors must respect symmetry mentioned above for transistors and resistors as in the figure 1.19, dummy devices must be placed on the perimeter of the array. For large capacitors can be used cross-coupling technigues as we do with resistors, but capacitors are more sensitive to wiring capacitance, demanding great care in the interconnection of the units [1].

Chapter 2

Proposed Matched Structures Classifcation Method

The theoretical background behind the mismatch of two or more identically designed devices in analog circuit design has been described in the previous chapter. This chapter is the practical part of this thesis based on an idea of parameter gradient modeling from reference [10]. Parameter gradient modeling is concerned with a systematic part of mismatch which may be effectively eliminated by a proper layout pattern. In order to be able to compare different layout patterns, the parameter gradient modeling, or in other words, the systematic mismatch modeling is an essential part of this work. This chapter describes systematic mismatch modeling and utilization this model for matched structures classification. However, it has to be said that it is not possible to model parameter gradient exactly without a feedback from a manufacturer. Therefore, resulting mismatches in percentages are never the same before and after manufacturing. Nevertheless, it is possible to use a conservative estimation for testing two or more different patterns immunity against to the parameter gradient presented in each manufacturing process. The proposed method works for each type of device, for example, transistors, capacitors and resistors, width to length ratio of MOS transistor is possible to set, unknown position of a pattern on the wafer is considered, different number devices and subdevices can be inserted into evaluated pattern including dummy devices. On the other hand, only systematic mismatches are eliminated by proposed method. Therefore, a designer needs to acknowledge the important layout rules described in the previous chapter when using this method. This chapter is organized as follows. The first section describes the parameter gradient modeling method, the second section is deals with implementation in the Matlab environment and the last section shows orientation in results used for classification of compared patterns.

2.1 Parameter Gradient Modeling

A value of a parameter at location (x, y) can be according to [10] modeled by two-dimensional function $p(x, y)$ assuming that fluctuations of a parameter in z axis have to be small and thus

negligible. This two-dimesional function has not to be known in advance from a manufacturer. This function can be roughly estimated and used for testing matched structures. There can exist linear and non-linear functions of a gradient parameter modeling. Nowadays submicrons processes is mainly a linear parameter gradient presented. Nevertheless, in this work are non-linear gradient up to fifth order considered allowing better evaluating of matched structures.

The two-dimensional function $p(x, y)$ used to model the parameter value that has only linear parameter gradient (1^{st} order) can be according to [10] described as

$$p_1(x, y) = G_1(x, y) + C \tag{2.1}$$

where (x, y) is the location of the point of interest, the position of a device, and C is constant irrespective to (x, y). Constant C represents a nominal value of a device, for example V_{th} of MOS transistor, capacitance of a capacitor or resistance of a resistor. The gradient of a parameter is represented as follows

$$G_1(x, y) = g_{1,0}x + g_{0,1}y \tag{2.2}$$

where $g_{1,0}$ and $g_{0,1}$ are the linear gradient coefficients. Function $G_1(x, y)$ can be further simplified when gradients are same in x and y directions when $g_{1,0} = g_{0,1}$

$$G_1(x, y) = g_{1,0}x + g_{1,0}y = g_{1,0}(x + y). \tag{2.3}$$

For higher order cases can be equation 2.1 easily extended. For n^{th} order gradient resulting in

$$p_n(x, y) = \sum_{i=1}^{n} G_i(x, y) + C \tag{2.4}$$

where

$$G_n(x, y) = \sum_{j=0}^{i} g_{j,i-j}x^j y^{i-j}. \tag{2.5}$$

In this work will be used only gradients up to fifth order, $i = n = [1, 2, 3, 4, 5]$ and gradients coefficients $g_{j,i-j}$ will be same value for each summand signed as a. Equations for individual gradient modeling of particular order can be easily calculated from 2.4. For this case equation 2.4 can be further modified as follows.

$$p_n(x, y) = a \sum_{i=1}^{n} \sum_{j=0}^{i} x^j y^{i-j} + C \tag{2.6}$$

In order to use equation 2.6 for calculation of parameter value at positions (x, y), the gradient inside of the unit cell must be neglected. Normally, the gradient effect inside of the unit cell should be averaged over the area of unit cell. However, the parameter change inside

small area of the unit cell will be small and negligible. Therefore, the parameter value can be represented by only one value at positions (x, y). For a device composed of m unit cells located at $(x_1, y_1)...(x_m, y_m)$, the overall parameter value will be a sum of each individual elements. It can be expressed as

$$P = \sum_{i=1}^{m} p_n(x_i, y_i). \tag{2.7}$$

Now consider simple differential pair layout consists two transistors A and two transistors B shown on the picture 2.1.

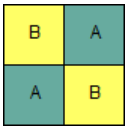

Figure 2.1: Common centroid layout

Ideally, for zero mismatch are values for both considered parameters P_A and P_B identical

$$\Omega = 2\left|\frac{P_A - P_B}{P_A + P_B}\right| 100 = 0. \tag{2.8}$$

In case of not equal number of devices A and B in considered layout topology as for example in the figure 2.2, the normalization a parameter by number of devices 2.9 is required in order to get correct mismatch value from expression 2.8

$$P = \frac{1}{m}\sum_{i=1}^{m} p_n(x_i, y_i). \tag{2.9}$$

In reality, a position of a pattern on the wafer is not known. Therefore, we cannot determine direction of undesirable parameter gradient. As a result, the rotation of a pattern in eight orthogonal directions is implemented in algorithm. These directions are R0, R90, R180, R270, MX, MY, MXR90, MYR90, where R is rotation in degrees and M is mirror belong to the particular axis. Example of rotated pattern is shown in the fiqure 2.3.

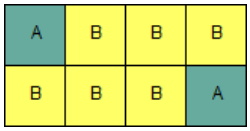

Figure 2.2: Example of structure with not equal number of A and B devices

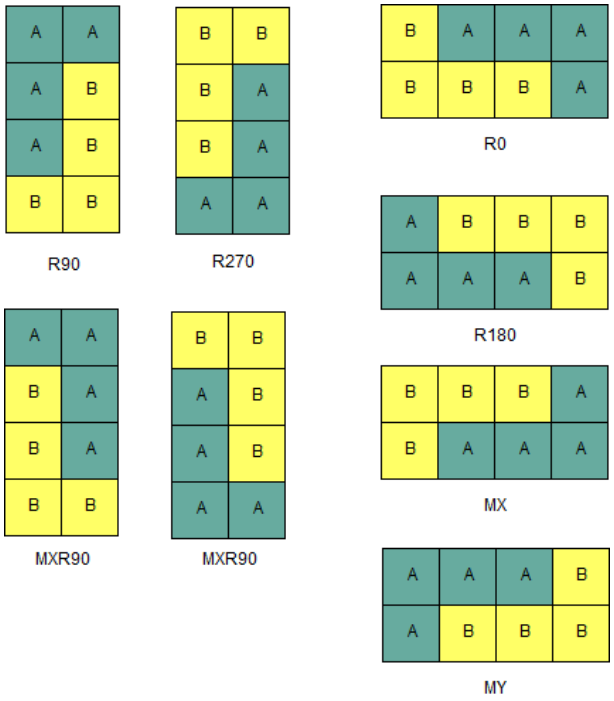

Figure 2.3: Rotation in all orhogonal directions

2.2 Implementation in MATLAB

This section describes implementation of the matched structures classification algorithm in MATLAB software. MATLAB is higher level programming language, has easy to built graphical user interface (GUI) and supports matrix operation, therefore has been selected for implementation. The code realization is mathematically based on equations stated in the previous chapter 2.1. The main purpose of this code is not to calculate exact mismatch values two or more devices because it is not technically possible to know gradient function before fabrication. However, it is possible estimate the gradient by two-dimensional function and use this function for classification of matched structures. In order to get deeper insight to purpose matched structures classification consider three different topologies shown in the figure 2.4. These structures contain eight subdevices of device A and eigth subdevices of device B. Matched devices can be transistors, capacitors, resistors etc. In case of a differential pair design we could be interested in V_{th} or β of MOS devices parameter changes with gradient in x and y direction. Nevertheless, it does not matter what parameter is considered because the main purpose of classification of matched structures is immunity of a structure against to gradient changes, it does not matter if it is V_{th}, β, capacitance or resistance. If we look at three different structures on the picture 2.4, it is hard to say what structure is better. The main purpose of matched structures classification is to sort several structures into chart where the first structure is the best from systematic mismatch point of view.

For calculation the gradient contribution each of devices A and B according to equation 2.6 stated in the previous chapter is necessary to assign (x, y) coordinates to all subdevices in the structure. It can be easily done, for square structures on the figure 2.4, by following MATLAB

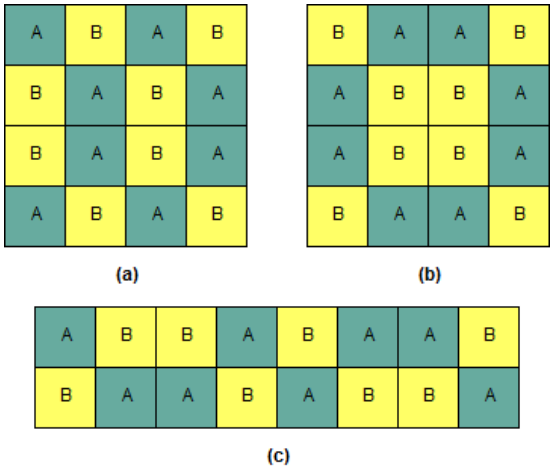

Figure 2.4: Example of structures A and B devices

function:

$$[\mathrm{X},\mathrm{Y}] = \mathrm{meshgrid}\,(0{:}1{:}3\,,0{:}1{:}3\,)$$

where the top left corner of structures in the figure 2.4 corresponds to point $(0,0)$. This point is an initial gradient point where parameter value of the device is equal to a nominal value and thus parameter change due to a parameter gradient is zero. Results from meshgrid MATLAB function for patterns (a, b) in figure 2.4 are the matrices 2.10 and 2.11. Each of subdevices in a structure has unique coordinates. In case of structure (c) in the figure 2.4 will have matrices $\mathbf{X}$ and $\mathbf{Y}$ two rows and eight columns 2.12 and 2.13. These $\mathbf{X}$ and $\mathbf{Y}$ matrices creates the mesh grid for the gradient values calculation on condition that the parameter value within device is neglected as is mentioned in the section 2.1. Distance between individual devices may be selected in microns, but for matched structures classification is not important what units are.

$$\mathbf{X} = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 0 & 1 & 2 & 3 \\ 0 & 1 & 2 & 3 \\ 0 & 1 & 2 & 3 \end{bmatrix} \tag{2.10}$$

$$\mathbf{Y} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 2 & 2 & 2 & 2 \\ 3 & 3 & 3 & 3 \end{bmatrix} \tag{2.11}$$

$$\mathbf{X} = \begin{bmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{bmatrix} \tag{2.12}$$

$$\mathbf{Y} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \tag{2.13}$$

For calculation the parameter value individual subdevices in the grid is used equation 2.6. On the assumption that the gradient coefficient a is 0.001 and nominal value C is equal to 1, the equation 2.6 is modified in the following form

$$p_n(x, y) = 0.001 \sum_{i=1}^{n} \sum_{j=0}^{i} x^j y^{i-j} + 1 \tag{2.14}$$

where x and y are coordinates of individual devices and $i = n = [1, 2, 3, 4, 5]$ because gradients up to fifth order are considered. The following figure 2.5 shows graphically modeled gradient functions up to fourth order. The star symbols represent positions of subdevices A and B in the grid as is depicted in figure 2.4, (a) and (b).

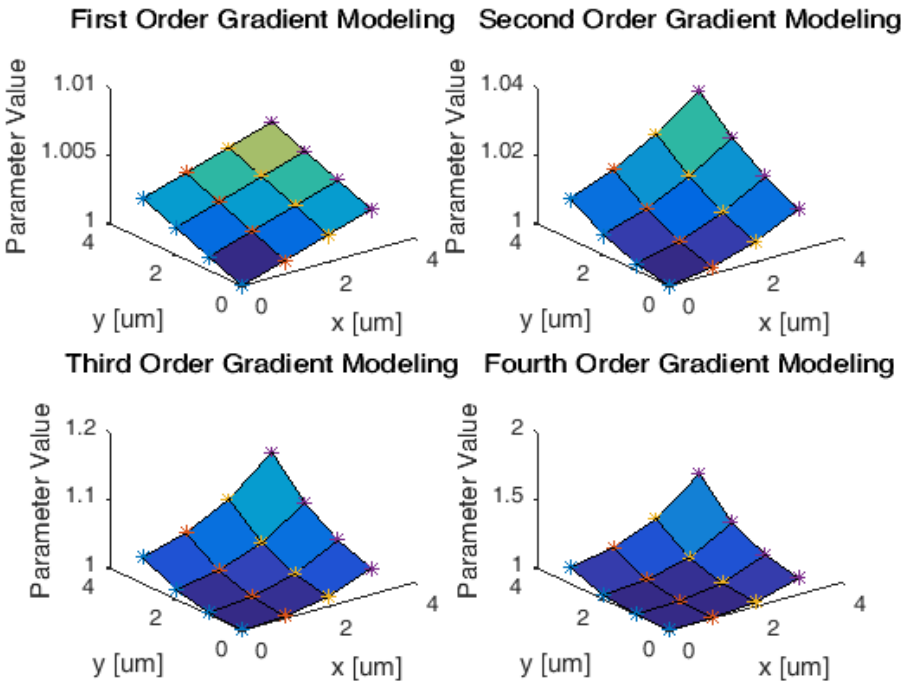

Figure 2.5: Visualization of a parameter gradient modeling

After calculation parameter values of all subdevices are these values summed by the equation 2.7 and normalized by equation 2.9. This procedure is repeated for all gradients orders. In case of structures in figure 2.4 is average parameter value of device A equal to

$$P_A = \frac{1}{8} \sum_{i=1}^{8} p_A(x_i, y_i) \tag{2.15}$$

and for device B

$$P_B = \frac{1}{8}\sum_{i=1}^{8} p_B(x_i, y_i). \tag{2.16}$$

Finally, an estimated mismatch value is calculated with equation 1.1. The block diagram of the proposed method is shown in the figure 2.6.

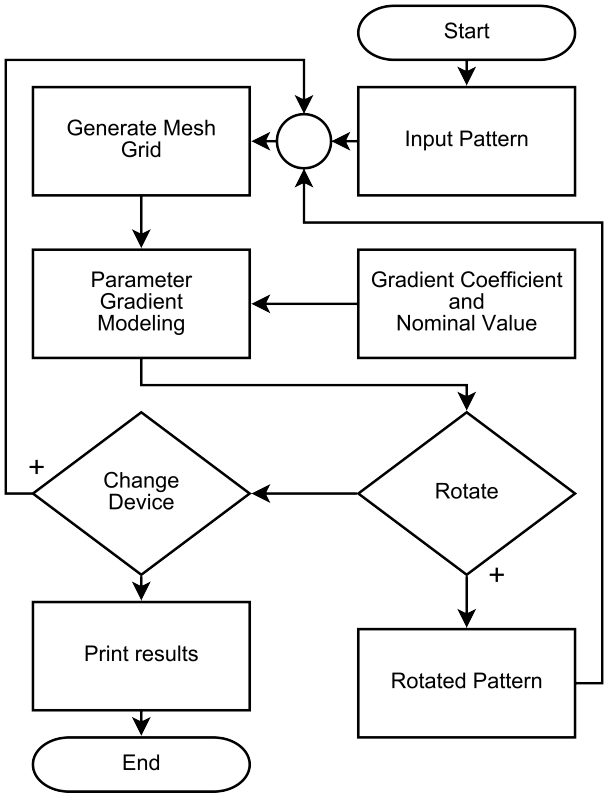

Figure 2.6: Block diagram of the proposed method

An input pattern can be load into the method by two ways. The first is by the Graphical User Interface (GUI) described in the following chapter 2.4. In this case are input data stored in variable *tableData* by following code.

```
tableData = get(handles.uitable2);
assignin('base', 'tableData', tableData.Data);
```

The second approach is to load multiple patterns at one by a text file. The function implementing data load from text file is shown below. This function removes comments and returns matrices of input patterns, W/L and weights separately. Using the text file is more closely described in separate chapter 2.5.

```
function out = load_sparse_data(filename)
fid = fopen(filename,'rt');
temp = textscan(fid, '%s', 'delimiter', '\n');
temp = [temp{:}];
```

```
fclose(fid);

%# remove comments
temp(cellfun('isempty',strfind(temp,'%')));
%# find empty lines
idxSep = find(cellfun(@isempty, temp));
%# separate matrices to different cells
temp2 = mat2cell(temp, diff([0; idxSep; numel(temp)]), 1);
%# remove empty lines
temp2(1:end-1) = cellfun(@(x) x(1:end-1), temp2(1:end-1), '
    UniformOutput',0);
%# convert cell arrays to double
out = cell(size(temp2));
for k = 1:numel(temp2)
        out{k} = cellfun(@str2num, temp2{k}, 'UniformOutput',0);
end
out = cellfun(@cell2mat, out, 'UniformOutput', 0);
out = out(~cellfun('isempty',out));
end
```

Mesh - grid is generated by simple one-row code every time when a new pattern is loaded or rotated. Variable *numC* is number of column of input pattern and *numR* is number of rows of input pattern.

```
[X,Y] =  meshgrid(0:1:numC,0:1:numR)
```

When the mesh grid is generated, a parameter value of individual devices is calculated by modeled parameter gradient modeling function. Following code calculates an estimated parameter gradient value all five orders. Matched devices are selected by variables *SelDevA* and *SelDevB*. The for cycle goes thru all elements in the table *tableData* and if the number of a device is equal to selected device, the parameter value of particular gradient order is calculated. The variable C is nominal value of a device.

```
for j = 1:5
for i=1:numOfElements
    if tableData(i)==SelDevA
        pA1(1,j) = pA1(1,j) + parameter1(X(i),Y(i),a,j) + C;
        numOfDevA = numOfDevA + 1;
    elseif tableData(i)==SelDevB
        pB1(1,j) = pB1(1,j) + parameter1(X(i),Y(i),a,j) + C;
        numOfDevB = numOfDevB + 1;
    else
        display('incorrect array elements');
```

```
    end
end
```

The function *parameter*1 contains modeled two-dimensional functions according equation 2.6. Code for *parameter*1 function is shown below. Parameters of this function are coordinates x and y, gradient coefficient a and variable o drives the switch.

```
function p = parameter1(x, y, a, o)

switch(o)
    case 1
        p = a(1)*(x^0*y^1 + x^1*y^0);
    case 2
        p = a(1)*(x^0*y^1 + x^1*y^0) + a(2)*(x^0*y^2 + x^1*y^1 + x^2*
            y^0);
    case 3
        p = a(1)*(x^0*y^1 + x^1*y^0) + a(2)*(x^0*y^2 + x^1*y^1 + x^2*
            y^0) + a(3)*(x^0*y^3 + x^1*y^2 + x^2*y^1 + x^3*y^0);
    case 4
        p = a(1)*(x^0*y^1 + x^1*y^0) + a(2)*(x^0*y^2 + x^1*y^1 + x^2*
            y^0) + a(3)*(x^0*y^3 + x^1*y^2 + x^2*y^1 + x^3*y^0) + a(4)
            *(x^0*y^4 + x^1*y^3 + x^2*y^2 + x^3*y^1 + x^4*y^0);
    case 5
        p = a(1)*(x^0*y^1 + x^1*y^0) + a(2)*(x^0*y^2 + x^1*y^1 + x^2*
            y^0) + a(3)*(x^0*y^3 + x^1*y^2 + x^2*y^1 + x^3*y^0) + a(4)
            *(x^0*y^4 + x^1*y^3 + x^2*y^2 + x^3*y^1 + x^4*y^0) + a(5)
            *(x^0*y^5 + x^1*y^4 + x^2*y^3 + x^3*y^2 + x^4*y^1 + x^5*y
            ^0);
end
end
```

A parameter values are then multiplied by eight orders and converted from double to integer because of limited computation accuracy of floating point format. There is also needed divide the result by number of devices according equation 2.9. Finally, the mismatch is calculated according equation 2.8.

```
pA1(1,j) = round((pA1(1,j)/numOfDevA)*10^8);
pB1(1,j) = round((pB1(1,j)/numOfDevB)*10^8);
omega(1,j) = 2*abs((pA1(1,j)-pB1(1,j))/(pA1(1,j)+pB1(1,j)))*100
```

The rotation is performed in the Matlab very easy. For rotation by 90° is used following command. For rotation 270° is simple this command three times repeated. Mirroring along x-axis is performed by *fliplr* command and mirroring along y-axis by *flipud* command.

```
R90 = rot90(pattern);
MX = fliplr(pattern);
MY = flipud(pattern);
```

Results printing in the GUI is handled by following command. There are needed a number to string conversion functions as well.

```
set(handles.textMyOutput, 'String', strwr);
```

In case of writing output data from the method into matching.log file is *diary* function used. The *diary* function writes between on and off states a text from MATLAB command window into the text file with name *matching.log*.

```
diary on
diary('matching.log');
disp('
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%'
    )
disp('Matched Structures Classification Algorithm')
disp('Designed by Pavel Vancura, CTU in Prague in cooperation with ')
disp('ST Microelectronics, Vlatimil Kote, Patrik Vacula, Adam Kubacak
     and Jiri Jakovenko')
disp('Version 1.0')
disp('20.12.2016')
disp('
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%'
    )
disp('Input Data')
disp('First is pattern followed by W/L and desired weights')
for i=1:dataSize
data{i}
end
disp('Parameters of Gradient Function')
disp('Gradient Coeffcient:')
a
disp('Nominal Value')
C
disp('Worse Case Mismatches for patterns A ... X [%]')
worsedir
disp('Worse Case Directions')
dir
disp('Evaluation Vectors for patterns A ... X [%]')
EV
```

```
diary off
```

Above mentioned parts of the proposed method algorithm code describes the most important fragments. The code itself contains hundreds lines supporting command which holds the whole algorithm together. However, these code lines are not important for method itself and thus is not needed explain here each line of this code.

2.3 Results Representation

The table 2.1 shows simulation results based on algorithm in matlab described in previous sections 2.1 and 2.2. Compared structures are these in the figure 2.4. All of these structures contains eight subdevices of device A and eigth subdevices of device B, it can be for example layout of a differential pair. According simulation results the best topology is, as expected, the structure in the figure 2.4 (b) with zero mismatch at first three orders and lowest mismatch at fourth and fifth orders. Zero values at first three orders are fully in agreement with the reference [10]. In this simple case with some layout design skills it is easy to determine what topology is better. On the other hand, in case of more complex topologies it is not easy to find better structure from mismatch point of view, it is main purpose of the proposed matched structures classification algorithm. In the first step, results at first order gradient are compared. If are values two or more structures zero at first order gradient then are compared values at second order gradient and so on up to fifth order. When values at the same order gradient differs, the value closer to zero win and better pattern can be detected. All patterns are classified in all eight orthogonal directions. These patterns are in this case very symmetrical, therefore values are in all orthogonal directions the same.

Table 2.1: Classification of matched structures in fig. 2.4

Pattern	Direction	Matching	Estimated Systematic Mismatch [%]				
			1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
2.4 **b**	R0, R90, R180, R270, MX, MY, MXR90, MYR90	A to B	0	0	0	0.177	1.43
2.4 **c**	R0, R90, R180, R270, MX, MY, MXR90, MYR90	A to B	0	0	0	0.338	1.67
2.4 **a**	R0, R90, R180, R270, MX, MY, MXR90, MYR90	A to B	0	0	0.096	0.753	3.42

The previous example can be applied to a differential pair layout design or when are the same number of A and B devices used. However, in the analog circuit design are frequently used patterns containing more than two devices and large number of subdevices. The current mirror layout depicted in the figure 2.8 is good example of this type of structure. Circuit diagram is shown in the figure 2.7 where current I_b is in the ideal case approximately equal to I_{ref} and current I_c is $2I_{ref}$. The transistor Q_1 is device A in the structure with $W/L = 1$ as well as device B (Q_2). Device C is transistor Q_3 with $W/L = 2$.

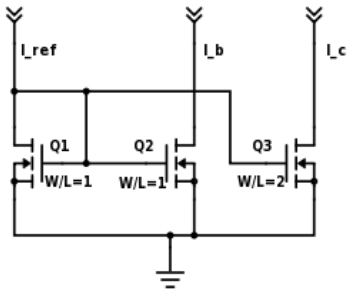

Figure 2.7: Multiple current mirror schematic

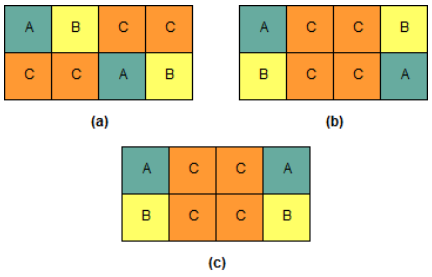

Figure 2.8: Example of multiple current mirror structures

Simulation results of structure depicted in figure 2.8 shows the table 2.2. The structure in the figure 2.8 (c) have poorer matching with compare to structures 2.8 (a) and 2.8 (b). The structure 2.8 (b) have better matching of device A to B than structure 2.8 (a). On other hand, the structure 2.8 (a) have better matching of device A to C. In this case it depends on an application if is more important to be more accurate current I_b or I_c.

2.3.1 Evaluation Vector

Apparently, results from matched structures classification algorithm in table 2.2 are not at first glance easy to understand. The purpose of the evaluation vector is to colligate matching's in a pattern to one vector containing only five numbers. Each of number corresponds to particular gradient order. Working principle of evaluation vector can be shown on classified patterns in the table 2.2 corresponds to figure 2.8. There are classified three different patterns with devices A, B and C. Two mismatches are evaluated, A to B and A to C in all orthogonal directions. Some directions gives the same results, therefore only four outputs for patterns 2.8 (a) and 2.8 (c)

Table 2.2: Classification matched structures in fig. 2.8

Pattern	Direction	Matching	Estimated Systematic Mismatch [%]				
			1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
2.8 **b**	R0, R180, MXR90,MYR90	A to B	**0**	**0.223**	**1.21**	**4.41**	**13.3**
		A to C	**0**	**0.241**	**1.42**	**5.57**	**17.9**
	R90, R270, MY, MX	A to B	0	0.149	0.732	2.51	7.09
		A to C	0	0.124	0.811	3.45	11.9
2.8 **a**	R0, MXR90	A to B	**0.099**	**0.447**	**1.71**	**5.95**	**18.3**
		A to C	0.049	0.124	0.371	1.35	4.88
	R90, MX	A to B	0.099	0.447	1.53	4.8	14.2
		A to C	0.049	0.124	0.269	0.705	2.12
	R180, MYR90	A to B	0.099	0.447	1.71	5.95	18.3
		A to C	**0.049**	**0.332**	**1.34**	**4.59**	**13.5**
	R270, MY	A to B	0.099	0.447	1.53	4.8	14.2
		A to C	0.049	0.323	1.26	4.09	12.1
2.8 **c**	R0, R90, MX,MXR90	A to B	**0.099**	**0.347**	**1.02**	**2.88**	**7.49**
		A to C	0.049	0.023	0.664	3.26	11.6
	R180, R270, MY, MY90	A to B	0.099	0.347	1.02	2.88	7.49
		A to C	**0.049**	**0.372**	**1.69**	**6.14**	**19.1**

are obtained. The pattern 2.8 (a) is less symmetric and therefore eight outputs are obtained. In the extreme case for matching A to B and A to C is sixteen outputs obtained. The first step in computation of evaluation vector is select one of orthogonal direction with the highest values - the worse case matching. This worse case matching is used as a representative result for particular matching. Therefore, only two outputs for matching's A to B and A to C instead of sixteen is obtained. The second step in computation of evaluation vector is weighting individual matching's. Actually, in a circuit design is very often one of matching's more important than another one. In case of current mirror circuit on the picture 2.7 can be matching A to B (current I_b) more important than matching A to C (current I_c). Let's assume that current I_b is most important with weight equal to 1 and current I_c have half importance with weight 2. The weight higher than 1 have lower importance because reciprocal value in computation is used. The evaluation vector is computed as follows.

After selection of a worse case matching are reciprocal values of weights calculated,

$$W_{ri} = \frac{1}{W_i} \tag{2.17}$$

where W_i is weigth of i_{th} device to the reference device A. Next the worse case directions of individual matchig's are multiplied by corresponding weighs,

$$\vec{M_{wi}} = \vec{M_i} W_{ri} \tag{2.18}$$

where $\vec{M_i} = [m_1, m_2, m_3, m_4, m_5]$ is one row matrix of mismatch particular device to device A containing five mathing numbers corresponding to particular gradient order. After weighting all

matching's orders are summed and divided by number of weighs,

$$E\vec{V} = \frac{\sum_{i=1}^{n} \vec{M_{wi}}}{dim(\vec{W})} \tag{2.19}$$

where $E\vec{V} = [ev_1, ev_2, ev_3, ev_4, ev_5]$ is the evaluation vector characterizing all mathing's in a pattern (A to B, A to C, ...,A to n) by only using five numbers. Evaluation vector highly reduce amount results from the algorithm and simplifies result representation. Therefore, a user can easily determine a better classified pattern. Lower numbers $ev_1..ev_5$ means better result.

Example of using evaluation vector will be good shown at above evaluated patterns of current mirror structures in figures 2.8 and 2.7. The table 2.2 is at first glance very large. The first reduction of data is by selection worse case directions for each device and each pattern. Worse case directions are in the table 2.2 boldfaced and again shown in the following table 2.3.

Table 2.3: Worse case directions table of structures classification in figure 2.8

Pattern	Direction	Matching of device	Estimated Systematic Mismatch [%]				
			1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
2.8 **b**	R0, R180, MX90, MX90	A to B	**0**	**0.223**	**1.21**	**4.41**	**13.3**
		A to C	**0**	**0.241**	**1.42**	**5.57**	**17.9**
2.8 **a**	R0, MX90	A to B	**0.099**	**0.447**	**1.71**	**5.95**	**18.3**
	R180, MYR90	A to C	**0.049**	**0.332**	**1.34**	**4.59**	**13.5**
2.8 **c**	R0, R90, MX, MX90	A to B	**0.099**	**0.347**	**1.02**	**2.88**	**7.49**
	R180, R270, MY, MY90	A to C	**0.049**	**0.372**	**1.69**	**6.14**	**19.1**

After worse cases selection, weights are specified. Let's say, matching A to B has weight 1 (most important) and matching A to C has weight 2 (less important). Then are reciprocal values computed according equation 2.17 and individual rows of the table 2.3 are weighted by the particular weight according equation 2.18. Finally, are individual matching's of each pattern summed and divided by the number of weights, by factor two in this case. Computed evaluation vectors are shown in the table 2.4.

Table 2.4: Evaluation vectors of patterns in the figure 2.8

Pattern	Values of Evaluation Vector [%]				
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
2.8 **b**	**0**	**0.14**	**0.75**	**2.74**	**8.26**
2.8 **c**	**0.06**	**0.26**	**0.93**	**2.97**	**8.52**
2.8 **a**	**0.06**	**0.3**	**1.19**	**4.12**	**12.55**

At first glance, the table 2.4 shows significant reduction of data and results are now more understandable. Futhermore, by evaluation vector is possible to build in the fact of different importance of individual matchings. As expected, the pattern 2.8 (b) has the best matching,

followed by 2.8 (c) and worse matching has pattern 2.8 (a). These results are valid for above mentioned weights 1 and 2.

2.4 Graphical User Interface

Two possible ways are possible for input data, extraction results and settings. The first is the graphical user interface (GUI) discussed in this section. The second approach is to use a text file for input data and settings and an output text file for results representation. Reading input data from text file allows calculation multiple patterns at once, it will be discuss in the following section in more detail. The GUI, in the figure 2.9, on the other hand, allows only one pattern evaluation at a time.

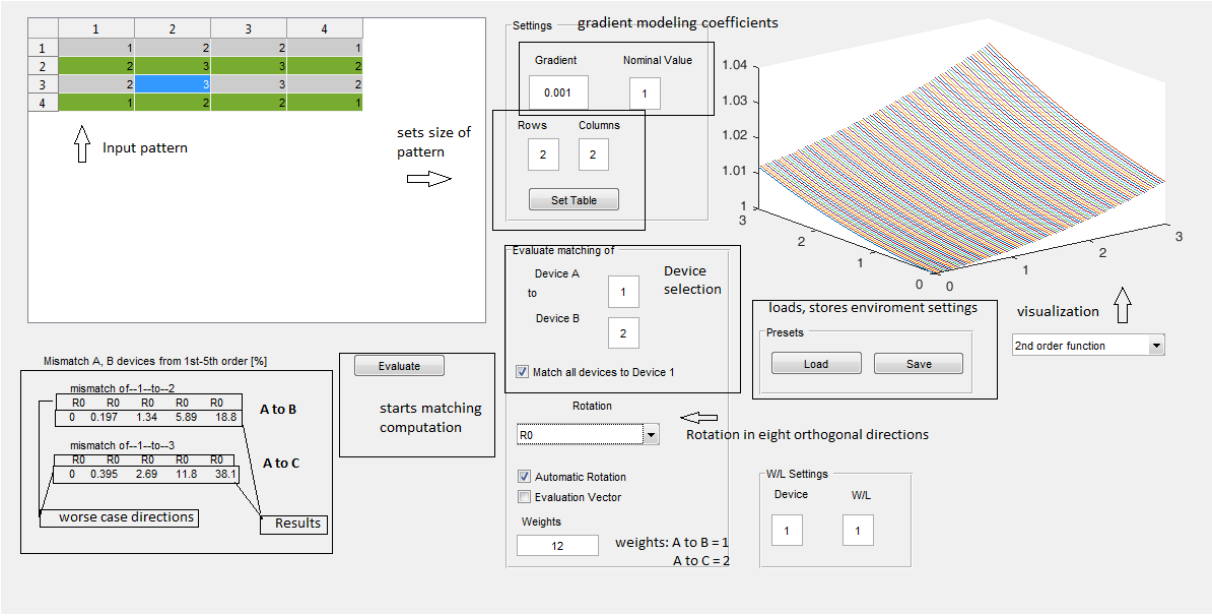

Figure 2.9: Graphical User Interface

GUI features are shortly described in the table 2.5. The gradient parameter modeling function, described in the section 2.1, is shaped by Gradient and Nominal Value constants. Gradient constant have to be much smaller than Nominal Value in order to get reasonable results. A size of the table in the upper left corner in the figure 2.9 is set by Rows and Columns constants and using Set Table button. The table is editable and accepts device numbers from 1 to n. The GUI, in compare to the text file input method, offers possibility to select the reference device by Device A and matched device by Device B. In the text file method is the reference device every time the Device A. If the Match of all devices to device 1 option is enabled, mismatches of all presented devices in a pattern are computed. In the Rotation section is possible to select rotation of the pattern in all orthogonal directions, or the pattern is rotated automatically by enabling the Automatic Rotation option and the worse case direction mismatch is automatically plotted in the bottom left GUI corner. If Evaluation Vector is enabled, the Weighs field becomes active. A number inserted to this field has to be $n-1$ digits, where n is number of devices in

the table. Individual digits means weighs of individual mismatches. For example, the number 112 means that mismatch A to B and A to C has weigh 1 and A to D has weigh 2. The weight 1 has higher priority.

Table 2.5: GUI features description

feature	**description**	**Note**
Input Pattern	inserts a input pattern, Device A = 1, Device B = 2 ..	
Gradient	sets the gradient coefficient a of gradient modeling function eqv. 2.6	reasonable value is $a << C$
Nominal Value	sets the nominal value C of a device in gradient modeling function eqv. 2.6	reasonable value is $C >> a$
Rows, Columns, Set Table	input pattern size settings	
Device A, Device B	selects a device for matching evaluation	
Match all devices to Device 1	computes matching of all devices to device A = 1 at once	
Load, Save	stores and loads presets	
Rotation	allows to rotate pattern in the one of eight orhogonal direction	
Automatic Rotation	automatically rotates an input pattern in all direction and selects a direction with worse case matching	
Evaluation Vector	enables evaluation vector computation	
Weights	sets weights for mathing of individual devices	i.e. 112 means that Device A a B have weight 1 and C has weight 2
Visualization	visualizates the modeled two dimensional function	
W/L settings	selects device and corresponding W/L settings	
Evaluate	starts matching computation	

2.5 Input Data Loading by the Text File

Another option how to load input data into proposed method is by text file. The main benefit is loading multiple patterns at once. If input data are successfully read, the method calculates evaluation vectors. These evaluation vectors and intermediate results are then written into another text file named matching.log. The input text file may be generated by the Cadance

layout editor using a SKILL function. Input file organization of patterns in the figure 2.8 is shown below.

```
%%%%%%%%%%%%%% Input Text File %%%%%%%%%%%%%%
%
% the first pattern

1,2,3,3
3,3,1,2

% W/L of individual devices

1,1,1

% weights

1,2

% second pattern

1,3,3,2
2,3,3,1

1,1,1

1,2

% third pattern

1,3,3,1
2,3,3,2

1,1,1

1,2
```

The text behind the % character is interpreted as a comment. After initial comments follows an empty line and then the first pattern. Individual elements of a pattern in a row are separated by commas and a new pattern's row is at a new line. After the first pattern follows empty line and W/L settings, or a comment finished by empty line and then W/L settings. W/L values always corresponds with a number of devices and are placed in one row separated by commas.

Finally, the weights are placed in the same manner as W/L values. Number of weights is always $n-1$ where n is number of devices in a pattern. Then is either end of the input file, or a next pattern follows in the same (pattern - empty line - W/L - empty line - weights) manner.

The output text file named matching.log is shown below. On the top of file are input patterns followed by W/L and desired weights respectively. Notice, the patterns belongs those in the figure 2.8. After input patterns are in the output file parameters of the modeled gradient function, namely the gradient coefficient a and the nominal value C. These variable are set in the top of code. Then follows the mismatch data of device A to B and A to C in worse case direction of all three patterns. Finally, are results of evaluation vectors shown. Notice, evaluation vectors values corresponds with the table 2.4.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Matched Structures Classification Algorithm
Designed by Pavel Vancura, CTU in Prague in cooperation with
ST Microelectronics
Version 1.0
18.5.2017
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Input Data
%First pattern followed by W/L and desired weights

    1     2     3     3
    3     3     1     2

    1     1     1

    1     2


%Second pattern followed by W/L and desired weights

    1     3     3     2
    2     3     3     1

    1     1     1

    1     2


%Third pattern followed by W/L and desired weights
```

```
     1     3     3     1
     2     3     3     2

     1     1     1


     1     2

%Parameters of Gradient Function
%Gradient Coeffcient:

a =

   1.0000e-03

%Nominal Value

C =

     1

%Worse Case Mismatches for patterns A ... X [%]

worsedir(:,:,1) =

    0.0998    0.4468    1.7136    5.9462   18.3455
    0.0499    0.3225    1.3439    4.5945   13.4954


worsedir(:,:,2) =

         0    0.1488    0.7319    2.5105    7.0876
         0    0.2731    1.5432    5.9574   18.9020


worsedir(:,:,3) =

    0.0998    0.3473    1.0246    2.8824    7.4949
    0.0499    0.3722    1.6889    6.1408   19.0968
```

```
Worse Case Directions

dir =

    'R0'    'R180'
    'R0'    'R0'
    'R0'    'R180'

%Evaluation Vectors for patterns A ... X [%]

EV =

    0.0624    0.3040    1.1928    4.1217   12.5466
         0    0.1427    0.7517    2.7446    8.2693
    0.0624    0.2667    0.9345    2.9764    8.5216
```

Chapter 3

Layout examples

The proposed method described in the chapter 2 is appropriate mainly for large patterns consisting of more than two devices and a large amount of subdevices. In the case of matching two transistors in a simple differential pair it usually is possible to use a common patterns as for instance in the figures 2.4 b and c. These simple patterns are able to eliminate higher orders parameter gradients [10]. In this chapter two layout examples will be shown in a design of charge redistribution successive approximation register (SAR) analog to digital converter (ADC) in 180 nm CMOS process. The charge redistribution SAR ADC contains a capacitive digital to analog converter (CDAC) and a comparator where is a good matching required. However, the CDAC suffers from parasitic capacitances precluding the use of sophisticated matched structures due to difficult interconnects. On the other hand, the comparator uses rather simpler patterns and therefore a common structures can be used. After all, the larger patterns will be shown where the proposed method has been used.

3.1 Charge Redistribution SAR ADC Design Problems

The simplified block diagram of charge redistribution SAR ADC with a split capacitor array is depicted on the figure 3.1. The split capacitor array needs only 63 capacitors in contrast to a regular 10-bit capacitor array which needs 1024 capacitors [11]. It is considerable saving of a silicon area. On the other hand, the split capacitor array has disadvantage that the split capacitor C_5 in the figure 3.1 needs to have the very exact value $\frac{32}{31}C_u$. Where C_u is the unit capacitor value, in this case 106 fF, 10x10 μm MIM capacitor [1]. Also, other capacitors needs to be exact as well, in order to have a regular voltage step on the comparator input and keep low integral and differential errors. If a voltage reference is 1.024 V, then the voltage step is $1.024/2^{10}$ thus 1 mV, which is very small value indeed. Ideally, an error should be less then 1/2 LSB. This error will strongly depends on parasitic capacitances and a proper layout. The capacitive array has three modes of operation, sampling mode, hold mode, and charge redistribution mode. Theory of the charge redistribution SAR ADC operation is greatly

[1] Metal Insulator Metal capacitor has high capacitance density per area

described in the reference [12]. Apart from CDAC, the SAR ADC contains the comparator block and the SAR logic. The comparator offset is the second stumbling block in the SAR ADC design, it strongly depends on a proper layout and good circuit design. The comparator contains the digital calibration in order to reduce offset even more. The following sections will be dedicated to CDAC and the comparator layout with considering matched structures.

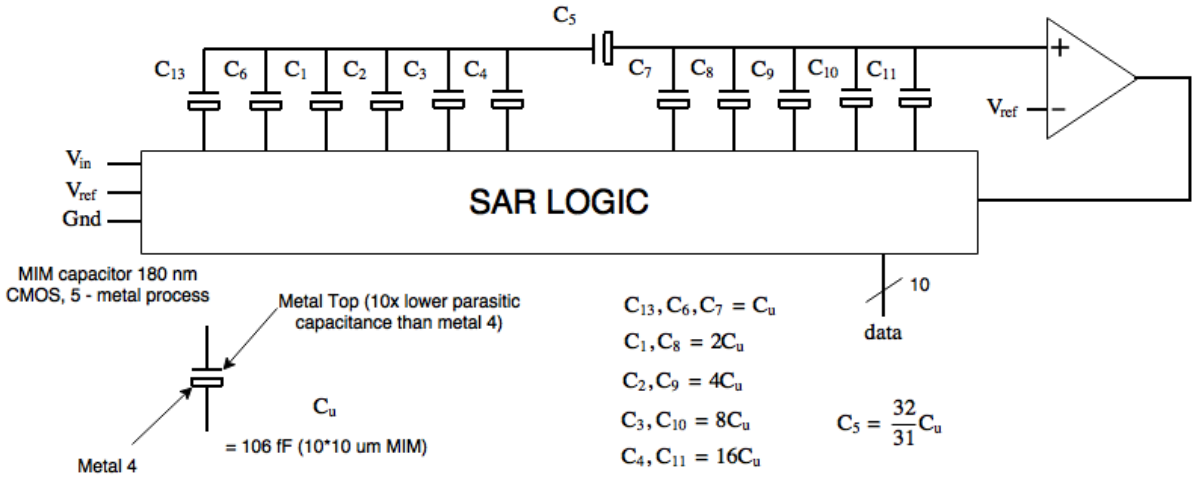

Figure 3.1: Charge redistribution SAR ADC block diagram

3.2 Capacitive DAC layout design

The SAR ADC has been designed in 0.18 micron high voltage SOI [2] CMOS six metal technology. This technology is specially designed for medical, industrial and automotive applications. High voltage support up to 200V, -40 to 175 °C temperature range. High capacitance single, double, triple MIM and Sandwich MIM are Capacitors are available. In the capacitive DAC design has been used 10x10 microns single MIM capacitor with capacitance 106 fF.

The CDAC has to have dimensions maximally 60x250 μm, to be conform with specification. Therefore, the 4x17 MIM capacitor array will be used, totally 63 MIMs for CDAC and 5 dummy MIMs. Each MIM has dimension 10x10 μm with capacitance 106 fF. In the 180 nm CMOS process is the MIM capacitor top plate connected to the metal TOP and the bottom plate is connected to the metal 4. Very important is notice that metal 4 has approximately 10x higher parasitic capacitance than the metal TOP. As a result, the right connection of MIM capacitors is required as is shown in the figure 3.1. Following figures depicts proposed capacitor layout topologies. These pattern were classified by the proposed method described in the 2. The first, depicted in the figure 3.2 uses quite sophisticated matched structures. Dummy devices are surrounded around the pattern. These dummy devices are added in order to reduce etching error.

The second concept depicted in the figure 3.3 uses simplified matched structures concept allowing easier interconnects.

[2] Silicon on Instulator, layered silicon insulator silicon substrate

Figure 3.2: The first concept of the CDAC layout

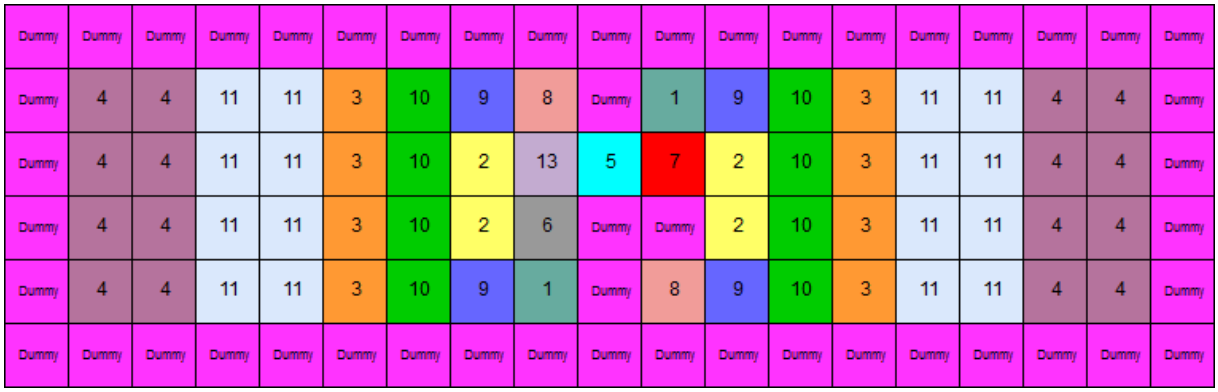

Figure 3.3: The second concept of the CDAC layout

The third approach, in the figure 3.4, uses no matched structures allowing very simple interconnection within the CDAC which very considerably decreases influence of parasitic capacitances. However, systematic mismatch in this case is not eliminated.

Figure 3.4: The third concept of the CDAC layout

Above depicted patterns have been classified by the proposed method in the chapter 2, evaluation vectors are shown in the table 3.1. Weighs of individual capacitors were set to one, evenly important. The reference device is always the device with the number one. Matching other devices is then calculated to this reference device and evaluation vector is computed.

The table 3.1 discovers important fact that patterns in the figure 3.2 and 3.3 have similar

Table 3.1: Evaluation vectors of CDAC arrays

Pattern Type	Values of Evaluation Vector [%]				
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
figure 3.2	0.04	1.59	17.79	49.91	71.59
figure 3.3	0.04	1.59	17.61	49.12	70.46
figure 3.4	0.24	4.63	33.67	74.52	96.97

matching results. The evaluation vector of pattern in the figure 3.4 has much worse values in compare with both counterparts, however interconnections between unit capacitors is very easy. Interconnections between unit capacitors needs to be as simple as possible because parasitic capacitances between metals incredibly increases integral and differential errors. Consequently, the pattern concept in the figure 3.3 is a good compromise between eliminating the systematic mismatch and keeping parasitic capacitances in a moderate level. Interconnections in the pattern 3.3 are still good feasible. This fact is easily discovered by the proposed method. Example of layout design of the capacitor array in SAR ADC is shown in the figure 3.5.

Figure 3.5: Example of capacitor array layout design

3.3 Comparator Layout Design

The comparator design for charge redistribution SAR ADC purposes needs to have a minimum offset. An offset value will depends on the circuit design, a offset cancelation method and on a transistor mismatch respectively. The last named occasion will be discussed in this section.

In the figure 3.6 a buffer circuit diagram is depicted. The buffer serves in the comparator circuitry as an isolation between the main comparator circuit and the capacitor array in order to avoid a charge injection into capacitor array. Between transistors in red frames, a low mismatch is required. These transistors are usually divided to 4,8 or 16 smaller subdevices connected in parallel and placed into a matched pattern.

Transistors M21 a M22 have W/L=25/0.72. They are divided by factor 8 with W/L ratio equal to 3.125/0.72 and connected in parallel. The pattern able to eliminate a parameter gradient up to third order depicted in the figure 3.7 is used [10]. This pattern has excellent matching characteristics calculated by proposed method described in the chapter 2. Estimated mismatch values in the table 3.2 are demonstrated. These values are fully in agreement in the reference

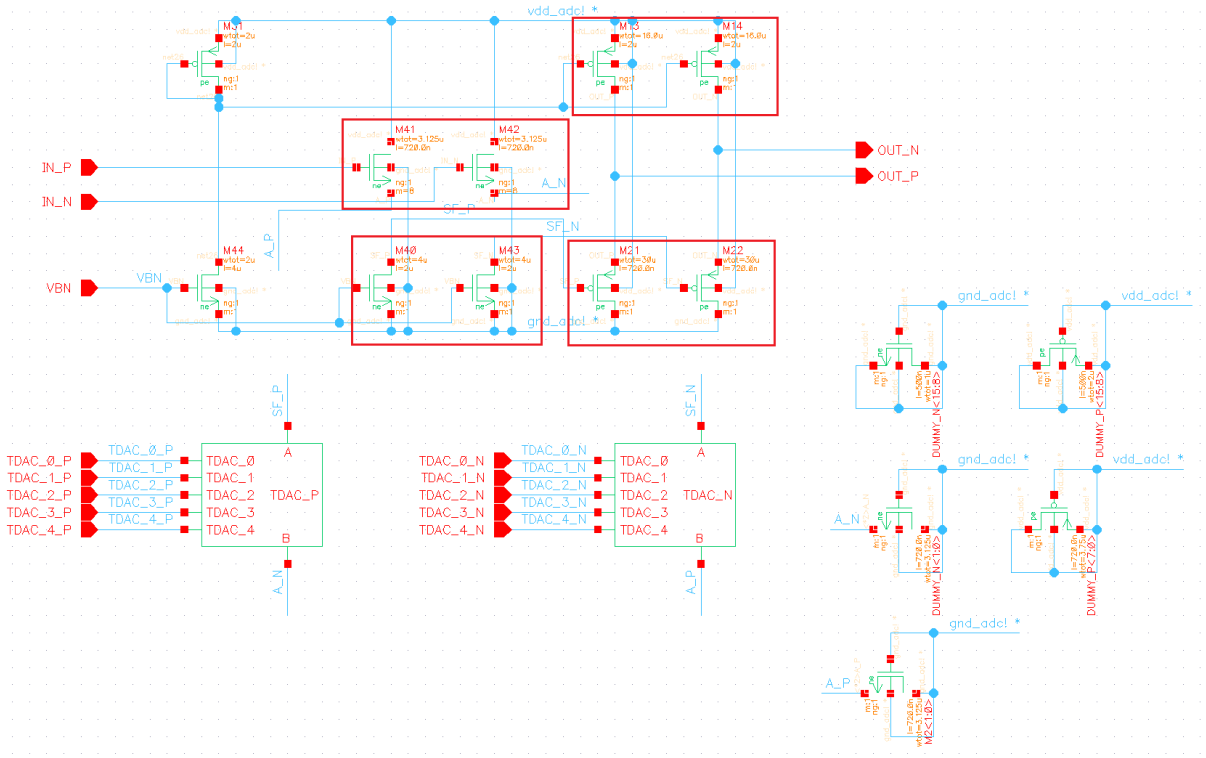

Figure 3.6: The buffer circuit design

[10].

B	A	A	B
A	B	B	A
A	B	B	A
B	A	A	B

Figure 3.7: The third order pattern eliminating higher orders parameter gradient

Two ways of realization the pattern in the figure 3.7 are shown in figures 3.8 and 3.9 respectively. The later one in the figure 3.9 is interdigitated layout and can be better for realization o smaller patterns as described in section 1.3.2. However, difference between these layouts is speculative.

Table 3.2: Estimated mismatch values of the third order pattern computed by the proposed method

pattern type	gradient order [%]				
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
figure 3.7	0	0	0	0.17	1.43

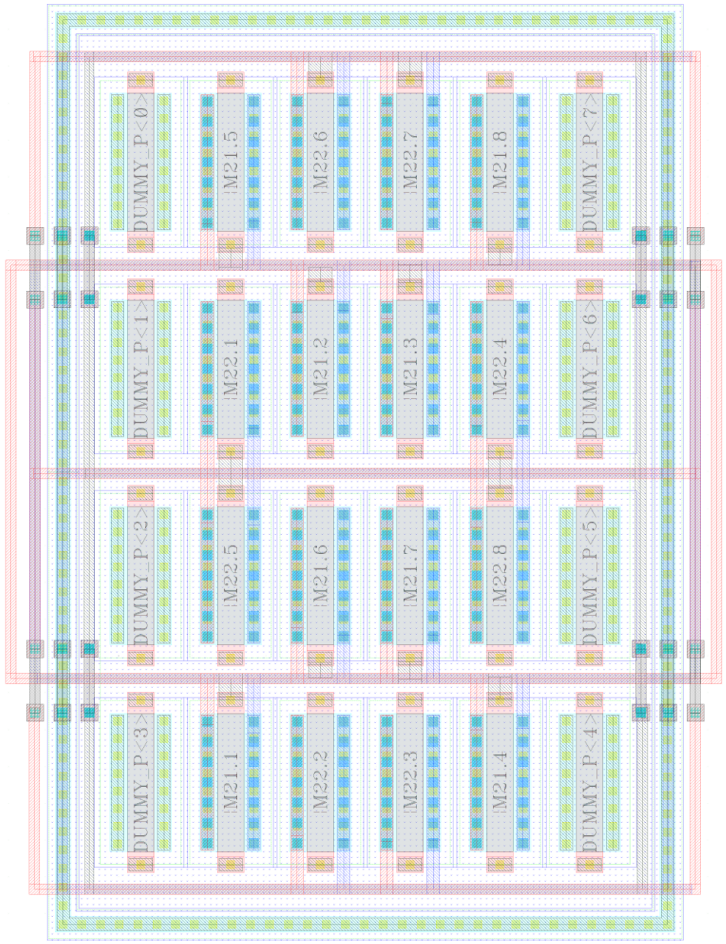

Figure 3.8: Layout of the third order pattern in the figure 3.7

The overall comparator schematic including digital offset compensation and the buffer in the figure 3.6 is shown in the figure 3.10. Here again is a good matching between transistors in red frames required. Matched structures are in this case very similar those in figures 3.8 and 3.9. Patterns of these matched structures are used from reference [10]. The complete layout of the comparator design is shown in the figure 3.11. The top of layout contains patterns of matched transistors in red frames depicted on previous figures and the bottom part is stacked by the digital calibration.

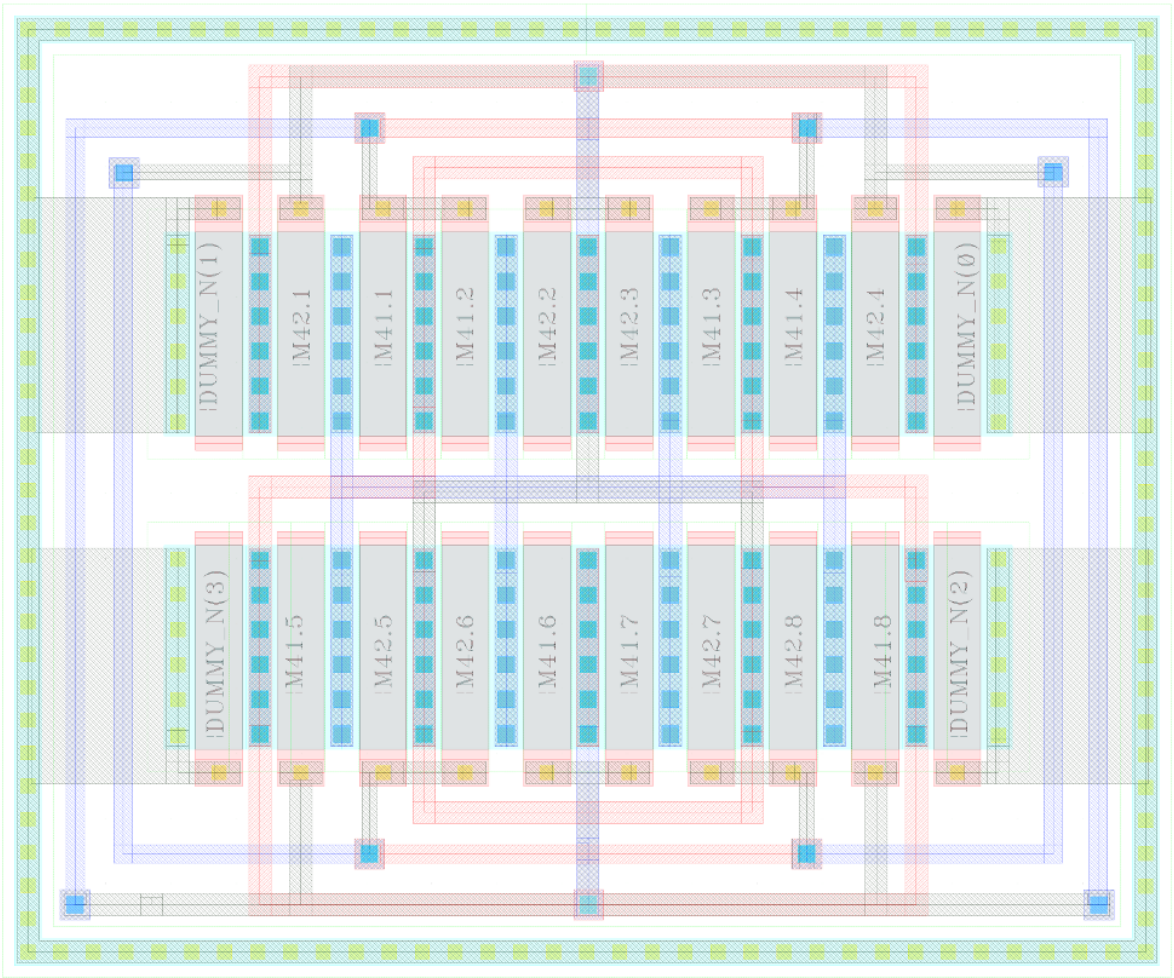

Figure 3.9: The interdigitated layout of the third order pattern in the figure 3.7

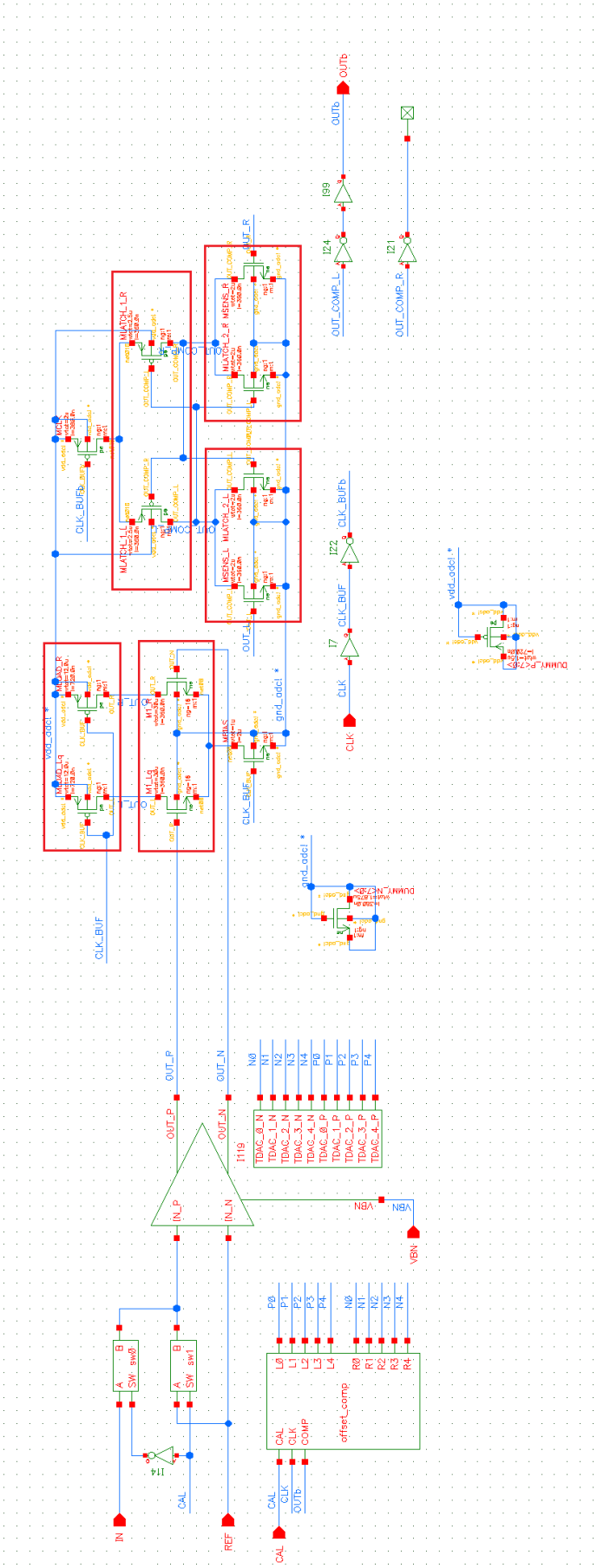

Figure 3.10: Comparator circuit schematic

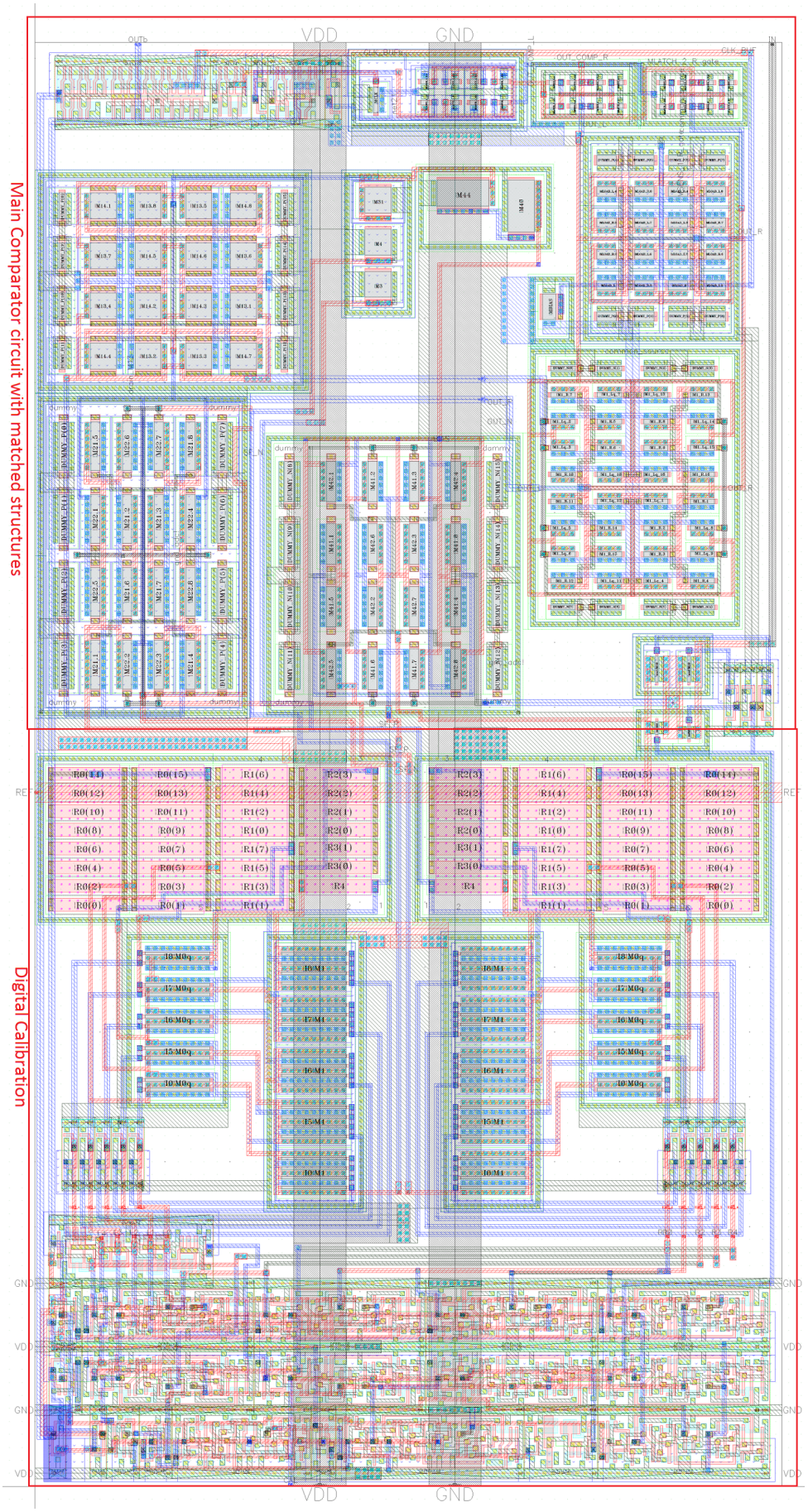

Figure 3.11: Comparator layout

Conclusion

The major objective of this thesis was to develop a method able to compare and classify different matched layout patterns. Compared layout structures always contains the same number of devices and subdevices but with a various arrangement in a structure. Therefore, first of all a different layout patterns needs to be designed and then the proposed method is used to sort out the best pattern with the highest immunity against to the systematic mismatch described in the first chapter. In order to be complete in the task of analog devices mismatch, the random mismatch theory with practical examples describing briefly how to solve a stochastic event in an analog design is analyzed in the first part of the thesis as well. Further proposed method requirements were implemented W/L settings, include dummy devices and take into account an unknown position on the wafer. The proposed method is usable for both active and passive devices. All requirements have been successfully implemented.

The main idea behind the proposed method is to model a parameter gradient caused by the systematic mismatch by the two-dimensional polynomial function. A parameter gradients in the z-axis and within a device area are neglected. Individual devices are placed in the mesh grid and the values of the modeled parameter gradient are calculated. The mathematical background is described in the second chapter. For input data loading for a single pattern the graphical user interface can be used. For loading multiple patterns at once it is better to use an input text file and select the best topology from an output file by comparing the values of evaluation vectors. The evaluation vector minimizes the amount of output data and simplifies a most robust topology selection. An input text file can be generated directly from the Cadance layout editor using a SKILL function, thus the proposed evaluation method in the Matlab can be directly linked to the Cadance evironment. Text file generation using SKILL is a good extension this work in the future. The text files used in this work were written in a text editor.

The third chapter shows how the matched structures classification method is used in the practice. Two practical examples are show in the design of 10-bit analog to digital converter with charge redistribution. The first example in this design is oriented to the capacitor's array where the method is used for classification of three different layout patterns. Here the method is very useful because it demonstrates that it is possible to use easy to interconnect matched structure instead of sophisticated matched structures with difficult interconnection. An interconnection within the capacitor's array increases parasitic capacitances and thus deteriorates properties of the converter. The second example is focused to the comparator design where matched

transistors pairs are used. The Matched structures used here are from the reference [10]. These patterns are simple with a few of subdevices, however the proposed method confirms that results are fully in agreement with results found in the [10]. Thereby it is shown that the proposed method works correctly.

The proposed method in this work is new and innovative. With reference to available literature, at the present time a similar matched structures classification method does not exist in scientific publications. The method is especially handy for a larger patterns where it is not easy at first sight to sort out a proper layout structure for example as, DA/AD converters, large resistors and capacitors arrays, current mirrors with a lot of branches etc. In these cases the proposed method saves time in the design process, improves effectivity and yield and also helps to reach a better performance of an analog circuit provided on the assumption that all basic layout fundamental describes at the end of the first chapter are preserved. The Proposed matched structures classification algorithm arose and is currently being used in practice in STMicroelectronics. Moreover, this work has been selected by Cadence company to alternate speaker position in CDNLive conference held 15-17.5 2017 in Munich, Germany.

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