CZECH TECHNICAL UNIVERSITY IN PRAGUE

FACULTY OF ELECTRICAL ENGINEERING

DEPARTMENT OF MICROELECTRONICS

Amplifier design for Sigma-Delta modulator

DIPLOMA THESIS

Program of study: Communications, Multimedia and Electronic

Field of study: Electronic

Supervisor: Doc. Ing. Jiří Jakovenko, PhD.

Jan Krupička

Prague 2016

České vysoké učení technické v Praze
Fakulta elektrotechnická

katedra mikroelektroniky

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: **Bc. K R U P I Č K A Jan**

Studijní program: Komunikace, multimédia a elektronika
Obor: Elektronika

Název tématu: **Návrh zesilovače pro Sigma-Delta modulátor**

Pokyny pro vypracování:

1) Kvalifikujte parametry zesilovače pro použití v sigma-delta modulátoru
2) Definujte základní pravidla pro návrh zesilovače zhlediska rychlosti přeběhu, zesílení a šumuvých vlastností
3) Navrhněte zesilovač v CMOS technologii z hlediska dosažení parametrů: Napájecí napětí 3,3 V, proudový odběr kolem 100 uA, UGB 18 MHz, zesílení větší než 120 dB
4) Analyzujte a zhodnoťte dosažené parametry zesilovače.

Seznam odborné literatury:

[1] BAKER, R. CMOS: circuit design, layout, and simulation. 3rd ed. Hoboken, NJ: Wiley, 2010, xxxiii, 1173 p. ISBN 9780470881323.
[2] ROSA, José M. CMOS sigma-delta converters: practical design guide. 2013. Hoboken: Wiley-Blackwell, 2013, xxviii, 398 p. ISBN 978-1-119-97925-8.
[3] KESTER, Walt. Data conversion handbook. 2005. Boston: Newnes, 2005, xxi, 953 p. Analog Devices series. ISBN 978-0-7506-7841-4.
[4] CHERRY, James A a W SNELGROVE. Continuous-time delta-sigma modulators for high -speed A/D/ conversion: theory, practice, and fundamental performance limits. 1999. Boston: Kluwer Academic Pub., 2000, xxix, 248 p. Kluwer international series in engineering and computer science, SECS 521. ISBN 0792386256.

Vedoucí: **doc. Jiří Jakovenko Ing., Ph.D.**

Platnost zadání: 9. 9. 2017

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vedoucí katedry

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děkan

V Praze dne 26. 2. 2016

Anotace

Předmětem diplomové práce je návrh operačního transkonduktančního zesilovače sigma-delta modulátoru v CMOS technologii. V úvodu jsou obecně popsány vlastnosti a parametry tranzistorů CMOS. Metodika návrhu je založena na EKV modelu, proto se tato práce zabývá i extrakcí jeho parametrů pro zvolenou technologii. Další část se zkoumá požadavky na zesilovač pracující v sigma-delta modulátoru a popisuje jednotlivé zvolené struktury zapojení. Návrh zesilovače je zaměřen na dosažení požadovaných parametrů. Těmi jsou vysoký DC zisk, rychlé ustálení výstupního napětí, nízké spotřeby v klidovém stavu a šumových vlastností. Celý návrh zesilovače probíhá v programu Cadence a jeho simulátoru Eldo. V poslední části jsou shrnuty dosažené vlastnosti navrženého zesilovače a jeho chování v sigma-delta modulátoru.

Annotation

The goal of the diploma thesis is design of operational transconductance amplifier for sigma-delta modulator in CMOS technology. In the introduction characteristics and parameters of CMOS devices are described generally. The design methodology is based on EKV model. Thus, one chapter focuses on its parameters extraction for concrete technology. Next parts analyze requirements of OTA working in sigma-delta modulator and describe particularly chosen sub-circuits. Design of the amplifier aims to achieve appropriate values of all important parameters such as high DC gain, fast settling the output voltage response, low quiescent consumption, and noise performance. The whole amplifier is designed in Cadence and its behavior simulated in Eldo. The last section discuses parameters of proposed OTA and its behavior in sigma-delta modulator.

Declaration

I declare that I completed my diploma thesis *Amplifier design for Sigma-Delta modulator* on my own with the contribution of my supervisor and consultants. I used only materials (literature, projects, articles) specified in the attached list.

Prague, 27. May 2016

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Signature

Acknowledgement

I would like to thank my supervisor Doc. Ing. Jiří Jakovenko, PhD., my colleagues in company *ST Microelectronics* especially Ing. Karel Znojemský and Ing. Martin Dřínovský. This thesis could not be written without their support and help. I also would like to thank my business unit manager Ing. Pavel Krejčí for the valuable opportunity to work in his design team in *ST Microelectronics*.

Prague, 27. May 2016

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Signature

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1 Introduction

The motivation for this diploma thesis can be found in personal electronics implementing capacitive touchscreen solution. As in other business sectors, customers require prices to descent continually. Thus, designers have to develop new methods for touch sensing controller enabling to produce a devices with smaller die size. Smaller die size allows higher integrity in fabrication process as well as lower prices.

The goal of this diploma thesis is to design one functional block in novel touch sensing method. It is novel method due to implementation of a sigma-delta converter. One of the key functional block in sigma-delta converter is amplifier. Therefore, the diploma thesis focuses on the amplifier and describes process of design. Amplifier for this task requires to achieve parameters which are analyzed as well. All design bases on *90 nm* CMOS technology process.

The diploma thesis originates as work of one student at part-time job in company *ST Microelectronics*. The diploma thesis should have taught the student a method so that he can use in similar tasks. It should have also formed inventions and enabled to clarify preferences. Student familiarized with CMOS technologies and their exercise in practical task. This is the most important contribution of diploma thesis.

2 Sigma-Delta Converter

The introduction into touch sensing controller should begin with description of the technique to find out that touch was released. A thin layer is placed under glass with forcing lines and sensing lines. These lines form X-Y grid. During the touch, a charge moves from forcing to sensing line. For successful detection of position of a touch it is necessary to convert the amount of the charge into digital code for next post-processing.

The conversion of the amount of charge into digital code ensures analog-to-digital converter (ADC). It can be separated in two categories depending on the rate of sampling. There is conventional AD converter which is the non-oversampling category. It samples the input signal at the Nyquist rate (Eq. 2.1) [1], where *B* is the bandwidth of the signal and *fs* is the sampling rate. The second category is called an oversampling AD converter whose sampling rate of input signal is much higher than the signal bandwidth. The relation between sampling rate f_S of input signal and required Nyquist condition is expressed in term oversampling ration *OSR* (Eq. 2.2).

$$f_s = 2 \cdot B \qquad \textit{Eq. 2.1}$$

$$OSR = \frac{f_S}{2 \cdot B} \qquad \textit{Eq. 2.2}$$

Resolution of oversampling ADC is much higher than for conventional one. The resolution is determined by digital signal processing instead of complex and very precise analog design. Differences between those converter processes can be seen in Fig. 2.1. TO minimize aliasing effects, signal passes through the filter. Then it is sampled by sample-and-hold circuit, quantized, and encoded into the required digital format. The oversampling ADCs employ much higher sampling rate than conventional ones. Thus an aliasing effect is not dominant. Therefore, the anti-aliasing filter is not necessary and simple first-order filter is required only. The sample-and-hold block is not needed to be implemented either because the modulator contains switch-capacitor circuit. More details about the circuit can be found in next sub-chapter. The output pulses of modulator represent average of input analog signal. These pulses are modulated in real time, therefore, it is not needed to hold the input value. Quantizer is a part of the modulator. The digital signal processing has three purposes, filtering any out-of-band quantization noise, suppressing out-of-band signal, and encoding output code into required format.

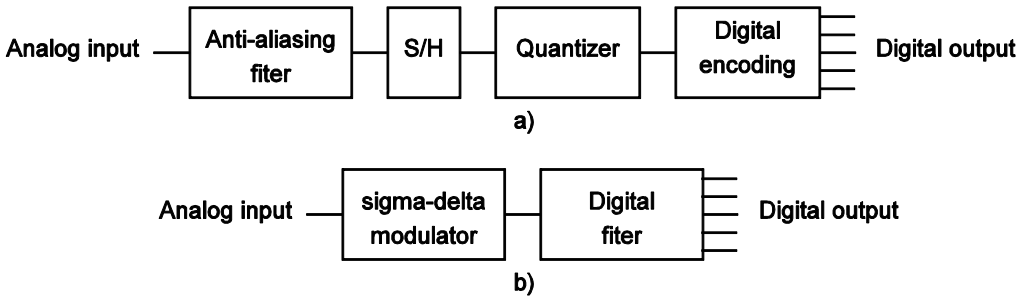

Fig. 2.1: Principle of ADCs a) non-oversampling, b) oversampling [1]

Intuitively, operation of sigma-delta ADC is illustrated in Fig. 6.11. Assuming that a DC signal is on the input V_I. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. This provides the negative feedback loop that forces the average dc voltage at node B to be equal to V_I. It implies that the average DAC output voltage must equal the input voltage V_I. The average DAC output voltage is controlled by the ones-density in the *1-bit* data stream from the comparator output. If the input signal goes positive towards $+V_{REF}$, the number of "ones" in the serial bit stream raises as well. The number of "zeros" decreases. Similarly, if the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases as well. The number of "zeros" increases. As it is described, sigma-delta modulator converts the average value of the input voltage into the serial bit stream. The last block, which contains digital filter and decimator, processes the serial bit stream and produces the final output data [3].

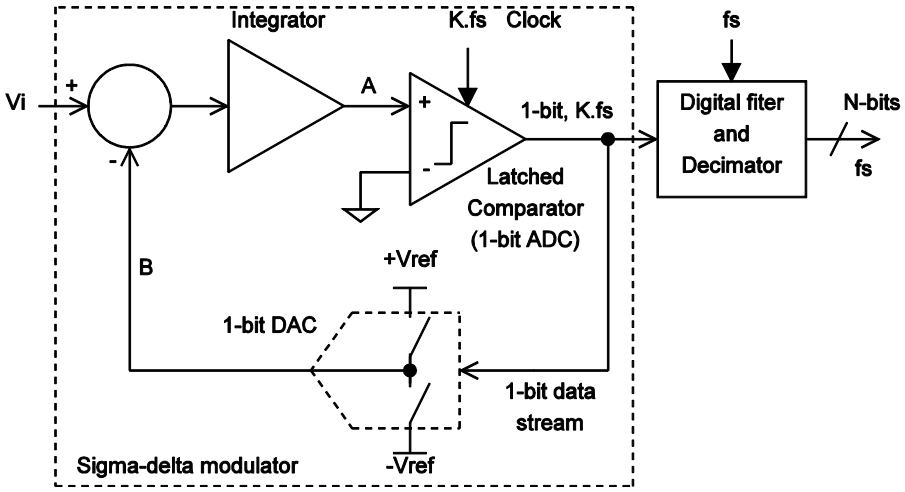

Fig. 2.2: First-order sigma-delta ADC [3]

3 CMOS Technology

A little introduction CMOS (Complementary metal-oxide-semiconductor) technology is given in this chapter. The technology is called complementary because there are used n-type and p-type device. For successful implementation to integrated circuit it is necessary to understand behavior of employed devices. That is the reason why many behavioral models of transistor were created in the past. They provide better understanding. Some of them can be used in hand calculation and some are used in very complex modeling in SPICE simulation. The used CMOS technology is internal of ST Microelectronics and it bases on *3.3* volts.

3.1 MOS Transistor

The most used device in CMOS technology is MOSFET transistor. It can be separated into two categories in dependence on type of doping: NMOS and PMOS. Transistor is four terminals non-linear device. The fourth terminal called *Bulk* connects substrate for NMOS or well for PMOS. Correct function of device is provided that the bulk must be connected to lowest potential for NMOS, respective highest potential for PMOS. The majority carriers in p-substrate of NMOS are holes. There is a non-inductive channel under gate-oxide. If voltage V_{GS} is increased, the gate gets more positive, electrons are pulled under the gate-oxide while the holes are removed from area under gate-oxide. The concentration of electrons is equal to the doping concentration of substrate and channel between drain and source becomes inductive. The voltage V_{GS} which creates equilibrium is defined as the threshold voltage V_{TH}. The behavior of transistor can be described as voltage controlled current source.

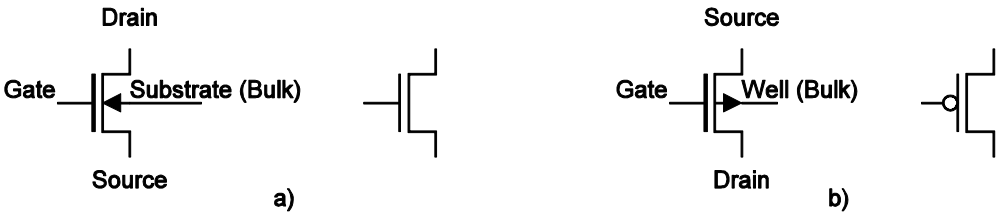

Fig. 3.1: Transistor schematic symbol used in this thesis a) NMOS, b) PMOS

3.1.1 Characteristic of MOSFET

If transistor is described as voltage controlled current source, details can be discussed. The output characteristic, $I_D = f(V_{DS})$, can be separated into two regions. The first one is the triode-

region and the second one is the saturation-region. The triode-region (aka linear or ohmic) is defined by conditions and drain current corresponds with Eq. 3.1 [1].

$$I_D = \mu_0 C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad \textit{Eq. 3.1}$$

$$for\ V_{GS} \geq V_{TH}\ and\ V_{DS} \leq V_{GS} - V_{TH}$$

where Id is drain current, μCox is technological constant, W is effective channel width, L is effective channel Length, V_{GS} is drain-source voltage, V_{TH} is threshold voltage and V_{DS} is drain-source voltage.

When $V_{DS} = V_{GS} - V_{TH}$ the charge distribution is zero at the end of channel-drain interface. This voltage is called saturation V_{DSsat}. It indicates when the channel charge becomes *pinched off* at the channel-drain interface. Hence another increase of drain-source voltage does not raise the drain current. If condition $V_{DS,sat} = V_{GS} - V_{TH}$ is substituted into Eq. 3.1, a term for drain current in saturation region can be obtained Eq. 3.2 [1]

$$I_D = \mu_0 C_{OX} \frac{W}{2L}(V_{GS} - V_{TH})^2 \qquad \textit{Eq. 3.2}$$

$$for\ V_{GS} \geq V_{TH}\ and\ V_{DS} \geq V_{GS} - V_{TH}.$$

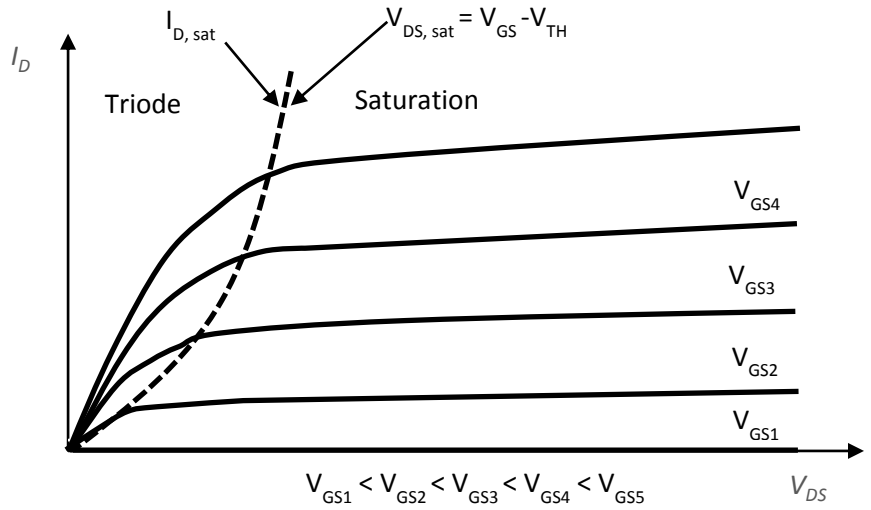

Fig. 3.2: The output characteristics of MOSFET transistor

There are two differences between PMOS and NMOS characteristic. Naturally, the polarity of all values are inverted. But there is also ratio between technology constant µCox of NMOS and PMOS. This is because mobility μ_p of holes is slower than μ_n of electrons. Generally, the μ_p could be two up to four times less than μ_n. Specific value of the ratio depends on technology process

3.1.2 Small Signal Model

Before calculation AC gain it is necessary to define DC operating point of each transistors in the circuit. Small-signal model can be used for simplification of the calculation [1] . It has linear relation but parameters strictly depend on the operating point. Change of DC drain current I_D corresponds to the change of gate-source voltage V_{GS} and small-signal model changes as well.

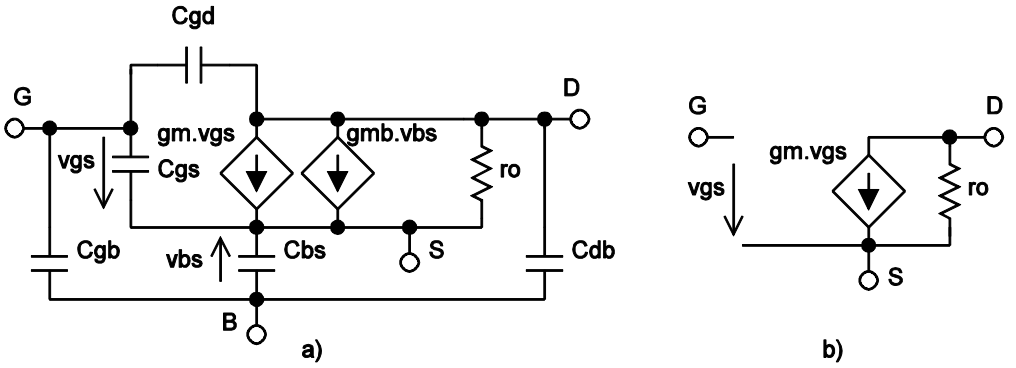

Fig. 3.3: MOS small signal mode a) Complex, b) Simplified [1]

The most significant parameter of small-signal model is transconductance g_m. The transconductance parameter g_m gives relation between AC small-signal input voltage v_{gs} and AC output current i_d at constant DC operating point (Eq. 3.3). If condition $|v_{gs}| << V_{GS}$ applies, Eq. 3.2 can be approximately obtained in an saturation-region given by Eq. 3.4 [1].

$$g_m = \left[\frac{\partial(i_d + I_D)}{\partial(v_{gs} + V_{GS})}\right]_{V_{GS}=const.}^{I_D=const.} = \mu_0 C_{OX} \frac{W}{L}\left(v_{gs} + V_{GS} - V_{TH}\right) \qquad \textit{Eq. 3.3}$$

$$g_m \cong \mu_0 C_{OX} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_0 C_{OX} \frac{W}{L}|I_D|} \qquad \textit{Eq. 3.4}$$

$$i_d = g_m \cdot v_{gs} \qquad \textit{Eq. 3.5}$$

The next important parameters represent output conductance g_{DS} (Eq. 3.6 [1]) of the transistor in saturation, respectively output resistance r_o (Eq. 3.7 [1]). They can be expressed as

$$g_{DS} = r_o{}^{-1} = \left[\frac{\partial(i_d + I_D)}{\partial(v_{ds} + V_{DS})}\right]_{V_{DS} = const.}^{I_D = const.} \qquad \textit{Eq. 3.6}$$

$$r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}, \qquad \textit{Eq. 3.7}$$

where λ is channel-length modulation parameter.

The last significant parameter describing AC behavior is called transition frequency f_T [1]. At the critical frequency f_T the transistor has no gain and becomes an attenuator. As a result, parasitic capacity C_{GS} occurs in parallel from gate to source and input signal is shorted through the C_{GS} to ground.

$$f_T \cong \frac{g_m}{2\pi C_{GS}} = \frac{3\mu_0 C_{OX} \cdot (V_{GS} - V_{TH})}{4\pi \cdot L^2 C_{OX}} = \frac{3\mu_0 \cdot V_{DS,sat}}{4\pi \cdot L^2} \qquad \textit{Eq. 3.8}$$

This parameter obviously relates to high-speed. To increase the speed, the smallest possible channel length and large $V_{DS,sat}$ need to be used. However, very small length corresponds to lower output resistance that means lower gain. Transition frequency for the PMOS device is also smaller than for NMOS one. The f_T of short-channel device can be written as [1]

$$f_T \cong \frac{V_{DS,sat}}{L}. \qquad \textit{Eq. 3.9}$$

3.1.3 Noise of MOSFET

The MOSFET transistor, as noise generator, produces undesired components. The thermal noise is caused by channel resistance. The flicker noise is due to the trapping of charges at the oxide-semiconductor interface [1]. All equations are obtained in [1]. As can be seen in Fig. 3.4, the source of output drain current is placed across the drain and source of the transistor. The source of input-referred noise is placed in front of gate.

Fig. 3.4: MOSFET models with a) drain current noise, b) input-referred noise [1]

Power spectral density *PSD* of MOSFET drain current noise includes both noise signals and correspond to Eq. 3.10 [1]

$$I_M^2 = I_{1/f}^2 + I_R^2 = \frac{KF \cdot I_D^{AF}}{f \cdot C_{OX}^2 LW} + \frac{8kT}{3} \cdot g_m, \qquad \textit{Eq. 3.10}$$

where *KF* is the flicker noise coefficient, *AF* is the flicker noise exponent and *f* is the frequency variable to integrate over.

Note that noise performance is referred to the input of the device. Relation between input and output of the device corresponds with transconductance g_m. Thus the input-referred noise PSD is given as [1]

$$V_{inoise}^2 = \frac{KF \cdot I_D^{AF}}{f \cdot C_{OX}^2 LW \cdot {g_m}^2} + \frac{8kT}{3g_m}. \qquad \textit{Eq. 3.11}$$

It is obvious that increasing tranconductance g_m (making the transistor wider) reduces input-referred flicker noise as well as thermal noise. Beware of circuits like a current mirror which does not have an input signal. Therefore it is required to focus on noise in output drain current. Statement is not obvious, which transistor (PMOS or NMOS) is chosen for low-noise design. In modern technologies (*350nm* and later), where n-type polysilicon is implemented to form a gate of the NMOS as well p-type polysilicon is used for PMOS, both devices have an equal noise performance [1].

3.1.4 Level of Inversion

Transistor operates in many regimes. The most of the transistor parameters depend on the level of inversion in which the transistor operates. There are three regimes in which MOS device can

operate: weak inversion, moderate inversion and strong inversion (Fig. 3.5). For given drain current, the inversion can be controlled by sizing of MOS devices.

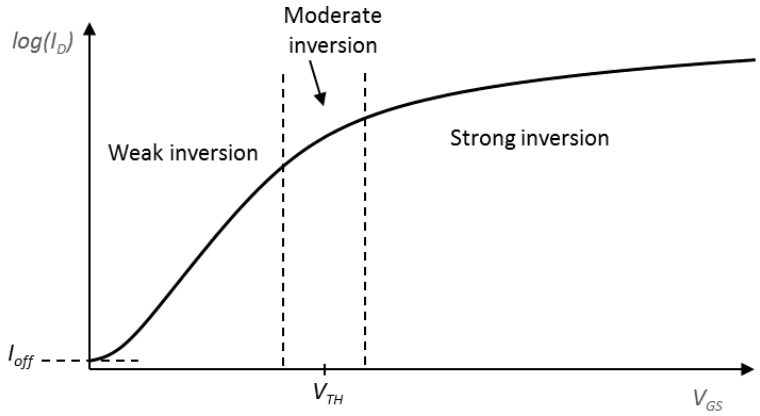

Fig. 3.5: MOSFET transfer characteristic [6]

The **weak inversion** (aka Subthreshold regime) has the channel weakly inverted. This allows to operate the transistor with small gate voltage. Since the substrate is weakly doped and there is not enough charge in the channel to generate a significant electric field to pull electrons from the source to the drain. Current flows by diffusion, not drift [6]. This operating regime is used for very low-power devices and input differential pair because it reaches maximum of transconductance efficiency g_m/I_D, minimum input-referred voltage noise *PSD* for given I_D, and minimum input offset voltage [9]. A negative feature is low transient frequency, thus low speed.

In the **moderate inversion** a transistor does not switch immediately from an exponential, weak-inversion behavior to a quadratic, strong-inversion behavior. There is a smooth transition between the two extremes where drift and diffusion generate the current with neither effect dominating [6].

The **strong-inversion** operation becomes when V_{GS} is sufficiently large than threshold voltage V_{TH}. The gate gets more positive, a large number electrons are pulled under the gate-oxide while the holes are removed from the area under gate-oxide. Current flows by drift, not diffusion. This operating regime is used for current mirrors because it reaches minimum current mismatch and maximum transient frequency [9]. A negative feature is large current noise density.

The changeovers between weak, moderate, and strong inversion can be approximately found by saturation voltage conditions $V_{DS,sat} = V_{GS} - V_{TH}$ or drain current conditions (Tab. 3.1). The specific current is I_S (Eq. 3.12 [6]) current depends on technology current I_O (Eq. 3.14 [5]) and dimensions of device.

Tab. 3.1: Criterial for inversion boundaries

Strong inversion	$V_{DS,sat} \geq 100\ mV$	$I_D \geq 10I_s$
Moderate inversion	$100\ mV > V_{DS,sat} > -100\ mV$	$10I_s > I_D > 0.1I_s$
Weak inversion	$V_{DS,sat} \leq -100\ mV$	$I_D \geq 0.1I_s$

$$I_S = I_O \frac{W}{L} \qquad \textit{Eq. 3.12}$$

3.2 EKV Transistors Model

The analog design is complicated task. How to set initial dimensions of the devices in topology, so that a large number of simulation runs is not effective to get the desired operation point. The very complex technology models cannot be used for hand design. The EKV transistor model transistor is one of the most popular analytical model for first-order hand design. The EKV transistor model provides an excellent match from weak through moderate to strong inversion and is yet simple to be used for hand design, optimization, and circuit parameter estimation.

3.2.1 Analytical Model

The EKV model of transistor is based on **inversion coefficient IC**, the parameter which modulates drain current trough all inversion regions. To ensure weak inversion set $IC \leq 0.1$. For strong inversion set $IC \geq 10$. The value in between (e.g. $IC = 1$) corresponds to moderate inversion. All of these conditions are based on terms in Tab. 3.1. The most significant equation of EKV model in saturation is [5]

$$I_D = 2n\mu_0 C_{OX} {U_T}^2 \frac{W}{L} ln^2\left(1 + e^{\frac{V_{GS}-V_{TH}}{2nU_T}}\right) = I_O \frac{W}{L} IC \qquad \textit{Eq. 3.13}$$

$$I_O = 2n\mu_0 C_{OX} {U_T}^2 \qquad \textit{Eq. 3.14}$$

where I_O is technology current, thermal voltage $U_T = kT/q$, the value for *300K* is *25.85mV* and *n* is modulation coefficient. Transconductance efficiency (Eq. 3.15 [7]) and drain-source saturation voltage (Eq. 3.16 [7]) can be obtained as follows,

$$\frac{g_m}{I_D} = \frac{1}{nU_T\left(\sqrt{IC + \frac{1}{4}} + \frac{1}{2}\right)} \qquad \textit{Eq. 3.15}$$

$$V_{DS,sat} = 2U_T\left[\left(\sqrt{IC + \tfrac{1}{4}} + \tfrac{1}{2}\right) + 1\right]. \qquad \textit{Eq. 3.16}$$

The gate-oxide capacitance expression is given as [7]

$$C_{GOX} = WLC_{OX} = \frac{L^2}{IC}\frac{I_D}{I_O}C_{OX}. \qquad \textit{Eq. 3.17}$$

3.3 Extraction of EKV Model Parameters

This chapter explicates a parameter extraction methodology. As it was shown in previous chapter, it is needed to know technology current for first-order hand design. For verification EKV model it is necessary to get the modulation coefficient *n* from another test bench. The EKV model is a complex model described by many parameters, not only few ones. According to [5] and [7] the extraction procedure is done, where dimensions of transistors W and L are set to *5 µm* for simplification.

3.3.1 Technology Current

First of all, it is necessary to extract technology current I_O. It depends on given technology and type of MOSFET, the typical values of I_O range from *100nA* to *500nA* for NMOS, and *40nA* to *120nA* for PMOS [6]. According to test bench (Fig. 3.6) *characteristic root of I_D vs. source voltage V_S* is plotted (Fig. 6.11). Note that the gate-source voltage must get the transistor in strong inversion saturation. From slope (Eq. 3.19 [5]) of decreasing function the technology current I_O (Eq. 5.1) can be read.

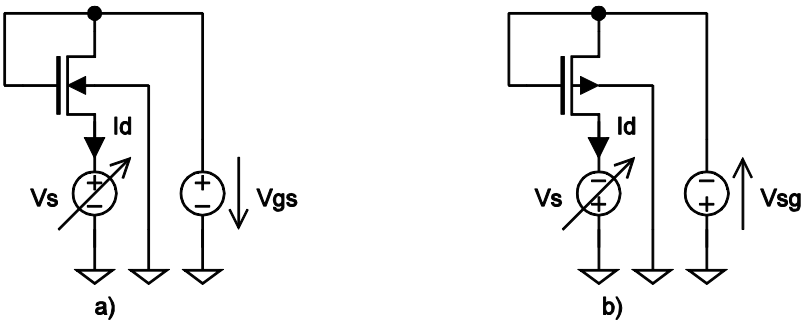

Fig. 3.6: Circuits used for the simulations of the $\sqrt{I_D}$ vs. V_S characteristic a) NMOS, b) PMOS [5]

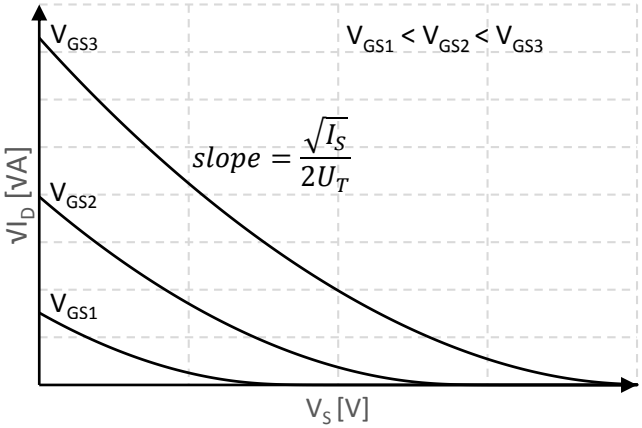

Fig. 3.7: Characteristics for slope obtaining [5]

$$\sqrt{I_D} = \sqrt{\frac{n\beta}{2}}\,(V_P - V_S) = \frac{\sqrt{I_S}}{2U_T}(V_P - V_S) \qquad \textit{Eq. 3.18}$$

$$slope = max\left(\frac{d\sqrt{I_D}}{dV_S}\right) \qquad \textit{Eq. 3.19}$$

$$I_0 = \frac{(slope \cdot 2U_T)^2}{\frac{W}{L}} \qquad \textit{Eq. 3.20}$$

3.3.2 Modulation Coefficient

After extraction of the technology current it is necessary found out the modulation coefficient *n* for verification of obtained results. Modulation coefficient can reach approximately a value *1.5*, depends on technology and type of MOSFET. According to test bench (Fig. 3.8) is plotted characteristic *of pinch-off voltage V_P vs. gate-source voltage* VGS (Fig. 3.11). The pinch-off

voltage V_P corresponds to the value of the channel potential for which the inversion charge becomes zero in a non-equilibrium situation. From pinch-off characteristic it is possible get threshold voltage V_{TH} (Eq. 3.22) which is determined as the particular value of V_G corresponding to the $V_P = 0$ cross point. The value of the drain current I_D (Eq. 3.21 [5]) equals approximately to half of the specific current I_S. The transistor is therefore biased in the middle of moderate inversion region. Modulation coefficient n is obtained from slope of pinch-off voltage characteristic (Eq. 3.23).

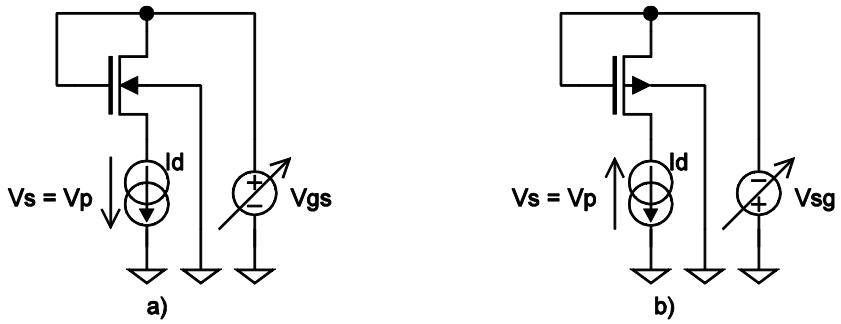

Fig. 3.8: Circuits used for the simulations of the pinch-off voltage a) NMOS, b) PMOS [5]

$$I_D = I_s \cdot [ln(2)]^2 \cong \frac{I_S}{2} = \frac{I_0}{2}\frac{W}{L} \qquad \textit{Eq. 3.21}$$

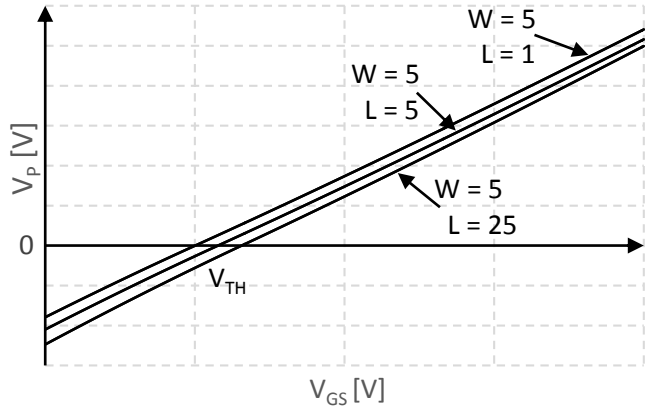

Fig. 3.9: Characteristics for modulation coefficient obtaining [5]

$$V_{TH} = V_{GS} \quad for\ V_P = 0 \qquad \textit{Eq. 3.22}$$

$$n = \left(\frac{dV_P}{dV_G}\right)^{-1} \qquad \textit{Eq. 3.23}$$

3.3.3 Verification of Results

Fitting results for a both transistors are plotted in Fig. 3.10 with a corresponding relative error in Fig. 3.11. The simulated characteristics are simply obtained by sweeping the gate-source voltage in range from *0.3 V* to *2 V* and plotting root of drain current. Cross points are calculated by Eq. 3.13 with obtained technology parameter. Below the range the relative error is significant. But in this operating range, which is sufficient considering used technology, the relative error does not exceed 20% over the whole VGS range.

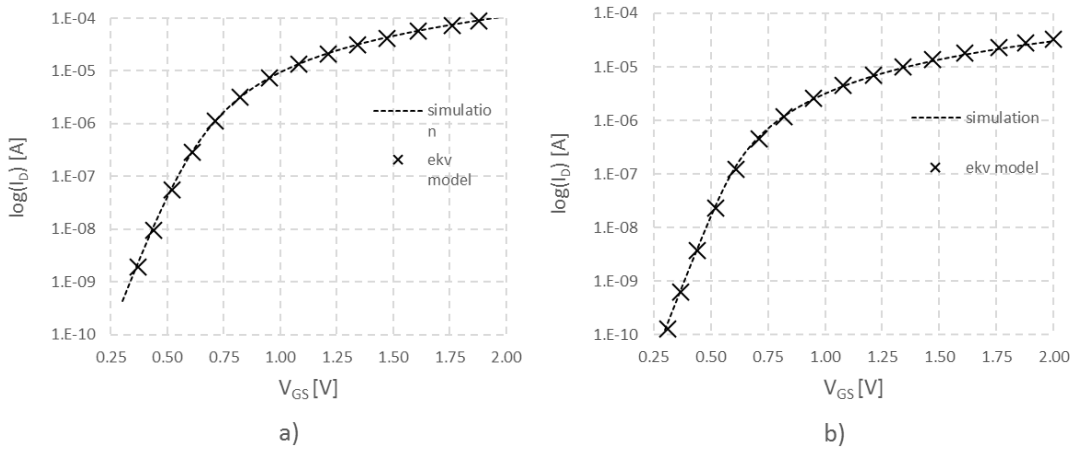

Fig. 3.10: Fitting results of the drain current a) NMOS, b) PMOS

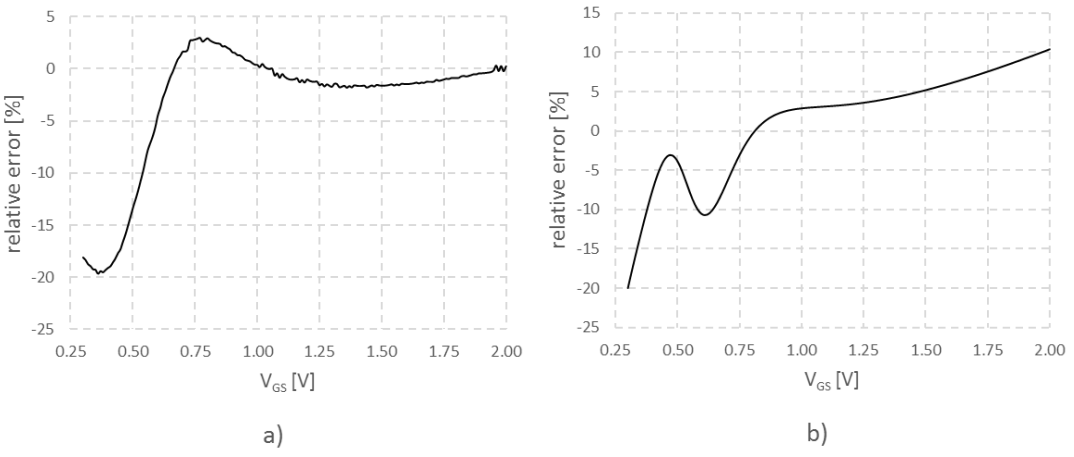

Fig. 3.11: Relative errors of the fitting a) NMOS, b) PMOS

4 Theoretical Study

The touch sensing controller with sigma-delta converter is a method which could bring a smaller device than previous solutions. Smaller die size increases yield of silicon wafer. Higher efficiency of chip fabrication makes a higher profit, stable costumers etc. The economic responsibility is assigned to management. Furthermore, the results of feasibility study indicate that the solution using sigma-delta converter provides smaller die's area and lower power consumption.

4.1 Amplifier in Σ-Δ Modulator

Amplifiers are basic blocs of sigma-delta modulator used for Switching Capacitor (SC) networks or active RC integrators, it depends on operational mode. Amplifier design usually comprises requirements for the DC gain, dynamic behavior and input referred noise. In this chapter main aspects are described for amplifier design and its parameters in dependence on behavior of sigma-delta modulator.

The ideal performance of the SC network employed in proposed sigma-delta ADC (Fig. 4.1) is derived in Eq. 4.1, where the output voltage response ΔV_O is caused by input step voltage V_I. The ideal SC networks implies that the input parasitic capacitor C_P is neglected and DC gain A_O reaches infinity.

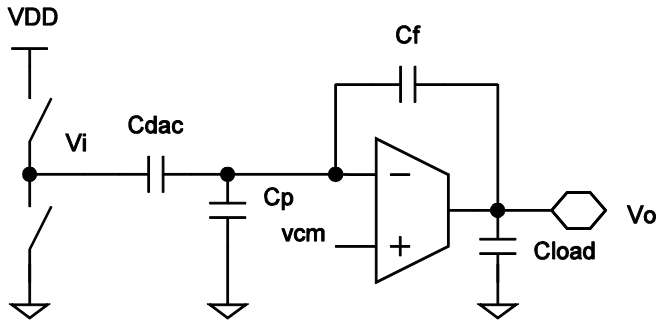

Fig. 4.1: Switching Capacitor network employed in sigma-delta modulator

$$\Delta V_O = V_I \frac{C_{DAC}}{C_F} \qquad \textit{Eq. 4.1}$$

4.1.1 Finite DC gain

The most discussed non ideal parameter is the finite amplifier DC gain. The SC network is affected by finite DC gain A_O (open-loop gain) and parasitic capacitor C_P, which is neglected. The expression can be obtained approximately for the output voltage response ΔV_O Eq. 4.2 [8] of the leaky SC network,

$$\Delta V_O = V_I \frac{C_{DAC}}{\frac{C_{DAC} + C_F}{A_O} + C_F} \qquad \textit{Eq. 4.2}$$

$$A_O = R_o \cdot g_m. \qquad \textit{Eq. 4.3}$$

It is obvious that to achieve an ideal case it is necessary to increase the DC gain A_O as much as possible. As can be seen in Fig. 4.1, according to SC theory the SC network employs a gain coefficient which is implemented as capacitor ratio. Of course the variations of capacitors in technological process might bring another non ideal effects, but this aspect is neglected here.

4.1.2 Dynamic Behavior

Speed limitation of amplifiers in SC networks cause errors in a charge transfer. Transient response performance for settling output voltage error will be higher as sampling frequency will increase. The time slot for the charge transfer gets reduced by increasing sampling frequency. At the end of every time slot the output of SC network must achieve the final voltage value safely. The dynamic limitation is given by a finite unity gain bandwidth *UGB*, phase margin *PM,* and slew-rate *SR*. It also corresponds with connected capacitors C_{DAC} and C_F as well as parasitic capacity C_P and an output capacity of the amplifier C_L. There is defined an equivalent capacitor C_{TOT} in Eq. 4.4. It corresponds with the SC network circuit in Fig. 4.1, which comprises both capacitor C_{DAC}, C_F and output capacity C_L. The parasitic capacity C_P is neglected for its small value.

$$C_{TOT} = C_L + \frac{C_{DAC} \| C_P \cdot C_F}{C_{DAC} \| C_P + C_F} \cong C_L + \frac{C_{DAC} \cdot C_F}{C_{DAC} + C_F} \qquad \textit{Eq. 4.4}$$

The **slew-rate** corresponds with maximum output current which can drive a load capacity. In proposed case the *SR* is obtained as [1]

$$SR = \frac{I_O}{C_{TOT}} = \frac{I_O}{C_L + \frac{C_{DAC} \cdot C_F}{C_{DAC} + C_F}}. \qquad \textit{Eq. 4.5}$$

For next minimization of the settling error it is necessary to define acceptable **unity gain bandwidth**, the frequency where gain equals one. According to references, the unity gain frequency *UGF* must be at least 5 [8] or 6 [4] higher than the sampling frequency f_S (Eq. 4.6).

$$UGF \geq 5 \cdot f_S \qquad \textit{Eq. 4.6}$$

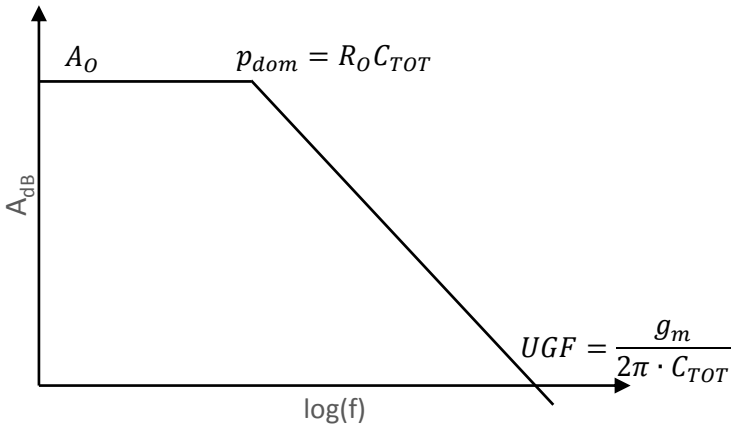

Fig. 4.2: AC characteristic of amplifier [8]

$$pole_{dom} = R_o C_{TOT} \qquad \textit{Eq. 4.7}$$

$$UGF = \frac{g_m}{2\pi \cdot C_{TOT}} \qquad \textit{Eq. 4.8}$$

AC characteristic summarize some important parameters of the amplifier. The first one is open-loop gain A_O. The frequency, where the gain decreases by *3 dB,* is dominant pole. Expression of this is given by Eq. 4.7 [8], where r_o is the output resistance of the amplifier. The next parameter *UGF* has been already mentioned. This parameter must fulfil the previous condition but it is not desirable to achieve much higher frequency. If gain of amplifier gets significantly under the one, the noise is suppressed obviously. The thermal noise is attenuated for higher band than *UGF*. Thus the AC characteristics also affect noise performance of the amplifier.

4.1.3 Input Referred Noise

The next parameter which affects significantly the accuracy of sigma-delta modulators, is input referred noise. There are three sources which can generate noise, thermal noise of capacitors, thermal noise and flicker noise of the amplifier, characteristics are in Fig. 4.3. The voltage is

sampled onto the input capacitor through the resistance of switch. This generates noise given by Eq. 4.9 [4], where *k* is Boltzmann's constant, *T* is absolute temperature, and *C* is the capacitance. Depending on resolution, this might require relatively large input capacitors. Particularly for high-resolution converters, integration of such capacitors onto chip might be problematic [4].

$$V_{onoise,RMS} = \sqrt{\frac{kT}{C}} \qquad \textit{Eq. 4.9}$$

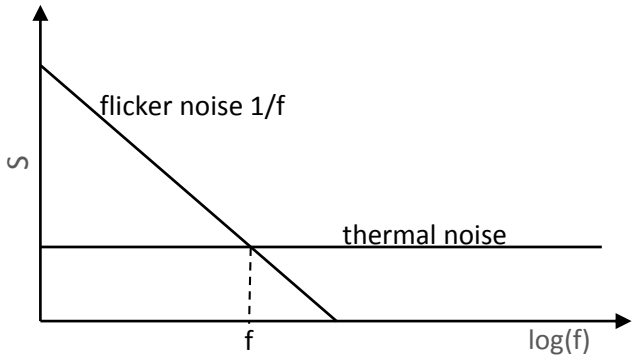

Fig. 4.3: Spectral noise density of the amplifier flicker and thermal noise

The thermal noise of the first amplifier must be kept small. It is inversely proportional to the transconductance g_m of the input MOS differential pair. The maximum transconductance g_m for given drain current can be controlled by level of inversion [4].

MOS transistor also has *1/f* flicker noise, where low-frequency noise increasing as *10dB/*dec with decreasing frequency [4].For required accuracy of sensing controller tens of accumulating runs are needed. Furthermore, a small amount of noise is accumulated during every run. After completing all runs, the accumulated noise is not negligible value and efficient number of bits decreases significantly. Many the least significant bits represent noise. Circuit of proposed sigma-delta modulator contains chopping scheme of feedback capacitor. Hence the most of low-frequency band of noise, the flicker noise, is attenuated. If limiting frequency *f of* flicker noise is lower than chopping frequency, the flicker noise should be attenuated completely.

4.2 Design Requirements

Before thinking about which circuit topology will be used, it is important to define parameters and requirements which proposed amplifier should achieve. This is one of the most difficult task in good analog design. Therefore, Let us summarize previous knowledge.

First of all, the amplifier works in SC network or active RC integrator and drives only capacitive load. Therefore, the proposed block is designed as **operational transconductance amplifier**. OTA is basically voltage controlled current source, in ideal case its output impedance equals infinity. Thus, it can drive only capacitive load and gain significantly decreases with resistive load.

Another important requirement is a **power consumption**. The whole sensing controller is part of portable device so must achieve very low-power consumption. A quiescent current is given by bias currents of transistors in the circuit. But the finite bias current causes slew-rate limitation and it is not able to charge a total capacitive load in specific case. **Class AB configuration** can achieve high speed and keeps very low quiescent current.

For minimization the **settling error** a high slew-rate, a safe phase margin, and sufficient unity gain bandwidth must be reached. The large current drives capacitive load due to AB configuration. However, very fast increase of the current itself is not enough. To minimize oscillations, the circuit has to quit the AB mode very fast as well. Because C_{TOT} might be changed, the OTA transconductance g_m and the criteria for *UGF* must be implemented for all C_{TOT} variations as well. C_{TOT} variations can be provided by connecting different value capacity of C_{DAC} or C_F. Also, the needless large value of transconductance g_m cannot reduce the thermal noise. Because the tranconductance g_m has relatively limits which are given by required AC characteristic. The high **DC gain** A_O also helps to reach required settling, because basic topology of OTA without any gain-enhanced sub-circuit cannot achieve it. The DC gain A_O must be increased by very high output resistance.

The proposed design of sensing controller does not implement differential processing of the charge. Thus amplifier has to have a **non-differential output**. Mentioned parameters and some other ones are summarized in Tab. 4.1.

Tab. 4.1: Summarized requirements of proposed OTA

Parameter	*Criterion*	*Value*
V_{DD}	*Technology*	*2.7 – 3.3 V*
I_Q	*Power consumption*	*100 µA*
C_{TOT}	$C_L + (C_{DAC} \cdot C_F) / (C_{DAC} + C_F)$	C_L*+ (0.5 ÷ 6.7) pF*
UGB	$UGF \geq 5 \cdot f_S$	*18 MHz*
SR	I_O / C_{TOT}	*Max.*
g_m	$C_{TOT} \cdot UGF$	*≤ 1.5 mS*
r_o	*Circuit topology*	10^0 *GΩ*
A_O	$g_m \cdot r_o$	*≥ 120 dB*

4.3 Biasing Circuit

The main topic of this this thesis is not to design an independent current source, which can provide biasing for an input stage, as well as output stage. There are used an ideal current source and elementary analog blocks to achieve right operational point of each transistors.

4.3.1 Current Mirror

The basic common circuit in analog integrated-circuits is called a current mirror. Its implementation has significant consequence because a current reference is also implemented on chip. It is a source of constant DC current which does not affect any temperature or power-supply voltage changes in ideal case. The current mirrors distribute the current replicas of reference. Thus by this technique another parts of circuit can be easily biased. The circuit of current mirror is illustrated in Fig. 4.4.

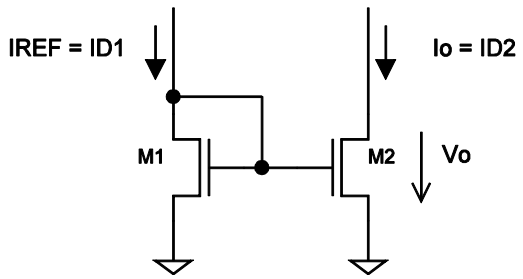

Fig. 4.4: Basic topology of the NMOS current mirror [1]

The principle explanation ca be described as follows. Drain and gate of M_1 are connected. Assuming that transistors M_1 and M_2 have the same channel dimension, the voltage condition can be written as $V_{DS1} = V_{GS1} = V_{GS2} = V_{DS2}$. According to the term of saturation operating region (Eq. 3.2) the transistor M_1 operates in saturation region, as well as M_2. The drain currents of both transistors represented by I_{REF} and I_O are equal. If voltage conditions are substituted into Eq. 3.2. a term [1] for current ratio can be obtained [1] as

$$\frac{I_O}{I_{REF}} = \frac{W_2/L_2}{W_1/L_1} \cdot \frac{1 + \lambda\left(V_O - V_{DS1,sat}\right)}{1 + \lambda\left(V_{DS1} - V_{DS1,sat}\right)} \cong \frac{W_2/L_2}{W_1/L_1}, \qquad \textit{Eq. 4.10}$$

where the final term neglects channel-length modulation parameter ($\lambda = 0$).

In practical design size of length-channel of both transistors are usually the same and thus length-channel ration is neglected. The currents ratio depends only on width-channel ration of devices. Of course the origin current I_{REF} does not equal to its replica I_O due to neglecting of variations in layout or technology process. The differences can reach up to *20 %*. There are many layout techniques to suppress currents mismatch. Hence a simple layout technique is discussed in chapter of design.

4.3.2 Biasing Circuit

In this thesis simple bias block is implemented (Fig. 4.5), which provides bias voltages V_{BIASN} for NMOS current mirrors and V_{BIASP} for PMOS ones as well. Biasing voltages set operating points of input stage and output regulated cascodes. Thus, currents flow through M_3 and M_5 must be selected bearing in mind requirements for biased circuits as well as for power dissipation. The current replicas can be achieved by size-channel ratio. Current I_{REF} is generated by reference.

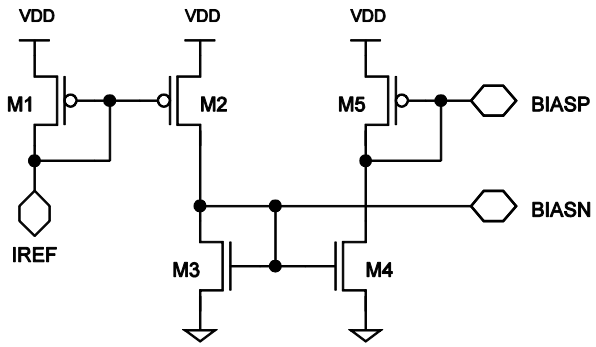

Fig. 4.5: Employed biasing circuit

4.4 Input Stage

One of the key block of every operational transconductance amplifier is differential amplifier. It significantly affects several parameters of the whole amplifier such as gain, slew rate, noise performance, or offset etc. Many variations of circuit topology of input stage can be employed for this task in dependence on its features. Illustrated circuits also have a complementary variation with PMOS transistors. Let us discuss the configuration possibilities.

4.4.1 Differential Amplifier

The most widely implemented basic circuit for differential amplifier is source-coupled pair, which is shown in Fig. 4.6. Transistor M_1 and M_2 also can be called a differential pair, diff-pair as shortcut. A biasing circuit must be comprised for principle description. Employing the current mirror is not necessary to implicate in explanation but it affects significantly behavior of another configurations of differential amplifier. However, the ideal current source is shown instead of ideal current source to keep the same condition.

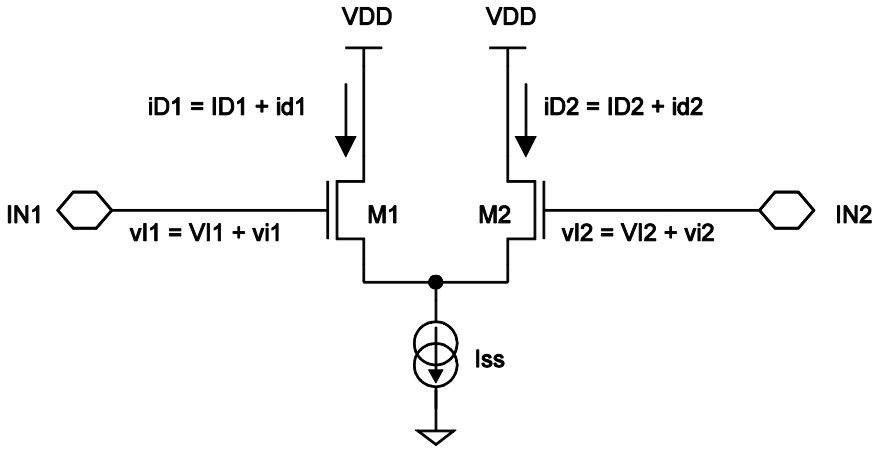

Fig. 4.6: Topology of the NMOS diff-pair [1]

Input voltage v_I of transistor M_1 and M_2 include AC and DC components, difference between them can be written as [1]

$$v_{DI} = v_{I1} - v_{I2} = V_{GS1} + v_{gs1} - V_{GS2} - v_{gs2}. \qquad \textit{Eq. 4.11}$$

If the gate voltages of transistors M_1 and M_2 are equal then a half of bias current ($I_{SS}/2$) flows through each transistor. When one of gate potentials becomes more positive, drain current i_D of

this transistor increases. However, biasing condition must be still valid, where drain currents consist of AC and DC components as well.

$$I_{SS} = i_{D1} + i_{D2} \qquad \textit{Eq. 4.12}$$

It is obvious that the basic configuration of diff-pair has slew-rate limitations. The maximum output current is provided by finite value of bias current I_{SS} (Eq. 4.12) [1]. Of course, increasing bias current can be reached higher slew-rate, but quiescent consumption increases proportionately. It is illusory to design the basic configuration of diff-pair working in SC network and keep power consumption as low as possible.

$$SR = \frac{I_{SS}}{C_{TOT}} \qquad \textit{Eq. 4.13}$$

To achieve minimum power consumption and maximize slew-rate limitations on the other side, differential amplifier in the class AB configuration can be employed. Then, slew-rate performance depends on the peak-current.

4.4.2 Class AB Differential Pair

There are many configuration possibilities how to reach peak-current and thus eliminate the slew-rate limitations. In fact, maximum current which drives a capacitive load does not equal infinity. But the value of peak-current raises up to the value 10 – 30 times higher than bias current I_{SS}, which is significant increase. In the thesis two types of class AB differential amplifier are studied.

The first one is *Source cross-coupled pair* [1] [8]. This circuit can operate in the class AB mode with significant output current. For right set DC operating point bias current I_{SS} must flow in all transistor in the circuit. To achieve this condition, devices channel sizes of devices must be same and both inputs to the pair are connected to the same voltage within the pair's common-mode input range [1]. All channel size of NMOS (exclusive biasing current mirrors M_5 – M_7) are the same as well as all PMOS channel sizes. Simplified schematic in Fig. 4.7b shows that transistors M_{11}, M_{21}, M_{31}, M_{41} work as biasing batteries, whose gate-source voltages are mirrored by M_1-M_4 to keep DC operating point. If voltage v_{I1} increases the transistor M_1 turns on, as well as M_3, because its gate potential of M_3 is constant. Thus, the drain current i_{D1} increases continually

when the potential of gate v_{I1} increases. Meanwhile, the gate-source voltage of M_4 also becomes more positive, therefore, transistor M_4 shuts off as well as M_2.

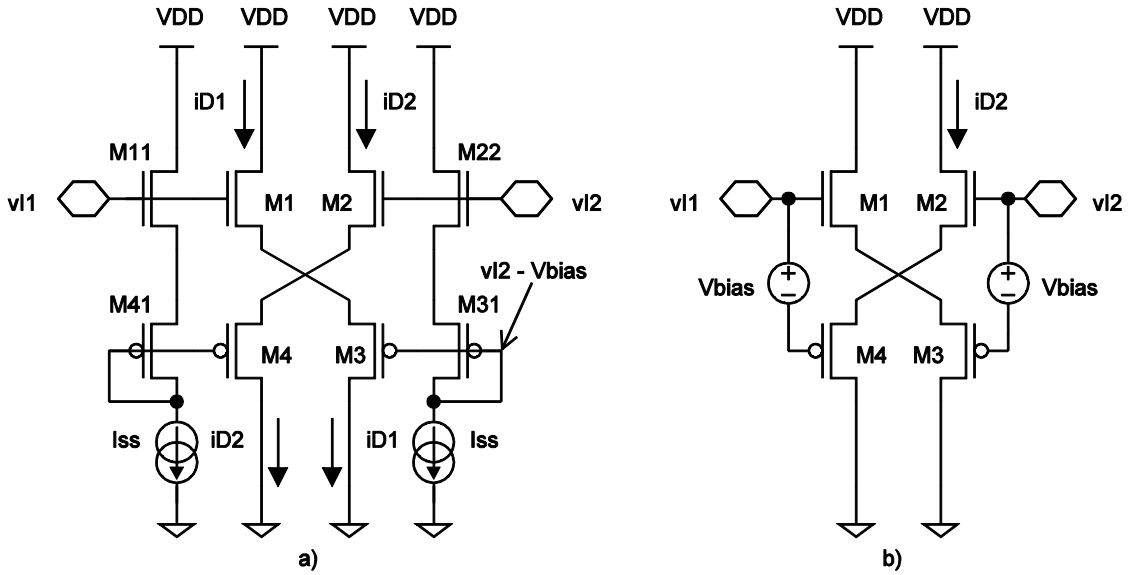

Fig. 4.7: Topology of a) cross-coupled diff. amplifier with NMOS input devices, b) simplify [1]

The second solution can be called *Differential pair with adaptive biasing*. More details about it are explained in the next chapter. One of the reasons why adaptive biasing configuration is employed in this case is shown in Fig. 4.8. The figure illustrates differences in a transfer characteristics among basic diff-pair, cross-coupled pair and diff-pair with adaptive biasing. All circuits are biased by the same value of current I_{SS}. As it is described in the previous chapter for basic diff-pair in term Eq. 4.12 , if one of the gates of M_1 or M_2 becomes much more positive, the maximum drain current i_D saturates at value of bias current I_{SS}. Both class AB configurations work properly. No saturations of the drain currents even if the gate potentials increase significantly. Unlike cross-coupled, solution with adaptive biasing pair has steeper slope of drain current for small input voltage difference. Therefore, small difference in input voltage can provide significant current amplitude.

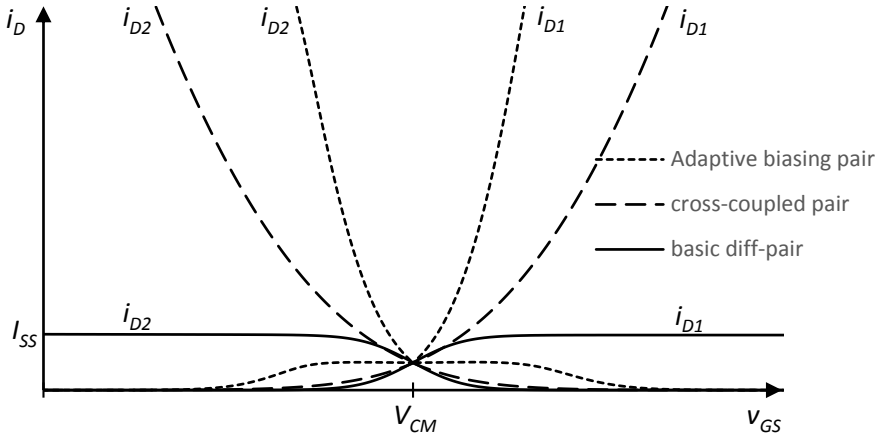

Fig. 4.8: The comparison basic diff-pair and class AB diff-pairs

4.4.3 Differential Pair with Adaptive Biasing

This configuration [1] [10] is derived from basic source-coupled pair. It achieves high output current capability along with reduced power dissipation. This cannot be strictly used only as AB configuration, its behavior also provides linear the transfer characteristic of diff-pair. Fig. 4.9 shows basic idea of adaptive biasing solution which includes basic source-coupled pair and ideal current sources. If input voltages v_{I1} and v_{I2} are equal, current sources I_{SS1} and I_{SS2} do not supply any bias current into circuit. Therefore the diff-pair is biased only I_{SS}. If input voltage v_{I1} increases more than v_{I2}, the current source I_{SS1} becomes non-zero and also biases the diff-pair. The same condition is valid for increasing input voltage v_{I2}, of course the second current source I_{SS2} becomes non-zero. The maximum output current of the basic diff-pair is equal to value of bias current I_{SS}. However, now the output current is limited to either $I_{SS} + I_{SS1}$ or $I_{SS} + I_{SS2}$.

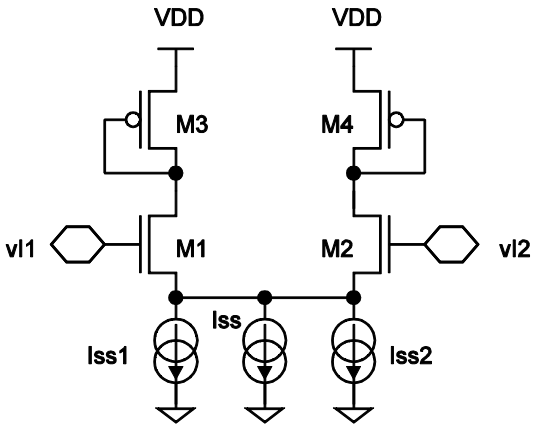

Fig. 4.9: Principle of diff-pair with adaptive biasing [1]

Fig. 4.10 illustrates how to implement the current source I_{SS2}. The current source I_{SS1} can be implemented with a similar assumption. There is used current subtraction circuit consisting of M_1 and M_2 to force equal currents which flow through each tails of differential pair. Note, that transistors M_1 – M_3 have a same channel width-to-length ratio. There are basically three operating modes depending on current conditions in diff-pair. If I_1 equals to I_2 or I_2 is smaller than I_1 a zero current flows through the transistor M_3. But if I_2 is larger than I_1 the, difference between them ($I_2 - I_1$) flows in M_3. Transistors M_3 and M_4 work as current mirror where M_4 is realized B times wider than M_3, thus current $B\cdot (I_2 - I_1)$ flows in M_4.

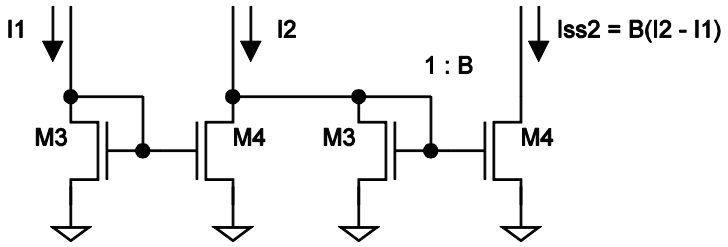

Fig. 4.10: Current source used in adaptive biasing [1]

The final implementation of whole diff-pair with adaptive biasing is shown in Fig. 4.11. This improved source-coupled pair includes nineteen transistors M_1 - M_{19}. Transistors M_1 and M_2 create well known basic diff-pair. PMOS transistor M_3 and M_4 provide mirroring differential current I_1 and I_2 into a rest of circuit. Let us focus only on left side of schematic because the right side works analogously. The sub-circuit of M_1, M_3 and M_5 – M_7 add positive feedback loop. Assuming M_2 is shut off, the maximum output current flowing through the M_1 is bias current I_{SS}. This current is mirrored in M_5 and M_6 and current flows through the M_7 (I_{SS2} source) are transform to simple term $B\cdot I_{SS}$. Transistor M_1 is continuously biased by I_{SS}, therefore the bias current which flows in M_1 is $I_{SS} + B\cdot I_{SS}$. Because the positive feedback is implemented, the total bias current increases as [1]

$$I_{TOT} = I_{SS} \cdot (1 + B + B^2 + B^3 + \cdots). \qquad \textit{Eq. 4.14}$$

If $B < 1$, this geometric series can be written as

$$I_{TOT} = \frac{I_{TOT}}{1 - B}. \qquad \textit{Eq. 4.15}$$

Depending on *B* coefficient the adaptive biasing differential amplifier can achieve different value of output current. If $B = 0$, the transistor M_7 does not exist as well as positive feedback loop, the maximum available bias current is only I_{SS}. For $B = ½$, according to Eq. 4.15 [1], the total bias current is $2 \cdot I_{SS}$. To eliminate slew-rate limitation, the value of *B* can be unity. Due to physical limits total output current could not reach infinite. However, the bias current exceeds many times the bias current in quiescent mode and this occasion is employed in the thesis.

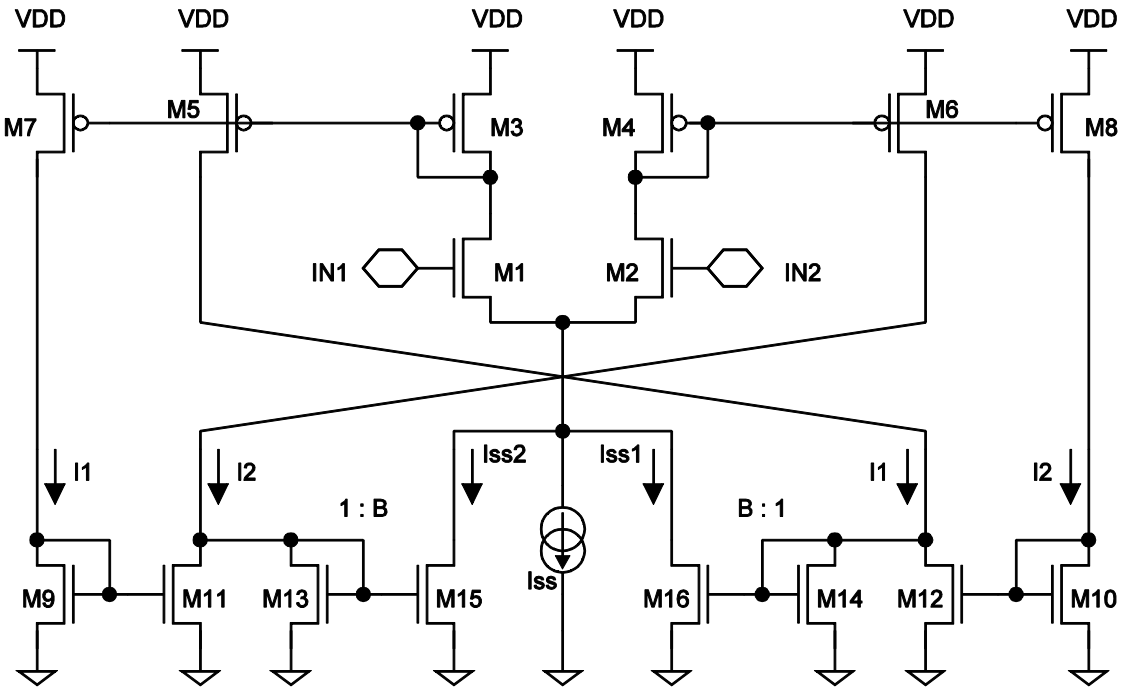

Fig. 4.11: Topology of diff-pair with adaptive biasing [1]

4.5 Output Stage

The output structure affects many significant parameters of operational transconductance amplifier. The output stage of any type of amplifier adjusts its output impedance R_{OUT}. OTA basically works as voltage controlled current source and, thus, its output impedance must achieve infinity in ideal case.

4.5.1 Current Mirror

The best way how to get the differential current to output node is utilizing the current mirror $M_{20} – M_{23}$ (Fig. 4.12). PMOS devices are extended by two transistors M_{20} and M_{23}, which form a half of output stage. The transistor M_{23} is *K* times wider than M_4 and loads to the output node K times larger than i_{D2} current. The second half of output stage is provided by NMOS devices M_{21}

and M_{22} which is K times wider than M_{21} as well. The output current which flows through the M_{22} is K times larger than i_{D1} is.

The constant K increases the output current as well as a DC gain of OTA (Eq. 4.16) [15]. Otherwise it supports AB configuration to maximize the output current but also increases rapidly power consumption in quiescent mode. Thus, it is strongly recommended the constant K to be equal to five at maximum. According to Eq. 4.18 [14] a non-dominant pole $p_{non\text{-}dom}$ is formed by gate-source capacitance of PMOS current mirrors. It is obvious that higher K constant adds more PMOS transistor in parallel and thus gate-source capacitance increases.

$$A_O = K \cdot g_{m1} \cdot R_O \qquad \textit{Eq. 4.16}$$

where g_{m1} is transconductance of input transistors M_1/M_2 and R_O can be written as,

$$R_O = r_{o22} \parallel r_{o23} \qquad \textit{Eq. 4.17}$$

$$p_{non-dom} = \frac{g_{m4}}{(3+K) \cdot C_{GS4}} \qquad \textit{Eq. 4.18}$$

Output resistance of transistor r_o can approximately reach values in units of $M\Omega$, thus, a total output resistance of OTA limits at hundreds $k\Omega$. If this basic configuration is employed maximal DC gain A_O of about *55 dB* can be reached, which is not enough for this design task. Other circuit configuration has to be implemented to increase the total output resistance of OTA. Because the tranconductance g_{m1} has relatively limits for given bias current as well as technology process. The DC gain A_O must be increased by very high output resistance.

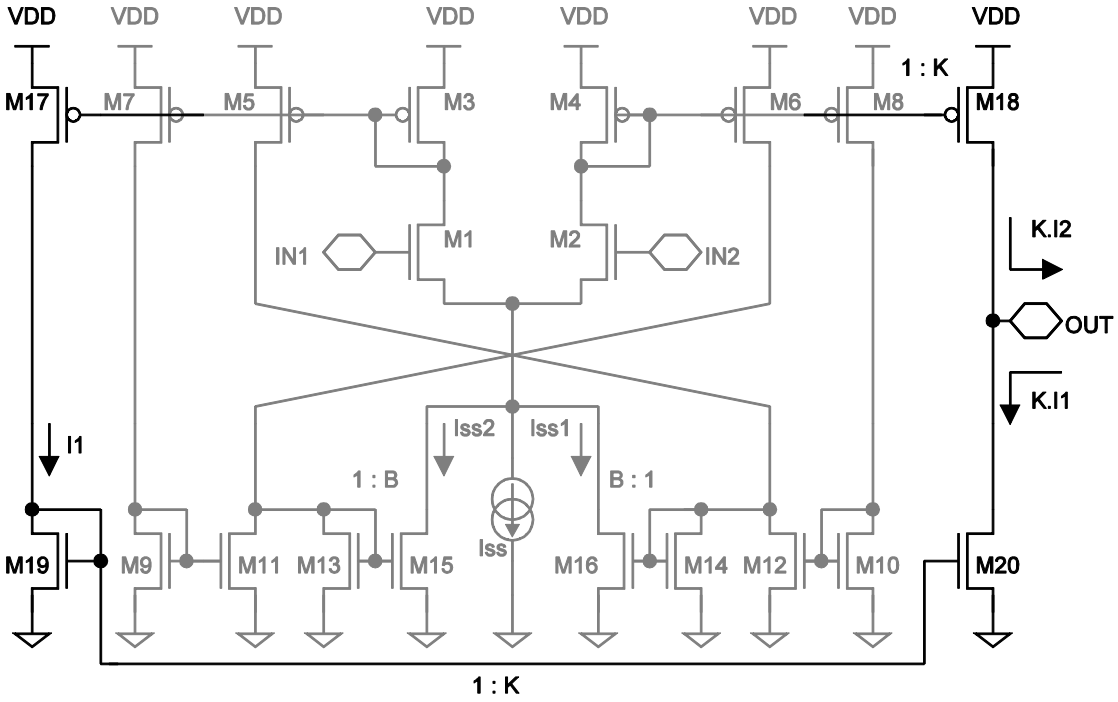

Fig. 4.12: Topology of input stage with output current mirrors [10]

4.5.2 Regulated Cascode

For more gain-enhancement special cascade structure is implemented [11] and [12], which is called regulated cascode. This improving circuit of current mirror features much higher output resistance than other cascode current mirrors and equals output voltage range of them. A basic principle of regulated cascode is shown on Fig. 4.13. In first view an amplifier *A* is neglected and a non-regulated cascode can be described as follows. The transistor M_1 converts the input voltage v_{IN} into drain current i_D which flows through the transistor M_2 to the output node. To achieve a high output resistance $r_{o,}$ it is necessary to suppress the channel-length modulation parameter of M_1 as form an Eq. 3.7. It means that drain-source voltage V_{DS} of M_1 must be kept stable. Therefore, in the regulated cascode the voltage amplifier *A* is used. It regulates V_{DS} to be equal to the bias voltage V_B. Thus, the drain-source voltage V_{DS} of M_1 is stable and the output resistance r_o increases.

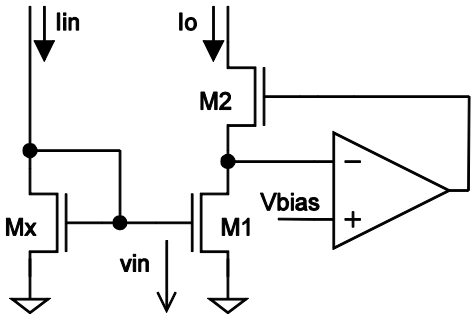

Fig. 4.13: Principle of Regulated Cascode – Amplifier [12]

Fig. 4.14 illustrates the implementation possibility of regulated cascode. The feedback loop and amplifier is implemented by transistor M_3. In this case the M_2 works as follower. Note that the feedback mechanism upon which the stabilization is based works even if M_2 is driven into the triode operating region, which extends the usable range for the output voltage [11].

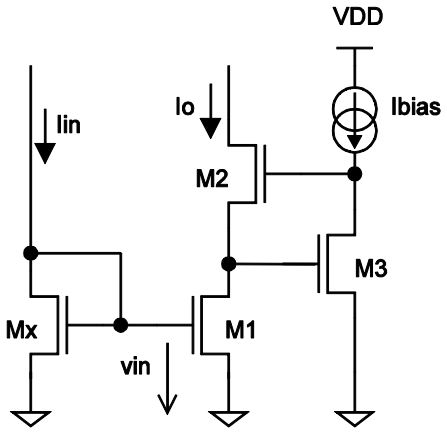

Fig. 4.14: Regulated cascode with NMOS devices [11]

The biasing conditions for circuit are following. It is required that transistor M_1 operates in saturation region, its v_{DS1} must exceed $V_{GS1} - V_{TH}$. It must be achieved even if the input voltage v_I changes. Thus, the maximum value v_I must be inserted for V_{GS1}. The next operating condition for transistors is setting them in strong inversion. This is required to keep a channel size as small as possible for high-frequency circuits.

Assuming that channel sizes of transistor M_1 and M_2 are different. Output voltage decreases from high values until v_{G2} equals to v_O. When output voltage v_O drops under this limit, the M_2 enters into the triode operating region. The feedback amplifier M_3 provides higher gate voltage v_{G2} for M_2 to keep the saturation current through M_1 and M_2. If output voltage v_O decreases even

more and M_2 cannot force the saturation current, the transistor M_1 also enters into the triode operating region. M_3 keeps saturation in operating region during all phases [11]. The minimum output voltage $v_{O,min}$, where the M_2 leaves the saturation region can be obtained as [11],

$$v_{O,min} = V_{GS1} - V_{TH} + V_{GS2} - V_{TH}. \qquad \textit{Eq. 4.19}$$

AC parameter a like output resistance can be obtained in Eq. 4.20 [11]. It is obvious that output resistance of the regulated cascode exceeds the basic cascode by gain factor *A*, which is $g_{m3}(r_{o3} + r_{oi})$. The gain factor *A* equals approximately to one hundred.

$$r_o = g_{m2} r_{o1} r_{o2} \cdot g_{m3}(r_{o3} + r_{oi}) = g_{m2} r_{o1} r_{o2} \cdot A \qquad \textit{Eq. 4.20}$$

A complementary circuit must be implemented for a second half of output stage where PMOS devices are used. Therefore, the output resistance of OTA equals to the parallel combination of r_o NMOS and PMOS cascode. This type of OTA's gain-boosting increases little bit more quiescent power consumption because another biasing is necessary. However, DC gain A_O of OTA exceeds a limit of *120 dB.*

5 Design

The final solutions for OTA design is shown and discussed in this chapter. Several topologies were explored for the thesis. This chapter also summarizes all knowledge which previous chapters were focused on. For design of initial channel-dimension the EKV transistor model, more precisely its inversion coefficient *IC,* is used. Final channel-dimensions trade off theoretical inversion regime and parameters of transistors depend on requirements of proposed OTA. Final dimensions of all transistors of each sub-circuits are summarized at the end of every sub-chapter.

Note that the transistor is four-terminal device, as chapter 3.1 describes. The *bulk* terminals are not illustrated in each schematics due to well-arranged aspect. If the schematic does not show the *bulk* connection, it is provided as follows. The *bulk* of PMOS device is connected to the highest potential in the circuit, it means power-supply voltage (aka V_{DD}). The *bulk* of NMOS device is connected to the lowest potential, the *GND* reference.

5.1 Biasing Circuit

The design process based on the inversion coefficient *IC* and its usage in EKV transistor model, which have been introduced in the previous chapter, will be discussed here. The current mirror should operate in strong inversion (*IC = 10*) because it reaches minimum current mismatch. However, saturation voltage $V_{DS,sat}$ increases with higher inversion coefficient. This causes decrease of the output voltage swing.

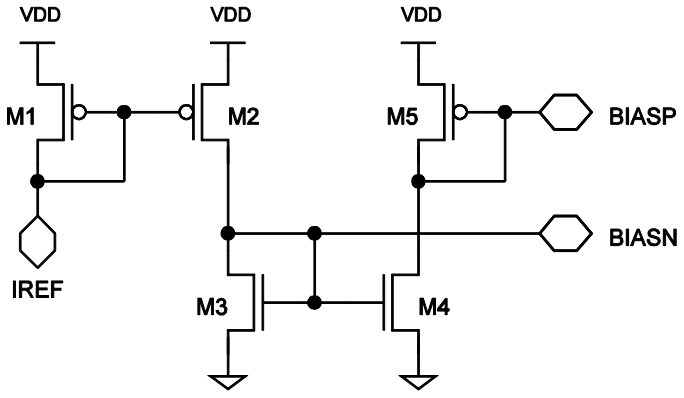

Fig. 5.1: Final topology of biasing circuit

Biasing circuit consists of two current mirrors as Fig. 5.1 shows. The design process is strictly focused on minimization of the current mismatch. The current mirroring cannot achieve unity

with basic topology. Two techniques are implemented for generating more accurate currents. The first one is the sizing of transistor, where large area of transistors can suppress the current mismatch. The second one is the layout technique, where one big transistor is separated into two small ones. The splitting parallel devices have the equal the channel-lengths as the big one but the channel-widths of each one are half.

A technique is called interdigitated layout, where changes in doping at different place on the die are spread between transistors more evenly [1]. The splitting devices are arranged along a common-center. Fig. 5.2 illustrates layout of basic current mirror (Fig. 4.4) where each device is separated in four parallel devices. The common-centroid layout techniques can avoid current mismatch affected by different temperature on die as well.

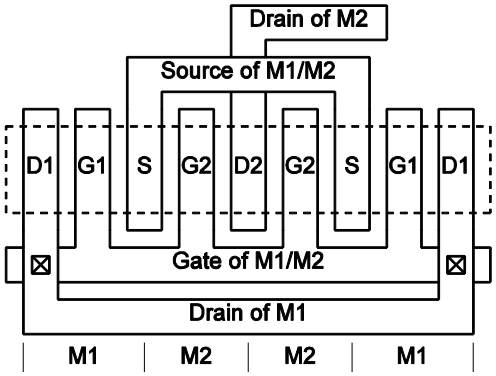

Fig. 5.2: Common-centroid layout of simple current mirror [1]

In Tab. 5.1, where final dimensions of transistors are shown, the parameter *W* means a total channel-width of transistor. Therefore, the in design process the channel-width is divided by multiply factor. Value of this factor is chosen within the design proves as well. Thus initial dimensions of channel-width are chosen about ten times bigger than allowed minimum size. Even more than ten does not dramatically minimize current mismatch, therefore, channel-widths are set *5 µm* for NMOS and *4 µm* for PMOS. If the inversion coefficient *IC = 6* is set, both types of current mirrors can reach approximately $V_{DS,sat} \approx 130\ mV$. An equation for calculation of the channel-width Eq. 5.1 is derived from Eq. 3.13. The gate-source voltage V_{GS3} of M_3 provides the bias voltage V_{BIASN} for all NMOS current mirrors. The voltage V_{GS5} provides the bias voltage V_{BIASP} for PMOS current mirror. References of current flow through the transistors M_3 is $I_{REFN} = 7.14\ \mu A$ and through the M_5 is $I_{REFP} = 7.15\ \mu A$.

$$W = \frac{I_D L}{I_O IC} \qquad \text{Eq. 5.1}$$

Tab. 5.1: Final transistor dimensions of the biasing circuit

Device	IC	I_D [µA]	L [µm]	W [µm]	Comment
M_1	6	2	5	19.6	2 devices in parallel
M_2	6	7	5	68.6	7 devices in parallel
$M_{3,4}$	6	7	5	17	2 devices in parallel both
M_5	6	7	4	54.9	2 devices in parallel

5.2 Input Stage

Initial condition for design corresponds to quiescent current. It means all channel-dimensions are designed with respect to *7 µA* and its multiples. This value of biasing current is chosen with respect to low power consumption in quiescent mode. The input stage affects significantly almost all OTA parameters. During the design process a conflict runs continuously among required parameters in Tab. 4.1. If anyone is tuned precisely the other one becomes unemployable. A balance must be found for the final solution. It has to be suitable for a particular task and purpose of the whole system behavioral.

Let us separate the circuit of input stage (Fig. 5.3) into three sub-circuits, the biasing sub-circuit, the differential pair, and the adaptive biasing sub-circuit.

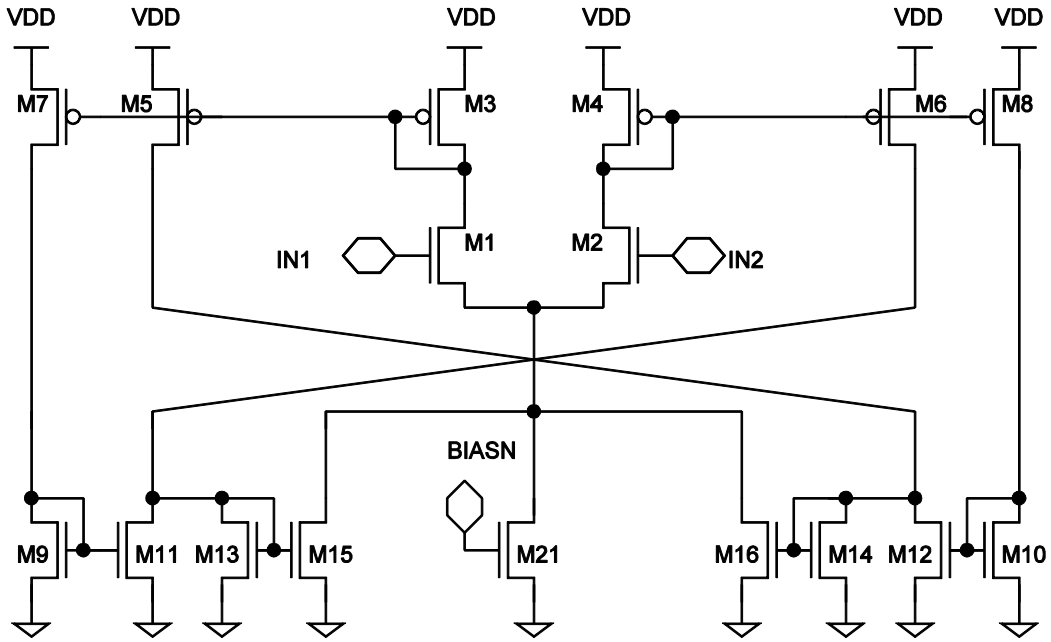

Fig. 5.3: Final topology of input stage

The **biasing sub-circuit** consists of one transistor M_{21} which provides a bias current to diff-pair. The bias voltage V_{BIASN} is controlled in biasing circuit, thus, the transistor dimension M_{21} is twice wider than NMOS transistor in biasing circuit. It obtains a double current gain. Therefore, biasing sub-circuit provides $I_{SS} = 14\ \mu A$, $7\ \mu A$ in each tail of diff-pair. Instead ideal 14 μA, the current flow through the M_{17} is $I_{SS} = 14.07\ \mu A$. The mismatch error reaches to *0.5 %*.

NMOS devices are implemented in the **differential pair**. The technology current I_O of NMOS device is four times higher than that of PMOS one. This causes four times smaller channel-width and reduces an input capacity as much as possible. To maximize transconductance parameter g_m for given biasing current and minimize input offset voltage, input transistors M_1 and M_2 should be weakly inverted ($IC = 0.1$). According to Eq. 3.11, higher g_m reduces the input-referred noise PSD as well. Weak inversion means a wider channel. This increases gate-oxide capacitance. A negative feature is a low transit frequency, thus low speed.

If the inversion coefficient is set lower than *0.1*, a technology limit occurs for given drain current. Therefore, wider input transistors do not cause of increasing transconductance g_m of diff-pair. However, little bit higher inversion coefficient ($IC < 1$) does not affect significantly the transconductance parameter g_m, it decreases about ten percent. The diff-pair transistors work in lightly moderate inversion and the gate-oxide capacitance decreases as well. Thus, the non-dominant pole is modulated into higher frequency. Stability can be improved by that. The unity-gain frequency of the whole OTA also depends highly on transconductance $g_{m1,2}$ as shown Eq. 5.2 [8], where C_{TOT} is strictly given and multiplying coefficient K can be changed in output stage. The requirement *UGF* should achieve around *18 MHz* which is not small value. Thus, the diff-pair transistors work in lightly moderate inversion as shown in Tab. 5.2.

$$UGF = \frac{g_{m\,OTA}}{2\pi \cdot C_{TOT}} = \frac{g_{m1,2}K}{2\pi \cdot C_{TOT}} \qquad \textit{Eq. 5.2}$$

The **adaptive biasing** sub-circuit is implemented by PMOS current mirrors and NMOS current mirrors. The most critical OTA parameters which are affected by PMOS current mirrors are systematic offset and non-dominant pole. These parameters demand trade-off. To minimalize the systematic offset it is required a large transistor area of PMOS devices $M_{3,5,7}$ as well as $M_{4,6,8}$. Into nodes (drain M_1 or M_2) where the PMOS current mirrors are connected are also formed the non-dominant pole by gate-oxide capacity (Eq. 4.18). There are summarized six parallel gate-oxide capacity in the sub-circuit (including multiplying coefficient *K* of output stage). Thus, the

design priority is to focus on forming of the non-dominant pole at the expense of systematic offset. As previous chapter describes, the frequency of the non-dominant pole must be at least three times higher than unity-gain frequency for achieving stability without any overshoot. Therefore, the channel-lengths of PMOS current mirrors are designed twice larger than technology process allows. Because setting minimum size could bring significant mismatch error due limits of the technology process. Both types of current mirrors (PMOS and NMOS) work in strong inversion (*IC = 10*).

Channel sizing of transistors M_{15}, M_{16} is very important. The adaptive bias current I_{SS1}, respectively the current I_{SS2} are generated there. As it is described in the previous chapter. If the *B* coefficient is set to unity, it suppresses the slew-rate limitation. So, the transistor M_{15} is matched with M_{13}. The transistor dimension of M_{16} must be same as M_{14} as well.

Tab. 5.2: Final transistor dimensions of the input stage

Device	***IC***	***I_D [µA]***	***L [µm]***	***W [µm]***	***Comment***
$M_{1,2}$	*1*	*14*	*1*	*40*	*High transconductance*
$M_{3,5,7}$	*15*	*14*	*0.78*	*8.5*	*Non-dom. Pole, reducing C_{GS}*
$M_{4,6,8}$	*15*	*14*	*0.78*	*8.5*	*Non-dom. Pole, reducing C_{GS}*
$M_{9,11,13,15}$	*10.1*	*14*	*1.5*	*6*	*Reducing C_{GS}. , non-dom. pole*
$M_{10,12,14,16}$	*10.1*	*14*	*1.5*	*6*	*Reducing C_{GS} , non-dom. pole*
M_{21}	*6*	*14*	*5*	*34*	*Depends on biasing current*

5.3 Output Stage

The output stage is designed with respect to connected load. It has capability which transforms the differential current into output node, as well as provides high output resistance R_O. The DC gain A_O is calculated by Eq. 4.18 where output resistance R_O has significant consequence.

The output stage combines two sub-circuits, the output current mirror and regulated cascode. These sub-circuits are highlighted in Fig. 5.4. This schematic also illustrates topology of the proposed OTA. Schematics from Cadence showing dimensions of devices and annotations of DC operation points can be found in Appendixes 8A.1, 8A.2 respectively.

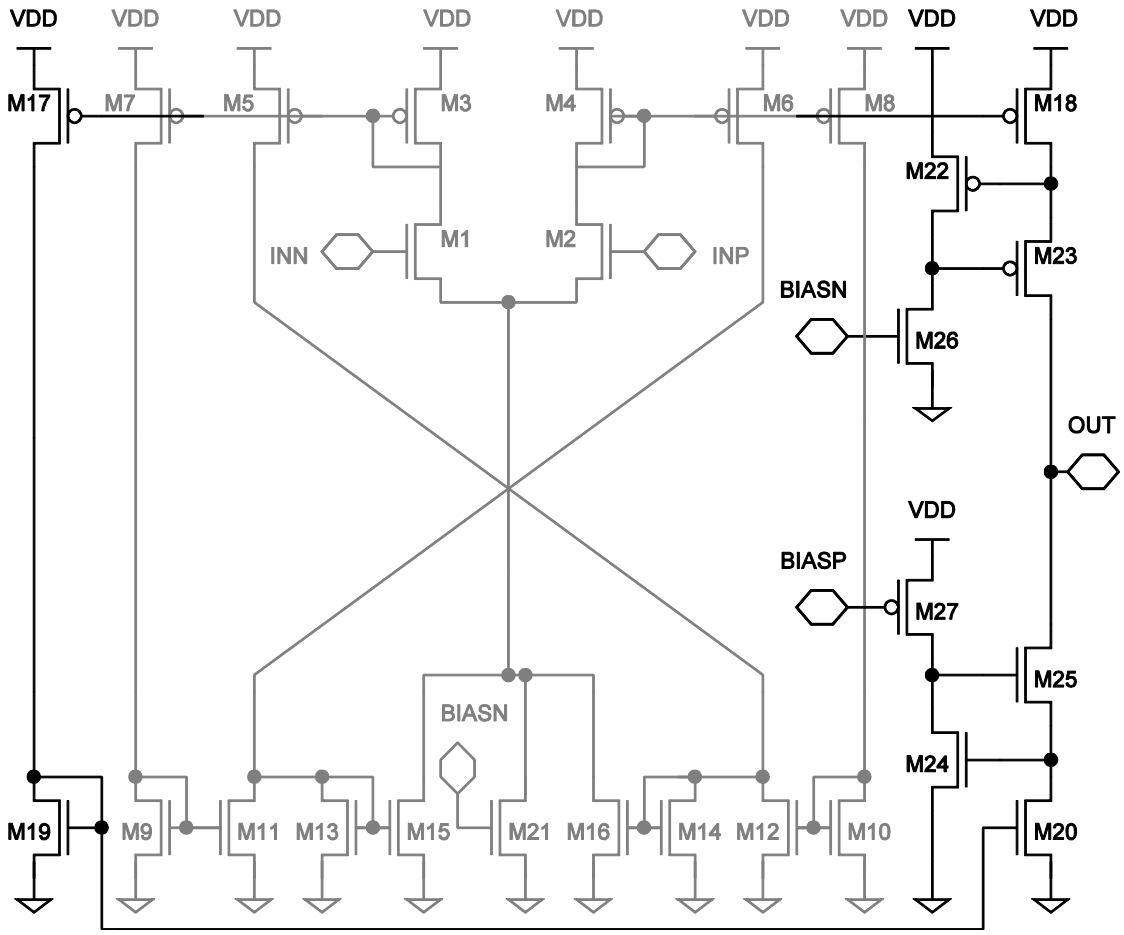

Fig. 5.4: Final topology of output stage

The first output sub-circuit is **current mirror.** The PMOS transistor M_{18}, which is connected directly to M_2 drain node, drives an output load by current K times larger than differential current i_{D2}. The multiply coefficient *K* is chosen three. Thus current of *21 μA* flows through the output stage in quiescent mode. Multiplying coefficient is three. This is enough for increasing the differential current along with the total power consumption is kept about *90 μA.* In the second half of the output stage, the differential current i_{D1} is mirrored by complementary current mirrors M_3-M_{17} and M_{19}-M_{20}. The transistor M_{20} provides the output current and it is three times wider than M_{19} as well. One big transistor is not design due to maximize dimension accuracy during technology but three devices in parallel are designed. In Eq. 5.3 [16] it can be shown the neglecting dimension mismatch, where *e* is technology accuracy and *W = L*.

$$3 = \frac{3 \cdot (W + e)}{L + e} \neq \frac{(3W + e)}{L + e} \qquad \textit{Eq. 5.3}$$

DC gain A_O of diff-pair with adaptive biasing and with basic current mirror achieves only *55 dB*. Therefore, it must be enhanced at least *65 dB* to reach the required DC gain *120 dB.* The **regulated cascode** can provide additional gain *65 dB* because it increases dramatically the output resistance R_O. The first necessary devices in the regulated cascode are M_{26} and M_{27} as current sources for biasing of local amplifiers. The bias current is selected to *7 µA*, thus, the sizing of M_{26} and M_{27} depends on biasing of circuit block. So, the design rules are the same as when the unity current gain should be obtained. The inversion coefficient for pairs M_{22}, M_{23} and M_{24}, M_{25} is selected *IC = 4*. It respects minimization of the saturation voltage $V_{DS,sat}$ of each transistors. $V_{DS,sat}$ can be achieved approximately $V_{DS,sat} \approx 100\ mV$. The output voltage swing rises as well. The range is V_{SS} + *720* and V_{DD} - *750.* In tails, where M_{22} and M_{24} work as a feedback loop and amplifier, the maximal currents of *7 µA* flow. Thus, dimensions of transistor are smaller than for M_{23} and M_{25}. This is caused by drain currents in M_{23} and M_{25} which are equal to *21 µA* in quiescent mode and even more during AB mode. Note that OTA gain is enhanced by extreme output resistance, thus, the noise performance is formed by ac characteristic.

Tab. 5.3: Final transistor dimensions of the output stage

Device	**IC**	**I_D [µA]**	**L [µm]**	**W [µm]**	**Comment**
M_{17}	15.1	14	0.78	8.5	Reducing C_{GS}
M_{18}	15.1	42	0.78	8.5	3 devices in parallel
M_{19}	10.1	14	1.5	6	Reducing C_{GS}
M_{20}	10.1	42	1.5	6	3 devices in parallel
M_{22}	4	7	0.5	10.3	Low $V_{DS,sat}$
M_{23}	4	21	0.5	31	3 devices in parallel
M_{24}	4	7	0.5	2.5	Low $V_{DS,sat}$
M_{25}	4	21	0.5	7.5	3 devices in parallel
M_{26}	6	7	5	17	Depends on biasing current
M_{27}	6	7	4	54.3	Depends on biasing current

6 Simulations

This is the most important chapter where final results are presented. For each behavior analysis there are illustrated schematic of testbench circuit, as well as plotted characteristic or graph. There are also discussed achieved parameters of proposed OTA. At the end of chapter in Tab. 6.2 all simulated parameters of OTA are summarized. The common simulation setup does not change for all simulations. Technology process, voltage, and temperature vary only in corner simulations. The nominal voltage conditions for simulations are supply voltage $V_{DD} = 3.3$ V, common mode voltage $V_{CM} = 1.65$ V, reference level $V_{SS} = 0$ V. The next simulation setup is temperature $T = 27$ °C and typical technology processes for NMOS and PMOS devices.

6.1 AC Behavioral

The proposed OTA works in SC network, where C_{TOT} can vary in range $1 – 7$ pF. The C_{TOT} depends on connected capacitor C_{DAC} and C_F. During the feasibility study optimal ratios between C_{DAC} and C_F have been analyzed. There are 4/8 and 4/40, the C_{TOT} is calculated approximately according to Eq. 4.4 as *3 pF*, *4 pF* respectively. Thus this values are used in simulation as capacitive load.

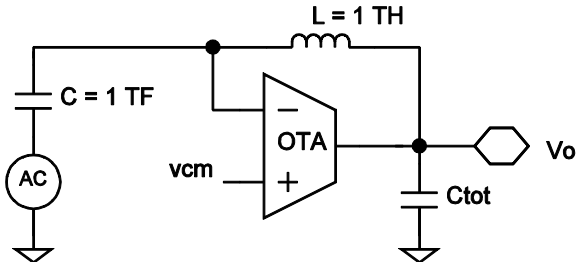

Fig. 6.1: Open loop testbench for AC analysis

An open loop AC analysis is simulated with AC killer (Fig. 6.1). This method uses a parallel combination of a capacitor and a coil in feedback loop with significant unreal value *C =1 TF* and *L = 1 TH*. However, at first of all, a positive input must be connected to V_{CM}. Before ac simulation, the DC operation point must be set. It means that the output of OTA loads a negative input via feedback loop to achieve the same voltage as V_{CM} is. The voltage difference cannot be reached accurately zero because the systematic offset is *56 µV*. That parameter is simulated during the design process. The coil impedance is zero for DC signal component, thus, the DC operation point can be set via feedback loop. The capacitor works as decupling against ground. Open loop for AC signal component is provided by very high coil impedance and the feedback loop is disconnected. The AC source loads the negative input through negligibly low capacitor impedance. The complete testbench simulation can be found in appendix 8A.3.

AC characteristic shows phase margin, gain margin, and shape for stability study of OTA. The best value of phase margin is *63 degrees, w*hich provides fast and smooth settling of the output voltage without any oscillations. One of the key task during the OTA design, which takes many simulation runs, is to achieve increase of the non-dominant pole. This implies reduction of sizes of transistors in adaptive biasing mirrors to achieve minimal gate-source capacitance.

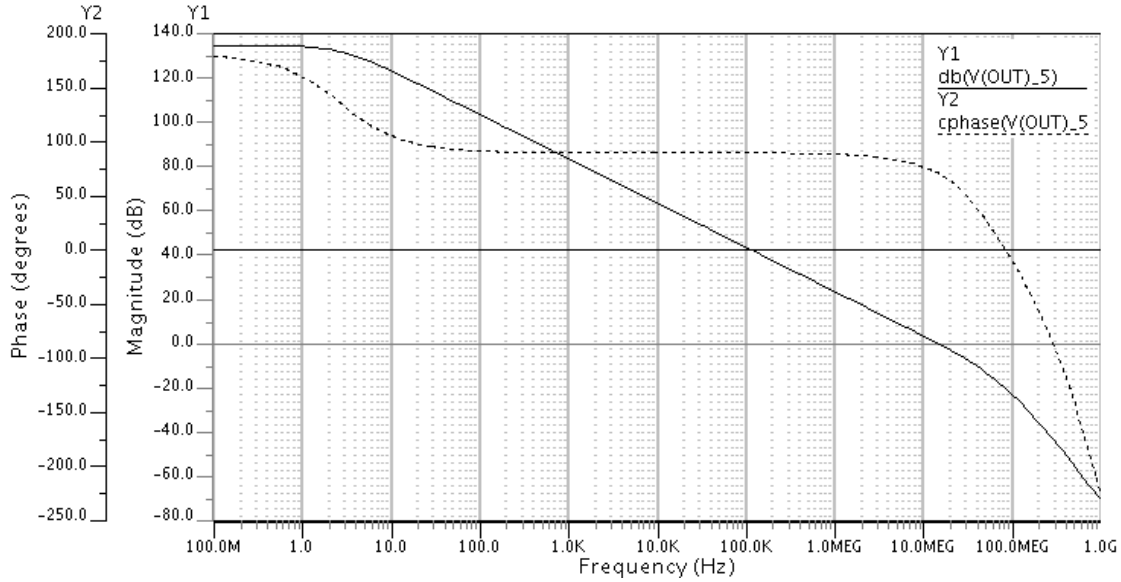

Fig. 6.2: Open loop AC characteristic for C_{TOT} = 4 pF

Tab. 6.1 summarizes AC parameters for nominal conditions as well as the worst and the best case. The nominal values are simulated as it was already described. The worst and the best case are detected by corner simulations. The minimum number of corner simulations is 45, where power supply voltage is changed in steps *2.7 V, 3.3 V, 3.6 V* the temperature is varied in steps *-40° C, 27° C, 125° C* and technology process corners implement *TT, FF, FS, SF, SS* combination. These shortcuts represent how the devices are doped. There exist three corners: T – typical, F – fast and S – slow. The first char of shortcuts describes donating of NMOS device and the second one describes donating of PMOS device. The control script code, AC characteristics, and results lists including parameters for all corners can be found in Appendixes 8A.4, 8A.5, 8A.6 and 8A.7.

Tab. 6.1: AC parameters

C_{TOT}	3pF			4pF		
	Worst/min	nominal	Best/max	Worst/min	nominal	Best/max
DC gain [dB]	128.5	134.7	138.4	128.5	134.7	138.3
Gain bandwidth [MHz]	15.6	18.9	21.9	11.9	14.4	16.7
Phase margin [deg]	63.9	65.2	67.1	70.1	71.1	72.6
Gain margin [dB]	17.6	18	18.6	20	20.5	21.1

The nominal AC parameter can be discussed as follows. The DC gain exceeds significantly the required one, this is caused by regulated cascode. The unity gain frequency depends on capacitive load of course. The required *UGF = 18 MHz* can be reached with $C_{TOT} = 3$ *pF* (capacitor's combination *4/8 pF*) - for higher capacitive loads the parameter *UGF* decreases. According to Eq. 4.6 the UGF should be at least *15 MHz*. The phase margin does not alternate significantly, the maximal dispersion is 2 degrees. For combination of capacitor *4/40 pF* the phase margin equals approximately 71 degrees. To achieve a high value of the phase margin and thus good stability it is necessary to precisely design current mirrors in the adaptive biasing sub-circuit.

Another parameter in frequency domain is called **common mode rejection ratio**. This parameter describes how the OTA suppresses the common mode voltage. If the same signal is connected on both input, amplifier should not reacted in ideal case. However, the Fig. 6.3 illustrates testbench for simulation of the common mode gain A_{CM}. DC component V_{CM} sets the DC operation point and AC component influences both inputs. The CMRR can be calculated as [1]

$$CMMR = 20log\frac{A_D}{A_{CM}}, \qquad \textit{Eq. 6.1}$$

where A_D is differential gain simulated in previous test, A_{CM} common mode gain.

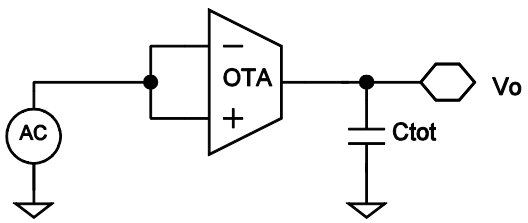

Fig. 6.3: Testbench for common mode gain A_{CM}

The result of common mode rejection ratio is plotted in the Fig. 6.4. The very high differential gain, simulated in previous test, causes the high CMRR - approximately *148 dB* at DC level.

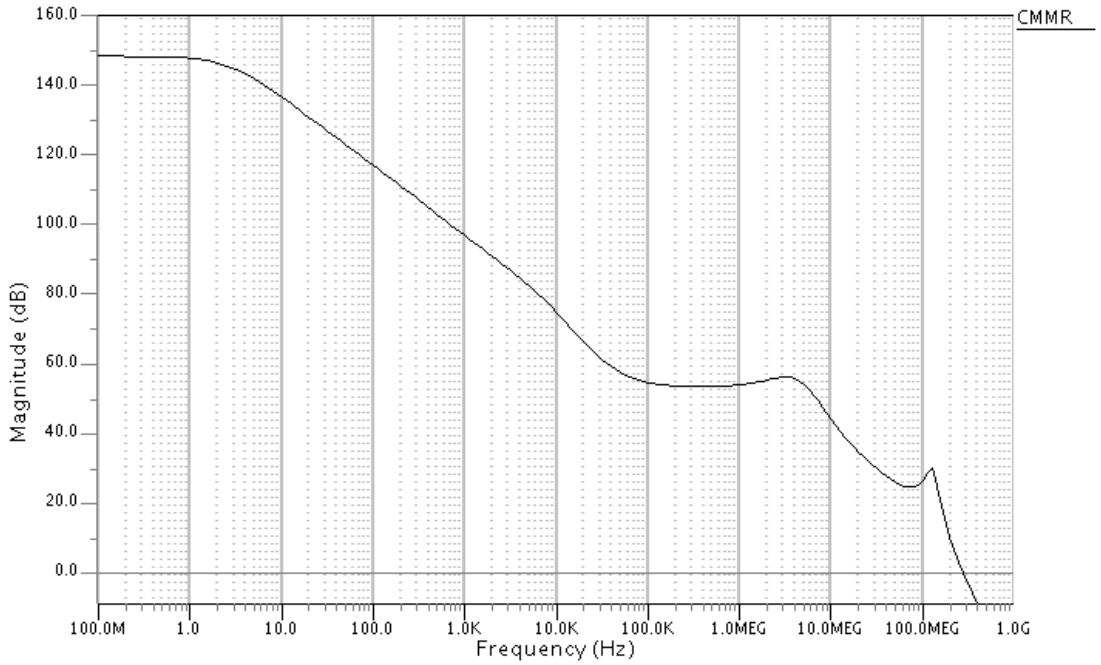

Fig. 6.4: Common mode rejection ratio characteristic

6.2 Dynamic Behavioral

The transient analyses describes how the proposed OTA behaves in time domain. During previous simulation of AC characteristic the DC operation point is calculated for quiescent mode. Small biasing current 7 μA flows through both transistors in differential pair. Thus, this case does not respect the condition in AB class mode, when the biasing current significantly raises. The g_m of OTA increases as well as *UGF* parameter does. The phase margin decreases and the output voltage could oscillate. The best way how to find out if OTA is stable or not is launching several transient simulation runs. As it can be seen in Tab. 6.1, the phase margins tested by corner simulations alternate maximally 2 degree from nominal value. Therefore, all transient analyses are simulation with nominal conditions.

The first parameter describing behavior in time domain is called **slew-rate.** It should be as high as possible. It implies for this design task, at the end of every *166 ns* time slot the output of OTA must achieve the final voltage value safely. The testbench schematic is in Fig. 6.5, where

amplifier is connected as unity gain amplifier. This case is critical state for studying oscillations and settling the output voltage response. The input voltage changes by *1 V* positive step and *1 V* negative step. The duration of each step equals *166 ns*. As capacitive load the worst case is chosen, $C_{TOT} = 4\ pF$. It can be observed that the proposed OTA operates in class AB mode by this testbench circuit.

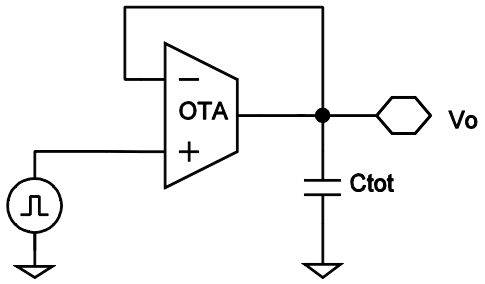

Fig. 6.5: Testbenches for dynamic analysis of slew-rate

Results of slew-rate simulation are plotted in Fig. 6.6a. Let us firstly discuss the response of one voltage step. Raising and falling time is not equal. The falling time is higher, this is caused by different problems. The first one is that the signal for negative step has to pass two current mirrors instead one for positive step. More parasitic capacities occur there. The second one is that there are implemented the NMOS differential pair and the NMOS biasing current source. For decreasing common mode input, the transconductance g_m reduces as well. Thus, differential current in diff-pair decreases and slew-rate is slower for falling edges (Fig. 6.6a). This also relates to common mode input range. If input voltage is very low, this low level cannot keep NMOS diff-pair and NMOS biasing current source in saturation [17]. The slew-rate can be quantified as follows. The proposed OTA achieves *63 V/µs* for positive step and *51 V/µs* for negative step.

As it can be seen in Fig. 6.6a and in detail (Fig. 6.6b), an overshoot on the output voltage occurs. This is provided by class AB mode when output current raises and g_m of OTA increase as well. Obviously, the phase margin does not reach the value 71 degrees during the class AB mode. However, with decreasing differential voltage, the output current and transconductance g_m approach quiescent mode and OTA behaves as AC characteristic illustrates. This feature provides smooth settling, and at the end of the step, the output voltage is settled with difference given by systematic offset 56 μV. Also, the high gain causes required settling because basic topology of OTA without any gain-enhanced sub-circuit cannot reach it. The bottom plot of Fig. 6.6a shows when class AB mode works. Instead of maximal *14 µA*, the adaptive biasing sub-circuit provides more than ten times higher value of the differential current during input edges. There are very

fast raise and fall of current thanks to precisely designed current mirrors in adaptive bias sub-circuit. It also can be seen that total output current reaches three times higher value than differential current. This is done by multiplying coefficient K of output current mirrors.

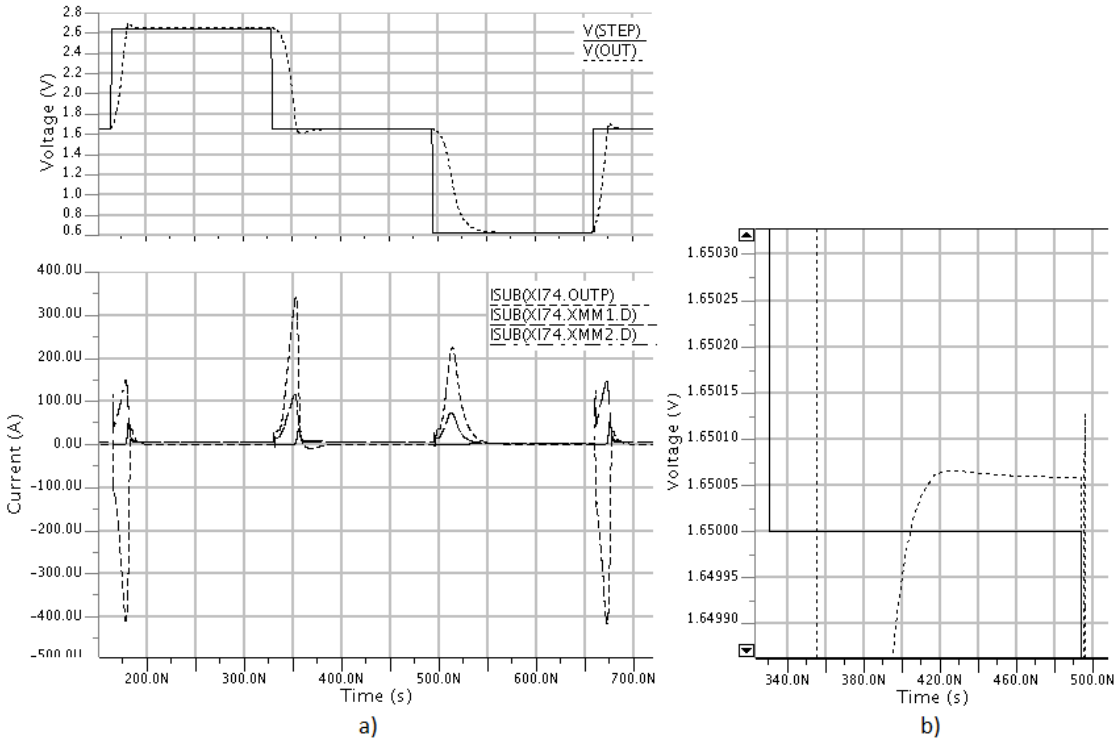

Fig. 6.6: Transient analysis a) slew-rate and output current, b) settling detail

The previous testbench is typical for quantification of slew-rate parameter of amplifier in general term, but the proposed OTA does never work with unity gain in sigma-delta modulator. The designed OTA works in switching capacitors network. This testbench is illustrated in Fig. 6.7, where duration of a step is also set *166 ns*. The capacitor C_F alternates *8 pF*, *40 pF* and $C_{DAC} = 4$ *pF* for both case. The switch bypasses the feedback capacitor C_F to discharge CF and set an initial condition in circuit as well as DC operation point of amplifier at the beginning of the simulation. The switch opens during transient analysis. The testbench circuit corresponds with real usage.

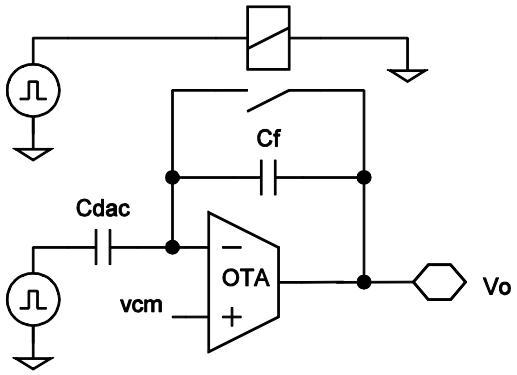

Fig. 6.7: Testbenches for dynamic analysis of SC network

The transient analysis of SC network with C_{TOT} variations results are as follows. Output currents are capable to drive loads in time. An overshoot occurs at the output voltage response. However, it can be seen in detail in Fig. 6.8b that the OTA in SC networks achieves smooth settling as well and systematic offset is also 56 *µV*. The settling output values are ensured by capacitor divider and corresponds to Eq. 4.1. The difference of potential should equal *1/4* V_{DD} for the case with capacitors ratio *4/8 pF*. Thus, the output voltage responses are *0.825 V* and *2.475 V*. For the second case, when capacitors ratio is *4/40 pF*, the difference of potential should equal *1/20* V_{DD}. Thus, the output voltage responses are *1.485 V* and *1.815 V*.

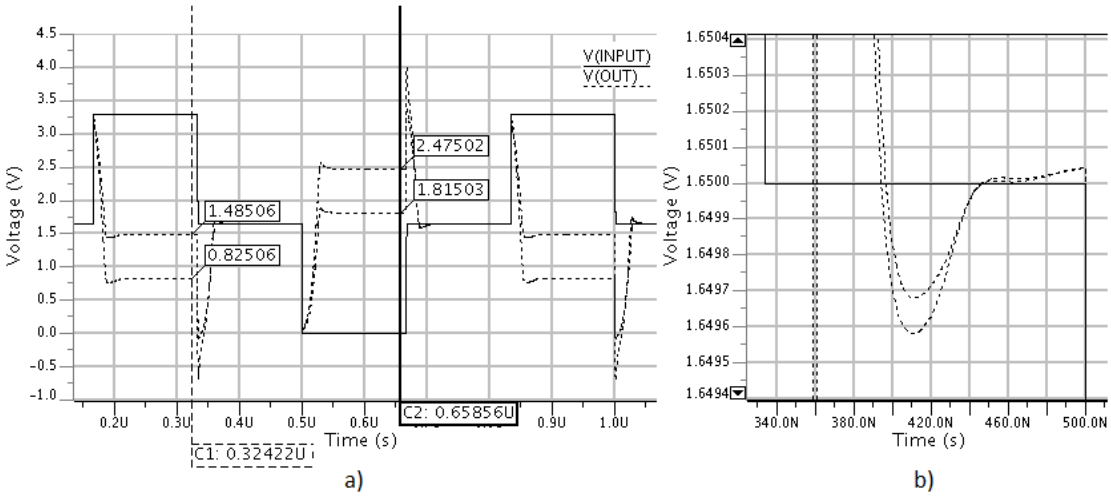

Fig. 6.8: Transient analysis a) SC network with C_{TOT} variations, b) settling detail

6.3 Noise Performance

Other important parameters describe noise performance. The first one is called output AC noise. Note that product that AC characteristic modulates the output AC noise is an input referred noise. At the beginning of design process the same testbench is chosen circuit for noise simulation as simulation of AC characteristic (Fig. 6.1). Method with AC killer provides completely wrong results of noise performance. It is caused by devices making the open loop feedback. Unfortunately, this testbench circuit (for noise simulation) was mostly used during design process. The methodology of noise simulation was changed during finishing of this work. It is described below. This is one of the reason why noise performance does not pass very well.

The new proposed method for output AC noise simulation is illustrated in Fig. 6.9. The key device in the circuit is VSTB source and its command for loop stability analysis. The classical method for stability analysis is to break the feedback loop at an appropriate point on AC analysis, while maintaining correct DC conditions. This means that the loop must be terminated with the appropriate impedance it 'sees' looking at the loop input [18]. It is necessary to define a source of noise and its noise frequency band. These parameters are common for the AC and noise simulations. This is included in control script code which can be found in appendix 8A.8. The capacitors placing corresponds with real usage. The switch bypasses the feedback capacitor C_F to discharge CF and sets an initial condition in the circuit. The DC operation point of amplifier must be saved at the beginning of the simulation. This testbench circuit also simulates AC characteristic. It is necessary to mention that AC characteristics simulated by AC killer are equal to AC characteristics simulated with LSTB command.

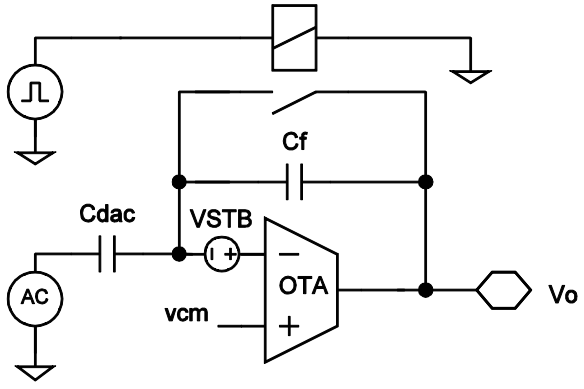

Fig. 6.9: Testbenches for noise analysis of proposed OTA

To quantify amount of noise root mean square is used of spectral noise density of output noise (Eq. 6.2). Circuit of proposed sigma-delta modulator contains chopping scheme of the feedback capacitor C_F, which is not depicted in this case. It causes that noise below the chopping frequency is attenuated, therefore, the frequency range of RMS can be considered between *100 kHz* to *1 GHz*.

$$RMS_{Onoise} = \sqrt{\int_{f_1}^{f_2} SND^2(f)df} \qquad \textit{Eq. 6.2}$$

The spectral noise density of the output is plotted in Fig. 6.10, where two curves are compared. The first one appertains to the proposed OTA and the second one appertains to initial amplifier. This amplifier is implemented in feasibility study and proposed OTA should replace it. It is obvious that the proposed OTA has better noise performance. Flat characteristic in middle of frequency range is caused by output regulated cascode. The form of RMS, which basically sums an area under the curve, has been employed. The value of RMS noise of the proposed OTA equals to *165 µV*. The value of RMS noise of the initial amplifier is *310 µV*, so the proposed OTA achieves approximately *47 %* improvement in the output noise at frequency range from *100 kHz* to *1 GHz*. Note that findings are simulated for open loop case.

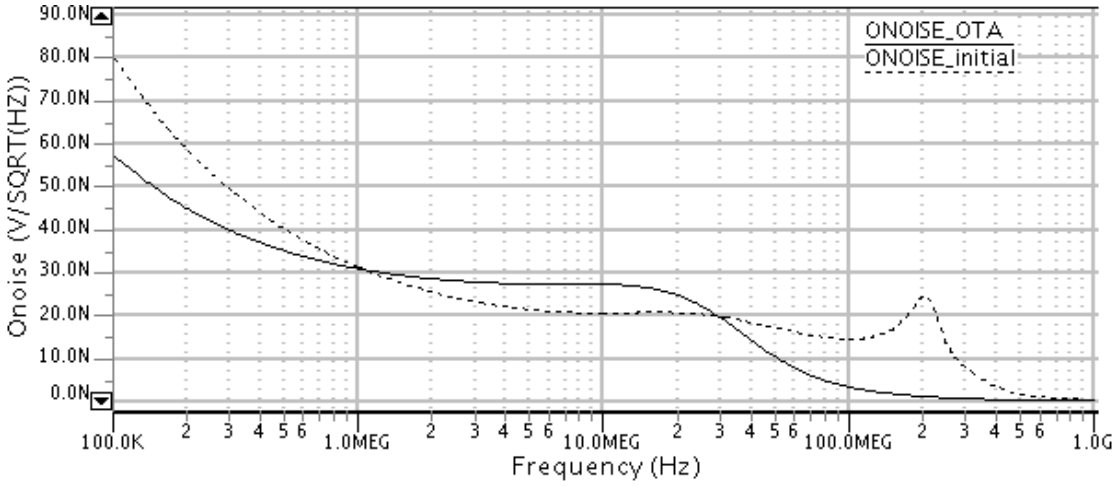

Fig. 6.10: The output spectral noise density of the proposed OTA and comparing amplifier

Another solution how to confirm noise performances is to embed the proposed OTA into sigma-delta converter and launch at least 20 noisetran runs. There must be also defined the range of the noise frequency band. The range is set from *0 Hz* to *200 MHz*. Setting a higher frequency

does not add a significant noise error according to Fig. 6.10. Setting zero frequency accelerates significantly an algorithm of calculation. The number of runs accurate results of the simulation [18]. The circuit of the whole system of sigma-delta converter cannot be published, because it contains a ST confidential information.

Details of noisetran can be found in Fig. 6.11, where results are plotted for capacitors ratio *4/8 pF* and 8 accumulation pairs. Note that OTA is not the only block with the noise performance in the sigma-delta modulator. However, it adds significant amount of noise. The difference of curves *2.13 mV* (Fig. 6.11a) is probably noise component sampled through an input switch. Accumulations imply that the signal passes through the sigma-delta modulator 16 times and noise could be summarized. The noise folding occurred. Noise from higher frequency band is folded around of DC component. Thus noise component is sampled as DC value [19]. In noise transient analysis a peak-to-peak value of curves in time domain should correspond with relation between RMS noise and peak-to-peak value. The suitable convert is *6.6 times the RMS value* which is exceeded only 0.1 % of the time [20]. Thus, sampled deviation can reach hundreds of microvolts. Noise component has not determination. It should be added in the first sampling action and neglected during the second one. Sigma-delta modulator accumulates even more than 16 times, it can be 128 accumulations. Therefore, the noise component brings a significant error of few millivolts (Fig. 6.11b) in converting process. To achieve a lower noise error the capacitors ratio *4/40 pF* can be used. The noise component decreases 10 times but output signal decreases as well. However, a signal-to-noise ratios are equal for both capacitor variations.

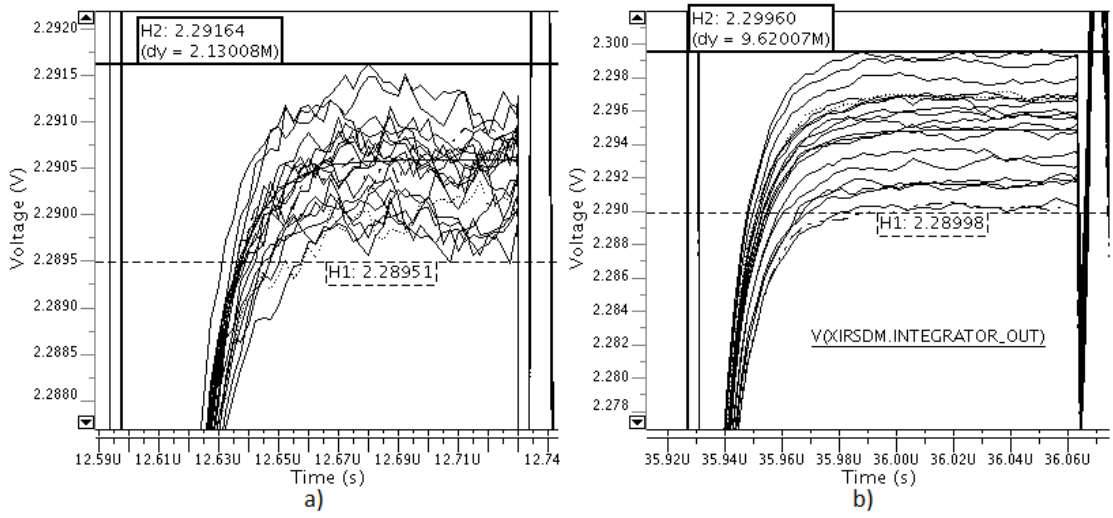

Fig. 6.11: 20 runs noise transient analysis of sigma-delta modulator

6.4 Summary of Results

All parameters have been discussed in previous sub-chapters in detail. Thus, recapitulation is summarized in Tab. 6.2 , where all parameters correspond to the worse case of capacitors ratio. It means $C_{DAC} = 4\ pF$ and $C_F = 40\ pF$ or $C_{TOT} = 4\ pF$ as one equivalent capacitor. However, noise performances are simulated for $C_{DAC} = 4\ pF$ and $C_F = 8\ pF$. Lower capacitor's ratio causes higher unity gain frequency. It provides worse value of RMS noise but SNR remains.

Tab. 6.2: Summarized parameters of proposed OTA

Parameter	*Worst case value*	*Nominal value*
DC gain	*128.5 dB*	*134.7 dB*
Unity gain bandwidth	*11.9 MHz*	*14.4 MHz*
Phase margin	*70.1°*	*71.1°*
Gain margin	*20 dB*	*20.5 dB*
PSSR *(DC level)*	*141.8 dB*	*148 dB*
Slew-rate	*53 V/µs*	*61 V/µs*
Systematic offset	*800 µV*	*56 µV*
Output swing	*Vss + 780 mV ÷ V_{DD} – 810 mV*	*Vss + 720 mV ÷ V_{DD} – 750 mV*
RMS noise	*192 µV*	*165 µV*
Quiescent supply current	*107.6 µA*	*105.7 µA*
Supply voltage	*2.7 V*	*3.3 V*

7 Conclusion

Before results of operational transconductance amplifier are discussed, it necessary to mention how the EKV model parameters extraction is well done step. It is very helpful for first-order hand design. Without any overstatement, using simply EKV models allow to start and finish this work. Especially if during design process final transistor dimensions must be redesigned many times.

The proposed operational transconductance amplifier can be summarized as follows. All parameters for settling of the output voltage response are achieved properly. The DC gain of around *130 dB* exceeds significantly the required *120 dB*, this is caused by regulated cascode sub-circuits. Even if this enhanced gain solution decreases the output swing, the proposed OTA settles the output voltage response correctly for all supply voltages and capacitive load variations. The proposed OTA also achieves stability over all technology process, supply voltage, and temperature corners without any additive compensative method. Unity gain frequency specified in the first approximation during task study was *18 MHz*. This value is exceeded unfortunately only for half capacitive load variations. This value is also required for good settling of the output voltage response, but previous parameters show properly settling as well. The *UGF* is raised dynamically during class AB mode. Therefore it is not necessary to reach strictly the defined *UGF* in DC operating point. Class AB configuration, implemented by adaptive biasing sub-circuit, also provides fast and safe driving all capacitive load variations. Of course the much monitored parameter as power consumption passes as well. The quiescent supply current is only *90 μA* for OTA circuit and *106 μA* including biasing circuit.

On the other hand, the lower OTA bandwidth modulates better noise performance. The value of RMS noise of the proposed OTA equals to *165 μV.* It achieves approximately *47 %* improvement in comparison with initial amplifier in operating frequency band. It is progress but implementation the proposed OTA into the sigma-delta converter cannot be recommended due to behavior in noise transient analysis. Design OTA, which provides noise error maximally one LSB, would take more development and deeper study.

8 References

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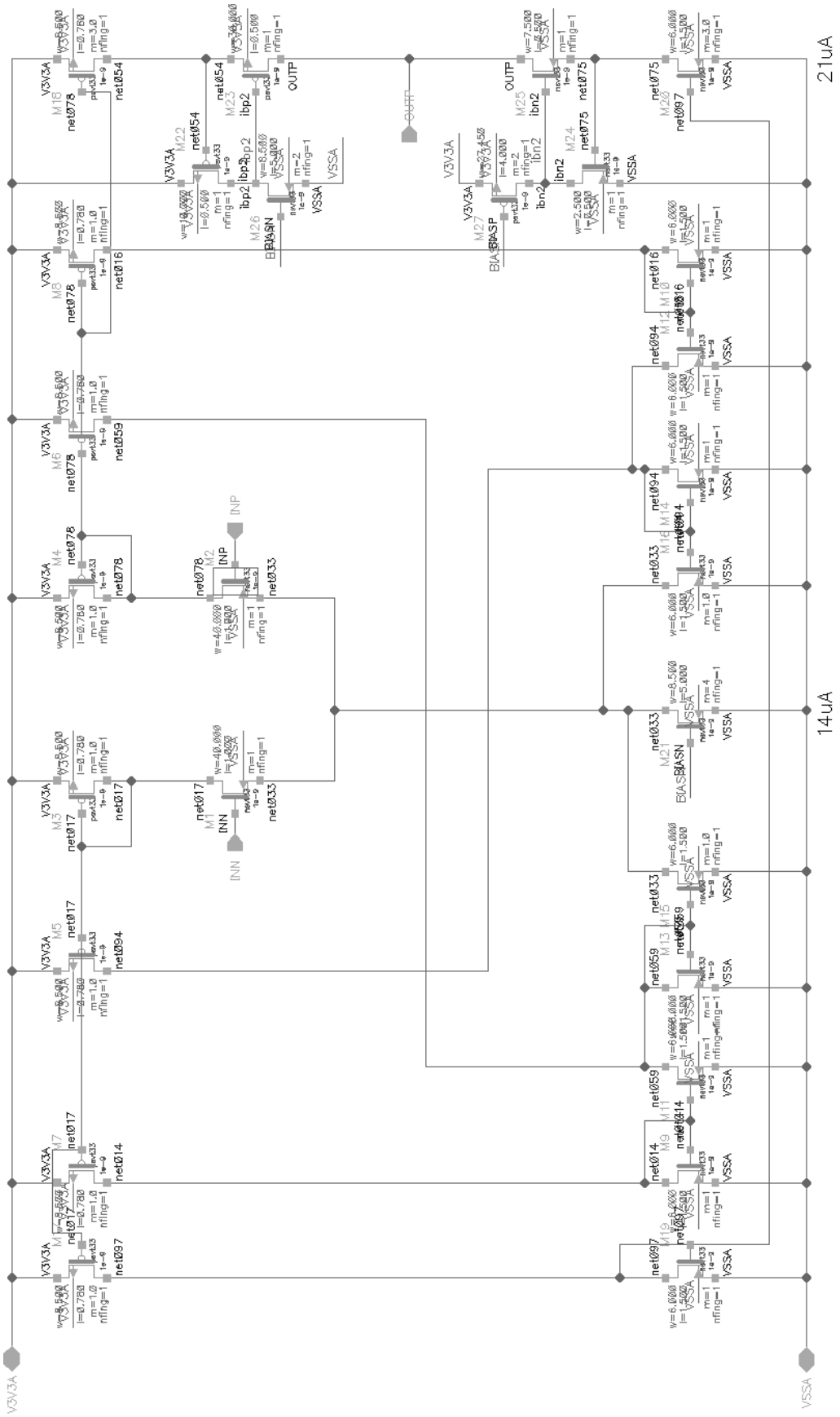
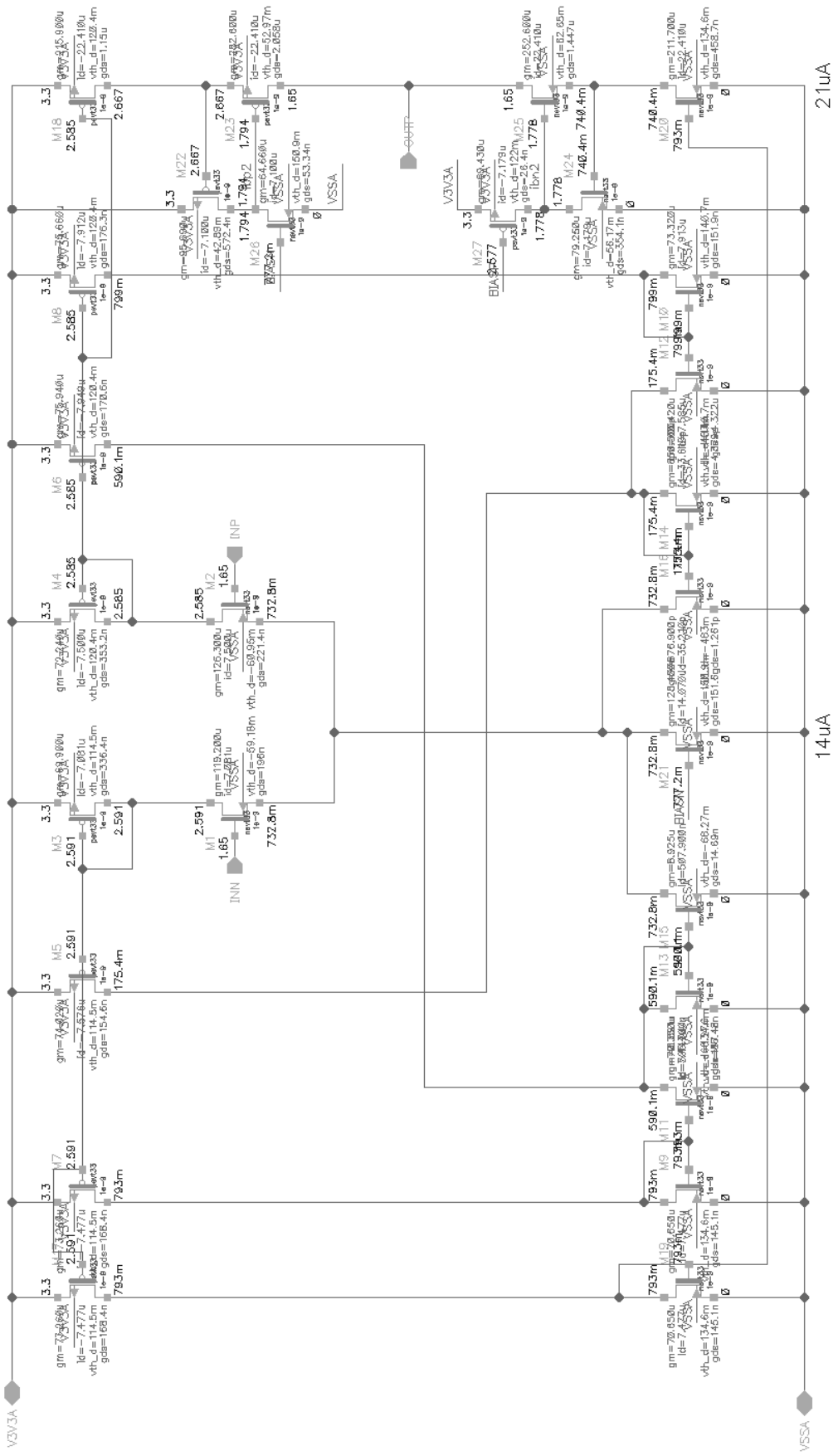
Appendix

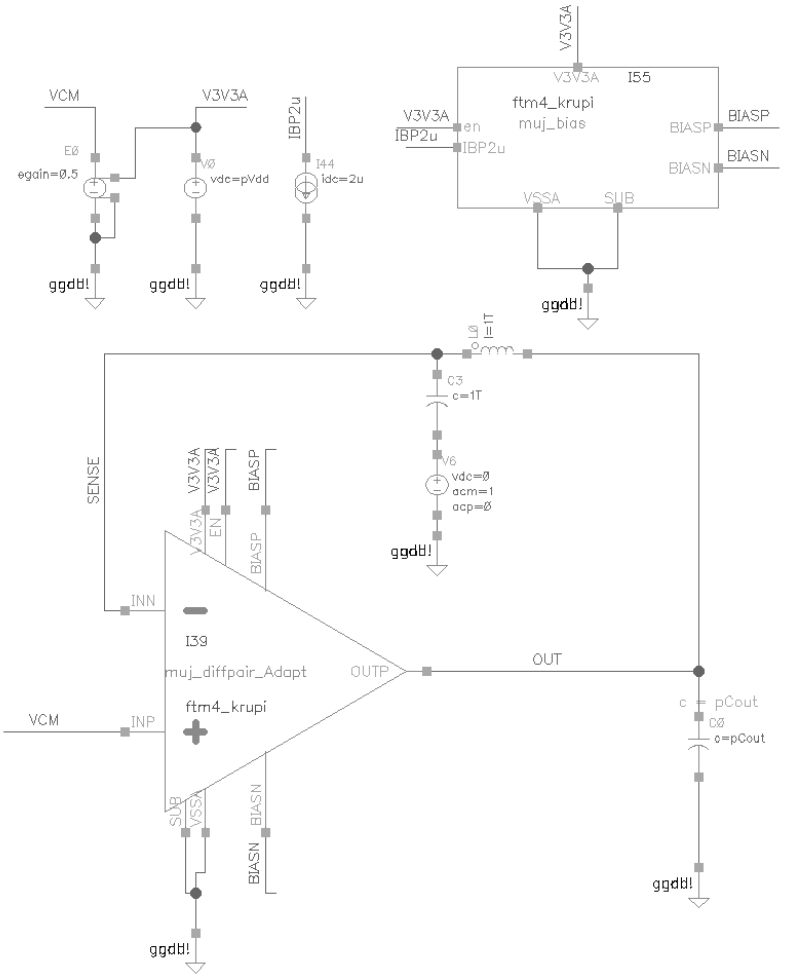
A.1 OTA schematic from Cadence with devices dimensions



A.2 OTA schematic from Cadence with DC operational point annotation



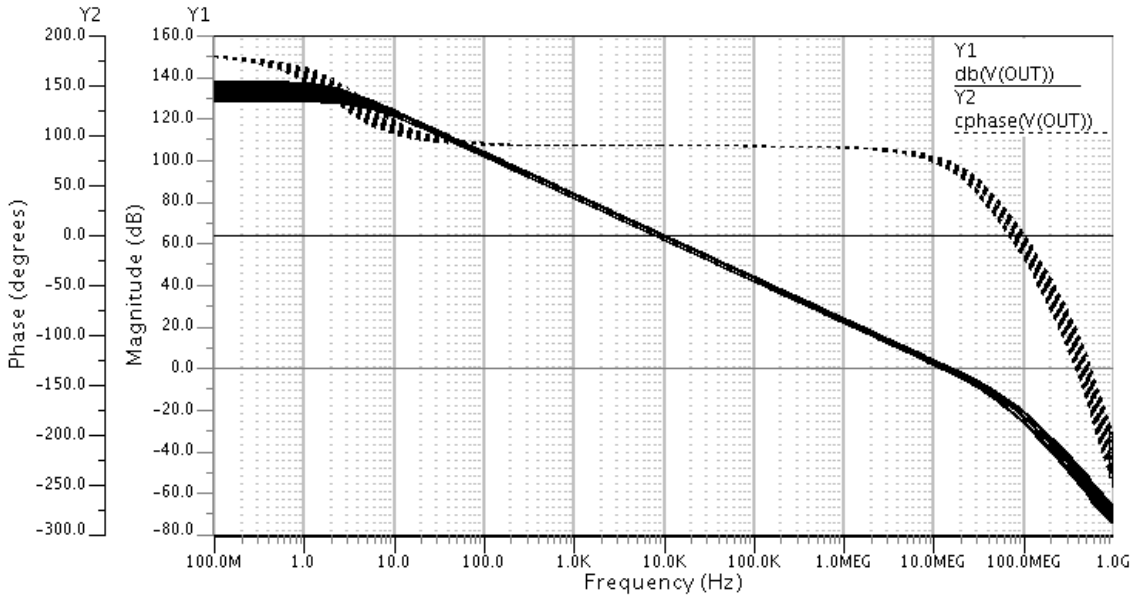
A.3 Full testbench schematic for AC analysis from Cadence with supply sources and biasing block

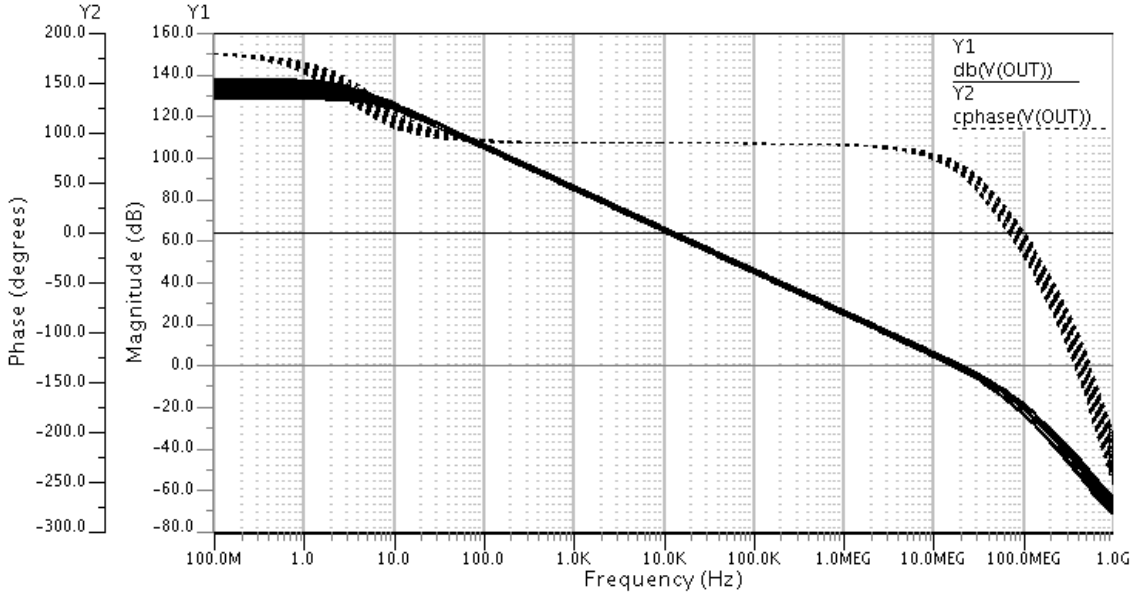


A.4 Control script code for corner simulation of AC characteristic

```
.extract rms(onoise, 100K, 1G)
.temp -40 27 125
.step param pVdd list 2.7 3.3 3.6

*.defwave gbp = FREQ*vm(out)
*.plot ac w(gbp) w(gbp2)

.extract ac label=PM yval(vp(out),extract(UGF))    ! vp(out) klesa 0 -
-> -180, pak preskoci na +180
.extract ac label=GM -yval(vdB(out),extract(invphase))
.extract ac label=UGF xthres(vdB(out),0dB)
.extract ac label=dcGAIN  max(vdB(out))
.extract ac label=invphase xthres(vp(out),0)

.extract label=min_GAIN min(dcGAIN)
.extract label=min_UGF min(UGF)
.extract label=min_PM min(PM)
.extract label=min_GM min(GM)

.extract label=max_GAIN max(dcGAIN)
.extract label=max_UGF max(UGF)
.extract label=max_PM max(PM)
.extract label=max_GM max(GM)

.alter
*path for lib_TT
.alter
*path for lib_FF
.alter
*path for lib_SF
.alter
*path for lib_FS
.alter
*path for lib_SS
```

A.5 Open loop AC characteristic over process, supply voltage, temperature for C_{TOT} capacitor 4pF (top) and 3 pF (bottom)





A.6 Results list for C_{TOT} capacitor *4 pF*

Run	Vdd	scenario	temp	dcGAIN	UGF	PM	GM
1	2.7	0	-40	135.45	15.632M	72.043	20.755
2	3.3	0	-40	137.11	16.154M	71.726	20.584
3	3.6	0	-40	137.61	16.408M	71.653	20.497
4	2.7	0	27	133.2	13.97M	71.32	20.603
5	3.3	0	27	134.72	14.419M	71.098	20.456
6	3.6	0	27	135.17	14.62M	71.118	20.379
7	2.7	0	125	130.09	12.131M	70.787	20.562
8	3.3	0	125	131.44	12.51M	70.806	20.428
9	3.6	0	125	131.77	12.675M	70.896	20.353
10	2.7	1	-40	135.45	15.632M	72.043	20.755
11	3.3	1	-40	137.11	16.154M	71.726	20.584
12	3.6	1	-40	137.61	16.408M	71.653	20.497
13	2.7	1	27	133.2	13.97M	71.32	20.603
14	3.3	1	27	134.72	14.419M	71.098	20.456
15	3.6	1	27	135.17	14.62M	71.118	20.379
16	2.7	1	125	130.09	12.131M	70.787	20.562
17	3.3	1	125	131.44	12.51M	70.806	20.428
18	3.6	1	125	131.77	12.675M	70.896	20.353
19	2.7	2	-40	135.01	15.851M	72.577	21.089
20	3.3	2	-40	136.5	16.432M	72.209	20.896
21	3.6	2	-40	136.94	16.693M	72.177	20.797
22	2.7	2	27	132.67	14.2M	71.818	20.945
23	3.3	2	27	134.05	14.682M	71.659	20.775
24	3.6	2	27	134.42	14.883M	71.722	20.685
25	2.7	2	125	128.53	12.361M	71.339	20.912
26	3.3	2	125	129.57	12.745M	71.459	20.755
27	3.6	2	125	129.72	12.914M	71.563	20.668
28	2.7	3	-40	134.6	15.553M	72.099	20.685
29	3.3	3	-40	136.19	16.082M	71.804	20.512
30	3.6	3	-40	136.64	16.342M	71.731	20.423
31	2.7	3	27	132.26	13.883M	71.387	20.53
32	3.3	3	27	133.72	14.333M	71.182	20.384
33	3.6	3	27	134.11	14.537M	71.204	20.305
34	2.7	3	125	129.04	12.031M	70.872	20.493
35	3.3	3	125	130.31	12.419M	70.882	20.354
36	3.6	3	125	130.58	12.578M	70.986	20.276
37	2.7	4	-40	136.08	15.71M	71.969	20.809
38	3.3	4	-40	137.82	16.231M	71.627	20.64
39	3.6	4	-40	138.34	16.48M	71.552	20.553
40	2.7	4	27	133.9	14.059M	71.231	20.656
41	3.3	4	27	135.51	14.508M	70.989	20.509
42	3.6	4	27	135.96	14.708M	71.006	20.432
43	2.7	4	125	130.86	12.239M	70.645	20.613
44	3.3	4	125	132.29	12.608M	70.693	20.479
45	3.6	4	125	132.57	12.78M	70.77	20.405
46	2.7	5	-40	135.8	15.416M	71.433	20.425
47	3.3	5	-40	137.65	15.891M	71.227	20.274
48	3.6	5	-40	138.21	16.134M	71.135	20.196
49	2.7	5	27	133.62	13.758M	70.756	20.264
50	3.3	5	27	135.32	14.162M	70.551	20.137
51	3.6	5	27	135.83	14.36M	70.533	20.471
52	2.7	5	125	130.74	11.908M	70.247	20.223
53	3.3	5	125	132.26	12.289M	70.148	20.107
54	3.6	5	125	132.69	12.449M	70.216	20.042

A.7 Results list for C_{TOT} capacitor *3 pF*

Run	Vdd	scenario	temp	dcGAIN	UGF	PM	GM
1	2.7	0	-40	135.45	20.539M	66.36	18.273
2	3.3	0	-40	137.11	21.239M	65.988	18.101
3	3.6	0	-40	137.61	21.563M	65.875	18.013
4	2.7	0	27	133.2	18.338M	65.481	18.121
5	3.3	0	27	134.72	18.927M	65.157	17.973
6	3.6	0	27	135.17	19.192M	65.112	17.895
7	2.7	0	125	130.09	15.863M	64.939	17.868
8	3.3	0	125	131.44	16.408M	64.693	17.943
9	3.6	0	125	131.77	16.645M	64.686	17.868
10	2.7	1	-40	135.45	20.539M	66.36	18.273
11	3.3	1	-40	137.11	21.239M	65.988	18.101
12	3.6	1	-40	137.61	21.563M	65.875	18.013
13	2.7	1	27	133.2	18.338M	65.481	18.121
14	3.3	1	27	134.72	18.927M	65.157	17.973
15	3.6	1	27	135.17	19.192M	65.112	17.895
16	2.7	1	125	130.09	15.863M	64.939	17.686
17	3.3	1	125	131.44	16.408M	64.693	17.943
18	3.6	1	125	131.77	16.645M	64.686	17.868
19	2.7	2	-40	135.01	20.88M	67.067	18.604
20	3.3	2	-40	136.5	21.607M	66.657	18.41
21	3.6	2	-40	136.94	21.942M	66.564	18.311
22	2.7	2	27	132.67	18.672M	66.158	18.46
23	3.3	2	27	134.05	19.281M	65.87	18.289
24	3.6	2	27	134.42	19.55M	65.861	18.198
25	2.7	2	125	128.53	16.201M	65.595	18.426
26	3.3	2	125	129.57	16.746M	65.46	18.268
27	3.6	2	125	129.72	16.98M	65.49	18.18
28	2.7	3	-40	134.6	20.444M	66.328	18.202
29	3.3	3	-40	136.19	21.169M	65.961	18.029
30	3.6	3	-40	136.65	21.502M	65.846	17.939
31	2.7	3	27	132.26	18.232M	65.454	18.048
32	3.3	3	27	133.72	18.838M	65.131	18.01
33	3.6	3	27	134.11	19.108M	65.087	17.869
34	2.7	3	125	129.04	15.751M	64.912	17.79
35	3.3	3	125	130.31	16.301M	64.668	18.328
36	3.6	3	125	130.58	16.541M	64.66	18.158
37	2.7	4	-40	136.08	20.633M	66.373	18.07
38	3.3	4	-40	137.82	21.314M	65.99	18.174
39	3.6	4	-40	138.35	21.63M	65.875	18.026
40	2.7	4	27	133.9	18.447M	65.481	17.949
41	3.3	4	27	135.51	19.02M	65.152	18.131
42	3.6	4	27	135.96	19.281M	65.105	17.995
43	2.7	4	125	130.86	15.993M	64.891	17.92
44	3.3	4	125	132.29	16.523M	64.672	17.945
45	3.6	4	125	132.57	16.757M	64.668	17.793
46	2.7	5	-40	135.8	20.195M	65.61	17.716
47	3.3	5	-40	137.65	20.882M	65.292	17.785
48	3.6	5	-40	138.21	21.195M	65.173	17.656
49	2.7	5	27	133.62	18.011M	64.76	17.588
50	3.3	5	27	135.32	18.58M	64.443	17.743
51	3.6	5	27	135.83	18.839M	64.373	17.626
52	2.7	5	125	130.74	15.564M	64.232	17.561
53	3.3	5	125	132.26	16.073M	63.946	17.626
54	3.6	5	125	132.69	16.31M	63.901	17.561

A.8 Control script code for noise simulation of proposed OTA

```
.param multiPo=3
.param multiP=1
.param nL=1
.param pWMb=27.45
.param pLMb=4
.param nWMb=8.5
.param nLMb=5
.param pWM=8.5
.param pLM=780m
.param nWM=6
.param nW=40
.param nLM=1.5
.param multiA=1
.param multi=3
.param Itail=14u
.param pVdd=3.3

.temp 27

.extract rms(onoise, 100K, 1G)

*.probe v
.option gramp=9 tuning=accurate aex be
.param Vdac_par = 1.65

.alter vstbop
.op
.tran 30n 30n
.probe v
.save ../ota1.iic time=25n


.alter vstb
.ac dec 100 10m 1g uic
.use ../ota1.iic ic
.lstb Vstb
.plot ac lstb_db
.plot ac lstb_p
.noise v(OUT) V4 1
.plot noise onoise
```