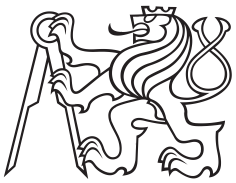
Master Thesis



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Design of low-dropout voltage regulator

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Field of study: Communications, Multimedia, Electronics
Subfield: Electronics
May 2016

Acknowledgements

I would like to sincerely thank to my supervisor doc. Ing. Jiří Jakovenko Ph.D an to my consultant Ing. Jiří Buryánec for their support and guidance throughout my work. I would also like to thank my family for supporting me throughout my studies.

Declaration

I declare that I have completed my diploma thesis on my own with the help of my supervisor and consultants. I only used materials listed in the bibliography.

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In Prague, . May 2016

Abstract

This thesis is focusing on design of low dropout voltage regulator (LDO) in general and on designing a specific LDO regulator to satisfy the given requirements. The preliminary chapters are dealing with the basic blocks such as error amplifier, pass transistor and with parameters of the LDO regulator such as line regulation load regulation etc. Basic design parameters of CMOS technology devices are presented after. Circuit is designed with emphasis on low quiescent current and dropout voltage, while stability is paramount. In last chapter, measurement results of parameters are presented and also corner analysis. The final LDO design achieves very low quiescent current in the range of microamperes.

Keywords: regulator, analog, stability

Supervisor: Doc. Ing., Jiří Jakovenko Ph.D.

Abstrakt

Tato práce je zaměřena na obecný návrh napěťového regulátoru s nízkým poklesem napětí (LDO) a na návrh konkrétního LDO regulátoru, který bude splňovat zadané parametry. Úvodní kapitoly se zabývají základními bloky jako je rozdílový zesilovač, regulující tranzistor a také se zabývají parametry LDO regulátoru, například regulací změny napájecího napětí a regulací změny zátěžového proudu apod. Poté jsou rozebrány základní návrhové parametry technologie CMOS. Obvod je navrhován s důrazem na co možná nejnižší klidový proud a minimalizaci potřebného vstupního napětí a zároveň musí být stabilní. V poslední kapitole jsou zhodnoceny naměřené výsledky parametrů a také analýza v rozích. Finální návrh LDO regulátoru dosahuje velmi nízkého klidového proudu v řádech mikroampér.

Klíčová slova: regulátor, analog, stabilita

Překlad názvu: Návrh napěťového regulátoru s nízkým rozdílem napětí

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Chapter 1

Introduction

With ever decreasing size of modern electronic devices, and not so much increasing battery efficiency, the electronic industry must push its limits in the power management systems. This leads to so called System on Chip architecture (SoC), where analog and digital digital are fabricated on the very same die. This lead to many different building blocks which may have different supply requirements and this is where a voltage regulator, DC-DC converter, switching regulator or their combination is utilized.

A power management unit may contain several power supply circuits as we can see in figure 1.1 which provide stable DC voltage under all load conditions and within a range of input voltage which is crucial for high frequency and high performance battery powered systems.

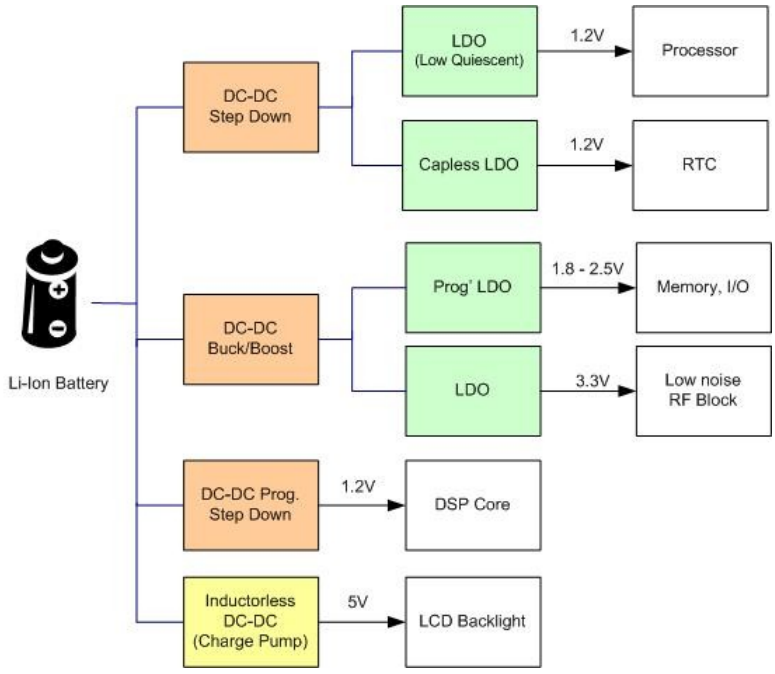

Figure 1.1: System on chip example, where LDOs are utilized [4]

1.1 Motivation

LDO regulator, being one of the fundamental building blocks of power management unit, is used in many portable battery powered systems, since constant and stable output voltage independent of the load impedance, input voltage variation, temperature and time is required as the battery discharges. This leads to to crucial stability improvement and noise reduction for subsequent circuits.

Since the technology trend is forcing designers to design circuits operating at lower supply voltages, the LDOs are ideal for providing multiple voltage levels and operate with a rather low dropout voltage. LDOs are also capable of minimizing current consumption down to microampers, which is crucial for current consumption of the sub-blocks in sleep mode.

Another important characteristic of linear voltage regulators is their ability to suppress supply voltage noise, thus shielding the noise-sensitive blocks, thus Power Supply Rejection Ratio (PSRR) is an important parameter of linear regulators. LDO voltage regulators are commonly used subsequently after switched regulators, which can efficiently regulate higher voltages, but their output is affected by ripple.

1.2 Objectives

This work is focused on designing an LDO voltage regulator in 180 nm process with GPDK180 process design kit. Specified output voltage is 1.5 V under all load conditions. Load current is in 10 uA to 1 mA range, with 10% error, so load current in range 9 uA to 1.1 mA must be expected. The regulator is stabilized via output capacitor, with 1 uF capacitance and 20% tolerance value. Equivalent series resistance also needs to be taken into account, since it it crucial in the design of many LDOs and allowed range of ESR must be specified. ESR range provided by specification is $10m\ \Omega$ to $300m\ \Omega$.

The input voltage varies from 1.7 V to 2 V and maximum quiescent current under all conditions should be lower than 10 uA. Temperature range is from $-50\ ^\circ C$ to $100\ ^\circ C$ which is in between industrial and military temperature grades. Another important parameter is PSRR, which determines how well the regulator rejects input voltage ripples and noise. PSRR is not specified, but we should aim for as large value as possible. And last but not least is the chip area, which determines how many dies can be placed upon one wafer, thus determining the cost of the chip.

In this paper, design of LDO voltage regulator and the trade-offs between his parameters will be presented.

Chapter 2

Linear Voltage Regulators

2.1 Voltage Regulators Fundamentals

A voltage regulator behaves as a constant voltage source by adjusting its internal resistance according to the changes of the load resistance.

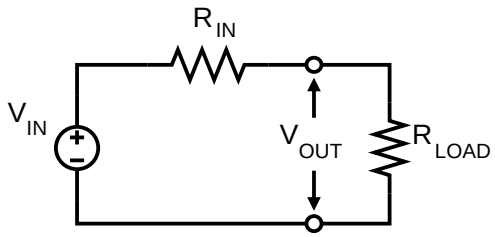

Figure 2.1: Constant-voltage source

The internal resistance of a constant voltage source 2.1 has to be significantly smaller than the external loading resistor so constant output voltage over a certain range of load changes is ensured.

The output voltage of this basic voltage source is calculated from a basic voltage divider:

$$V_{OUT} = V_{IN} \times \frac{R_{LOAD}}{R_{LOAD} + R_{IN}} = V_{IN} \times \frac{1}{1 + \frac{R_{IN}}{R_{LOAD}}} \quad [V] \tag{2.1}$$

If no load is present ($R_{LOAD} = \infty$), the maximum possible output voltage is equal to the voltage at the regulator input. Increasing the load causes output voltage to drop from its maximum value and introduces an output-voltage error E_{VO}. The definition of this error is percentage difference between V_{OUT} under no-load condition ($V_{OUT-MAX}$), and V_{OUT} under load ($V_{OUT-LOAD}$).

$$E_{VO} = \frac{V_{OUT-MAX} - V_{OUT-LOAD}}{V_{OUT-MAX}} \times 100 \quad [\%] \tag{2.2}$$

V_{IN} can be replaced with V_{OUT} and $V_{OUT-LOAD}$ can be substituted by the value from equation 2.1, this way we get the voltage error expressed through the resistor ratio of R_{IN} to R_{LOAD} as follows:

$$E_{VO} = \frac{R_{IN}}{R_{IN} + R_{LOAD}} \times 100 \quad [\%] \tag{2.3}$$

As we can see in following plot, the voltage error E_{VO} is increasing with decreasing load resistance R_{LOAD}

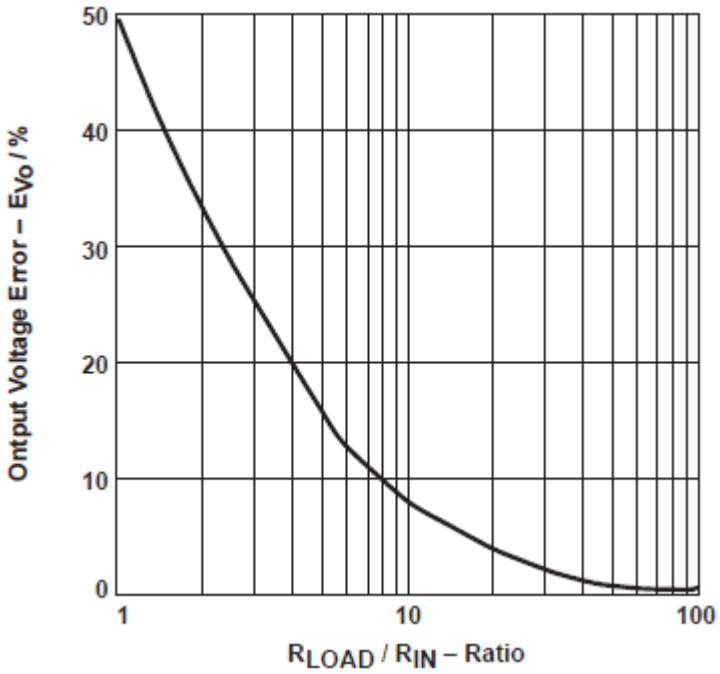

Figure 2.2: Output-Voltage Error vs Load Resistance [9]

For this error to be minimized we need to introduce some kind of feedback circuit, that senses any occurring load changes and adjust a variable internal resistor of the source to keep a constant ratio of internal-resistance to load-resistance: $R_{IN}/R_{LOAD} = k$.

$$R_{IN} = R_{LOAD} \times k \quad [\Omega] \tag{2.4}$$

Based on this assumption we can see that R_{IN} is following R_{LOAD} in a linear fashion:

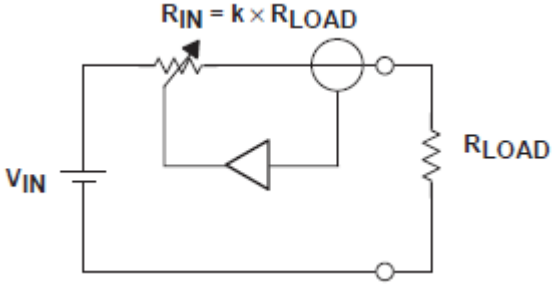

Figure 2.3: Linear relation between R_{IN} and R_{LOAD}

We can differentiate between two basic topologies of linear regulators, basic voltage regulators and low dropout voltage regulators. The basic types of voltage regulators were used prior to the LDO type, because they are more stable and does not need an output capacitor to ensure their stability. On the other hand they require rather large input voltage to be properly biased, or we can say they have high dropout voltage.

Older linear voltage regulators mainly used NPN or PNP bipolar junction transistor as a pass element, but with higher demand for lower supply voltages and lower quiescent current, they have been replaced by MOSFETs. Main disadvantage of BJT transistors is that their base current is proportional to the load current

$$Iq = \frac{I_load}{\beta} \quad [A] \tag{2.5}$$

This current can be reduced by cascading BJT transistors at the expense of increased dropout voltage.

Compared to base current of BJT transistor, the gate current of MOSFET is negligible and is not dependent on the load current, because the transistor is controlled by voltage. With CMOS technology being the most

2.2 Low Dropout Voltage Regulator

As the name suggest, LDOs are linear regulators which require much less voltage difference between its input and output to properly regulate the input voltage. In figure 2.4 we can see a classic topology of an LDO regulator. It consist of pass element, an error amplifier and a resistor feedback network. The feedback network comprises of resistive voltage divider, which delivers scaled output voltage which is equal to the reference voltage when the output is at its nominal voltage. The error amplifier is constantly comparing the reference voltage and the voltage being feed from the voltage divider. This difference is amplified and the output of the error amplifier drives the pass element to keep the output voltage level at desired value.

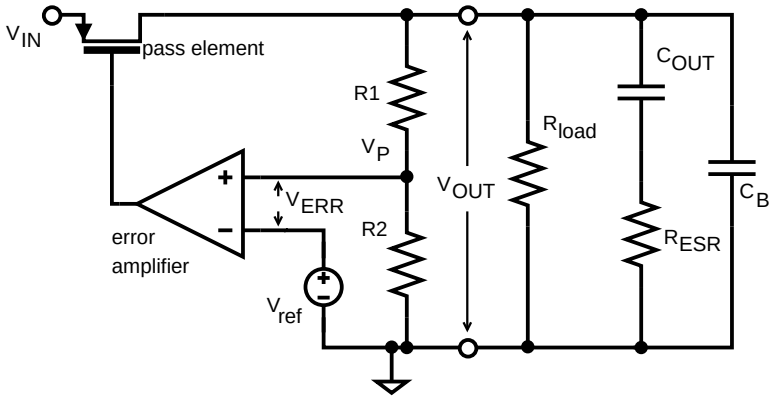

Figure 2.4: Basic linear voltage regulator

In the figure 2.4 we can identify following building blocks:

2.2.1 The Voltage Reference

Voltage reference sets the operating point of the error amplifier, thus it is the starting point of all regulators. In most cases this voltage reference is of the band-gap type, because it provides ability to work at low supply voltages, and its accuracy and its stability under varying temperature is sufficient for design of linear regulators. Important parameters of the voltage reference is its output noise and contribution to the overall PSRR of the error amplifier, these effect can be minimized by adding passive component filters, like RC filters.

2.2.2 The Error Amplifier

Error amplifier design must be kept as simple as possible, so it does not draw too much of current. The less current branches it has, the less current it draws from the input and thus the overall quiescent current is lower. Also as we try to make the quiescent current as low as possible, there is a trade-off between biasing current and performance of the error amplifier (bandwidth, slew rate etc.). Since the gate capacitance of the pass element will be quite large, the output resistance of the error amplifier should be as low as possible to ensure stability of the system. The DC open loop gain should be high under all load conditions to ensure accuracy of the output. Bandwidth of the amplifier should be large enough to react fast upon changes of the load conditions and input voltages. Output voltage swing of the amplifier is also important, because at low load currents, the pass device needs to be turned off, which leads to the error amplifier output being driven close to one of the supply rails depending on the pass device type.

Error amplifier takes the voltage scaled down by the voltage divider composed of resistors R_1 and R_2 $V_P = V_{OUT}R_1/(R_1 + R_2)$, compares it with the reference voltage and adjusts the resistance of the pass element to drive the error signal ($V_{ERR} = V_P - V_{REF}$) as close to zero as possible. If we set $V_{REF} = V_P$ the we get V_{OUT} as:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times V_{REF} \quad [V] \tag{2.6}$$

This applies only if input voltage V_{IN} is high enough to keep the error amplifier and the pass transistor from falling into triode region, this sets the value of dropout voltage, which will be discussed later.

2.2.3 The Feedback Network

Resistive feedback network scales the output voltage V_{OUT} for the comparison against the reference voltage V_{REF} by the error amplifier. Due to the fixed V_{REF} the only way to change the output voltage is through ratio of R_2/R_1. The current flowing through the divider contributes to the quiescent current of the voltage regulator, so for low consumption it is necessary to properly scale the value of the resistors so it correlates with the load current and

with the current consumption of the error amplifier. For example, if the consumption of the error amplifier is 50 uA, resistances in hundreds of $k\Omega$ lead to current in μA. But if the consumption of the error amplifier is in μA and the overall quiescent current of the LDO needs to be as low as possible, the resistance have to be in $M\Omega$ to reduce the quiescent current. This leads to a trade-off between area consumption and parasitic capacitance of the resistors, which may have impact on the stability of the system and quiescent current of the LDO voltage regulator.

An alternative topology to the resistive network is one comprising of MOS transistors in figure 2.5.

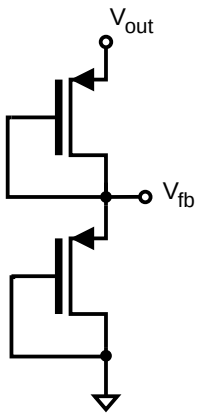

Figure 2.5: Mosfet divider

This design can reduce the area of the divider, but the channel length of the transistors has to be large to produce large output resistances. As a result, parasitic capacitance of transistors increases and can impose a slew rate reduction which affect the ability of the error amplifier to react on output voltage variations. If the area is not a constraint, the resistive divider is a better option, since it can provide less current consumption and less capacitance.

2.2.4 The Series-pass Element

Pass element is transferring large currents from input to the load and is driven by the error amplifier in a feedback loop. There are various topologies of pass elements but since this works is focusing on design of an LDO in a CMOS technology, only MOSFET pass elements will be described.

PMOS pass element voltage V_{GS} is tied to the V_{dd} supply rail of the regulator, thus the minimum required voltage is given by minimum drain source voltage V_{ds}, required for the pass transistor to stay in saturation region and regulate properly. PMOS dropout voltage is defined by equation 2.7

$$V_{dropout,PMOS} = V_{out} + V_{dsat,PASS} \quad [V] \tag{2.7}$$

If the input voltage falls bellow dropout voltage, the pass transistor operates in the linear region, the open-loop gain of the system deteriorates and regulator

accuracy decreases. Ultimately PMOS pass element gate voltage is moving towards ground as the load current increases, so for large output currents, the pass device has to be very large or the input voltage of the LDO has to be increased, because the gate of the pass transistor cant be pulled lower than the ground level. So the PMOS is not suitable for very low voltage applications.

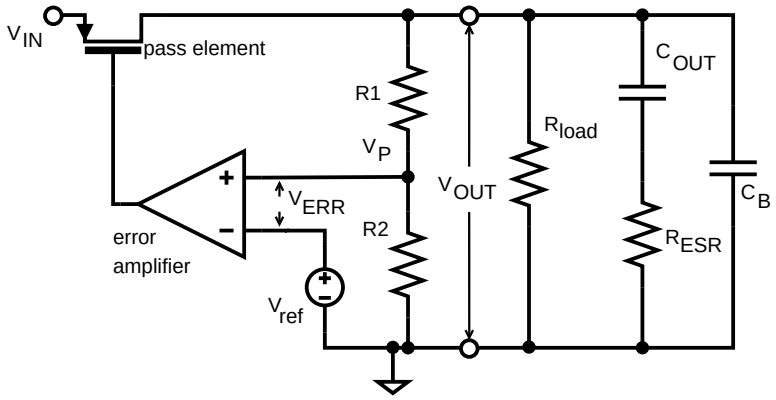

Figure 2.6: LDO with PMOS pass element [17]

NMOS pass element has advantage of source follower configuration, so the output node is at the source of the transistor, which translates lower output resistance, which may improve stability, but that depends on the size of the output capacitor. On the other hand, the minimum required voltage of NMOS transistor is given by equation 2.8, because voltage V_{GS} of the pass transistor is tied to the output voltage and needs to be always higher than the output voltage.

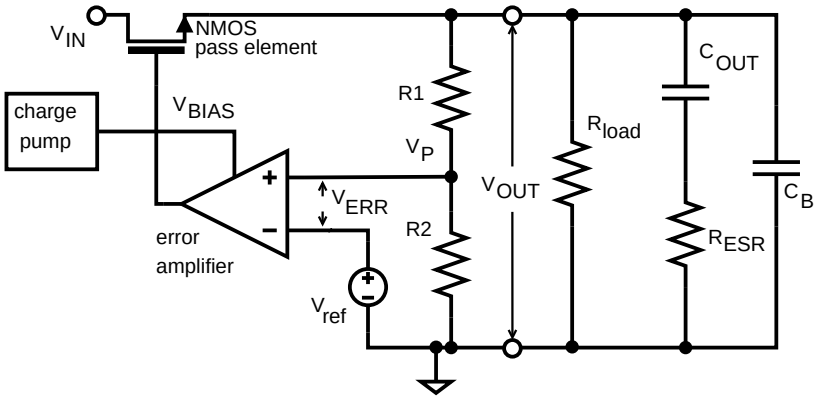

Figure 2.7: LDO with NMOS pass element [17]

$$V_{dropout,NMOS} = V_{out} + V_{GS,PASS} \quad [V] \tag{2.8}$$

Sometimes, to exploit the advantages of the NMOS pass device a charge pump is used, to pull the gate voltage of the transistor higher. The circuit is

larger and more complex, but very low input, output and dropout voltage can be achieved this way.

2.2.5 Output Capacitor

The output capacitor ensures, that during load transients, the current is delivered immediately to the load until the error amplifier catches up. It also plays essential role in the stability of the system, because it form an low frequency pole and also a zero, at higher frequencies.

The zero correlates with the Equivalent Series Resistance (ESR) of the capacitor, which is modeled as a resistance in a series with a capacitor. Specified ESR range of used 1 uF capacitor is from 10 $m\Omega$ to 300 $m\Omega$. This restricts us to use only capacitors with ESR in this range.

Capacitor types with ESR values in this range are:

- polymer electrolytic capacitor
- low-ESR tantalum capacitor
- ceramic capacitor

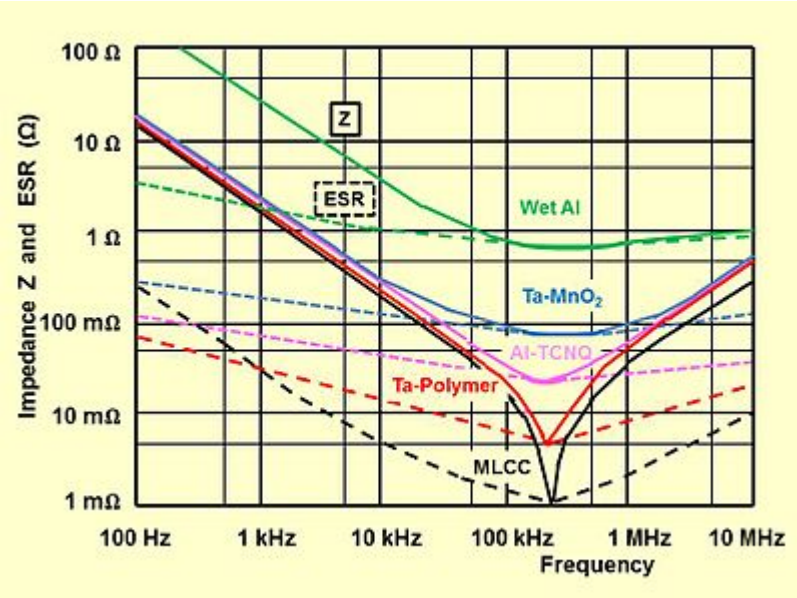

Figure 2.8: Comparison of various capacitors ESR [18]

Lower ESR translates into minimal overshoots during load transients, since ESR value restricts the current flow from the capacitor to the load. ON the other hand, higher ESR may provide better stability.

2.3 LDO Parameters

In this section, basic steady state and transient parameters of LDO regulators will be presented.

2.3.1 Dropout Voltage

Dropout voltage represents the differential voltage between input and output node of the voltage regulator at which the circuit ceases to regulate against further decrease of the input voltage. This occurs as the input voltage approaches the output voltage from above. For the regulator to remain sensitive to changes in output voltages, transistors are usually designed to stay in their high gain mode (saturation) and input voltage V_{IN} defines how much headroom the transistors have. Lowering V_{IN} lowers the dynamic voltage range of the transistors with which the transistor operate in the feedback loop to control the output voltage. Thus if one or more transistors start falling out of their saturation into triode, gain of the system deteriorates and the output voltage V_{OUT} starts to deviate from specified output voltage $V_{O'}$

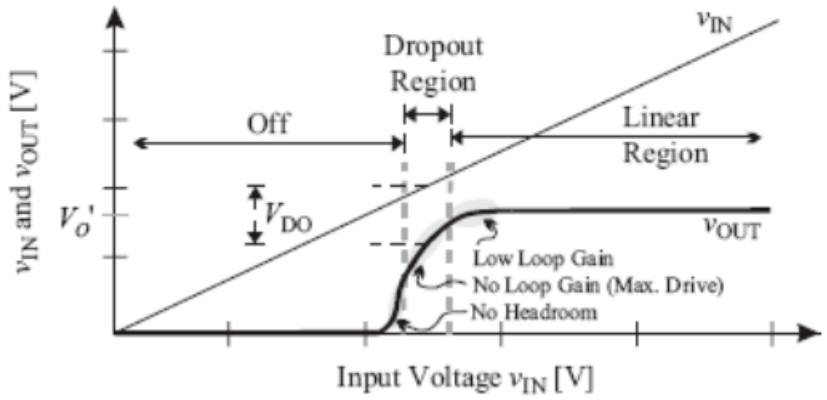

Figure 2.9: Input-output behavior of linear regulator [11]

In the dropout region, the loop gain is so low, that the pass device starts to behave like a switch, because of the absence of the control its conductivity, thus the output voltage V_{OUT} will be difference between input voltage and pass device ohmic drop.

$$V_{OUT,drop} = V_{IN} - V_{PASS} = V_{IN} - I_{LOAD}R_{PASS} = V_{IN} - V_{DO} \quad [V] \quad (2.9)$$

2.3.2 Quiescent Current

Quiescent, or ground current is the difference between input and output currents. Low quiescent current is needed to maximize efficiency, especially in low power systems.

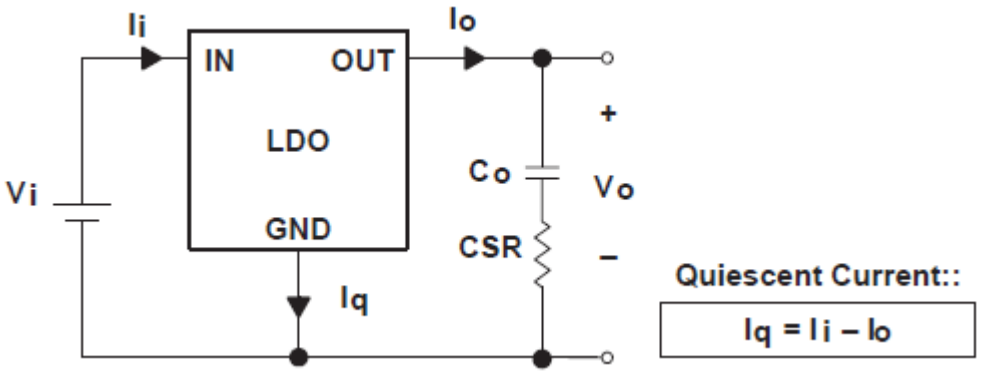

Figure 2.10: Quiescent current of an LDO regulator [11]

All internal blocks (bad-gap reference, sensing resistors and error amplifier and other blocks) have their share in increase of the quiescent current due to their bias currents. Series pass element gate drive current also contributes to the quiescent current increase.

2.3.3 Efficiency

LDO regulator efficiency is limited by the quiescent current and input to output voltages as stated in following equation.

$$Efficiency = \frac{I_o V_o}{(I_o + I_q)V_i} \times 100 \quad [\%] \tag{2.10}$$

High efficiency can be achieved by minimizing the dropout voltage and quiescent current. The voltage difference between the input and the output should be minimal, to keep power dissipation as low a possible ($PowerDissipation = (V_i - V_o)I_o$). The input to output voltage difference is the defining factor determining power efficiency, regardless of the load conditions.

2.3.4 Transient Response

Transient response is defined as maximum output voltage variation for a load current step or a input voltage step. It is a function of output capacitor and its equivalent series resistance (ESR) and if needed, the bypass capacitor can be added to furthermore improve the transient response. The equation of the maximum voltage variation at the output is defined as follows:

$$\Delta V_{tr,max} = \frac{I_{o,max}}{C_o + C_b}\Delta t_1 + \Delta V_{ESR} \quad [V] \tag{2.11}$$

Where Δt_1 is defined by the closed loop bandwidth of an LDO regulator. ΔV_{ESR} is the voltage variation resulting from the presence of the ESR (R_{ESR}) of the output capacitor. The value of maximum output voltage transient is determined by the application.

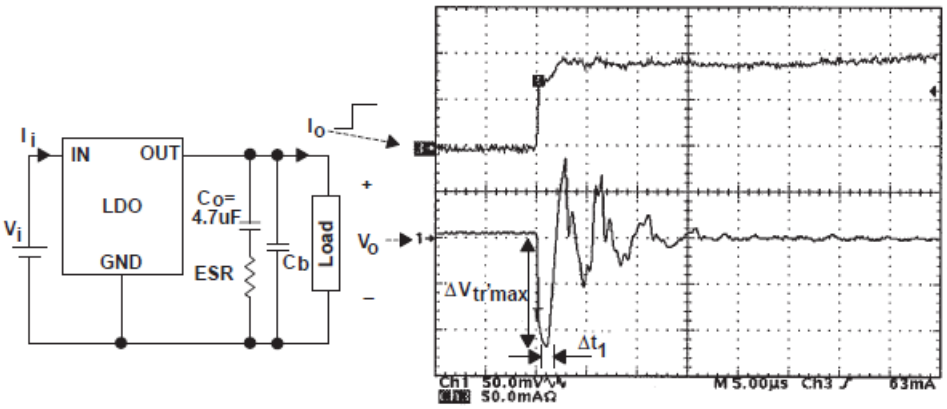

Figure 2.11: Load transient response of an LDO regulator [11]

In figure 2.11 we can observe the transient of a 1.2 V, 100 mA LDO regulator with output capacitor od 4.7 uF when a step change of load current was applied.

2.3.5 Line Regulation

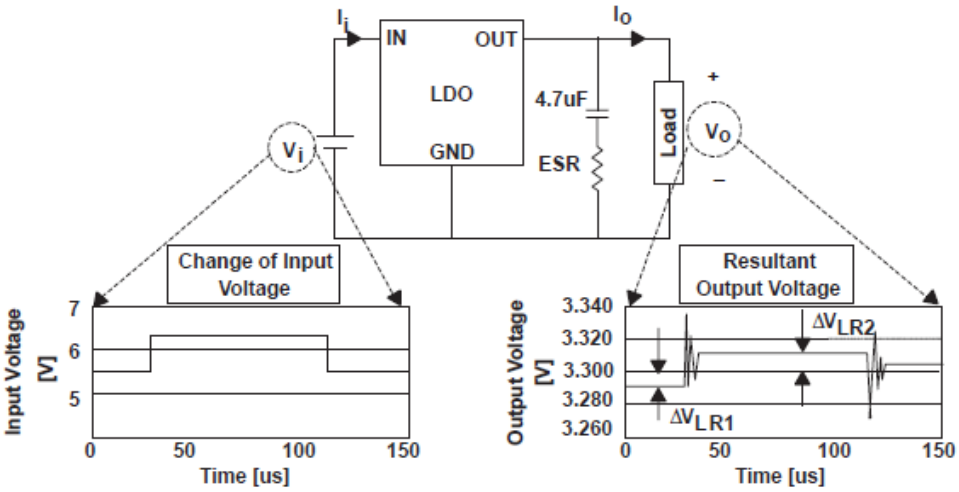

Figure 2.12: Line transient response of TPS76933 [11]

Line regulation is a parameter defining the ability of the regulator to maintain the desired output voltage with varying input voltage. It is defined as:

$$Line\ regulation = \frac{\Delta V_o}{\Delta V_i} \quad [V/V] \tag{2.12}$$

Where A_{PASS} is the gain of the pass device, β is the feedback factor and A_{EA} is the gain if the error amplifier. The line regulation improves with open loop gain, but increasing gain too much can hinder stability, so that

must be taken into consideration. The line regulation is proportional to the open loop gain, but basically its is a power supply ripple rejection at DC frequencies. Figure 2.12 shows how the TPS76933 LDO regulator responds to the line transient step. With increasing input voltage, the output voltage variation also increases. Since line regulation is a steady state parameter (is is measured after transient), it can be measure as variance of output voltage upon changing of the input voltage, which is shown in figure 2.13

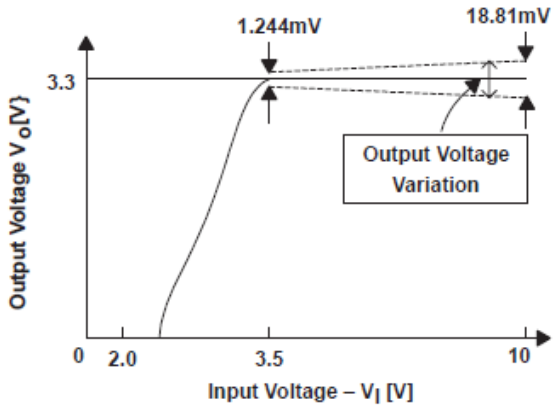

Figure 2.13: Line regulation of TPS76933 [11]

2.3.6 Load Regulation

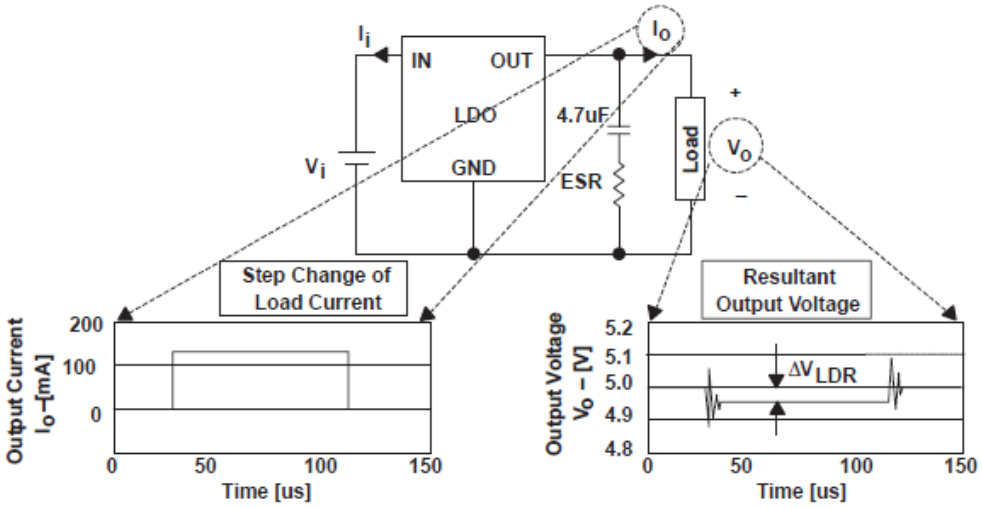

Figure 2.14: Load transient response of TPS76933 [11]

If the load current increases, the load capacitor supplies the current to the load, this changes the output voltage which is the sensed by the resistive divider a fed back to the amplifier who compensates the change in the the output voltage by allowing more current to flow through the pass transistor.

Load regulation is a parameter defining the ability of the regulator to maintain the desired output voltage with varying load current. It is defined as:

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} = \frac{r_{oPASS}}{1 + \beta A_{PASS} A_{EA}} \quad [V/A] \tag{2.13}$$

Where r_{oPASS} is the is the output resistance of the pass device. Increasing open loop gain improves load regulation as in the case of line regulation.

Load regulation can also be viewed as output voltage varying with the load current as seen in fig 2.15

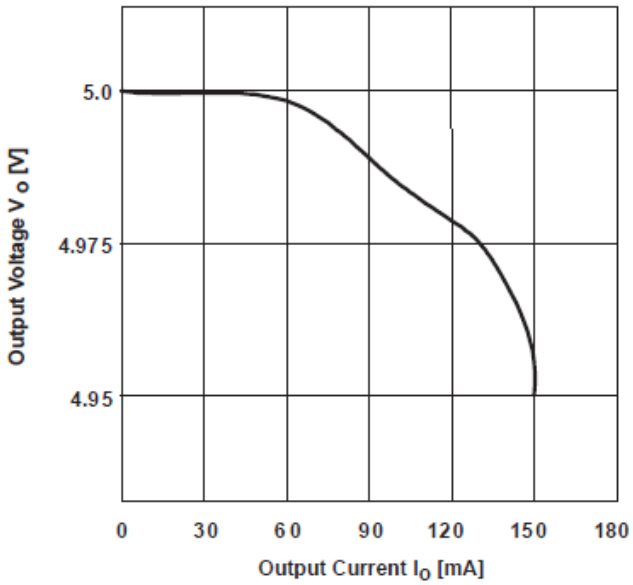

Figure 2.15: Load regulation of TPS76933 [11]

2.3.7 Power Supply Rejection

Power supply rejection ratio (PSRR), also known as ripple rejection is regulator's ability to prevent fluctuation of regulated output voltage caused by input voltage variation. PSRR equation is the same as for line regulation, but the whole frequency spectrum is taken into consideration.

PSRR is dominantly defined by the control loop. Low ESR value of output capacitor and its high capacitance improves power supply rejection ratio.

$$PSRR(\omega) = 20 \cdot log_{10} \frac{A(\omega)}{A_{supply}(\omega)} \quad [dB] \tag{2.14}$$

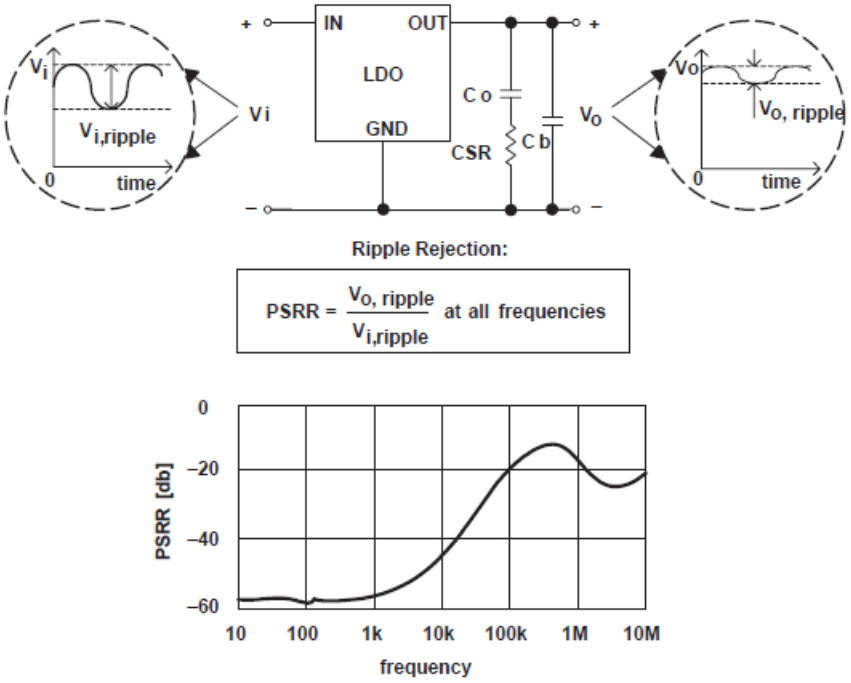

Figure 2.16: Power supply rejection ratio [11]

Chapter 3

CMOS Process Specification

To properly design circuits in CMOS technology the designer has to be aware of the relationships between various parameters of the MOS transistors and its electrical characteristics. In this chapter various simulations of used mosfet transistors will be presented together with basic theory of operation. Characteristics were obtained using Spectre circuit simulator in Cadence simulation environment. nmos1 and pmos1 transistors models were used, which are based on bsim3v3 model.

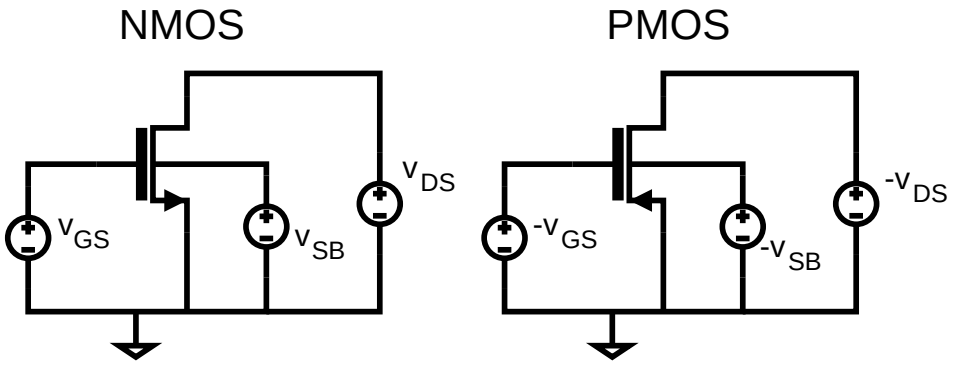

Figure 3.1: NMOS and PMOS testbench

3.1 MOSFET Regions of Operation

A MOSFET has three regions of operation depending on the value of V_{GS}, subthreshold, strong inversion and velocity saturation. In each of these regions, the transistor can operate in linear or saturation region. On figure 3.2 we can see how are the regions separated in terms of current flowing through the transistor and change of V_{GS}. Figure 3.3 is plotted with logarithmic scale on y-axis, so the regions are visually more clearly separated.

The MOSFET has additional two regions of operation which are related to the drain source voltage V_{DS}. The transistor is either in linear (triode) region where

$$V_{DS} < V_{DS,sat} = V_{OV} = V_{GS} - V_{TH} \quad [V] \tag{3.1}$$

or in the saturation region

$$V_{DS} > V_{DS,sat} = V_{OV} = V_{GS} - V_{TH} \quad [V] \tag{3.2}$$

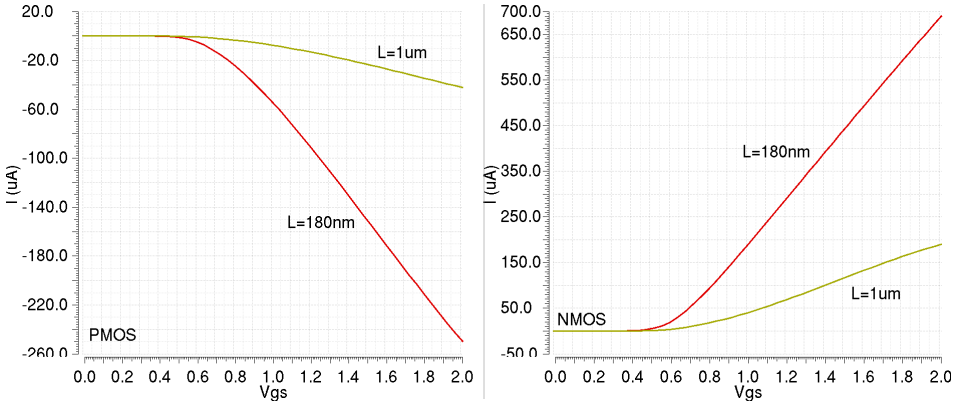

Figure 3.2: Ids vs Vgs of NMOS and PMOS for W=1um and L=180nm; L=1um, Vds=1V

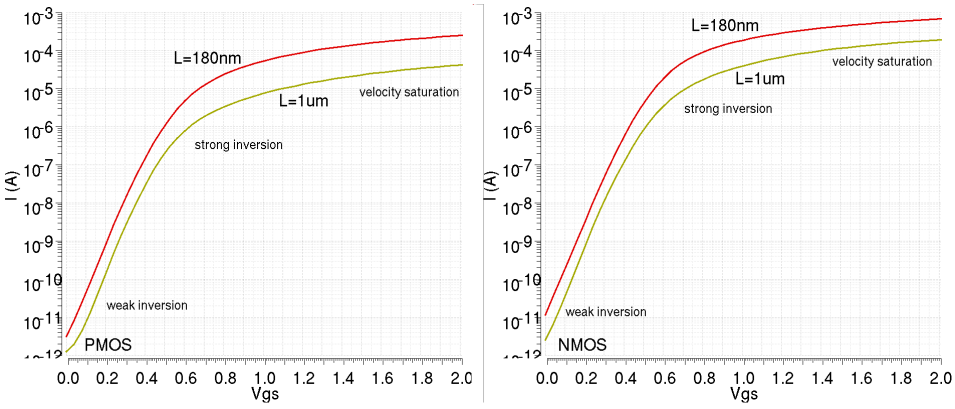

Figure 3.3: Ids vs Vgs of NMOS and PMOS for W=1um and L=180nm; L=1um, Vds=1V in logarithmic scale

3.1.1 Strong Inversion

The most used region is the strong inversion region, in which moderate current is flowing through the transistor at the set V_{GS}. In this region, the transistor is modeled by the most fundamental CMOS analog design equation, also known as the square-law equation,

$$I_D = \frac{1}{2}\mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad [A] \tag{3.3}$$

where μ is the mobility of the charge carriers in the channel, C_{ox} is the gate-oxide capacitance, W is the width of the channel and L is the length of the channel. Equation 3.3 is applicable if the transistor is in saturation

($V_{DS} \geq V_{GS} - V_{TH}$), otherwise, the transistor is in linear (triode) region, where equation drain current is defined as

$$I_D = \mu C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad [A] \tag{3.4}$$

If the drain to source voltage V_DS is very small, the current I_{DS} is almost linearly dependent on voltage V_{DS}, so the transistor behaves as a resistor. Equation 3.5 can be simplified by neglecting the term V_{DS}^2, thus we get

$$R_{on} = \frac{1}{\mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})} \quad [\Omega] \tag{3.5}$$

3.1.2 Weak Inversion

AT lower current, MOSFET operates in weak inversion, which translates into very small channel conductivity. The channel is practically not yet formed and the drift current, which flows through the channel in strong inversion is replaced with a diffusion current. The model is very different from square-law model, as the current in relation to gate source voltage express exponential behavior.

$$I_{DS,weak} = I_{D_0} \frac{W}{L} \exp\left(\frac{V_{GS}}{\frac{nkT}{q}} \right) \quad [A] \tag{3.6}$$

k is the Boltzmann factor, q is the charge charge of an electron thus expression kT/q is about 26 mV at room temperature. The parameter n is derived from the sub-threshold swing and it depends on the bias conditions, and is usually between 1.2 and 1.5. This behavior is very close to the bipolar transistor operations, but the difference is in the scaling factor n. The border between weak and strong inversion can be derived from transconductances and current in both regions and is about 70 mV (strong inversion start at about $V_{TH} + 70\ mV$), this region is sometimes called moderate inversion.

Weak inversion in general is characterized by high ratio of g_m/I_{DS}, it is thus most efficient in terms of power consumption, but the absolute values of both current and transconductance are very low, so the noise becomes a large problem and only low speed circuits are achievable.

3.1.3 Velocity Saturation

At high drain to source currents, the I_{DS} starts to change linearly with V_{GS}, this is mainly because of velocity saturation. Because of high electric fields in the channel, all charge carriers move at maximum speed v_{sat}.

$$I_{DS_{vsat}} = W C_{ox} V_{sat} (V_{GS} - V_{TH}) \quad [A] \tag{3.7}$$

As a designer, we want to stay away from this region as far as possible, because in velocity saturation, with increasing current, the transconductance does not increase, but the current consumption does.

3.2 Transconductance g_m

Transconductance g_m is extremely important parameter in analog design as it defines the ratio of voltage v_{gs} and i_d. It is important to note that transconductance is a small signal parameter. Its value is evaluated as a slope at DC operating values of V_{GS} and I_{DS}. Transconductance is given as a derivation of I_{DS} in all three regions.

For strong inversion, the transconductance is given by equation

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2 I_{DS} \mu C_{ox} \frac{W}{L}} = \frac{2 I_{DS}}{V_{GS} - V_{TH}} \quad [S] \tag{3.8}$$

It is key in determining the gain of amplifiers and it is an overall performance characteristic of a transistor. According to the three equations above, it may not be certain if transconductance is proportional to square root of the drain source current or directly to the current. When W/L ratio is constant the g_m is proportional to the square root, when the $V_{GS} - V_{TH}$ is fixed, the g_m is proportional to the current itself.

The main reason why we avoid the velocity saturation is that the transconductance become almost constant, it is also derived from the current equation by derivation

$$g_m \approx W C_{ox} v_{sat} \quad [S] \tag{3.9}$$

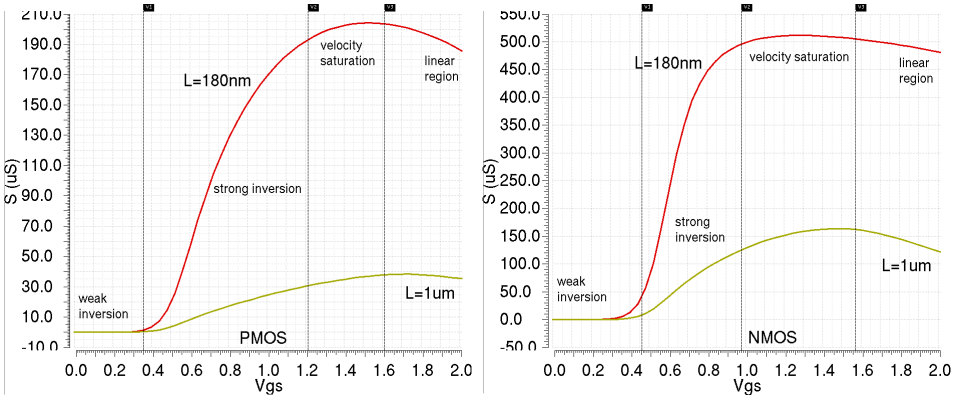

Figure 3.4: gm vs Vgs of NMOS and PMOS for W=1um and L=180nm; W=1um Vds=1V

In the figure 3.4 we can also see the three different regions of operation. As the V_{GS} increases we can see that in velocity saturation, the g_m curve is flattening and then start to fall. As the V_{GS} increases, the overdrive voltage $V_{GS} - V_{TH}$ also increases, thus the transistor requires larger $V_{DS,sat}$ to remain in saturation. The fall is nothing else than transition from saturation to linear region, where transconductance is very low. Another important observation is that transconductance is about three times lower for PMOS transistor, than for NMOS transistor, that is caused by different mobility of holes and electrons.

3.3 g_m/I_{DS} vs V_{GS}

Another way to define in which state the most transistor is g_m/I_D. This metric is used especially in modern analog design, because it combines the previous relations to provide a more convenient way of designing transistor. Especialy in bsim 3v3 model, the design with the overdrive voltage is not precise, because at lower overdrive voltages, the model does not evaluate them correctly.

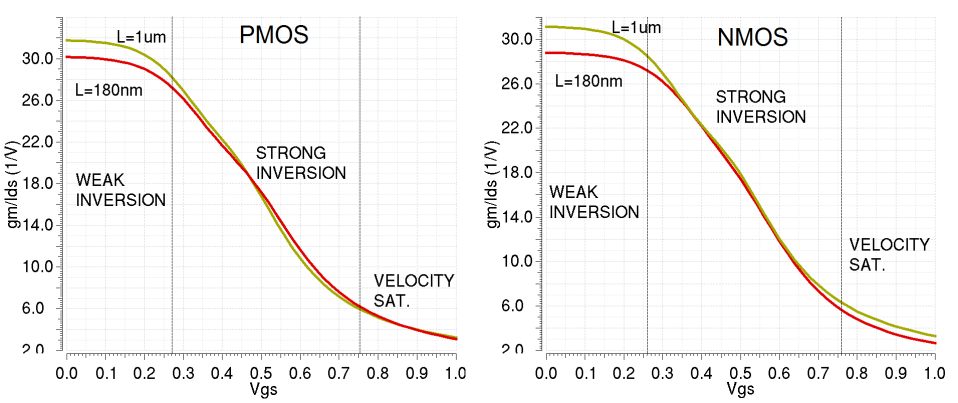

Figure 3.5: gm/Id vs Vgs of NMOS and PMOS for W=1um and L=1um; L=180nm, Vds=1V

3.4 I_{DS} V_{DS} Relation

As said earlier depending on the value of the overdrive voltage $V_{GS} - V_{TH}$ and voltage V_{DS} the transistor can operate either in linear or saturation region. As we can see in the following figures, the current rises almost linearly (linear region) at low values of V_{DS}, then moves into nonlinear region, which is the border between linear and saturation region and in saturation it should stay constant. As we can see that is not the case, because of the effect called channel length modulation.

3.4.1 Channel Length Modulation

Channel length modulation effect is caused by increasing width of the depletion region at the drain-channel PN junction. When $V_{DS} = V_{GS} - V_{TH}$, the inversion layer at the junction ceases to exist and further increase in V_{DS} decreases effective length of the channel. Because of the phenomena a small increase in I_{DS} can be observed.

Channel length modulation is modeled by λ parameter in square law equation 3.3 and is directly proportional to the absolute length of the channel. As we can see in 3.10 increasing channel length reduces the effect of channel

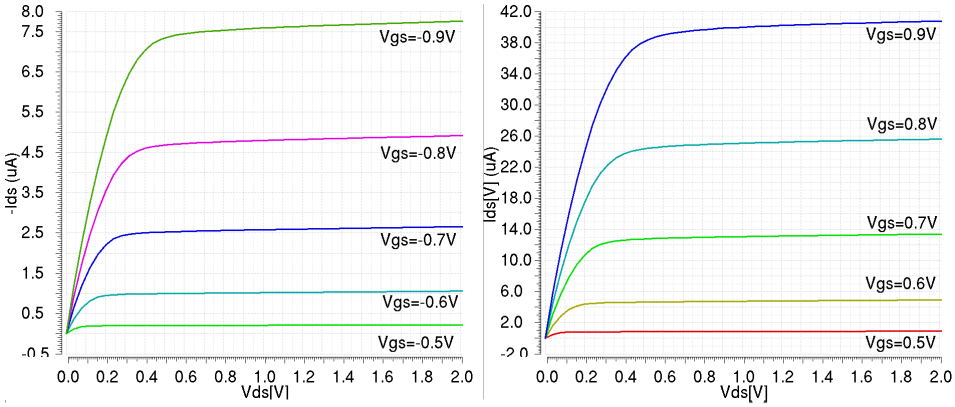

Figure 3.6: Ids vs Vds of NMOS and PMOS for W=1um and L=1um

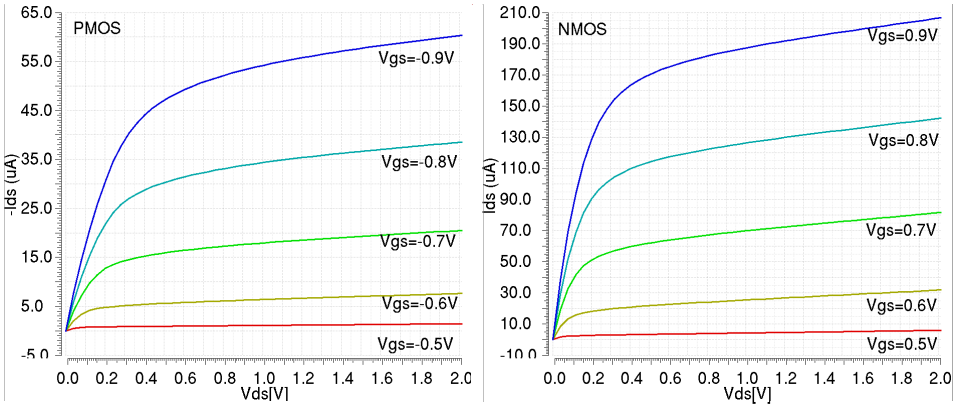

Figure 3.7: Ids vs Vds of NMOS and PMOS for W=1um and L=180nm

length modulation.

$$\lambda = \frac{1}{V_E L} \quad [1/V] \tag{3.10}$$

V_E is Early voltage and can be found as an intersection of all current slopes in classic I_{DS} vs V_{DS} with varying V_{GS}. There it is an constant and from it, output resistance can be derived.

$$r_{ds} = \frac{V_E L}{I_{DS}} = \frac{1}{\lambda I_{DS}} \quad [\Omega] \tag{3.11}$$

This equation is very handy because output resistance is used as a small signal parameter in gain calculation and defines locations of poles and zeros in stability analysis. Thus the designer must choose proper length of the device and proper biasing current to achieve his goal. If we want to increase resistance by increasing length, the width must be also larger to maintain the same biasing point as before. This can have negative effect in increase of the parasitic capacitance of the device, one of many things to be considered during the design. On figures 3.8 and 3.9 we can see how devices behave when with swept L and I_{DS}.

The sudden transitions we can see in the figure 3.8 are caused by the GPDK0180 model. The model file is separated into sections with different

parameters for different length of the transistor, so the transitions occur due to the model file parameter change.

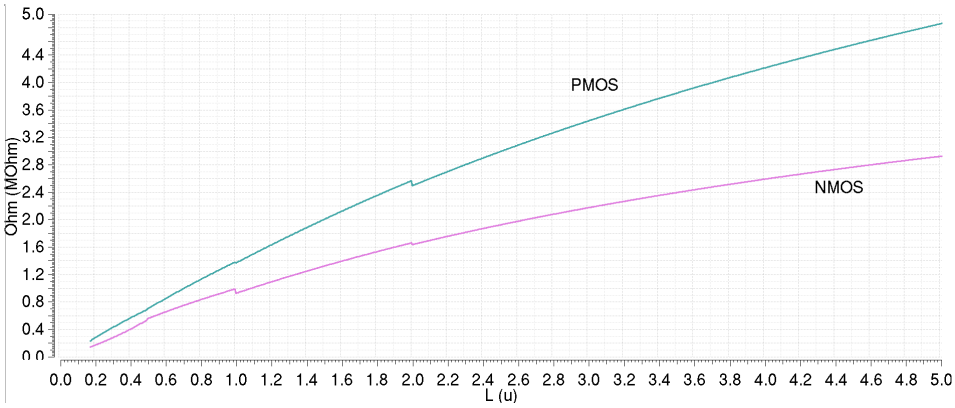

Figure 3.8: rds vs L of NMOS and PMOS for W/L=5 Ids = 20uA

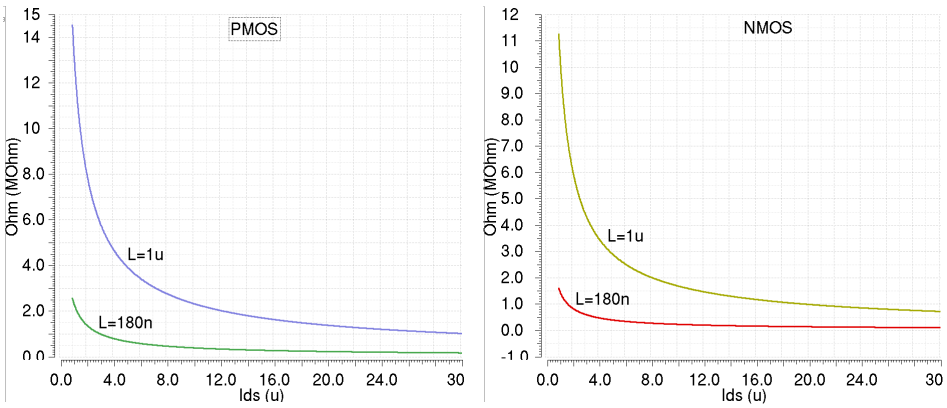

Figure 3.9: rds vs Ids of NMOS and PMOS for W/L=5 and L=180nm, L=1um

3.5 Threshold Voltage

Threshold voltage in an important parameter for design. It defines current I_{DS} and overdrive voltage as well, so it is important to know, how it changes with other parameters of a MOSFET device.

3.5.1 Body Effect

Body effect shows the effect of source to bulk voltage V_{SB} on threshold voltage. Increasing V_{SB} will increase the depletion layer width under the channel and thus V_{TH} increases too and I_{DS} decreases.

$$V_{TH} = V_{T0} + \gamma \left[\sqrt{|2\Phi| + V_{SB}} - \sqrt{|2\Phi|} \right] \quad [V] \tag{3.12}$$

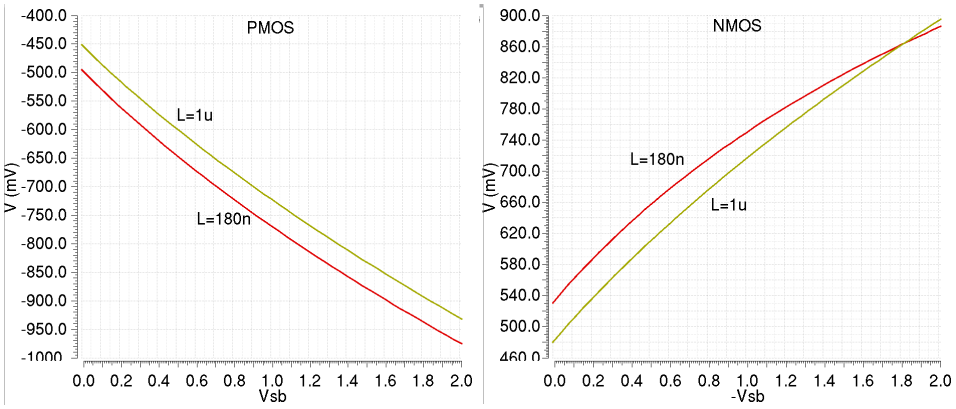

Figure 3.10: Vth vs Vsb of NMOS and PMOS for W/L=5 and L=180nm, L=1um, Vds=1, Vgs=1

Where γ is is junction depletion region coefficient and depends on the used technology but is not voltage dependent. Φ is Fermi potential. This effect can be avoided by connecting bulk to source of the transistor, but that is not always possible, since it depends on the technology. Also, it adds a technology step into manufacturing process, so the cost of the chip rises. Since our technology used P-doped substrate, the bulks of all NMOS devices are connected to the most negative potential to ensure that PN junction substrate diodes of the device stay reverse-biased. PMOS devices on the other hand are put into an N-well so they can have their own substrate, which allows PMOS devices to have their bulk always connected to their source, regardless of their position in the circuit.

On figure 3.11 we can see a that V_{TH} increases at shorter channel lengths. This is called reverse short channel effect which is a result of non-uniform channel doping (halo doping). Channels are more doped near the drain and source terminals which reduces the size of depletion region near these junctions. At shorter channel length the doping of the source overlaps the doping of the drain, which increases the average channel doping concentration and this translates into increase of threshold voltage.

Also effect of the process must be taken into account. Process parameters are roughly the same for the same die, but the absolute values from die to die can vary significantly. So called process corners must be taken into account, which means that we have to predict, how much can process corner change and simulate for the worst cases. The corner values should be made available by the foundry and include maximum change in absolute values like oxide thickness t_{ox}, threshold voltage, gate length and gate width. Here in figure 3.11 can see the model file parameter transitions even more clearly than in the previous figures, because the model file has different threshold voltages for different channel lengths, hence we see the sharp transitions in the threshold voltage along with its smooth change with channel length.

And last but not least, is the effect of temperature on threshold voltage.

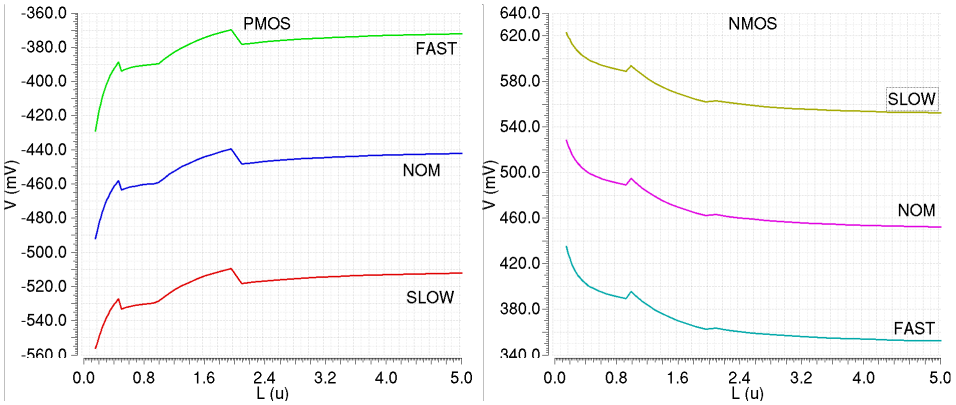

Figure 3.11: Vth vs L of NMOS and PMOS for W/L=5 and L=180nm, L=1um, Vds=1, Vgs=1

From [2] the temperature coefficient of threshold voltage is defined as

$$TCV_{TH} = \frac{1}{V_{TH}} \frac{\delta V_{TH}}{\delta T} \quad [1/K] \tag{3.13}$$

and thus threshold voltage can be written as a function of temperature as

$$V_{TH}(T) = V_{TH}(T_0) \cdot (1 + TCV_{TH}) \cdot (T - T_0)) \quad [V] \tag{3.14}$$

As we can see on fig 3.12, the variation in threshold voltage with temperature changes is quite significant. This introduces another corner to be analyzed, because the circuit must function properly over given temperature range.

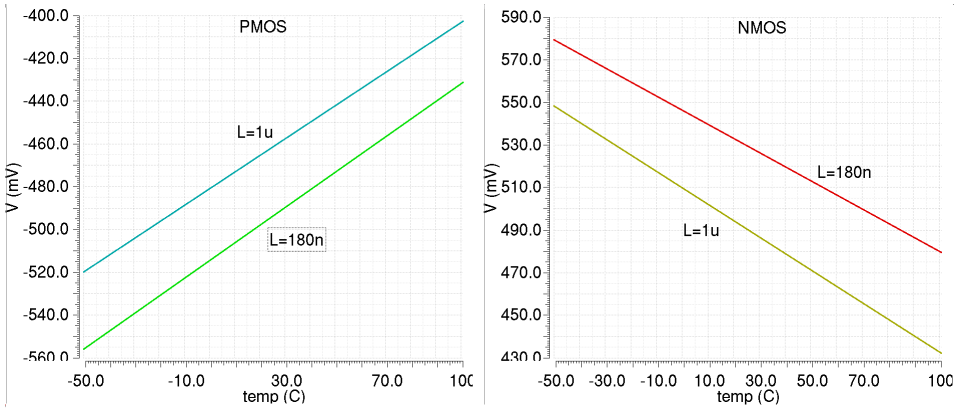

Figure 3.12: Vth vs temperature of NMOS and PMOS for W/L=5 and L=180nm, L=1um, Vds=1, Vgs=1

3.6 Passive Components

One can hardly design any circuit without use of passive elements like resistors or capacitors, especially when trying to stabilize the circuit in negative

feedback configuration. Problem is that resistors and capacitors take large areas on the chip which is not cost-effective in terms of fabrication, thus we try to minimize their values as much as possible.

3.6.1 Resistors

A resistor is made with a given resistive layer, depending on the type of resistor. Its resistance is given by:

$$R = 2 \cdot R_{cont} + R_{\square} \cdot \frac{L}{W} \quad [\Omega] \tag{3.15}$$

Where $R_{\square}$ is the sheet resistance measured in ohms per square units ($\Omega/_{\square}$), R_{cont} is resistance of the contacts, W is width and L is length. The sheet resistance is given by:

$$R_{\square} = \frac{\rho}{t} \quad [\omega/\square] \tag{3.16}$$

Where ρ is resistivity of the material, t is its thickness

In GPDK180 we have diffused as well as poly-silicon resistors. Since we are aiming for maintaining stability by introducing zeros in to the system, the poly-silicon resistor is the best choice, because it has lower temperature coefficient and overall better accuracy. Poly-silicon layer resistors have small resistance values, but we have high-resistance poly-silicon resistor at our disposal as well as low-resistance poly-silicon.

Accuracy

From the 3.15 without the contact resistance, we can write the standard deviation of resistance as:

$$(\sigma_R)^2 = \left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta \rho}{\rho}\right)^2 + \left(\frac{\Delta t}{t}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 \tag{3.17}$$

The accuracy is affected by the process (doping, physical structure, defects), environment (stress, temperature), litography (mask making, etching). All these parameters have impact on the final value of a resistor and its absolute accuracy.

While absolute accuracy of a single resistor is very poor (in tens of percents), the relative accuracy also called matching accuracy can be achieved very small (under one percent) with the right layout rules.

Temperature Coefficient

Temperature coefficient represent the resistor value dependence on ambient temperature. The value of resistor is usually specified as $R(T_0)$ for room temperature and from it, its resistance dependence upon temperature is defined as:

$$R(T) = R(T_0) \cdot (1 + TCR1 \cdot (T - T_0)) \quad [\omega] \tag{3.18}$$

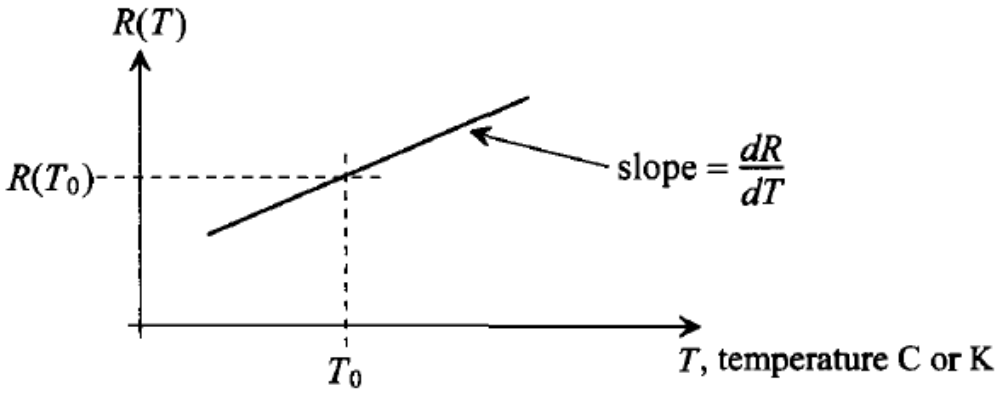

Figure 3.13: Dependence of resistor value upon temperature [2]

Where T is the actual temperature of the resistor and the first order coefficient of a resistor $TCR1$ is given by:

$$TCR1 = \frac{1}{R} \cdot \frac{dR}{dT} \quad [1/K] \tag{3.19}$$

This is only first order term and for example SPICE simulator also utilizes the second order temperature coefficient, so the more precise equations is:

$$R(T) = R(T_0) \cdot [(1 + TCR1 \cdot (T - T_0)) + TCR2 \cdot (T - T_0)^2] \quad [\Omega] \tag{3.20}$$

It is important to note, that temperature coefficient can be both positive or negative. It depends on the

Voltage Coefficient

Voltage coefficient is another important contributor to the change of resistor value and is given by:

$$VCR = \frac{1}{R} \cdot \frac{dR}{dV} \quad [1/V] \tag{3.21}$$

Where V is the average voltage applied to the resistor. That is sum of the voltages on each end of the resistor divided by two. The equation for resistance dependent on voltage is then given by:

$$R(V) = R(V_0) \cdot [(1 + VCR1 \cdot (V - V_0)) + VCR2 \cdot (V - V_0)^2] \quad [\Omega] \tag{3.22}$$

Where the value $R(V_0)$ is the value of resistor at voltage V_0.

3.6.2 Capacitors

In GPDK180 we have two capacitor models. First is mimcap, which is metal-insulator-metal capacitor and has low capacitance. Second is nmoscap, which is nothing else than NMOS device behaving as a capacitor (drain, source and bulk connected together). Nmoscap has higher capacitance to area ratio, but

its capacitance is not as stable under varying temperature and voltage as in the case of mimcap.

Temperature and voltage coefficients for capacitors are defined in the same way as for resistors.

3.6.3 Passive Component Parameters

Capacitors		Resistors	
device	Plate capacitance fF/um^2	device	Sheet resistance $\Omega/\square$
mimcap	1.1	Polyhres	352
nmoscap	8	Polyres	7.5
-	-	Mres	0.01

Table 3.1: GPDK180 passive component values

3.7 Technology Parameters

Parameter	NMOS	PMOS
Max. supply voltage	3.3 V	3.3 V
Maximum gate length	20 um	20 um
Minimum gate length	180 nm	180 nm
Maximum gate width	100 um	100 um
Minimum gate width	420 nm	420 nm
Threshold voltage (V_{SB}=0)	0.48 V	-0.43 V
Gate oxide thickness t_{ox}	4 nm	4 nm
Gate oxide Cap. C_{ox}	8.62 fF/um^2	8.62 fF/um^2
Transconductance parameter KP	327 uA/V^2	64 uA/V^2

Table 3.2: GPDK180 process parameters

Chapter 4

Stability and Power Supply Rejection

Feedback is essential for correct operation of linear regulators. The load current values may be in decades apart, so the system needs feedback to correctly adjust itself to the varying load. As we are not trying to design an oscillator, this chapter will be dealing with negative feedback only, which is essential for regulation voltages and currents.

4.1 Feedback Loop

In figure 4.1 we can see basic building blocks of an feedback loop. The loop must contain a sampling circuit, which senses the output and a mixer, which mixes the input sign s_I with signal from the feedback loop s_{FB}.

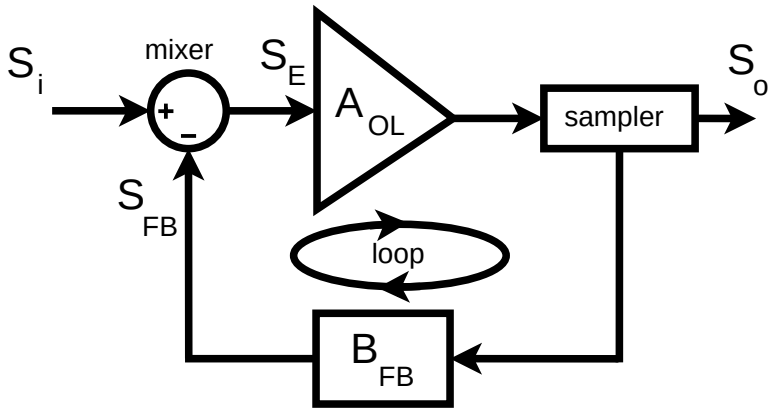

Figure 4.1: block representation of feedback loop

Gain from mixer to to the sampler is called forward open-loop gain or A_{OL} and the β_{FB} represent the feedback factor. Combining them, we can define the loop gain A_{LG} across the whole loop as

$$A_{LG} = A_{OL}\beta_{FB} \tag{4.1}$$

Since the loop implements negative feedback, the gain across the loop is inverting, that is why the input mixer has negative sign. When A_{OL} or β_{FB} becomes negative, the feedback becomes positive and that may leads to oscillation, depending on the magnitude of A_{OL}.

The regulation effect is obtained from the A_{OL} itself, because the system stabilizes when the error signal s_E which is a difference between input signal s_I and feedback signal s_{FB}, is close to zero. The feedback signal s_{FB} practically mirrors s_I. We can write

$$s_E = s_I - s_{FB} = s_I - s_E A_{OL}\beta_{FB} = s_i - s_E A_{LG} = \frac{s_I}{1 + A_{LG}} \tag{4.2}$$

and it its clear that the higher the A_{LG} is, the close to zero the error signal is. Thus, increasing loop gain translates into better accuracy.

$$s_{FB} = s_E A_{OL}\beta_{FB} = s_E A_{LG} = (s_I - s_{FB})A_{LG} = \frac{s_I A_{LG}}{1 + A_{LG}} \approx s_I \tag{4.3}$$

Feedback factor β_{FB} purpose is to sense output signal s_O and translate it so it is comparable with input signal s_I.

$$s_O = (s_I - s_{FB})A_{OL} = (s_I - s_O\beta_{FB})A_{OL} = \frac{s_I A_{OL}}{1 + A_{OL}\beta_{FB}} \approx \frac{s_I}{\beta_{FB}} \tag{4.4}$$

Now we can define closed-loop gain A_{CL}

$$A_{CL} = \frac{s_O}{s_I} = \frac{A_{OL}}{1 + A_{OL}\beta_{FB}} \approx \frac{1}{\beta_{FB}} \tag{4.5}$$

From these equation we can come to few important conclusions about feedback loop. The effective gain which is between s_I and s_O is the smaller one of A_{OL} and $1/\beta_{FB}$. Feedback factor is usually a lot smaller, especially in the case of regulators.

So the β_{FB} defines how is the output scaled to the input at steady state and open-loop gain defines how fast the system regulates itself to match the scaled output to the input.

4.2 Stability

Now when we defined open loop gain of negative feedback, we can define and analyze the criteria of stability of the system. The open-loop gain is a function of frequency and as such its transfer function may contain various poles and zeros which define system stability.

Poles are roots of the transfer function denominator and zeros are the roots of the numerator. They can further be split into left half plane and right half plane poles and zeros in the s-plane. Basic criterion for stable system is that no pole is in the right half plane, since its impulse response is increasing exponential function. Poles and zeros have different effect on magnitude and phase plot of open loop gain transfer function. It is important to note that the phase shift start at frequency decade below the pole or zero and ends decade above, so the phase shift at the pole or zero frequency is 45 degrees.

The pole on lowest frequency set the frequency where open loop gain falls bellow one, or unity-gain frequency. We can say that if the phase at this

type	magnitude	phase shift
LHP pole	-20db/dec	-90 deg.
RHP zero	+20db/dec	-90 deg.
LHP zero	+20db/dec	+90 deg.

Table 4.1: Pole and zeros effect on Phase and Gain

frequency did not change more than 180° the system is stable, because when the phase crosses 180° and the gain is below unity, the system does not produce unbounded output. However in multi-pole systems, the phase may deteriorate faster than gain and problems with stability may arise.

In practice, even the simplest form of feedback introduces at least one pole, which limits the frequency bandwidth (GBW) of the system. At this pole, open loop gain starts to decrease at rate of $-20\ dB/dec.$ and the phase shifts by $-90°$. The GBW for this one pole system can be defined as

$$GBW = A_{LG} \cdot \beta_{FB} \cdot pBW = f_{0dB} \quad [f] \tag{4.6}$$

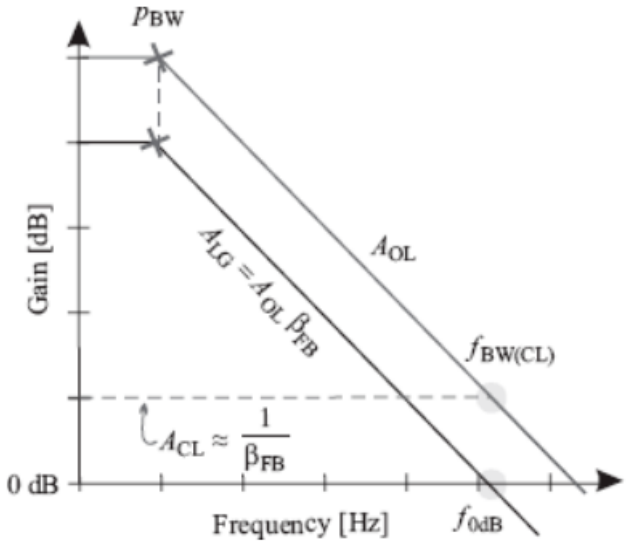

Figure 4.2: A_{LG}, A_{OL}, A_{CL} responses [15]

As we can see, the closed-loop gain is constant and starts to fall when open-loop gain reaches zero decibels. The open loop gain equals to 1 ($0dB$) at the unity-gain frequency f_{0db} for this single pole system. Closed-loop gain pole is higher than the open-loop gain and loop gain magnitude is $1/\beta_{FB}$ lower than the magnitude of open loop gain. β_{FB} is usually lower or equal to 1 and it states how "strong" feedback is applied.

Uncompensated System

In real circuit, every node introduces a pole so it is common to that the system will have more poles in its bandwidth. Also gain is obtained by large

transconductances, feeding currents into high-impedance nodes so even a small parasitic capacitance, shunting large resistance can introduce a low frequency pole. In figure 4.3 we can see how the response of two poles of which the second one is in the bandwidth of the first one (dominant pole). At the frequency of the second pole, the gain starts to drop at $-40dB/dec$

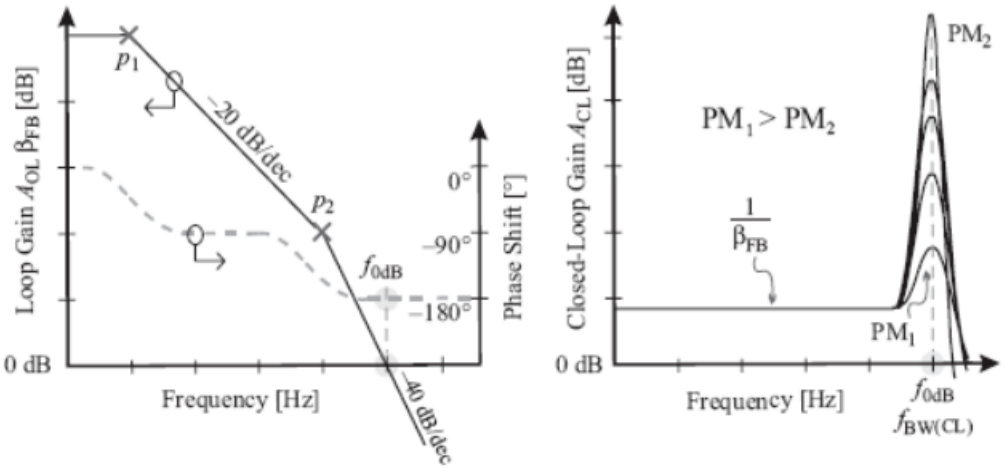

Figure 4.3: Uncompensated loop-gain and closed-loop gain responses [15]

but the phase is already only 135° and reaches 180° phase shift before unity loop-gain. At that point, the output of the system rises exponentially and the loop amplifies any noise at f_{0dB}. This leads to instability and possible oscillation at the output of the system.

Compensated System

Vulnerability of feedback systems to oscillation forces us to closely simulate the system and assure that it is stable under all operating and bias conditions. Lets define two elementary stability criteria, which defines how robust or how far is the system from unstable region.

First one and the most important is *phase margin* PM, which states how much the phase shifted at unity loop gain frequency f_{0dB}

$$PM = 180° - |\Delta\phi| \Big|_{f=f_{0dB}} \quad [degrees] \tag{4.7}$$

Second one is *gain margin* GM, which states how much the loop gain drops before the phase shifts by 180° and the feedback becomes positive.

$$GM = 20\log_{10}|A_{OL}\beta_{BF}| \ [dB] \tag{4.8}$$

The goal of the compensation is to shift second pole to the unity gain frequency or higher, that gives us a minimum of 45° PM or to introduces LHP zeros to compensate the phase shift of the poles. As we can see in fig 4.4 there are three poles of interest, p_1 is dominant, p_X effect is compensated

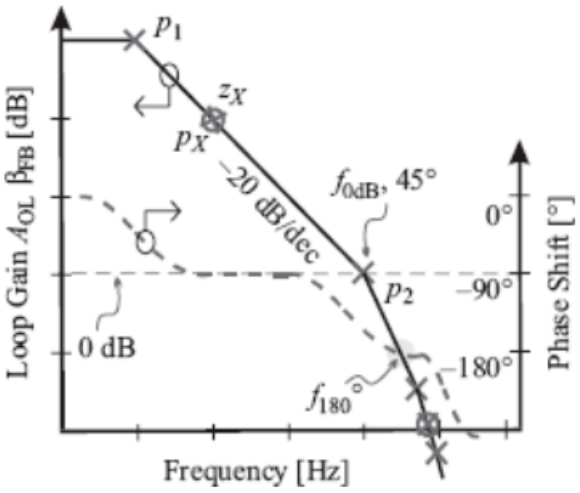

Figure 4.4: Compensated loop-gain gain response [15]

with LHP zero z_X, p_2 is at f_{0dB}, the rest is almost a decade above unity gain frequency and does not contribute much to the phase shift at f_{0db}.

Phase margin is also very important parameter in determining the time response of a system to a step input. On the figure 4.5 we can observer how output behaves. When the phase margin is low, the output suffers from large overshoot and undershoot and ringing. When the phase margin is high, the settling time is long. So ideal value of phase margin is about 72°, where the best compromise between settling time and ringing is achieved.

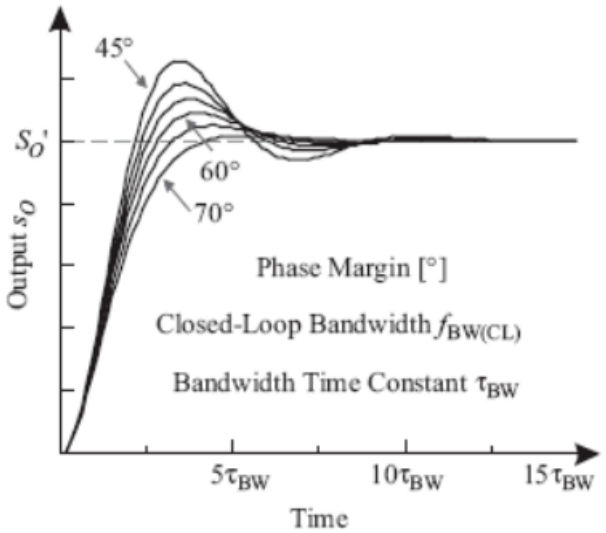

Figure 4.5: Compensated time-domain response to a stepped input [15]

4.2.1 LDO Small Signal Model

Now that we have defined basic stability criteria, to analyze the stability of the LDO, it is useful to present a small signal model. The error amplifier A_E

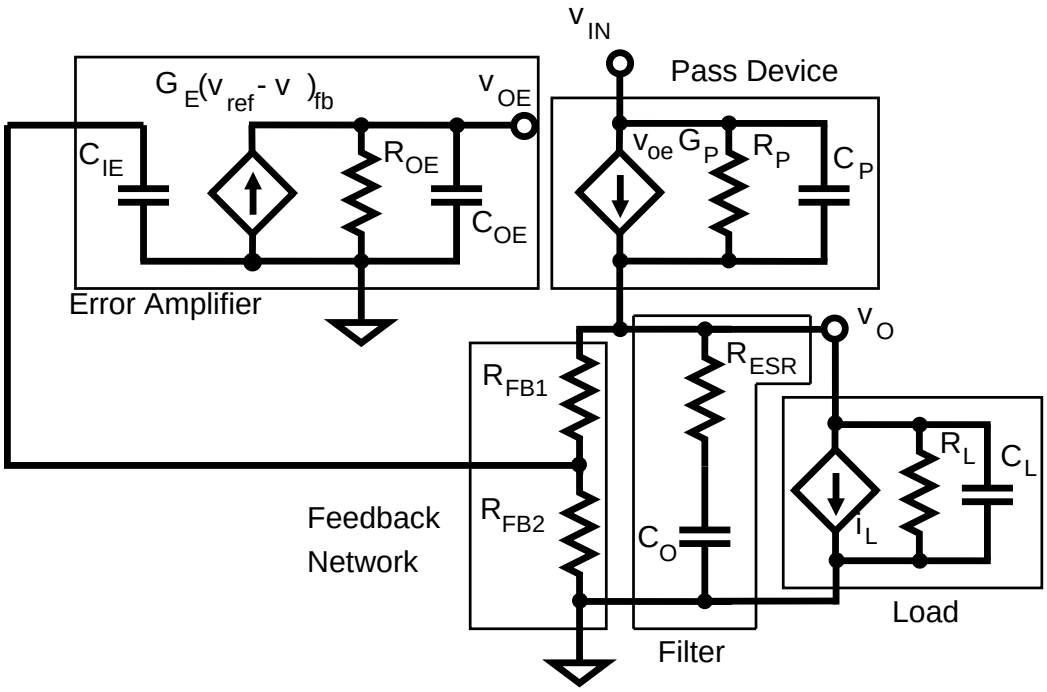

Figure 4.6: Small signal model of LDO linear voltage regulator

has a large output resistance R_{OE} which the large capacitance at its output, coming mainly from the large pass device, shunts and creates a pole at low frequency.

$$p_{A_E} = \frac{1}{2\pi R_{OE} C_{OE}} \quad [Hz] \tag{4.9}$$

Another pole will be at the output where output capacitors C_O, C_L and C_P shunt output resistances R_{FB1}, R_{FB2}, R_L and R_P. If we take into account that the output capacitor will be large and the resistance of pass device will be small, the equation can be reduced as follows.

$$p_O = \frac{1}{2\pi(R_{FB1} + R_{FB2}||R_L||R_P)(C_O + C_L + C_P)} \approx \frac{1}{2\pi C_O R_P} \quad [Hz] \tag{4.10}$$

Since the output capacitor incorporates a equivalent series resistance, it form a zero.

$$z_{ESR} = \frac{1}{2\pi C_O R_{ESR}} \quad [Hz] \tag{4.11}$$

This zero can be used as a phase saving zero in our design, if we shift it to low enough frequencies, but that depends of the size of the capacitor and its ESR depends on its type.

The frequency response of an uncompensated LDO can look like this. The

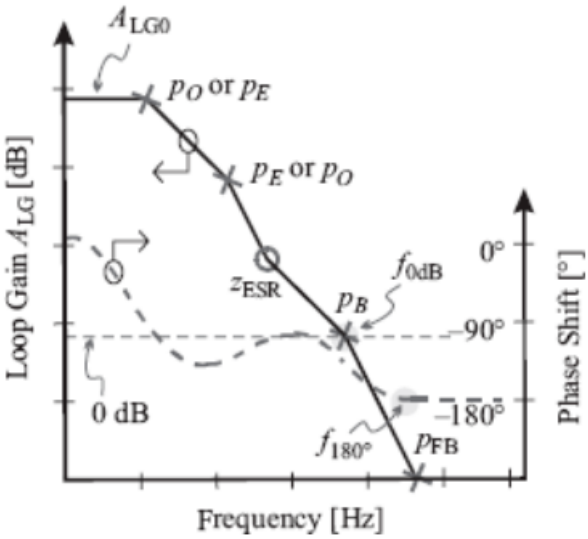

Figure 4.7: Frequency response of uncompesated LDO [15]

pole at the output of the error amplifier p_{EA} and the pole at the output of the LDO p_O are both at low frequency which and that causes the system to be rather unstable.

When stabilizing an LDO we have to choose between two main paths, based upon our specification. The first one places output pole at low frequency by adding large output capacitor C_O, thus making it dominant. This method is mainly used in high power LDO application with large load transients, upto hundreds of mA. That forces us to shift the pole of the error amplifier to largest frequency possible or to introduce phase saving zeros to compensate its effect.

Second path places the pole at the output of the error amplifier at low frequency, making it dominant. This requires the output capacitor to be as small as possible, but that makes the system sensitive to load transients. Thus, this type of compensation is suitable for lower currents and on-chip type of LDOs.

Since our specification says to use $1uF$ output capacitor, our dominant pole is the output pole, thus our goal is to push the pole p_{EA} at the output of the error amplifier to highest possible frequency. This can be accomplished by reducing output resistance of the error amplifier R_OE, but that also reduces the overall loop-gain of the system which results in reduction of the accuracy at the LDO output and also in higher quiescent current. The stability design issue of our case will be presented in the design chapter.

4.2.2 Power Supply Ripple Rejection

As said before, the LDO linear voltage regulator is commonly used as a second stage after a switched-mode regulator, to filter its output ripple. The power supply rejection (PSR) is defined as ability of the circuit to oppose the

fluctuations of voltage at its supply rails. Both negative and positive supply rail should be taken into account, but since we have single positive supply rail, we will be dealing only with positive PSR.

Power supply gain A_{IN} is the small signal gain of from the positive supply rail, to the output of the circuit. PSR is defined as its reciprocal value.

$$PSR = \frac{1}{A_{IN}} = \frac{\delta v_{in}}{\delta v_o} = \frac{v_{in}}{v_o} \tag{4.12}$$

To analyze PSR of an LDO and to obtain voltage gain A_{IN} from power supply to output a voltage divider model is utilized. Such a model is in the figure 4.8 Pass device transconductance G_P feeds the ripple from the error

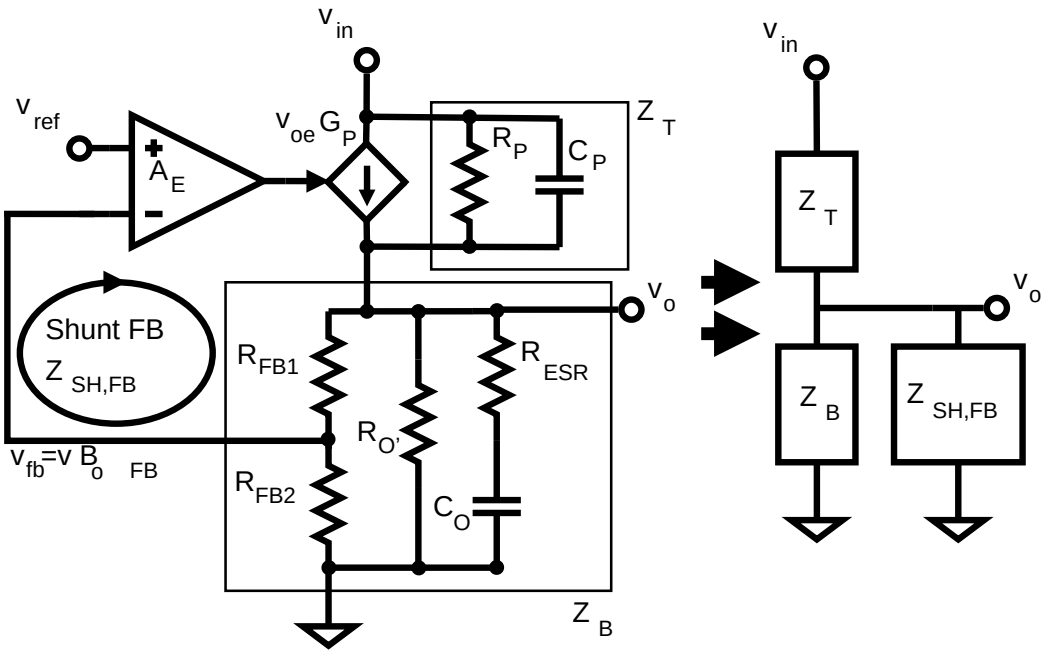

Figure 4.8: Voltage divider model of LDO

amplifier A_E to the output and it depends on the type of the pass how that noise affect the LDO output. If we have NMOS type pass device, the noise that is present at the gate of the transistor is reproduced at its output, so the error amplifier should suppress as much noise as possible.

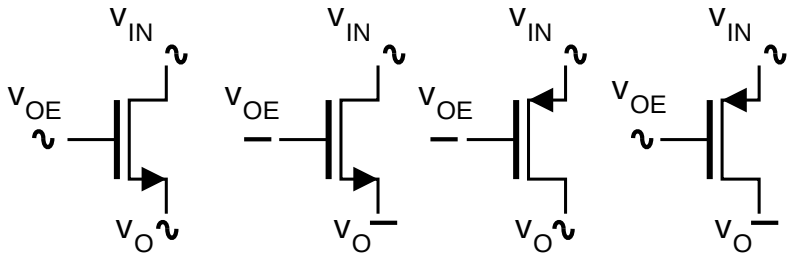

Figure 4.9: Illustration of ripple feed of NMOS and PMOS pass devices

On the other hand, when a PMOS type pass device is used, the source is connected directly to the input supply, so when they do not have any supply noise at their gate, the supply noise from source is transferred to the drain through transconductance. When same supply noise is applied at the gate of the pass transistor, it cancels out the effect of the supply noise at the source. So it is not always convenient to have supply noise-free output of the error amplifier A_E.

Since we will be using differential amplifier as an input mixer of the reference and feedback voltage, it is an important step to discuss its PSR behavior. The amplifier will be loaded with current mirror and depending on the type of the mirror, the PSR will be either large at the output of the error amplifier or low.

If we take a look at small signal models of current mirrors, the ripples at the input supply v_in creates a small signal current i_in through the their resistances R_{EQ} and $1/g_m$ and since the $1/g_m$ part is small it can be neglected as follows:

$$i_{in} = \frac{v_{in}}{R_{EQ} + 1/gm} \approx \frac{v_{in}}{R_{EQ}} \quad [A] \tag{4.13}$$

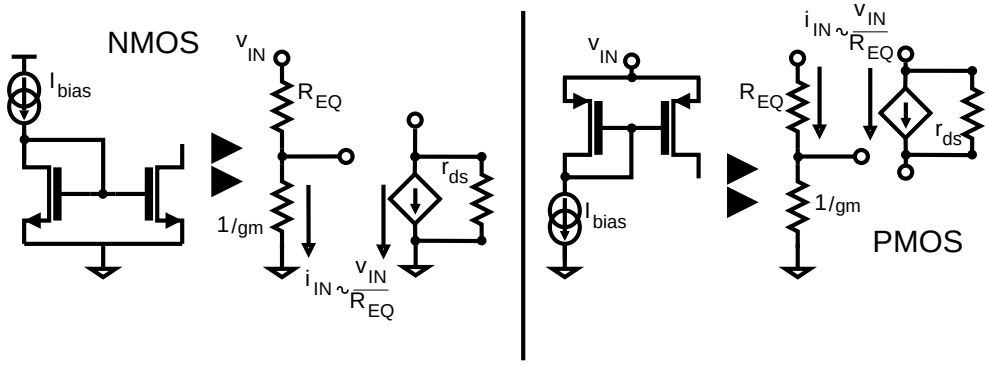

Figure 4.10: Illustration of ripple feed of NMOS and PMOS pass devices

From figure 4.10 it is obvious, that NMOS mirror sinks supply ripple, while PMOS mirror sources the ripple to its output. Thus if their output is connected together, and are balanced, then NMOS sinks the ripples of PMOS and the output should be ripple-free.

Now, if we return to the voltage divider model we introduced earlier we can write

$$A_{IN} = \frac{1}{PSR} = \frac{v_o}{v_{in}} = \frac{Z_{B'}}{T_T + Z_{B'}} \tag{4.14}$$

Where $Z_{B'}$ is the combination of impedance Z_B and $Z_{SH,FB}$. Now to discover the effects of the frequency upon PSR, we need to analyze equation 4.14 over frequency. At low frequency, capacitors does not affect the circuit and as [15] states, the power supply gain reduces to

$$A_{IN0} = \frac{1}{PSR_0} = \frac{1}{A_{LG0}} \approx LNR \tag{4.15}$$

The variation of PSR across frequency is caused by the capacitor beginning to shunt the resistances in the voltage divider model. At low frequencies, the $Z_{SH,FB}$ shunts Z_B and the PSR is defined by the loop gain A_{LG}. At moderate frequencies, above the f_{0dB}, the $Z_{SH,FB}$ impedance increases and this increases the output ripple and the output ripple at this point peaks. At high frequencies, the output capacitor start to shunt R_{FB1} and R_{FB2}, the ripple start to decrease again. Thus the PSR can be divided into three regions as seen in following figure.

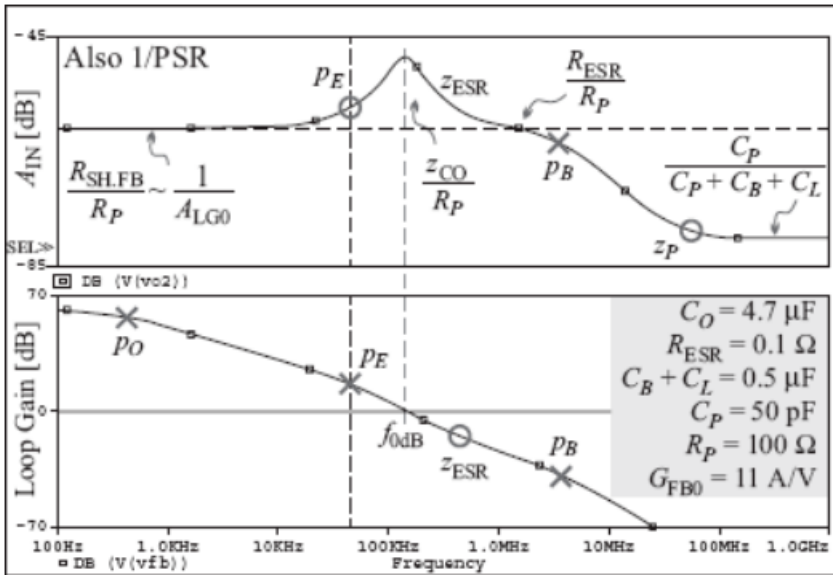

Figure 4.11: Three regions of LDO power supply ripple rejection [15]

Chapter 5
LDO Design

To start designing LDO, we need to first look at the specifications that were given to us. We have to design a low dropout voltage regulator with these parameters:

- output voltage $1.5V$
- input voltage from $1.7V$ to $2V$
- input reference voltage $1.2V$
- load current from $10uA$ to $1mA$ with $10\%error$
- fastest change in load current $1us$
- output capacitor of $1uF$ with 20% error
- temperature in range $-50°C$ to $100°C$
- maximum quiescent current $10uA$
- biasing current of $100nA$ with 20% error and temperature coefficient of $3mV/K$

From these specifications, we can derive, that the circuit must me simple, because the current consumption has to be minimal. The best way to start designing an LDO regulator is from the output, so we start with designing the pass device and feedback resistor divider.

5.1 Feedback Voltage Divider

At first, we need to define the ratio of the feedback factor β_{FB} which states what the division of the output voltage will be, before its comparation with reference voltage via the differential amplifier. The reference voltage is $1.2V$ and the output voltage is $1.5V$ so the feedback factor in ours case is

$$\beta_{FB} = \frac{V_FB}{V_O} = \frac{1.2}{1.5} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = 0.8 \tag{5.1}$$

The ratio between the resistors is known, but we must also define absolute values for the sake of current consumption (the current through the divider is wasted) and stability, because we will be using the divider to assure stability of the circuit, that will be dealt with later.

5.2 Pass Element Design

From the input voltage range which is from 1.7 V to 2 V and output voltage specification which is 1.5V we can derive, that maximum dropout voltage can be 200 mV. We have two choices of pass devices to choose from, NMOS or PMOS. As stated in subsection 2.2.4, the PMOS has substantially lower demand on the minimum input voltage, because the minimum voltage needed to stay in saturation is given only by its saturation voltage $V_{DS,sat}$. If we wanted to use NMOS, it would be possible, but because of input voltage specification, a charge pump would be needed, to raise the gate voltage of the NMOS pass element to sufficient level for it to be under proper bias conditions. That would furthermore complicate our circuit and since we have tight specification on low quiescent current it would be also inefficient in terms of power consumption. The PMOS is ultimately the best choice for out application because of its low dropout voltage.

Now that we decided that our pass element will be a PMOS device, we need to take into account maximum load current that will be flowing through it. Specification states 1mA maximum load current with up to 10% possible variation and that gives us a total of 1.1mA maximum load current. We want the pass transistor to stay in the saturation region under all load conditions, so we will utilize square-law equation for drain current to calculate the minimum W/L ratio of the pass device. Neglecting channel length modulation we have

$$I_D = \frac{1}{2}\mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \Rightarrow \frac{W}{L} = \frac{I_D}{\frac{1}{2}\mu C_{ox} \cdot (V_{GS} - V_{TH})^2} \quad [A] \quad (5.2)$$

but this value could change drastically under the effect of process corners and temperature, so to be sure that the pass device does not goes into triode region, the pass device should be scaled to larger W/L according to the worst corner in simulation, but not extensively high, because the larger the area of the gate, the larger the capacitance which slows the the response of the system and deteriorates its stability.

5.3 Buffer

Now that we have chosen the pass device we may continue in the design of next stages. Since the pass device gate area is large, it introduce a large parasitic capacitance C_{IP} at its gate. In our case the capacitance is not so large to impose a slew-rate constraint, but it poses a problem for the system stability, because to produce sufficient loop gain A_{LG}, there must be a large resistance R_{OE} in the node at the output of the error amplifier A_E. R_{OE}

together with C_{IP} introduce a low-frequency pole p_{OE} which will threaten the stability of the system. Thus a buffer amplifier A_B is utilized. A_B must have small input capacitance, small output impedance and large enough voltage swing across its output to be able to both shut the pass device off and drive it fully at maximum load current. A PMOS source follower has been chosen. Its problem is however, that it may hinder the dropout voltage of the PMOS pass device, because of how low its source-gate voltage can fall in respect to V_{IN}.

$$V_{DO} \propto \frac{1}{V_{SG,PASS}} = \frac{1}{V_{IN} - V_{O,BUF}} = \frac{1}{V_{IN} - (V_{SG,BUF} + V_{OE})} \quad [V] \quad (5.3)$$

Where V_{DO} is dropout voltage, $V_{SG,PASS}$ is pass transistor source-gate voltage, V_{IN} is input voltage, $V_{O,BUF}$ is buffer output voltage, $V_{SG,BUG}$ is buffer source-gate voltage and V_{OE} is error amplifier output voltage.

5.4 Error Amplifier

To choose the right topology for the error amplifier, we have to consider all the previous constraints and parameters as in the case of pass device and buffer. The goal should be low quiescent current, proper bias under all load current and input voltage conditions and also high enough gain to provide sufficient accuracy and PSR at the output, but not excessively high so that the system remains stable. Systematic and random input-referred offset should be low as well. Another thing to be considered is the architecture of the error amplifier itself, so it can drive the buffer properly.

5.4.1 Differential Pair

The reference voltage v_{ref} may be a limiting factor when selecting the differential amplifier topology. If we take a look at the PMOS differential pair, the minimal headroom it needs above V_{ref} is

$$V_{IN,min} = V_{ref} + V_{SD,sat} + V_{SG} = 2 \cdot V_{SD,sat} + V_{THP} + V_{ref} \quad [V] \quad (5.4)$$

Where $V_{IN,min}$ is the minimum input voltage, $V_{SD,sat}$ is the saturation voltage of PMOS, V_{THP} is its threshold voltage and V_{SG} is its source-gate voltage.

For the NMOS differential pair, the situation changes. The V_{ref} defines the headroom for the input pair and the biasing transistor M_T. The reference voltage has to be large enough to bias both M_T and input pair.

$$V_{ref,min} = V_{GS} + V_{DS,sat} = 2 \cdot V_{DS,sat} + V_{THN} \quad [V] \quad (5.5)$$

Since the minimal input voltage is 1.7 V and V_{ref} is 1.2 V, the headroom of 0.5 V is not enough for PMOS differential pair. So here, the choice is pretty straightforward, NMOS differential pair.

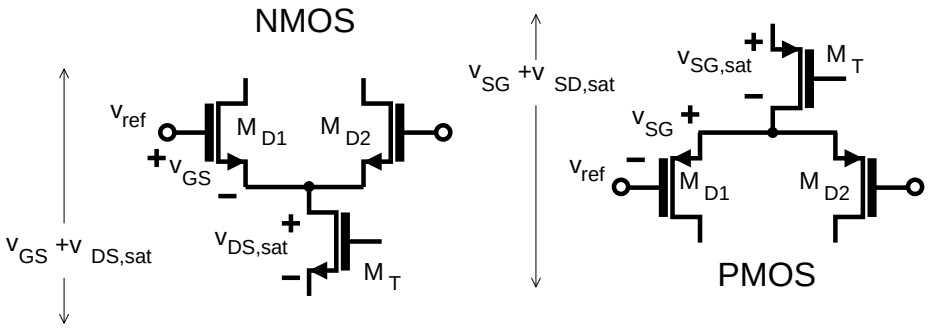

Figure 5.1: Headroom limits of PMOS and NMOS differential pair [15]

5.4.2 Error Amplifier Topology

A symmetrical OTA (operational transconductance amplifier) has been chosen as a final topology. The schematic is in figure 5.2. Compared to simple ota with differential pair, it has two more current branches, so it has larger quiescent current, but the main advantage of this topology is its large output swing. The minimum and maximum voltage at its output is limited only by the saturation voltage of the two transistors. So the minimum output voltage is the saturation voltage of NMOS.

$$V_{OE,min} = V_{DS,sat} \quad [V] \tag{5.6}$$

And the maximum is the saturation voltage of PMOS at the output stage.

$$V_{OE,max} = V_{IN} - V_{SD,sat} \quad [V] \tag{5.7}$$

This ensures that the error amplifier can drive the buffer and thus the pass transistor properly over specified load current conditions. The GBW of the OTA is large enough compared to the output dominant pole, so that is not a limiting factor. In terms of PSR the circuit is not completely symmetrical and the derivation of it is not so straight forward as for simple OTA with only one load current mirror. The PSR at the output of the symmetrical OTA depends on the summing of the NMOS a PMOS type mirrors PSR contributions. Also every node, except the output node of the OTA is gate-drain connected, which means that impedance at those nodes is low, because the impedance looking into the gate is $1/g_m$. In small signal model, this reduces the resistance at internal nodes to roughly $1/g_m$.

5.5 Final Design

In this section we will take closer look at the operation of the proposed LDO, how specified variation of parameters influence stability and bias conditions. The final design schematic is presented in figure 5.3, all bulks of NMOS transistors are connected to ground and all bulks of PMOS are connected to supply.

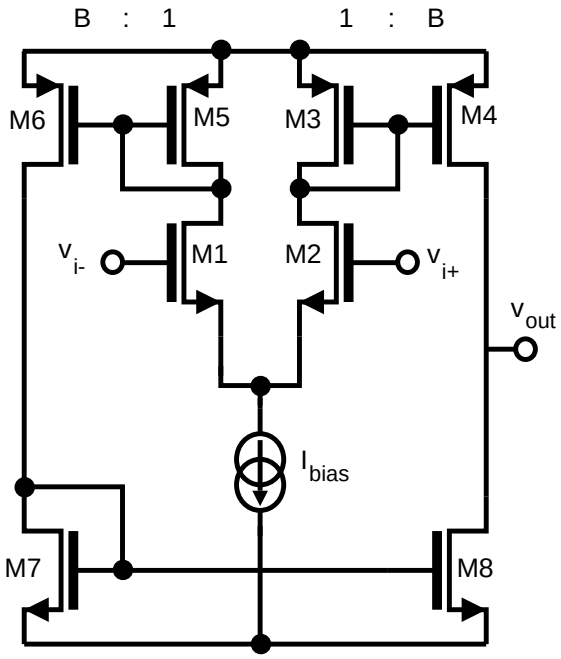

Figure 5.2: Symmetrical OTA schematic

First, we need to assure that the circuit is properly biased, assuring that every transistor is in saturation region is of paramount importance. Since the specification says that quiescent current has to be under $10uA$, we may predict that the W/L ratios of the error amplifier and the buffer wont be too large, because there wont be any excessive currents flowing. Next we should strive for putting the current mirrors into the strong inversion region for better matching, but again, since there are going to be small currents, its may is hard to achieve that, since increasing length of the transistors to push them into strong inversion also increases output resistance at the nodes and we are sacrificing stability for the sake of matching, which is not optimal. Therefore, we target to obtain as small g_m/I_D ratio as we can, to the extent of not compromising stability. Voltage v_{ref} is 1.2 V and that is high enough for the differential pair M1-M2 and the biasing transistor M4 to stay in saturation. Since the differential pair is for the sake of gain in weak inversion, $V_{DS,sat}$ of M1,M2 is low and thus it does not hinder the V_{DS} voltage headroom for upper current mirrors comprising of transistors M5-M6 and M7-M8. The main problem with saturation is with the transistor M10 at the output of the error amplifier. When the load current rises, the V_{SG} of the pass transistor needs to be increased via the feedback, to push more current through the pass transistor. Thus, the voltage at gate and at the buffer output V_{BUF} decreases and the output of the error amplifier V_{OE} also decreases, because it is only level shifted voltage from the buffer output. This may lead to transistor M10 falling into triode region, which would significantly reduce the gain of the error amplifier and thus overall accuracy and ability of the circuit to regulate properly. To ensure that the transistor M10 stays in saturation, we have to

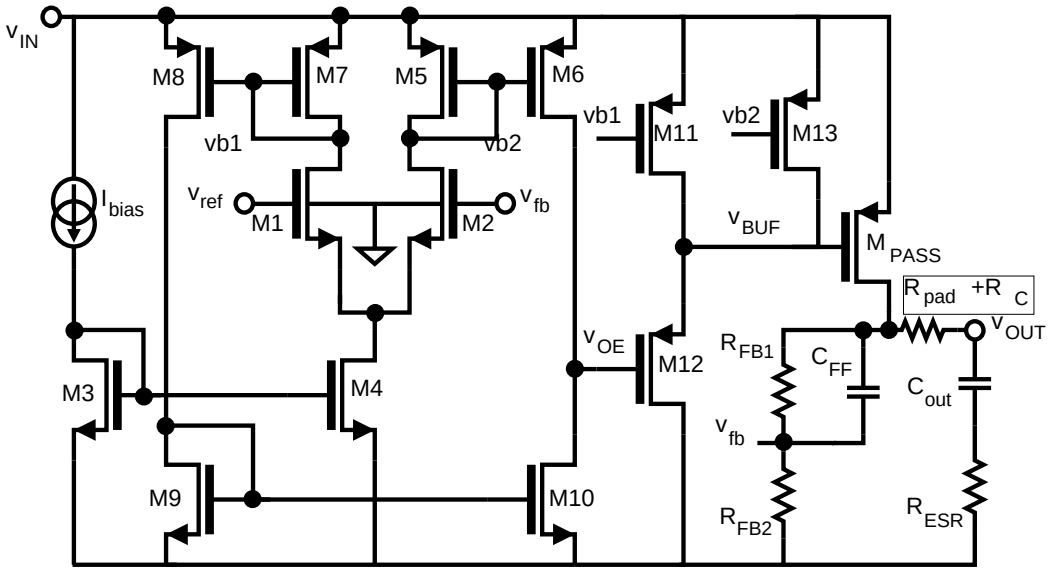

Figure 5.3: Final schematic of the proposed LDO

take a look at the worst corner, which will cause the highest voltage level shift of the buffer and design the buffer W/L ratio accordingly, so the M10 stays in saturation under all conditions. The W/L ratio of M_{PASS} is given by the maximum load current as stated earlier.

If we are sure that we have the circuit under proper bias conditions, we have to ensure that it is stable under all load conditions. In section 4.2 we have outlined the stability requirements and now we will take closer look at the exact poles and zeros of the final circuit. The output pole p_O is defined primarily by the resistance of the pass device R_P and the output capacitor C_O.

$$p_O = \frac{1}{2\pi C_O R_P} \quad [Hz] \tag{5.8}$$

The resistance of the pass device R_P relies on the load current. This is stated in equation 3.11, the larger the current I_{DS} the smaller the output resistance. From this we can assume, that the output pole p_O will be shifting with load current changes. Since mainly the output pole defines the unity-gain bandwidth f_{0db}, the bandwidth is also dependent on the load current. Under smaller load, the R_P is large and f_0dB is at very low frequency, the system is responding slowly to the changes of the input voltage and load current, but is unconditionally stable, because the rest of the poles lie high above the f_0dB. The other poles we need to take into account are the pole at the output of the error amplifier and at the output of the buffer. The error amplifier pole will be at low frequencies due to the high output resistance of the error amplifier. The pole is defined by its output resistance and the capacitance at its output

$$p_{A_E} = \frac{1}{2\pi R_{OE} C_{OE}} \quad [Hz] \tag{5.9}$$

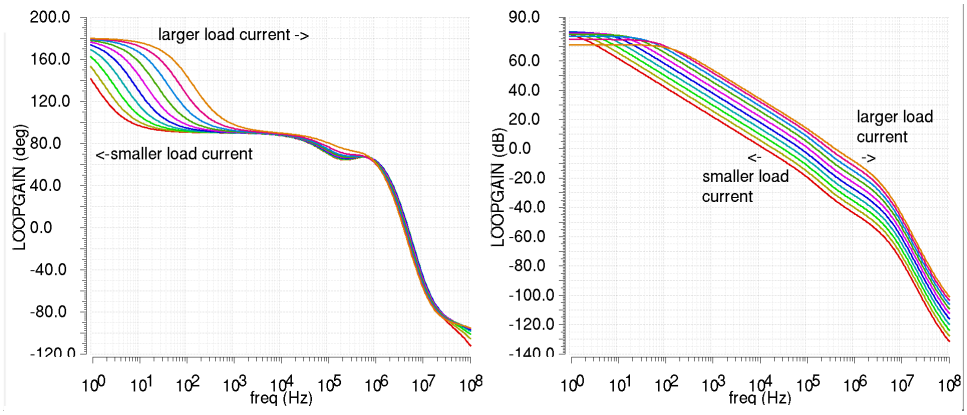

Figure 5.4: Dominant pole shifting to higher frequency with higher load current

where R_{OE} incorporates parallel combination of output resistances of transistors M6 and M10 and C_{OE} is the sum of parasitic capacitance present at the node.

The pole at the output of the buffer is defined similarly to the previous pole, but the buffer output resistance is much lower, due to the source of the Transistor M12 being connected to the node. This introduces resistance $1/g_m$ to the parallel combination of the output resistances, and since it is significantly smaller compared to the drain resistances of transistors M11 and M13, the output pole can be ultimately defined as

$$p_{A_{BUF}} = \frac{1}{2\pi \frac{1}{g_{m,12}} C_{O,BUF}} \quad [Hz] \tag{5.10}$$

where capacitance at the output of the buffer $C_{O,BUF}$ is mainly defined by the parasitic capacitance present at the gate of the PMOS pass device. The buffer output pole will be past the unity-gain bandwidth f_{0dB}. To push these poles to higher frequencies we can increase the biasing current of the error amplifier. This reduces the output resistance at all nodes and also increase the g_m of M12. Here a trade-off between stability, quiescent current and gain is presented, because loop gain A_{LG} is partly defined by the gain of the error amplifier A_{OE}. Since out specification states that the quiescent current must be under $10uA$ we aim for lowest value possible and we need to choose different way in stabilizing the system.

In our case more convenient way is to insert in phase zeros, which to an extent cancel the effects of the poles and allow us to keep phase from shifting by more than 135°.

One such zero is implicitly present because of the output capacitor equivalent series resistance (ESR).

$$z_{ESR} = \frac{1}{2\pi C_O R_{ESR}} \quad [Hz] \tag{5.11}$$

This zero can be utilized, but its effect on the stability can vary substantially with temperature and fabrication corners, that must be taken into account.

Also, at the minimum specified ESR, the zero will be at very high frequency and will not save almost any phase. But since the maximum load current is 1.1 mA, if we put a small resistance R_{pad} to the path of the load current, we can push the z_{ESR} to lower frequencies, and lose only small portion of output voltage. This also simulates the resistance of the pad and, which we decided to be between $200 - 500\ m\Omega$. This way we secure, that the circuit is stable for specified range of ESR. Since the error amplifier pole p_{A_E} will be below $f_{0dB,min}$ and z_{ESR} will be around f_{0dB} the phase margin would be deteriorated by buffer output pole $p_{A_{BUF}}$ and also by the parasitic poles at high frequencies, because their combined effect can have impact on the phase margin and especially gain margin.

It is important to introduce other zero which can be added by shunting the feedback resistor R_{FB1} with feed-forward capacitor C_{FF}. Thus we get

$$z_{FF} = \frac{1}{2\pi R_{FB1} C_{FF}} \quad [Hz] \tag{5.12}$$

For the sake of current consumption, it is convenient for us to make the resistors R_{FB1} and R_{FB2} as large as possible, but not too large, to properly drive the capacitance at the gate of transistor M2. This allows us to make capacitance C_{FF} relatively small so it does not consume vast area.

The best way to address the stability issue is to put the z_{FF} near the p_{A_E} and z_{ESR} near the $f_{0dB,min}$, since the minimum specified ESR is so small, it is more convenient for the z_{ESR} to be at higher frequency than z_{FF}. The final design phase and open loop gain response is in the next figure. The first pole is clearly the dominant output pole. Next we have sort of smooth transition and then z_{FF} is at about the same frequency as p_{A_E} which is past $100kHz$. The next transition is in between 1 MhZ and 10 MhZ where the effect of the $p_{A_{BUF}}$ and other parasitic is introduced and is to some extent compensated by the z_{ESR}.

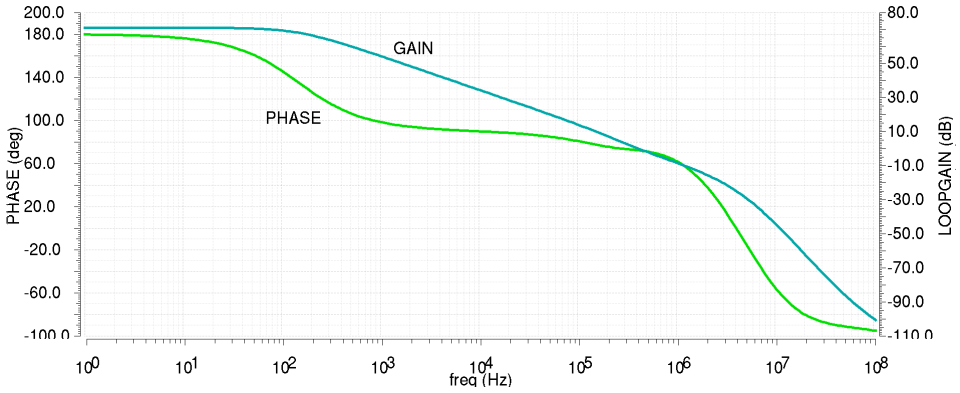

Figure 5.5: Phase and open-loop gain response of the final circuit at nominal corner

Now that we are assured that circuit is stable at the nominal corner, we should check the variation of the output due to the random offset. Problem is that the GPDK180 does not have mismatch modeled correctly. So to predict

the mismatch to at least some extent, the schematic was fully imported into GPDK090 technology. From the simulation the three-sigma variation of the output voltage was under 5 mV, but since the process constants which define the mismatch of the GPDK180 model are not known, it is only an crude approximation. The results from monte carlo simulation are in the following figure 5.6. The gate area of the devices was enlarged so that the threshold voltage mismatch (which was the highest) was minimized, based on the Pelgrom model [3].

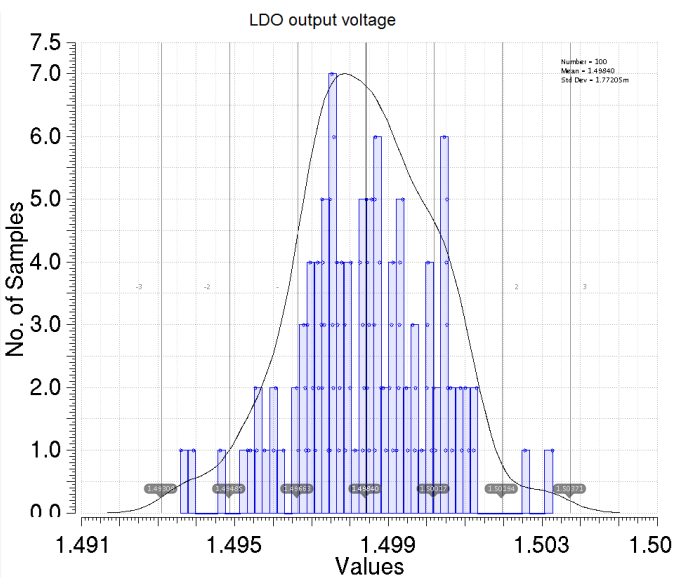

Figure 5.6: Distribution of the output voltage from monte carlo simulation

Device	W/L [um]
M_1 , M_2	2·20/1
M_3	1/20
M_4	10 ·(1/20)
M_5, M_6	3/3
M_7, M_8	3/3
M_9, M_{10}	2/5
M_{11}, M_{13}	3/3
M_{12}	10/0.6
M_{PASS}	10·(40/0.18)
Total Area 452 um^2	

Table 5.1: Final sizes of the circuit devices

component	W [um]	L [um]	value
R_{FB1}	0.6	340.85	200 $k\Omega$
R_{FB2}	0.6	1363.4	800 $k\Omega$
R_C	0.3	15	0.5 Ω
C_{FF}	62.5	20	7 pF
Total Area 2277 um^2			

Table 5.2: Final sizes of the circuit passive components

5.6 DC Results

This section focuses on steady state parameters of the LDO. They represent values at which the system settles after the transient response fades away.

5.6.1 Dropout Voltage

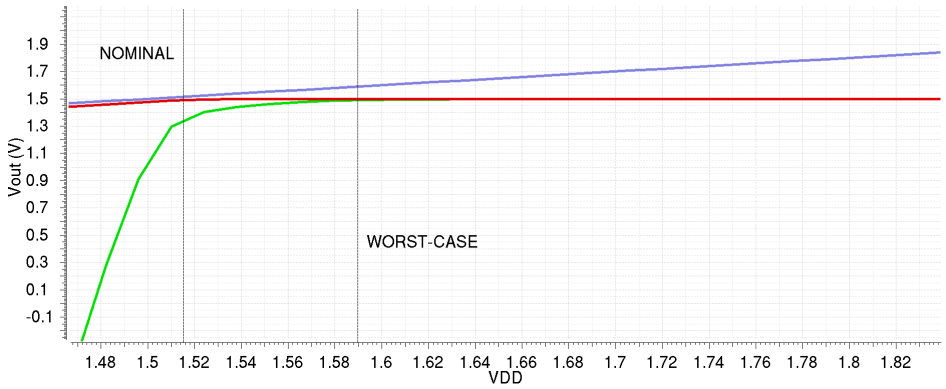

Figure 5.7: Input voltage sweep - dropout and regulation region

The dropout voltage was measured as the input voltage at which the output voltage starts to drop from its nominal value of 1.5 V and it was measured under maximum load current of 1.1 mA and in nominal corner. In figure 5.7 we can see, how the regulator ceases to regulate when input voltage falls bellow 1.57 V, that is when the pass transistor starts to operate in triode region and the system looses gain. Thus the feedback loop cannot keep output value as precise as before.

5.6.2 Line Regulation

The line regulation defines how the output behaves under slow change of the input supply. It is basically the steady DC power supply gain of the regulator. As we sweep the voltage at the input, we can observe the changing value at the output and calculate how much the output has changed with respect to the input. In the figure 5.8, the line regulation for nominal and worst corner

is presented. The worst corner, as expected, is for the lowest bias current and largest output capacitor, that translates into lower gain, which is proportional to the line regulation.

Figure 5.8: Line regulation for nominal and worst corner

5.6.3 Load Regulation

Another steady state parameter is load regulation. Since the loop gain is finite, the regulator cannot completely cancel the effect of changing load current. The load regulation is in figure 5.10.

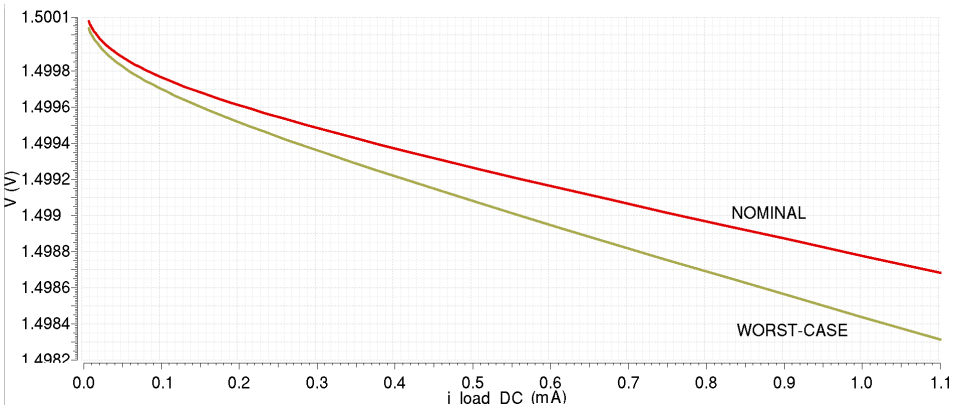

Figure 5.9: Load regulation for nominal and worst corner

5.6.4 Temperature Variation

It is useful to plot how the output changes with temperature, because the ambient temperature is could vary significantly, depending on the application where the LDO would be used.

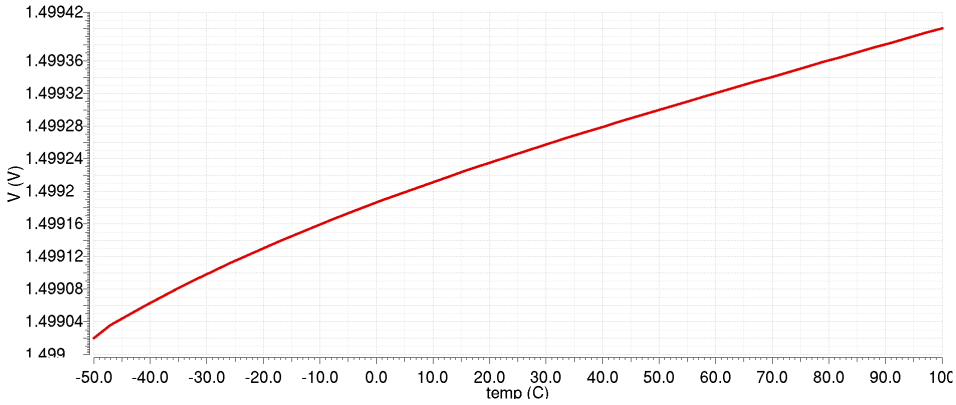

Figure 5.10: Output voltage variation with temperature

5.7 AC Parameters

It is important to measure the open loop parameters as open-loop gain and phase to define phase margin and gain margin. Also the unity gain bandwidth f_{0dB} defines how fast can the circuit react to changes at the output or input. Open loop parameters like phase margin also defines how the circuit behaves under step response inputs and such. But, the most important parameter is stability, which is defined by phase and gain margin. We are aiming at phase margin of at least 45° in the worst corner. In figure 5.11 we can see the same shifting of the dominant pole we talked about earlier, plus the shift of the the zeros and other poles due to the change of bias conditions. The most obvious deviation is when the load current is minimal (9 uA), then the dominant pole is at the lowest frequency.

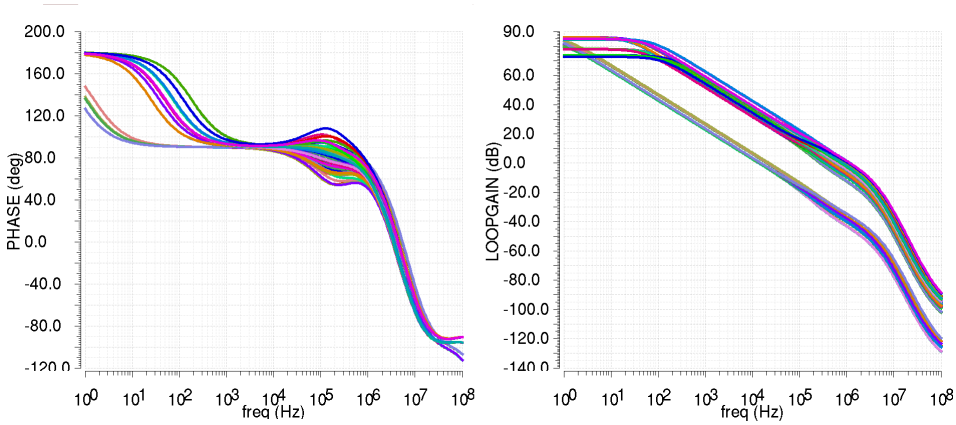

Figure 5.11: Open loop gain and phase over specified corners

We can see that the gain bandwidth f_{0dB} shifts a lot, it is therefore useful to plot its behavior. In figure 5.12 we can see that with load current, the f_{0db} rises and phase margin accordingly to it falls. We can see that the minimum phase margin is not at the maximum output current, but around 250 uA,

this needs to be taken into account later during the overall corner simulation.

Next important parameter from AC domain is Power Supply Ripple Rejection or PSR (shortly Power Supply Rejection). We know that it defines how well can the regulator suppress changing input voltage over wide frequency range. It is important to note, that in our design, the PSR at the very output of the LDO is affected by the RC filter, which is formed from the output capacitor and the resistance of the pad. It starts to filter high frequency supply signals just below the unity gain bandwidth. Normally, we would see drop in the magnitude of PSR around unity gain bandwidth, as it is in figure 5.13, but since the RC filter start to filter the signal, the unity gain bandwidth effect is compensated and the PSR is even better after that. Since the PSR was not the scope of this work, we can settle with the 50 dB value, which is satisfying.

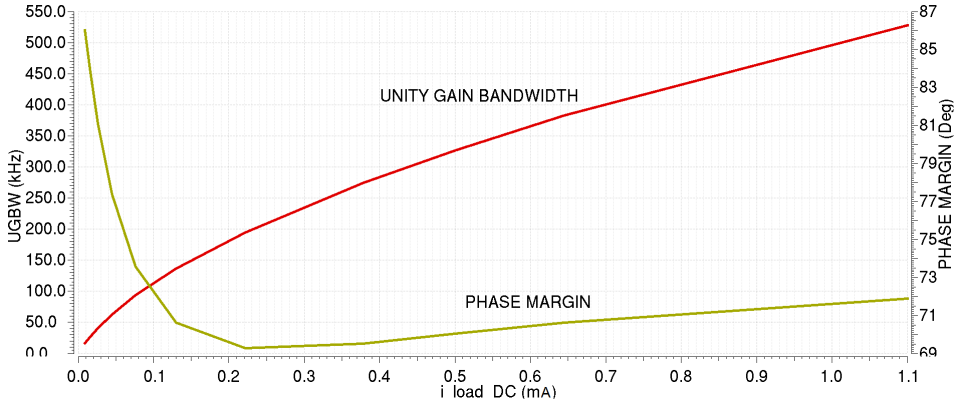

Figure 5.12: Unity gain bandwidth and Phase margin vs. load current

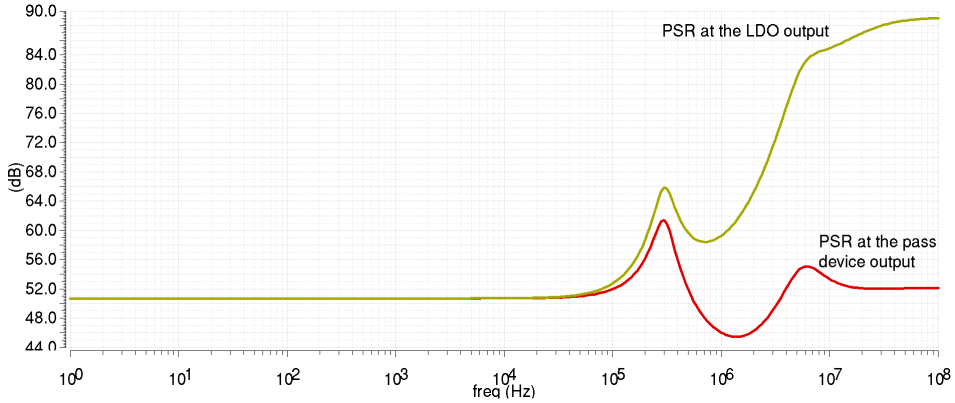

Figure 5.13: Power supply ripple rejection - PSR at the output of the LDO regulator and before the RC filter at the output

5.8 Transient Analysis

We simulated the open loop AC responses and DC response of the system which gave us satisfying results, they are mostly helpful approximations of the behavior of the circuit. Most important analysis is transient, because it test how the circuit behaves in real time with varying large signal transients. Two most important parameters of LDO regulator in transient domain are Load and Line Transient responses. If we simulated correctly and the circuit is stable, we should not see any oscillations or ringing during the step responses.

5.8.1 Load Transient

In figure 5.14 we can see the load transient response with frequency of 5 kHz so the signal has enough time to settle. Since the system has huge phase margin at low load current, the transition from maximum load current to minimum load current is slow, smooth and without any overshoots. On the other hand, the transition from minimum load current to maximum load current, where phase margin is around 70° is fast and with small overshoot,

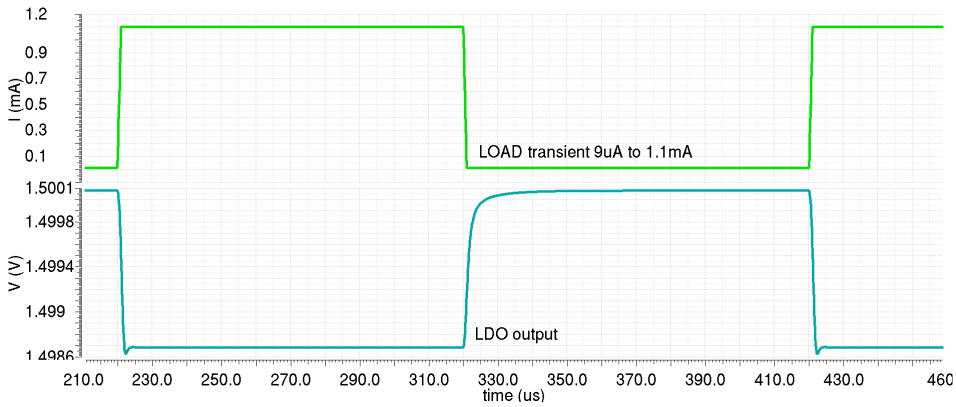

Figure 5.14: Load transient from 9uA to 1.1mA at low frequency of 5kHz

which is mainly caused by the ESR of the output capacitor. The larger the current step and ESR is, the larger the overshoot, because the capacitor is trying to source the current to the load, before the regulator starts to regulate and the ESR is in the way of the current from capacitor, so there is a voltage drop on it. Since ESR in our application is not very large and load current is also small, these overshoots tend to be in the range of milivolts, which is optimal.

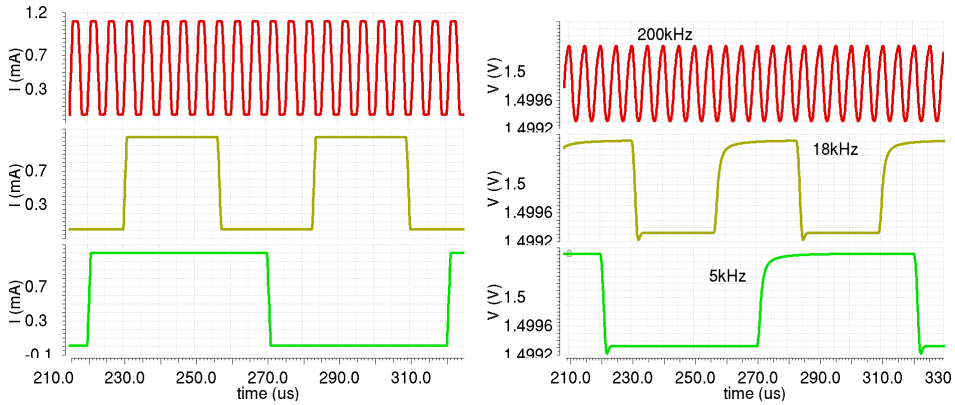

Figure 5.15: Load transient from 9uA to 1.1mA for 5kHz, 18.5kHz and 200kHz

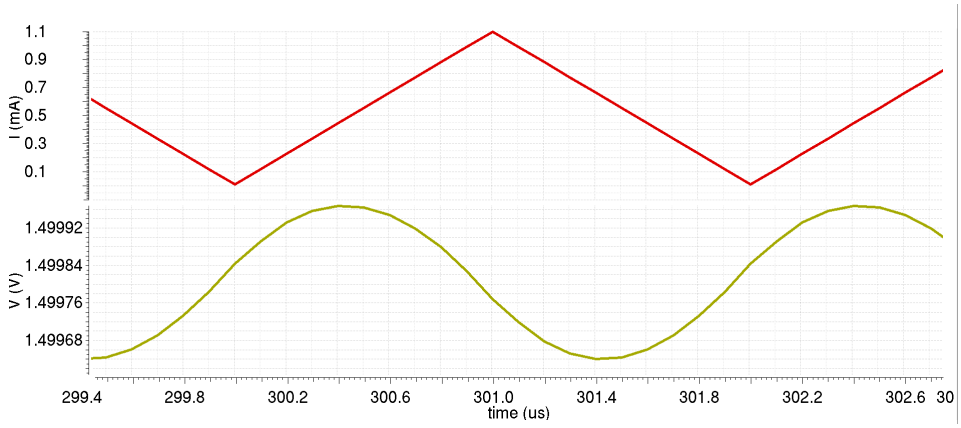

Figure 5.16: Load transient from 9uA to 1.1mA at 1MHz

We can see from figure 5.15 that with increasing frequency of the transient, the output does not really settle, because the gain of the system decrease and the system cannot respond to the changes of the output fast enough. When the frequency of the transient changes is above the bandwidth of the system, the regulator does not have time to react before just oscillates between high and low load states, but can actually never settle. This can be seen in figure 5.16.

5.8.2 Line Transient

The line transient behaves quite differently from the load transient. The difference between the steady state voltages of the line transient is much lower, because it corresponds with the power supply rejection and line regulation. Also, we can see, that the overshoots are in opposite directions to the overshoots of the load transient. And there is large difference between line transient for small and large load current. In figure 5.17 we can see the the response at maximum load current and in figure 5.18

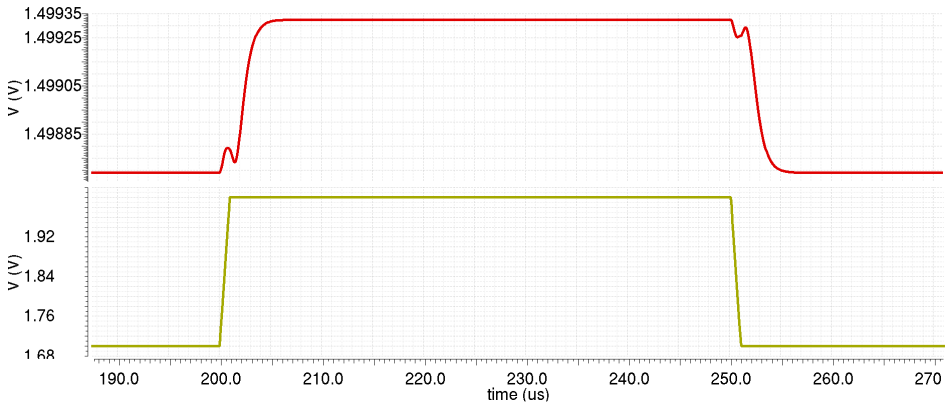

Figure 5.17: Line transient from 1.7v to 2V for load current of 1.1mA at 5kHz frequency

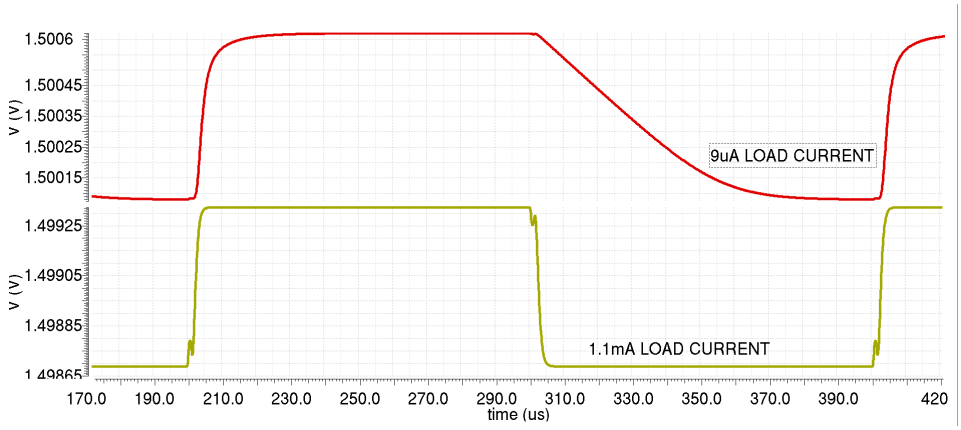

Figure 5.18: Line transient from 1.7v to 2V for load current of 1.1mA and 9uA at 5kHz frequency

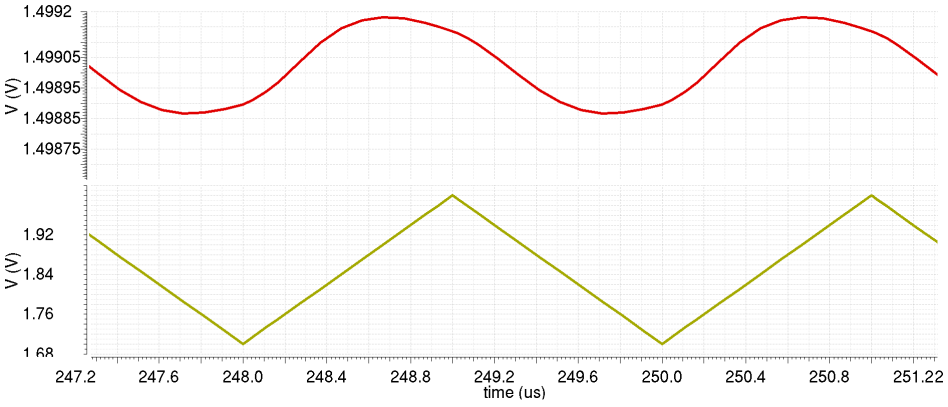

Figure 5.19: Line transient from 1.7 V to 2 V for load current of 1.1 mA at 1 MHz frequency

we can see the comparison with small load current. Clearly when the

voltage rises, the response is fast, because the capacitor is charged by the current from the supply, but when the voltage drops, the output capacitor holds its value for quite a long time, because it is discharged only by a small load current of about 15 uA.

Line transient at higher frequencies that bandwidth of the system has similar effect as in the case of high frequency load transient, the out can react properly to the fast changing input and just oscillate in between normal steady states. This can be seen in figure 5.19.

5.8.3 Power Supply Ripple Rejection

Measuring the PSR is quite straightforward in transient domain. We will superimpose a transient ripple signal on the V_{IN} supply line and the ratio of the output ripple to the input ripple should give us roughly the same PSR that we received from AC analysis. In figure

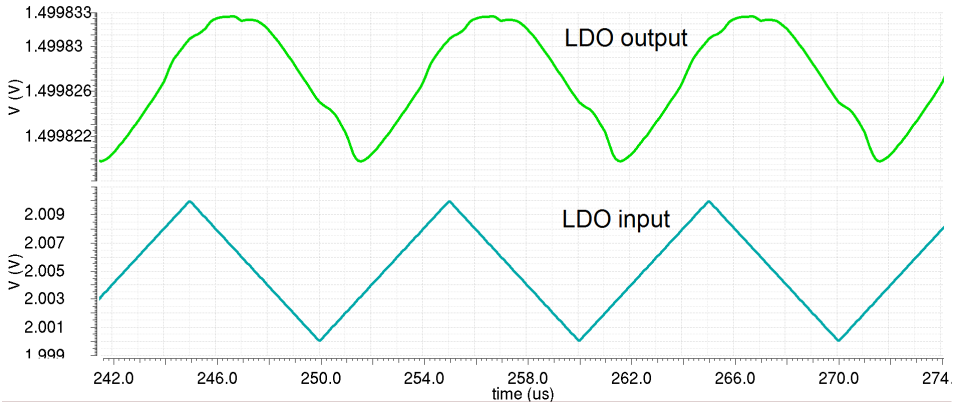

Figure 5.20: Transient response to power supply ripple of 10 mV

5.20 we can see the output versus input voltage, when 10 mV ripple is superimposed to the supply line. The output changes in the range of microvolts and the total PSR given by the total change of the input voltage to the total change of the output voltage

$$PSR = \frac{\Delta v_{in}}{\Delta v_{out}} \tag{5.13}$$

which gives us about 50 dB PSR depending on the frequency and the simulation corner, which are going to be analysed later in this chapter.

5.9 Corner Analysis

The last step in verification of the circuit is so called corner analysis. The process parameters like, oxide thickness, carrier mobility, width and length of the gate vary and different dies are fabricated with different absolute parameters. Especially passive components like resistors and capacitors may

differ up to 20% in absolute value, but ratio of resistor to resistor is much more precise in the same die, the error is about 0.1%. These changes in the absolute resistance will affect the quiescent current and the position of the compensation zeros. By specification, we have to take into account corners in table 5.3.

corner parameter	range
input voltage (V_{in})	1.7 V to 2 V
load current (I_{load})	9 uA to 1.1 mA
bias current (I_{bias})	80 nA to 120 nA
temperature (Temp)	$-50°C$ to $100°C$
output capacitor value (C_{out})	0.8 uF to 1.2 uF
output capacitor ESR (R_{ESR})	0.01 Ω to 0.3 Ω
pad resistance (R_{pad})	0.2 Ω to 0.5 Ω
combination of 9 process corners XXX (NMOS-PMOS-RESISTOR)	

Table 5.3: Parameter corners and their ranges

We can to some extent predict the behavior of some parameters in different corners, but for example phase and gain margin are hard to predict, so this simulation is vital to verify, that the circuit is stable under all conditions. If we analyze corner analysis table, we can see that the parameters behave as we predicted earlier. Quiescent current is largest for fast resistor corner, where the total resistance of the feedback divider is smallest. Unity gain bandwidth is low when the load current is low. To an extent we can predict the behavior, but without analyzing all corners, we cannot be sure, that for example some transistor does not fall out of saturation region at some process corner.

Corner Analysis										
parameter	Nom.	WC	Proc.	V_{in}	I_{load}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
$V_{out,min}$ [V]	1.499	1.498	SSF	min	max	max	max	min	min	max
$V_{out,max}$ [V]	1.499	1.502	FFS	max	min	min	max	min	min	min
$V_{drop,max}$ [mV]	15.6	89.64	SSF	-	max	max	min	min	min	min
I_q [uA]	4.62	6.43	FFF	max	max	max	max	min	min	min
$M10_{hdr}$ [mV]	355.5m	106.6	SSF	min	max	min	min	min	min	min
DC gain [dB]	76.1	67	SSF	min	max	max	min	max	max	max
UGBW [MHz]	0.571	0.012	SFS	max	min	min	max	max	min	min
PM [deg.]	65.1	48.6	SSF	max	max	min	min	min	min	min
GM [dB]	21.39	13.54	FSS	max	max	max	max	min	max	max
$PSR_{UGBW/10}$ [dB]	54.2	43.21	SSF	min	max	max	min	min	min	min
PSR_{UGBW} [dB]	57.8	51.08	FFS	min	max	min	min	min	max	min
$PSR_{UGBW*10}$ [dB]	82	57.9	FFS	min	max	max	min	min	max	max

Table 5.4: Corner analysis for process, parameters and temperature corners od DC and AC parameters

Transient analysis parameter corners were measured for low frequency

signal of 5 kHz, so that the output has enough time to settle, so we can properly measure the transient load and line responses. It is assumed, that the output will not be changing frequently, but between minimum and maximum values, especially load current.

Line transient corners								
Settling time for high to low line transient								
Nom.	WC	Proc.	I_{load}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
3.7 us	78.91 us	SFS	min	min	max	max	min	max
Settling time for low to high line transient								
Nom.	WC	Proc.	I_{load}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
3.7 us	33.1 us	FFS	min	min	max	max	max	max
Percent overshoot for high to low line transient								
Nom.	WC	Proc.	I_{load}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
0	12.7%	SFF	220 uA	min	min	min	min	min
Percent overshoot for low to high line transient								
Nom.	WC	Proc.	I_{load}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
0	6.25%	FFS	220 uA	min	min	min	min	min

Table 5.5: Corner analysis for process, parameters and temperature corners for line transient analysis

Load transient corners								
Settling time for high to low load transient								
Nom.	WC	Proc.	V_{in}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
2.6 us	16.2 us	FFS	max	max	max	max	max	max
Settling time for low to high load transient								
Nom.	WC	Proc.	V_{in}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
2.5 us	5.5 us	FSS	min	max	max	max	max	max
Percent overshoot for high to low load transient								
Nom.	WC	Proc.	V_{in}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
0	1.3%	SFF	max	min	min	min	min	min
Percent overshoot for low to high load transient								
Nom.	WC	Proc.	V_{in}	I_{bias}	Temp	C_{out}	R_{ESR}	R_{pad}
6.7 %	36.6%	SFS	max	min	min	min	min	min

Table 5.6: Corner analysis for process, parameters and temperature corners for load transient analysis

Chapter 6

Conclusion

In this work, design of an LDO regulator in GPDK180 technology, to meet specified parameters, is presented. There were several parameters that were taken into account during the design, but the main focus was on the quiescent current, which was specified to be under 10 uA. Firstly, we discussed the typical parameters of the LDO regulators, how are they interpreted and how to measure them. After that the GPDK180 technology parameters were analyzed, to obtain better understanding of how the devices we used behave under different conditions. In chapter 4 we reviewed general design of various LDO regulators, different topologies and their pros and cons. The most important task in designing LDO voltage regulator is maintaining stability under all load conditions. The means by which this is achieved are also contained in chapter 4. In chapter 5.5 we dealt with the design of the LDO regulator. From the load current and dropout voltage a PMOS pass device has been chosen as the best option for our application. Since the pass device is a high capacity load, an operational transconductance amplifier was utilized as the error amplifier. Symmetrical OTA topology has been chosen for its wide output swing, because the voltage at its output will be varying significantly with changing load conditions.

Parameter	Specification	Nominal results
$I_{load,max}$	$<$ 1.1 mA	1.1 mA
I_q	$<$ 10 uA	4.62 uA
V_{out}	1.5 V	1.499 V
V_{drop}	<0.2 V	15.6 mV
UGBW	-	571 kHz
PM	$>$ 45° at WC	48.6° at WC
GM	-	13.54 at WC
PSR_{DC}	-	54.2 dB
$PSR_{1\ MHz}$	-	62.5 dB
Area on chip	-	2730 um^2
Efficiency	-	82%

Table 6.1: Comparison of specified and accomplished parameters

The circuit was stabilized with PMOS source follower buffer amplifier and by utilizing phase saving zeros. Parameters of the designed LDO voltage regulators were measured using Spectre simulator in Cadence design environment. From table 6.1 it is clear that the specifications have been met. Designed LDO regulator is stable under all process and parameter corners, which is essential. The small output current is offset with small quiescent current and very low dropout voltage. The efficiency depends on the input voltage and ranges from 75% to 88% depending on the input voltage.

The final design meets the specification but there is wide room for improvement. Biasing techniques in respect to load current could be implemented to achieve stability at larger output currents while keeping the efficiency of the circuit relatively constant. For PSR enhancement, various feed-forward techniques to cancel-out the power supply noise more efficiently could be exploited in the future work.

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Appendices

Appendix A

Cadence Schematics

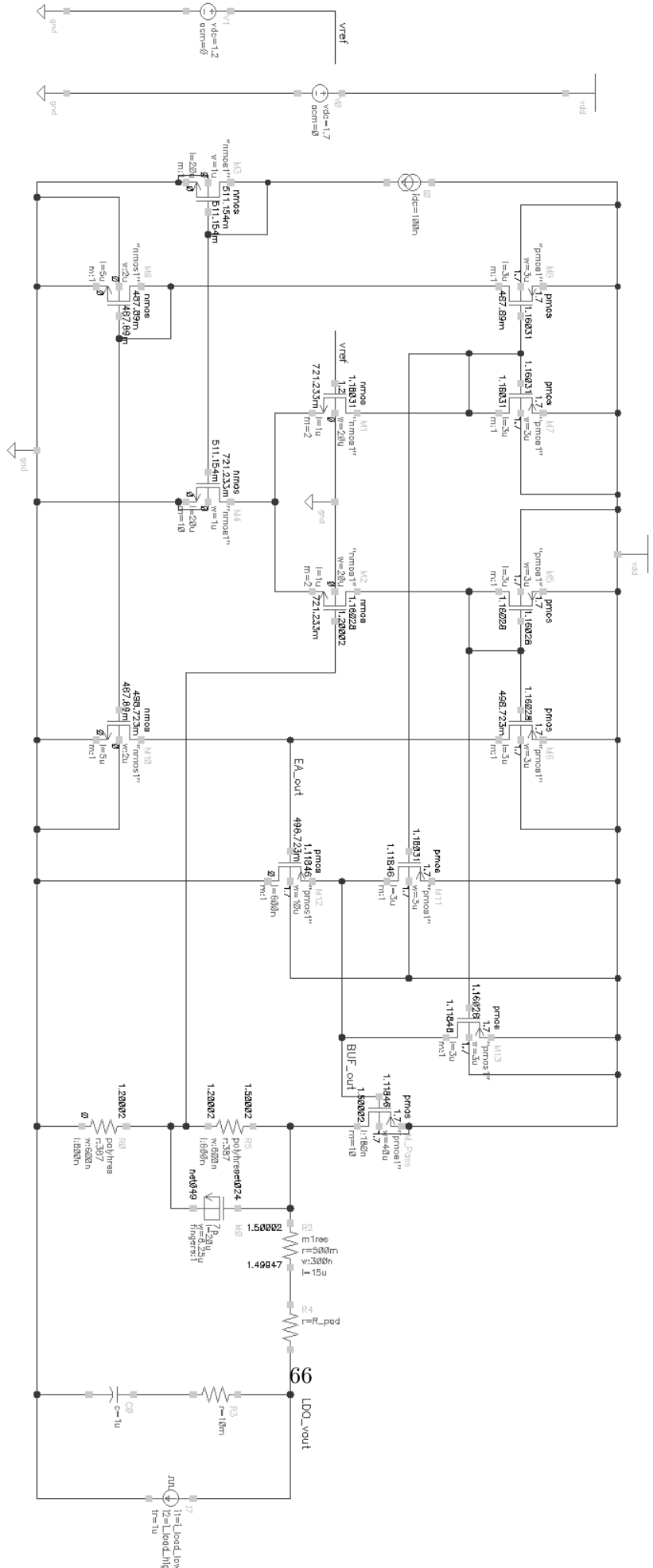

Figure A.1: Schematic from Cadence simulator