This thesis presents a complete hardware and software design of an embedded computer vision module based on FPGA that combines FAST feature extraction with BRIEF/GRIEF descriptor and is capable of real-time mobile robot navigation. Moreover, the student presents a framework for FPGA embedded implementation of feature-based image processing algorithms.

The results show that embedded implementation of FAST and BRIEF/GRIEF is accurate compared to their CPU counterparts, while processing the complete image on the fly as it is captured. In my opinion, this is thanks to an elegant tailored architecture and careful implementation, but also to a smart selection of a detector and a descriptor that can accomplish robot navigation and are also very well suited for FPGA implementation (highly parallelizable and all integer arithmetics, for example). In this sense, although the high level modules presented in the general framework are the stages present in most (if not all) feature-based algorithms, in my opinion the challenge is in developing parallel architectures to achieve real time performance, specially on-the-fly implementations that adapt to the proposed framework.

As a technological note, the proposed solution utilizes a FPGA development board together with an ARM Cortex M3 microcontroller board developed by the author, for a total price of usd 118 (with academic license). I would suggest to look into the ZyBo board, that presents a Zynq chip including in a single chip the FPGA together with a dual core ARM A9 processor, for 125 usd (academic price). The A9 processor has native SIMD floating point instructions, that could simplify the real time implementation of more complex descriptors like SURF.

In all, the thesis is well presented and clear, and shows an elegant FPGA architecture and complete embedded module that achieves the proposed goal: an image processing embedded module capable of mobile robot navigation. Hence, I propose the thesis to be graded

A - Excellent.

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