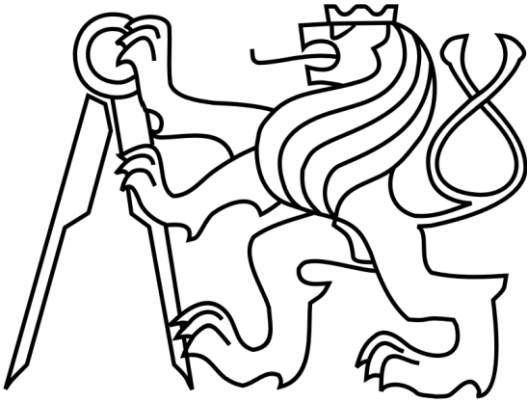
Czech Technical University in Prague

FACULTY OF ELECTRICAL ENGINEERING

Department of Electrotechnology



MASTER'S THESIS

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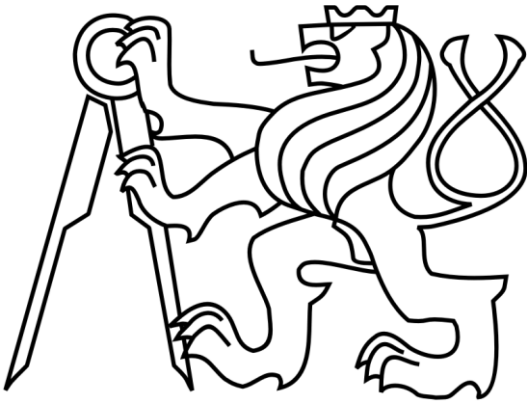

MASTER'S THESIS

Quantify quality parameters during conformal coating process of printed circuit board

Kvantifikace kvalitativních parametrů v procesu lakování desek plošných spojů

Student: Jan Umlauf

Academical year: 2014/2015

České vysoké učení technické v Praze
Fakulta elektrotechnická

katedra elektroenergetiky

ZADÁNÍ DIPLOMOVÉ PRÁCE

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Studijní program: Elektrotechnika, energetika a management
Obor: Elektroenergetika

Název tématu: **Kvantifikace kvalitativních parametrů v procesu lakování desek plošných spojů**

Pokyny pro vypracování:

1) Seznamte se s kontaminací a technologií lakování desek plošných spojů.
2) Na vybraných vzorcích proveďte posouzení kontaminace desek plošných spojů a posuďte kvalitu laku.
3) Výsledky posouzení porovnejte a vyhodnoťte.

Seznam odborné literatury:

[1] IPC normy
[2] ABEL M., CIMBUREK V.: Bezolovnaté pájení v legislativě i praxi, ABE.TEC, Pardubice 2005, ISBN 80-903597-0-1
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[4] HWANG J. S.: Modern Solder Technology for Competitive Electronics Manufacturing

Vedoucí: Ing. Karel Dušek, Ph.D.

Platnost zadání: do konce letního semestru 2015/2016

L.S.

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děkan

V Praze dne 1. 4. 2015

Declaration

I hereby declare that I wrote presented Master's thesis by myself and I stated every used information resource in accordance with Methodical instruction about abidance of ethical principles applied during creation of university's works.

Prohlášení

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských prací.

V Praze dne

With special thanks,

The greatest merit on this thesis has my leader and mentor Ing. Pavel Hanzlík, who lead my through, gave advices and improved me as a professional and human. I would like to thank to the head of the thesis Ing. Karel Dušek Ph.D. who aided me in enormous way. I was able to finish my work. There was also a lot of help from my colleagues, who listened, opposed and provided their support at time of need.

Content:

Abstract:

Main objective of this thesis is quality assurance of conformal coating process. Proper quality parameters and characteristics are evaluated and quantified. Quantification exactly and objectively reflects reality and allows us to improve processes. Conformal coating is mentioned only partly. Thesis is focused on incoming goods. Contamination of printed circuit boards is main interest. Effects caused by contamination and reduction of contamination are suggested in conclusion.

Abstrakt:

Hlavním cílem této práce je zajištění kvality lakovacího procesu. K tomu je potřeba najít a zvolit optimální kvalitativní parametry, jejichž vyčíslení nejpřesněji a nejobjektivněji vyjadřuje zkoumanou skutečnost. Samotný proces lakování je probírán spíše okrajově, hlavním bodem zájmu je vstupní materiál. Zvláštním předmětem zájmu je kontaminace desek plošných spojů. V závěru je shrnut vliv na lakování a možnosti snížení kontaminace.

Key words:

Conformal coating, quality, printed circuit boards, contamination, ionic contamination

Klíčová slova:

Lakovací proces, kvalita, desky plošných spojů, kontaminace, iontová kontaminace

Introduction:

Conformal coating is used as protection to chosen base. In this work, printed circuit board is being coated. Importance is given to the dielectric quality and protection against moistening.

Characteristics before application are crucial. Viscosity allows us to properly apply the lacquer. While it's surface tension is important when it has to form a bond with board. When drying time would be too long, coating could not be used in production due to time and resources spend in oven. Bonding on the basic level and ability to not create transitions is relevant for double coating or reparations.

Parameters of the produced printed circuit board are eighty percent of success. It is the top priority to inspect the boards prior to lacquer. While changing coating is easier than improving the process, the processes are keys to success. Ionic contamination of the board is inspected through the production. Flux and resin residues are partly link to the ionic contamination as it reflects cleanliness, but residues have to be inspected independently. Flux residues attract humidity and can eventually lead to delamination.

How to coat the board is skill requiring experience. Lines taken in order to bring good results, smoothness and economy of the programing of the conformal coating line, cleanliness and handling precautions are learned through the quantification process. Thickness is optimized. Uniformity, equability and adhesion are evaluated and compared to the norms.

Quantification of quality parameters has simple meaning. On many occasions, more pictures, studies, tables and models are used instead of words. Numbers are quality performance meters. There are paragraphs and topics in this thesis, but it can be sorted into three: quality of the printed circuit board in production, quality of the coating and coating process as an interaction between those two.

"Measurement is the first step that leads to control and eventually to improvement. If you can't measure something, you can't understand it. If you can't understand it, you can't control it. If you can't control it, you can't improve it."

Dr. Harrington, H. James. CIO (Sep 1999), p. 19.

List of standards and description:

Proper set of test methods must be chosen in order to objectively evaluate the process. Introduction into standards helps with basic orientation.

IPC J-STD-001. chapter 8: Requirements for Soldered Electrical and Electronic Assemblies

This document describes methods for electronic assembly manufacturing and processing soldering materials. Criteria for materials, verification methods for solder joints and assemblies.

IPC-A-610. 10.4: Acceptability of Electronic Assemblies

This norm helps quality assurance to choose whatever part can be used or not. Pictures, microsections and guidance is provided to make a right decision.

IPC-TM-650. Environmental test methods

Norm provides specification of environmental test methods. Lot of information is taken from this standard.

IPC-TM-650. 2.3.25 Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract

This method should be highlighted as half of thesis relies on it. Although IPC specifies 1,56 μg NaCl Eq./cm^2, those requirements are much higher in industry.

IPC TP 1113. Circuit Board Ionic Cleanliness Measurement

Manual describes methods and limitations of the ionic contamination measurement and influences of various flux types.

IEC – 68-2

Those are methods for climatic reliability testing of electronic assemblies. IEC 60068 determines suitability of components, assemblies and other parts in usage transportation and storage under different climatic conditions.

IPC-HdbK-830. Guidelines for Design, Selection and Application of Conformal Coatings

This handbook provides assistance to make choice regarding conformal coating. What can be achieved by conformal coating application and how to verify the results.

PCB's contamination experiments:

Review of

IPC-TM-650. 2.1.1.2 Microsectioning—Semi or Automatic Technique Microsection Equipment

This method specifies procedure for metallographic specimen preparation through microsectioning. Process's goal is exact evaluation of laminates, copper foils, plating and mainly coating. This process is actually often applied as a solution for unclear cases concerning electronics or mechanical issues.

More than often the safety procedures have to be followed. Either from the point of view of material and environment (refer to Material Safety Data Sheet = MSDS) or from the point of view of assembly itself, where it's disassembly might be dangerous.

Used apparatus contain grinder, sample alignment tools, mount molds, marble plate for correct mounting, pressure system capable to store the coupon at around 2 bars, potting material, air extraction area during curing time, polishing equipment, abrasive paper an polishing cloths, diamond abrasive, polishing lubricant, micro etch solution and microscope.

It is important to follow recommended steps in order to create the good microsection sample or coupon. Then the quality is going to be kept and evaluation of the sample is going to bring the results.

The key in this process is initial selection. More often the product or assembly is very big and therefore selecting the proper position to microsection and also the correct plane might be the hardest decision that can either lead to results or prolong the evaluation. When the place is chosen, then the correct cut-off method (Picture T1) must be made. Abrasion by grinder or directly by blades has to be done sensitively in order to not damage the evaluated area that would change the result and decisions. According the IPC the edge should be around 2 mm from the evaluated areas. From the experience, 3 or 4 mm is suitable even for coating analysis.

PCB's contamination experiments:

After the sample is taken, it is necessary to polish the edges by abrasive paper to prevent the burrs. Inspection of sample afterwards is required. If sample is damaged, it is required to take new one. It is necessary to solder the sample in order to properly inspect plated-through holes. Correct approach is first applying the flux and let it be activated, then placing it into the lead-free solder bath (Picture 2) for 10 +1/-0 s @ 288 °C. European Union suggests several alloys that conform with RoHS standard (Restriction of Hazardous Substances) Sn96,5Ag3,5. For solder paste there is often 0,75 of Cu at the expense of Sn. This provides thermal shock and evaluation of solder wettability.

Note: Mostly the solder shock evaluation was not used, because of it's damage to the inspected coating. Nevertheless it is important to note this step.

Correct mounting of the sample is important in reducing the process time. Alignment tool must correctly attach the sample but it is not allowed to damage the sample. Marble surface is also a great help in this (sometimes) endeavor.

Note: Project to find suitable potting material was initiated, because the standard epoxy was not usable for the microsection analysis as it corrupted the coating (Picture T6). After that no thickness measurement was possible or meaningful. Possible solutions for this problem were found. See the dedicated project after this section.

According the IPC potting material must have a low shrink rate, and the cure temperature must be less than 93 °C. Potting material is in most cases composed of two elements, it is important to mixing them in right rate and carefully.

Plastic or rubber container for potting material with sample is suggested. If the material is not very plastic, release agent should be used. Hardening process is fast, lot of heat is produced and voids can be present in the microsection. Pressure pot is desired to prevent voids occurrence. Pressure around 2 bars is enough, when increased temperature would be used, than for 50 °C, it is around 1,75 bars. This is for safety (because the pot has some limits) and can

be calculated to match the exact environment according the equation of state, where only pressure and temperature are variables. Increased temperature is used for rapid hardening, general oven is recommended. Air extraction system is important for personal safety.

Creating a flexible traceability system is desirable. Permanently mark the specimen after curing is finished. Good specimen is without voids in whole volume, without gaps between the material and sample and PTHs are completely filled. It has to be solid in order to be grinded and polished. Picture T4 shows such grinding and polishing machine with chemistry

Grinding of the sample has in general three steps. Abrasive paper increases the grit size through the process (P180, P400 and P1000). Revolutions per minute around 200, water cooled and residues separation are key parameters. IPC also suggests pressure for automatically prepared specimens. With abrasive grit size change, it is key to also rotate the sample by 90 °. Careful manipulation (to not scratch the surface) is important for the final products.

Specimen has PTHs, evaluated part, SMD component etc. in the center. It is upright unless specified otherwise. Scratches has size same as abrasive grit size paper. No residues are present on the sample. Surface is planar and therefore polishing is going to be easy, otherwise whole sample is not going to touch the polishing cloth.

Two or three steps of polishing with napless and nap type of cloth deliver good results. Revolutions can be kept or decreased. It highly depends on the type of the polish abrasive. Cleaning between steps should not be overlooked. There is no water present during the polishing to clean it. Same quality characteristics apply after polishing.

Microetch solution and cleaning are last steps when copper is being evaluated. It allows visual inspection of the copper. It is important to distinct the plated and galvanized copper.

PCB’s contamination experiments:

Picture T1: Edging saw

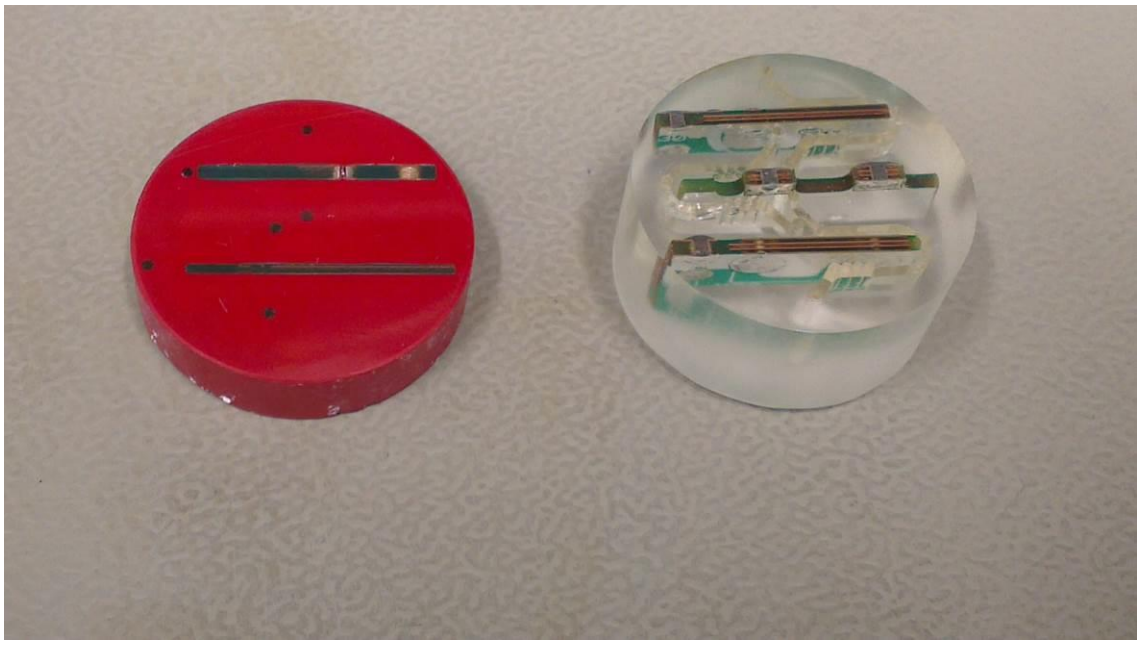
Picture T2: Solder bath

PCB's contamination experiments:

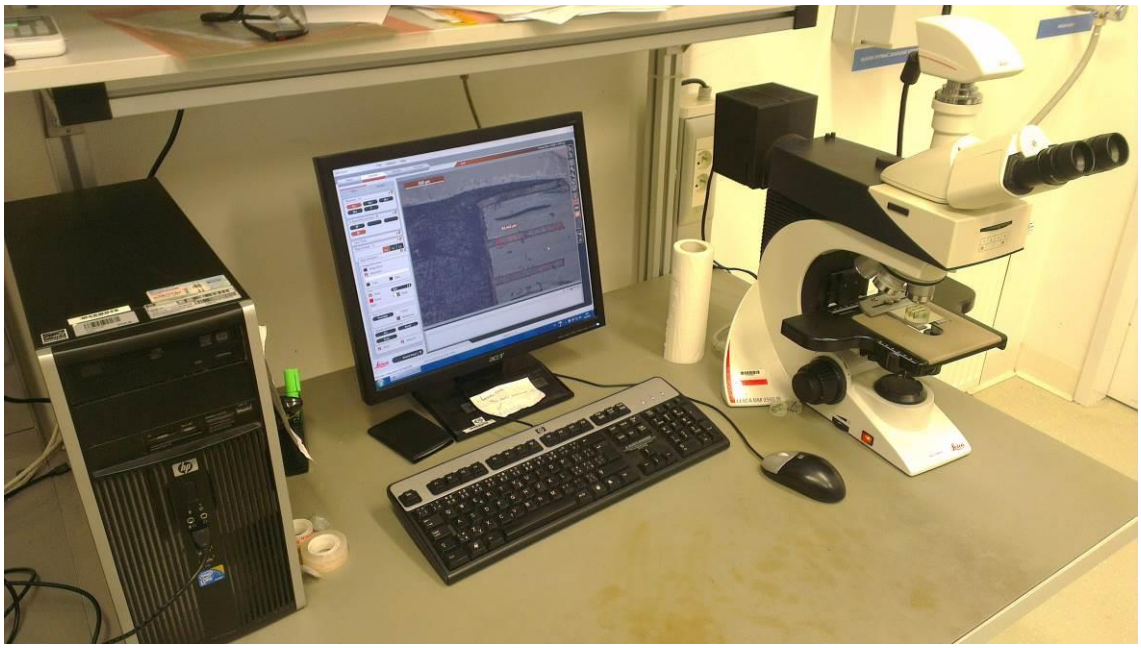
Picture T3: Extraction system necessary during curing time

Picture T4: Grinder and polisher

PCB's contamination experiments:



Picture T5: Microsection coupons, different epoxy is necessary is used



Picture T6: Evaluation station, Microscope is required, Leica 500x

PCB's contamination experiments:

Overall project to find suitable filler for microsections

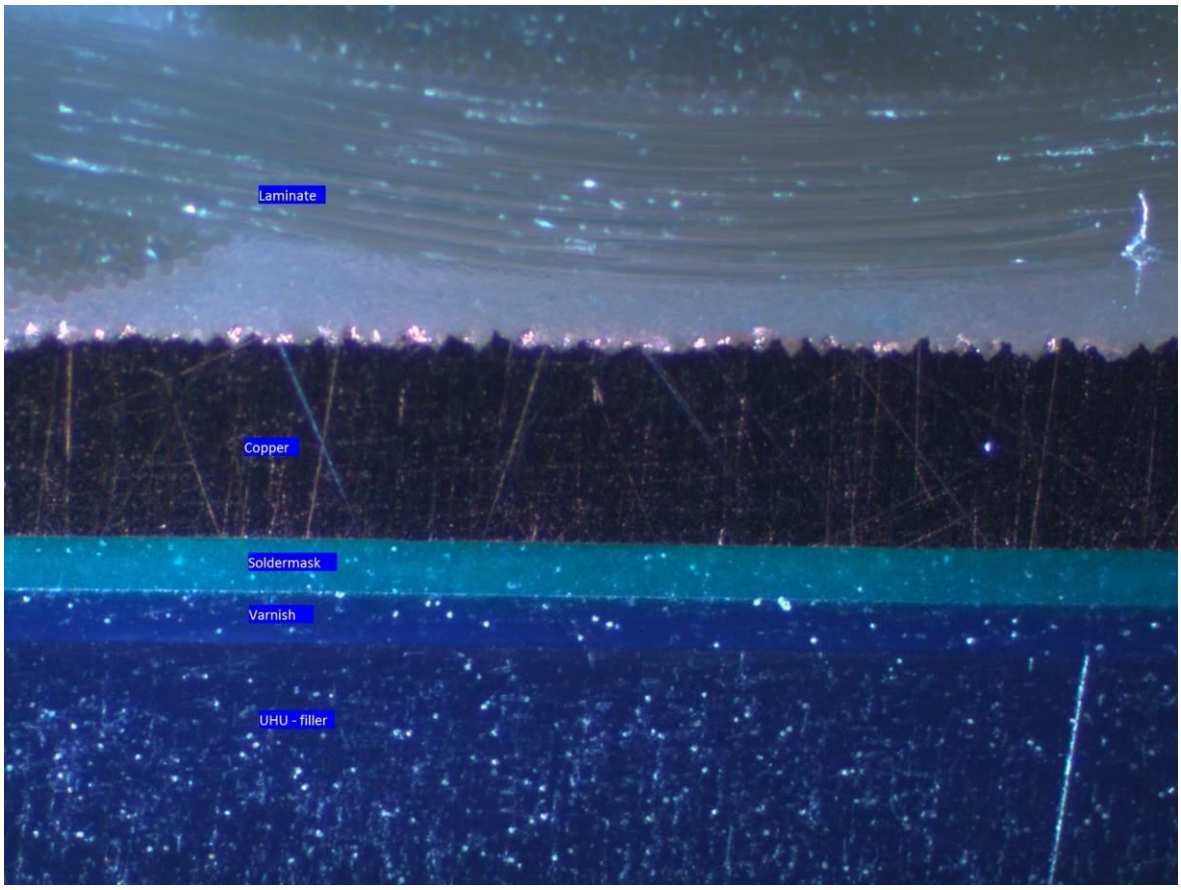
Varnish was corrupted by our standard epoxy. After that no thickness measurement was possible or meaningful. Possible solutions for this problem were found.

Adhesive/filler:

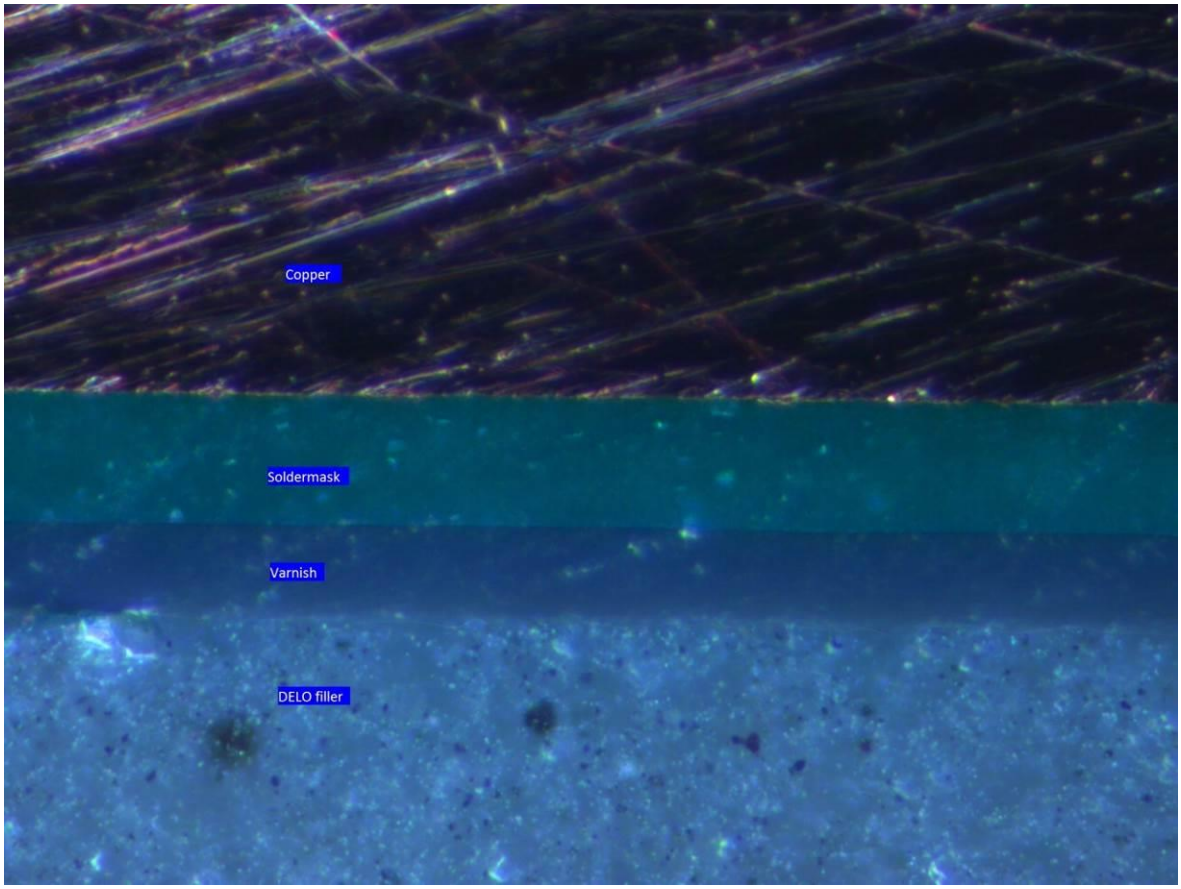
Using other types of adhesive, such as UHU or DELO
DELO has very long solidify period (around 6-8 hours) and on light it has very little contrast against varnish. On the other hand it has no negative influence on varnish. Using UV light this filler has best contrast between varnish and filler. Chosen way is using double component adhesive UHU. Hardening process takes about 20 minutes under increased temperature in oven (90 °C). Other possible way is using water based coating. Tested BALAKRYL UNI white. It creates protective layer that also serves as contrast film. Epoxy filler is possible. This time it damages paint and not varnish. UHU adhesive is still better choice.

Coating can serve as contrast film, that has no impact on varnish or filler. S6005 based paint damaged varnish. Same issue was with paint in spray.

PCB’s contamination experiments:

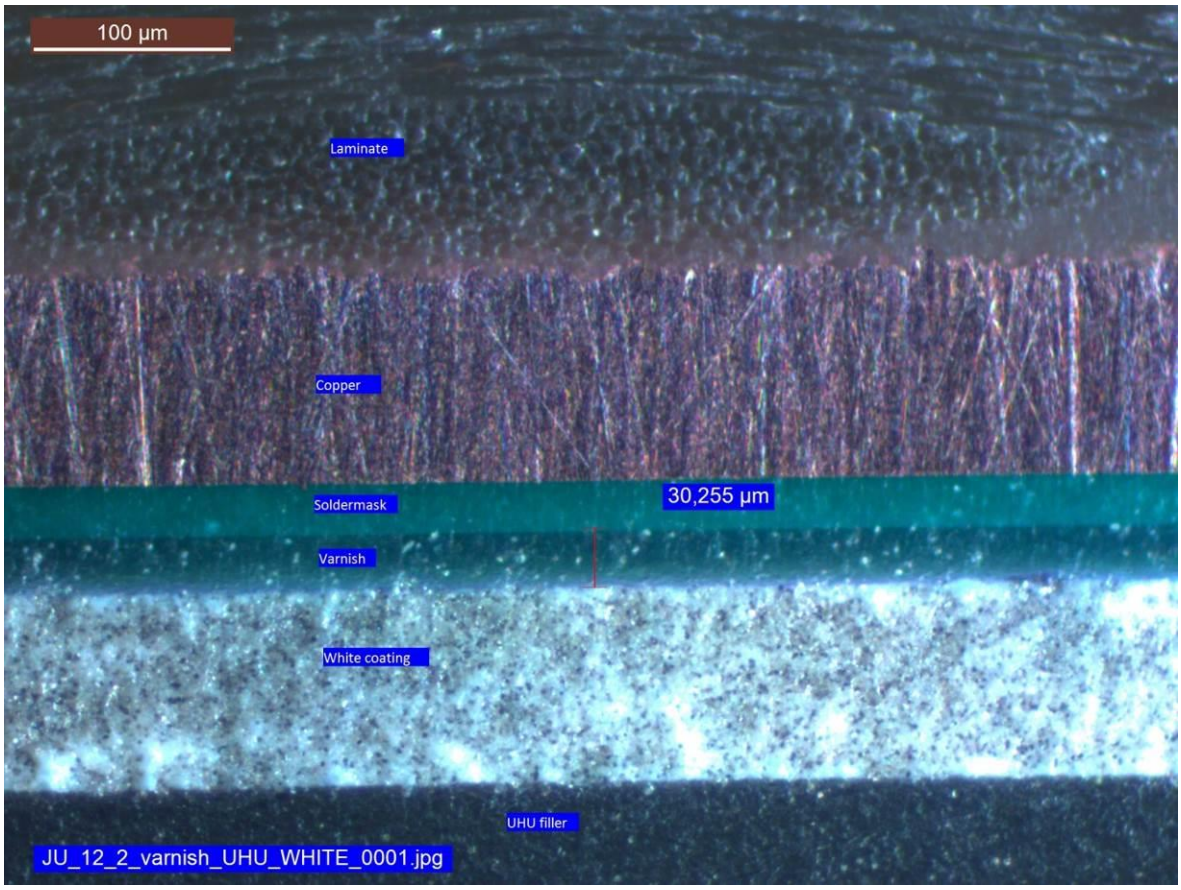


Picture T7: Microsection sample

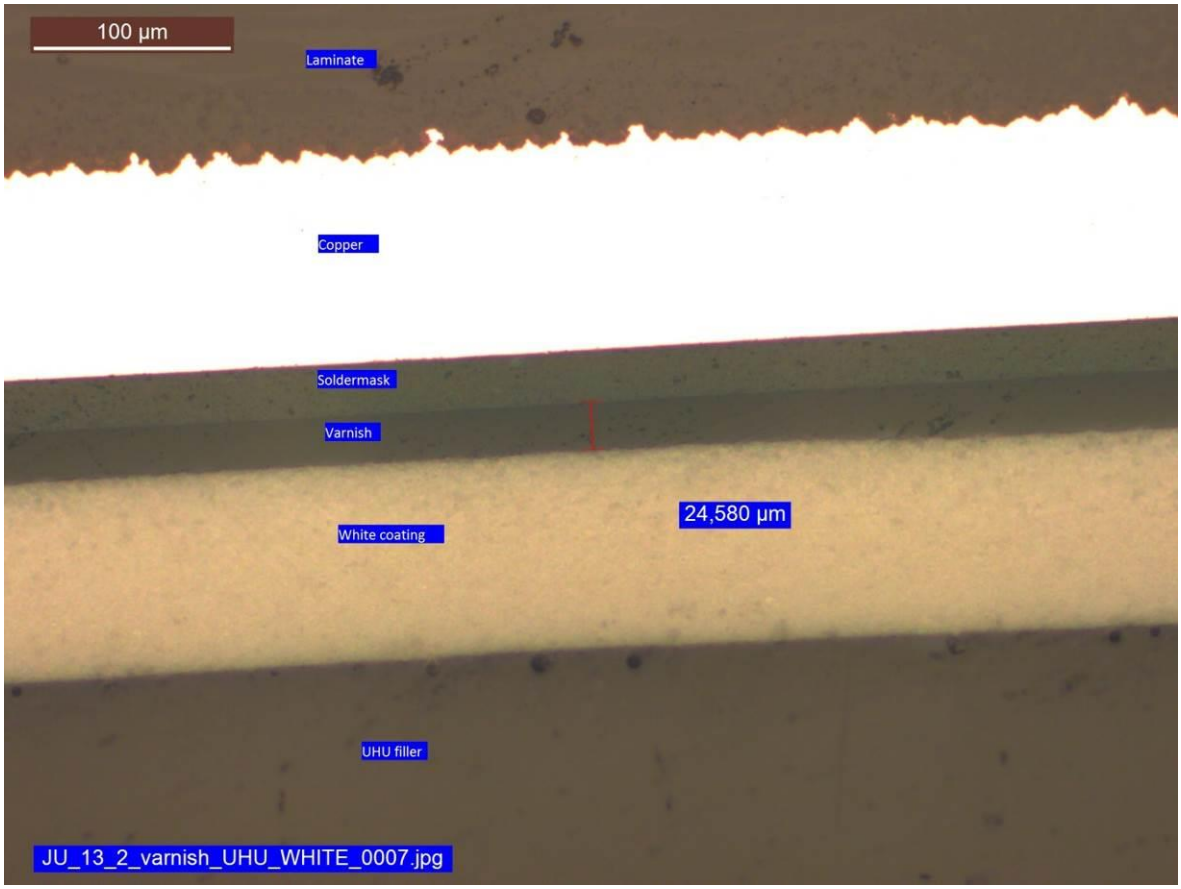


Picture T8: Microsection sample

PCB's contamination experiments:



Picture T9: Microsection sample



Picture T10: Microsection sample

Results:

Based on microsections, UHU torns varnish apart from solder/soldermask. It is not clear if it is caused by intense stress. Only on certain areas this has happened. Those could have been already damaged or at least weakened.

On our test PCBs everything was fine. Layer was new but dried and also three times thicker.

This issue requires deeper test. Another and better fillers should be studied. Or temperture could be decreased. But this would make process slower and leakage worse.

In the end for the future project the standard industry potting material (red colored) was used. Chemical unreactivity, good contrast, leakage and time consumption are more or less solved. It looks like it will be necesseary to let the microsection solidify longer in order to achieve microsection without any damage caused by our test process. Issue concerning higher adhesion between varnish and filler to varnish and soldermask, which tears varnish off. Goal is to deliver best possible and accurate results.

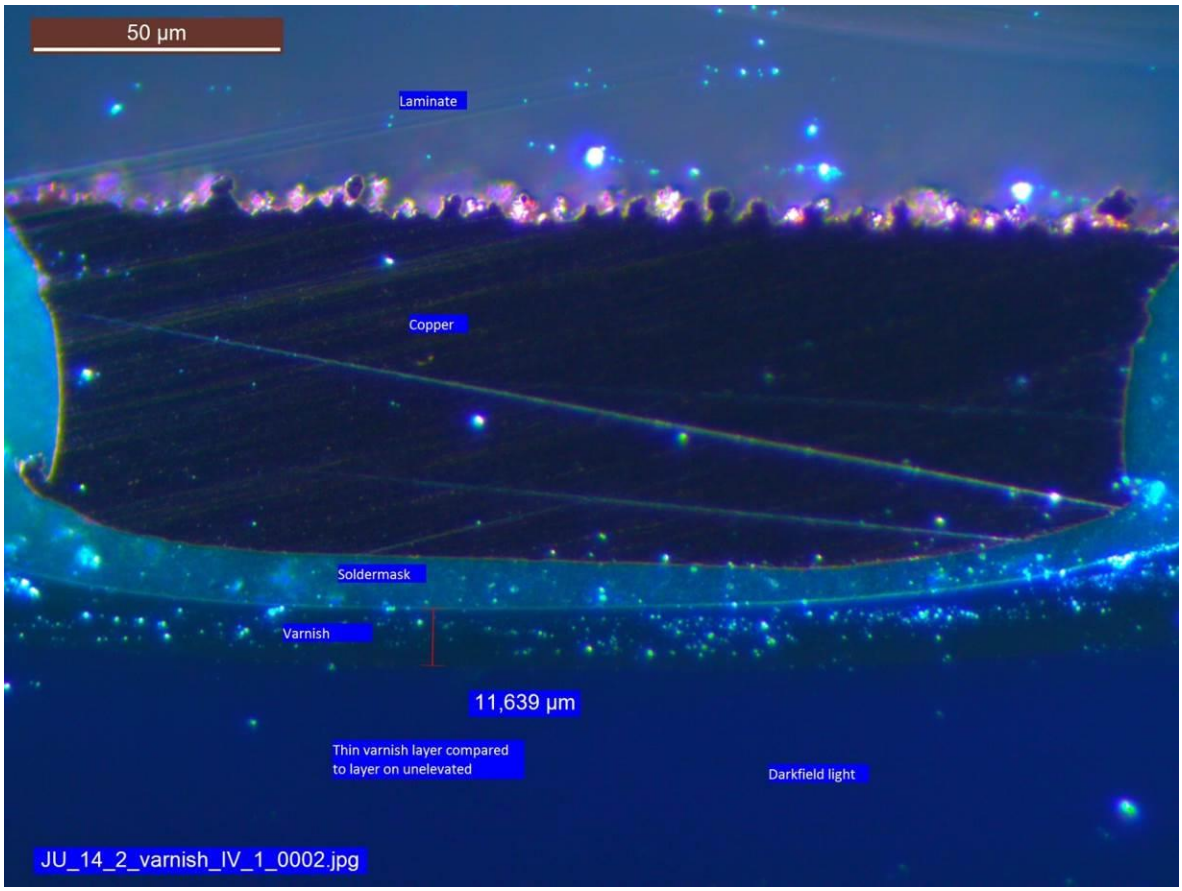
Light:

Different types of microsection's and PCBA's lightning were used. UV – ultraviolet for increasing contrast between varnish and filler or soldermask. In microscope it is not always clear if darkfield lightning (DF) is prefered to brightfield lightning (BF). Different situations require different approches.

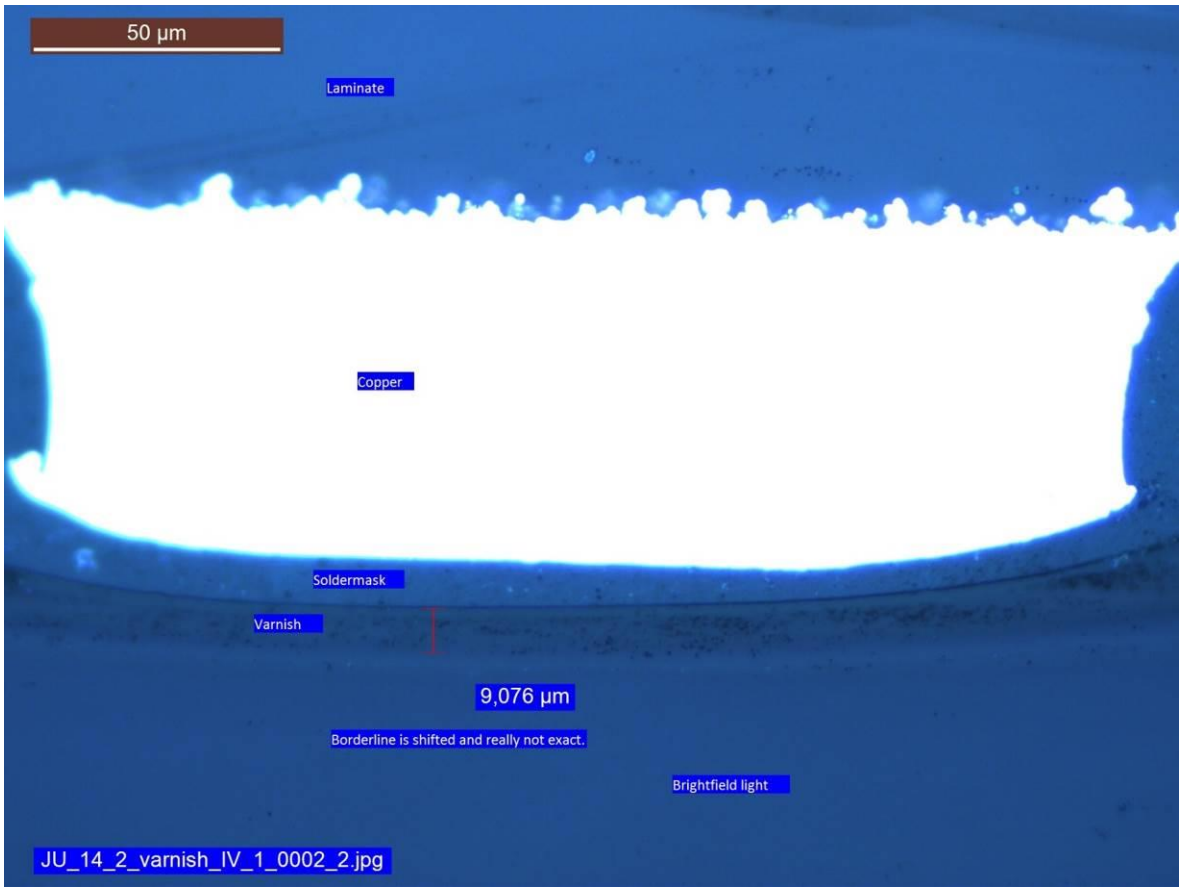
Results: In the majority of cases DF is used. Higher contrast is what is neccesseary for thickness measurement and good orientation in microsection. Sometimes BF was good as second picture for clear and full view on given situation.

Also for best results BF is very sensitive fine tuning. Eg. Gamma correction, saturation, exposure, atc.

PCB's contamination experiments:



Picture T11: Microsection sample, Darkfield light



Picture T12: Microsection sample, Brightfield light

SMT line theory

SMT stands for surface-mount technology. It is a method for production of electronic circuits. Most critical is distinction between SMD (surface-mount device) placement and classic THT (through-hole technology). Placement is on the PCBs (printed circuit boards). In general the SMD is smaller than it's THT counterpart as it possesses no pins or short leads.

Assembly of such circuit is cheaper and consumes less energy. Higher components densities can be reached. Big power transformers, chokes and coupling capacitors still require the THT. In general both technologies are used together to bring the best results. SMT comes first, because it would be impossible to mount the components with transformers, also volume under big THT components can be used. Wave soldering would not be as effective and THT components would face the reflow oven. Manipulation with SMDs is easier, etc. There are too many reasons.

Three critical pieces of drawn electrical circuit are wires, components and transitions. Wires are represented by printed circuit board, components are SMDs and transitions are created by solder paste (or paste). Physical bond to the PCB is created either by solder paste or glue.

Parts of SMT line (Picture T13) are boards storage, rotation and carrier machine, applicator of paste and glue through stencil, placement machine, which is critical and most precise, reflow oven and AOI (automatical optical inspection).

Often the components are hold only by solder joints. Evaluated SMT line has on RLP or reflow side of boards only this type of connection. Those solder joints are created through the solder paste activation in reflow oven. Adhesive is used on the WLP or wave side of the board, which is solder waved after assembly with the rest of the THT components. Those joint are created between SMD's contacts and solder pads on the PCB. Solder paste is often

Sn95,75Ag3,5Cu0,75 alloy plus flux. Those are small particles, mostly in ball shape that are melted together, while flux cleans the pad and SMD's contact from residues, oxides etc., forming a bond.

Solder paste is applied through stainless steel stencil with brush (Picture T14). It has to be processed in certain time as it has limited usability. Glue is applied in the same manner in case of SMDs that are later wave soldered.

Pick and place machine (Picture T15) takes components from the reel (Picture T16) and places them on the PCB. It places tenths of thousands assemblies per hour while skilled operator can do hundreds. It takes the component with air jet.

Reflow oven (Picture T17) is the critical piece of the technology process. While position of the pads, paste and components can create lot of issues, reflow process, proper setup of the temperature profile and timing, atmosphere etc. is vital. Techniques and theory is described in the experiment, where it is linked to the quality parameters. Temperature from the oven is delivered to the board through the radiation and/or through convection. Two temperatures are critical. Low temperature must allow bond to be formed, paste activated, etc. High temperature is risk for the parts. Tension between board and component can crack SMD.

Evaluated SMT line did not possess washing machine, which is often composed of IPA (isopropyl alcohol) plus water and sonic cleaning. Waste disposal is an issue and logistics and storage is problematic. There are MSL (Moisture sensitivity level) SMDs that require special care and storage (Picture T18). Paste and process is designed as no-clean. Best results and pricier are through cleaning.

In general, SMT can be introduced to the industry, where certain processes are prepared. Company is mid to big size and investments in millions are option. Skilled personal is required (technology, repairs and visual inspection). Delivered results are then worth the input.

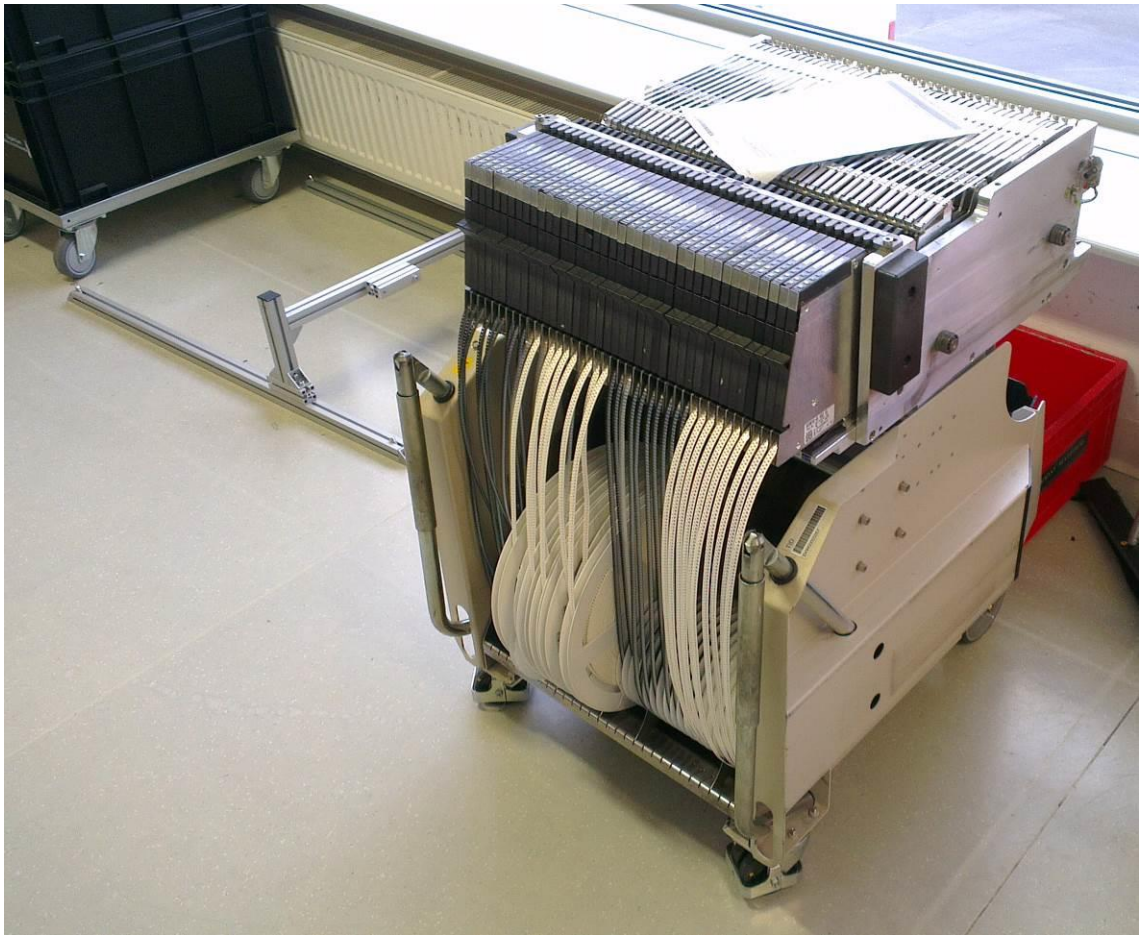
PCB's contamination experiments:

Picture T13: SMT line overview

Picture T14: Machine with stencil for paste aplication

PCB’s contamination experiments:

Picture T15: Pick and place machine



Picture T16: Reels with SMDs

PCB's contamination experiments:

Picture T17: Reflow oven

Picture T18: Drying cabinet for MSL > 1 SMDs

PCB's contamination experiments:

Wave soldering

Wave soldering (Picture T19) is the process that creates electrically conductive bond between printed circuit board and components. It is used for THT components and for surface mounted components. It saves costs and time. Quality is also higher. Upgrade from wave soldering is to selective soldering method.

In order to use the wave soldering (Picture T21), several conditions have to be fulfilled. It is necessary to have PCB designed with solder resist or solder mask. It prevent solder to be attached everywhere, only where joints are exposed. It is also important to create enough pad spacing. This ensures that no short circuit is going to occur.

There are several steps before quality joint is formed. Everything begins with right design, but first the relatively clean board has to be assembled. Pins are on the bottom of the board. Board enters the machine, where flux is applied to the bottom. Flux is activated at the preheat section (Picture T22) and evaporates cleaning the board. When board has proper temperature, so the shock from solder wave is small, it reaches the wave solder and solder attaches to the exposed conductive parts. It is cooled by forced convection on naturally (Picture T23). Joint is formed.

No board, surface and joint is clean enough, therefore fluxing is necessary. It cleans and removes oxidation in same way as flux during reflow does. Flux is applied to the soldered side. Joints are going to be of low quality when there is not enough of it. Or if too much is applied there is going to be lot of residues left on the board. It causes degradation and possibly a failure. Flux is applied by the spray.

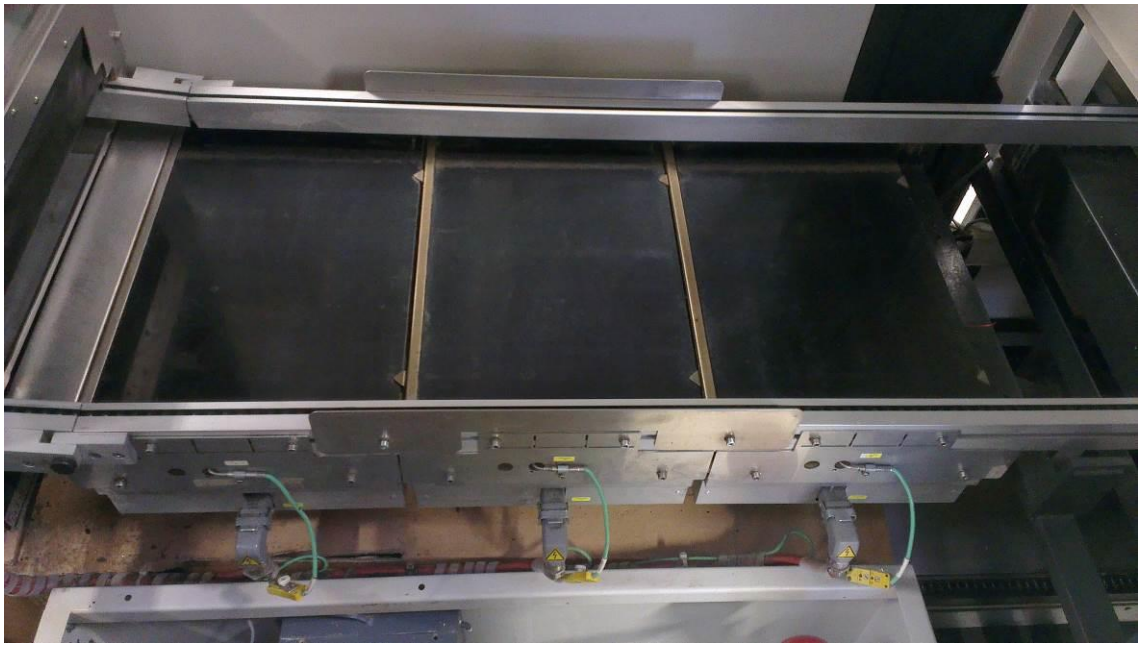
Heat absorbed during wave soldering is far greater than during manual soldering. It is the most severe portion during manufacturing and life cycle. During production board can withstand 1 or 2 wave soldering with 3 being the

top. It also takes a lot of load during reflow (or double reflow). Preheat minimizes the thermal shock and decreases failure rate. Even heating is ensured by hot air and also infra-red heaters. Another important reason is proper flux activation.

In general, wave soldering should be considered as very production and goal oriented method for creating a quality solder joint. However this method puts a lot of stress on the board. High contamination levels are expected.
Selective soldering is more precise and therefore does not damage the board by heat. It is also better with SMT process components. There are SMT components that are designed for wave and components that are not. In quality and price are the differences. The most recent laser technology completely removes stencils (masks) from the process. It is very precise and requires perfect programming, but delivers best results.

PCB’s contamination experiments:

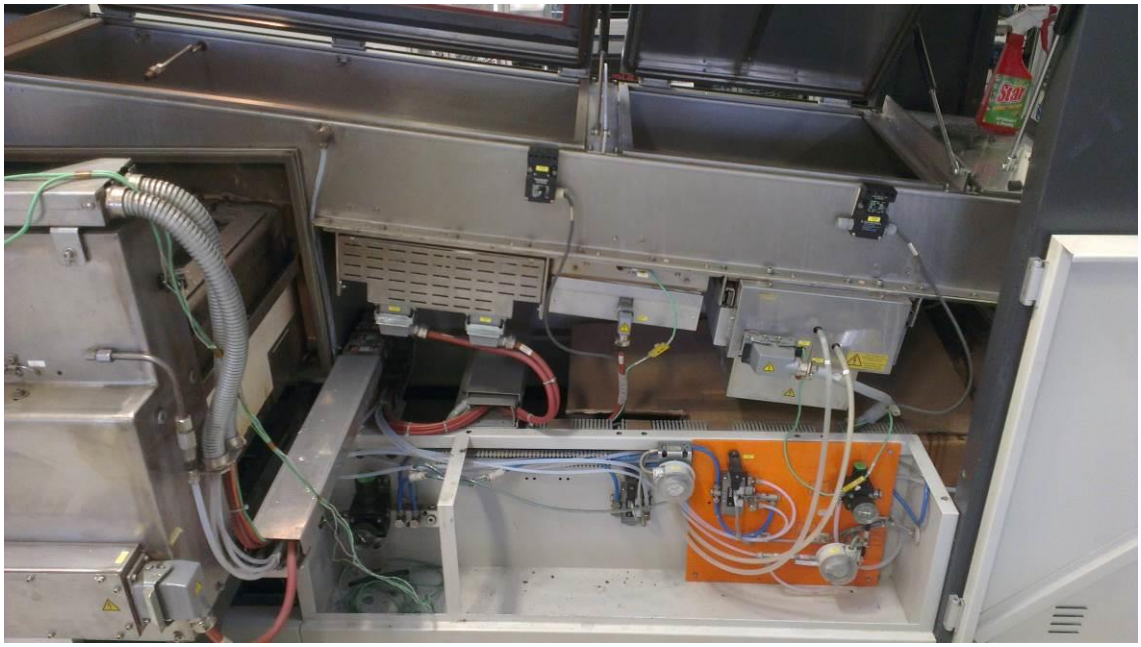
Picture T19: Wave soldering line



Picture T20: Preheating area

PCB’s contamination experiments:

Picture T21: Area with wave soldering



Picture T22: Electronics for preheating

PCB’s contamination experiments:

Picture T23: Cooling is not forced

Picture T24: Cleaning is necessary step

Conformal coating line

Conformal coating is protective material used on printed circuit boards. Humidity, dust particles, chemicals and direct electric break through are prevented from causing any issues to the product. It is also better solution than potting as coated boards are easily repairable. Mechanical stress and vibrations are decreased. It is especially relevant at high temperatures.
It is also in conformance with increasing the assembly density.

Inline variety (Picture T25) for printed circuit boards uses spraying technology. It is the evaluated method. Brush coating is undesirable as it requires skilled operator that devotes a lot of time into work. Quality is also highly variable to robotically applied layers. It is nevertheless used for repairing or after electrical circuit was repaired. Inline sprayed ones are highly uniform, cost oriented, stable in time and has many additional features that prevent failures. Dipping is another technology that can be used. It requires printed circuit board to be designed in certain way as sprayed ones are designed with different properties in mind. It is also repeatable and very importantly, coating covers every device and piece of board. This disqualifies a lot of boards to be coated in this way. No heat sinks, light emitting diodes or potentiometers can be present at time of coating. Dipping is perfect method for winding goods manufacturing as coating creates precise cover required by those products.

Inline spray technology is highly selective and upgradable according new specifications. Pressured at around 5 bars coating is applied by precise jet (Picture 27). Viscosity and therefore volume of thinner must be kept at defined tolerances. Layer thickness is controlled through the jet's speed while pressure and flow is constant in time.
Board or whole product enters line in mask that holds it tightly. It is necessary step for line manufacturing. Same method is used for wave soldering.
When first layer (in most cases, BOT or bottom one is chosen as first) is coated than board proceeds to the manipulator that rotates the board, so that TOP side coating can be applied.

PCB's contamination experiments:

Accelerated curing by oven (Picture T26) is introduced, because (time) efficiency is essential for mass production. Temperature profile is applied for around 30 minutes. Proper temperature decreases curing time and prevents damage of the coating. Accelerated curing and drying is not as beneficial to the water based coatings as they always require more time than acrylic based ones.

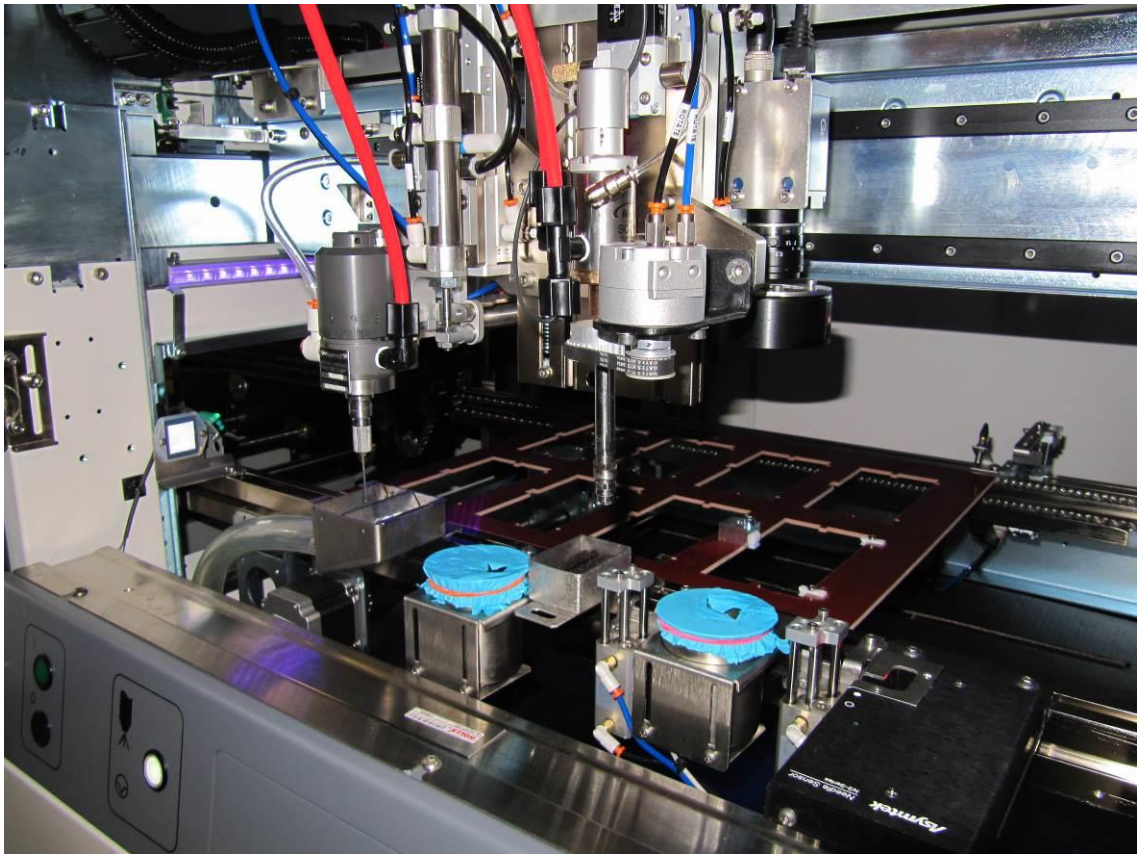
It is important to understand, that in those coating there is a thinner and filler. Thinner evaporates and only filler is left on board. Therefore there is a volume and mass difference. Wet and dry films can be measured and evaluated, but with difference in thickness. In this report I am going to address the dry film thickness unless specified otherwise.

There are epoxy, silicone, polyurethane, amorphous fluoropolymer based coatings except for mentioned acrylic and water based coatings.

Picture T25: Conformal coating line

PCB's contamination experiments:

Picture T26: Oven



Picture T27: Most precise machinery (head) of the conformal coating line

Ionic contamination theory

Ionic contamination is quality parameter of product that refers to the amount of dissolvable conductive elements on the specimen. It is mostly referenced to the surface area.

Ionic contaminants such as bromide, fluoride, potassium, sodium, organic acids or chloride can cause many quality issues and failures. Conductivity of those ions cause electrical leakage. Metal migration and corrosion is present.

Ionic contamination present on the board becomes more active in highly humid ambient. Conductivity on surface is increased.

Mixture of 75 % (in volume) of isopropyl alcohol (IPA) and 25 % deionized water (DI water) is used as extraction medium that dissolves residues from evaluated printed. Theory behind this mixture is that water is substance with high polarity and IPA with low polarity. Substances with similar polarity can be dissolved. Therefore this solution has ability to dissolve low polarity and high polarity substances.

When the ions are dissolved solvent's conductivity is increased. It is measured pre and after the dissolving. Solution is continuously filtered and cleaned to be used again. Direct voltage (DC) is applied and conductivity is measured. As a reference grams of NaCl are used. It is also important to note the surface's area.

There are several limitations. It is only a partly cleanliness factor. Only ions and only dissolvable ions are measured. (In reality, there are none ions on the surface, those are in neutral form and ions are formed when this stable substance is dissolved into IPA + DI-water mixture. Mechanical particles (dust, dirt, burrs, etc.) are problematic as it contaminates the device itself. It is ionography and not ionospectrography based test. It is not possible to evaluate components separately. Another disadvantage is in insufficient exposures that

can always occur and therefore nothing is dissolved, measured and recorded. It is desirable to use resin and flux detection tests in addition to evaluate state as a whole. Test also does not indicate where the highest concentration of the ionic contamination is. It is an averaging method. So everything might seem to be ok, while there will be one or two highly densely contaminated areas. This is also proven by experiment.

Picture T28: Ionograph with accessories

Goal:

Main goal of the test is to find out how much contamination is added to the PCBA by SMD and wave soldering process. This study must be continued by experiments that analyze added contamination from other sources to prevent data corruption.

About testing tooling:

Contamination is measured by Ionograph 500M STD from Invicta UK, developed by SCS Coating. We do not use ionic chromatography.
Contamination is measured in $\mu g.cm^{-2}$ Eq NaCl. It is average over whole PCB. NaCl is reference. It is not Ion-contamination-spectrometer, which measure each element separately. In text I won't mention this unit again, any number linked to contamination is in those.
Residues are indicated by Zestron resin test and Zestron flux test. Those are visual tests, contamination degree is observed by reaction, but it is not quantifiable.

Experiment No. 1:

Quantifying contamination of delivered boards and our assembly process eq. manipulation, SMD assembly, reflowing in oven and wave soldering. During THT assembly parts variation, operators and ambient is involved. This was removed from experiment.

Introduction:

With all the measurement done what I can say with certainty is that no matter what process we were observing, one sample at a time is not enough. Measurement takes long periods of time (from as little as 5 min to 1 hour). More measurements can be done over time, but one or two per day is not enough.
Almost no trends can be extracted from data taken. Without knowledge of the process, without knowledge of any additional contaminations brought from ambient, it will be very challenging to gain value from tests.

PCB's contamination experiments:

PCBs were stored in suitable area. All manipulation in gloves, transport in clean packs. For exception that are noted there was no physical contact.

Handling:

This part contains my observations. It might bring some questions and disagreements. And that is the reason why I stated my standings on this matter. As my intentions are to make this process better and clear. I followed instructions with sole exception where doing so to the extreme would change nothing as I explain in paragraphs that come.

I was very careful during manipulation with samples. I handled PCBs, calipers, hydrometer and other possibly sensitive material in gloves (or in at least one glove). My assumption is that even if I was wearing both, my results would be the same or worse. If I would stay in laboratory and my operation would be limited I would wear both, which I did.

Second hand was used for shield (Ionograph) manipulation, operating computer (keyboard + mouse) and such. This was precautious, because in this way there is no possibility I would touch anything with my naked hand. Those basic things that need to be done are in fact sources for contamination. This way I was mentally forced to not switch or change hands. It was not stressful and without any higher control over myself.

During wave soldering process I used Solder process operator to handle everything that could be source of contamination for my gloves. PCBAs manipulation was my sole and peerless purpose in this regard.

Data:

Far most contaminating process is wave soldering. Contamination goes from twice to four times values of fail point.
Expected trend of autonomous self-cleaning process was not found. It could be there but is clouded in high variation of data. Let's say if cleaning would be 3-10 % per day and standard deviation would be around 20-30 % of the mean, then there is no way to find it.

PCB's contamination experiments:

Wave soldering was done twice. Testing was different. First time there were weights put onto PCB (to match the pressure put on the PCB from soldering wave). Those weights were highly contaminated and even left traces of this contamination on the PCB. Nevertheless during second test this was bypassed by second PCB working as a shield. I take it as not a fully standard procedure, because regularly THT components add substantial amounts of weight. On the other hand, that option seems to be present. Then it should be traced as well even if it is not a direct cause from the wave.

Contamination was varying in time. In case of RLP contamination was growing instead of decreasing. Storage and manipulation was not an issue. If this is caused by ambient so be it. PCB was stored in regular conditions.

Calipers and I suspect that hydrometer also are contaminants by themselves. Because hydrometer is placed into solution during pre-test I see no bigger issue with that. But calipers are used during test and subsequently interfere with measurement. This was measured to 0,04. It is considerable amount. Clean/delivered PCB has contamination 0,03-0,05. Not an issue with PCBA (0,5-3).

Flux and resin contamination:

Delivered, manipulated, reflow side, wave side pre and after wave on none of those samples were found traces of flux or resin contamination. White or brown areas suggesting anything are not present at all.

From this I suspect that our manufacturing process is without any issues in this way.

(Since then I found major issues. This statement was wrong, but at that time, everything lead me to believe so. See next experiments.)

Verification:

Unquestionable data are most important. With this in mind I did verification process twice, whenever data looked corrupted. Even in shorter periods than suggested. Both were without any doubts.

Ionograph needs to be calibrated with specifically prepared and defined solution. It is similar to resistance and inductance calibration before RLC measurement with RLC analyzer.

Mined data:

First tests were always done directly after process or in 1 hour.

Delivered PCBs:
Delivered PCBs taken directly from the MBB are not contaminated at all. Contamination of 0,04 are minimal measured levels. I even took one from the top and one from the middle. Results are the same.

Manipulated PCBs:
During manipulation nothing considerable happens. Results are 0,08. It is twice as much, but initial levels are very low. It is caused more by deviation than anything else. Other possible source for contamination is packaging.
As a manipulation I consider standard process of unpacking and preparation for SMD assembly. Packaging (for delivery between SMD and laboratory) was added.

RLP (without components), RLP with components (only reflow side):
I would like to put those two under one paragraph to compare differences. Contamination grows to 0,50 for assembled board and to 0,90 for unassembled one. This shows us, that SMDs are not contaminants. Rather paste and adhesive are.
Here our expectations were torn apart. Instead of "cleaning" contamination grew. Could be contaminated from elsewhere, but I see no way how.

WLP (RLP + WLP side):
WLP and RLP side has lower contamination than RLP side by itself. This bears very interesting information. WLP process could be very clean (as there is no increase). Or contamination could be here after autonomous RLP side cleaning this ends in similar levels, thus making RLP assembly measurement corrupted. Also this measurement can be corrupted, but I suspect, that no cleaning

between takes place as higher levels are expected. Deviance is last possibility that can not be excluded and is surely present too.

Calipers contamination:
Calipers were tested once and this test is therefore very limited. I put calipers into solution for 30 sec – 1 min (according my feeling to match the duration I usually spend). It brought contamination to 0,04.

Closure:

There are two possible ways how to close this project. We can either accept that contamination is highly unstable and close this in this way. We collected some basic data, so it was very important insight into this domain.
If we want to match this process correctly I expect, that at least 20-30 samples per single area are necessary. Delivery and manipulation looks ok, this work can be shaved off. My proposition if we go this way would be 18 samples on RLP side another 18 RLP+WLP and 32 after wave. I would do only one test of resin and flux test on PCBAs after wave soldering.
Note: 18 = 3x6 (3 samples at a time in 6 batches, twice first day and then next four in 5-6 days to cover one week
32(30) = 5x6 + 2 (5 samples at a time in 6 batches) + RTZ + FTZ
Those are two packages per 40 PCBs.

PCB's contamination experiments:

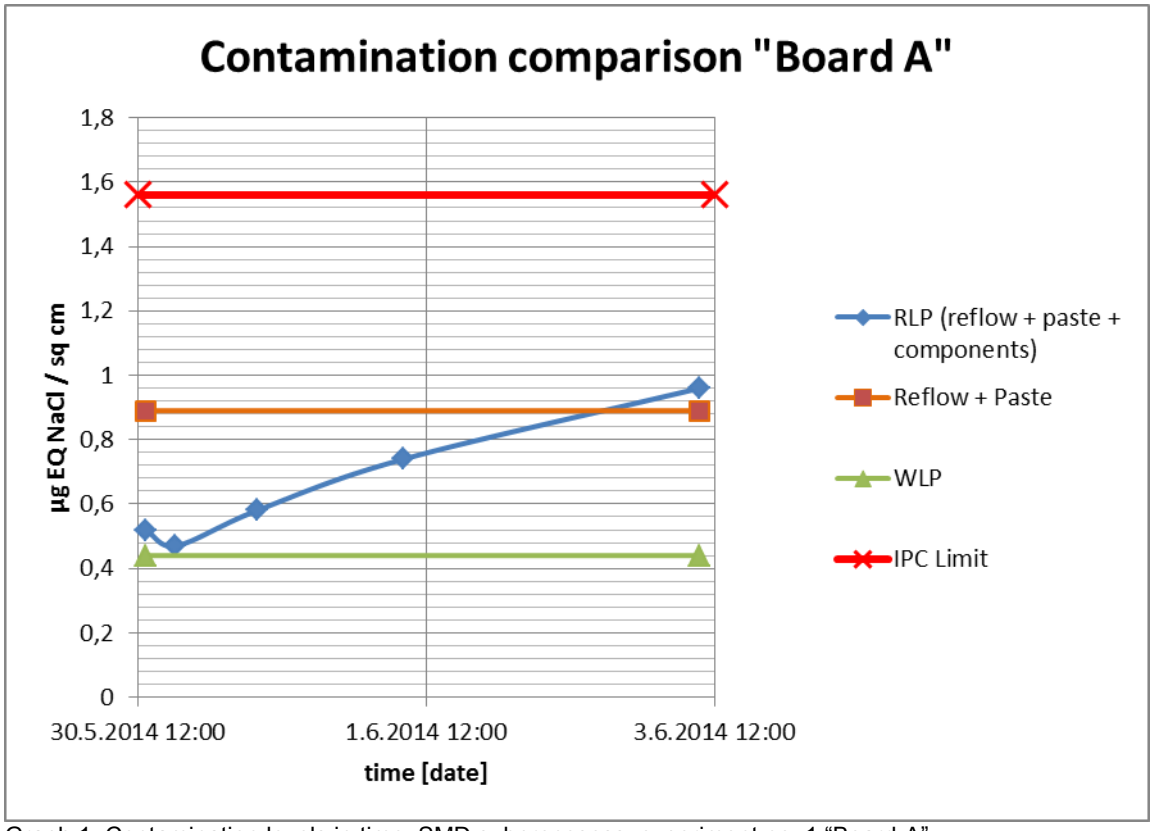
Graphs and tables:

Delivered		Manipulation		Reflow + Paste	
26.5.2014 8:40	0,04	30.5.14 11:10	0,13	30.5.14 12:37	0,96
26.5.2014 8:55	0,02	30.5.14 12:13	0,07	30.5.14 12:56	0,82
26.5.2014 9:05	0,05	30.5.14 12:25	0,05		
µ	0,04	µ	0,08	µ	0,89

Table 1: Contamination levels, experiment no. 1,"Board A"

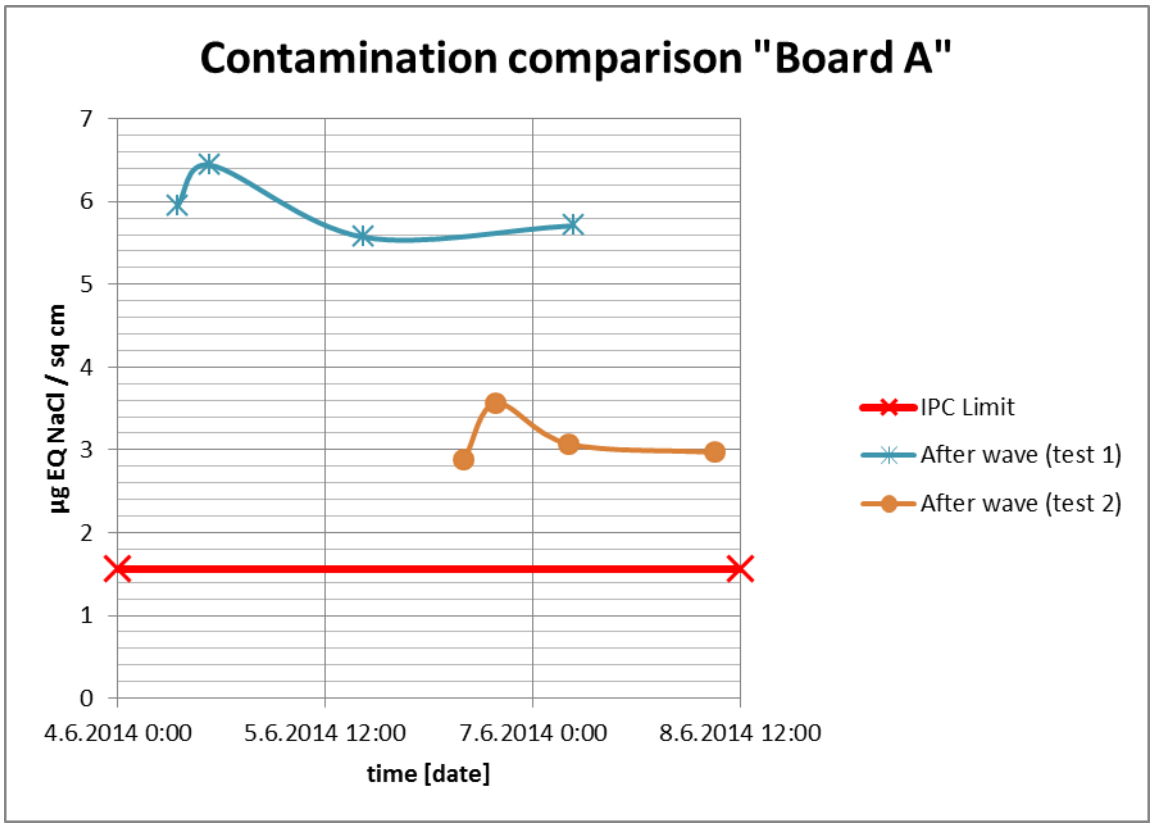
RLP (reflow + paste + components)		WLP		After wave (test 1)		After wave (test 2)	
30.5.14 13:19	0,52	2.6.14 13:11	0,44	4.6.14 10:23	5,95	6.6.2014 12:04	2,88
30.5.14 18:18	0,47	3.6.14 10:06	0,44	4.6.14 16:04	6,44	6.6.2014 17:35	3,56
31.5.14 7:49	0,58			5.6.14 18:38	5,57	7.6.2014 6:16	3,07
1.6.14 8:18	0,74			7.6.14 7:01	5,71	8.6.2014 7:37	2,97
3.6.14 9:31	0,96						

Table 2: Contamination levels, experiment no. 1,"Board A"



Graph 1: Contamination levels in time, SMD subprocesess, experiment no. 1,"Board A"

PCB's contamination experiments:



Graph 2: Contamination levels in time, Wave soldering, experiment no. 1,"Board A"

Experiment No. 2:

Second experiment evaluates SMD and Wave soldering process.

Goal:

Main goal of the test is to find out how much contamination is added to the PCBA by SMD and wave soldering process. This study must be continued by experiment, that analyze added contamination from other sources to prevent data corruption.
This is a second run of the tests. Very much can be gained by cross analysis.

Basics:

Selected sample was part of the bigger order and was treated just as any other part. Manipulation was done in regular manner (income, storage and SMD line). I entered into process after SMD assembly and moved APs to the solder process (to cross THT assembly).
Those boards were manufactured on SMD line No.: 1 As opposed to the past test, where it was done on No.: 2. Soldering took place in the A (in both cases).

Timing:

Assembled boards were first measured after 3 hours (SMD mounting). Then those boards were soldered after approximately 24 hours. Again were measured, right after that. Another is planned after 1, 3 and 5 days.
One measurement takes 30 to 60 minutes (plus regeneration and manipulation). Measurement is contamination dependent (there is a correlation).

Sample size:

Whole order was 40 boards. 40 boards were assembled. 20 measured and 20 soldered. Then those soldered were also measured.
20 was separated into 4 batches. Measurement is done directly after test, 1, 3 and 5 days. It is necessary as it took 5 hours to properly test single batch.

PCB's contamination experiments:

Additions:

Additional 24 boards were tested. Except for delivered ones, all other boards were designated to be scrapped. Before anything those were first cleaned in the IPA.

This gives us some thoughts about what can happen and what can be gained or lost by selected actions.

Purpose	Sample size
Delivered and packed "board B"	4
Cleaned and labeled	4
Neat finger prints	4
Sweaty fingers	4
Dirty gloves	4
Fall to the ground	2
Lying in the oven	2

Table 3: Sample sizes, experiment no. 2

Contamination [µg eq NaCl . cm^{-2}]	
Action	µ
Sweaty fingers	0,22
Neat fingers	0,06
Dirty gloves	0,09
Fall to ground	0,16
Inside oven	0,05
Clean + label	0,09

Table 4: Contamination levels from operations, experiment no. 2

Results:

Delivered "Board A2":

Contamination [µg eq NaCl . cm^{-2}]				
µ	σ	Min	Max	c [%]
0,38	0,073	0,30	0,44	19,4

Table 5: Contamination from supplier, experiment no. 2

PCB's contamination experiments:

After SMD assembly:

Contamination [µg eq NaCl . cm^{-2}]						
t [date]	1	2	3	4	5	6
18.9.2014 9:30	2,31	2,22	1,88	2,23	1,97	
19.9.2014 9:12	2,83	2,53	2,27	2,29	2,31	
21.9.2014 9:15	2,27	2,11	2,62	2,29	2,70	1,89
23.9.2014 8:27	2,19	2,41	1,94	1,83	2,25	1,61

Contamination [µg eq NaCl . cm^{-2}]				
µ	σ	c [%]	Min	Max
2,12	0,186	8,8	1,88	2,31
2,45	0,239	9,8	2,27	2,83
2,31	0,305	13,2	1,89	2,70
2,04	0,297	14,6	1,61	2,41

Table 6: Added contamination by SMD, experiment no. 2

$$\mu = 2{,}23 \text{ µg eq NaCl . cm}^{-2}$$

After solder wave:

Contamination [µg eq NaCl . cm^{-2}]						
t [date]	1	2	3	4	5	6
19.9.2014 15:45	5,24	5,15	5,76	5,32		
20.9.2014 12:21	6,47	6,26	6,92			
22.9.2014 9:57	7,15	5,95	7,04	6,22	5,59	
24.9.2014 10:36	8,73	6,88	8,07	7,17	5,85	

Contamination [µg eq NaCl . cm^{-2}]				
µ	σ	c [%]	Min	Max
5,37	0,271	5,0	5,15	5,76
6,55	0,337	5,1	6,26	6,92
6,39	0,682	10,7	5,59	7,15
7,34	1,110	15,1	5,85	8,73

Table 7: Added contamination by Wave soldering, experiment no. 2

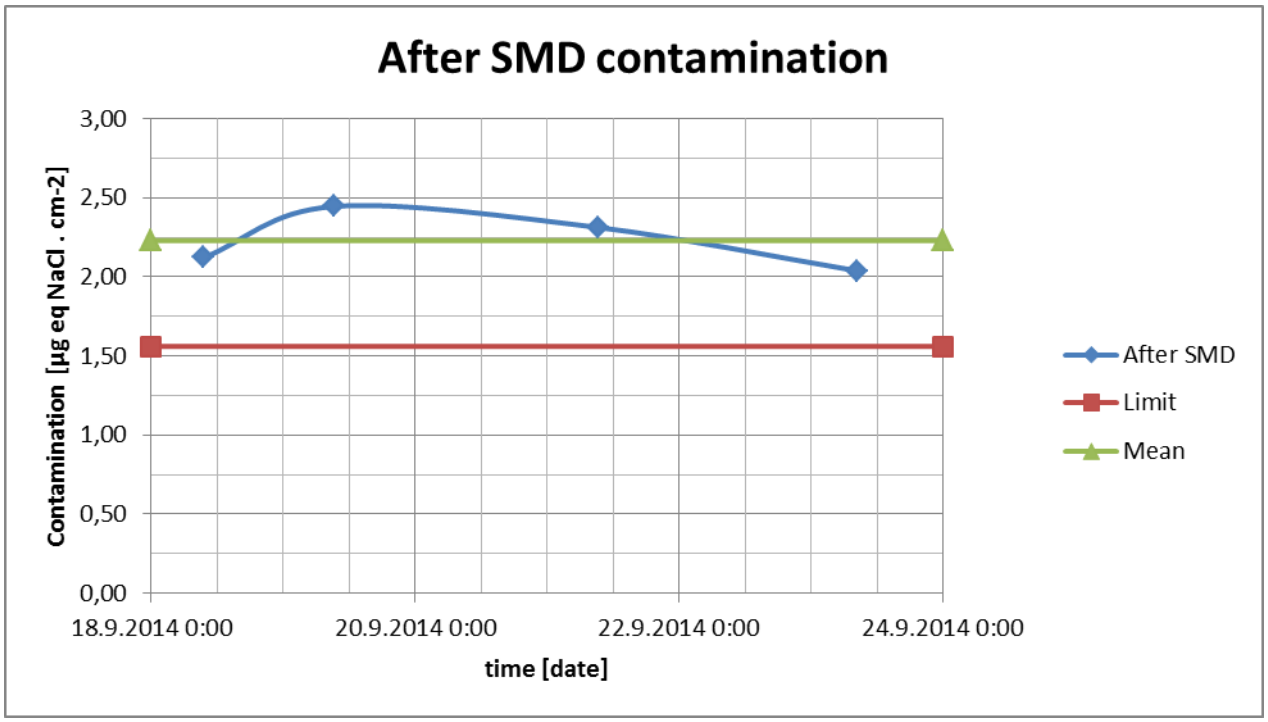
$$\mu = 6{,}41 \text{ µg eq NaCl . cm}^{-2}$$

µ - mean

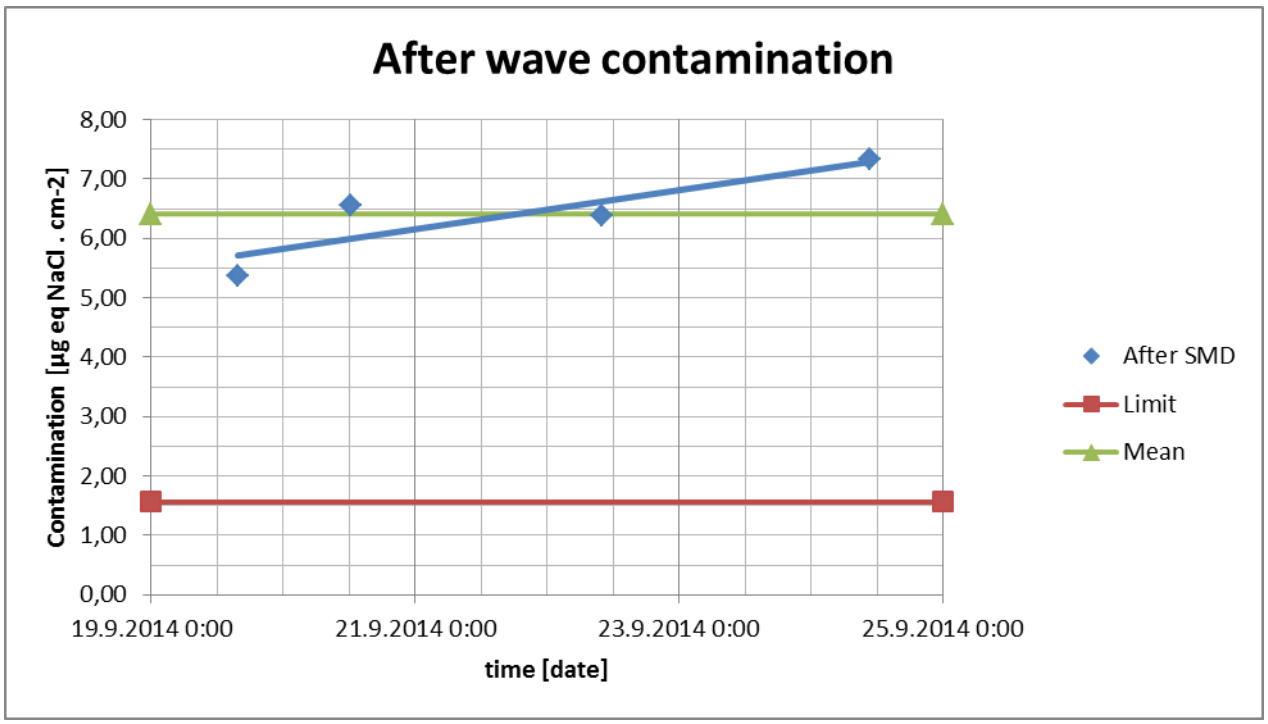
σ – standard deviation

c – variation coefficient = σ/µ

PCB's contamination experiments:



Graph 3: Contamination levels in time, SMD process, experiment no. 2,"Board B"



Graph 4: Contamination levels in time, Wave soldering process, experiment no. 2,"Board B"

Results (second = actual experiment):

Delivered – SMD, Delta Contamination = **1,85 µg eq NaCl . cm^{-2}**

SMD – Soldered, Delta Contamination = **4,18 µg eq NaCl . cm^{-2}**

Past time- for comparison, SMD 2 line assembly:

Results (first experiment):

After SMD μ = 0,65 μg eq NaCl . cm^{-2}

Initial contamination was μ = 0,04 μg eq NaCl . cm^{-2}

After wave μ = 3,12 μg eq NaCl . cm^{-2}

Delivered – SMD, Delta Contamination = **0,61 μg eq NaCl . cm^{-2}**

SMD – Soldered, Delta Contamination = **2,47 μg eq NaCl . cm^{-2}**

Commentary:

There are 20 samples for each. There is always some variance in the process. It is followed by differences in operator and laboratory worker, even laboratory equipment or cleanliness of gloves. Time variance can not be offset as it takes around 1 hour to measure each sample. This brings us to 3 days at minimum. So my guess is sample size is optimal.

Comparison:

Different SMD contamination is one thing that stands out. There is a big difference, even if additional possible contaminants and deviation of process are included.

My conclusion is higher cleanliness of SMD line 2. Possibly due to cleaning/maintenance during KW 18 (tests took place KW 20). While on SMD line 1 maintained during KW 29 and evaluated during KW 38.

Soldering process also shows high difference. But it is high variance process and highly uncontrollable (I had my doubts and already rejected few results). As even a weight, that is placed on the board can move and change the results. Variation is increasing with time.

Results show, that during time contamination is increasing/decreasing to some equilibrium. This process looks to be longer than 5 days.

PCB's contamination experiments:

	SMD contamination	Wave contamination
First experiment	0,61 µg eq NaCl.cm^{-2}	2,47 µg eq NaCl.cm^{-2}
Second experiment	1,85 µg eq NaCl.cm^{-2}	4,18 µg eq NaCl.cm^{-2}

Table 8: Contamination levels comparison

There is not exact answer to the given question. Variance is very high. I propose to check contamination (after SMD) regularly, on just single board and find out more. I would do one or two boards per week and per SMD line.

We need to get process under control. No matter the current state. There are more variables to be quantified. Those are time, line 1/2, input material, assembly, maintenance period, etc.

Incoming boards are relatively all right. Those are not perfect, but would easily pass. Most contamination is wave soldering, then SMD assembly and manipulation.

Experiment No.3:

Deep evaluation of possible contamination sources on SMD assembly only.

Testing:

"Board B"

Module PCBA was solely done on SMD line 2. Those were taken from serial batch. Handling and production are those, that are regularly used.

Three types of tests were done:

Contamination has different characteristics and methods are different. Residues from paste, soldermask's impurities, handling issues etc. In general methods, which are used have variable and attributive (more or less) results. Ionic contamination is measured in µg eq NaCl . cm^{-2}. Zestron resin and flux tests (with upcoming tinten test) are visual test, that show presence of residues.

Ionic contamination:

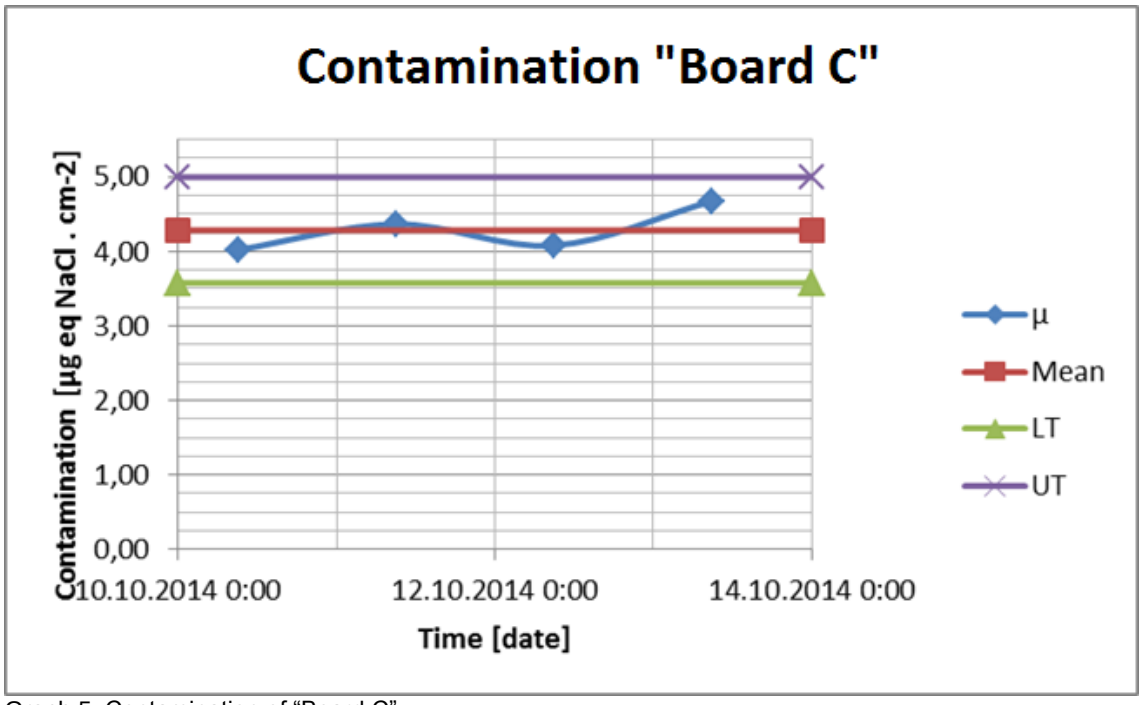
Four times six boards were measured. Time variance is a lot lower than general variance of the sample batch, time dependence is not findable. Based on graph no. 1, we can confirm results within σ range.

Contamination levels are **three times higher** (see table no. 1) than those suggested by IPC. (1,56 µg eq NaCl . cm^{-2})

Contamination [µg eq NaCl . cm^{-2}]					
t [date]	µ	σ	c [%]	Min	Max
10.10.2014 9:00	4,02	0,671	16,7	3,16	4,97
11.10.2014 9:00	4,37	0,352	8,1	4,01	4,78
12.10.2014 9:00	4,08	0,628	15,4	3,18	5,09
13.10.2014 9:00	4,68	1,015	21,7	3,71	6,66
	Contamination [µg eq NaCl . cm^{-2}]				
	µ	σ	c [%]	Min	Max
	4,29	0,711	16,6	3,16	6,66

Table 9: Contamination, Double RLP, Experiment No. 3, "Board C"

PCB's contamination experiments:

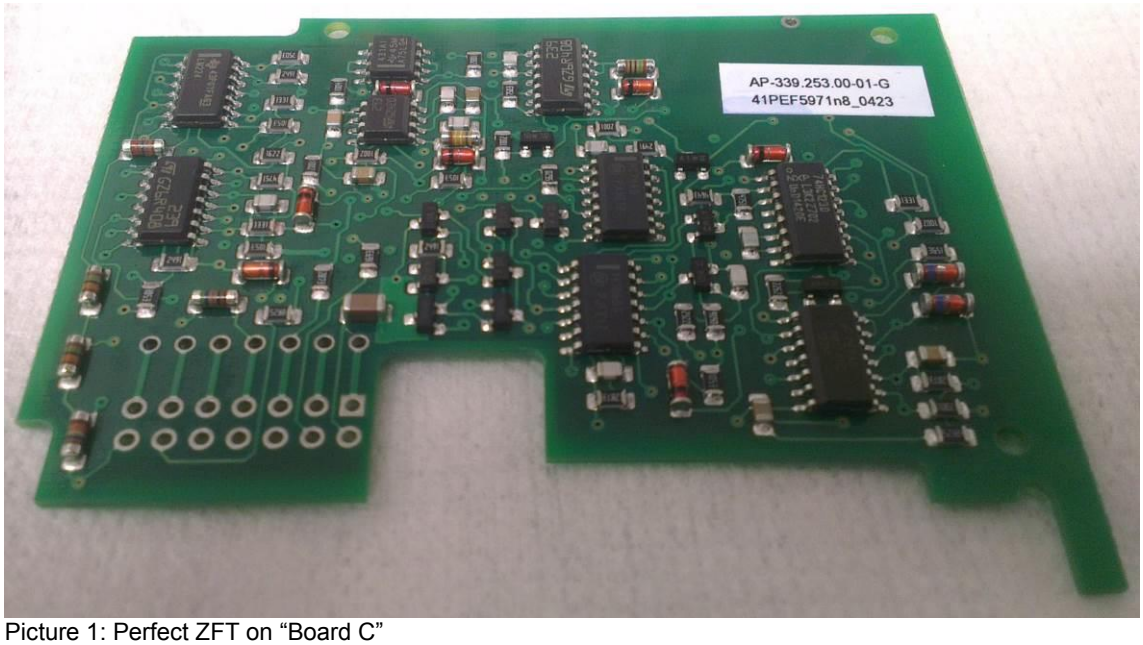


Graph 5: Contamination of "Board C"

Flux test:

There is no reaction to flux. Board and assembly **are free of those residues**.

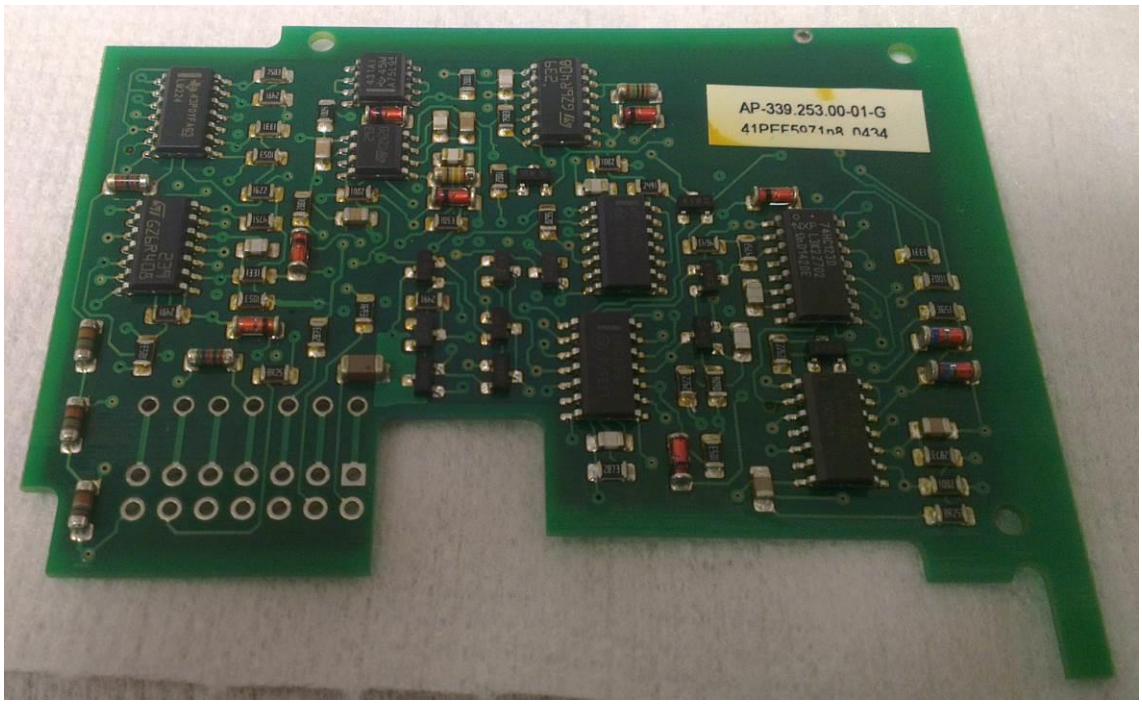
Blue color in the top right corner would be misinterpretation (label) – picture no. 1.



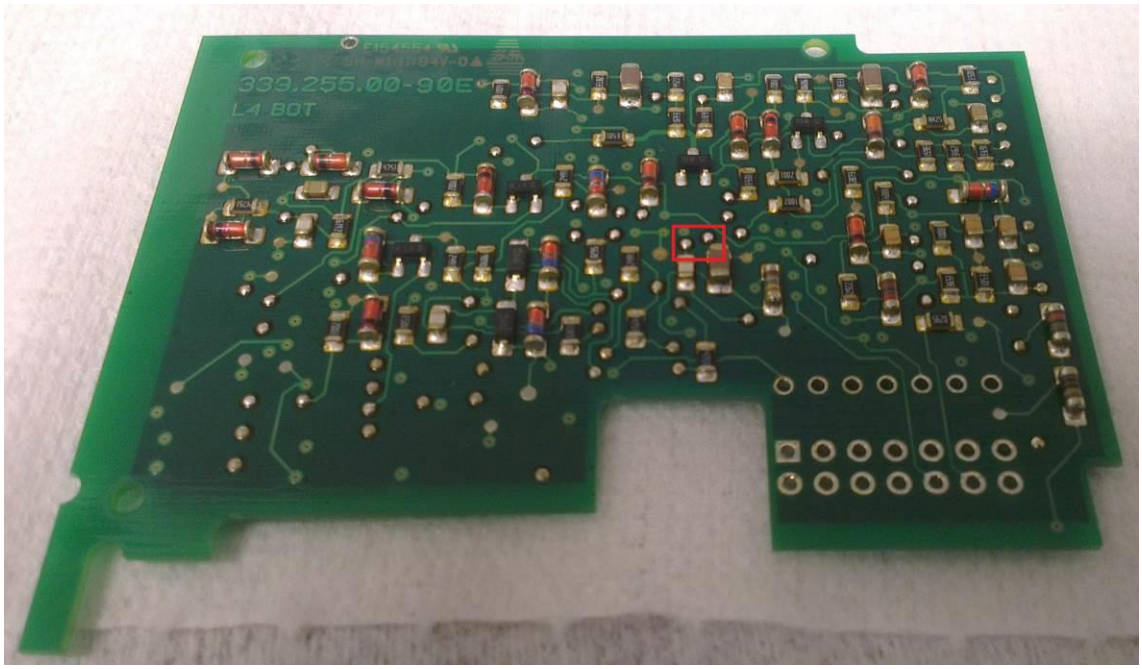
Picture 1: Perfect ZFT on "Board C"

PCB's contamination experiments:

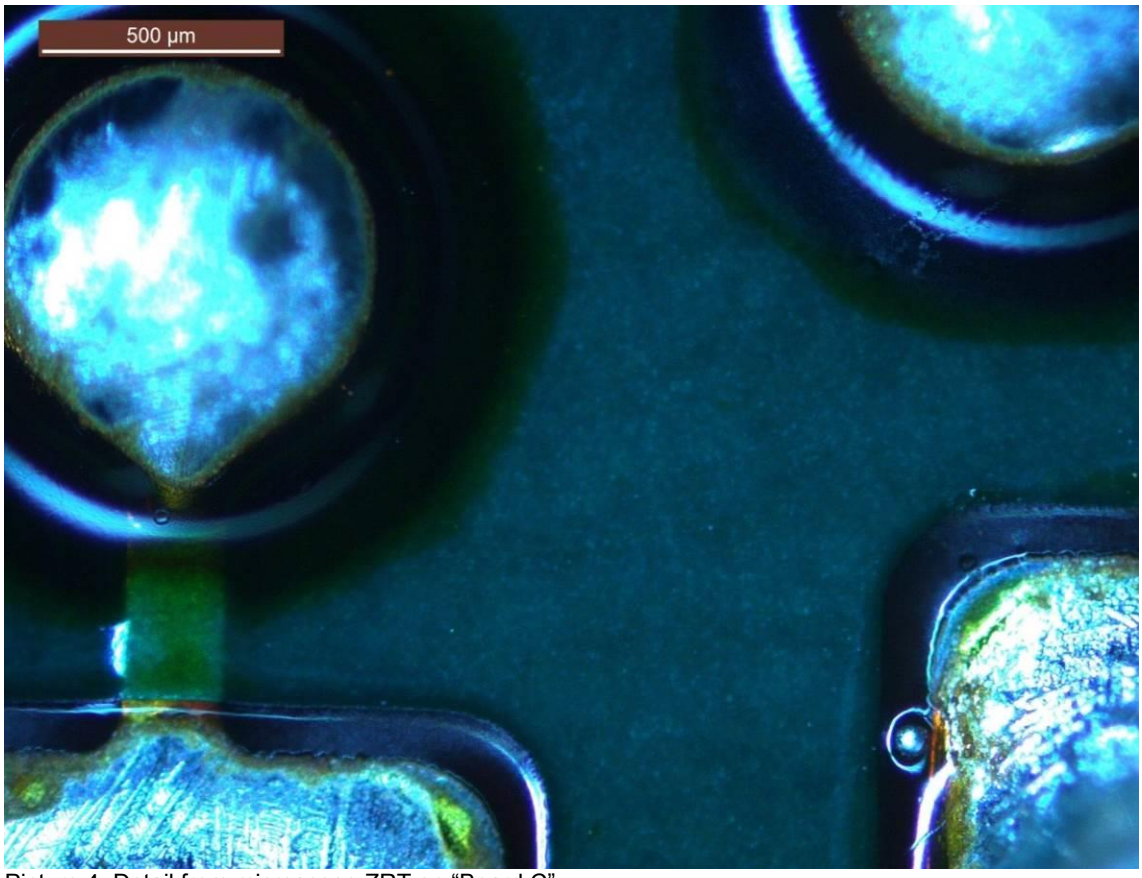
Resin test:
Results show us "very" **high resin residues** from reflow (double reflow, paste)
– picture no. 2, no. 3 and no. 4.



Picture 2: ZRT on "Board C"



Picture 3: ZRT on "Board C"

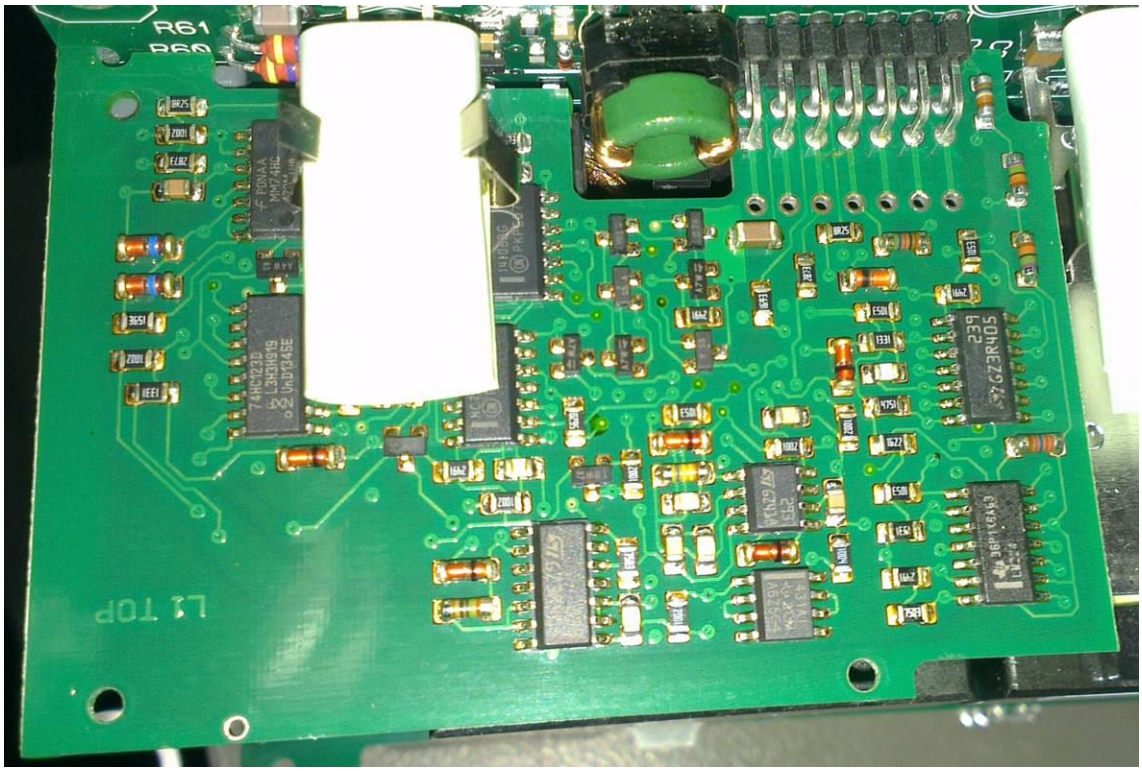


Picture 4: Detail from microscope ZRT on "Board C"

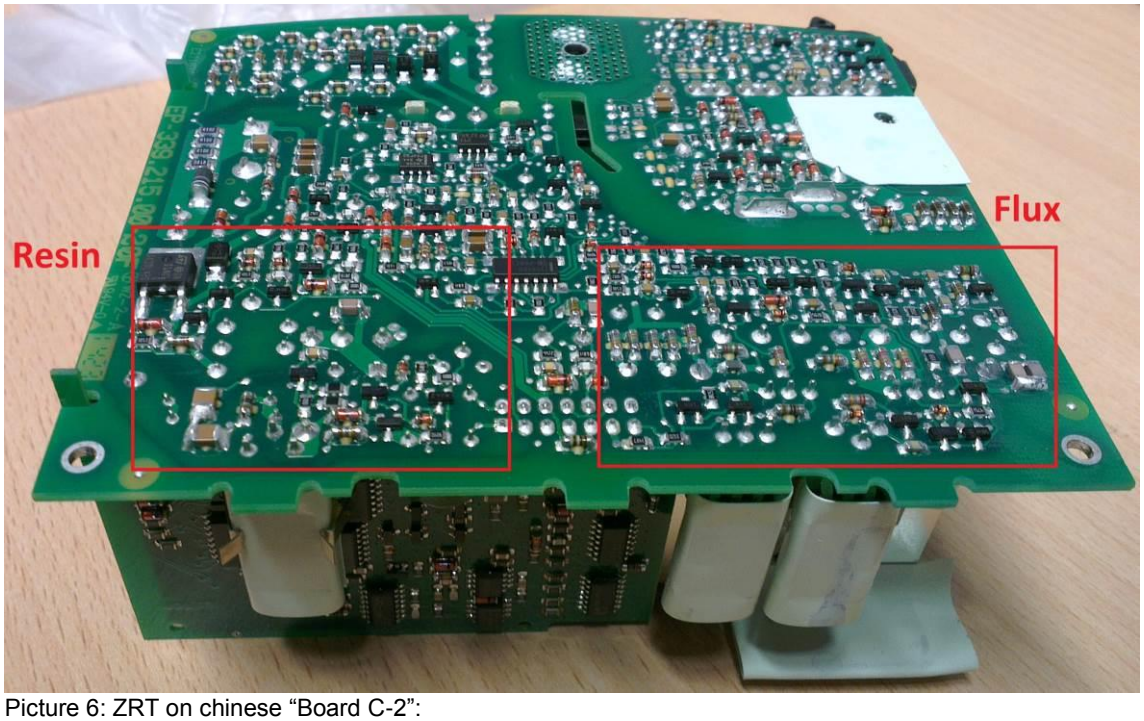
Comparison to chinese "Board B":

Chinese "Board C" is same (in matter of resin residues) as our "Board C" board. It is same even after long time since it was manufactured.
Chinese "Board B" is in good shape. It is similar to CZ results. Main boards after wave soldering are fine.

PCB's contamination experiments:



Picture 5: ZRT on chinese "Board C":

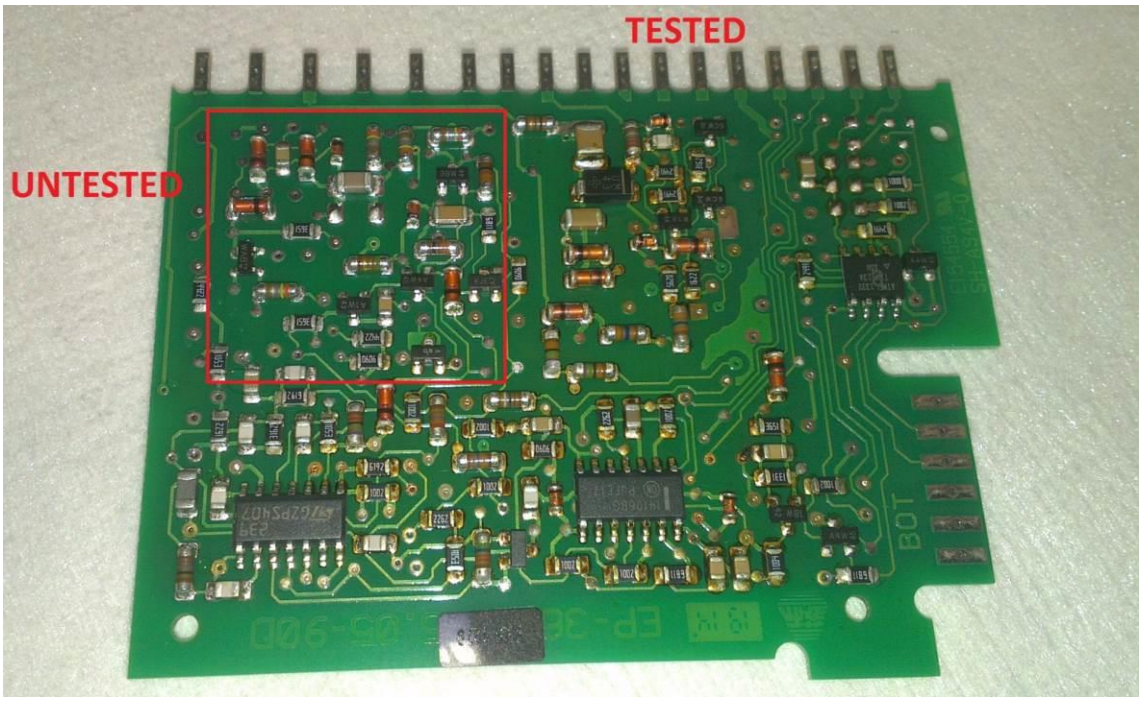


Picture 6: ZRT on chinese "Board C-2":

Note: Affected boards after RLP showed substantially higher resin contaminant levels than boards after wave soldering.

Additional resin testing:

It is not single issue, but general one. This PCB was measured and even three weeks after it was manufactured it shows same results.



Picture 7: ZRT on "Board D"

CZ SMD lines comparison:

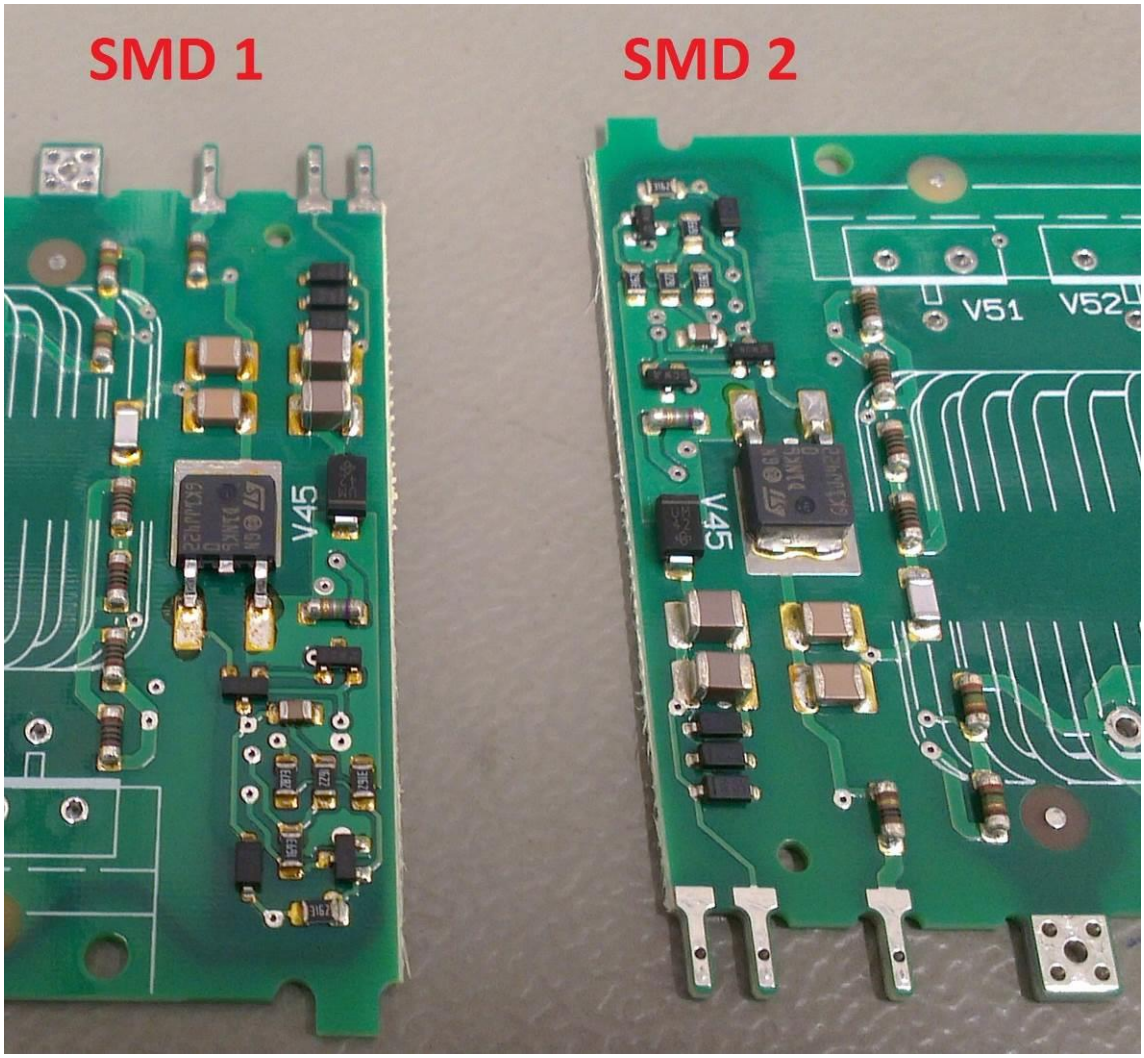
"Board E" was taken as standard (I would like to note, that reason for wide range of used boards is simply to be more flexible, time and resources effective as I do test in subordination to manufacturing.)
"Board E" was compared partly assembled (one reflow side) and in second test only paste was applied. This was done one SMD 1 and SMD 2. By comparison we found, that by resin (and also ionic contamination) test **SMD 1 adds more contamination** to the board. In case of ionic contamination it is by 30 %. Zestron resin test is somehow similar (more or less **by 30 %**).

Multiply [%]			
Affection by SMDs		Lines difference	
SMD 1	69,23	38,64	Paste
SMD 2	82,09	28,85	Assembly
Mean	75,66	33,74	
Chosen	**75,00**	**30,00**	

Table 10: Comparison contamination of "Board E", see paragraph under table

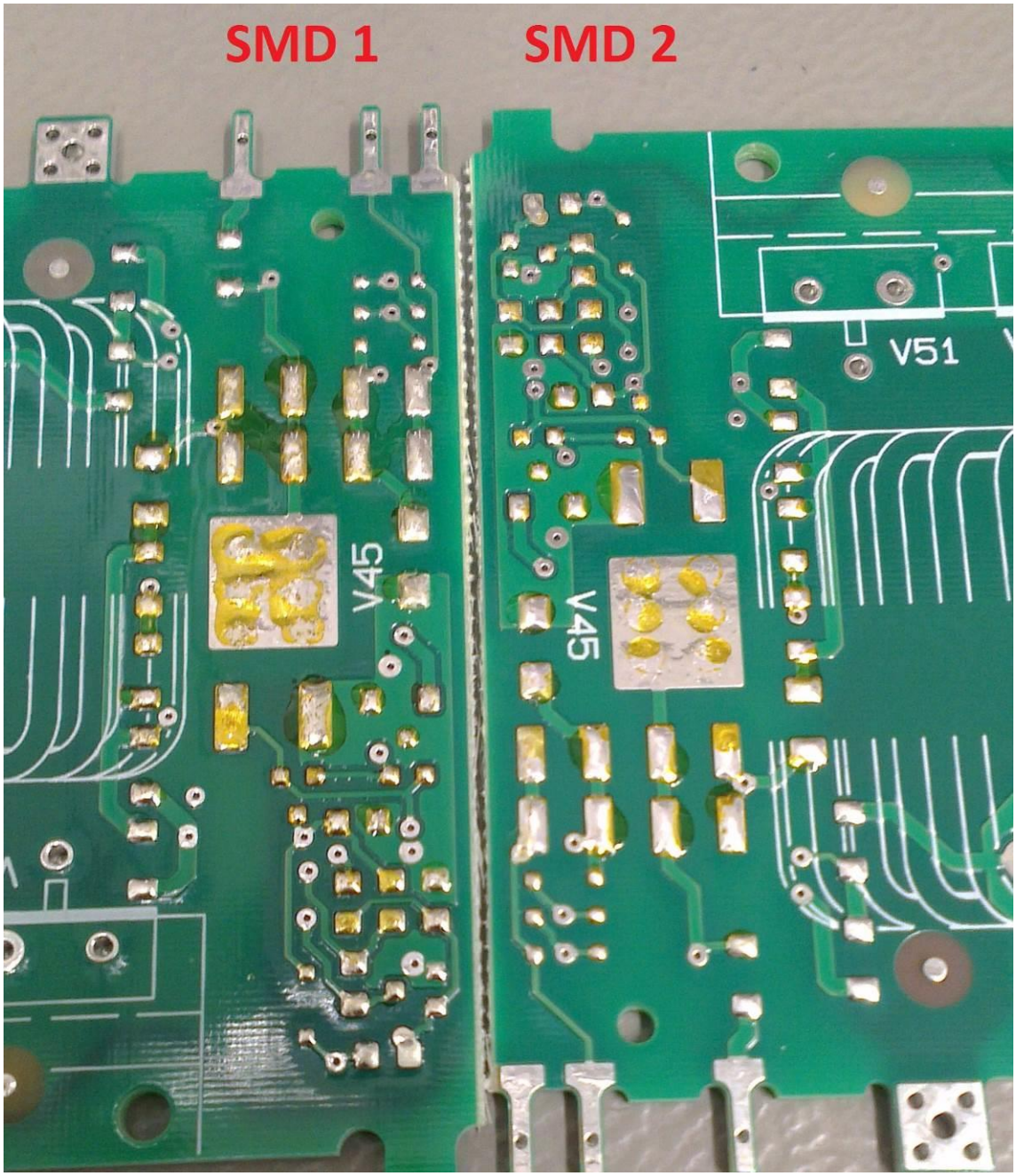
Table can be easily misinterpreted. SMD line 1 adds more contamination to the board between 30 and 40 % (higher sample might be required). PCB is more contaminated when it is not assembled (more paste is present and „visible" to spectrometer).

PCB’s contamination experiments:



Picture 8: Comparison ZRT on “Board E”

PCB’s contamination experiments:



Picture 9: Comparison ZRT on “Board E”

Results:

Ionic contamination:
Ionic contamination of PCBA (SMD) is higher than specified by IPC. In case of module boards it is 2 or 3 times higher. Main boards have lower results. My calculations leads me to believe, that levels are based on pads area. Module boards have higher density of SMDs and are double reflowed. Important will be results broad by practical conformal coating. If those will not fail and process will be under control, then we can manufacture and constantly improve our methods.

Resin and flux tests:
Pasted areas shows resin residues. From this perspective wave soldering is clean process. Flux residues are not present on either module or main boards.

Comparison tests:
SMD line 1 is 30 % more contaminated than SMD line 2. Resin tests are similar in this manner. There is a different nitrogen atmosphere, which might be a reason. Additional testing is planned.
Resin test are same on CZ and CN side of RLP and wave soldering.

SMD Paste influence:

Measured contamination is one measured by ionic spectrometer.
SMD is line used to manufacture those.
Unmasked fraction is size of pads related to whole board (not based on gerber data, additional precision might be required).
Reference contamination is measured contamination related to unmasked fraction of the board.

Results are quite constant, which gives me assumption, that contamination is highly based on contamination brought by paste.
Results are altered by several coefficients, which might or might not be questioned.

All of those tests are on higher sample sizes to be relevant.

Partnumber:	Measured Contamination [µg.cm^{-2} - board]:	SMD:	Unmasked fraction [%]:	Reference contamination [µg.cm^{-2} - paste]:
"Board B"	4,29	Only 2	16,24	28,39
"Board F"	1,02	One on 2	3,79	26,70
"Board G"	4,43	Only 2	18,78	27,67
"Board E"	2,23	One on 2	5,92	31,23
"Board D"	4,30	1 and 2	17,33	28,32

Table 11: Referencing contamination to pasted area

Results are around 30 µg.cm^{-2} EQ NaCl related to cm^{-2} of pasted area.

Calculation:
Reference = f (Measured contamination, Area of board, Area of pads, SMD line, Correction factor added during measurement – 20 % added by components, incoming PCB correction)

PCB's contamination experiments:

Basically:
Reference = (Measured – initial contamination from supplier) * (coefficient of added area by components) / (Unmasked fraction weighted by 1,30 coefficient according SMD 1 and 2 contamination difference)

Reasons:

Initial contamination is either measured or is set to 0,10 $\mu g.cm^{-2}$ EQ NaCl according my experience. It is mostly important with lower contamination levels (around 0,80 – 1,00).

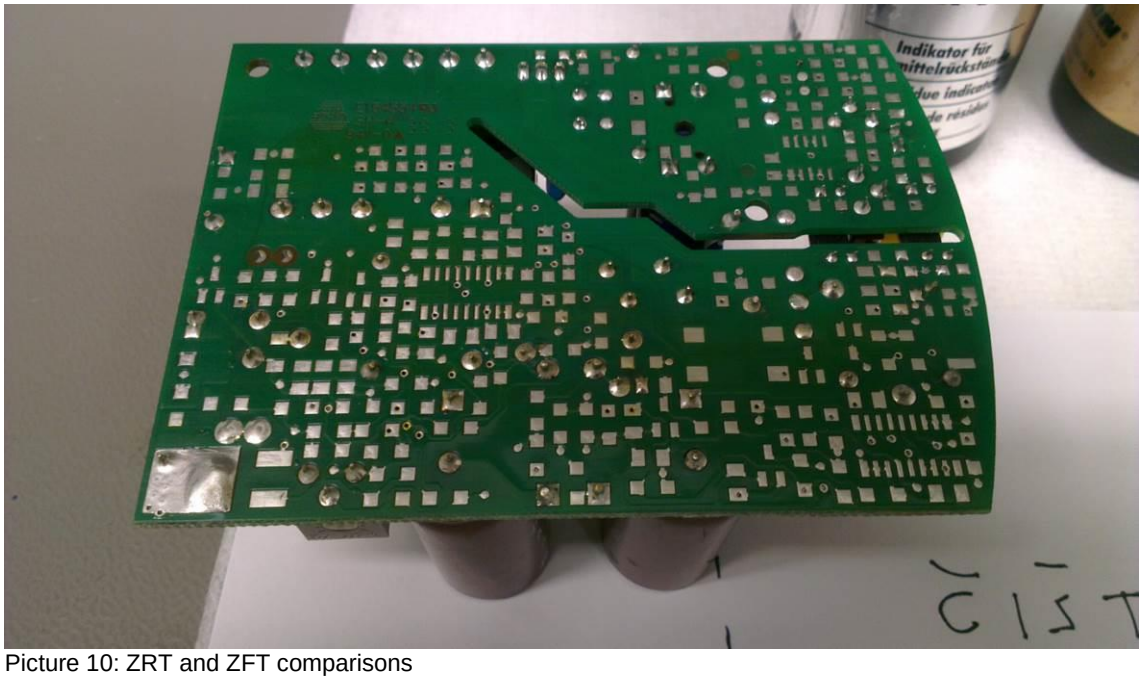
Coefficient of added area is important, because area is counted to physical area, while contamination measurement is based on increased area (which is actually higher due to added components).

SMD lines difference coefficient weights (just like weighting is used in mean counting) areas, because single board can be reflowed in both ovens. We needed one result to prove our thought had real basis, which still might or might not have. I have not counted type II error probability, which might be misleading anyway. But my results are based on fact, that module and main boards gone through this test and brought same results.

Different contamination levels, different unmasked areas, different SMD lines lead me to believe, that thought is right. Model is not perfect and paste is not sole contaminant. What we got is an insight.

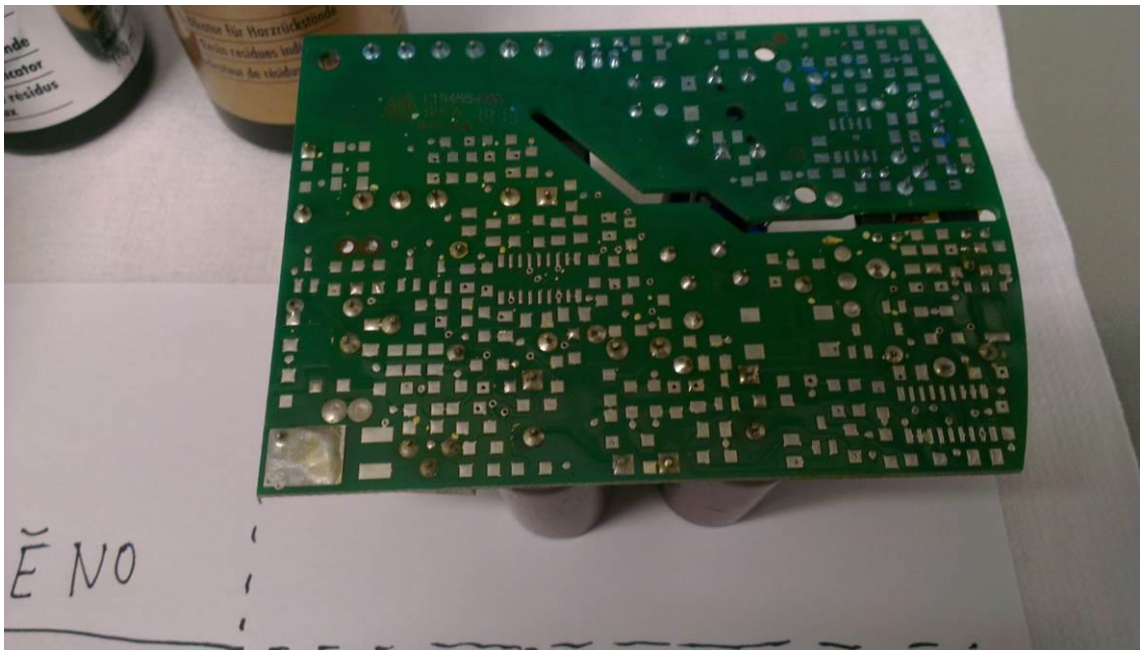
Resin test qualification:

Those results are taken from prior testing (proposed new tin for soldering). There is an method/procedure of how it should be interpreted. But those are great samples for comparison. In this case it was soldering (not SMD paste). In top right is Zestron flux test (ZFT), in bottom left is Zestron resin test (ZRT). Breakdown is nothing means board is perfect. Slightly blue or yellow (brown) indicates beginning of issues. Higher reaction is identified by expressive coloring. Picture no. 10 is perfect example, how board should look like after testing. Only leftovers are on soldermask. Picture no. 11 has beginning issues and process according to standards could be passible, but has to be improved. Last picture - no. 12 shows major residues.

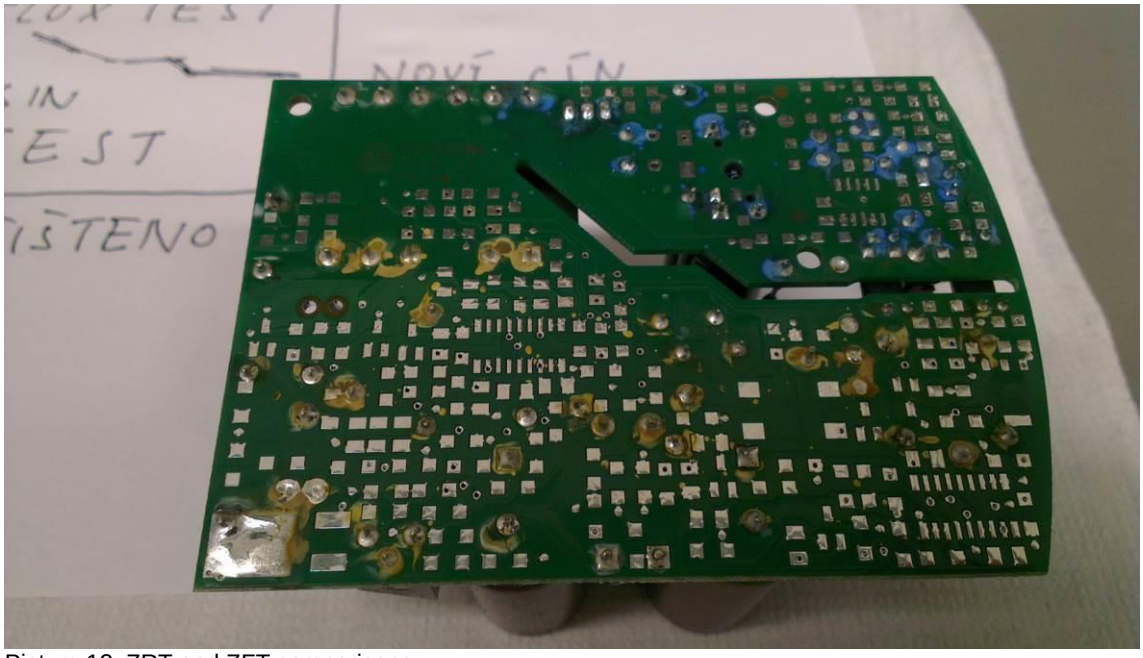


Picture 10: ZRT and ZFT comparisons

PCB’s contamination experiments:



Picture 11: ZRT and ZFT comparisons



Picture 12: ZRT and ZFT comparisons

How oxygen at SMD oven affects contamination:

Testing:

Two parameters were set as critical, those were inspected. Ionic contamination and resin test.

Sample size was 4 pieces per testing level. Three are used for ionic contamination, one for resin test.

Three testing levels were inspected. According atmosphere analyzer, those were 700, 1500 and 10000 ppm of O_2 in atmosphere. Measuring point was at soak. Soak is where flux is being activated.

Board H was set as standard. (Interestingly, in past Board D2, which is double reflowed showed same results as this single side reflowing.)

SMD line 2, which has better setup and lower O_2 concentration (1000 vs 10000 ppm at reflow point).

Results:

0_2 Concentration	700 ppm	1500 ppm	10000 ppm
μ [μg EQ NaCl/sq cm]	3,97	3,00	1,28
	3,40	2,88	3,05
	3,07	3,67	2,19
μ [μg EQ NaCl/sq cm]	3,48	3,18	2,17
σ [μg EQ NaCl/sq cm]	0,46	0,43	0,89
c [%]	13	13	41

Table 12: Contamination as s function of atmosphere's quality

Standard deviation is very high. I would question those results. During samples preparation stage, atmosphere was not very stable.

On the other hand, it looks by my assumptions according resin test results. Even those are not to be taken as quantifiable.

Resin test was used only on board's fraction.

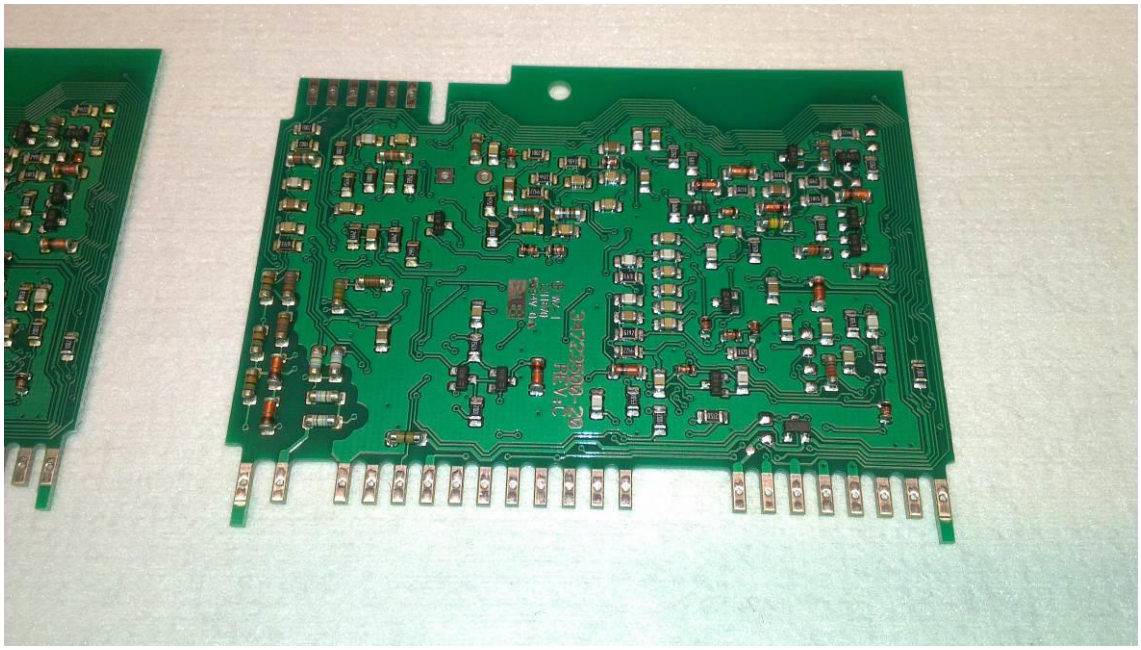
How oxygen at SMD oven affects contamination:

Future of the tests:

Because of setup instability additional testing with higher sample sizes would be required. I will cut 1 500 ppm and use standard (700 ppm) and higher (10 000 ppm).

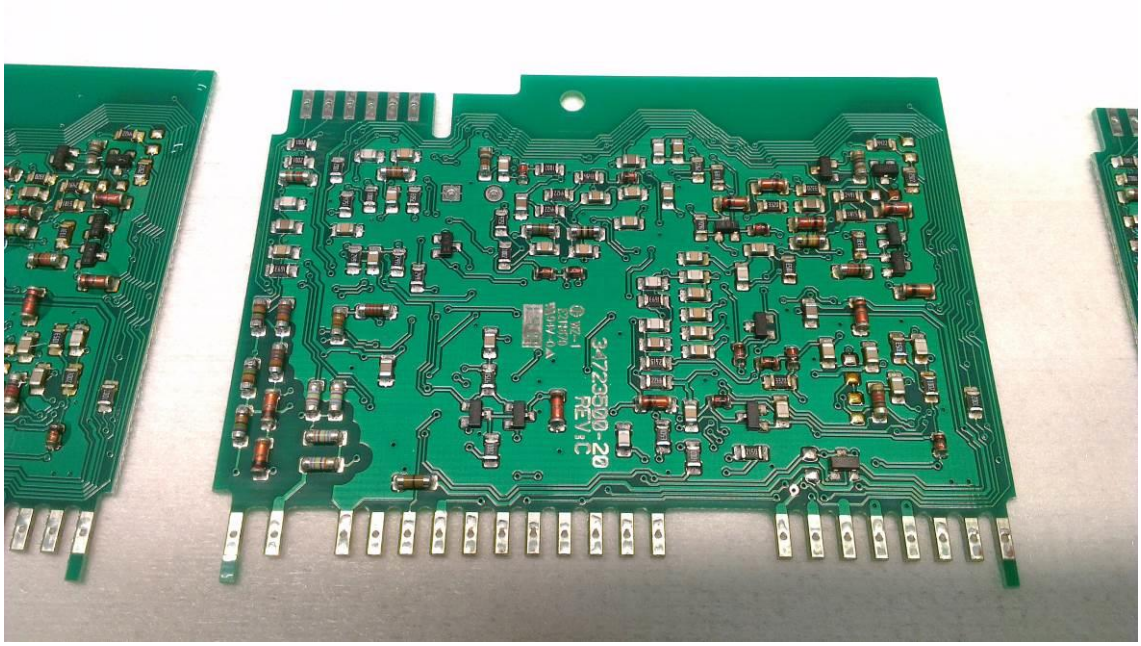
Main board will be chosen as those seems to be more stable in results.

Pictures:

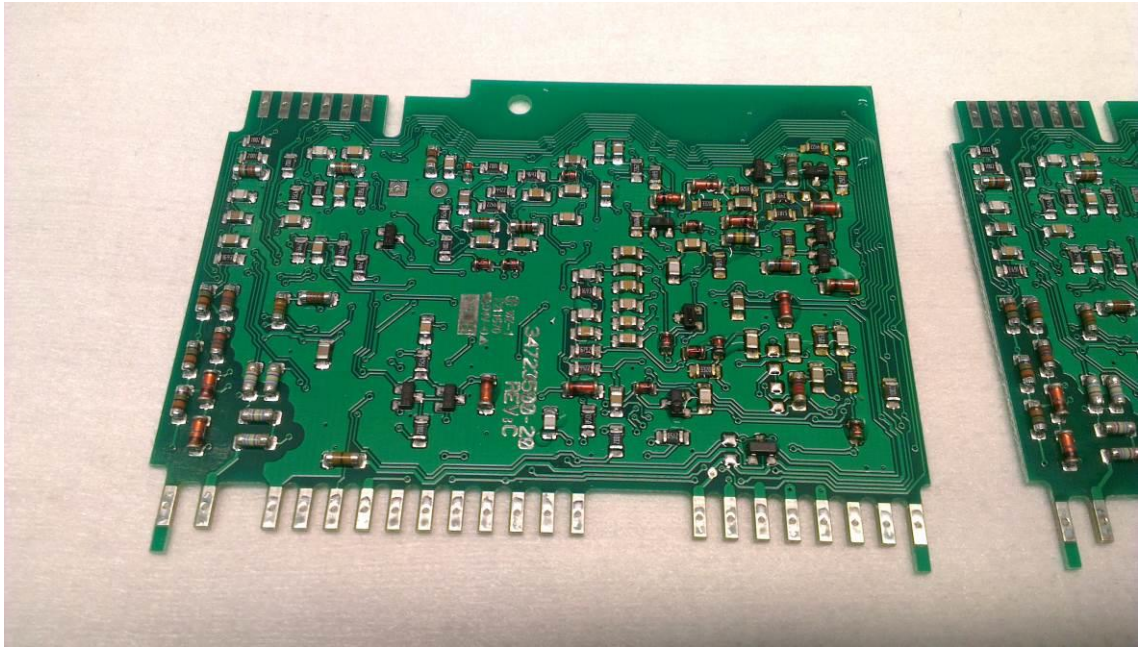


Picture 13: 700 ppm O_2

How oxygen at SMD oven affects contamination:



Picture 14: 1500 ppm O_2



Picture 15: 10000 ppm O_2

Second testing:

Two very distinguish atmospheres, first case was more or less atmosphere of standard process (circa 1 300 ppm of O_2, rest is N_2). Second experiment was 18 000 ppm of O_2.

Measuring point was same eg. soak (part of the oven, where paste is activated).

Contamination [µg EQ NaCl . cm^{-2}]		
O_2	1300 ppm	18000 ppm
Samples	0,98	0,57
	1,15	0,86
	0,66	0,58
	0,79	0,80
	1,34	0,84
	0,80	1,02
	1,05	0,85
	0,83	1,19
	1,01	0,88
	0,94	0,84
µ	**0,955**	**0,843**
σ	0,198	0,182
c	20,7	21,6

Table 13: Second experiment - Contamination as s function of atmosphere's quality

Evaluation:

Correlation between atmosphere's quality and ionic contamination was not found. Variance of the process is too high. It should be understood as it is not a source of differences between SMD 1's oven and SMD 2's oven.

Very limited range of atmosphere's quality was inspected. Highly inappropriate atmosphere would most likely have serious impact.

All results are hidden within variance of the process and tolerances of the measurement.

Contamination temperature dependancy:

Goal:

Improvement of cleanliness during reflowing process on SMD assembly is key. Is ionic contamination of PCBA's temperature dependent? Can activation of paste (flux) and complete removal of residues be achieved?

Experiment:

Board H was taken as a sample. 40 boards were divided into two groups. First one was reflowed according general setup. Second one had increased temperature. Contamination was measured 9x2 times (two boards per measurement). Remaining boards were used on flux, resin and tinten test.

Theory:

(Basic theory to back up the thinking.)
There are four stages in reflow oven: preheat, thermal soak, reflow and cooling. During preheat, thermal rising of 1 – 3 °C per second have to be kept (thermal stress caused to the SMD). Purpose of the thermal soak is activation of the flux and oxidation reduction of the pads. It should be around 1 – 2 minutes. During reflow time (20 – 40 s), solder is activated and joint is created, best possible wetting is desired. Maximal temperature have to be according the weakest component. At temperatures above 260 °C board can be damaged and intermetallic grows. Down ramping around 4 °C per second is recommended.
Preheat and soak point temperatures were increased by 10 °C. Therefore activation of the flux should be better. While this increase will not damage the board and also thermal rising is kept within limits. Speed of the line was not altered and therefore times were not changed.

SMT process notes:

There are three types of heat profiles in the SMD RLP process. There is also one special for glue hardening. The highest one is for special power boards made of aluminum. Those boards absorb most energy. Lower is for the main boards and the lowest for the module boards.

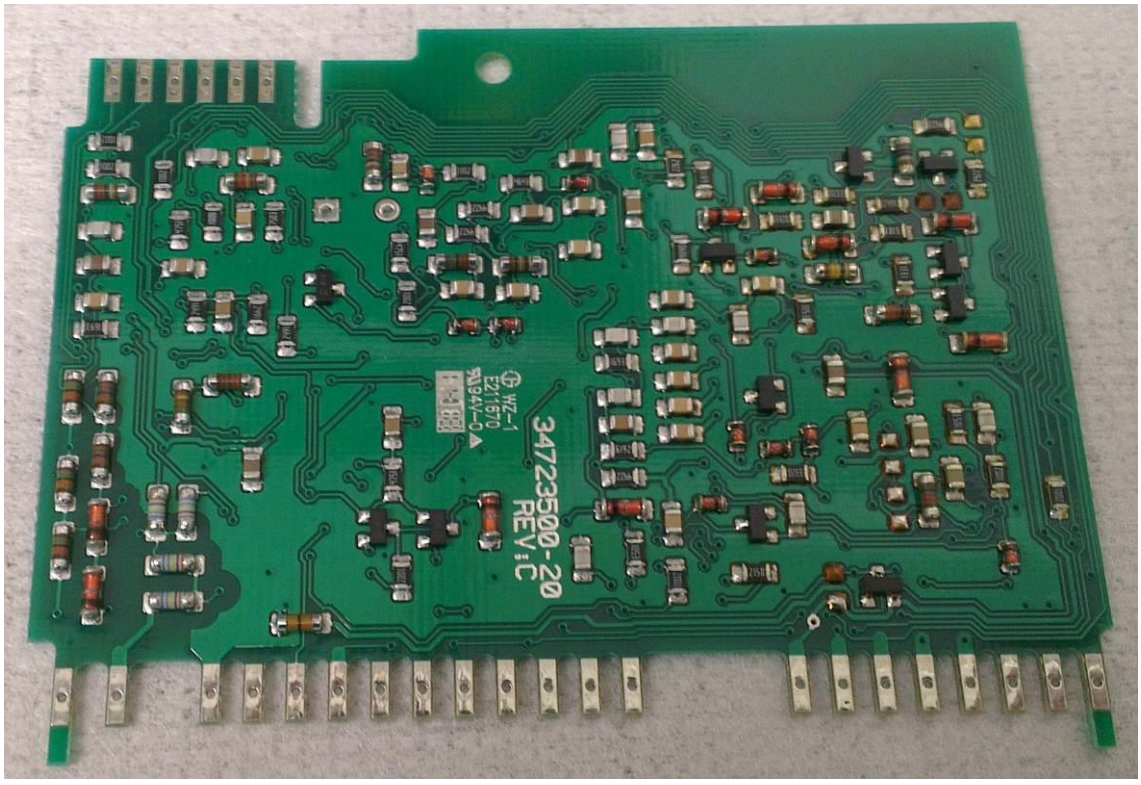
Contamination temperature dependancy:

Some of the difference between the main and module boards could be in this. On the other hand, tests with special board with thermometer were done to match the best profile. This is done on regular (one week) basis.

Results:

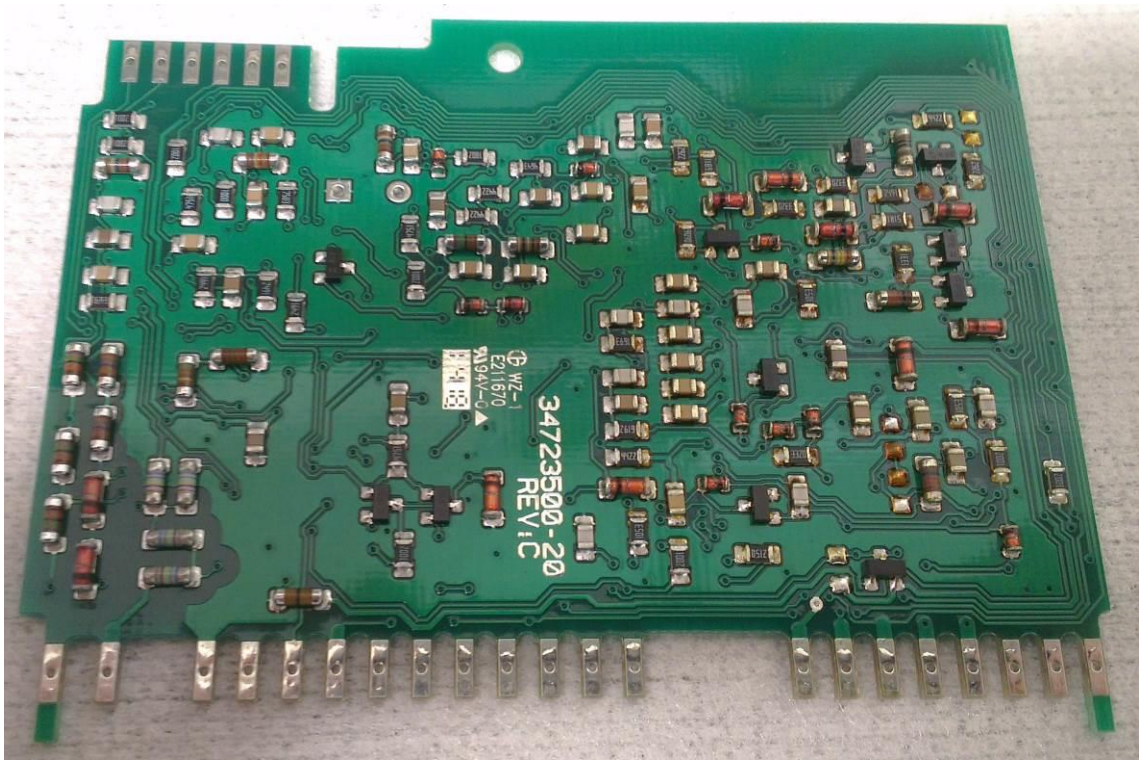
No flux residues were detected. Resin test is positive in both cases. Tinten test measured 35 $mN.m^{-1}$ (no difference between two profiles). All results are according the long term measurements.

Attachments:



Picture 16: Flux and resin test (regular profile)

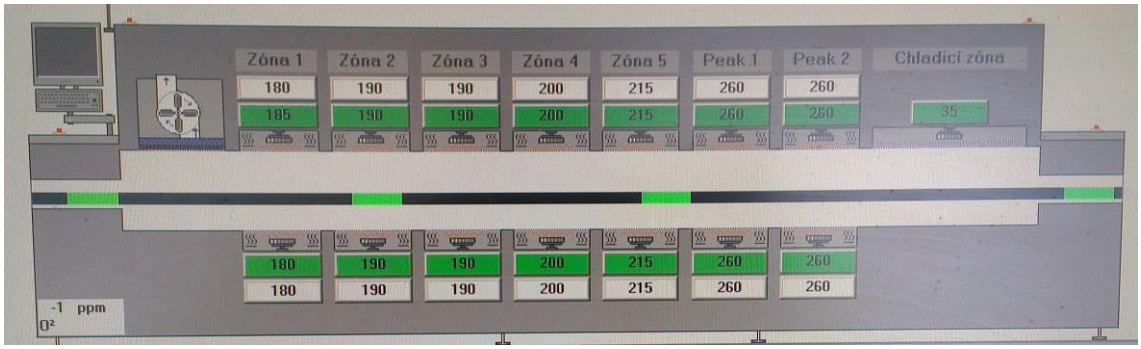
Contamination temperature dependancy:



Picture 17: Flux and resin test (profile + 10 °C)

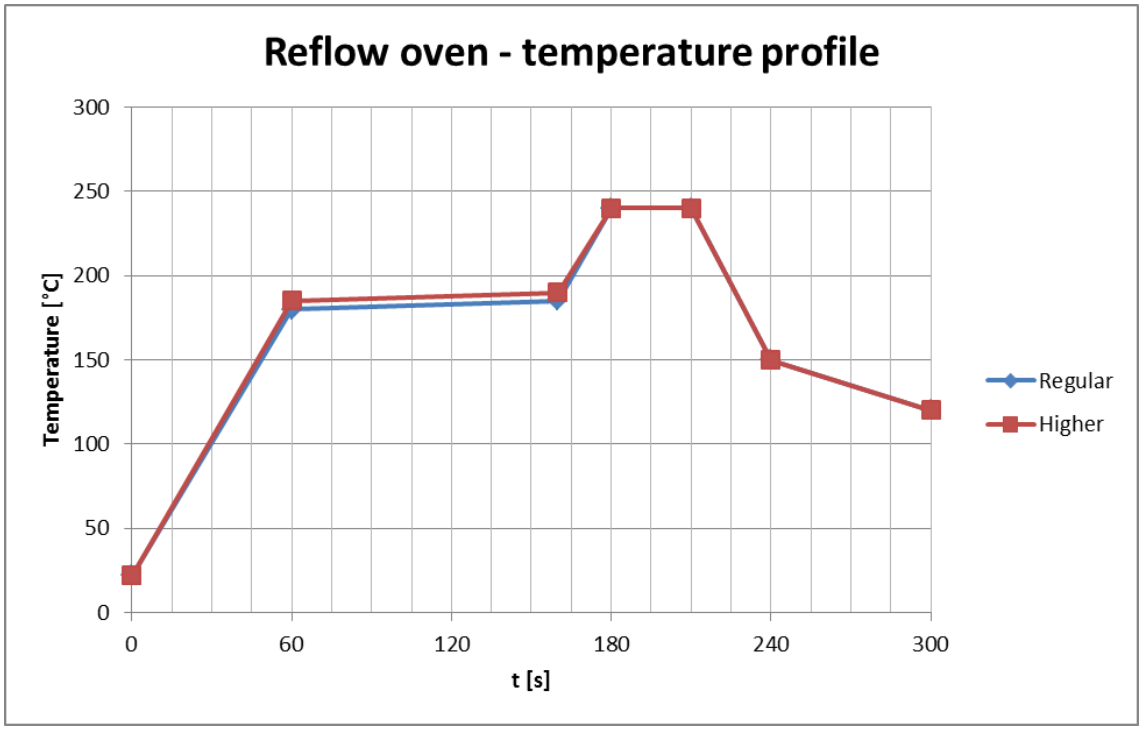
Contamination [µg . cm^{-2} EG NaCl]					
Normal profile			Higher temperature profile		
µ	σ	C [%]	µ	σ	C [%]
4,24	0,61	14,5	3,86	0,46	11,9

Table 14: Contamination difference

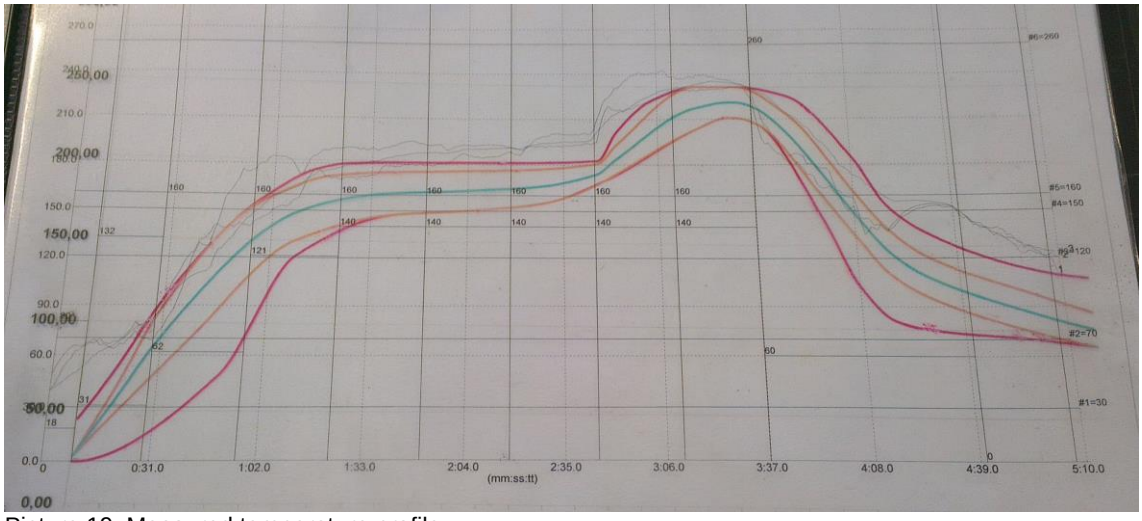


Picture 18: Flux and resin test (profile + 10 °C)

Contamination temperature dependancy:

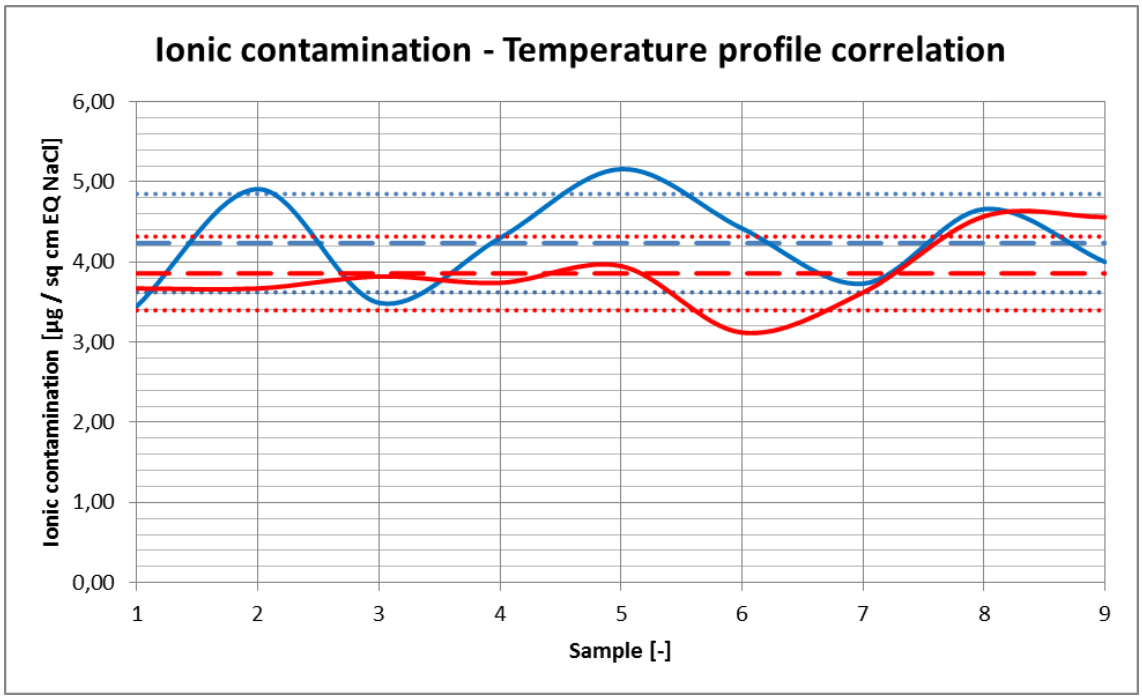


Graph 6: Model to point out difference



Picture 19: Measured temperature profile

Contamination temperature dependancy:



Graph 7: Ionic contamination (Blue = regular, Red = higher temperature)

$$F = \frac{\widetilde{\sigma_1^2}}{\widetilde{\sigma_2^2}} = \frac{n_1(n_2-1)\,s_1^2}{n_2(n_1-1)\,s_2^2}$$

Calculation 1: Statistical relevance of variation (NOT Relevant)

$$T = \frac{m-\mu_0}{s}\cdot\sqrt{n-1}$$

Calculation 2: Statistical relevance of means (ARE Relevant)

Evaluation:

Contamination decreased with increased temperature. Difference is around 9 %. Statistical analysis proved, that those differences are relevant (on p = 5 %). And also variation differences are not relevant.

Solder waved board A – Contamination:

Goal:

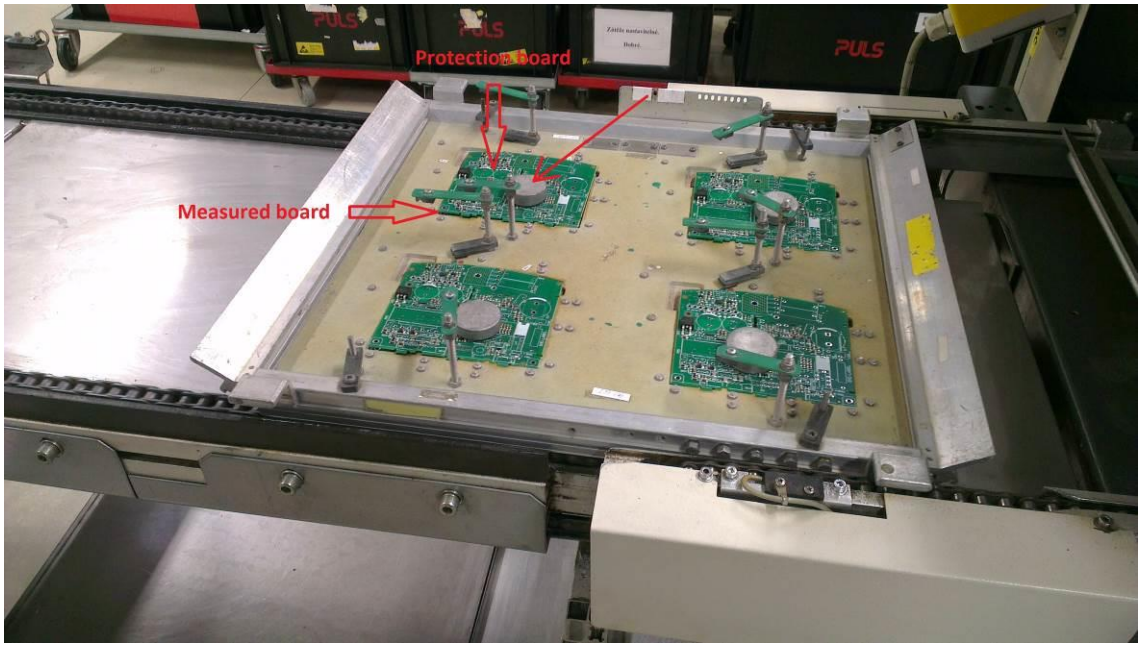
Goal is measurement of ionic contamination of board A, Zestron resin test, zestron flux test and tinten test.

Notes:

Four samples – 3 measured for ionic contamination, last one taken for additional tests.

Boards went through standard process and manipulation. Boards were stored for around 14 days on stock.

Waving on hall A (Friday = before weekend's maintenance). Boards without THT, additional weight on (shielded by another boards – contamination protection), see Picture 20.



Picture 20: Process of soldering

Results:

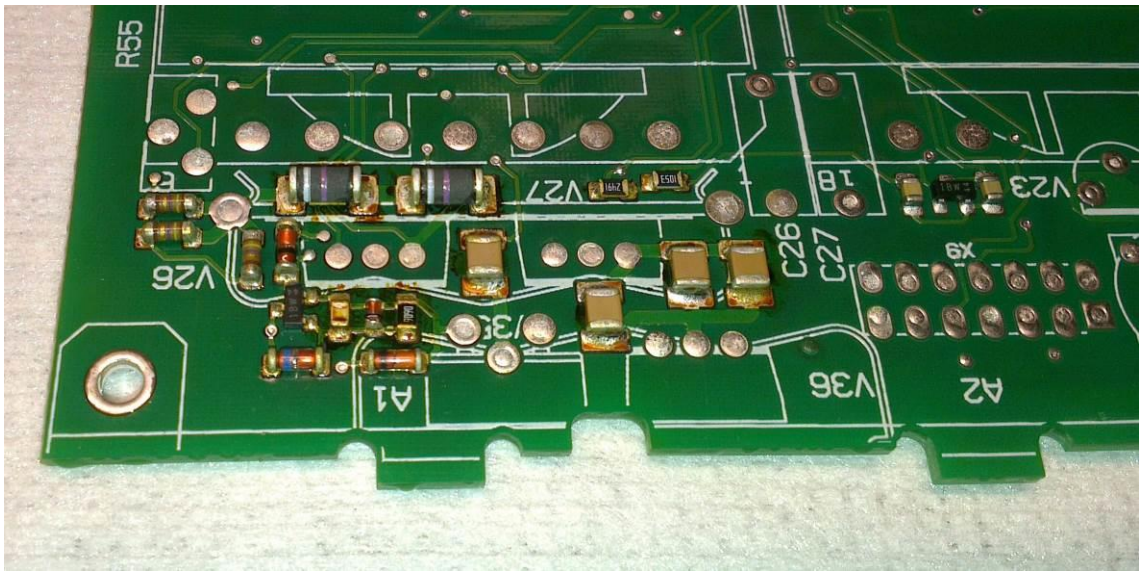
Contamination [µg . cm^{-2} EQ NaCl]				
1	2	3		µ
10,55	10,04	10,22		10,27

Table 15: Contamination results

Solder waved board A – Contamination:

Surface tension [mN/m]	
TOP	BOT
35	44

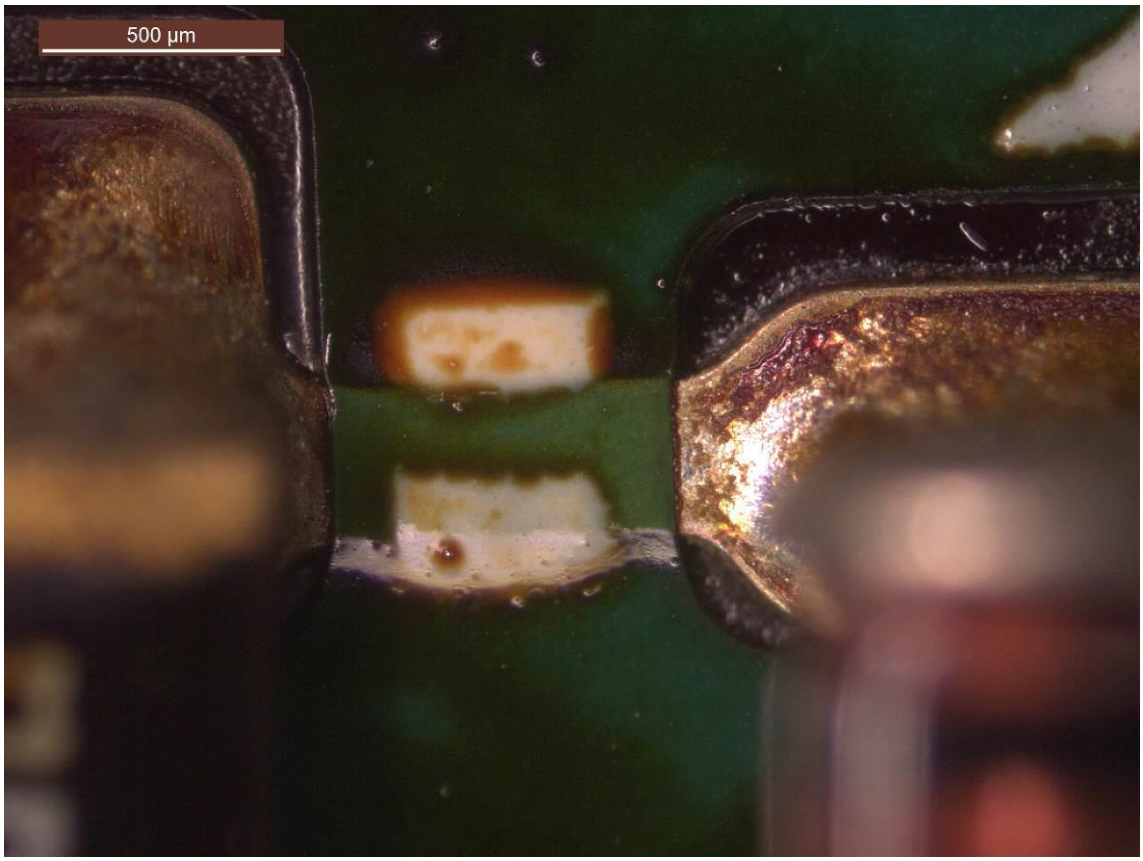
Table 16: Surface tension (tinten test)



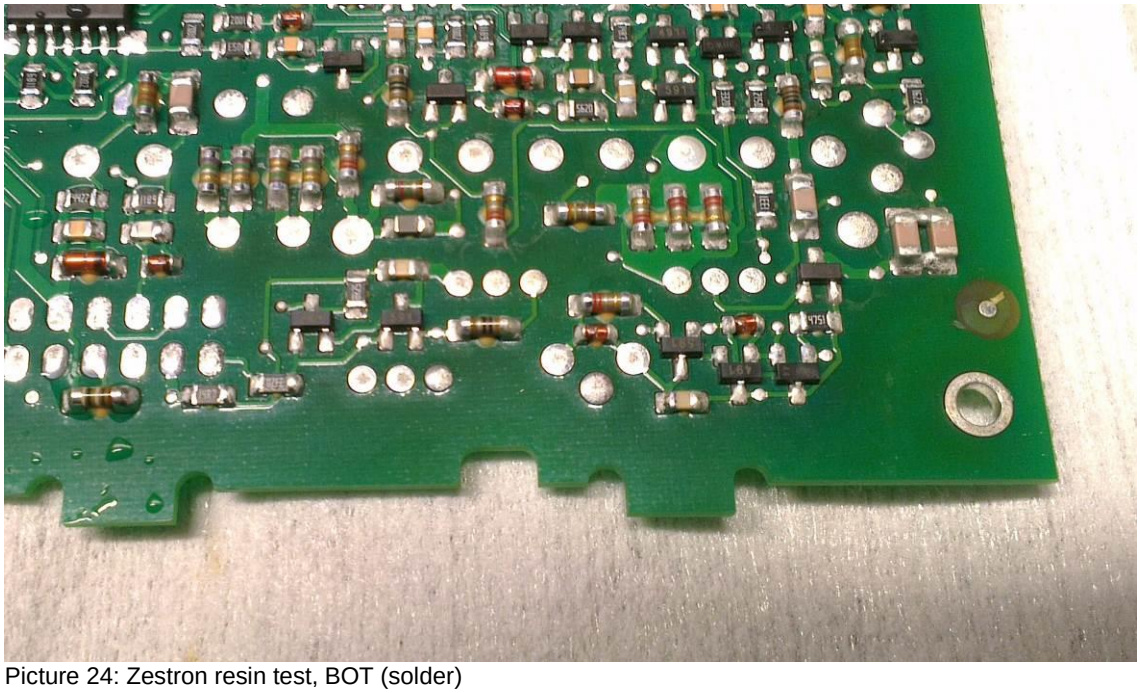
Picture 21: Zestron resin test, TOP (paste)

Picture 22: Zestron resin test, TOP (paste)

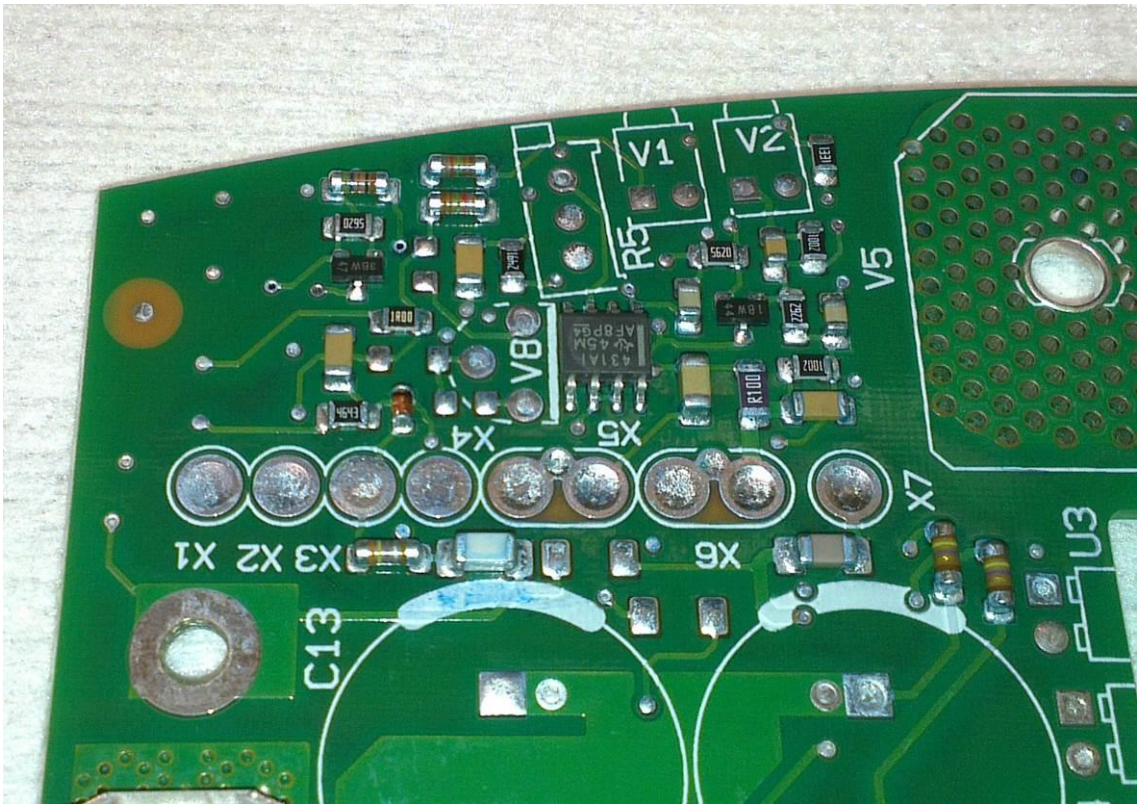
Solder waved board A – Contamination:



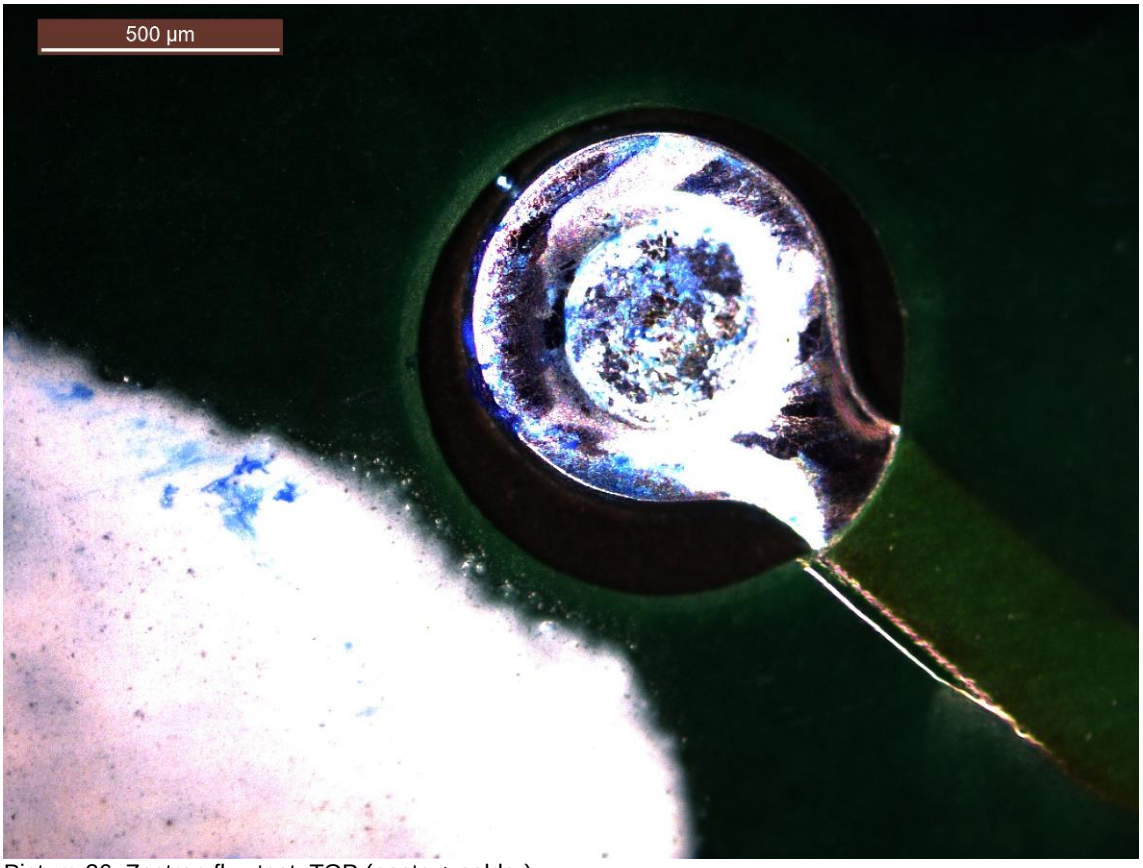
Picture 23: Zestron resin test, TOP (paste)


Picture 24: Zestron resin test, BOT (solder)

Solder waved board A – Contamination:

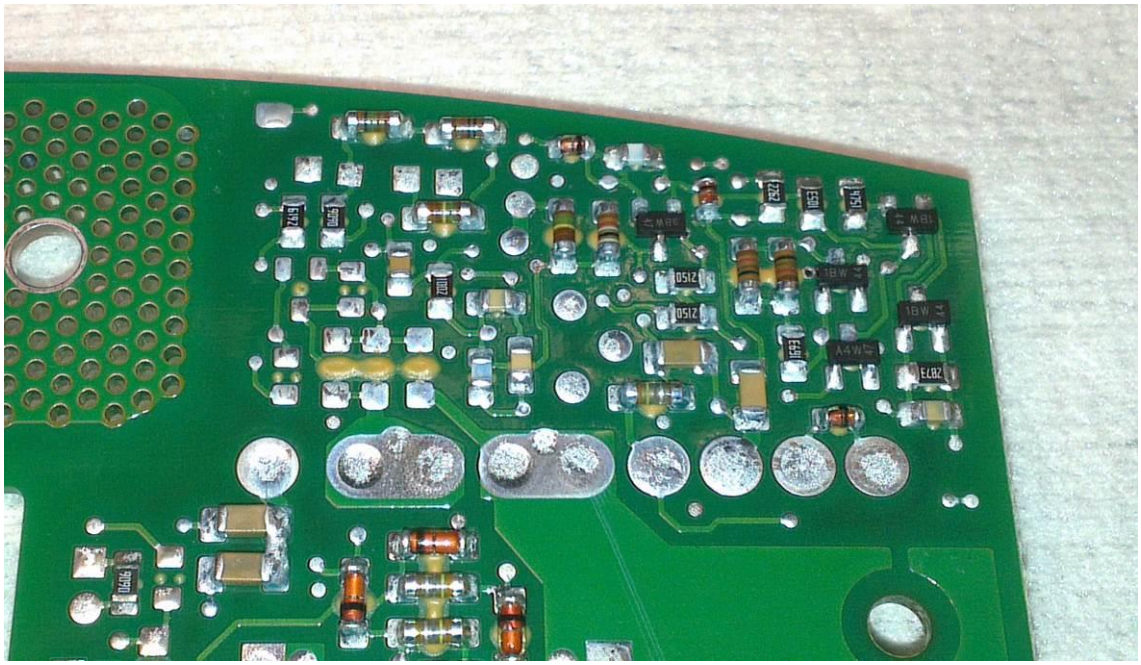


Picture 25: Zestron flux test, TOP (paste + solder)

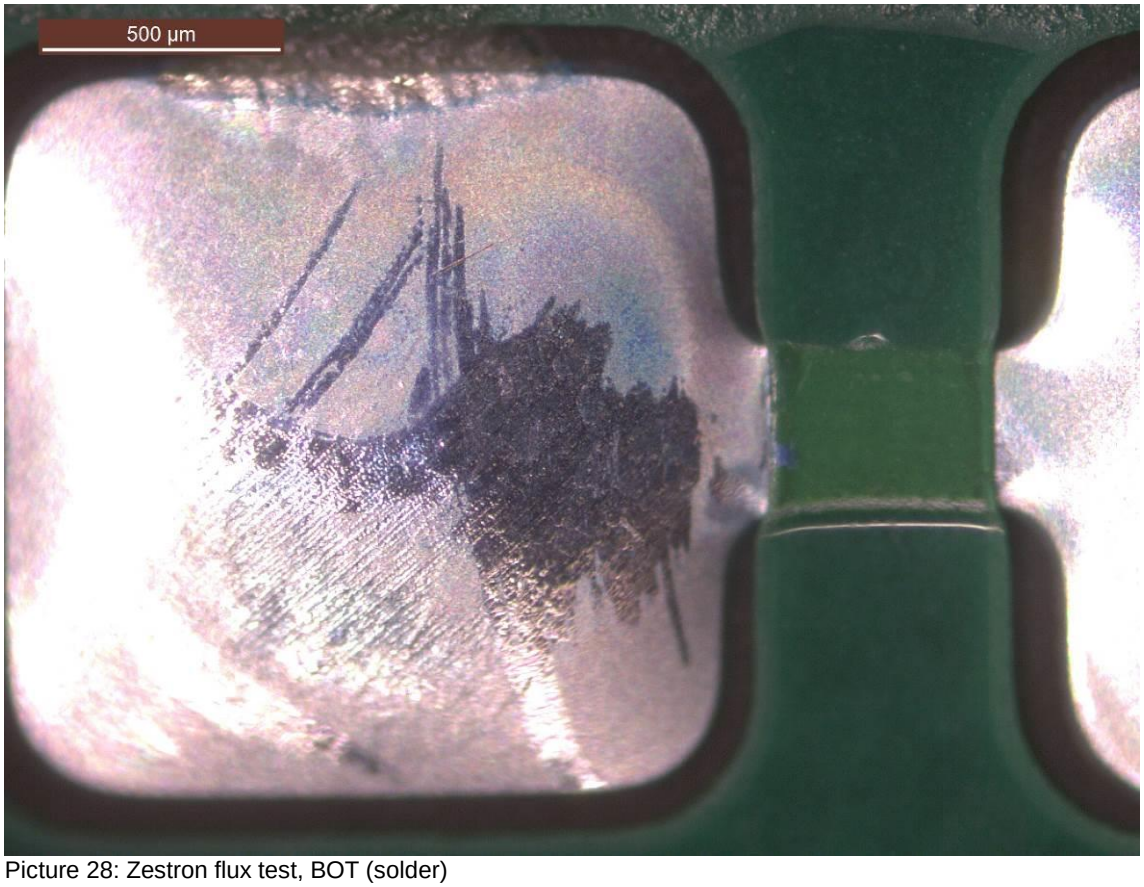


Picture 26: Zestron flux test, TOP (paste + solder)

Solder waved board A – Contamination:

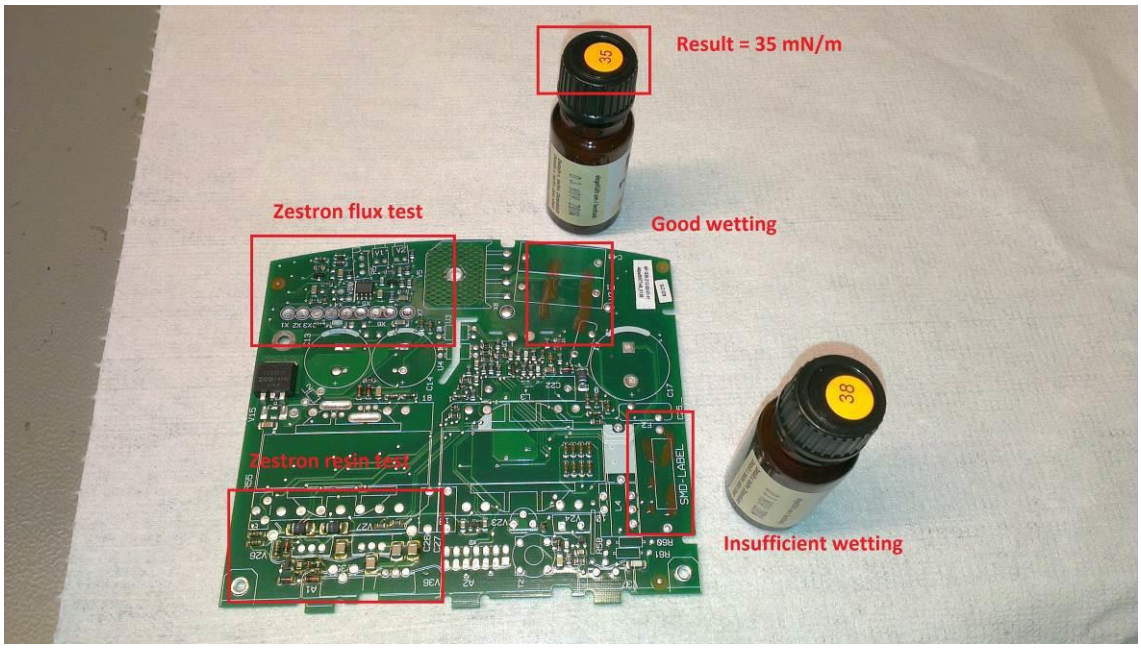


Picture 27: Zestron flux test, BOT (solder)

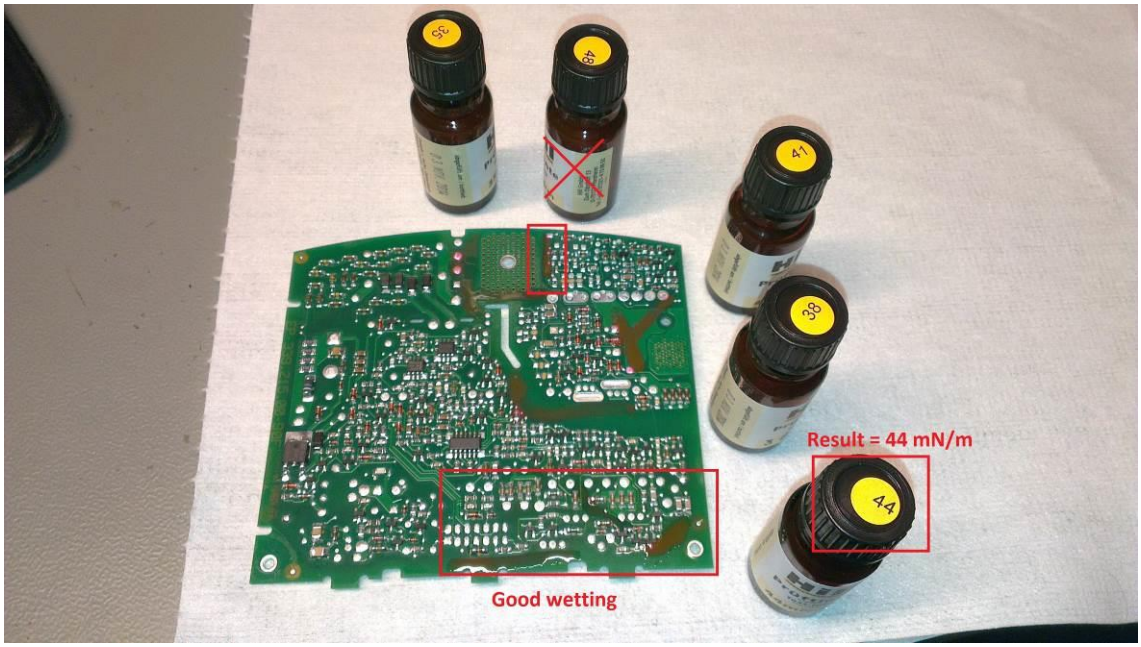


Picture 28: Zestron flux test, BOT (solder)

Solder waved board A – Contamination:



Picture 29: Tinten test, TOP (reflowed)



Picture 30: Tinten test, BOT (soldered)

Evaluation:

This board is heavily contaminated. It does not look like, that contamination came from SMD process. Issues with flux residues are not regular and solder wave process is considered free of those issues. Every clue pointed toward maintenance would solve this. This matter is going to be deeply evaluated in the future, as SMD was first priority.

CCQ – 0 – General introduction:

Requirement/Specification:	Result/Measurement:	Status:
See dedicated chapters	See dedicated chapters	 ACCEPTED

Dense sum:

Qualification of first product is finished

General qualification is going to be finished after:

- IPC boards are evaluated
- Boards from EPN are examined (during another product evaluation)
- HT compatibility during product, that require such abilities
- Process audit
- External (outsourced) companies finish their testing

Possible improvements:

Contamination

- Ionic contamination added during reflow and soldering process
- Resin residues added by reflow
- High surface tension of the board

Cleanliness

- Handling
- Possible gloves
- Protect the product from hairs, dust, particles and other impurities

Uniformity and thickness

- Lower variance of the thickness
- Keep thickness within tolerances (lower – safety, upper – wrinkles, adhesion, quality and therefore – safety)
- Lower thickness to lower the process costs

Step:	Prerequisite:	Status:	Specification:	Result:	OK/NOK:	Finished:	>= RTT:
1 - Color	Boards with varnish	Tests are finished.	Coloriess, transparent, flourescent (acc Datasheet from Peters, varnish SL 1307 FLZ 234)	Coloriess, transparent, fluorescent (single and double coating)	OK	23.10.2014	Delivered (batch from RTT) is OK.
	"Paper" with varnish						
2 - Viscosity	DIN 53211 or DIN EN ISO 2431 cup	First test was done on 21/10/14 (varnish 02/15, LOT 1-304-1-605492), second @ 19,8 °C on 22/10/14, unless requested tests are finished	Acc DIN 53211, 4 mm Cup : 23 +/- 2 s @ 20 °C	27,0 26,2 26,5 s = 26,6 s @ 21 °C 29,4 29,1 28,6 = 29,0 s @ 19,8 °C	NOK (conditionally accepted)	22.10.2014	Viscosity is lower. See results down. RTT uses SL 1306.
3 - SL 1307 HT Compatibility	Lacquer						
4 - Process audit	Programs are done, other specifications are either met or conditionally accepted						
5 - Zestron tinten test	Boards from stock, after SMD and completely assembled, compare test between different boards suppliers needs to be either approved to be done on different boards or same boards need to be ordered	Tests were done on each board	Surface tension is high enough (specify) - note > 40 mN/m The surface energy of the laminate or solder resist can have a huge impact on the ability of the conformal coating to stick or adhere. To achieve the optimum adhesion, it is necessary to ensure that the the surface energy of the substrate is above that of the conformal coating material to be applied. Zestron specifies > 40 mN/m.	Lowest results are 30 mN/m WLP and RLP between 35 and 41 mN/m.	OK (Process limits will be set accordingly, long term testing necessary)	10.11.2014	Applies to RTT, same conditions for both.
6 - Zestron resin test			No resin residues are found and contamination is within range or residues are found but lacquer is adhesive enough, 1,56 µm.cm-2 EQ NaCl	Residues found on RLP sides, WLP is fine, also soldering is clean	NOK conditionally ok	11.11.2014	
7 - Zestron flux test				Boards are clean, free of flux residues	OK	11.11.2014	
8 - Ionic contamination				Module boards are more contamined	NOK (stable results)	11.11.2014	

Table 0-1: General tests for lacquer and boards

CCQ – 0 – General introduction:

Step:	Prerequisite specification:	Status:	Specification:	Result:	OK/NOK:	Finished:	>= RTT:
9 - Uniformity, coverage	Boards with varnish	Uniformity is very low (variance is high), coverage of SMDs and terminals is not enough	Any voids, holes, wrinkles, streaks, cracking, delamination, blistering, or peeling of coating or other evidence of loss of adhesion, or discoloration of conductors shall be reported. Any legends shall be clearly visible through the coating.	Few impurities (3-10 mm long hairs) c. variance is 13,2/29,2 %	OK	24.10.2014	Equality is very high, lot better than our. This was improved. Bubbles and fingerprints on RTT.
	"Paper" with varnish			Few impurities (3-10 mm long hairs) c. variance is 12,6 %	OK	24.10.2014	
	Manufactured boards			AP-339.250.00-01 is highly uneven, it can be spotted even visually without microsectioning	NOK (AP-339.250.00-01, see 10-Thickness)	28.11.2014	
10 - Thickness	Boards with varnish	Most of the surface has thickness high enough (except for SMDs edges)	30 - 130 µm in dry state	Microsection 40,4 µm @ σ = 11,8 µm; Ultrasonic 47,6 µm @ σ = 6,3 µm	OK	24.10.2014	Manufactured boards and lacquered by RTT has thickness from 17 to 33 µm; Our are more thick
	"Paper" with varnish			Weighted thickness 45,9 µm Microsection 55,7 µm @ σ = 7,0 µm	OK	24.10.2014	
	Manufactured boards			AP-339.250.00-01 has high variance. Even 0 µm on SMD edges, on SMD top, SMD contact has high thickness, board is very uneven 8 µm up to 200 µm (30.10.14)	NOK (Upper and lower limits, > 130 µm - on plain board)	28.11.2014	
11 - Adhesion (mash cut)	Boards with varnish	Boards succesfully passed, base copper ones and specified ones, where assemblies do not prevent testing.	Result 0, 1, 2 ... acc DIN 2409 specification (smallest area torn away)	Result is class 0 (perfect) Although some minor adhesion issues came up on microsection.	OK	11.11.2014	Varnish (on assembled board) meets the required specification - class 0.
	Manufactured boards						
12 - High voltage test	ipc boards	Boards succesfully passed.	HV tester WEK-LABCZ or Stanek, test done by continuous and constant voltage growth. 100 kV/mm	Result is 90 kV/mm.	OK	9.12.2014	Both are PASS
13 - Adhesion (tape test)	Manufactured boards	Boards succesfully passed, base copper ones and specified ones, where assemblies do not prevent testing.	No varnish remains on tape, see 11 - Adhesion	Class 5 with one except, that was class 4 (double layer on copper board).	OK	11.11.2014	Varnish (on assembled board) meets the required specification - class 5.
14 - Double coating	ipc boards	Boards succesfully passed.	See 9 - Uniformity, coverage + 11 + 12 + 13 + Voids and issues on the transition are not present	All requirements are met.	OK	29.11.2014	Only specific tests are microsection analysis for proper bonding, deeper thickness evaluation and extended
	Boards with varnish	Tests were done, thickness can be very high (up to 250 - 300 µm). With proper programming most of the issues were overcome.			OK		
	"Paper" with varnish						
	Manufactured boards						

Table 0-2: Specific experiments

Additional experiments:

Step:	Prerequisite:	Status:	Specification:	Result:	OK/NOK:	Finished:	>= RTT:
1 - Color (SL 1306 N FLZ aging)	Enough time or using difference	Testing was done on lacquer, that has been used by repairmen on daily for 30 - 60 minutes since the fall of August (circa 2 months).	Color stability	Color is same	OK	22.10.2014	1306 lacquer, not compared to 1307.
2 - Viscosity (SL 1306 N FLZ aging)			Viscosity is within specified tolerance even after prolonged period of time. For SL 1306 FLZ N 23 and 4 mm cup, it is 60 +/- 5 s.	72,0 75,4 76,2 = 74,5 s 155,3 155,3 157,0 = 155,9 s @ 19,8 °C	Aging is relevant	22.10.2014	
10 - Thickness	THT - coating	Tested	30 µm +20/-5 µm in dry state	0 µm at edges	NOK	7.11.2014	Not passed by either.

Table 0-3: Additional experiments

Step:	Specification:	Result:	OK/NOK:	>= RTT:
1 - Color	Colorless, transparent, flourescent (both)	Colorless, transparent, fluorescent (single and double coating)	OK	PASS
2 - Viscosity	Acc DIN 53211, 4 mm Cup : 23 +/- 2 s @ 20 °C; 60 +/- 5 s in case of SL 1306	1307: 27,0 26,2 26,5 s = 26,6 s @ 21 °C 29,4 29,1 28,6 = 29,0 s @ 19,8 °C 1306: 72,0 75,4 76,2 = 74,5 s @ 19,8 °C	OK	PASS
9 - Uniformity, coverage	Any voids, holes, wrinkles, streaks, cracking, delamination, blistering, or peeling of coating or other evidence of loss of adhesion, or discoloration of conductors shall be reported. Any legends shall be clearly visible through the coating.	Inequality in CC was improved. Too thick layers, which cause wrinkles were thinned. Edges must be improved (both sides). RTT has many more issues - impurities, fingerprints.	OK	PASS
10 - Thickness	30 - 130 µm in dry state	PULS coating is over upper limit. High inequality. It was already improved, but additional improvements are desirable. Lacquered by RTT have thicknesses from 17 to 33 µm.	OK	PASS
11 - Adhesion (mash cut)	Result 0, 1, 2 ... acc DIN 2409 specification (smallest area torn away)	Result is class 0 (perfect) - both (RTT was only tested on assembled boards)	OK	PASS
12 - High voltage test	100 kV/mm	Result is 93 kV/mm, passed basic HV test.	OK	PASS
13 - Adhesion (tape test)	No varnish remains on tape, see 11 - Adhesion	Class 5 with one except, that was class 4 (double layer on copper board). Limited test on RTT meets the criteria.	OK	PASS
14 - Double coating	See 9 - Uniformity, coverage + 11 + 12 + 13 + Voids and issues on the transition are not present	All requirements are met.	OK	Only specific tests are microsection analysis for proper bonding, deeper thickness evaluation and extended adhesion experiments.

Table 0-4: >= RTT

CCQ – 1 - Color:

Requirement/Specification:	Result/Measurement:	Status:
Colorless, transparent, fluorescent (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)	Colorless, transparent, fluorescent	 PASS

Specification:
Colorless, transparent, fluorescent (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)

Result:
Colorless, transparent, fluorescent

Methods, test:
Visual inspection, under „bulbs + fluorescent tubes“ and „UV light“

Inspected single and double conformal coating layers

Based on paper and copper.

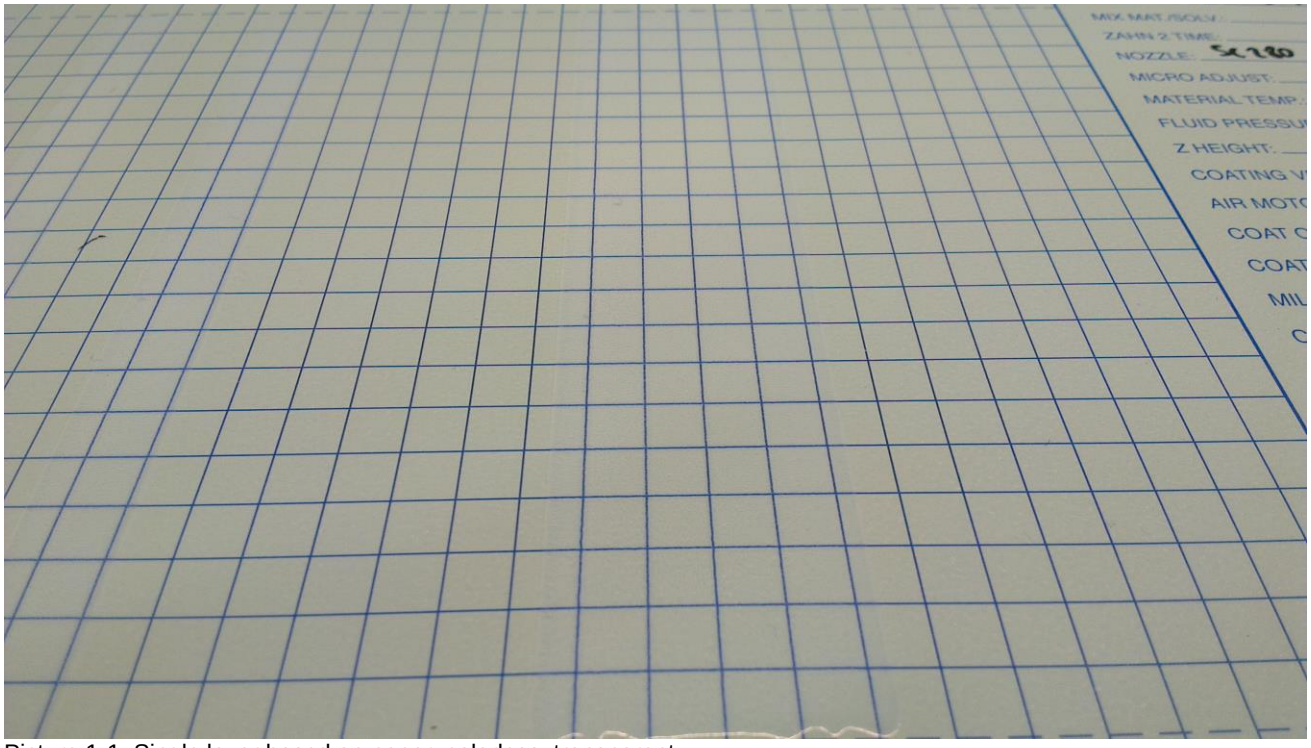
Documentation:
Batch: usability till 02/15, LOT 1-304-1-605492

Evaluation:
Results reflect specified characteristics. Neither paper, copper or double layer affect result.

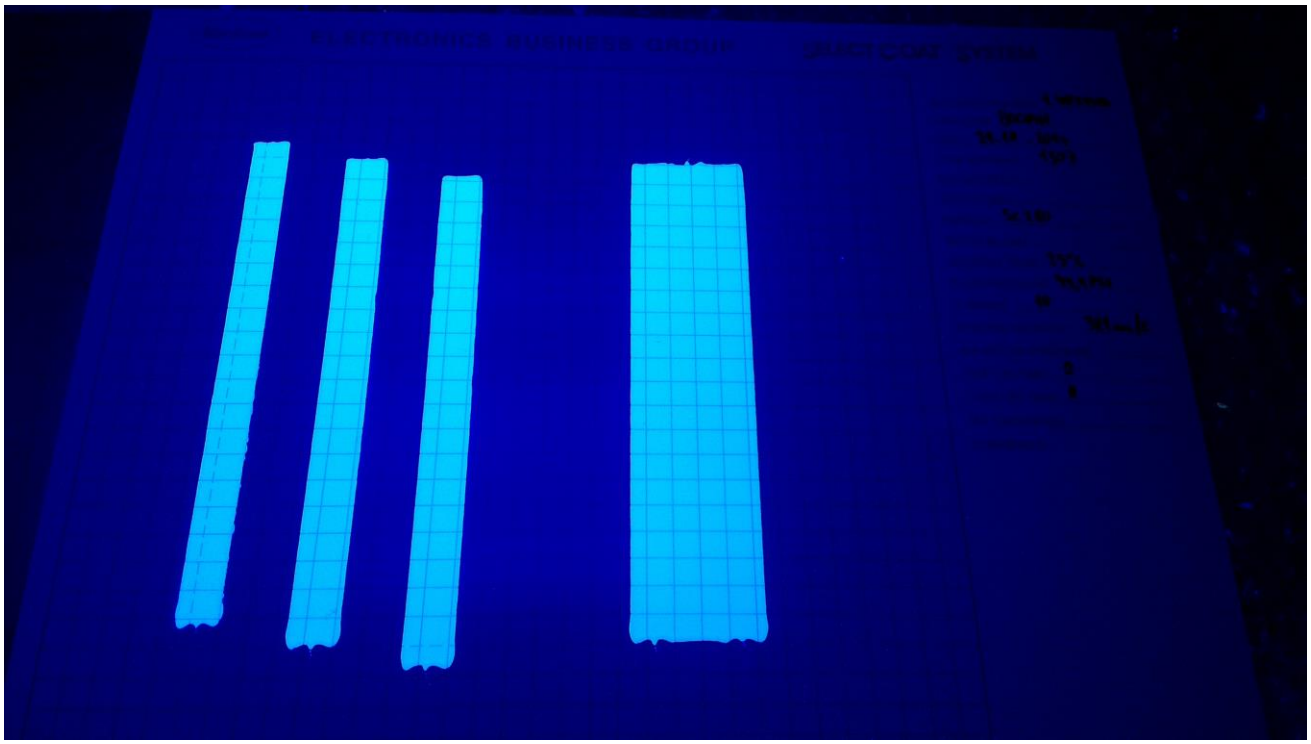
Conclusion is **PASS/OK**.

CCQ – 1 - Color:

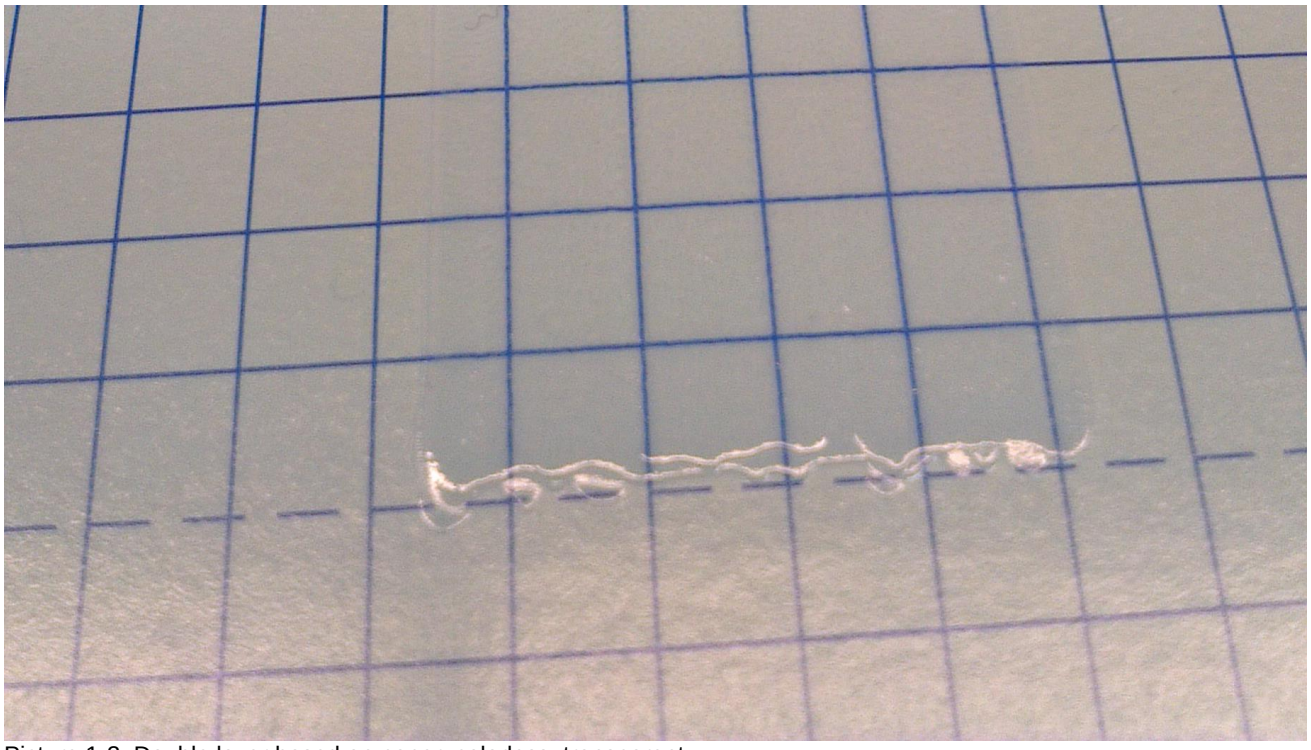
Attachments:



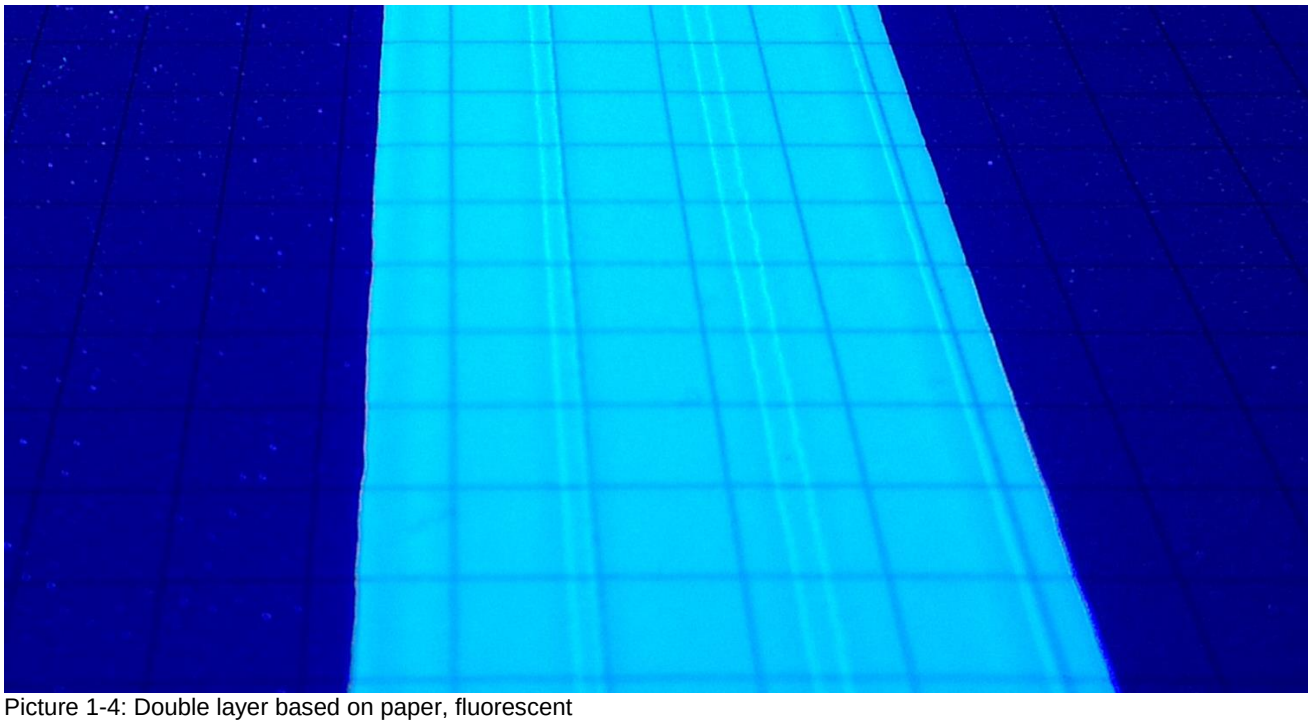
Picture 1-1: Single layer based on paper, colorless, transparent


Picture 1-2: Single layer based on paper, fluorescent

CCQ – 1 - Color:

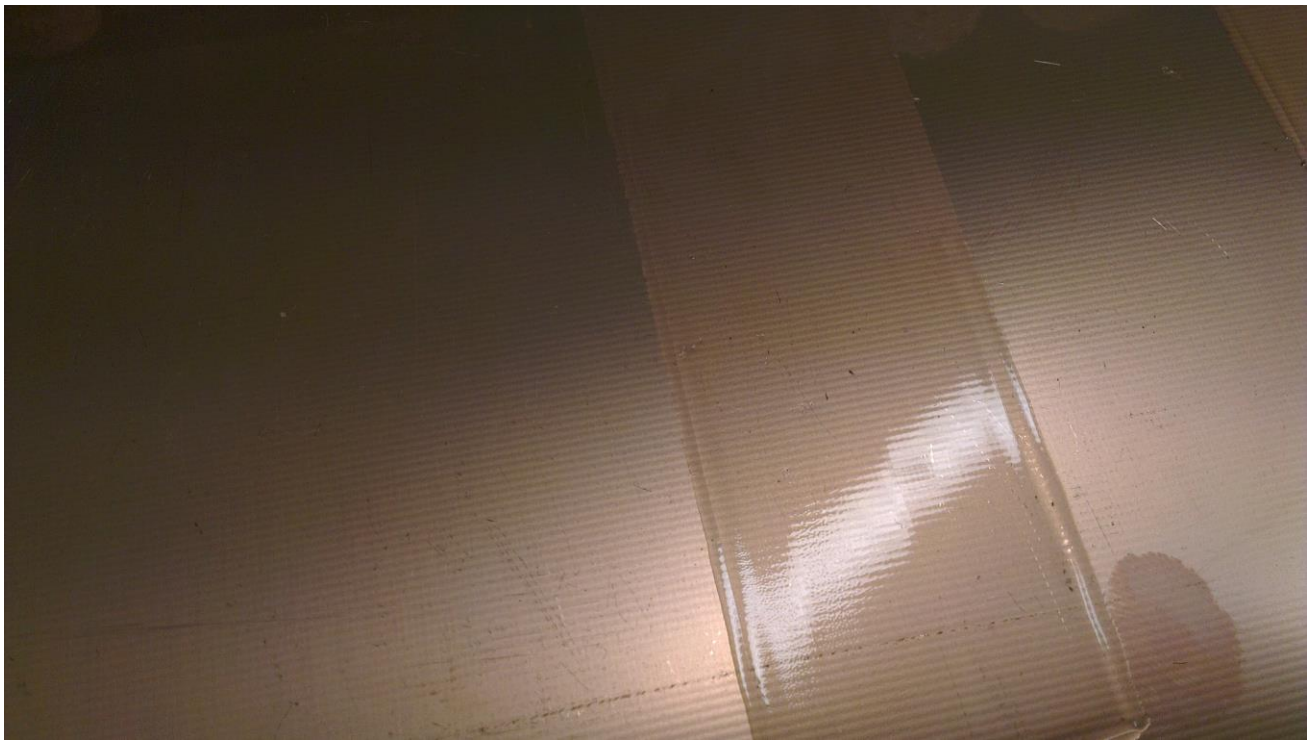


Picture 1-3: Double layer based on paper, colorless, transparent



Picture 1-4: Double layer based on paper, fluorescent

CCQ – 1 - Color:



Picture 1-4: Double layer based on copper

CCQ – 2 - Viscosity:

Requirement/Specification:	Result/Measurement:	Status:
ISO 2431, 4 mm Cup : 23 +/- 2 s @ 20 °C (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)	26,6 s @ 21,0 °C 29,0 s @ 19,8 °C	 CONDITIONALLY ACCEPTED

Specification:

ISO 2431, 4 mm Cup : 23 +/- 2 s @ 20 °C (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)

Result:

26,6 s @ 21,0 °C

29,0 s @ 19,8 °C

Methods, test:

ISO 2431, 4 mm Cup

Cup is filled to the edge with the lacquer. Cup has hole in the bottom. Time starts counting from the moment varnish is released till the first flow interruption. Time reflects viscosity. It is inversely proportional.

Documentation:

Batch: usability till 02/15, LOT 1-304-1-605492

Evaluation:

Viscosity is function of temperature. Because it is hardly controllable, two were used to properly determine the result. Varnish is less viscous than specified. It is still **conditionally accepted**.

(Nonconformity is minor, does not affect our ability to apply varnish properly.)

Attachments:

Viscosity [s]	
Temperature = 21,0 °C	Temperature = 19,8 °C
27,0	29,4
26,2	29,1
26,5	28,6
26,6 s	29,0 s

Table 2-1: Viscosity results

CCQ – 2 - Viscosity:

Picture 2-1: DIN 53211, 4 mm Cup

CCQ – 5 – Tinten test: (SH)

Requirement/Specification:	Result/Measurement:	Status:
Surface tension of the board > 40 $mN.m^{-1}$ (acc. Zestron)	30 – 41 $mN.m^{-1}$	 Our standard needs to be properly specified.

Specification:

Surface tension of the board is specified as > 40 $mN.m^{-1}$ (Schweigart, Helmut. EPP EUROPE SEPTEMBER / OCTOBER 2007. How clean do assemblies have to be?)

Result:

Results are not stable in a process. In general EPs are 30 – 35 $mN.m^{-1}$ while assembled boards has surface tension of 35 – 41 $mN.m^{-1}$.

Methods, test:

Test is based on finding the liquid with specified surface tension that does not wet the board anymore. Picture 5-2 note, that dynamic behavior is inspected.

Documentation:

Product A

Suhang boards

Evaluation:

Critical is value before coating as surface is wetted with liquid while it's surface tension is lower than board's. Flux and cleaning the board rises the value, in a minor way, similar to the results. Standard for our boards and process needs to be adjusted. (See other qualification steps for informed decision.)

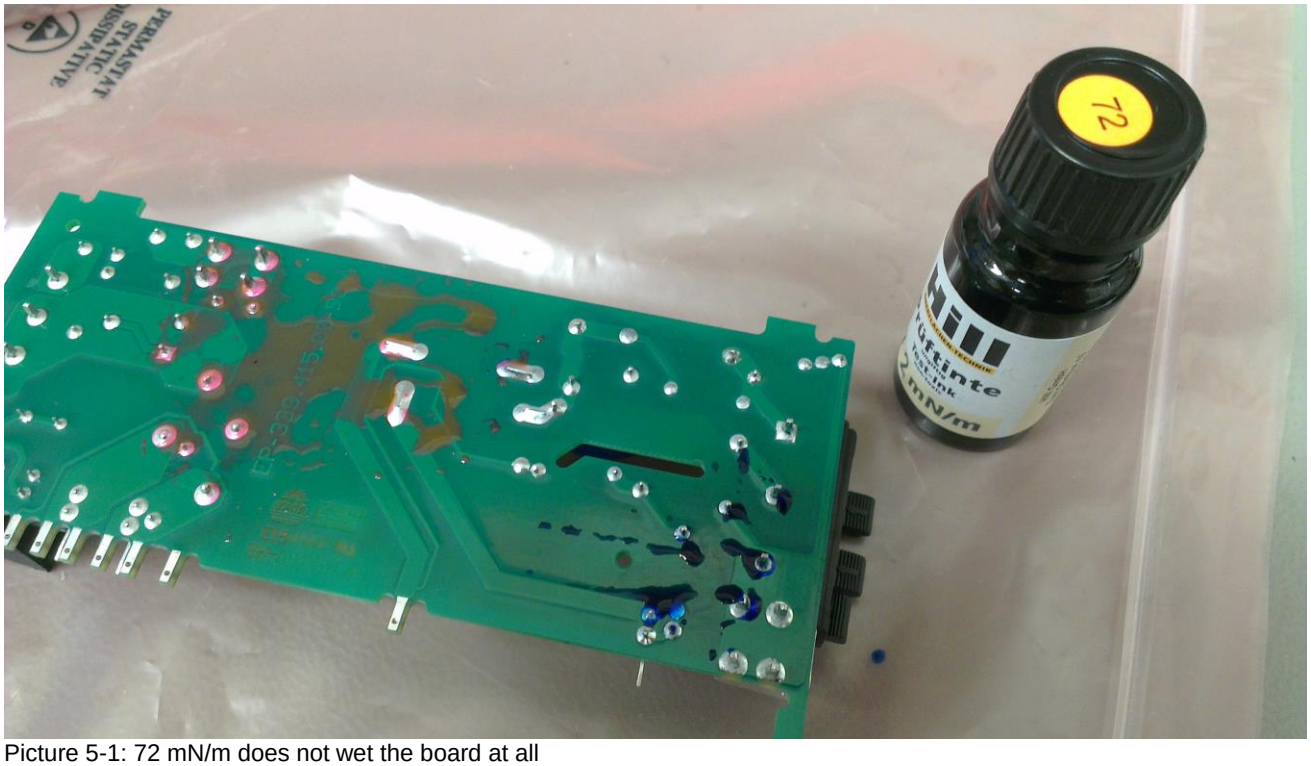
Picture 5-1 shows that 72 mN.m-1 tinten does not wet the board. It is similar value to the tap water. While 30 $mN.m^{-1}$ is not issue, it is closer to the ethanol. In this case we can not clean the boards with water. It would be ineffective, while the adjusted liquid with alcohol would be able to.

CCQ – 5 – Tinten test: (SH)

Attachments:

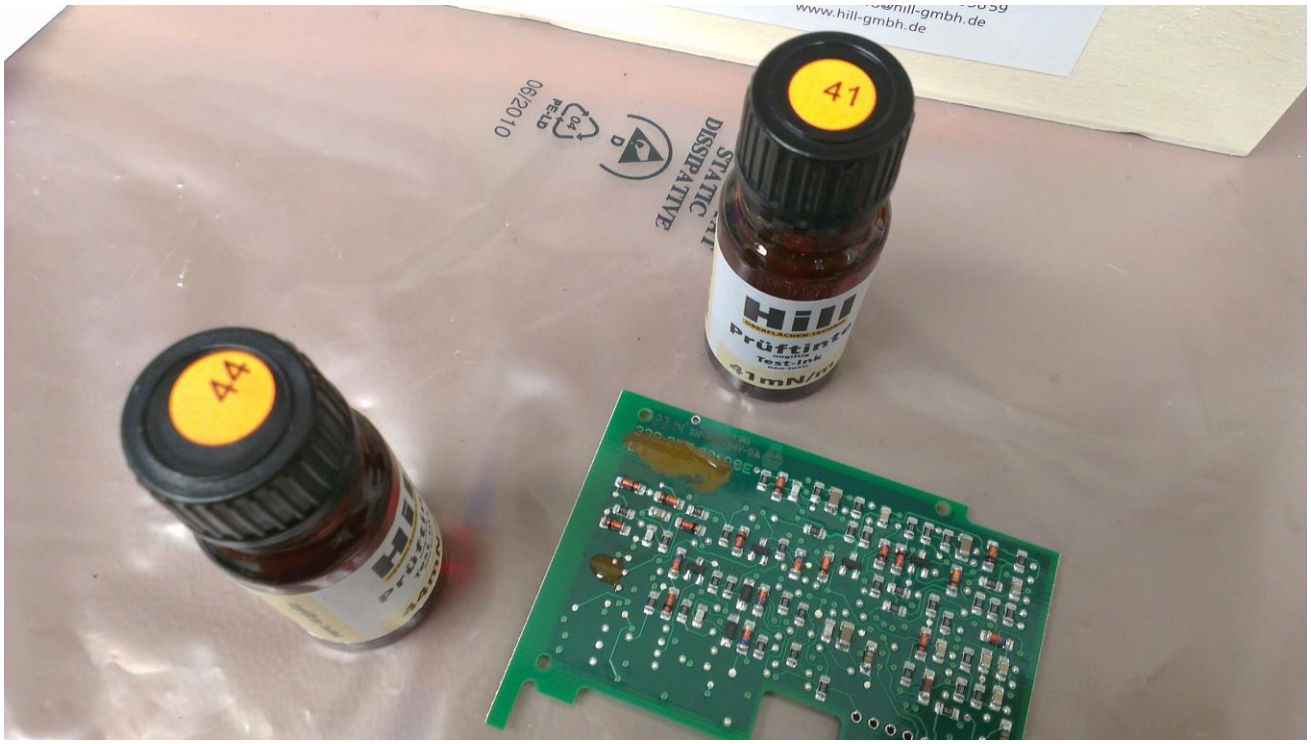
Partnumber:	Surface tension [mN/m]	
Delivered board A		38
Board A	RLP	38
Board A	WLP	41
Board A	WLP	38
Delivered board C		35
Board C	RLP	38
Board C	RLP	38
Delivered board K		30
Board K	Wave	35

Table 5-1: Tinten test results



Picture 5-1: 72 mN/m does not wet the board at all

CCQ – 5 – Tinten test: (SH)



Picture 5-2: Difference between 41 and 44 mN/m

CCQ – 6 – Zestron resin test: (SH)

Requirement/Specification:	Result/Measurement:	Status:
Test is negative. Test liquid does not indicate any resin residues.	Test is positive. (See table 6-1)	✗ FAIL

Specification:
Test is negative. Test liquid does not indicate any resin residues.

Result:
Test found residues after SMD. Paste leaves residues on the board. Wave soldering does not leave any traces of resin.

Methods, test:
Zestron resin test is applied on the board. After 3 minutes is washed away with demineralized or deionized water. Brown or yellow spots indicate residues.

Documentation:
Product A

Suhang boards

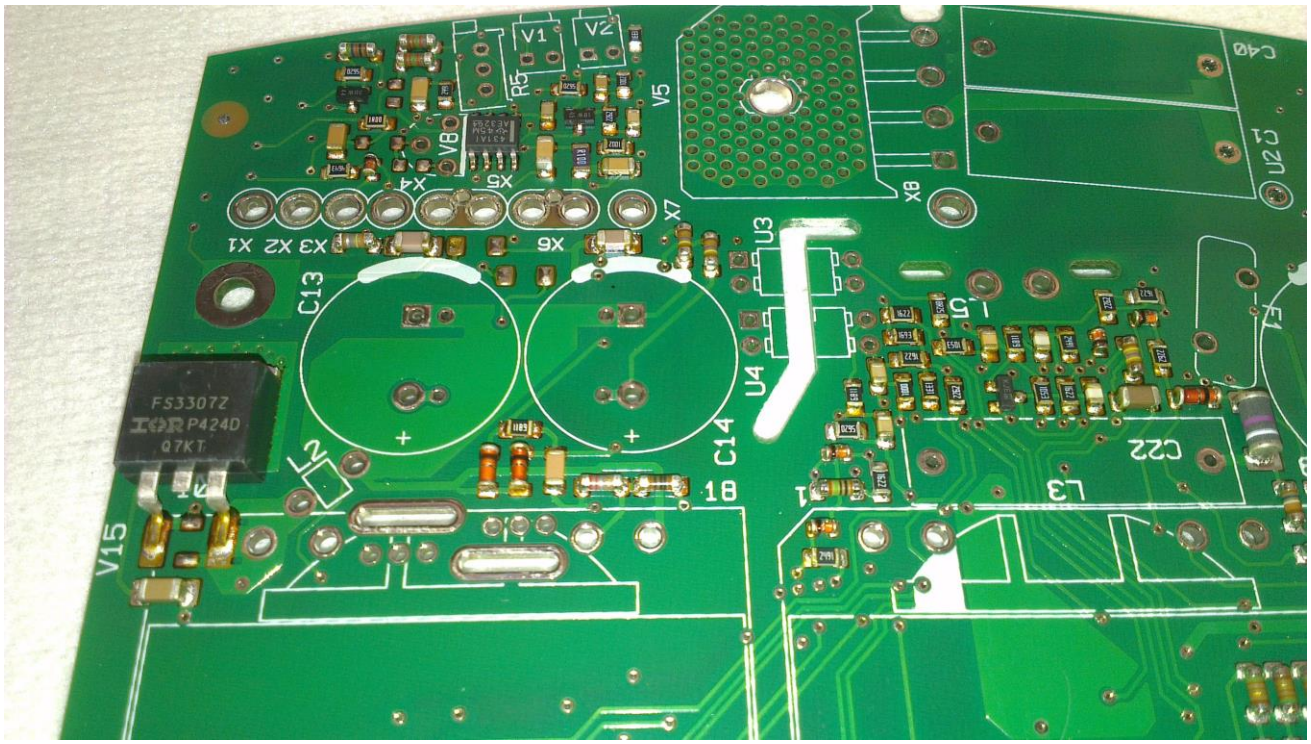
Evaluation:
Our production shows tendencies in this matter. While there were not any in May 2014, when similar test was run (different boards). In table, any **RLP is NOK**. Result is **FAIL**.

Attachments:

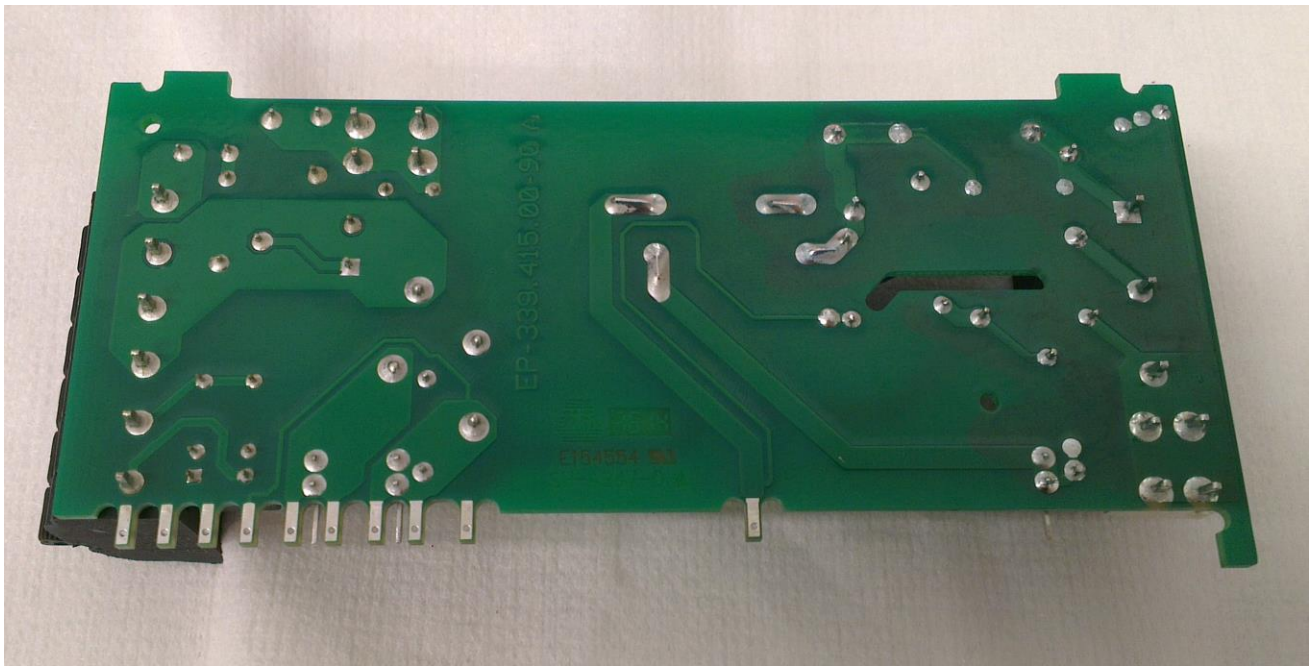
	Main		Module		Support
Clear	OK		OK		OK
SMD	NOK (RLP)	OK (WLP)	NOK (RLP)		-
THT	NOK (RLP)	OK (WLP)	NOK (RLP)	OK (solder)	OK

Table 6-1: Results

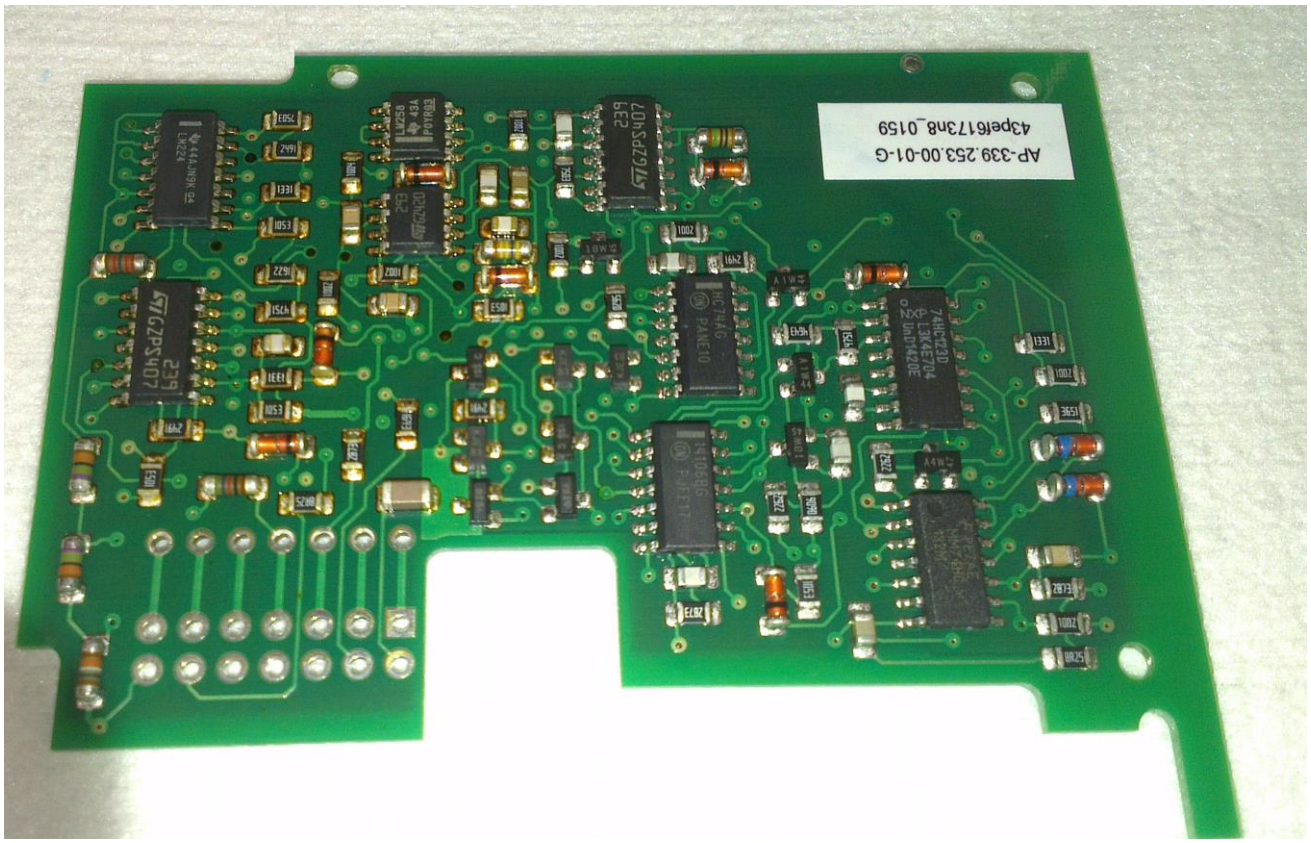
CCQ – 6 – Zestron resin test: (SH)



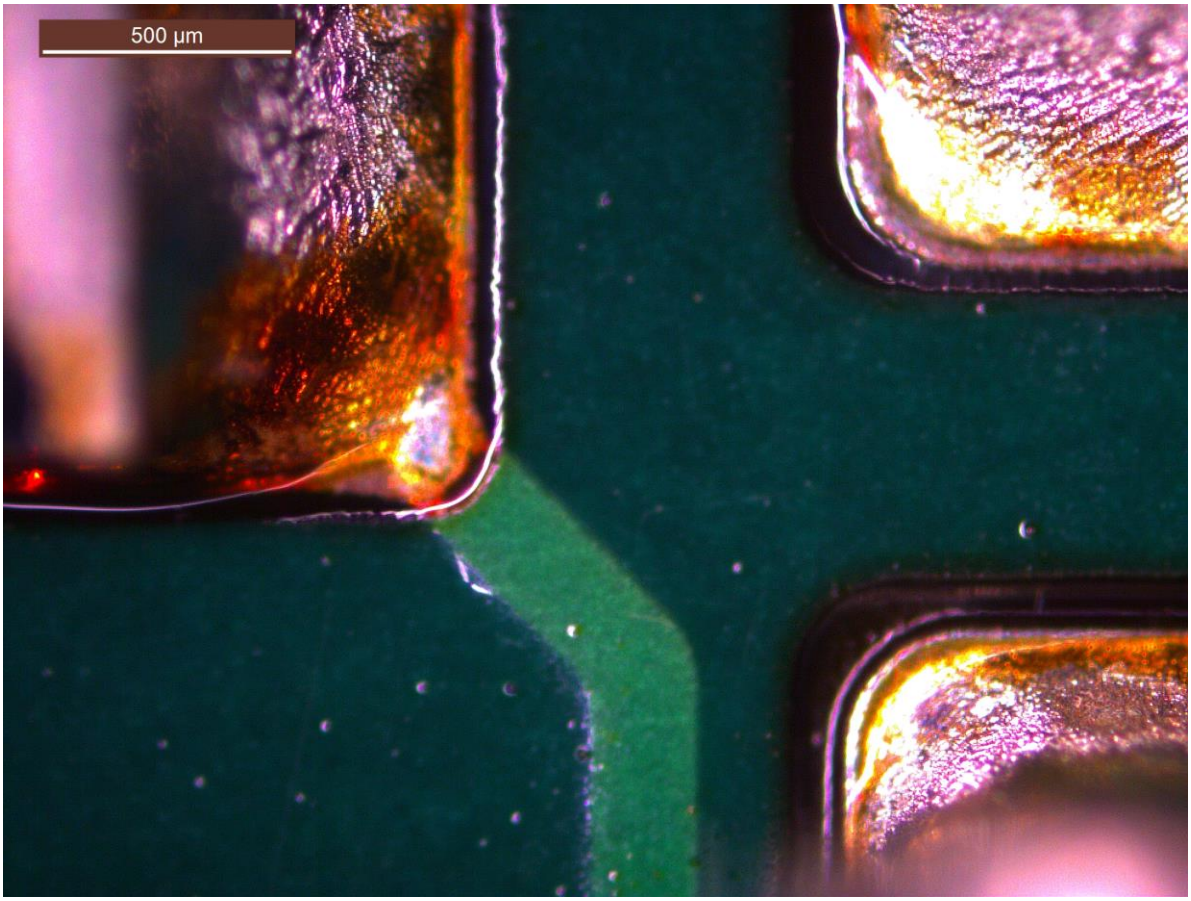
Picture 6-1: Areas on pads are contaminated


Picture 6-2: No indication of resin residues

CCQ – 6 – Zestron resin test: (SH)

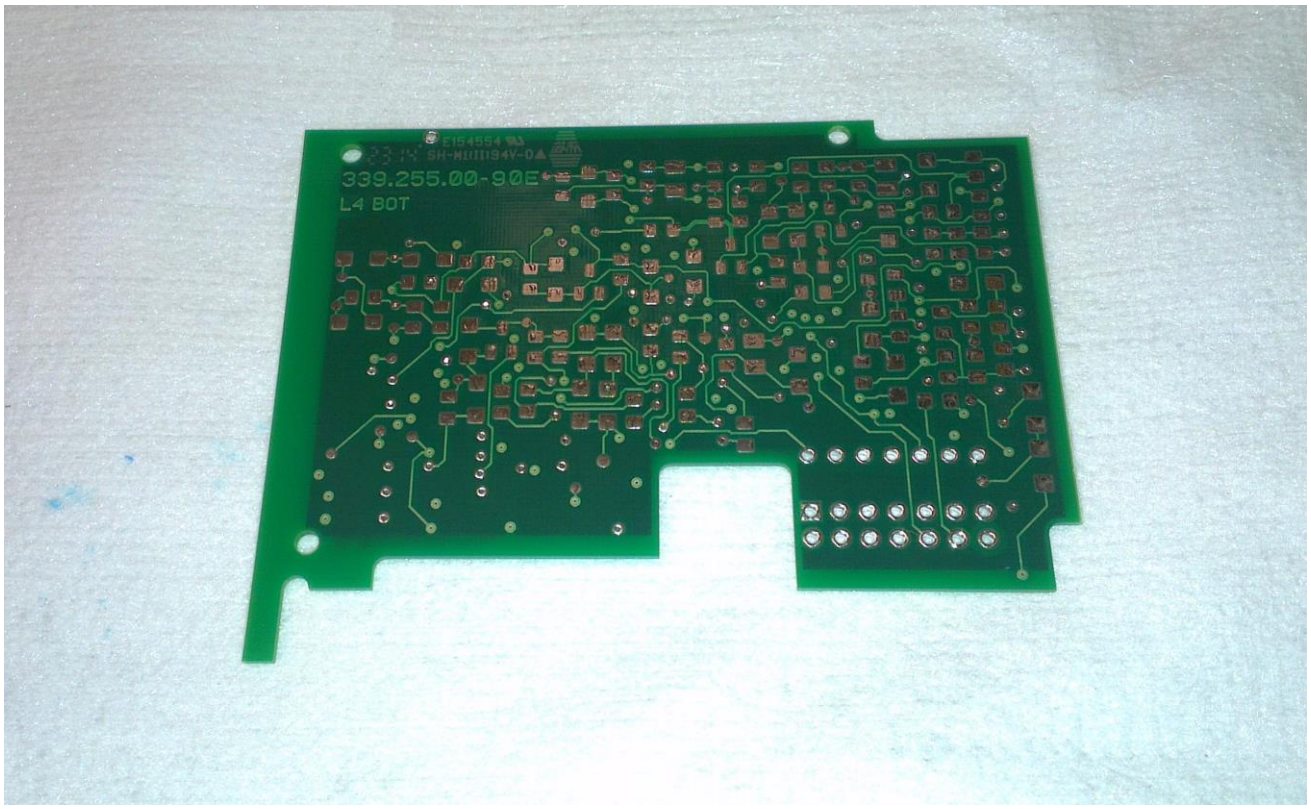


Picture 6-3: Resin test on left side (Flux test on right side – PASS)

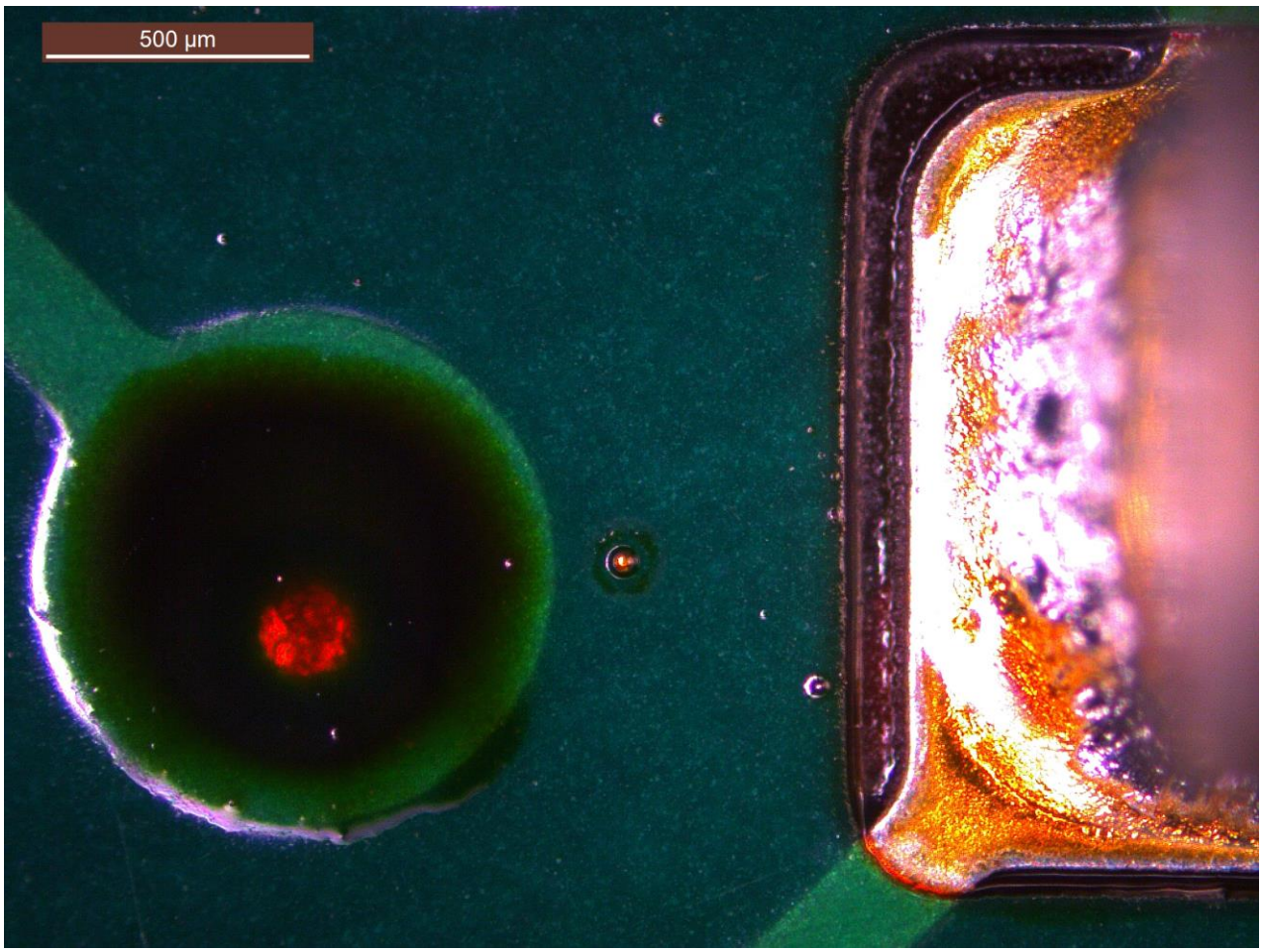


Picture 6-4: Microscopy detail

CCQ – 6 – Zestron resin test: (SH)



Picture 6-5: Delivered boards are OK



Picture 6-6: Microscopy detail

CCQ – 7 – Zestron flux test: (SH)

Requirement/Specification:	Result/Measurement:	Status:
Test is negative. Test liquid does not indicate any flux residues.	Test is negative.	 PASS

Specification:
Test is negative. Test liquid does not indicate any flux residues.

Result:
Test did not find any residues after SMD and wave soldering.

Methods, test:
Zestron flux test is applied on the board. After 1 minute test is washed away with demineralized or deionized water. Blue or white spots indicate residues.

Documentation:
Product
Suhang boards

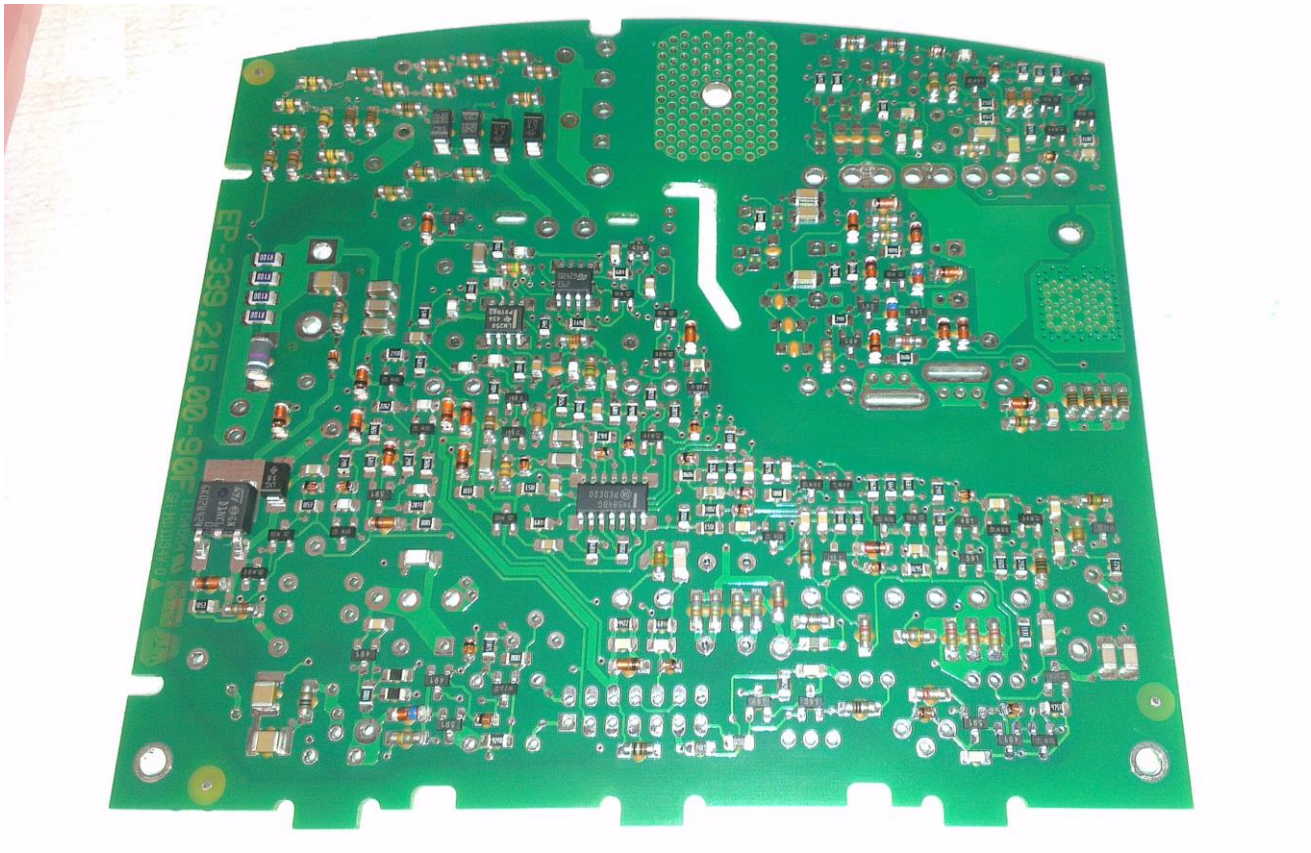
Evaluation:
Our production shows no tendency in this matter. Result is **PASS**.

Attachments:

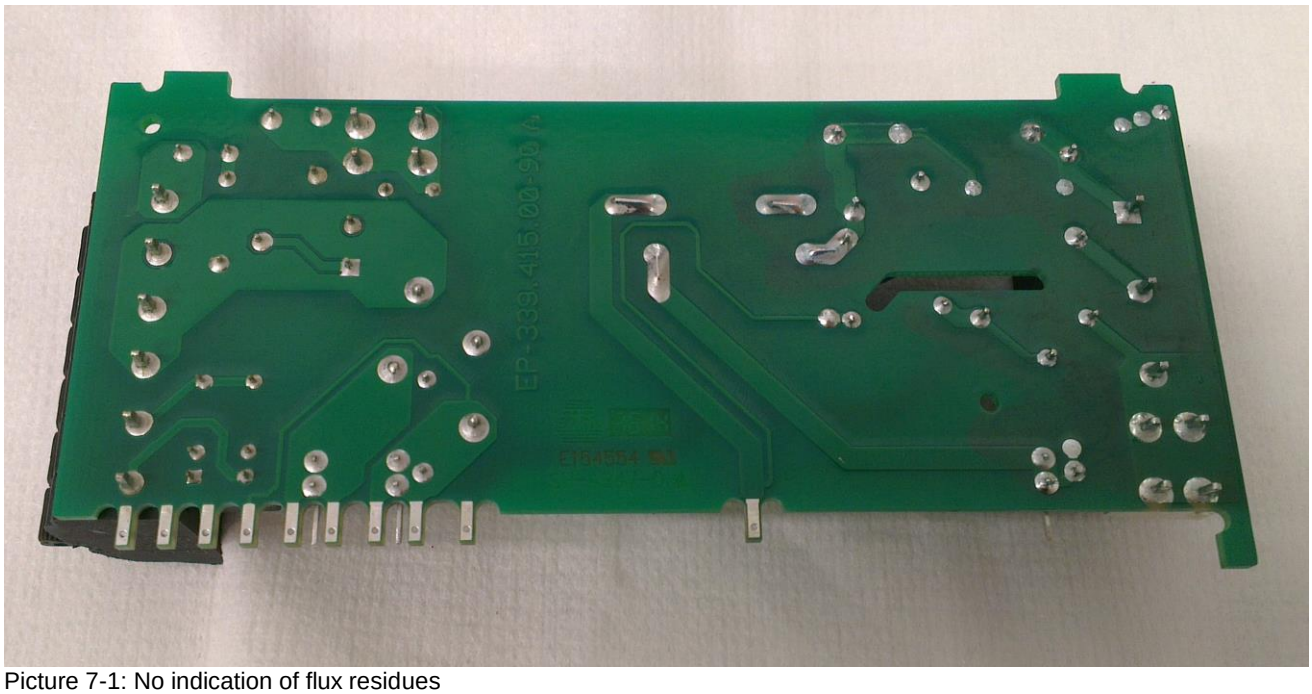
	Main		Module		Support
Clear	OK		OK		OK
SMD	OK	OK	OK	OK	-
THT	OK	OK	OK	OK	OK

Table 7-1: Results

CCQ – 7 – Zestron flux test: (SH)



Picture 7-1: Board is clean



Picture 7-1: No indication of flux residues

CCQ – 8 – Ionic contamination: (SH)

Requirement/Specification:	Result/Measurement:	Status:
< 1,56 µg EQ NaCl.cm^{-2}	Delivered and main boards PASS. Module boards FAIL. (See table 8-1)	✗ FAIL

Specification:
IPC-TM-650, < 1,56 µg EQ NaCl.cm^{-2}

Result:
Module boards (C are >6 µg EQ NaCl.cm^{-2}. delivered and main board A is <1,56 µg EQ NaCl.cm^{-2}.

Methods, test:
IPC-TM-650, Method 2.3.25

Documentation:
Product A

Suhang boards

Evaluation:
Many results has been measured and recorded since the start of the projects. All are similar to those results. Contamination is proportional to the amount of applied paste. As a whole, result is **FAIL**.

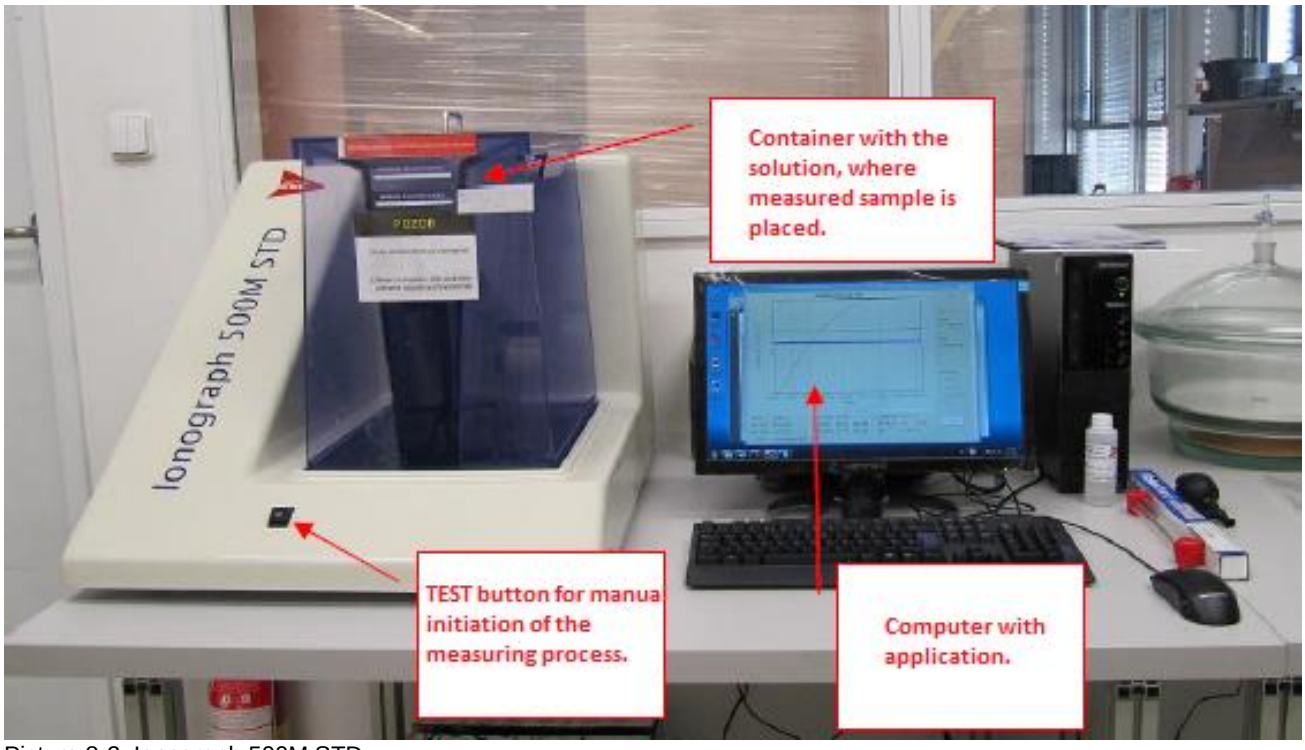
Attachments:

	Main	Module	Support
Clear	0,12	0,11	0,13
SMD	1,07	6,32	-
THT	-	-	-

Table 8-1: Results

CCQ – 8 – Ionic contamination: (SH)

Picture 8-1: Contamination of AP-339.253.00-01 (sample)



Picture 8-2: Ionograph 500M STD

CCQ – 9 – Uniformity: (SH)

Requirement/Specification:	Result/Measurement:	Status:
See specification	See results	 PASS

Specification:

Any voids, holes, wrinkles, streaks, cracking, delamination, blistering, or peeling of the coating or other evidence of loss of adhesion, or discoloration of the conductors shall be reported. Any legends shall be clearly visible through the coating.

Result:

No loss of adhesion was present except of little tearing caused by epoxy during microsection (single case). Discoloration was not found. Samples were without voids and holes, but in case of thick layers blistering and also wrinkles were detected. Even on picture 9-5, layer was not thick enough on SMD's edges.

Methods, test:

Microsection

Documentation:

Suhang boards

Evaluation:

Adhesion and thickness are evaluated in different part of the report. Any issues caused by thick layer can be (and were) removed. This was proved by additional testing on updated versions of programs. For this reason, I consider this requirement as **PASS-**ed.

Insufficient coating on edges of SMDs and THT's pins persist. It passes the condition of same and better than RTT's coating.

Attachments:

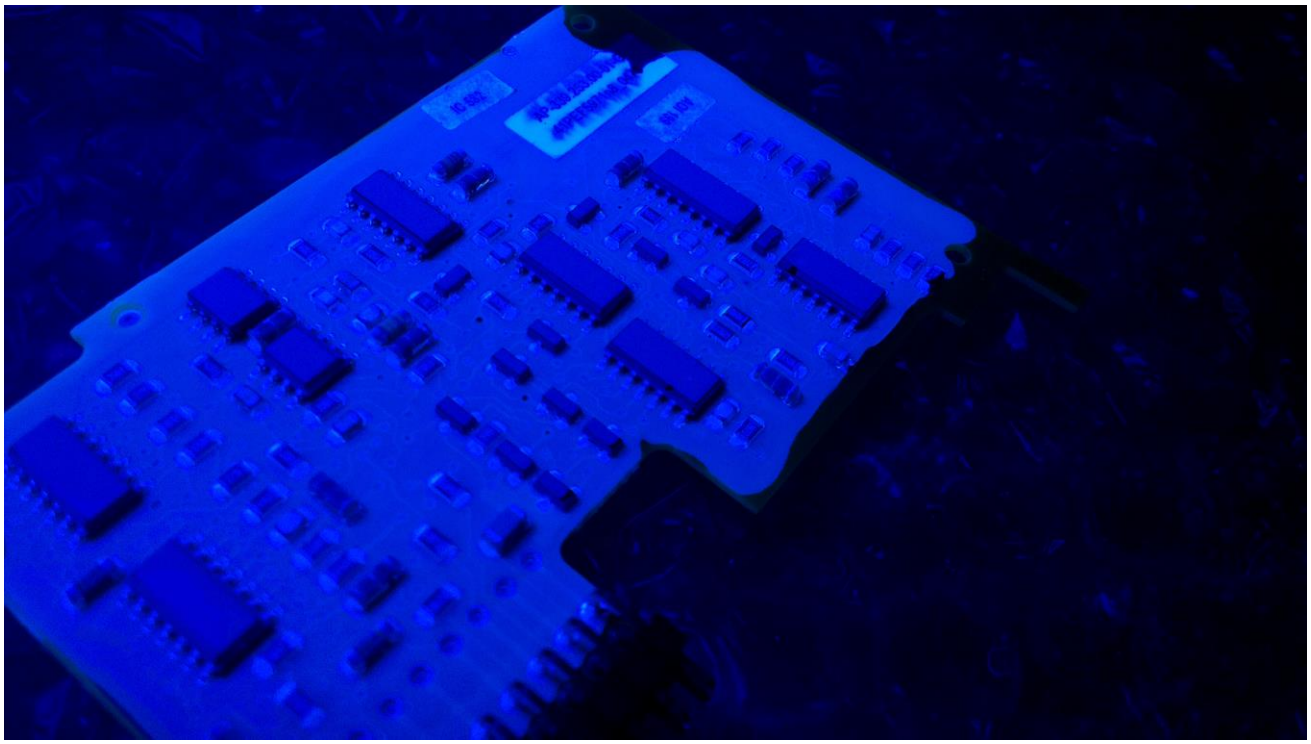
Note: Pictures are samples of prime issues. It should be taken as lead. Board C has set of SMD resistors that are hard to coat. Coating prior to THT assembly should be considered.

CCQ – 9 – Uniformity: (SH)

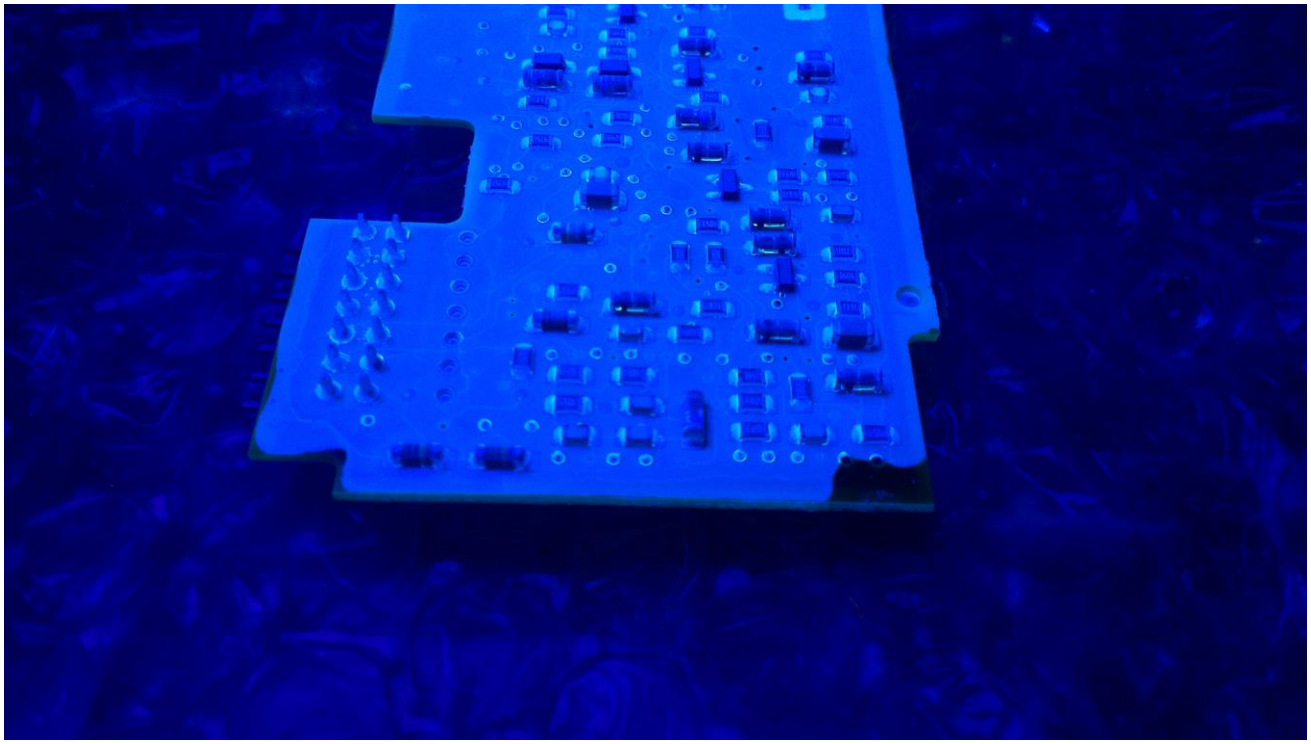
Picture 9-1: SMD components are not coated

Picture 9-2: Updated version, edges are still issue

CCQ – 9 – Uniformity: (SH)

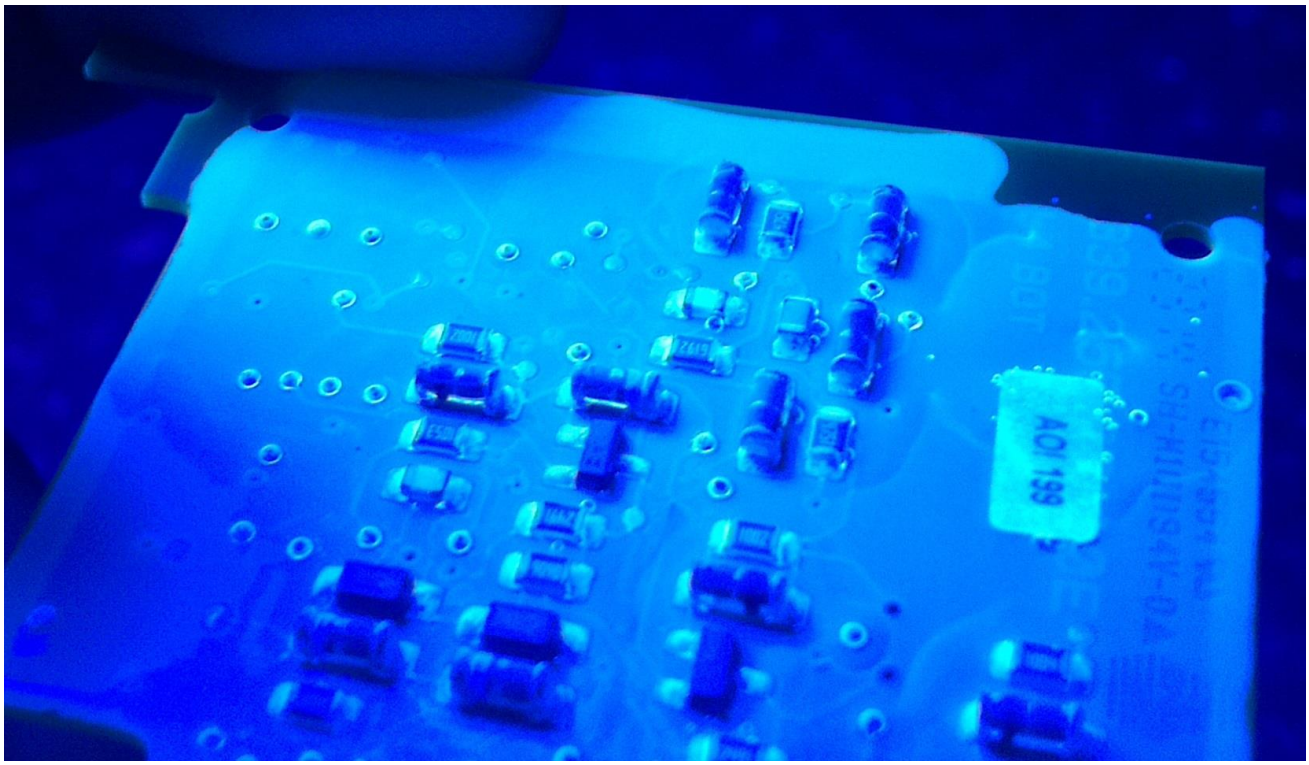


Picture 9-3: Edges are not covered

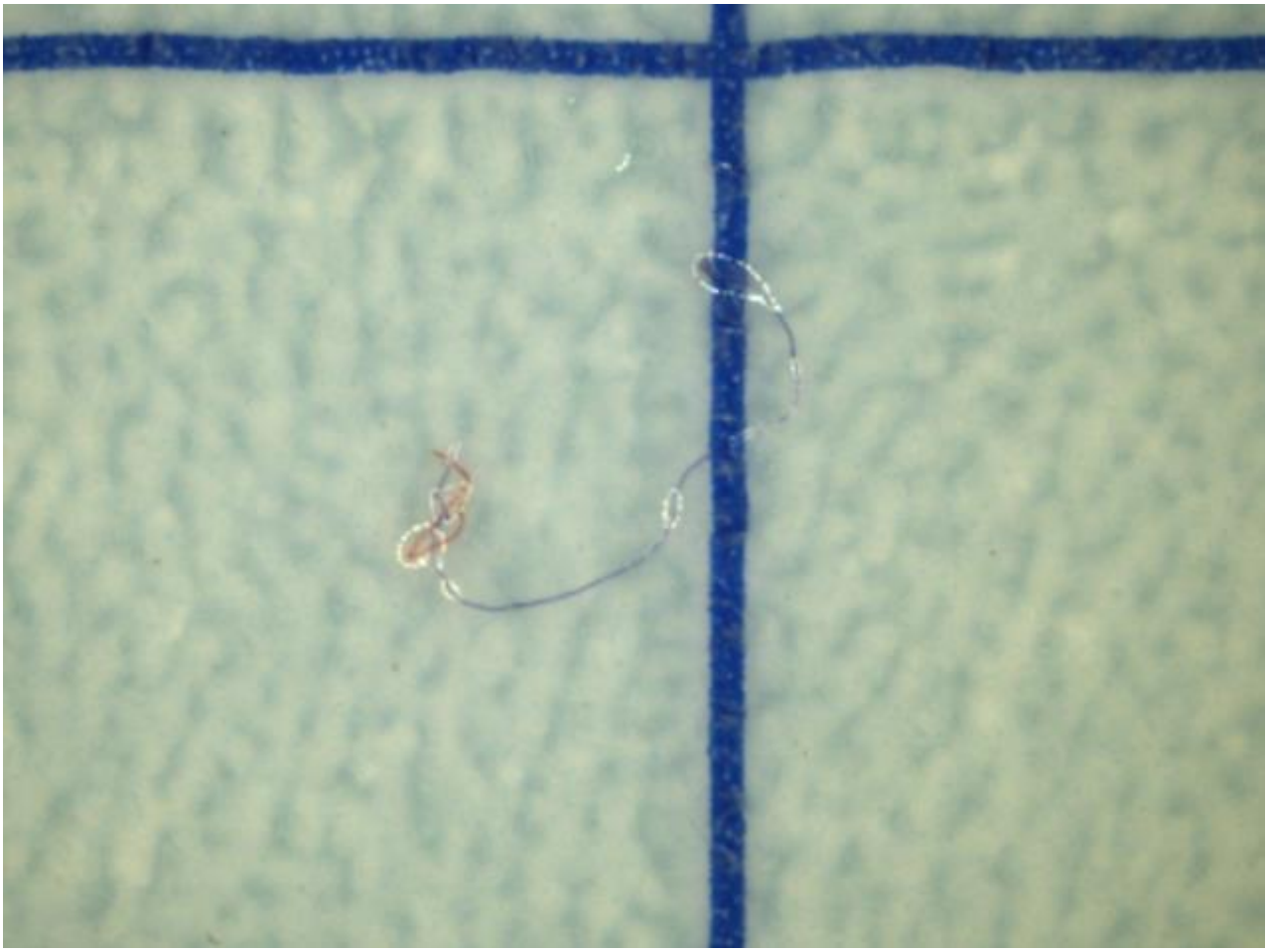


Picture 9-4: Conductive paths are not sufficiently covered

CCQ – 9 – Uniformity: (SH)

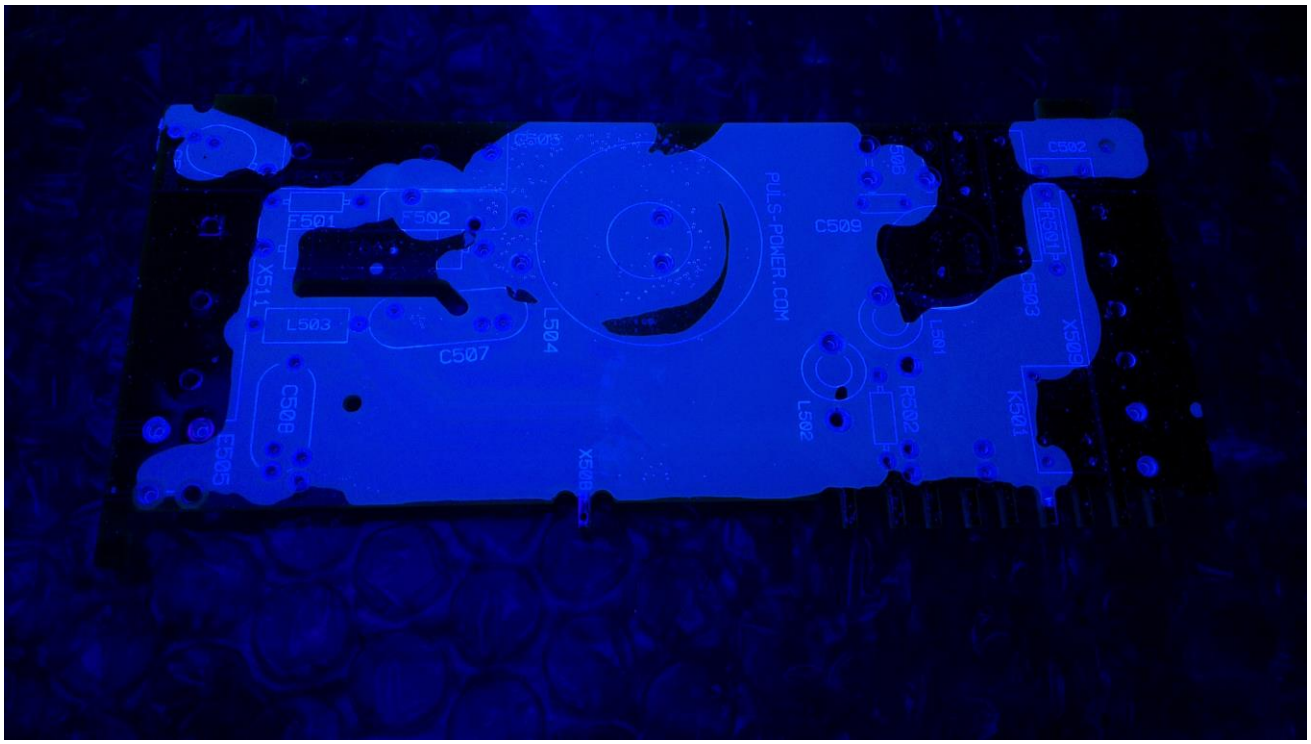


Picture 9-5: Wrinkles, amount of varnish was decreased



Picture 9-6: Impurities (sample paper boards; clean ambient free of dust)

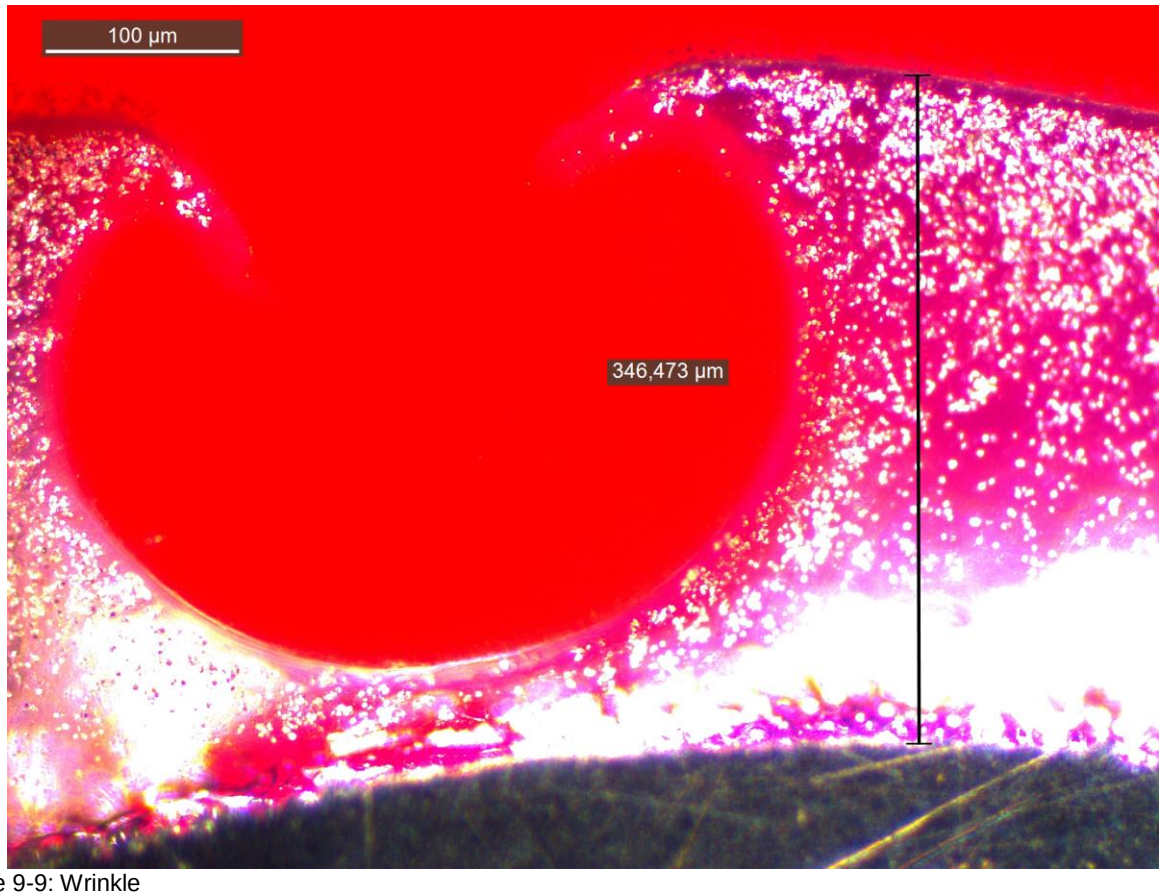
CCQ – 9 – Uniformity: (SH)



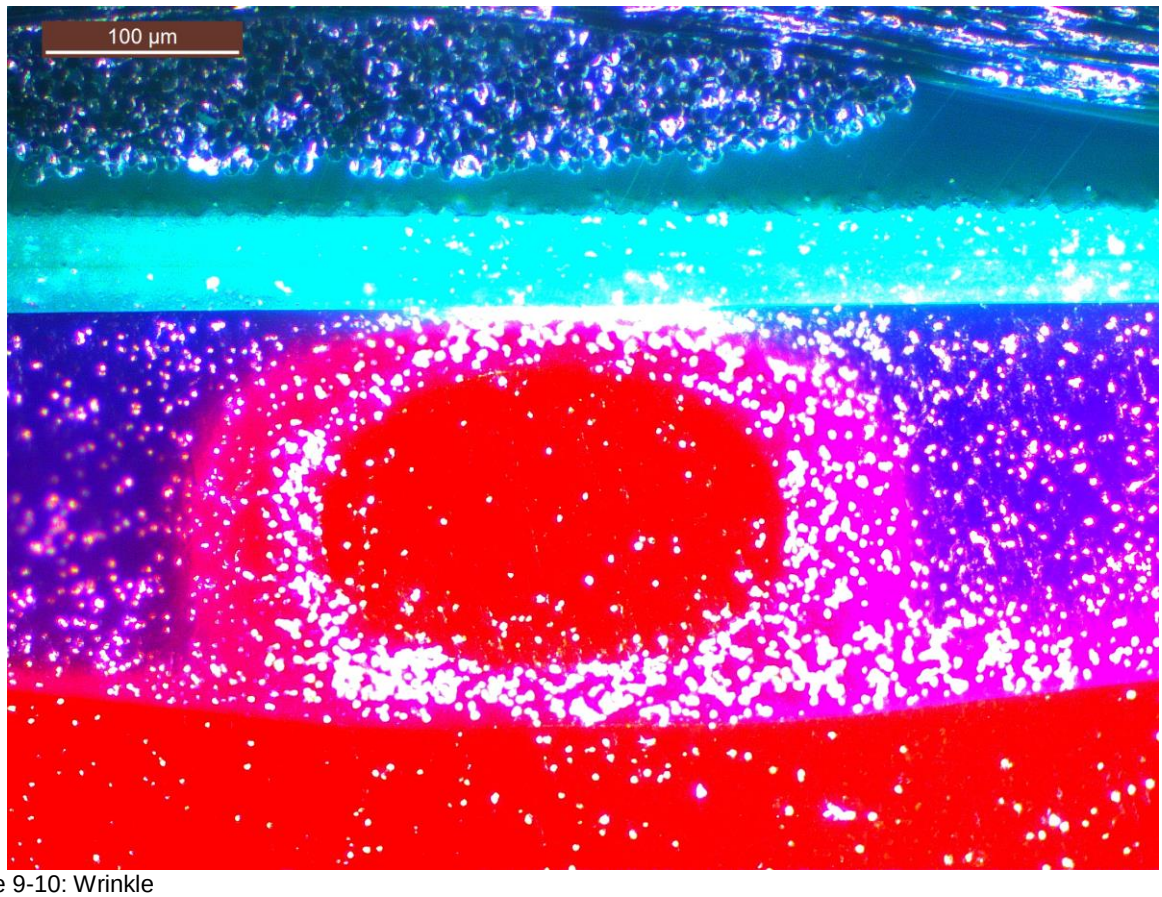
Picture 9-7: Wrinkles (in this case, it is because of thick layer – assemblies are missing)

Picture 9-8: Wrinkles – thick, but still not enough for several SMDs (viscosity)

CCQ – 9 – Uniformity: (SH)

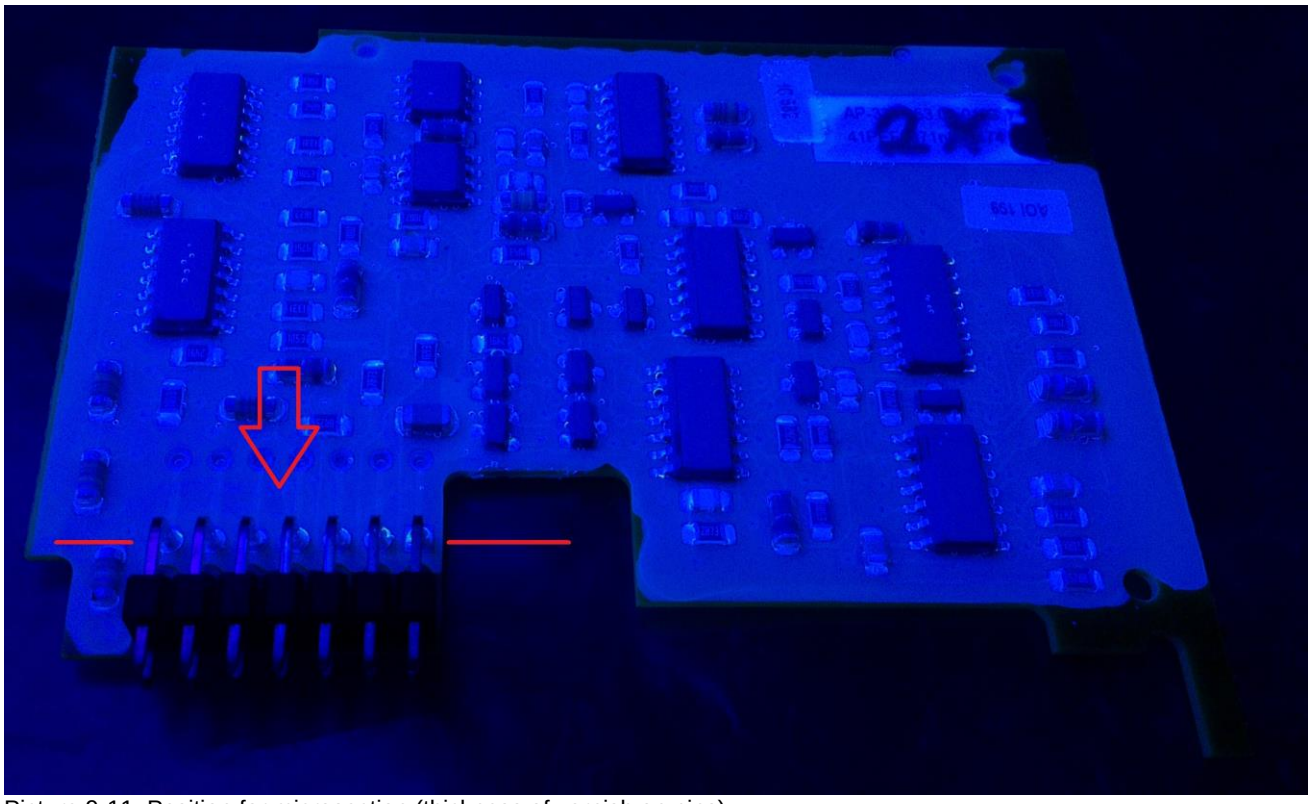


Picture 9-9: Wrinkle

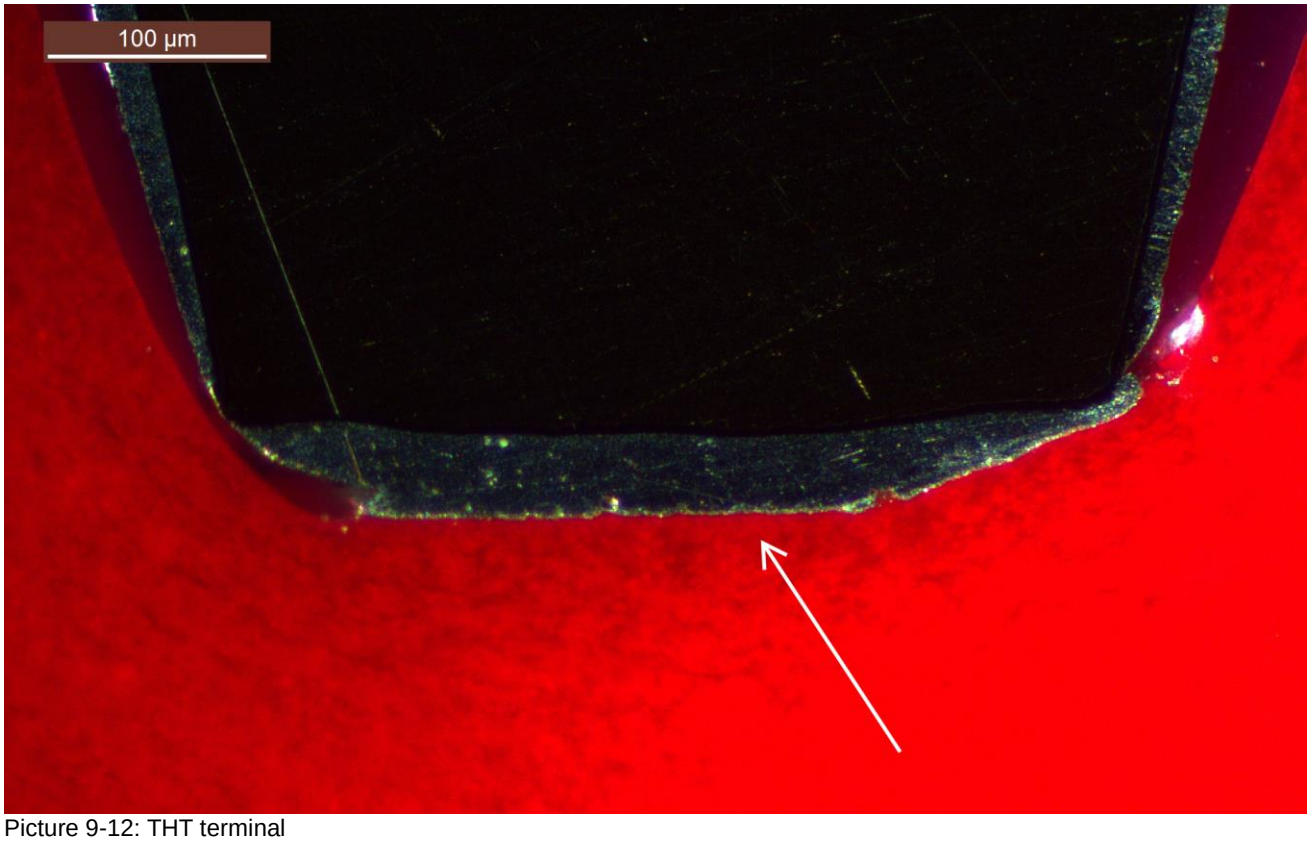


Picture 9-10: Wrinkle

CCQ – 9 – Uniformity: (SH)

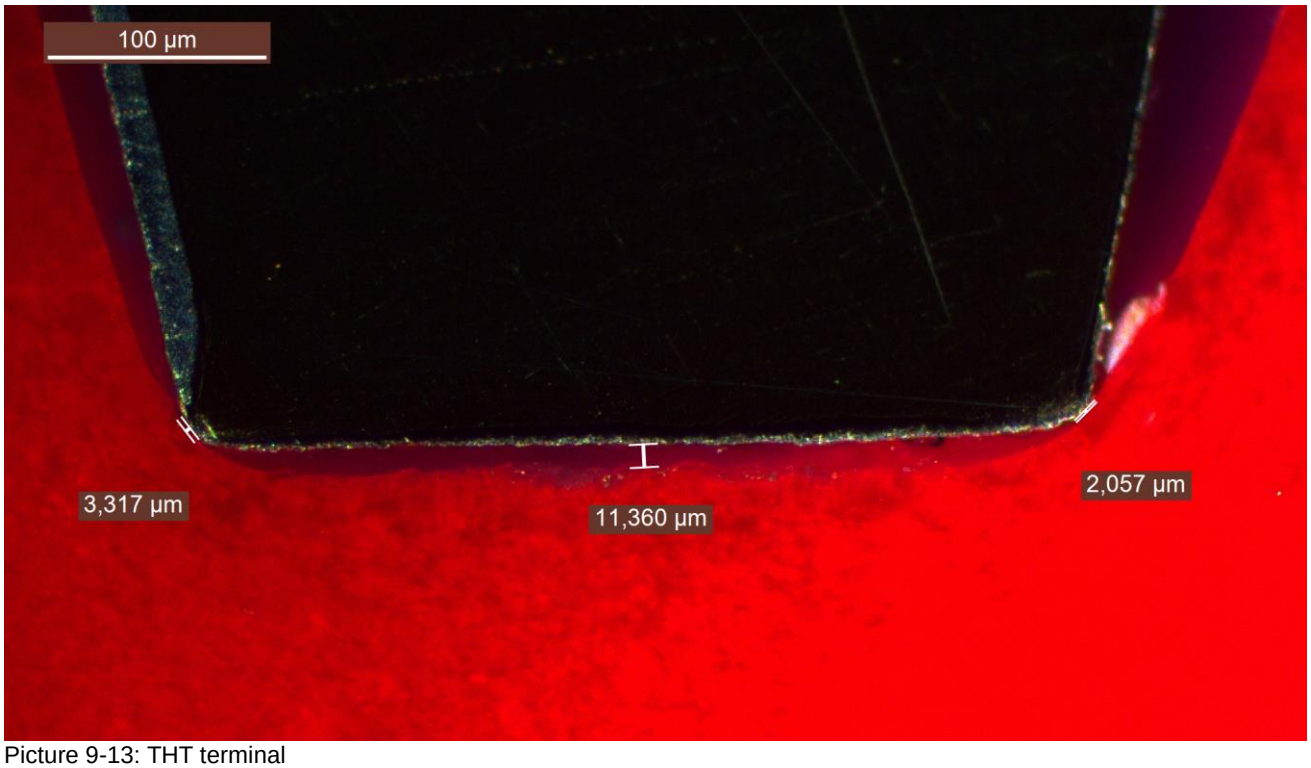


Picture 9-11: Position for microsection (thickness of varnish on pins)



Picture 9-12: THT terminal

CCQ – 9 – Uniformity: (SH)



Picture 9-13: THT terminal

CCQ – 10 – Thickness: (SH)

Requirement/Specification:	Result/Measurement:	Status:
Requirement 25 – 75 µm IPC J-STD-001 (30 – 130 µm) in dry state	Many results, see tables (pins and SMD edges are critical)	 PASS (conditions)

Specification:
Required thickness is 25 – 75 µm, IPC J-STD-001 states 30 – 130 µm

Result:
Results should be taken as a possibility for process improvement. In extremes, there is 0 µm and also 800 µm.

Methods, test:
Ultrasonic measurement

Microsection

Calculation

Documentation:
Product A

Suhang boards

Evaluation:
IPC's suggestions are important for its upper limit. Layer too thick can damage glass components. Tension would be too much for them. I consider result as **PASS**. Thin layers were adjusted. Coating on edges and pins is same or better than RTT's.

Thick layers are not ideal. Except other things, bubbles are present and adhesion is lower.

Additional tabled thicknesses as a function of jet's speed will provide needed information.

Attachments:

µ [µm]	σ [µm]	c [%]	min [µm]	max [µm]
47,6	6,3	13,2	35,5	58,7

Table 10-1: Single layer, ultrasonic measurement

µ [µm]	σ [µm]	c [%]	min [µm]	max [µm]
40,4	11,8	29,2	25,6	64,3

Table 10-2: Single layer, microsection

CCQ – 10 – Thickness: (SH)

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
96,0	45,8	47,7	49,1	193,0

Table 10-3: Double layer, ultrasonic measurement (here results are corrupted as board suffered from inequality of surface – angled and flowed to side)

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
96,9	49,3	50,9	31,7	190,3

Table 10-3: Double layer, microsection (here results are corrupted as board suffered from inequality of surface – angled and flowed to side)

a [mm]	b [mm]	ρ [g.cm^{-3}]	m_1 [g]	m_2 [g]	t [μm]
25,4	12,7	1	0,1011	0,0863	45,9

Table 10-4: Single layer, on paper, Weight increment method was chosen as some reference for microsection.

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
55,7	7,0	12,6	45,7	67,5

Table 10-5: Single layer, on paper, microsection

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
27,6	28,3	102,3	0,0	84,9

Table 10-6: Microsection I, board C

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
73,8	44,2	59,9	9,9	129,5

Table 10-7: Microsection II, board C

μ [μm]	σ [μm]	c [%]	min [μm]	max [μm]
95,1	57,4	60,3	5,2	204,0

Table 10-6: Microsection I, board K (for populated – reason for high variance)

Single	
Speed [cm/min?]	Thickness [μm]
190	43,0
381	25,3
750	11,1

Table 9-1: Correlation between jet's speed and thickness of coating (single)

CCQ – 10 – Thickness: (SH)

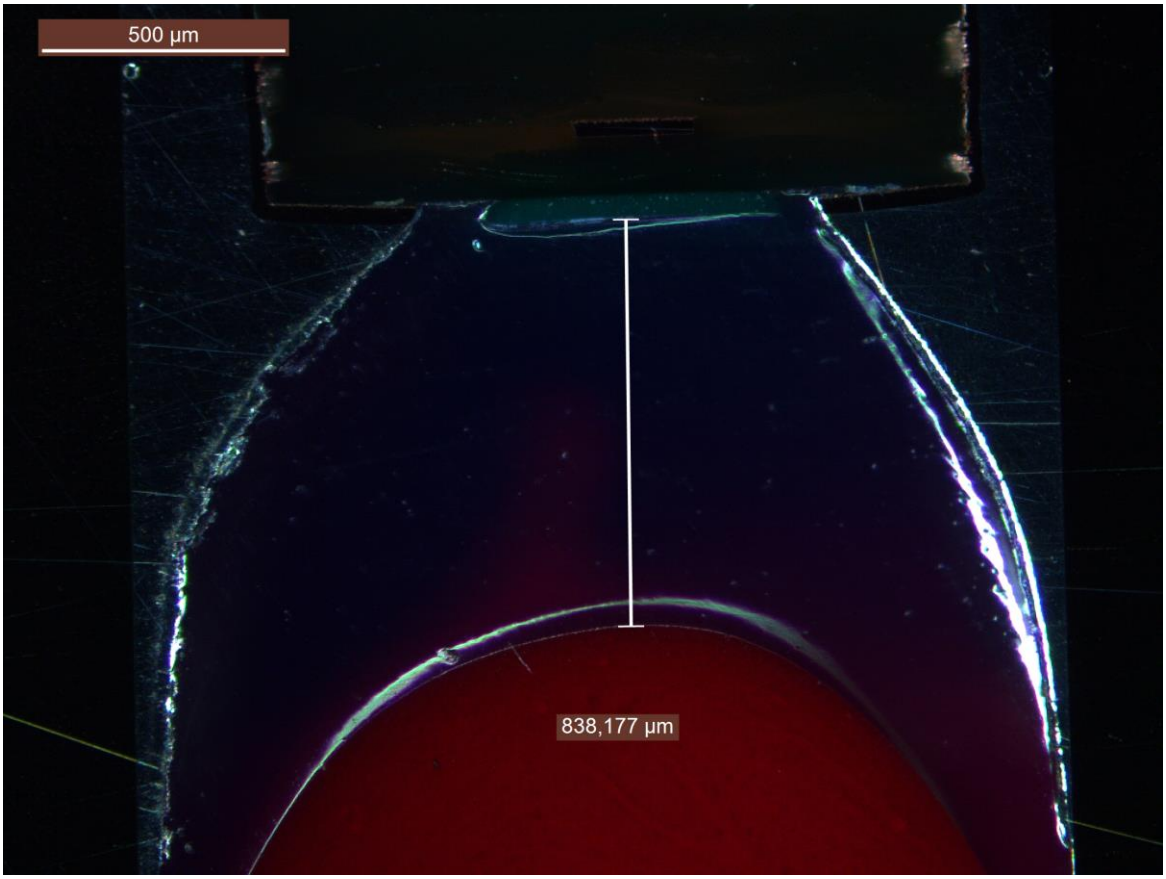
Double layer Thickness [µm]		Second (speeds)		
		190	381	750
First	190	168,4	83,8	X
	381	99,5	66,0	X
	750	X	39,0	15,4

Table 9-2: Correlation between jet's speed and thickness of coating (double)

Second layer is rotated (90 ° angle)		
First speed	Second speed	Thickness [µm]
190	381	173,7
381	381	127,7

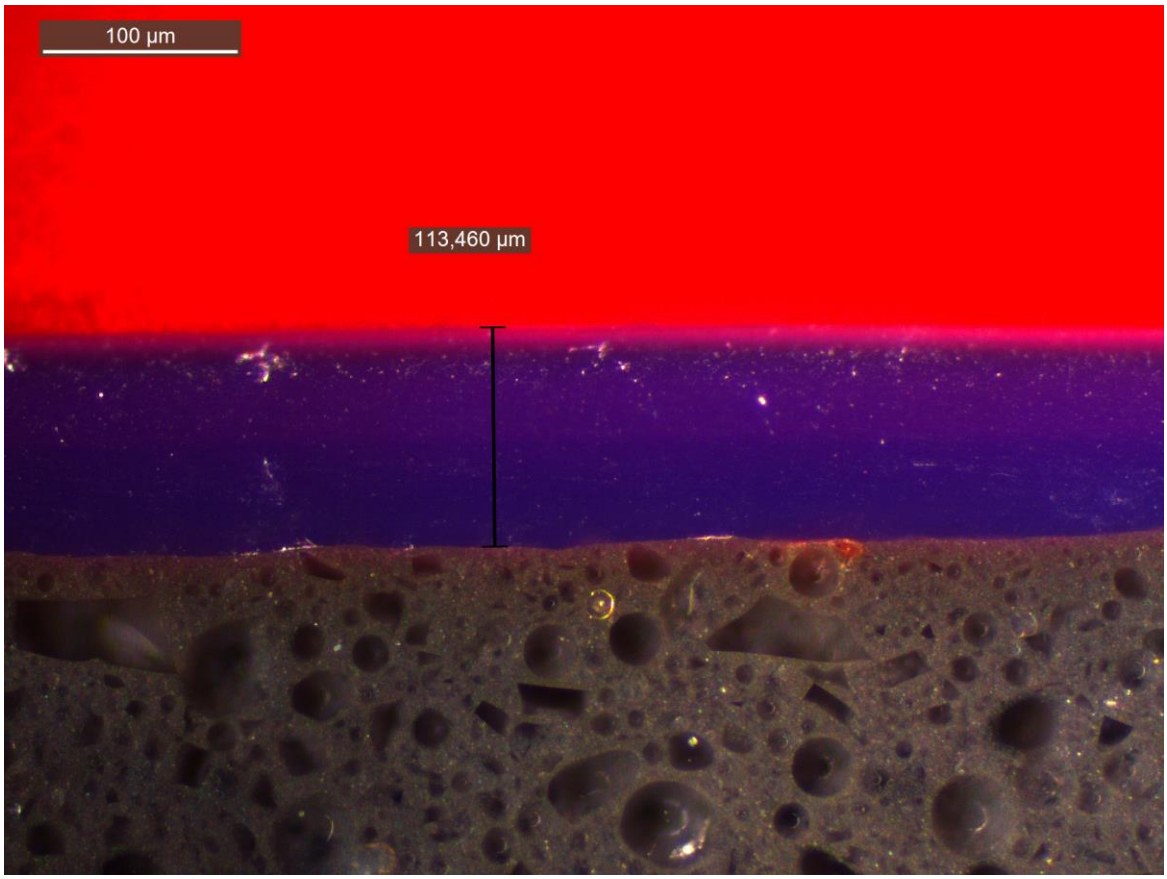
Table 9-3: Thicknesses while jet is rotated

Note: All pictures (microscopy of microsection) are taken from product A. Assembled boards with semi-final programs. (Microsections of coated unpopulated boards were not ideal as programs are balanced for assemblies, where additional coating is required.)

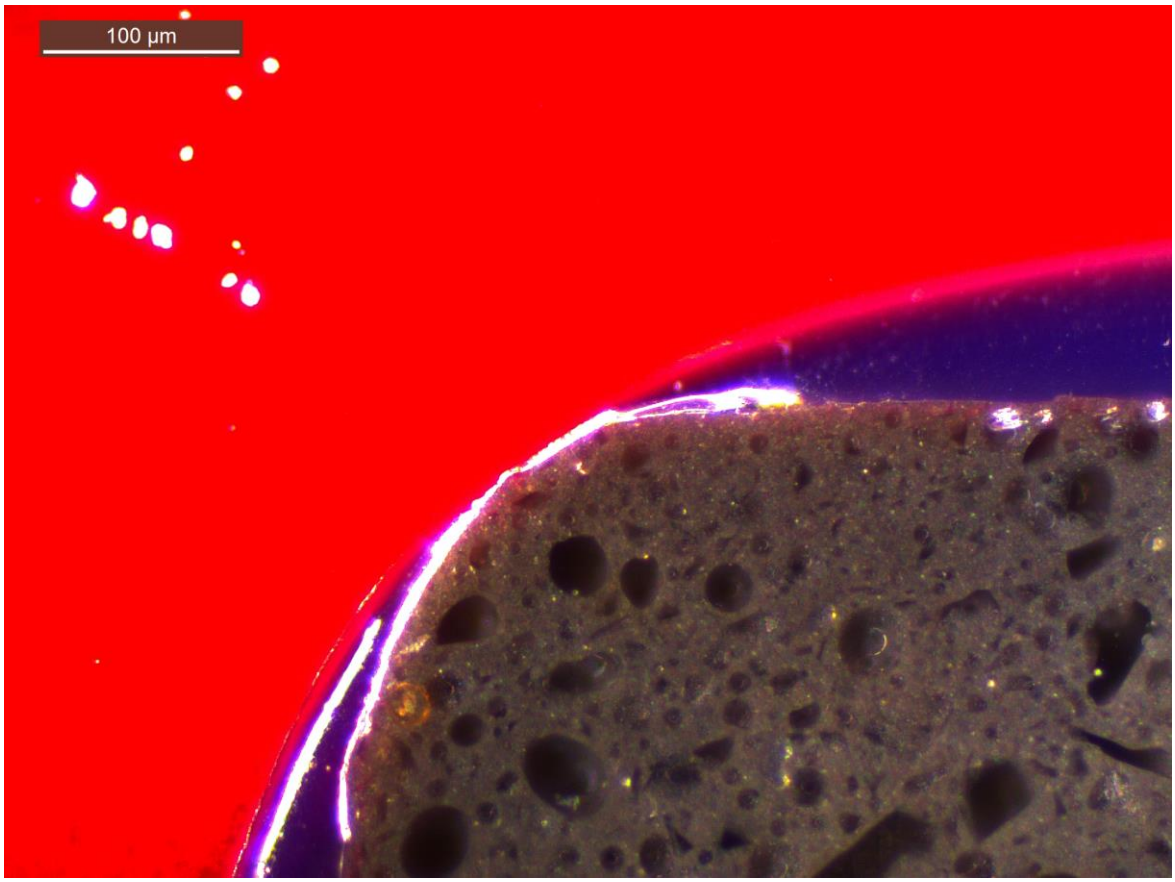


Picture 10-1: High thickness between terminals, double layer

CCQ – 10 – Thickness: (SH)



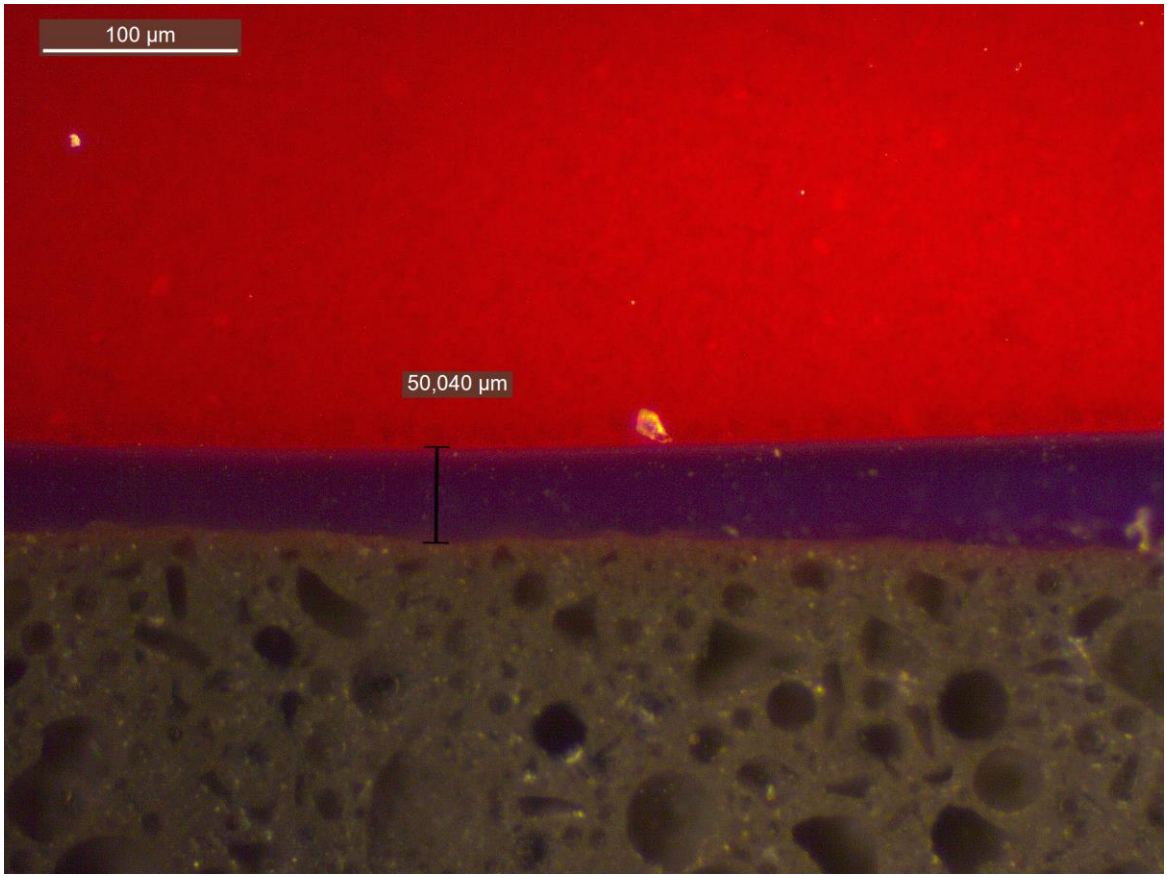
Picture 10-2: Very thick layer on top of SMD, double layer



Picture 10-3: Edge of SMD, double layer

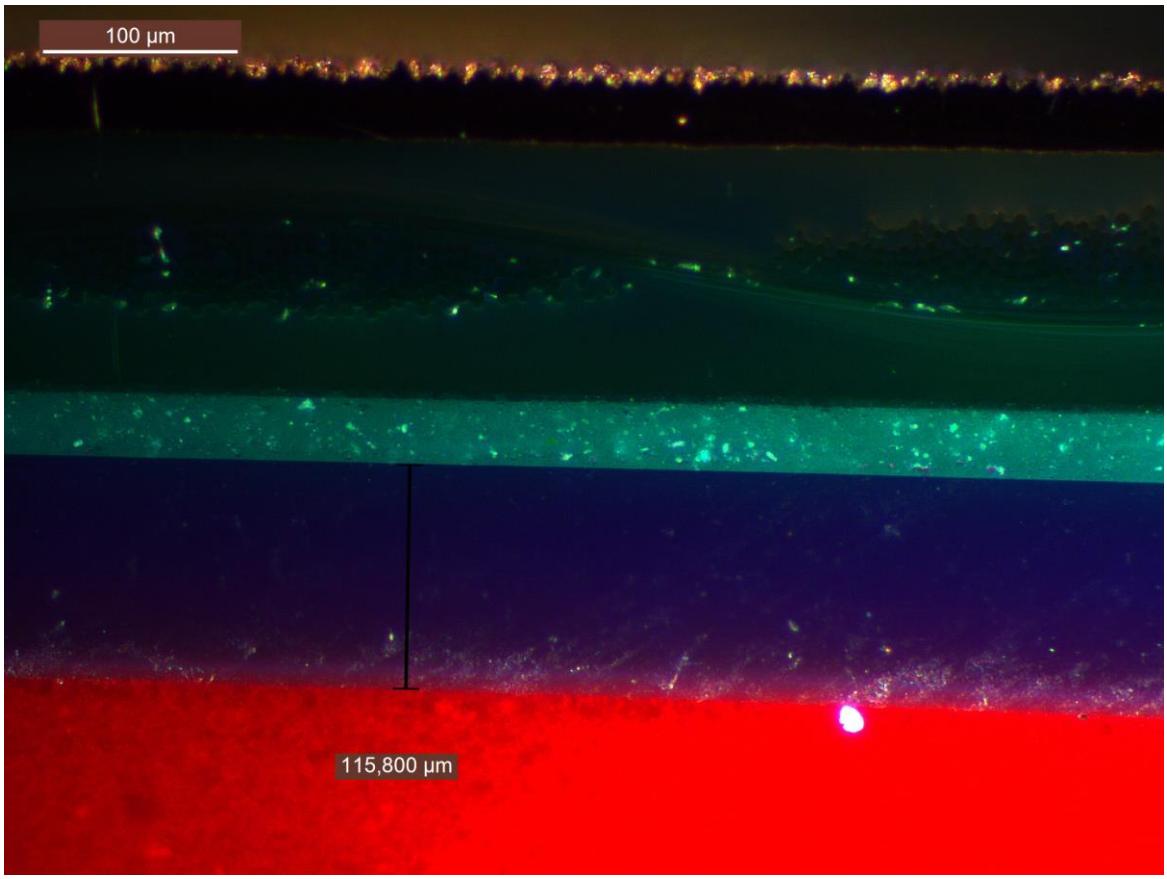
CCQ – 10 – Thickness: (SH)

Picture 10-4: Double layer

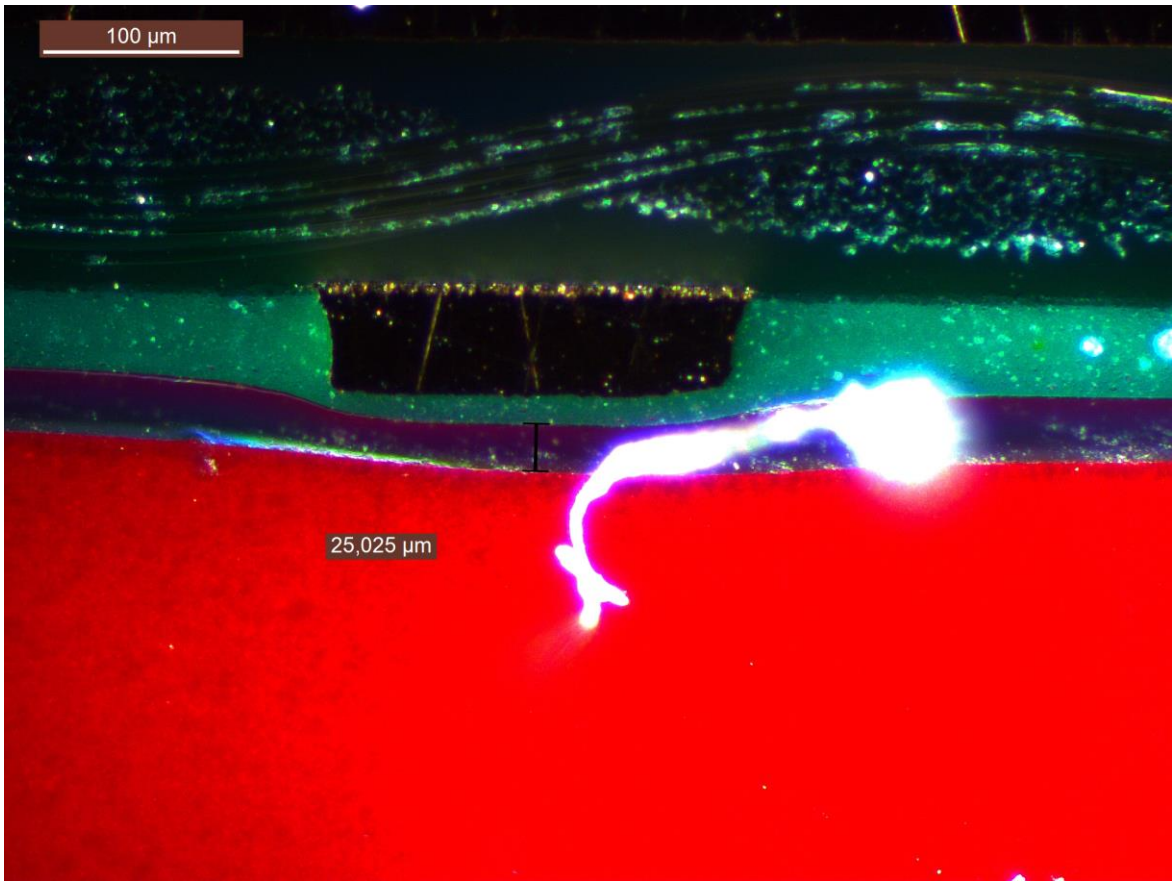


Picture 10-5: Layer on top of SMD, single layer

CCQ – 10 – Thickness: (SH)

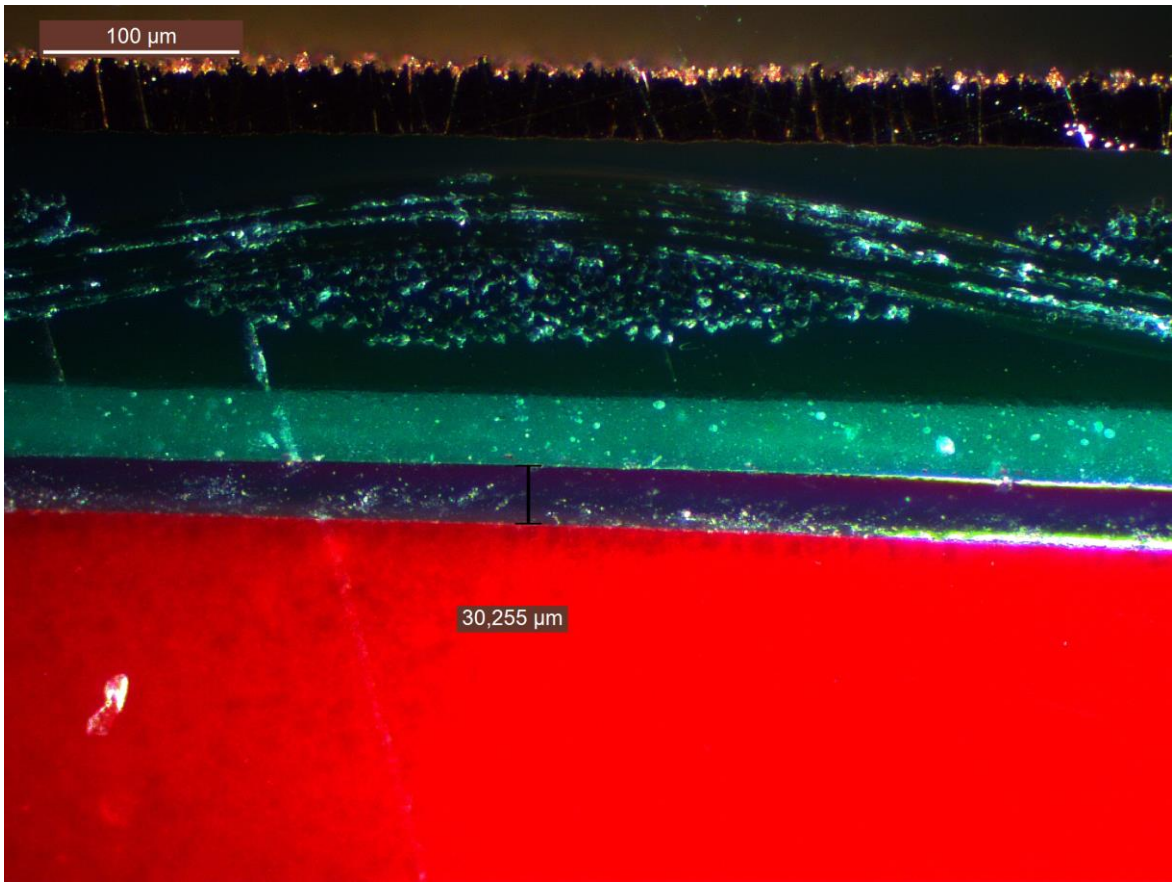


Picture 10-6: Single layer



Picture 10-7: Single layer, border line thickness

CCQ – 10 – Thickness: (SH)



Picture 10-8: Single layer

CCQ – 11 – Mash cut (adhesion test): (SH)

Requirement/Specification:	Result/Measurement:	Status:
Class 0 acc. DIN EN 2409	Class 0	 PASS

Specification:
Class 0 acc. DIN EN 2409

Result:
Class 0

Methods, test:
DIN EN 2409 specifies procedure how to process and evaluate results. Coated copper sample board is cut with defined blade in 1, 2 or 3 mm spacing. Then it is stressed by scrubbing brush. Precise adhesive tape is used for tearing the coating apart. Percentage of affected area determinates the class.

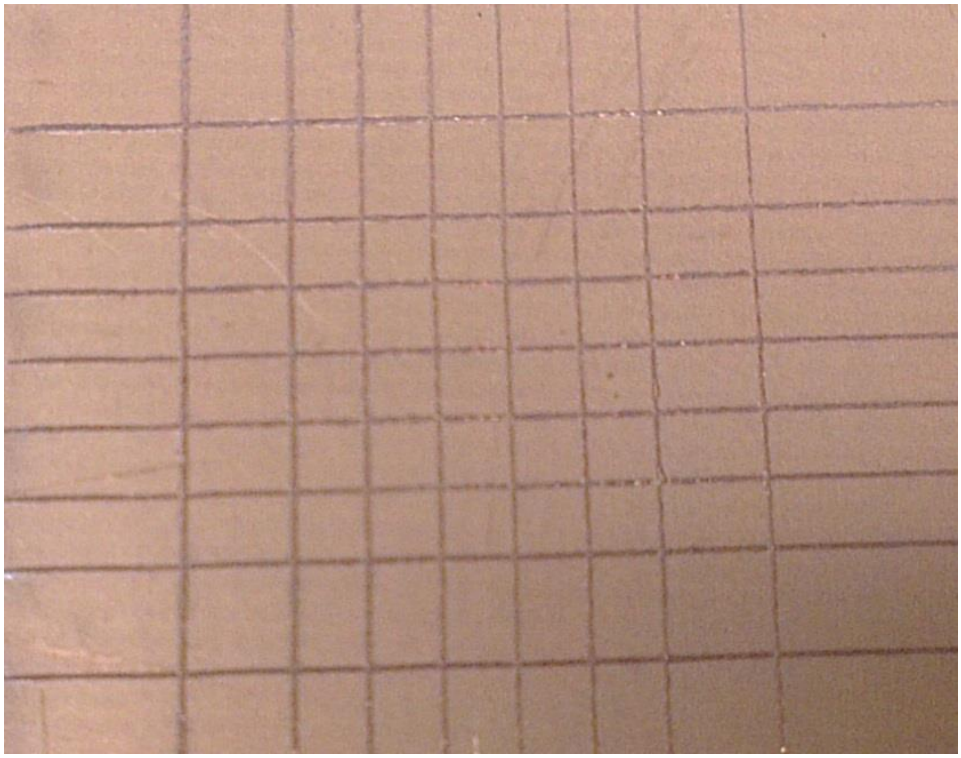
Documentation:
Product A

Suhang boards

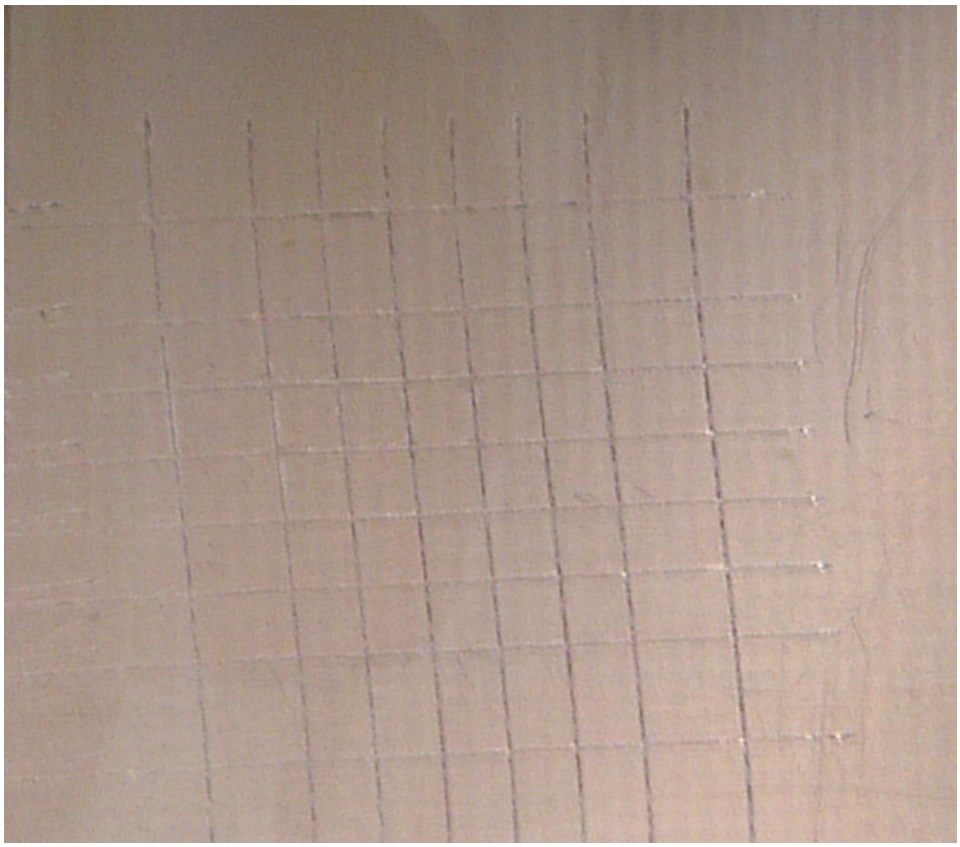
Evaluation:
Across all testing (DIN ISO 2409 and ASTM 3359) there were issues only in two cases. Those were Class 1/Class 4 (ASTM has decreasing rate). This issue was on double coated with thicknesses over 200 µm. Result is **PASS**.

CCQ – 11 – Mash cut (adhesion test): (SH)

Attachments:

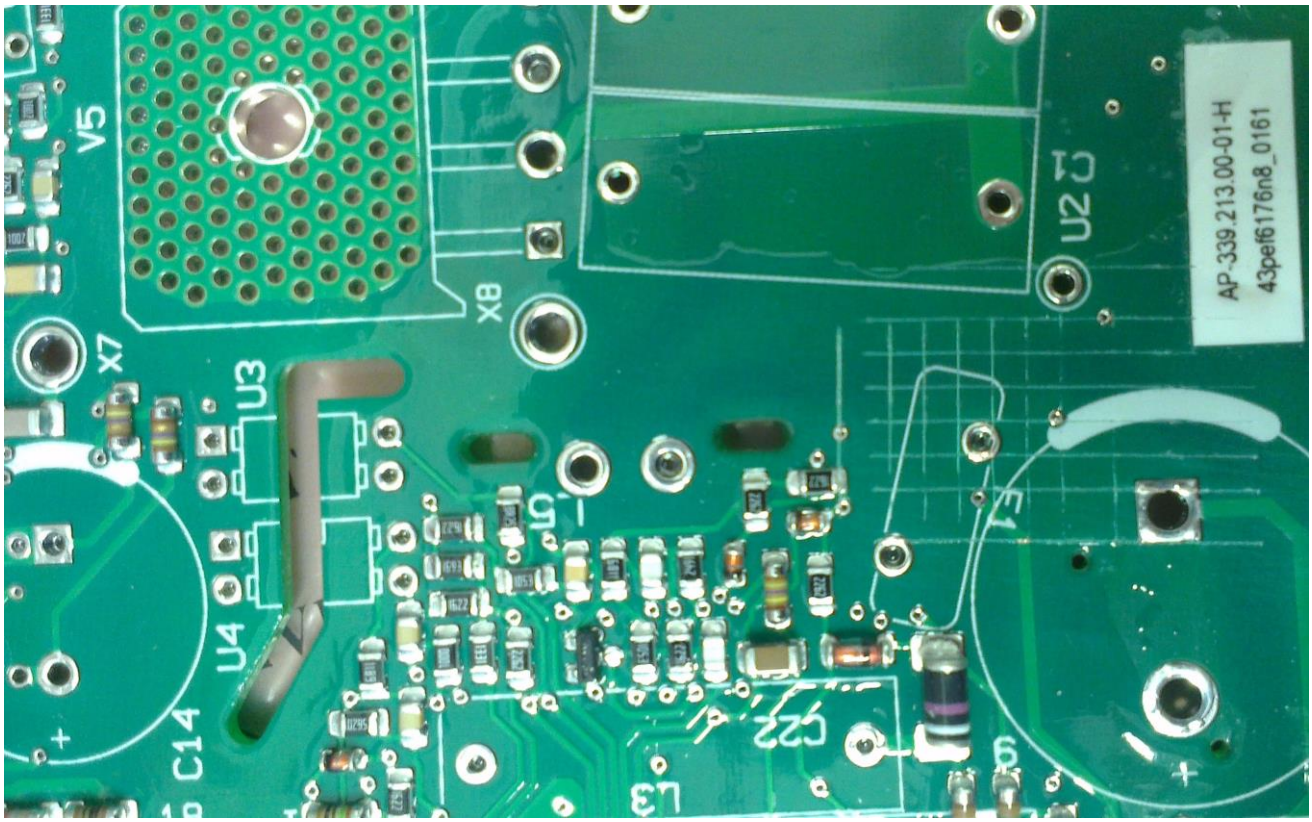


Picture 11-1: Double coated, 2 mm spacing

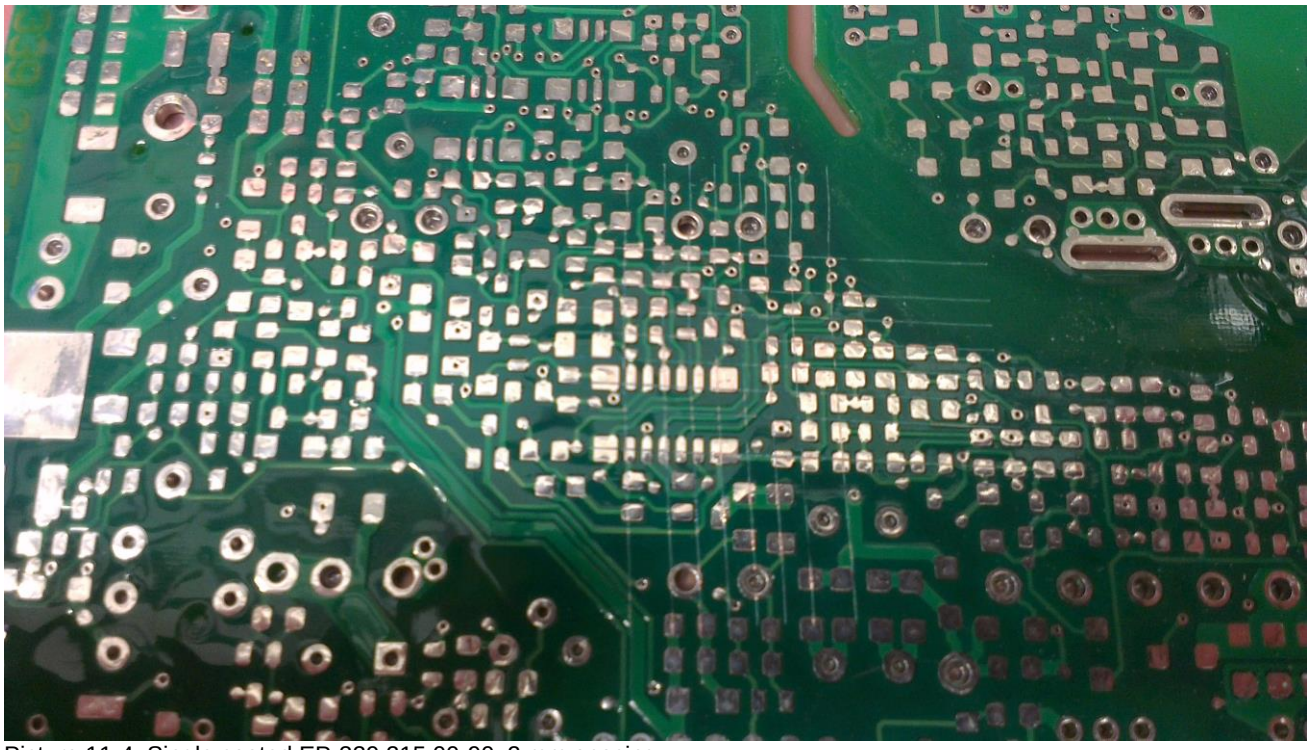


Picture 11-2: Single coated, 2 mm spacing

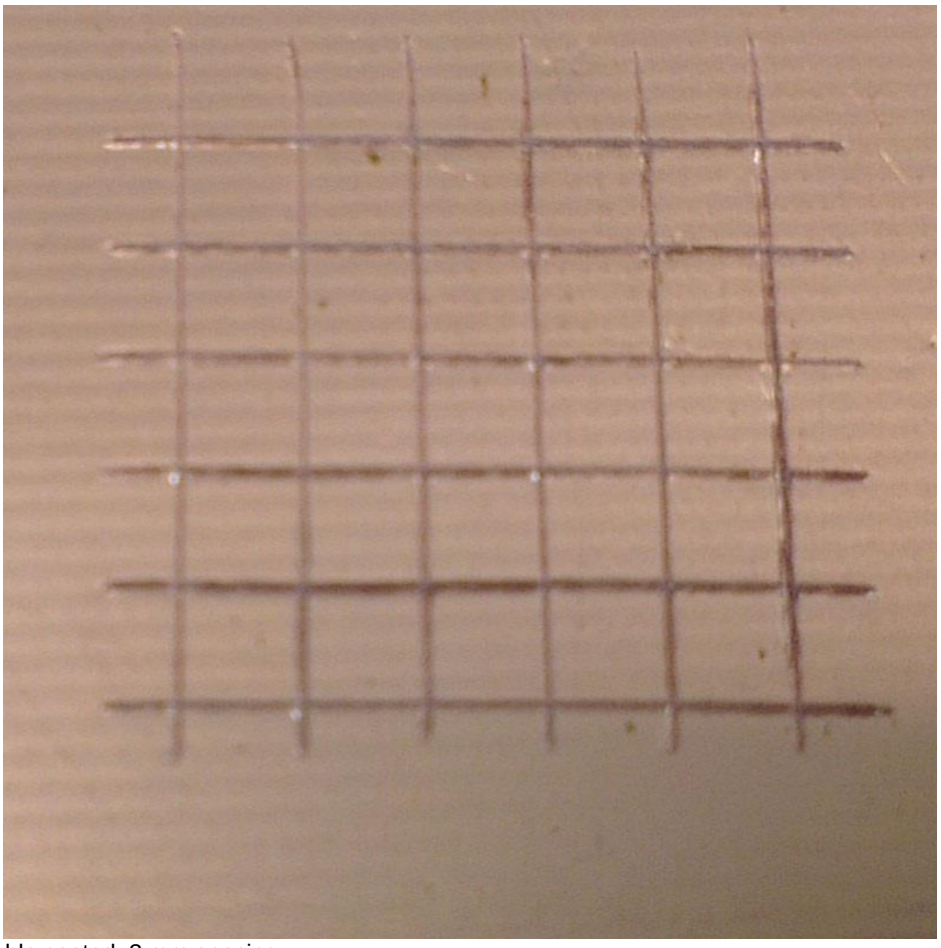
CCQ – 11 – Mash cut (adhesion test): (SH)



Picture 11-3: Single coated AP-339.213.00-01H, 2 mm spacing


Picture 11-4: Single coated EP-339.215.00-90, 2 mm spacing

CCQ – 11 – Mash cut (adhesion test): (SH)



Picture 11-5: Double coated, 3 mm spacing

Picture 11-6: Equipment

CCQ – 12 – Dielectric withstand voltage: SH

Requirement/Specification:	Result/Measurement:	Status:
IPC-TM-650, 2.5.6.1; DIN EN 60243-1; 100 kV.mm-1 (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)	85 – 103 kV.mm-1 (see attachment)	 PASS

Specification:

100 kV/mm, (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)

Result:

85 – 103 kV.mm^{-1} (see Attachments)

Methods, test:

IPC-TM-650, 2.5.6.1

Breakthrough 3 times on each thickness (9 in total)

Thickness measured 10 times + microsection on each (9 times 10 in total)

Documentation:

Product A

specification of the varnish

HIOKI 3153 Withstanding HITESTER

Ultrasonic thickness measurement

Suhang boards

Evaluation:

Dielectric withstanding voltage is lower than specified. Additional test on complete AN-339 (2,5 kV and 500 V between electrodes see High voltage test reports) was PASS.

Insulation was damaged on position where electrical field is homogenous (edges and corners exhibit fields with higher concentration), see Picture 12-2.

Note: It was highlighted to me, that speed 381 mm.s^{-1} is one that is used and preferred. With performance of the 750 mm.s^{-1}, I propose to not consider this speed (and also with this trace size) as a sole insulator. Meaning, it is no to be used without additional 381 mm/s layer etc.

With standard voltage being OK and concerning variability of results, this could be easily taken as **PASS**.

CCQ – 12 – Dielectric withstand voltage: SH

Attachments:

Speed [mm/s]	t_{MIC} [µm]	Min [µm]	Mean [µm]	Max [µm]	σ [µm]	C [%]
190	69,3	51,0	58,4	66,0	3,51	6,02
381	32,7	29,1	32,3	34,8	1,58	4,88
750	17,6	12,6	16,7	20,6	2,00	11,99

Table 12-1: Measured thickness

t_{MIC} is thickness measured by microsection to verify the ultrasonic results.
Min is minimal thickness, Max is maximal thickness, it is based on 30 samples.
σ is standard deviation (with normal distribution)
C is variation coefficient
Voltage is based on 3 sample (3 times breakthrough on each thickness/speed)

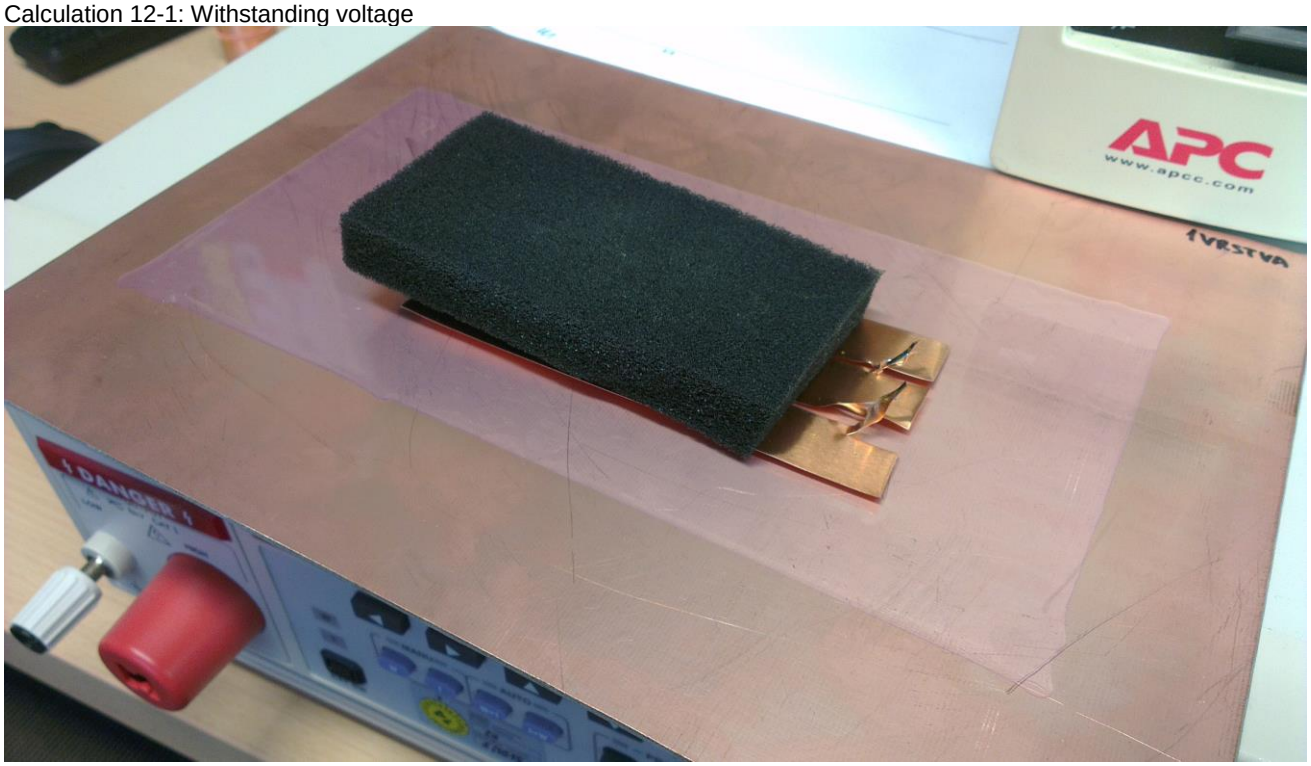
U [V]	E(min) [kV/mm]	E(mean) [kV/mm]	E(LT) [kV/mm]
5000	98,0	85,6	91,1
3000	103,1	92,9	97,6
670	53,2	40,2	45,7

Table 12-2: Withstanding voltage

$$E = \frac{U}{d} = 98{,}0 \text{ kV.mm}^{-1}$$

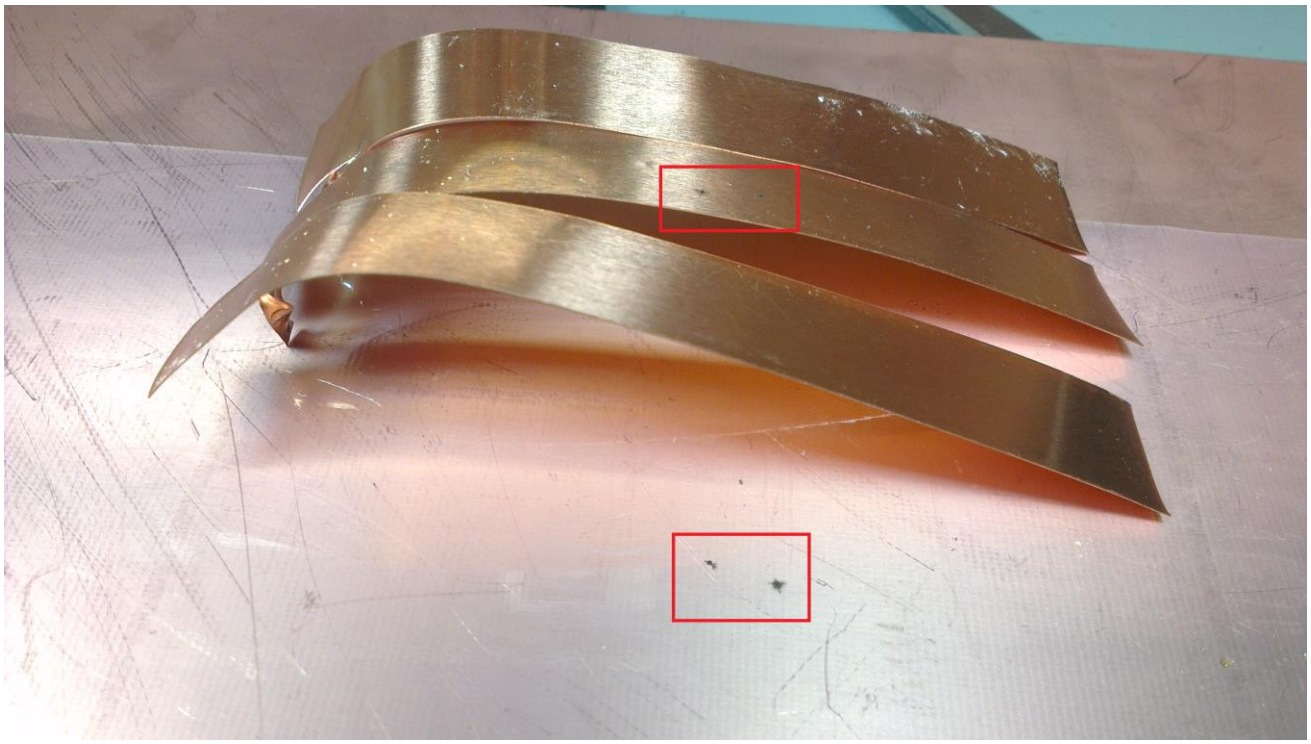
E (min) is calculated with minimal thickness and given voltage.
E (mean) is calculated with mean thickness and given voltage.
E (LT) is calculated with mean thickness minus standard deviation and given voltage.

Calculation 12-1: Withstanding voltage

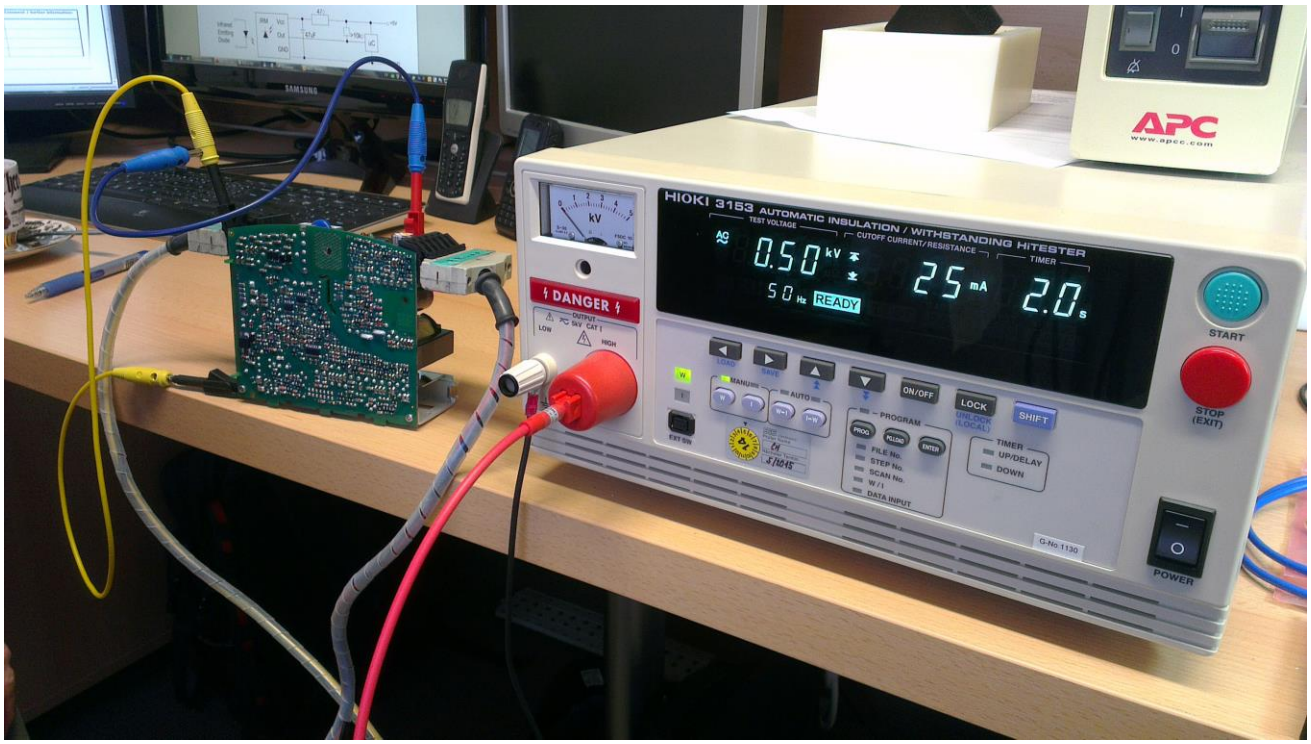


Picture 12-1: Dielectric system testing

CCQ – 12 – Dielectric withstand voltage: SH

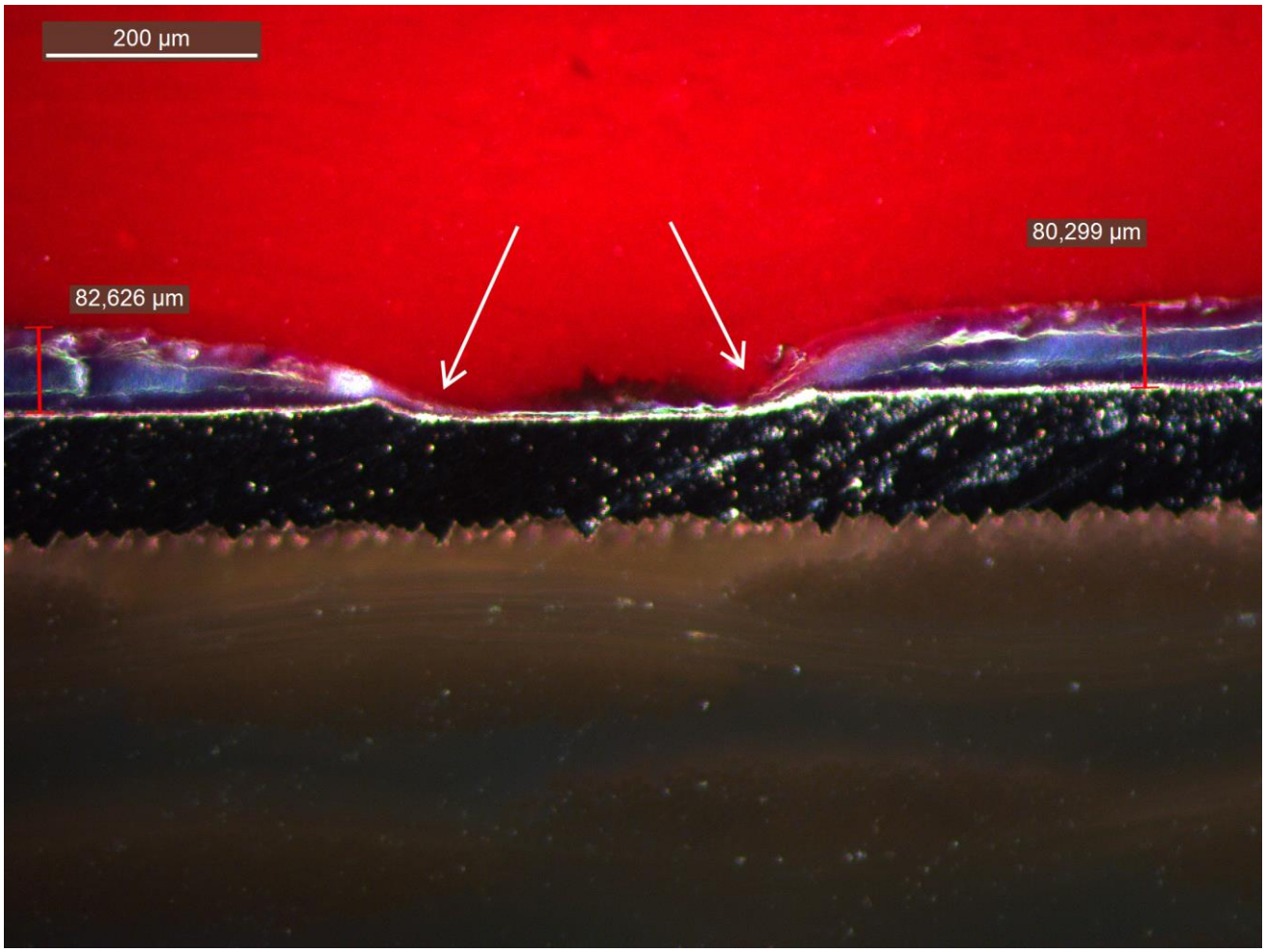


Picture 12-2: Position

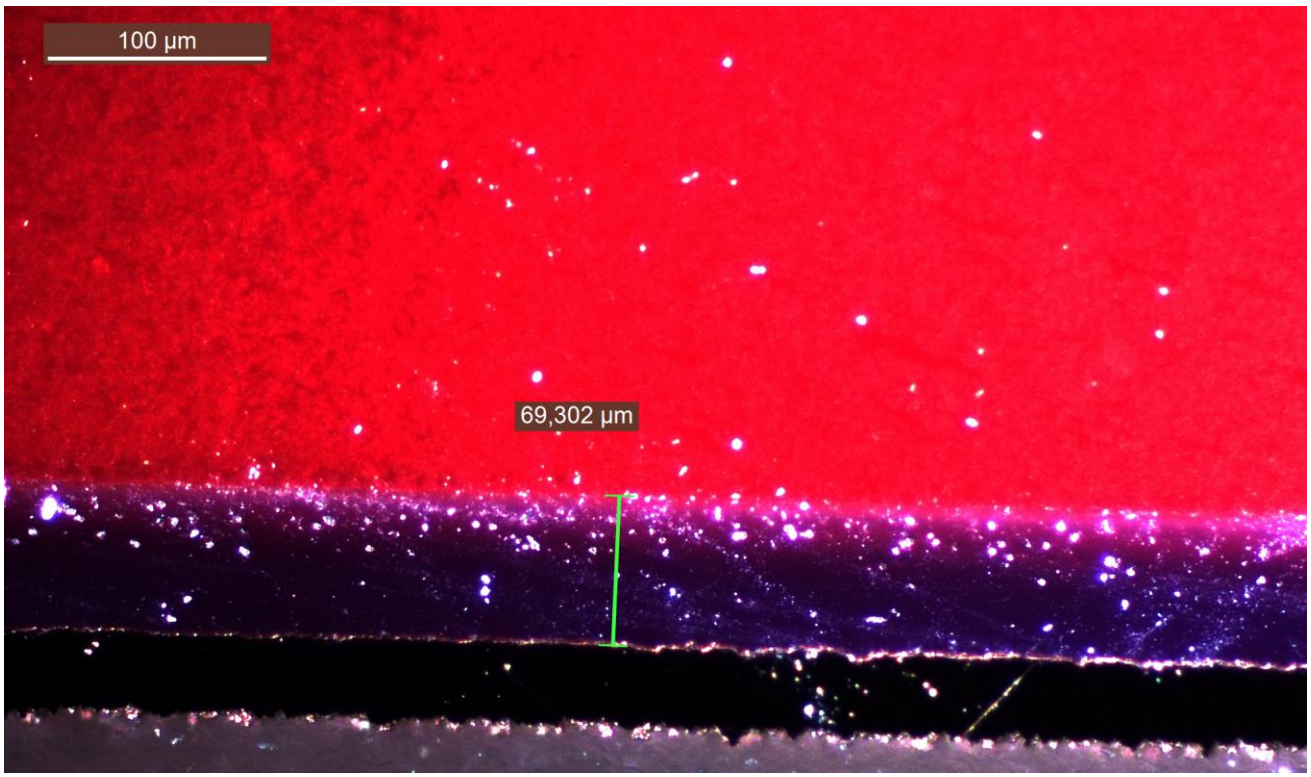


Picture 12-3: HIOKI 3153

CCQ – 12 – Dielectric withstand voltage: SH



Picture 12-4: Microsection of breaked insulation (different test method)



Picture 12-5: Thickness for speed 190 mm/s

CCQ – 13 – Tape test (adhesion test): (SH)

Requirement/Specification:	Result/Measurement:	Status:
Class 5 acc. DIN EN 2409	Class 5 and 4 (see details)	 PASS

Specification:
Class 5 acc. ASTM 3359 Method B

Result:
Class 5

Class 4 (Double coated)

Methods, test:
DIN EN 2409 specifies procedure how to process and evaluate results. Coated copper sample board is cut with defined blade in 1 and 1,5 mm spacing. Then it is stressed by scrubbing brush. Precise adhesive tape is used for tearing the coating apart. Percentage of affected area determinates the class.

Documentation:
Product A

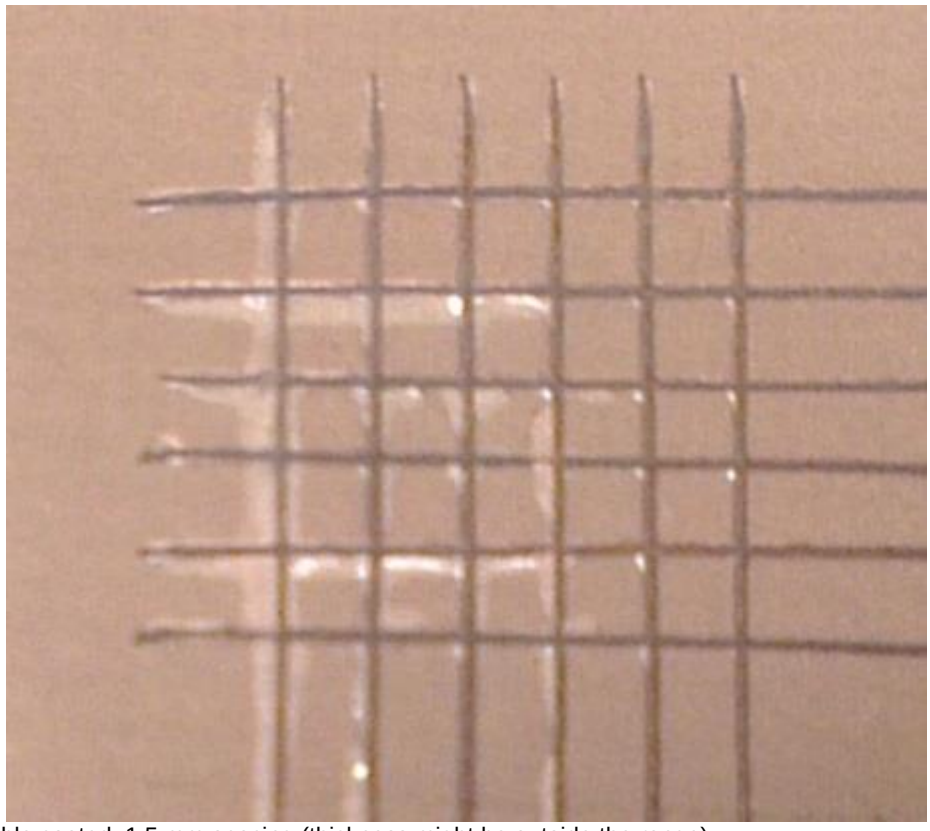
Suhang boards

Evaluation:
Across all testing (DIN ISO 2409 and ASTM 3359) there were issues only in two cases. Those were Class 1/Class 4 (ASTM has decreasing rate). This issue was on double coated with thicknesses over 200 µm. Result is **PASS**.

CCQ – 13 – Tape test (adhesion test): (SH)

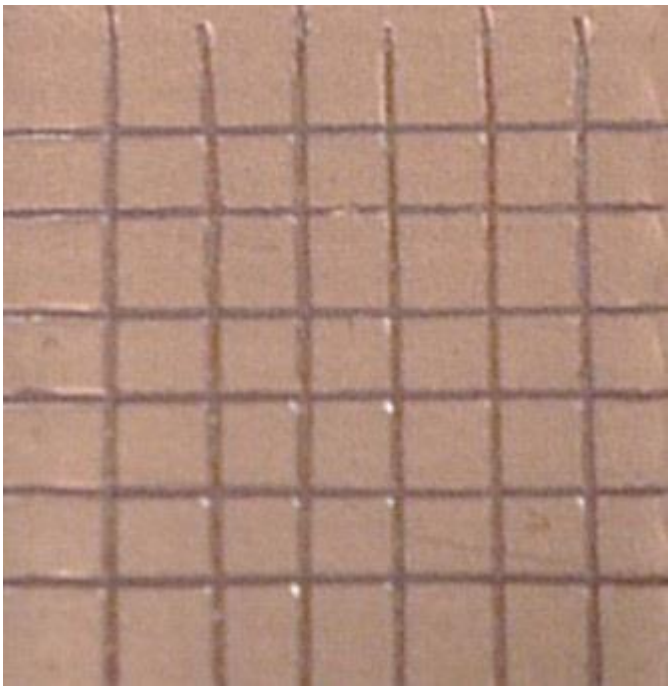
Attachments:

Picture 13-1: Equipment

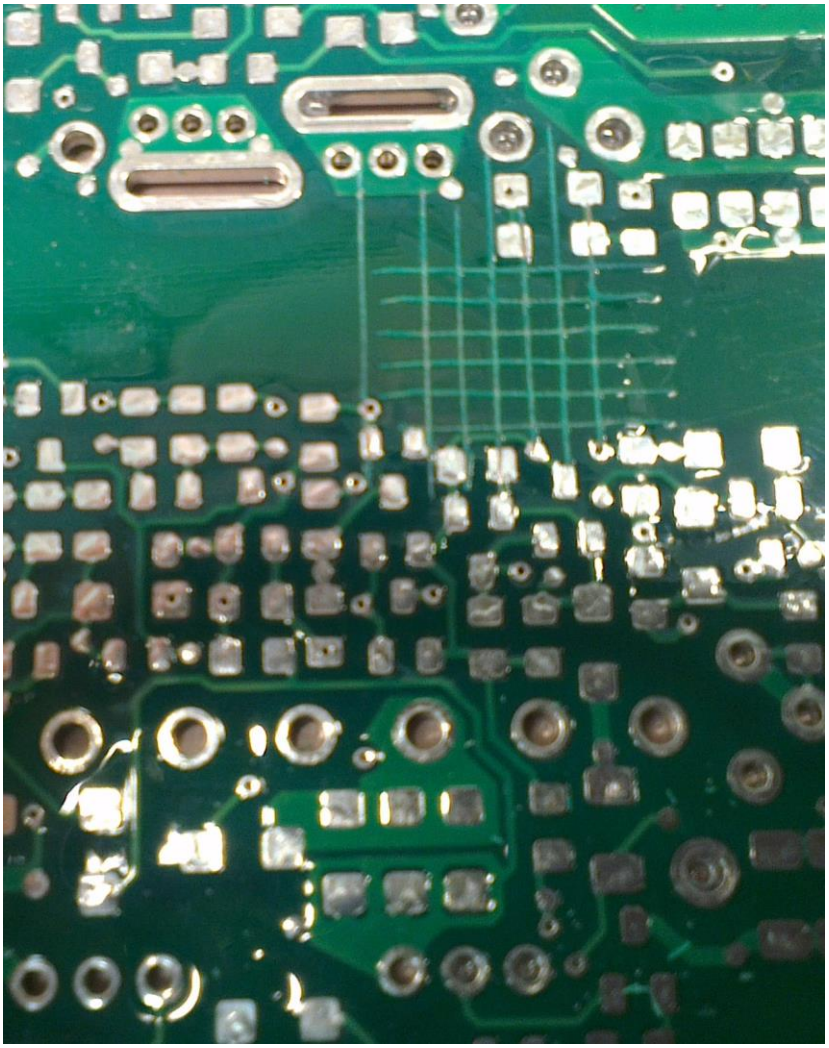


Picture 13-2: Double coated, 1,5 mm spacing (thickness might be outside the range)

CCQ – 13 – Tape test (adhesion test): (SH)

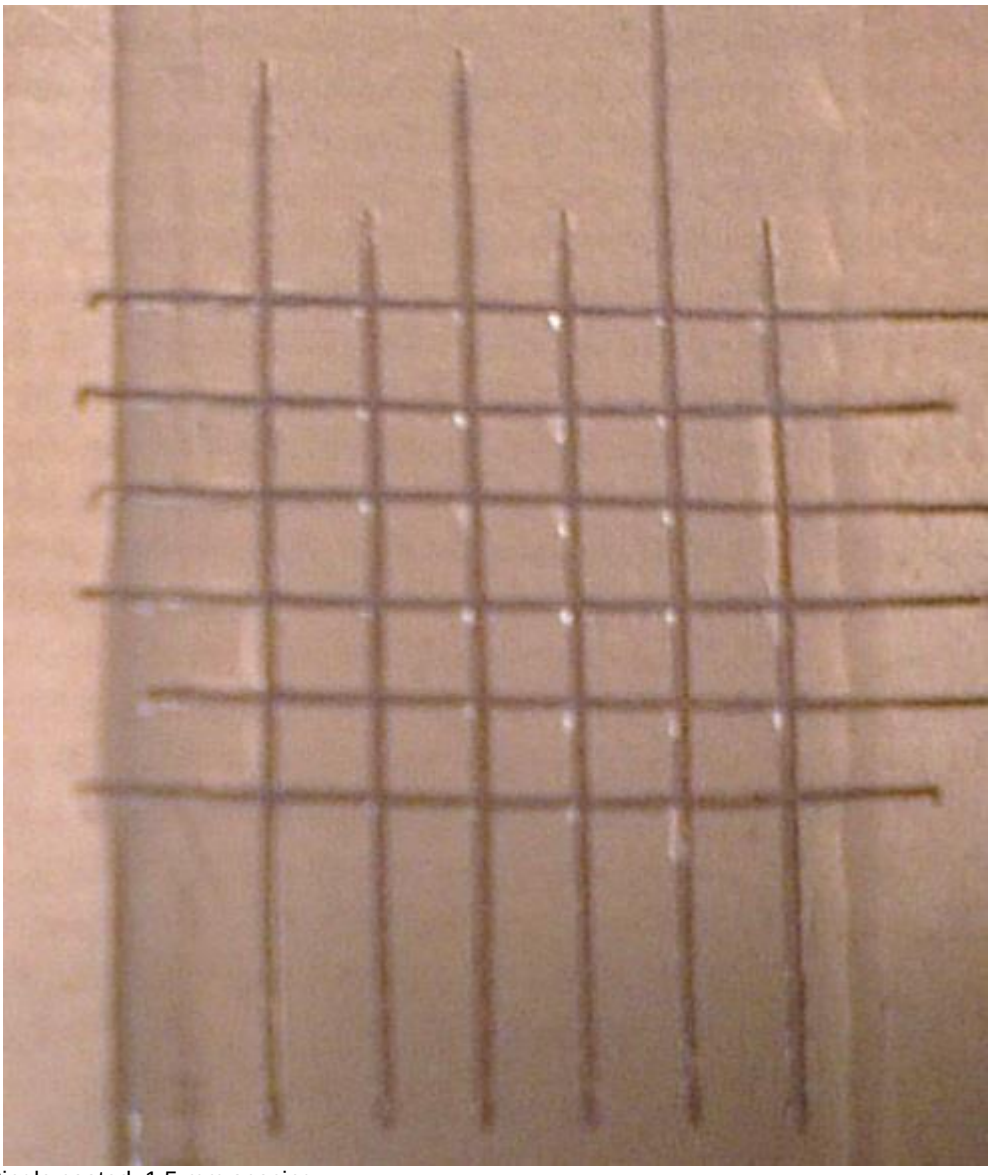


Picture 13-3: Double coated, 1,5 mm spacing (PASS)



Picture 13-4: Single coated board A, 1,5 mm spacing

CCQ – 13 – Tape test (adhesion test): (SH)



Picture 13-5: Single coated, 1,5 mm spacing

CCQ – 14 – Double coating: (SH)

Requirement/Specification:	Result/Measurement:	Status:
See specifications	See results (Concerning specific double coated requirement)	 PASS

Specification:

1-Color, 2-Viscosity, 3-SL 1307 HT Compatibility

- Varnish based, no additional testing

4-Process audit

- needs to be specified

5-Tinten test, 6-Zestron resin test, 7-Zestron flux test, 8-Ionic contamination

- minor or no intervention to single/double coated

9-Uniformity

- additional stress and equality
- proper bonds between layers

10-Thickness

- additional layer vs. requirements 25 – 75 µm

11-Adhesion (mash cut)

- difference, proper bond

12-High voltage test

- considering proper and tight bonding, additional test might not be required

13-Adhesion (tape test)

- see 11-Adhesion

Result:

9-Uniformity

- too thick layer creates wrinkles
- proper storage is required until second layer is touch dry (impurities, first layer is impaired and strong bond is created – during this time it needs to be protected)

10-Thickness

- only certain combinations of speeds are recommended

11-Adhesion (mash cut)

- perfect, class 0

CCQ – 14 – Double coating: (SH)

12-Dielectric withstanding voltage

- double coated was not tested (single coated NOK)

13-Adhesion (tape test)

- single issue was found (class 4 out of 5)
- ASTM specifies films up to 125 μm (while I consider several samples outside this condition)

Methods, test:

See respective chapter.

Documentation:

Many, see respective chapter.

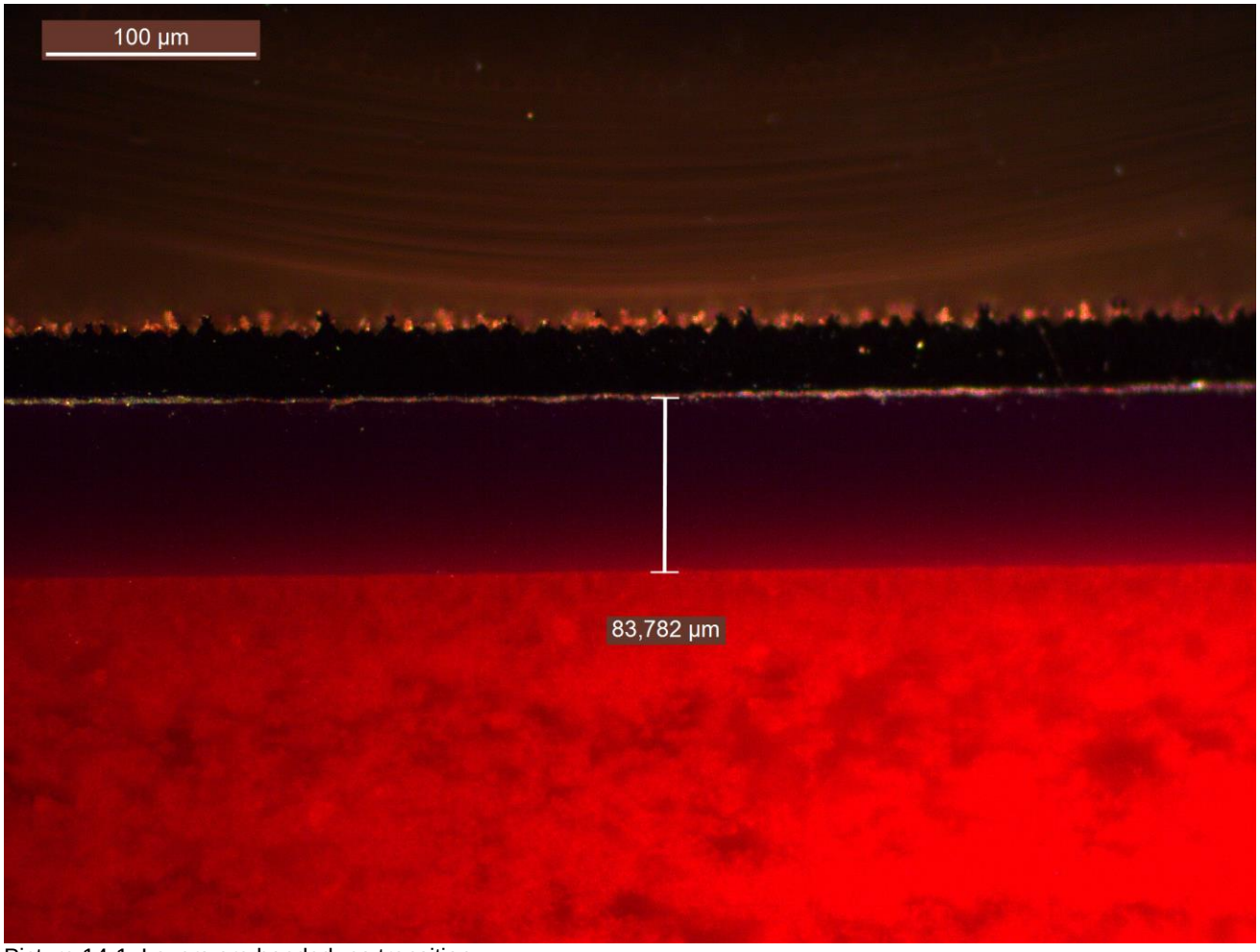
Evaluation:

Strong bonds are created between two layers. Even with prolonged periods of time, there is no transition (Picture 14-1).

Thickness within tolerances can be reached, when certain combinations of jet's speeds are used. It is critical as adhesion and layer's stability is disturbed.

CCQ – 14 – Double coating: (SH)

Attachments:



Picture 14-1: Layers are bonded, no transition

CCQ – 15 – Does CC meets the Quality?

Requirement/Specification:	Result/Measurement:	Status:
CC=>RTT	CC=>RTT	 PASS (see High voltage)

Specification:
Every specification is met or exceeds the results by RTT.

Result:
CC was proven to be good enough and is better in specific characteristics than RTT. Product A passed standard voltage test.

Methods, test:
See chapters 1 to 14.

Documentation:
See chapters 1 to 14.

Evaluation:
If required additional testing of thickness, uniformity, bonding and withstand voltage might be processed. From historical view only exact withstand voltage was not recorded (knowledge of mine and expert's opinion). Burned power source was examined in detail. Thicknesses and bonding was inspected. Uniformity and thicknesses were also evaluated during two project mapping RTT's performance.

We have not reached desired quality, but in several ways we exceeded RTT's. With proper working instructions and tuned programs, results are going to be prefect.

See attached picture 15-1, general table and dedicated chapters for detailed information.

CCQ – 5 – Tinten test: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Surface tension of the board > 40 $mN.m^{-1}$ (acc. Zestron)	41 – 44 $mN.m^{-1}$	 Our standard needs to be properly specified.

Specification:
Surface tension of the board is specified as > 40 $mN.m^{-1}$ (Schweigart, Helmut. EPP EUROPE SEPTEMBER / OCTOBER 2007. How clean do assemblies have to be?)

Result:
Results on unpopulated boards are between 41 – 44 $mN.m^{-1}$.

Methods, test:
Test is based on finding the liquid with specified surface tension that does not wet the board anymore. Picture 5-2-2 note, that dynamic behavior is inspected.

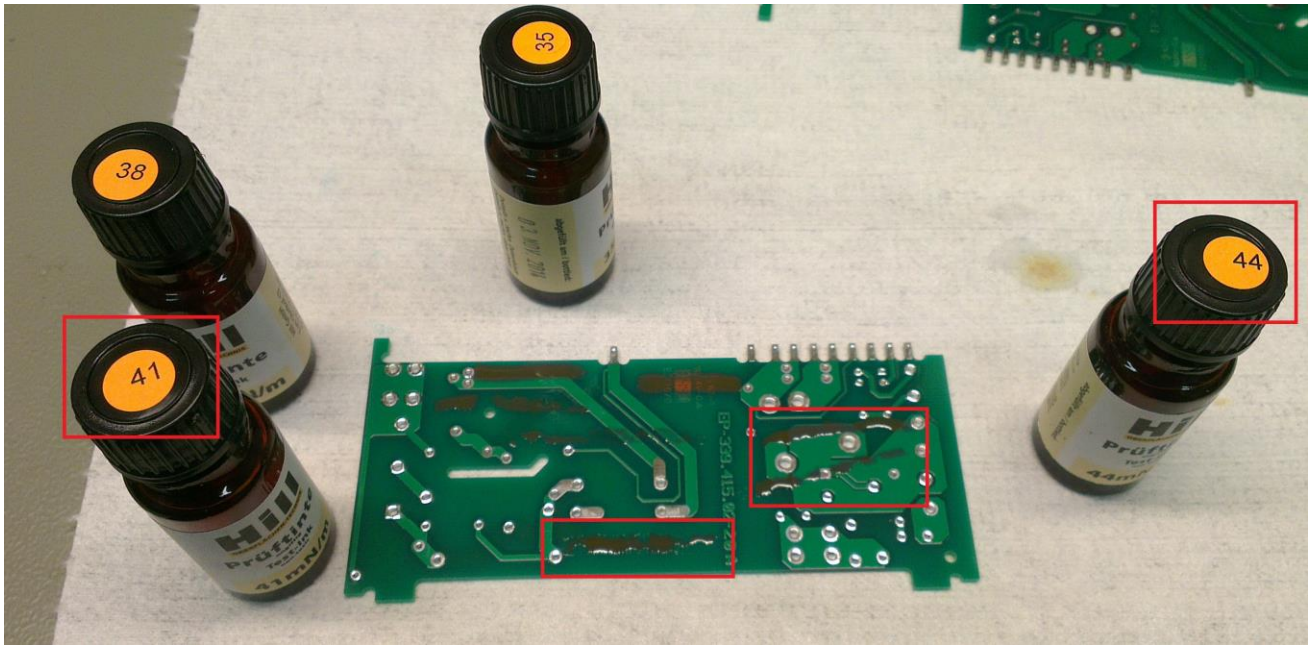
Documentation:
Product A

Wanzheng boards

Evaluation:
Critical is value before coating as surface is wetted with liquid while it's surface tension is lower than board's. Flux and cleaning the board rises the value, in a minor way, similar to the results. Standard for our boards and process needs to be adjusted. (See other qualification steps for informed decision.)

CCQ – 5 – Tinten test: (WZ)

Attachments:



Picture 5-2-1: Result between 41 – 44 mN/m

CCQ – 6 – Zestron resin test: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Test is negative. Test liquid does not indicate any flux residues.	Test is negative.	 PASS

Specification:

Test is negative. Test liquid does not indicate any flux residues.

Result:

Test found no residues on the delivered boards.

Methods, test:

Zestron resin test is applied on the board. After 3 minutes is washed away with demineralized or deionized water. Brown or yellow spots indicate residues.

Documentation:

Product A

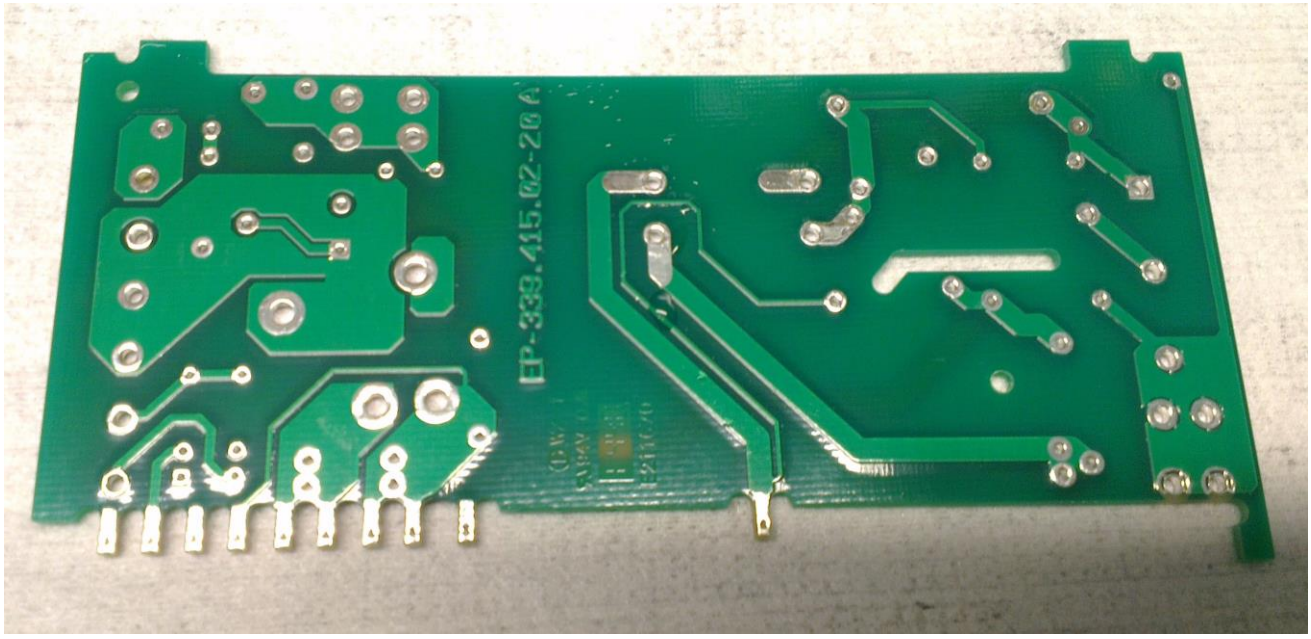
Wanzheng boards

Evaluation:

Delivered board is not affected. Result is **PASS.**

CCQ – 6 – Zestron resin test: (WZ)

Attachments:



Picture 6-2-1: No indication of the residues

CCQ – 7 – Zestron flux test: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Test is negative. Test liquid does not indicate any flux residues.	Test is negative.	 PASS

Specification:
Test is negative. Test liquid does not indicate any flux residues.

Result:
Test did not find any residues.

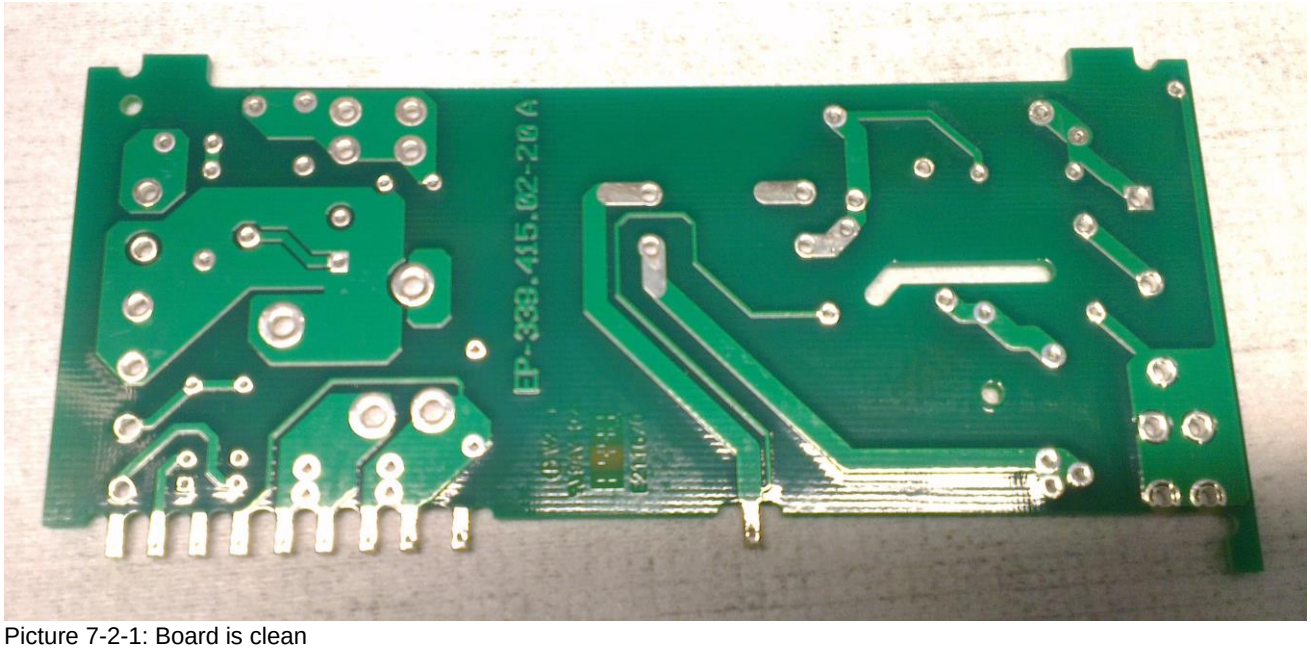
Methods, test:
Zestron flux test is applied on the board. After 1 minute test is washed away with demineralized or deionized water. Blue or white spots indicate residues.

Documentation:
Product A

Wanzheng boards

Evaluation:
Delivered boards are clean. Result is **PASS**.

Attachments:



Picture 7-2-1: Board is clean

CCQ – 8 – Ionic contamination: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
< 1,56 µg EQ NaCl.cm^{-2}	Delivered board passes the criteria. (see the evaluation)	 PASS

Specification:
IPC-TM-650, < 1,56 µg EQ NaCl.cm^{-2}

Result:
Module boards C are >6 µg EQ NaCl.cm^{-2}. EPs and Main board is < 1,56 µg EQ NaCl.cm^{-2}.

Methods, test:
IPC-TM-650, Method 2.3.25

Documentation:
Product A

Wanzheng boards

Evaluation:
Delivered board's contamination is within the specification. Although those results are very high for boards, that were not processed yet. For future test I would propose lower acceptance/critical level (0,3 – 0,4 µg EQ NaCl.cm^{-2}). Result is **PASS**.

Attachments:

EP-339.415.02-20A					
Contamination [µg . cm^{-2} EQ NaCl]					
1	2	3	4	5	µ
0,45	0,43	0,59	0,51	0,38	0,47

Table 8-2-1: Results

CCQ – 9 – Uniformity: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
See specification	Without any obstacles.	 PASS

Specification:
Any voids, holes, wrinkles, streaks, cracking, delamination, blistering, or peeling of the coating or other evidence of loss of adhesion, or discoloration of the conductors shall be reported. Any legends shall be clearly visible through the coating.

Result:
PASS

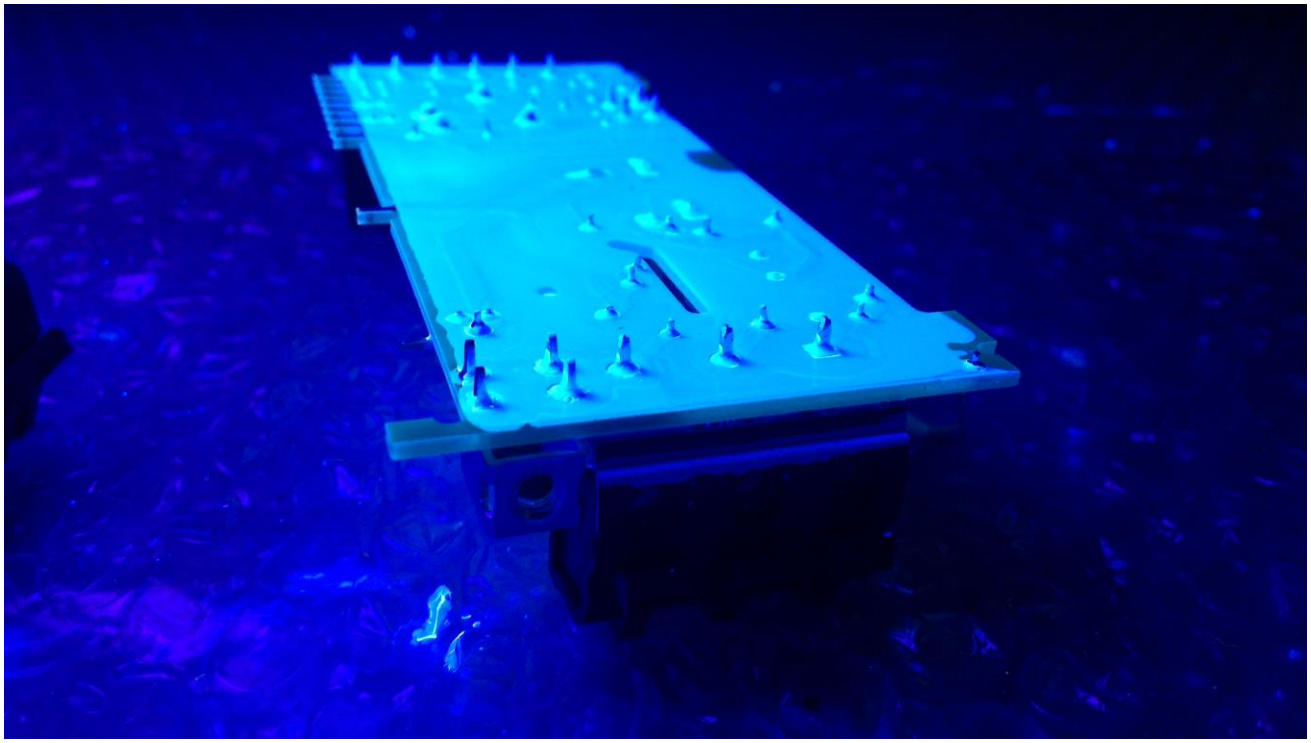
Methods, test:
Microsection

Documentation:
Wanzheng boards

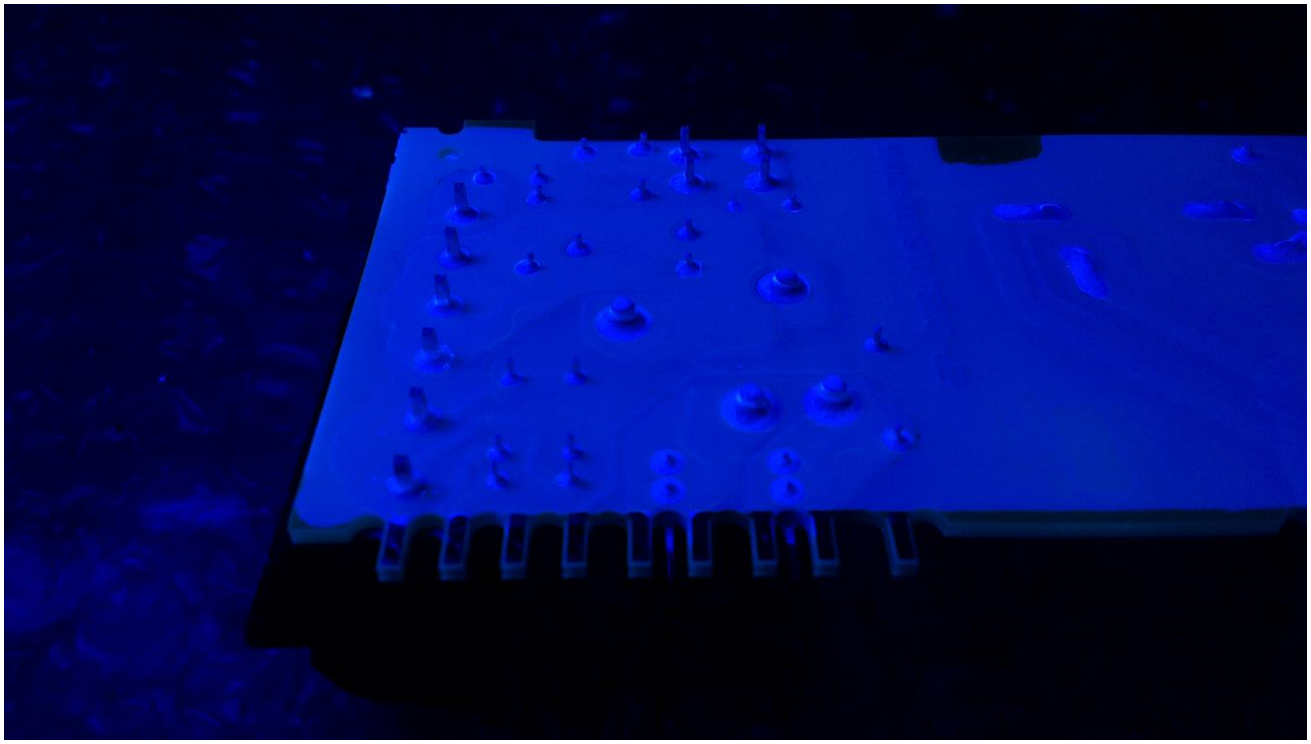
Evaluation:
There is one flaw and that is the lacquered terminal. As I have not seen this issue anywhere else, I would consider this a overcomable (acc documentation). From the point of view of the specification, it is PASS.

CCQ – 9 – Uniformity: (WZ)

Attachments:

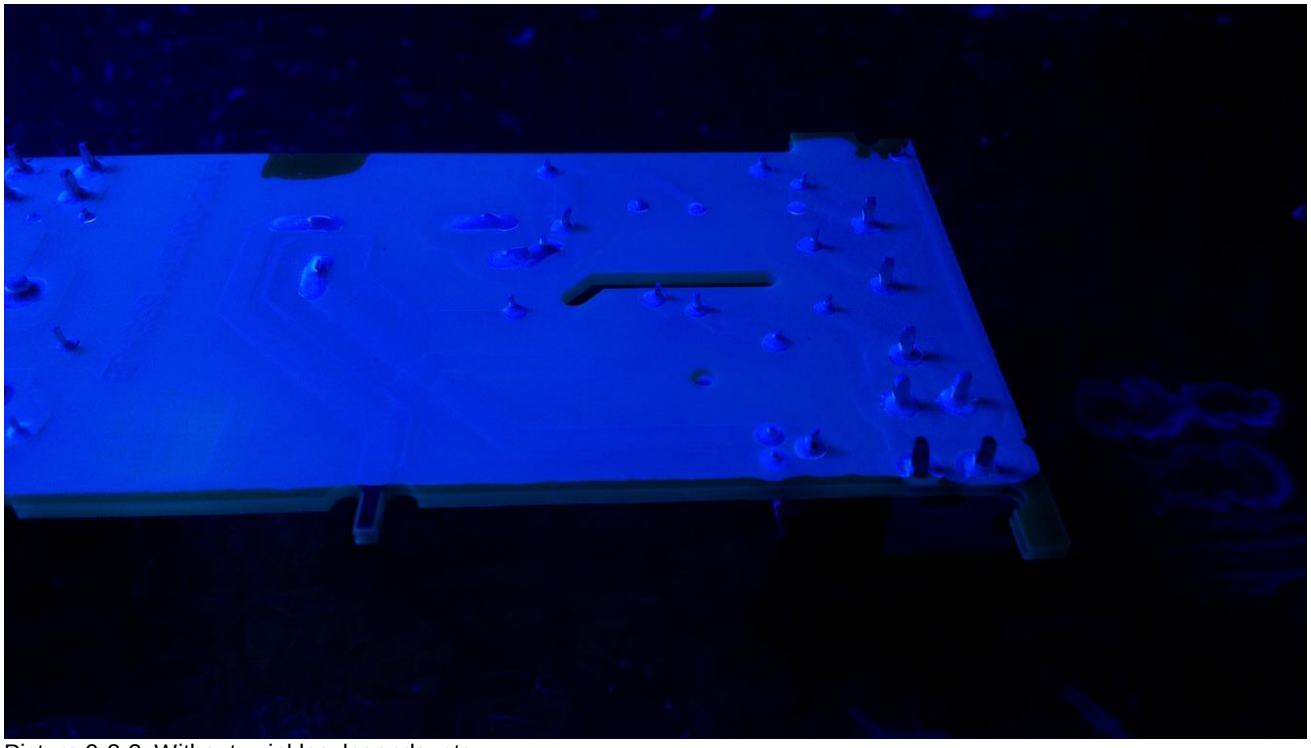


Picture 9-2-1: Lacquered terminal



Picture 9-2-2: Thick pins were microsectioned

CCQ – 9 – Uniformity: (WZ)



Picture 9-2-3: Without wrinkles, legends, etc.

CCQ – 10 – Thickness: (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Requirement 25 – 75 µm IPC J-STD-001 (30 – 130 µm) in dry state	See tables and pictures (pins are critical)	 PASS (conditions)

Specification:
Required thickness is 25 – 75 µm, IPC J-STD-001 states 30 – 130 µm

Result:
See attachment

Methods, test:
Ultrasonic measurements

Microsection

Calculation

Documentation:
Product A

Wanzheng boards

Evaluation:
Measured thickness is (mostly) in tolerances. There is no obvious distinction from the other supplier. Program for this board is optimized. Although edges on pins are still not properly coated, rest of the pin is. It seems agreeable to use more lacquer on the pins as it covers the conductor. While layer on bottom of the soldering is thick, on the sides of the pin, it is around the specified thickness.

Attachments:

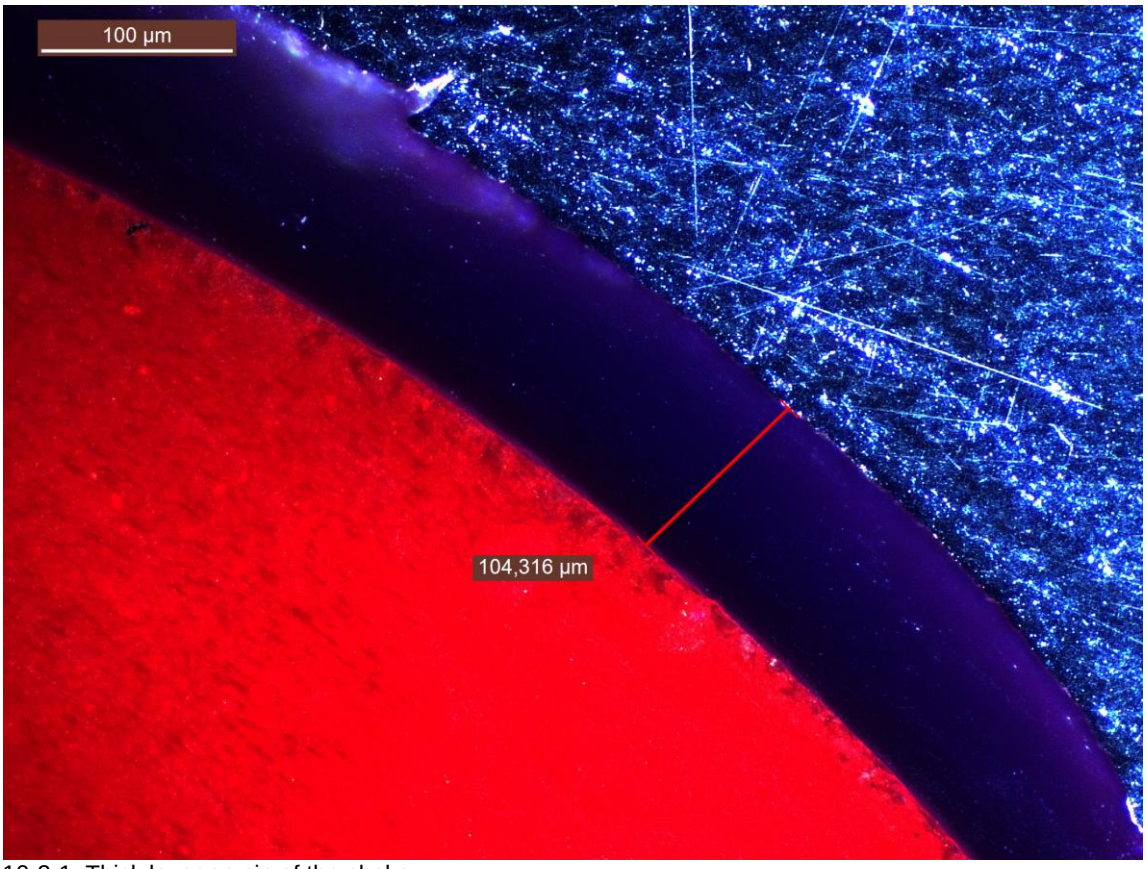
µ [µm]	σ [µm]	C [µm]
30,0	15,4	51

Table 10-1W: Board K by supplier WZ, on plain

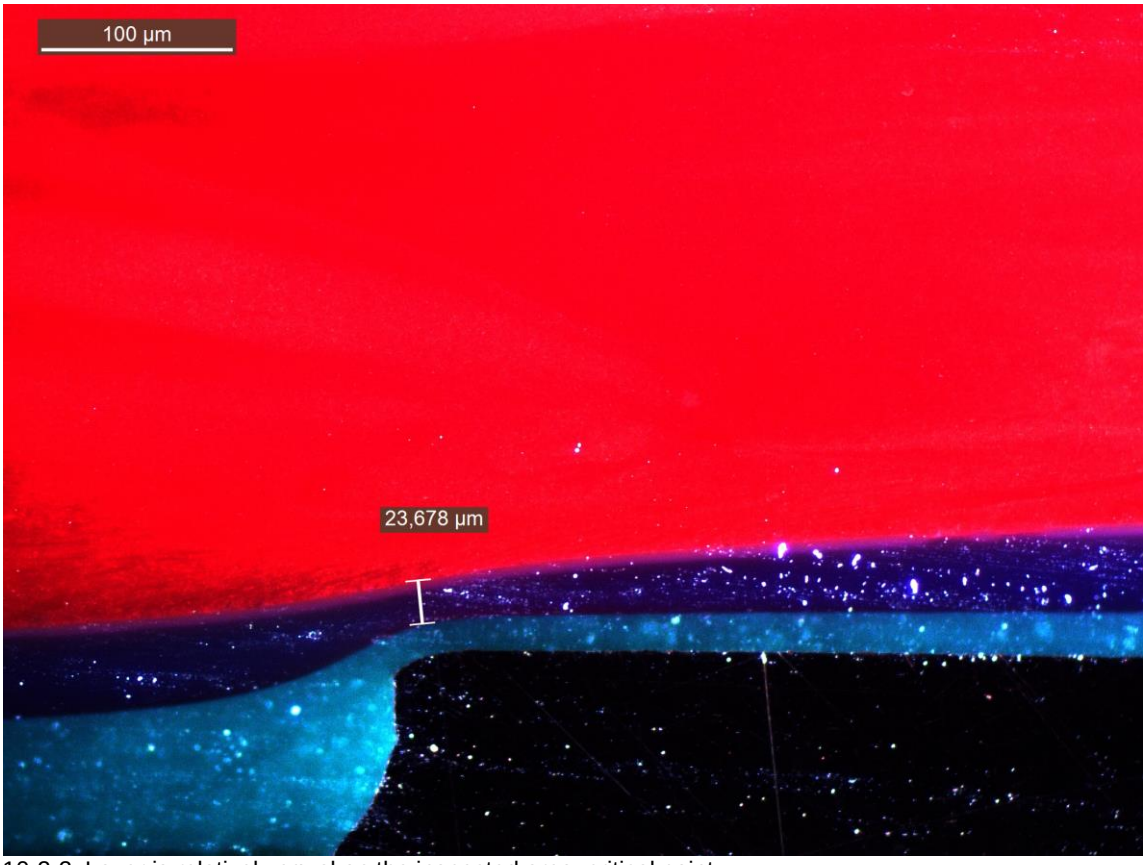
µ [µm]	σ [µm]	C [µm]
126,5	43,2	34

Table 10-2W: Board K by supplier WZ, around THT chokes (on TOP)

CCQ – 10 – Thickness: (WZ)

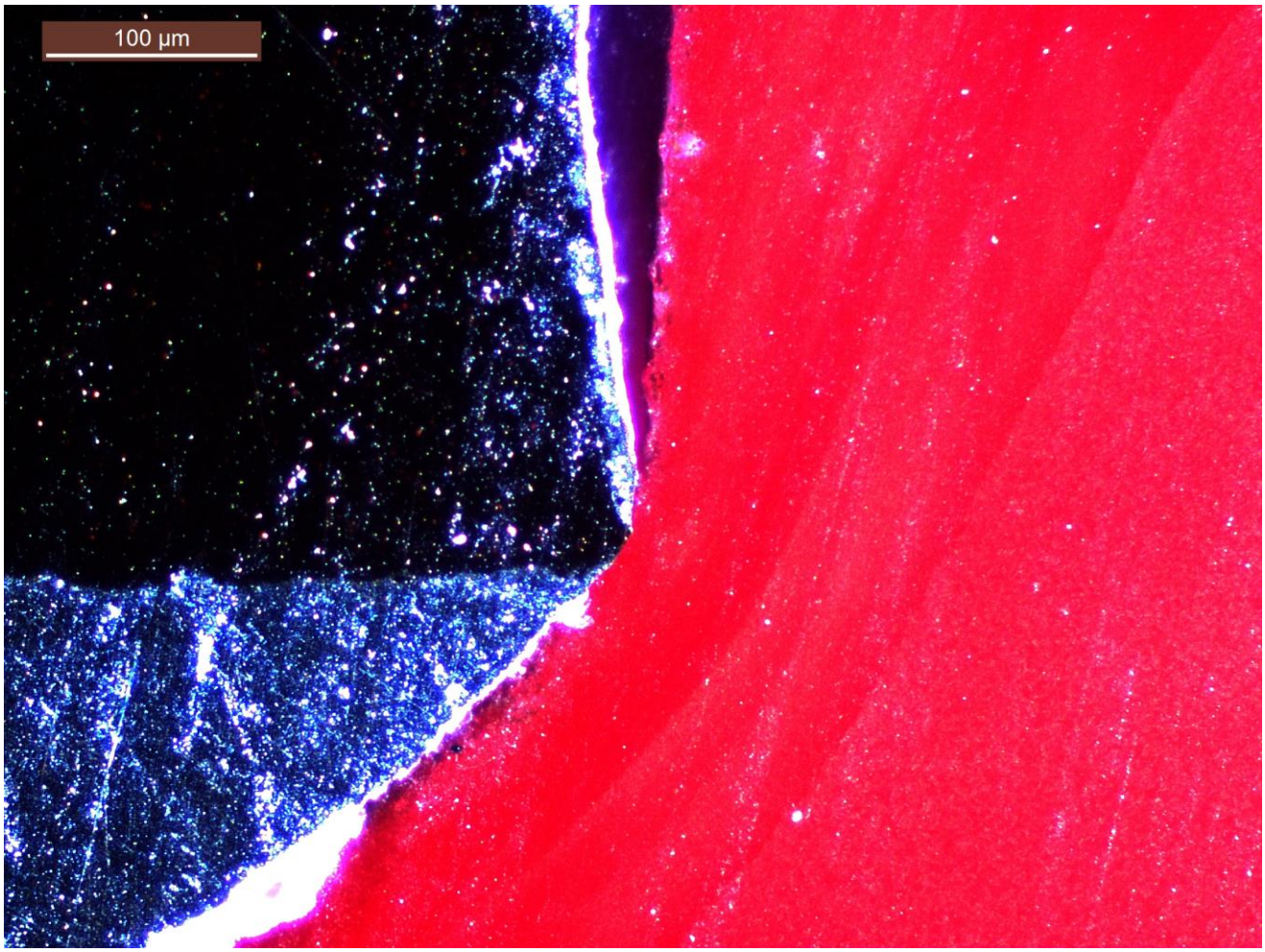


Picture 10-2-1: Thick layer on pin of the choke



Picture 10-2-2: Layer is relatively equal on the inspected area, critical point

CCQ – 10 – Thickness: (WZ)



Picture 10-2-3: Edges are still critical

CCQ – 11 – Mash cut (adhesion test): (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Class 0 acc. DIN EN 2409	Class 0	 PASS

Specification:
Class 0 acc. DIN EN 2409

Result:
Class 0

Methods, test:
DIN EN 2409 specifies procedure how to process and evaluate results. Coated copper sample board is cut with defined blade in 1, 2 or 3 mm spacing. Then it is stressed by scrubbing brush. Precise adhesive tape is used for tearing the coating apart. Percentage of affected area determinates the class.

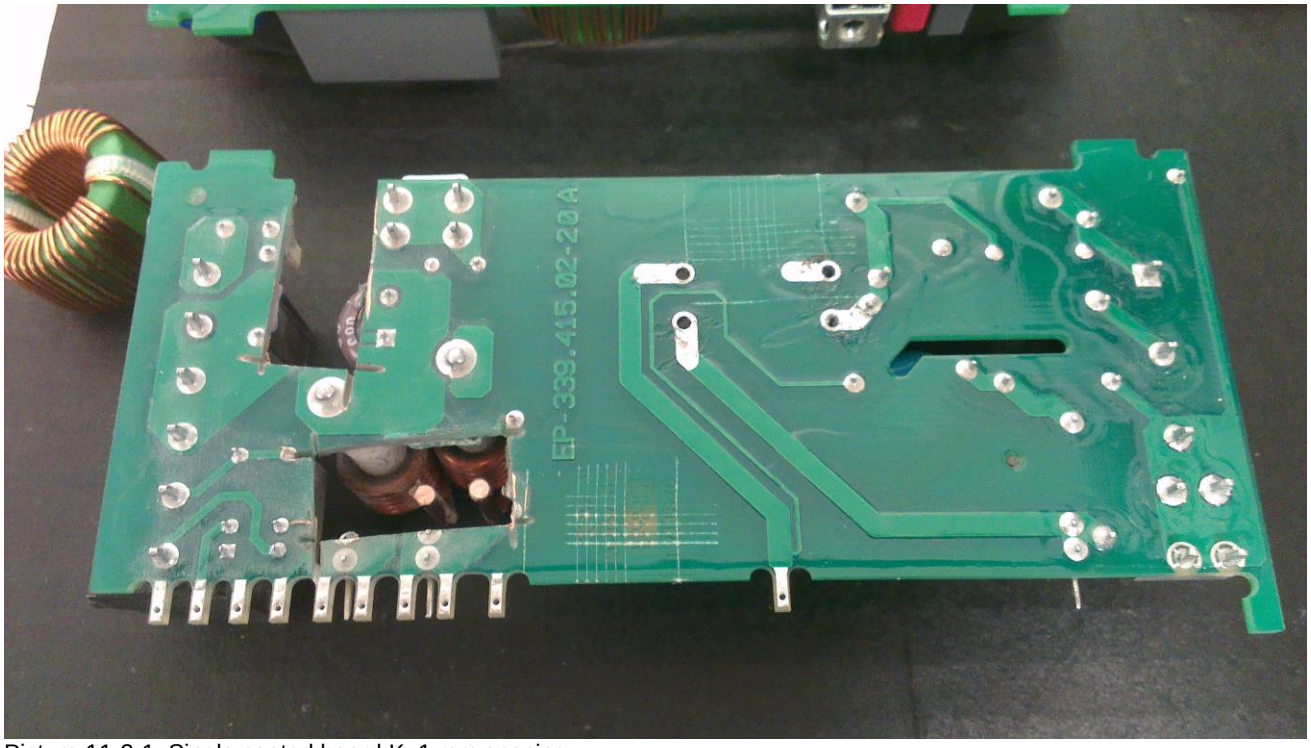
Documentation:
Product A

Wanzheng boards

Evaluation:
There are no issues at all – Class 0. Picture 11-1 is a bit misleading. Samples from WanZheng are same as from Suhang.

CCQ – 11 – Mash cut (adhesion test): (WZ)

Attachments:



Picture 11-2-1: Single coated board K, 1 mm spacing

Picture 11-2-2: Equipment

CCQ – 13 – Tape test (adhesion test): (WZ)

Requirement/Specification:	Result/Measurement:	Status:
Class 5 acc. ASTM 3359 Method B	Class 5	 PASS

Specification:
Class 5 acc. ASTM 3359 Method B

Result:
Class 5

Methods, test:
ASTM 3359 Method B specifies procedure how to process and evaluate results. Coated copper sample board is cut with defined blade in 1 and 1,5 mm spacing. Then it is stressed by scrubbing brush. Precise adhesive tape is used for tearing the coating apart. Percentage of affected area determinates the class.

Documentation:
Product A

WanZheng boards

Evaluation:
There are no issues at all – Class 5. Picture 13-1 is a bit misleading. Samples from WanZheng are same as from Suhang.

Attachments:

See 11-2-1 and 11-2-2.

CCQ – 12 – Withstand. voltage =>RTT:

Requirement/Specification:	Result/Measurement:	Status:
IPC-TM-650, 2.5.6.1; DIN EN 60243-1; CC 100 kV/mm, RTT 65 kV/mm	85 – 103 kV/mm RTT 23 – 75 kV/mm (see attachment)	 PASS

Specification:

100 $kV.mm^{-1}$, (acc. Datasheet from Peters, varnish SL 1307 FLZ 234)

65 $kV.mm^{-1}$, (acc. Datasheet from Peters, varnish SL 1306 N)

Result:

CC 85 – 103 $kV.mm^{-1}$ (see Attachments)

RTT 23 – 75 $kV.mm^{-1}$

Methods, test:

IPC-TM-650, 2.5.6.1

Breakthrough 3 times on each thickness (9 in total)

Thickness measured 10 times + microsection on each (9 times 10 in total)

RTT measured 3 times

Documentation:

Product A

specification of the varnish

HIOKI 3153 Withstanding HITESTER

Ultrasonic thickness measurement

Evaluation:

RTT's inequality is very high, it is even in contradiction to the measured samples on lacquered power devices. There is around twice the thickness on edges (1 cm wide). A lot of wrinkles and impurities are present on the evaluated sample. Those were source of the very low withstanding voltage. Withstanding voltage is PASS in case of a better sample (good sample would not be a proper term as there are still impurities).

Note: With those samples I have to reevaluate my opinion (backed up by measurements) about RTT's better equality.

Our process and samples **are considered as =>** RTT's.

CCQ – 12 – Withstand. voltage =>RTT:

Attachments:

$$E = \frac{U}{d} = 26{,}7\ kV.mm^{-1}$$

E is calculated with minimal thickness and given voltage.

Calculation 12-1R: Withstanding voltage

Voltage [V]		E [kV.mm^{-1}]	
660	770	22,9	26,7

Thickness [µm]				
30,7	36,8	30,6	31,4	31,5
32,2	29,1	30,9	28,8	33,2

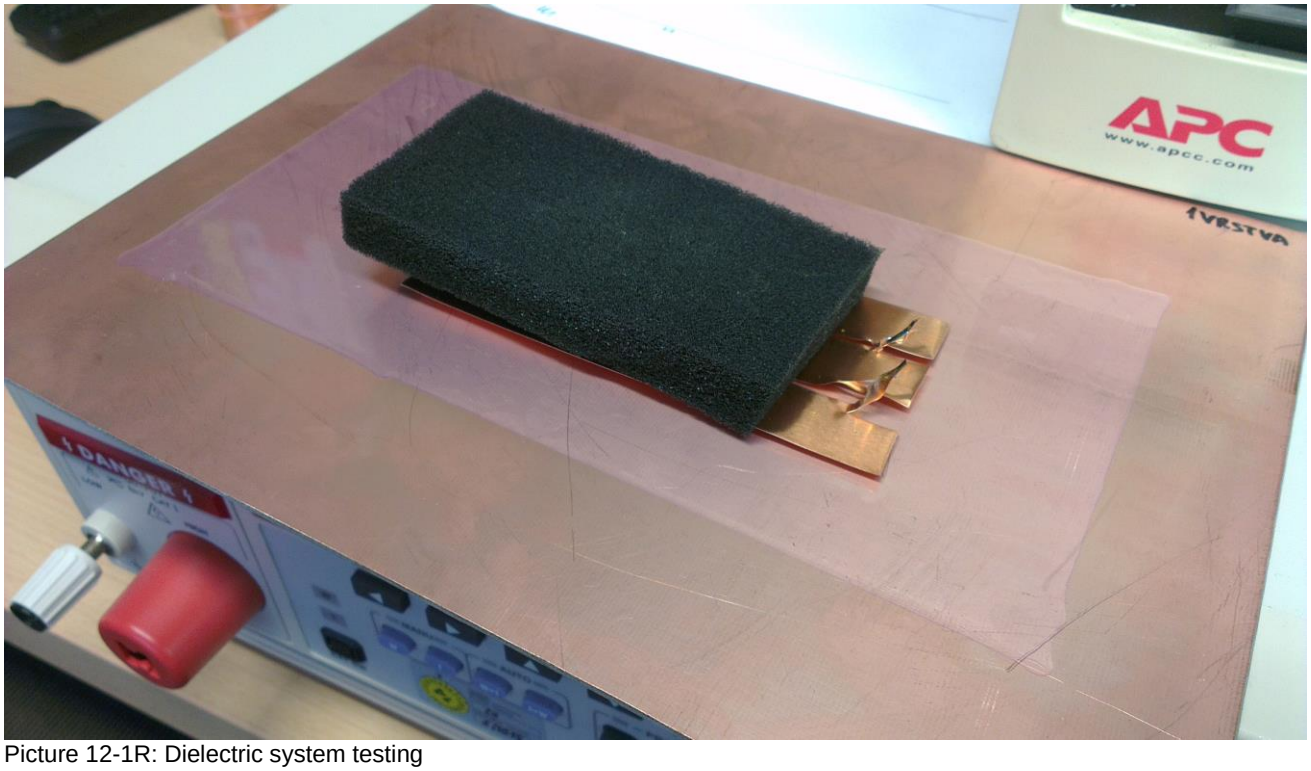
µ [µm]	σ [µm]	C [%]	Min [µm]
31,5	2,3	7	28,8

Voltage [V]	E [kV.mm^{-1}]
3000	74,8

Thickness [µm]				
40,5	46,8	48,9	67,9	45,3
40,7	62,0	40,1	48,7	68,5

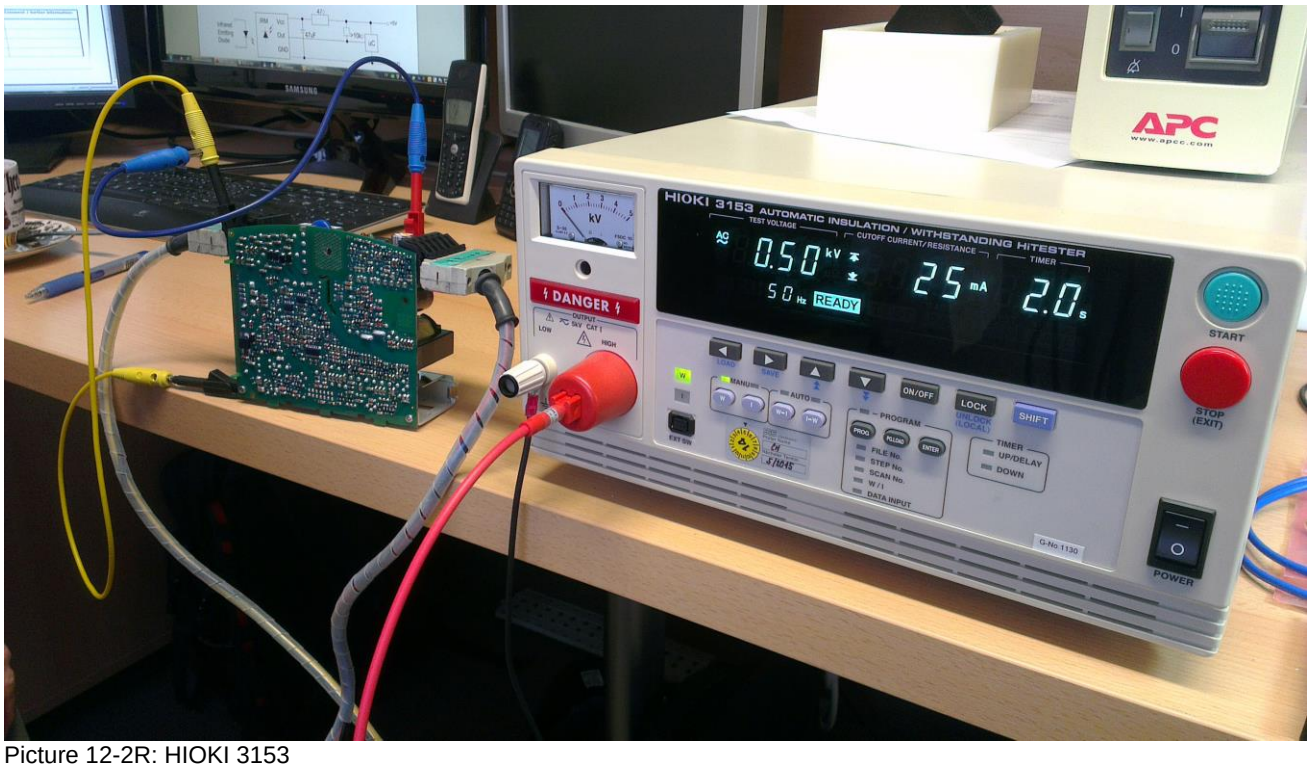
µ [µm]	σ [µm]	C [%]	Min [µm]
50,9	11,1	22	40,1

Table 12-1R: RTT Withstanding voltage

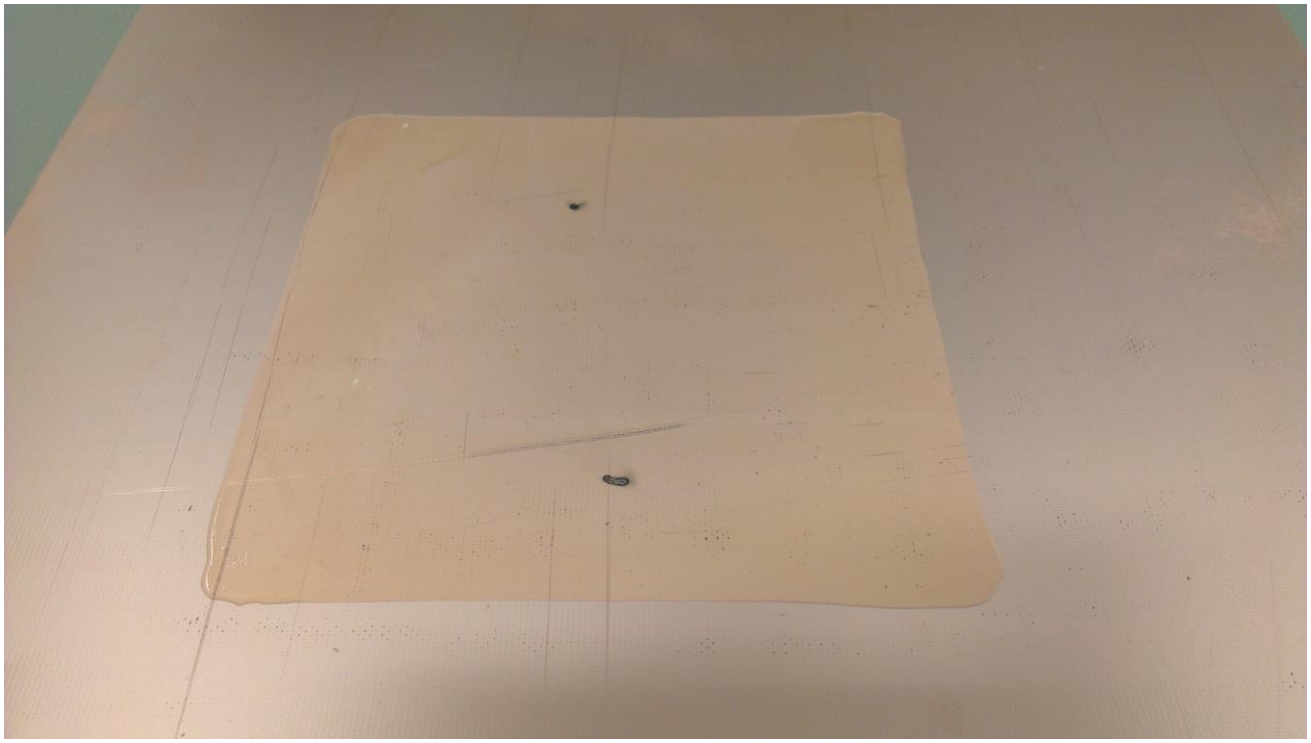


Picture 12-1R: Dielectric system testing

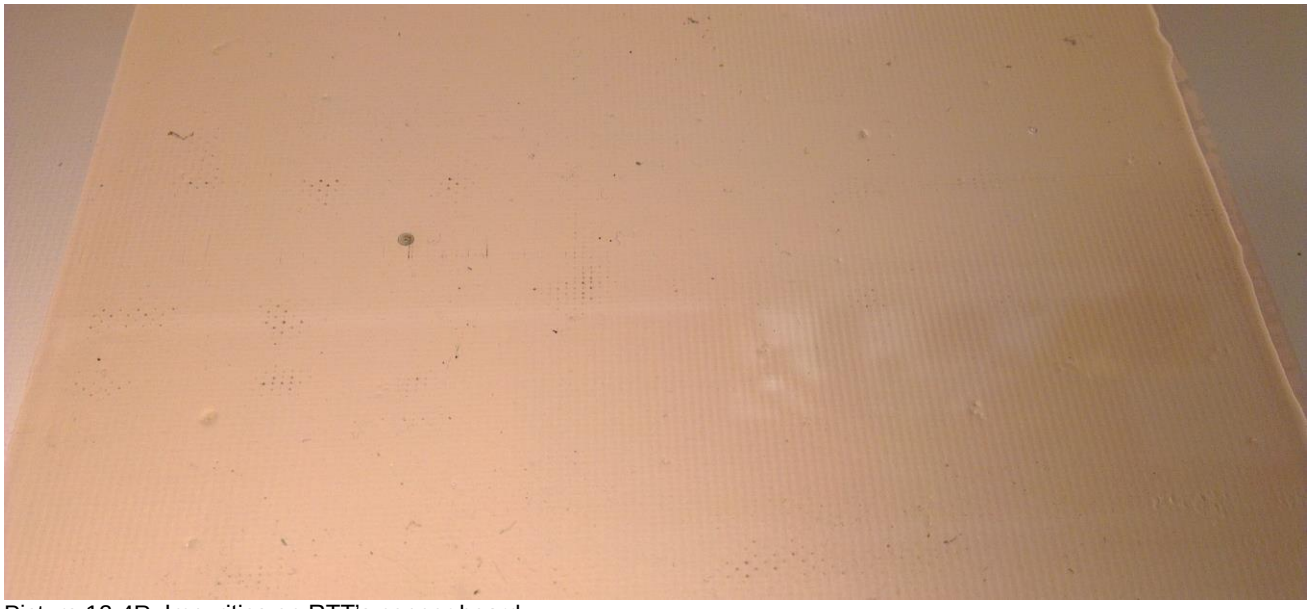
CCQ – 12 – Withstand. voltage =>RTT:



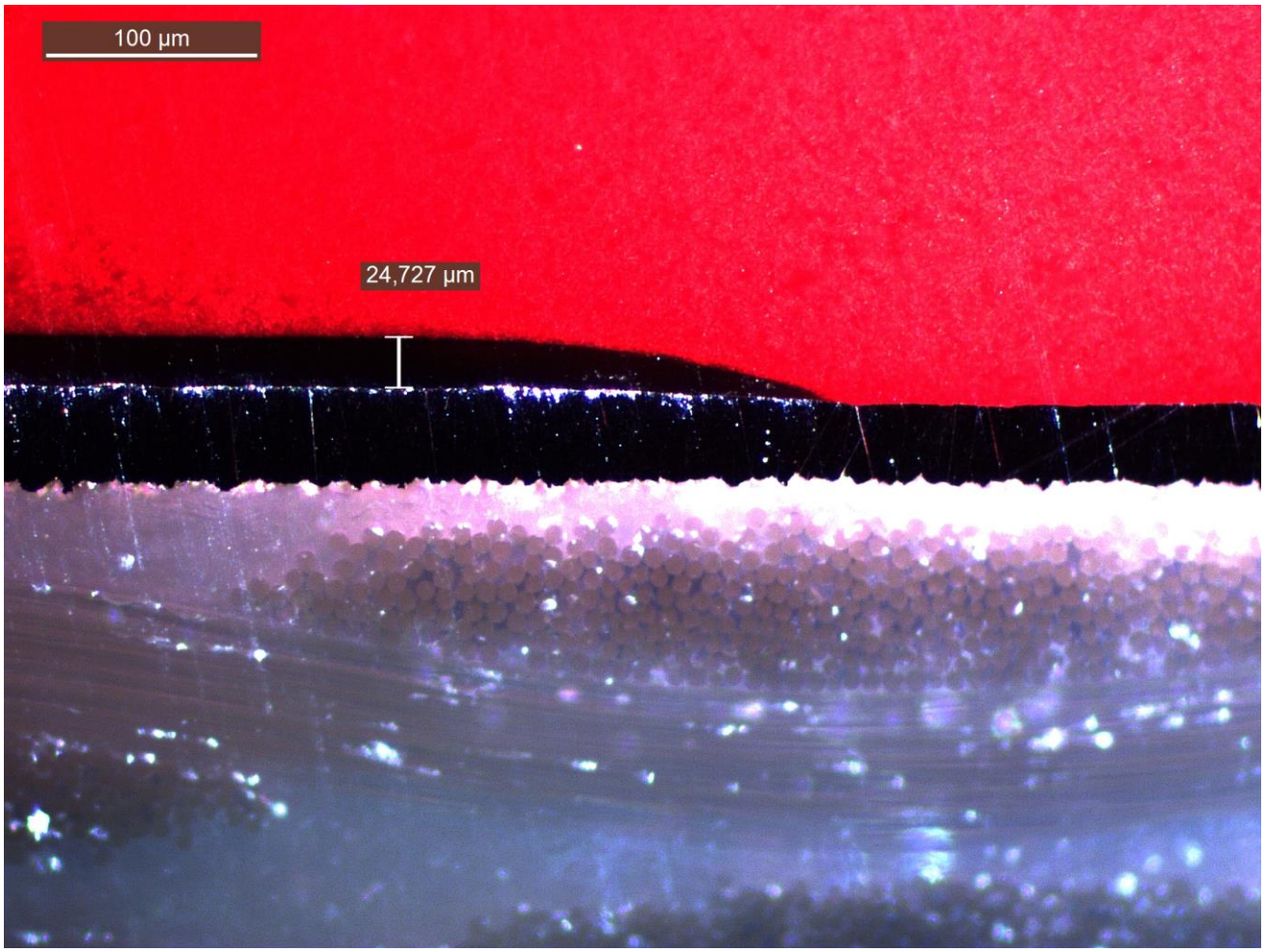
Picture 12-2R: HIOKI 3153


Picture 12-3R: Breakthrough RTT

CCQ – 12 – Withstand. voltage =>RTT:



Picture 12-4R: Impurities on RTT's copper board



Picture 12-5R: Microsection of breakthrough (770V, resulting in 31,7 kV/mm

IPC boards evaluation:

Sample boards: IPC-B-25A

Overview:

Partnumber	Manufacturer:	Solder mask:	Fail:	Note:
IPC board A	EPN	Peters LPEMER	0,00%	Two materials
		TYPE GL2467SM-DG		
		UL: E80215		
IPC board B	WANZHENG	KUANG SHUN	100,00%	Areas around fiducials
		TYPE KSM-S6188/KSM-18		
		UL: E189912		
IPC board C	SUHANG	Shenzhen Rongda	0,00%	Perfect
		TYPE H-9100		
		UL: E203293		
IPC board D	SUHANG	JiangSu Himonia	55,56%	22,22 % wide area 33,33 % small area
		TYPE HSR-200 GK52S		
		UL: E338120		

Table 17: Coating results

Partnumber:	Manufacturer:	Surface tension [mN . m^{-1}]	Ionic contamination [µg EQ NaCl . cm^{-2}]
IPC board A	EPN	35	0,05
IPC board B	WZ	48	0,95
IPC board C	SH	38	3,12
IPC board D	SH	48	2,20

Table 18: Quality of boards (notice those with different behavior)

Evaluation:

Reason for the coating was to prepare a test. I have not assumed that the preparation will evolve into a test. This do not alter results neither jeopardize the evaluation of the tests suggested by IPC.

There is clear positive correlation between surface tension and ionic contamination. It is important as similar progress was documented in the production process.

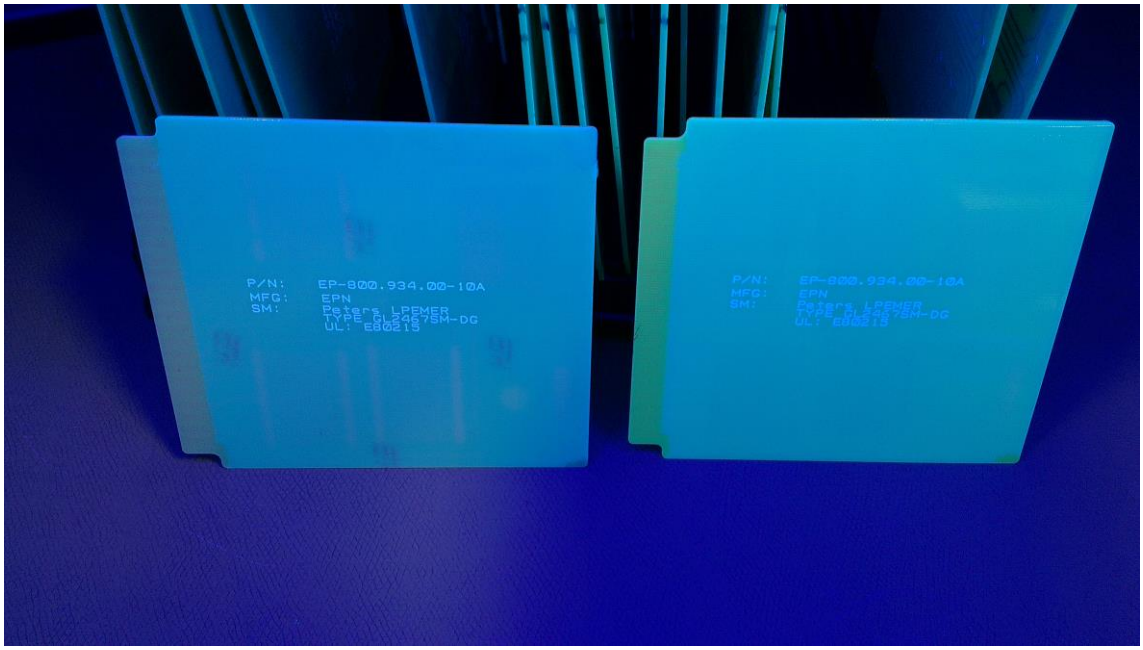
Although knowledge tells us, that with higher surface tension of the board, coating should be easier, this test proved the opposite.

Common sense also suggests, that more samples wet a board, the better. Coating acted differently.

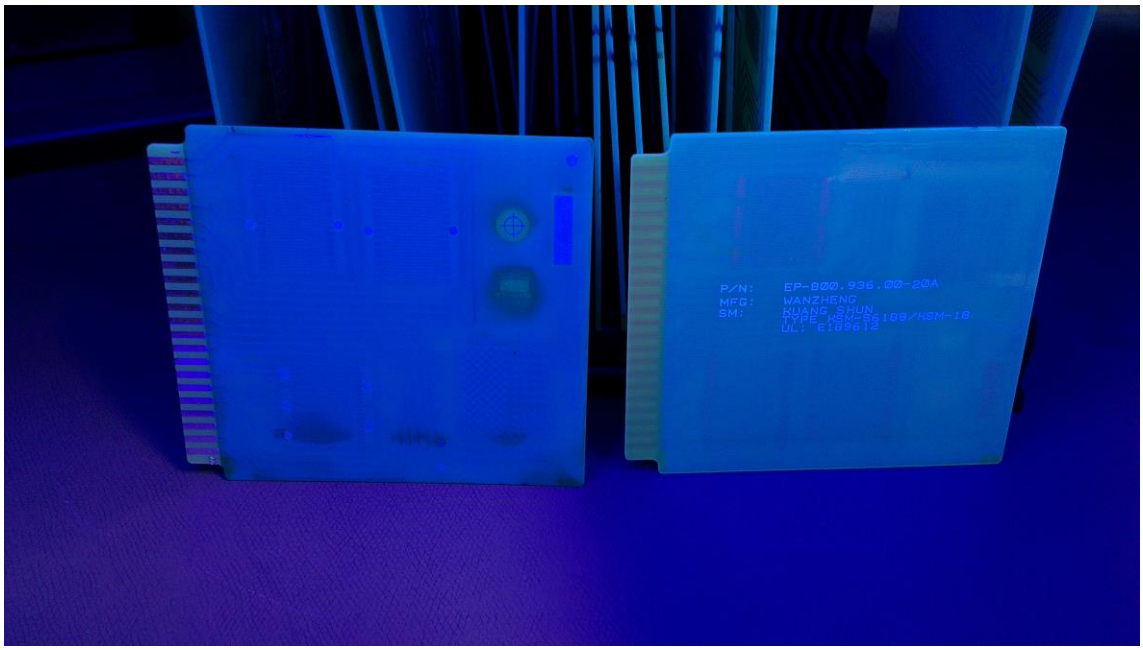
After cleaning the IPC board B in isopropyl alcohol (IPA, C_3H_7OH) wettability of boards drastically improved (2 out of 2 were ok, instead of 0 out of 9).

IPC boards evaluation:

Pictures:

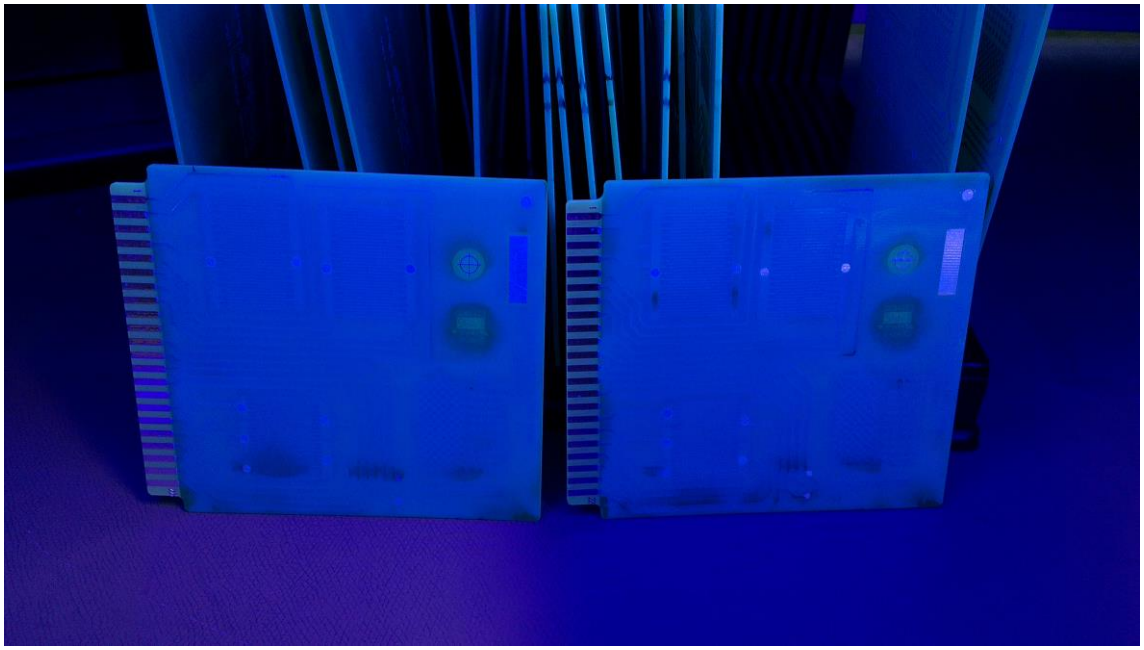


Picture 1: IPC board A, two different materials (note color + legend)



Picture 2: IPC board B, issues with base material? Fiduals

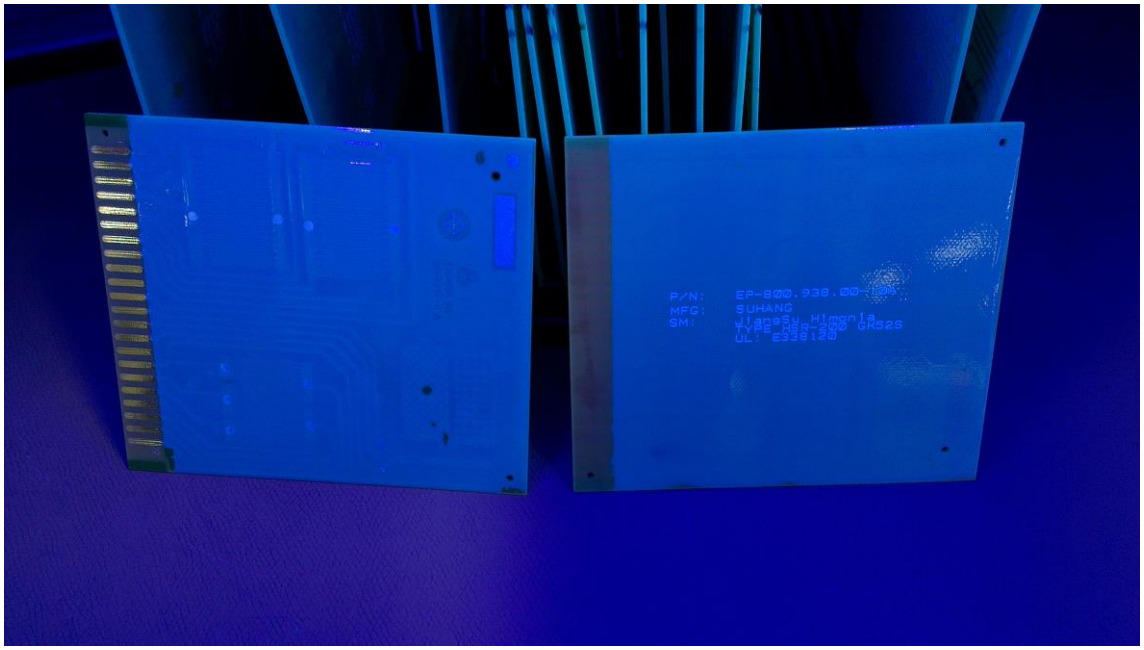
IPC boards evaluation:



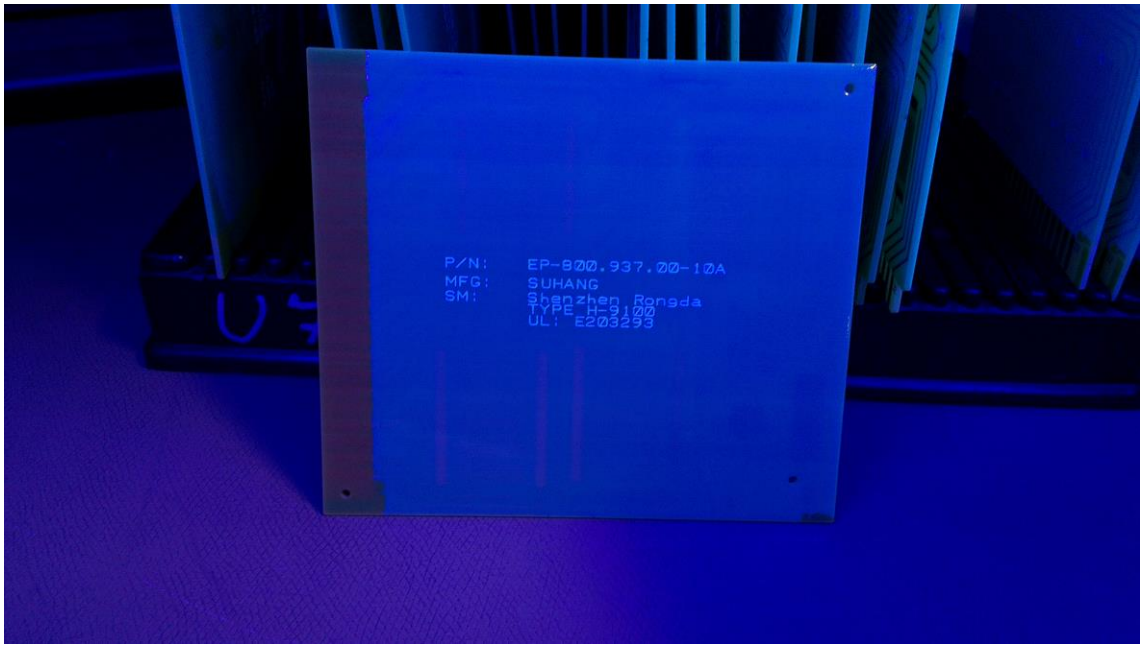
Picture 3: IPC board B, issues with base material? Fiducial

Picture 4: IPC board D, wide area

IPC boards evaluation:

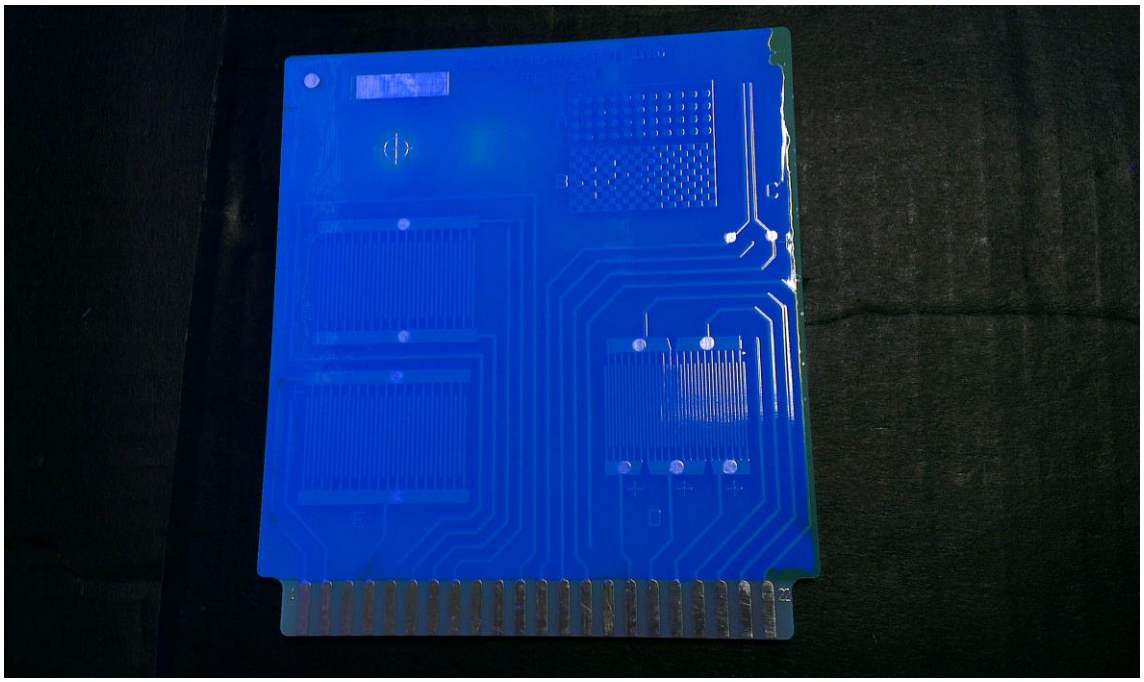


Picture 5: IPC board D, small areas

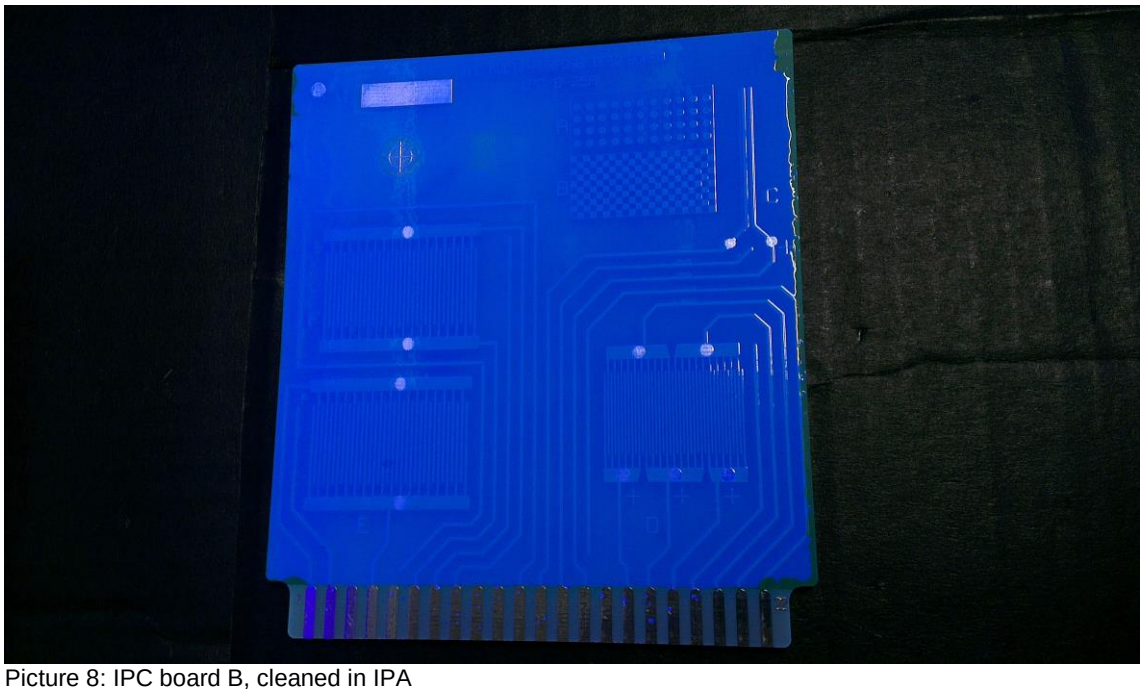


Picture 6: IPC board C, notes to SM

IPC boards evaluation:

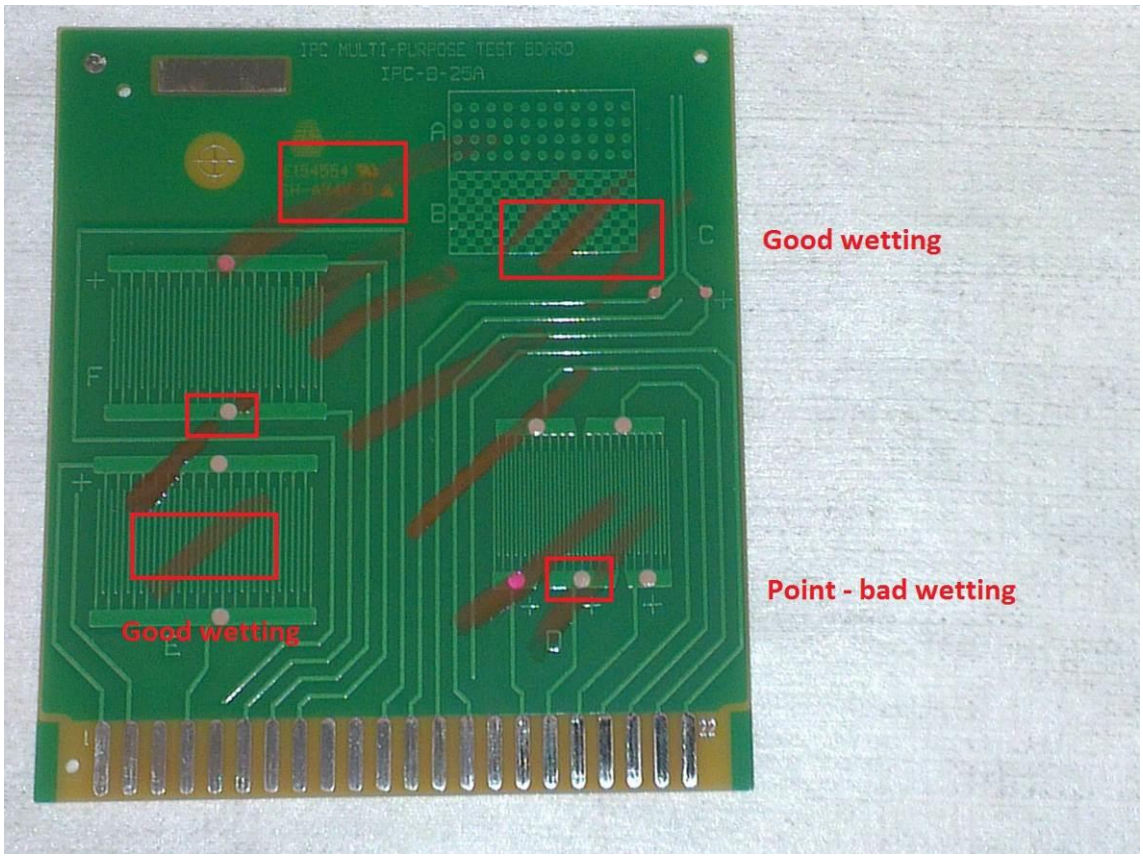


Picture 7: IPC board B, cleaned in IPA



Picture 8: IPC board B, cleaned in IPA

IPC boards evaluation:



Picture 9: IPC board C, Wettability

Conclusion:

Crucial assembly issues are proper activation of paste during reflow process. Ionic contamination is directly linked to pad density, therefore complexity of the board have to be inspected before any verdicts are made. Resin residues come with this inability to activate the paste. Solder wave can add lot of additional ionic contamination. It depends on maintenance of the production line.

Soak temperature is important in order to decrease contamination. Devices must withstand this change thermally. By volume, contents in air are not as important. No correlation to the contamination was found.

Quality parameters quantification of coating process led to success. Coating process delivers good results and characteristics of the lacquer are as specified in provided datasheet. Therefore company coating can be used instead of outsourced one. Minor nonconformities of the production are conditionally accepted and improvement can began.

Literature:

IPC-TM-650. Environmental test methods

IPC-A-610. Acceptability of printed boards

ISO 2431. Paints and varnishes. *Determination of flow time by use of flow cups*

DIN ISO 2409, Paints and varnishes. *Cross-cut test*

ASTM D3359, Standard Test Methods for Measuring Adhesion by Tape Test

Schweigart, Helmut. EPP EUROPE SEPTEMBER / OCTOBER 2007. *How clean do assemblies have to be?*

List of abbreviations:

IPC - International trade association for the printed-board and electronics assembly industries

IEC – Independent Electoral Commission

ASTM - American Society for Testing and Materials

DIN - Deutsches Institut für Normung

EN – European standards

ISO - International Organization for Standardization

SMT – Surface-mount technology

SMD – Surface-mount device

THT – Through-hole technology

MSL – Moisture sensitivity level

MBB – Moisture barrier bag

PCB – Printed circuit board

PCBA – Printed circuit board assembled

RLP – Reflow side of the PCB

WLP – Wave soldering side of the PCB

RTZ/ZRT – Resin test Zestron/Zestron resin test

FTZ/ZFT – Flux test Zestron/Zestron flux test

CC – Conformal coating (line)

IPA – Isopropyl alcohol

DI-water – Deionized water

CN - China

CZ - Czech

HT – Highly thixotropic

HV – High voltage

EPN – supplier of PCB

RTT – supplier of CC

WZ – supplier of PCB

SH – Supplier of PCB

WEK/IGC – Wareneingang Kontrolle/Incoming goods control