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F3

Faculty of Electrical Engineering
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Modeling of Spiral Polysilicon Divider in High Voltage MOSFET Transistor and Leakage

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Declaration

I declare that my doctoral dissertation thesis was prepared personally and bibliography used duly cited. This thesis and the results presented were created without any violation of copyright of third parties.

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Abstract

The power consumption is one of the most important integrated circuit parameters. It is crucial to know the circuit's estimated leakage power since such a bound will enable the designers to ensure that the circuit meets the standby power constraints which impacts battery life in portable devices. It means that the leakage of MOSFET devices have to be modeled accurately. The first fundamental thesis aim is the accurate gate dimension dependent drain and source leakage modeling. The second fundamental thesis aim is the enhanced model of high voltage spiral divider that allows designing of circuits that can actively control the power consumption.

The leakage current in standard MOSFET models (BSIM3/BSIM4) is typically modeled by drain-bulk and source-bulk diodes. This modeling method does not consider the impact of several parasitic bipolar devices. For the accurate modeling the impact of the following bipolar transistors has to be considered: a lateral bipolar transistor drain-bulk-source, a vertical bipolar transistor drain-bulk-substrate (only in isolated structures), and a vertical bipolar transistor source-bulk-substrate (only in isolated structures). For example, the drain or source leakage as a function of gate length cannot be modeled without the scalable parasitic bipolar devices. This thesis demonstrates the structure of a proposed macro model, implemented scalability (in most cases nonlinear), developed scaling equations, and physical explanation of this scaling.

The splitting of the scaling equations to the area, perimeter and constant segments makes the higher geometry accuracy than the using a conventional area factor scaling. The parasitic BJTs are not active when MOSFET operates in the standard regime in ON state and take part only in drain and source leakage in OFF state or in non-standard operation where drain-bulk or source-bulk junction is in forward regime.

Finally, the comparison of measured data vs. simulation is presented in order to confirm the model validity. This model improvement solves not only leakage current scaling, but it also accounts for additional parasitic bipolar effects, such as current injection to the substrate.

Next chapters deal with the enhanced accurate DC and RF model of nonlinear spiral polysilicon voltage divider. The high resistance polysilicon divider is a sensing part of the high voltage start-up MOSFET transistor that can operate up to 700 V. The strong electric field in low doped drain drift area located under the low doped polysilicon spiral divider causes a lot of parasitic effects that have a significant influence on DC and RF device characteristics and makes divider ratio voltage and frequency dependent.

This thesis presents the structure of a proposed model, implemented voltage, frequency and temperature dependency, and scalability. A special attention is paid to the ability of the created model to cover the mismatch and influence of a variation of process parameters on the device characteristics. The statistical process variation model is created based on measurement about 30000 devices and mismatch model is based on measurement about 3000 devices.

The modeling results are compared with measured data and the maximal relative model error of the divider ratio is less then 1.1 % and a typical application is also demonstrated.

Keywords: High voltage start-up MOSFET, pinch-off, high voltage spiral divider, leakage current, MOS, LDMOS, modeling, characterization, parameter extraction, statistical modeling.

Abstrakt

Spotřeba energie je jedním z nejdůležitějších parametrů integrovaných obvodů. Je velmi důležité znát odhadovanou velikost svodového proudu, což návrhářům umožní zajistit, aby obvod splňoval požadavky na pohotovostní režim, který má vliv na výdrž baterie v přenosných zařízeních. To znamená, že svodový proud v MOS tranzistorech musí být modelován přesně. Prvním zásadním cílem práce je přesné modelování svodového proudu drainu a source závislého na rozměrech hradla. Druhým zásadním cílem práce je vylepšený model vysokonapěťového spirálového děliče, umožňující navrhování obvodů, který může aktivně řídit spotřebu energie.

Svodový proud ve standardních MOSFET modelech (BSIM3/BSIM4) je typicky modelován diodami drain-bulk a source-bulk. Tato metoda nebere v úvahu vliv několika parazitních bipolárních tranzistorů. Pro přesné modelování vliv následujích bipolárních tranzistorů musí být vzat v úvahu: laterální bipolární tranzistor drain-bulk-source, vertikální tranzistor drain-bulk-substrát (v i izolovaných strukturách) a vertikální tranzistor source-bulk-substrát (v i izolovaných strukturách). Například svodový proud drainu a source jako funkce délky hradla nemůže být modelován bez parazitních bipolárních tranzistorů závislých na rozměru hradla. Tato práce demonstruje strukturu navrženého makro modelu, implementovanou rozměrovou závislost (ve většině případů nelineární), vyvinuté rozměrově závislé rovnice a fyzikální vysvětlení.

Rozdělení rozměrově závislých rovnic na složku plošnou, obvodovou a konstantní způsobuje větší přesnost modelu než použítí konvenční závislosti přes faktor plochy. Parazitní BJT nejsou aktivní, když MOSFET pracuje ve standardním režimu v ON stavu, ale mají vliv na svodový proud, pokud je MOSFET v OFF stavu nebo v nestandardním zapojení, kdy je drain-bulk nebo source-bulk přechod v propustném stavu.

Nakonec je prezentováno porovnání měřených a simulovaných dat, aby se potvrdila platnost modelu. Toto vylepšení modelu řeší nejen závislost svodového proudu na rozměru hradla, ale bere v úvahu také další bipolární efekty, například injekci nosičů do substrátu.

Další kapitoly se zabývají vylepšeným přesným DC a RF modelem nelinárního spirálového polykřemíkového napěťového děliče. Vysoce rezistivní polykřemíkový dělič je snímací částí vysokonapěťového start-up MOSFET tranzistoru, který může pracovat až do 700 V. Vysoké elektrické pole v nízko dotovaném polykřemíkovém spirálovém děliči způsobuje mnoho parazitních efektů, které mají významný vliv na DC a RF charakteristiky součástky a způsobuje napěťově a frekvenčně závislý poměr děliče.

Práce prezentuje strukturu navrženého modelu, implementovanou napěťovou, frekvenční, teplotní a rozměrovou závislost. Speciální pozornost je věnována schopnosti vytvořeného modelu pokrýt mismatch a vliv variace procesních parametrů na charakteristiky součástky. Model statistické variace procesu je vytvořen na základě měření asi 30000 součástek a mismatch model je založen na měření asi 3000 součástek.

Výsledky modelování jsou porovnány s měřenými daty a maximální relativní chyba modelu poměru děliče je menší než 1.1 % a typická aplikace je také demonstrována.

Klíčová slova: Vysokonapěťový start-up MOSFET, prahové napětí, vysokonapěťový spirálový dělič, svodový proud, MOS LDMOS, modelování, charakterizace, extrakce parametrů, statistické modelování

Překlad titulu: Modelování spirálového polykřemíkového děliče ve vysokonapěťovém MOSFET tranzistoru a svodového proudu

Contents

List of Tables

List of Figures

List of Figures cont.

Chapter 1
Introduction

Nowadays, the power consumption is one of the most important integrated circuit parameters. Almost all semiconductor devices manufacturers make an effort to design products with the lowest power consumption as reasonably achievable.

As an example, how important the power consumption is, are the following independent statistics and analysis from U.S. Energy Information Administration and analysis from ON Semiconductor company[1]. Every year more than 160 billion kWh are consumed in residential homes in the United States. 3–4 % of electricity consumed in the United States each year is lost inside inefficient power supplies of products like

- desktop computers,
- notebook computers,
- televisions,
- game consoles,
- DVD players, etc.

Employing energy efficient solutions can increase the efficiency of home electronic products by 20 %, which means reducing the energy consumption by more than 32 billion kWh per year, reducing Carbon (CO_2) emissions by 43.5 billion pounds, eliminating 1 million kilotons of CO_2 emissions over 10 years, and eliminating 100 new coal fired power plants.

Increasing the efficiency of these products by 20 % could mean more than $3.2 billion in energy savings per years in the United States alone. Or enough power to supply Alaska, Delaware, Hawaii, Idaho, and Maine combined. It is interesting to imagine the impact globally. Increasing of the world electricity consumption is expected as is shown in Fig 1.1. Considering this facts, minimizing the power consumption becomes inevitable.

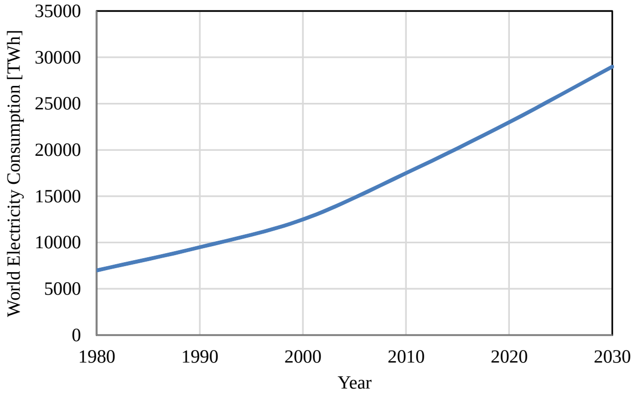

Figure 1.1. World electricity consumption

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[1] Adopted from Rory Gonzalez, *ON Semiconductor*, available at `https://www.youtube.com/watch?v=3NUSMlilQdw`. © Semiconductor Components Industries, LLC, 2011. See App. D.

1.1 Current Situation of the Studied Problem (State-of-the-Art)

The power consumption can be divided into the two main categories [1]:

- **Active (dynamic) power**: arises from the repeated capacitance charge and discharge through parasitics on the output of the gates.
- **Static power**: caused by currents that leaks through transistors even when they are turned off.

There are five main leakage current sources (causing static power consumption) in a CMOS circuits [2]:

- **Subthreshold leakage** in the channel of an OFF transistor between the source and drain terminals.
- **Source/drain junction leakage** (reverse-biased).
- **Gate leakage** (tunneling current through the gate oxide insulation).
- **Gate induced drain leakage** GIDL (due to the high electric field effect in the drain junction, can be minimized by the doping profile in the drain).
- **Punchthrough** (occurs in short channel devices, can be controlled by using implants at the bottom or the edges of the source and drain junction boundaries).

Exponential increases projected for the two principal components of static power consumption: subthreshold leakage and gate leakage shows Fig. 1.2.

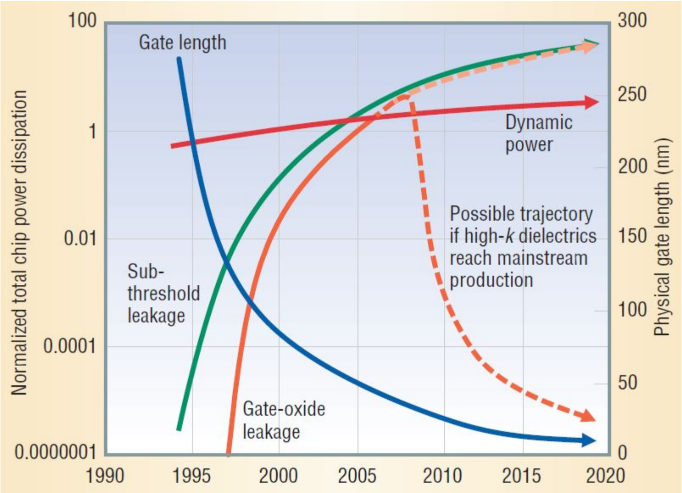


Figure 1.2. Total chip dynamic and static power dissipation trends based on the International Technology Roadmap for Semiconductors. The two power plots for static power represent the 2002 ITRS projections normalized to those for 2001. The dynamic power increase assumes a doubling of on-chip devices every two years. Reprinted from "Leakage Current: Moore's Law Meets Static Power," by N. S. Kim, et al., 2003, *Computer, 36(12)*, p. 69. © 2003 by the IEEE. Reprinted with permission, see App. D.

Reducing the supply voltage decreases the power consumption but also reduces the circuit's maximum operating frequency.

Here are other more sophisticated techniques for minimizing the power consumption[3].

- **Active (dynamic) power**: The following techniques are used to minimize active power consumption :
  - **Clock gating**.
  - **Voltage islands** (Lower operating voltages reduces active power in a quadratic way. Using voltage islands in areas of a chip where performance and speed of that functional unit is non-critical saves the power).
  - **Dynamic voltage and frequency scaling** (DVFS) (The active operating voltage and frequency are changed based on demand of the load. High load = nominal voltage and frequency, low load = the voltage or the frequency is scaled down to perform at a lower speed but provides the benefit of low active power consumption).
  - **On-die voltage regulators** (On-die voltage regulators are specifically designed to meet the demands of various active and static power requirements).
  - **3D-IC** (Stacking ICs that communicate with one another to minimize the signal interconnect, e.g. using Through Silicon Vias TSV).
- **Static power**: The following techniques are used to minimize static power consumption:
  - **Power-gating** (Provides the leakage power savings for a device in standby).
  - **Multi-threshold voltage transistor usage** [4](Swapping of nominal threshold voltage gates with higher threshold voltage gates. The sub-threshold leakage is inversely proportional to the threshold voltage in CMOS).
  - **Active back-bias** (Increasing the bias voltage of the substrate nodes in CMOS reduces the leakage current but essentially increases the threshold voltage).

Other interesting techniques for minimizing the power consumption are summarized in the following text.

A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems is described in [5].

An Energy-Saving Rate-Harmonized Scheduler guarantees that every idle duration can be used to switch into sleep mode [6]. Energy-Saving Rate-Harmonized Scheduling saves 16.8 % energy compared to conventional Rate-Monotonic Scheduling.

An intelligent energy optimization approach for MPI based applications in HPC systems is described in [7].

The paper [8] focuses on cache leakage reduction and proposes the first Timing-Aware Cache Leakage Control (TACLC) mechanism. TACLC exploits system slack to turn cache lines into low-leakage states provided that the timing constraint is met. The experimental results demonstrate that TACLC effectively utilizes system slack to reduce cache leakage.

Scheduling and interconnection design to minimize the interconnection's energy consumption without performance degradation is described in [9].

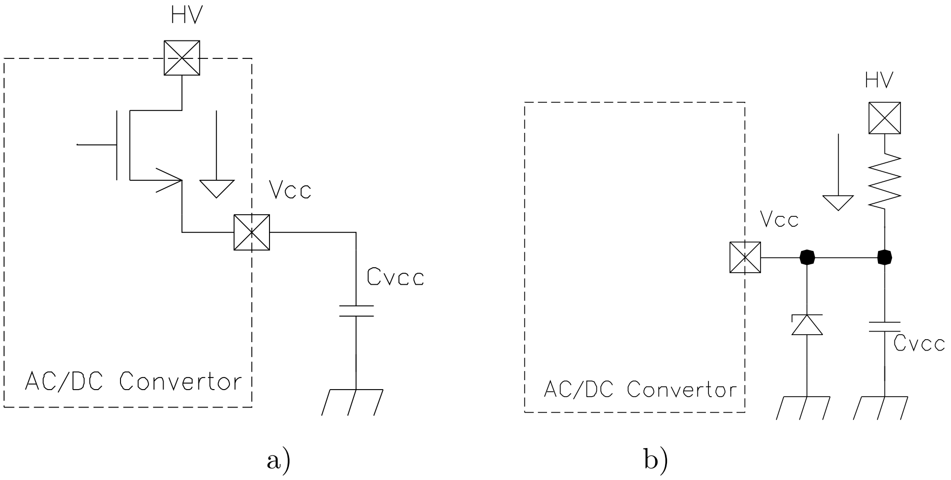
In the paper [10], a novel technique for optimizing electronic circuits by resizing transistor parameters using single perceptron neural network is proposed.

Off-state leakage current is one of two principal sources of power dissipation in today's microprocessors. Intel chairman Andrew Grove cited off-state current leakage in particular as a limiting factor in future microprocessor integration [11] in comments on power consumption problem at the 2002 International Electron Devices Meeting.

It is crucial to know the circuit's estimated leakage power since such a bound will enable the designers to ensure that the circuit meets the standby power constraints which impacts battery life in portable devices [2]. It means that the leakage of MOSFET devices have to be modeled accurately.

The leakage current in standard MOSFET models (BSIM3/BSIM4) is typically modeled by drain-bulk and source-bulk diodes. This modeling method does not consider the impact of several parasitic bipolar devices. For the accurate modeling the impact of the following bipolar transistors has to be considered: a lateral bipolar transistor drain-bulk-source, a vertical bipolar transistor drain-bulk-substrate (only in isolated structures), and a vertical bipolar transistor source-bulk-substrate (only in isolated structures). For example, the drain or source leakage as a function of gate length cannot be modeled without the scalable parasitic bipolar devices. The first part of this thesis deals with accurate gate dimension dependent drain and source leakage modeling.

Another possibility of minimizing the power consumptions provides the circuits with sophisticated integrated features that dynamically adapts the power consumption to actual loads or power supply. Such a circuit includes the control circuit that is sensing the input/output voltage in order to dynamically adapts the power consumption. In case of AC/DC convertor the input voltage can be up to 400 V. For sensing this high input voltage a HV divider is commonly used. If the external HV divider is connected to the convertor then resistor is a source of a power consumption (see Fig 1.3b). If the convertor uses integrated HV sensing divider (see Fig 1.3a) then charging of the external capacitor C_{VCC} can be controlled by the circuit based on HV supply and can be switched off. The second part of this thesis deals with accurate modeling of this integrated high voltage divider.



a) b)

Figure 1.3. Comparison of the a) circuit with integrated HV sensing divider and b) circuit with external HV sensing divider

In the third part of this thesis a special attention is paid to the ability of the created model to cover the mismatch and influence of a variation of process parameters on the device characteristics.

1.2 Aims of the Thesis

The thesis is organized as follows:

- **Chapter 1** gives a brief overview of the current situation of the studied problems, literature overview and aims of the thesis.
- **Chapter 2** deals with the accurate gate dimension dependent drain and source leakage modeling and demonstrates the structure of a proposed macro models, implemented scalability (in most cases nonlinear), developed scaling equations, and physical explanation of this scaling. Finally, the comparison of measured data vs. simulation is presented in order to confirm the model validity. This model improvement solves not only leakage current scaling, but it also accounts for additional parasitic bipolar effects, such as current injection to the substrate.
- **Chapter 3** describes the structure and applications of the high voltage MOSFET with integrated nonlinear spiral high voltage polysilicon divider.
- **Chapter 4** deals with the proposed and implemented DC and AC model of the nonlinear spiral high voltage polysilicon divider.
- **Chapter 5** describes proposed and implemented high voltage divider statistical modeling.
- **Chapter 6** contains conclusions and final remarks.

The thesis aims can be summarized as follows

- Designing the characterization test chip containing required devices with sufficient number of various dimensions.
- Extracting the parasitic bipolar transistors for various MOSFET and LDMOS gate dimensions.
- Proposing new models of the MOSFET and LDMOS drain and source leakage that are dependent on the gate dimensions and implementing them into the commercial simulators.
- Extracting, developing and implementing new model of the nonlinear high voltage spiral polysilicon divider in HV start-up MOSFET.
- Evaluating statistical data and making new HV divider model responsive to the statistical process variation.
- Comparing new developed models with measured data and identifying changes of the simulation times.

`The fundamental results (new scientific findings) of this thesis are described in Chapters 2, 4 and 5.`

This thesis was prepared based on the plainTEX template – officially recommended design style CTUstyle for doctoral (Ph.D.) theses at the Czech Technical University in Prague.

1.3 Used Modeling Methodology

The following list of steps describes model development flow used for this thesis:

- **1. Characterization test chip design** - At first characterization test chip was designed in software Cadence Virtuoso Layout. For leakage modeling a lot of MOSFET and LDMOS devices were placed on this test chip in different dimensions and configurations. Test chip contains all structures necessary for characterization of the process and making predictive SPICE models. Therefore it's typically very large chip – full reticle. HV MOSFET was placed into several layout structures allowing various type of measurement (eg. DC, AC, mismatch, etc.).

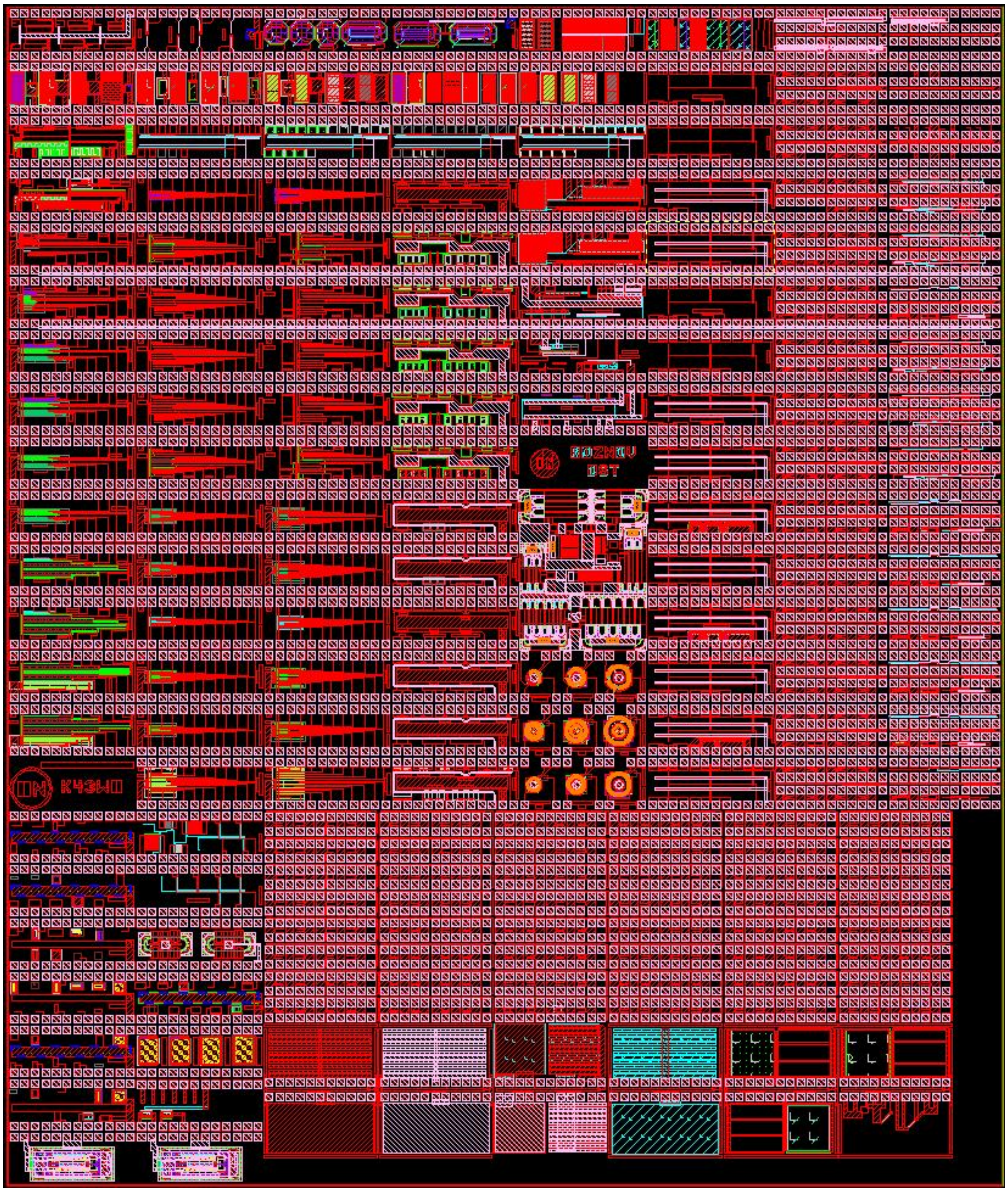


Figure 1.4. Characterization test chip.

- **2. Process control monitoring (PCM) test chip design** - PCM test chip was designed in software Cadence Virtuoso Layout and added into all following production masks (each fabricated standard production wafer then contains PCM test chip with required devices for statistical modeling). PCM has defined testplan measured in each wafer before testing production device. Measurement must pass the defined criteria. PCM is used for monitoring distribution of main process parameters and generation of corner models and statistical models.

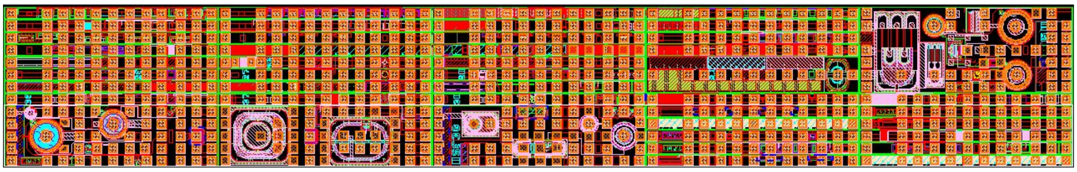


Figure 1.5. Process control monitoring test chip.

- **3. Test chip manufacturing** - Test chips were manufactured in analog 1 μm CMOS technology and wafers best matching process means were selected for measurement. Also three experimental process split lots were fabricated (high resistance implant dose 85 %, 100 % and 115 %) for extraction of temperature coefficients dependency on polysilicon sheet resistance.
- **4. Measurement methods definition** - The measurement methods had to be selected, set, adjusted and tested, especially AC methods (it was experimented with external loads, finally the load $C_{\text{load}} = 330$ nF was selected).
- **5. Measurements for the leakage modeling**:
  - S-parameters measurements for resistances and some other BJTs' parameters extraction.

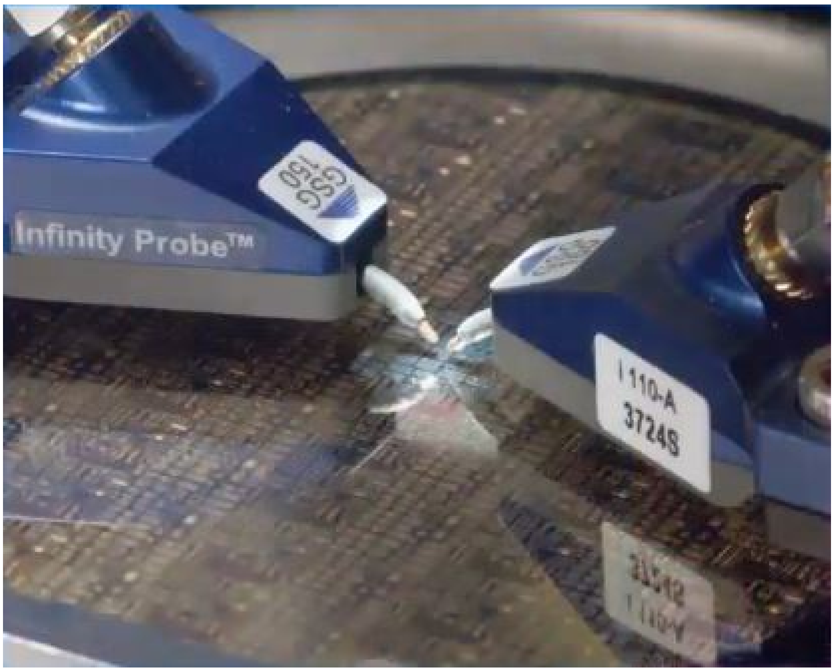


Figure 1.6. On-wafer S-parameters measurement. 1)

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1) Retrieved from video 15 February, 2015, from IC-CAP Device Modeling Software - Measurement Control and Parameter Extraction, Keysight Technologies, Visible `http://www.keysight.com/en/pc-1297149/ic-cap-device-modeling-software-measurement-control-and-parameter-extraction`

  - DC measurements at various temperatures −40, −20, 0, 27, 60, 90, 125, and 150 °C (I_DV_G and I_DV_D, parasitic BJTs measurement: forward and reverse Gummel characteristics I_CV_{BE}, I_BV_{BE}, and I_EV_{BC}, I_BV_{BC}, forward and reverse output characteristics I_CV_{CE} and I_EV_{EC}, resistances R_E, R_B, R_C measurements).
  - CV measurements (C_{BE}, C_{BC}).

- **6. Measurements for the HV divider modeling**:
  - Ratio DC measurement (for various V_S at temperatures −40, −20, 0, 27, 60, 90, 125, and 150 °C).
  - Ratio AC measurement (for various V_D)
  - High resistance implant dose process split temperature coefficients measurement (for temperatures −40, −20, 0, 27, 60, 90, 125, and 150 °C).
- **7. Export/import data** - Measured data were exported from measurement database DAM (ON Semiconductor internal measurement and data management system, thesis author is employee) in .mdm file format and then imported into IC-CAP (Integrated Circuit Characterization and Analysis Program, Keysight Technologies)
- **8. Measurement data quality verification** - The quality of measured data was verified (e.g. comparing same bias points from different measurement methods, verifying measured data trends, physical data scaling, etc.)
- **9. TCAD simulations** - Many TCAD simulations were done in Synopsys Sentaurus Workbench (simulations of leakages for various device dimensions at various temperatures, simulations of electrostatic potential distribution in HV MOSFET for various biases).
- **10. Model development and parameter extraction** - Models were developed in IC-CAP together with parameter extraction. For leakage modeling, the separate models for each device dimension were extracted. Finally, the scaling equations for each model parameter was developed to fit extracted models for all device dimensions. The dependency of temperature coefficients on polysilicon sheet resistance was extracted from the experimental process split lots (the high resistance implant dose 85 %, 100 %, and 115 %).
- **11. Model implementation** - The all new developed models were implemented into the commercial simulators HSPICE (Synopsys), ELDO (Mentor) and SPECTRE (Cadence).
- **12. Simulated and measured data comparison** - All measured data were compared with simulated data and all discrepancies were eliminated by model or equation corrections.
- **13. Model testing** - The all new developed models were verified in their defined operation areas at temperatures from −50 to 200 °C. The important requirement was that the new developed models had smooth derivatives of simulated characteristics.
- **14. Statistical data export** - The big amount of statistical data measured on PCM chip was exported from the factory (almost 30000 measured devices).
- **15. Statistical data evaluation** - Statistical data were evaluated and electrical process variation parameters were calculated.
- **16. Statistical parameters implementation** - The statistical model parameters were implemented in to the new developed models. The mapping equations between model parameters and statistical electrical process parameters were also implemented by using master variables.
- **17. Statistical parameters extraction** - The statistical model parameters were extracted by using Forward or Backward propagation of variances.

- **18. Corner models extraction** - The corner libraries (worst case corner models) were also implemented.
- **19. Monte Carlo verification** - All the new developed models were verified by comparison of Monte Carlo simulations and process variation.
- **20. Final application verification** - The simulation speeds were measured and compared with conventional models and are acceptable. Any convergency issue was not observed during the verification realized on several real designs.

Chapter 2

Gate Dimension Dependent Drain and Source Leakage

In this chapter the first fundamental thesis result is descibed. This chapter deals with the accurate gate dimension dependent drain and source leakage modeling and demonstrates the structure of a proposed macro models, implemented scalability (in most cases nonlinear), developed scaling equations, and physical explanation of this scaling.

2.1 Introduction

The BSIM3v3 or BSIM4 model [12] is very often used for the MOSFET transistors modeling. These models provide very good accuracy and the BSIM4 model is also used in this chapter. The leakage current is modeled by drain-bulk and source-bulk diodes in this model (e.g. by parameters J_{SS}, J_{SD}, J_{SWS}, J_{SWD}, etc.), and the diodes are scaled with the area and perimeter of the drain and source by component parameters a_d, p_d, a_s and p_s). This method is described in detail in [13–15]. The leakage modeling for four-terminal MOSFET was also published in [16].

However, there exist the operation areas where these methods are not sufficient. Especially, the real current redistribution in OFF state is not taken into account, which means that the lateral drain to source injection is not modeled. Moreover, in the case of an isolated MOSFET the injection to the substrate is not also modeled. The correct modeling of above mentioned effects, that is introduced in this chapter, makes the model more precise not only in OFF state (the drain leakage current, the source leakage current), but also in the case of an nonstandard biasing (open drain-bulk or source-bulk junction).

In order to demonstrate these phenomena, an isolated P-channel MOSFET and an N-channel lateral DMOS were selected as a testcases. In the following sections the improved modeling methods are described for these two testcases.

2.2 P-channel MOSFET

2.2.1 Crossection and modeling

An example of more general isolated MOSFET, in this case the P-channel MOSFET, is shown in Fig. 2.1. The source and drain are formed from P^+ layer and the bulk from nwell. This configuration forms two parasitic vertical substrate transistors and one parasitic lateral transistor. An emitter of the first substrate transistor is formed from the drain, a base from the bulk, and a collector from the substrate. The same applies for the second substrate transistor, however an emitter is formed from the source. The parasitic lateral transistor occurs between source and drain where the source is an emitter, the bulk is a base and the source is a collector.

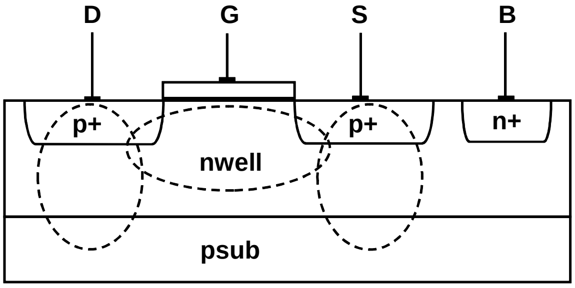


Figure 2.1. Crossection of P-channel MOSFET with indication of parasitic BJTs

These three parasitic bipolar transistors are scaled with the gate length and width and have significant impact on the leakage characteristics. If the standard BSIM4 model with the parasitic diodes is used for the modeling of this P-channel MOSFET, the leakage modeling is not accurate. This standard model does not consider the impact of the parasitics bipolar transistors, e.g. an injection to the substrate or lateral channel injection. The possible solution by using the SPICE models [17] is shown in Fig. 2.2 where all three parasitic bipolar devices are added without the necessity of adding the new circuit nodes. In this case the source-bulk and the drain-bulk parasitic diode parameters of the BSIM4 model have to be suppressed. The dependency of the model parameters of the parasitic bipolar transistors on the gate length and gate width are described in next two sections. The standard Gummel-Poon model [18] is used for modeling of these BJTs.

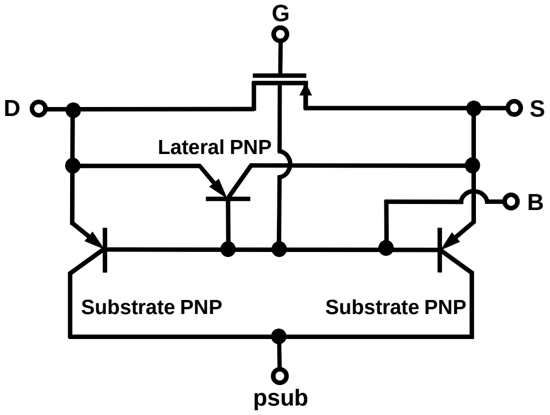


Figure 2.2. Updated MOSFET model with parasitic BJTs

The component parameters are given by

$$\begin{aligned} a_d &= W_{\mathrm{G}} L_{\mathrm{D}} \\ a_s &= W_{\mathrm{G}} L_{\mathrm{S}} \\ p_d &= 2(W_{\mathrm{G}} + L_{\mathrm{D}}) \\ p_s &= 2(W_{\mathrm{G}} + L_{\mathrm{S}}) \end{aligned} \tag{1}$$

where W_{G} is the gate width of MOSFET, a_d and p_d are an area and a perimeter of the drain, a_s and p_s are an area and a perimeter of the source, and L_{D} and L_{S} are the lengths of the drain and source.

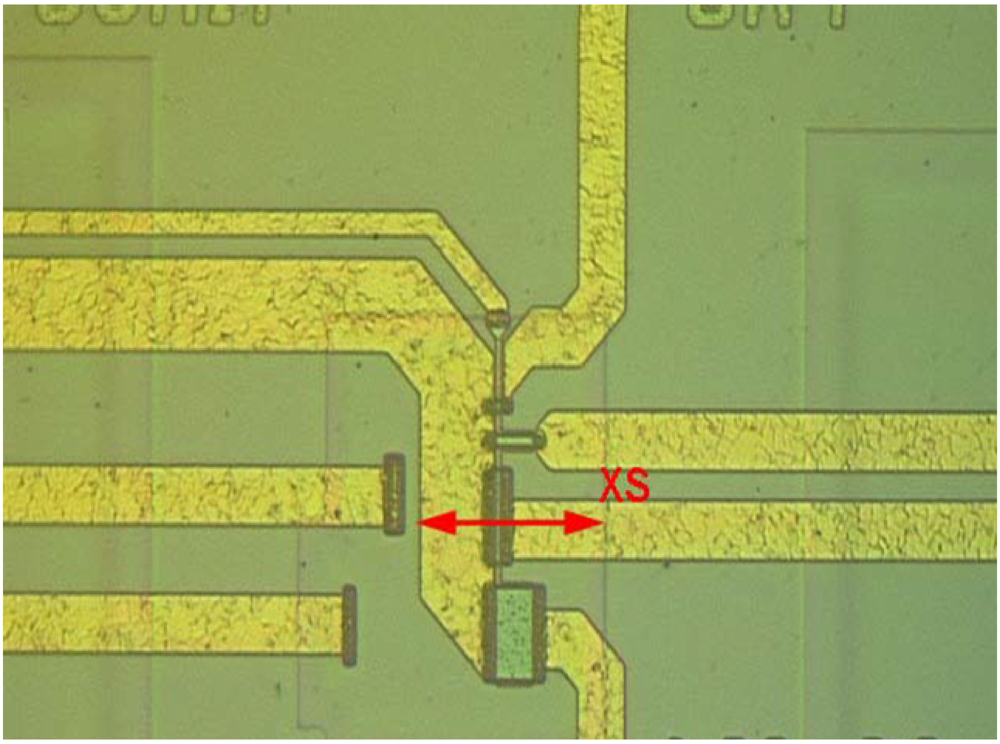


Figure 2.3. Photo of the chip for construction analysis (the red arrows indicates the cat).

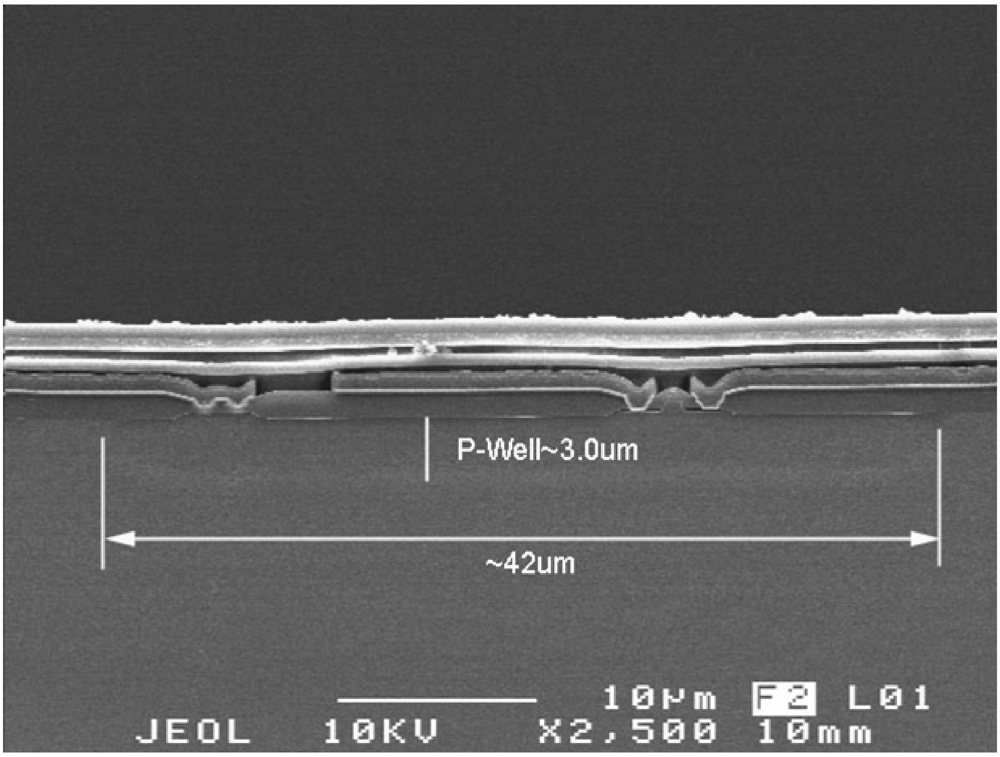


Figure 2.4. Photo from the MOSFET construction analysis - bulk (pwell). The whole MOSFET structure is shown.

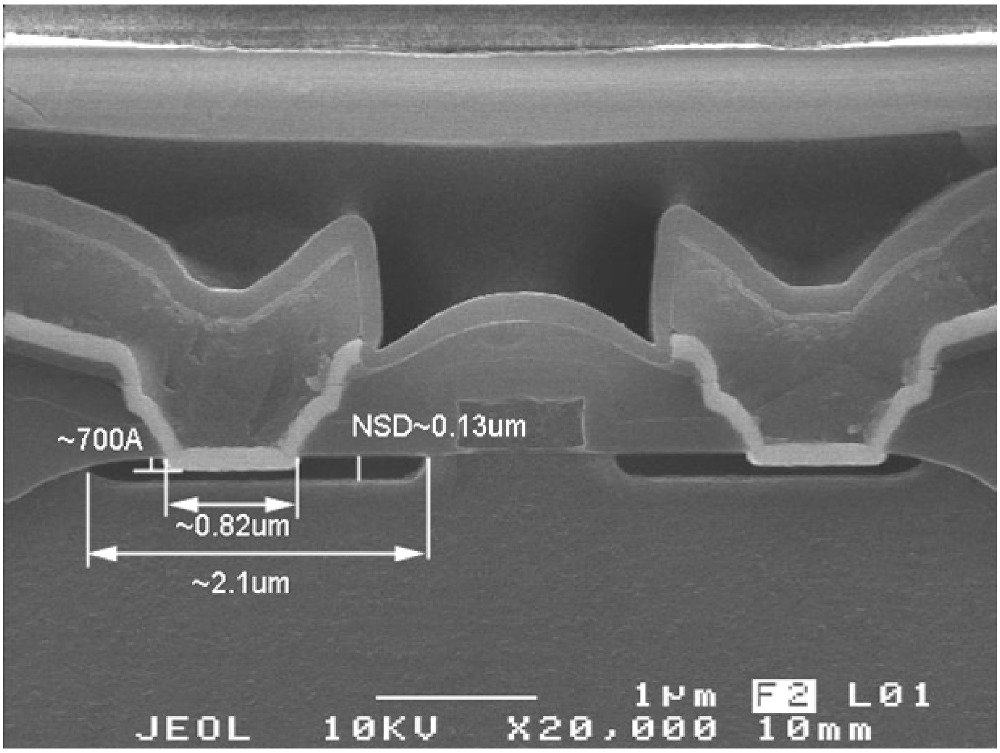


Figure 2.5. Photo of the MOSFET construction analysis - drain, source and gate are shown in detail.

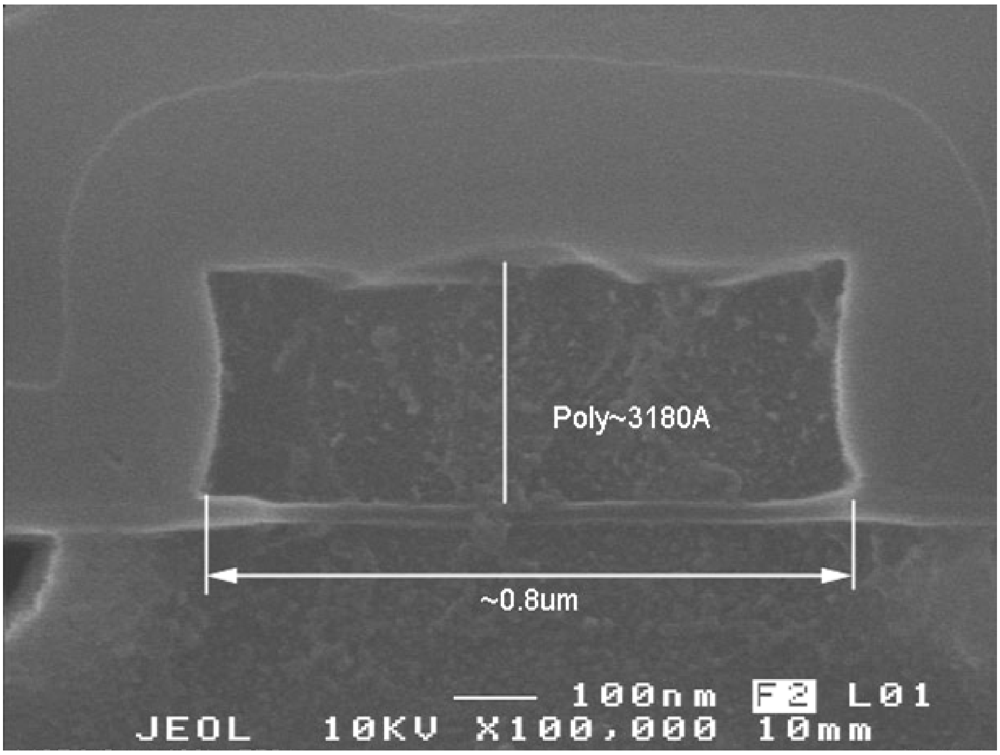


Figure 2.6. Photo of the MOSFET construction analysis - gate is shown in more detail.

2.2.2 Substrate vertical parasitic BJTs

The model parameters of the substrate vertical parasitic BJTs reflect the dependency on gate dimensions and also the impact of the current redistribution between vertical and lateral parasitic BJTs. The values of the model parameters are replaced by equations with scaling parameters.

The model parameter I_S (transport saturation current) is defined as

$$I_S = \left(j_{sa} \ln \frac{L_\mathrm{G}}{L_0} + j_{sb} \right) a_d + j_{sp} p_d + j_{sc} \tag{2}$$

where j_{sa}, j_{sb}, j_{sp}, and j_{sc} are the extracted scaling parameters and $L_0 = 1$ µm is the reference gate length. This equation implies that the parameter I_S is linearly dependent on gate width W_G which is shown in Fig. 2.7.

The logarithmic dependency of the parameter I_S on the gate length L_G that also comes from (2) is shown in Fig. 2.8. This gate length dependency controls the current redistribution between the substrate vertical and the lateral BJT. The lateral injection from the drain to the source is more significant than the injection to the substrate for the short gate lengths. Therefore, the parameter I_S of the vertical BJT is logarithmically decreased for the short gate lengths. The dependency of I_S on $W_\mathrm{G}/L_\mathrm{G}$ is shown in Fig. 2.9.

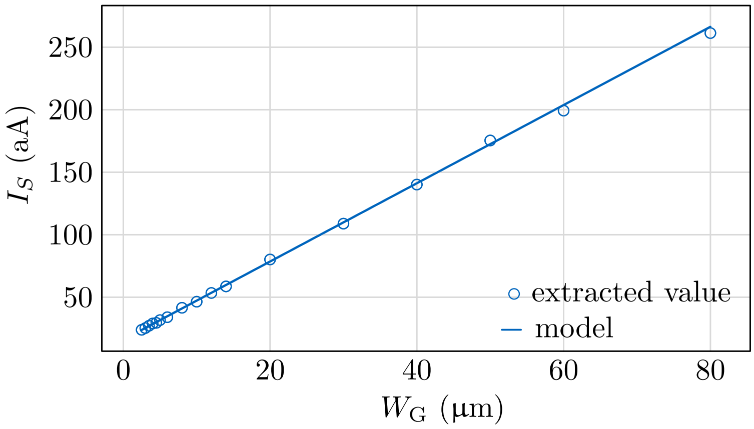


Figure 2.7. Vertical parasitic BJT: I_S vs W_G.

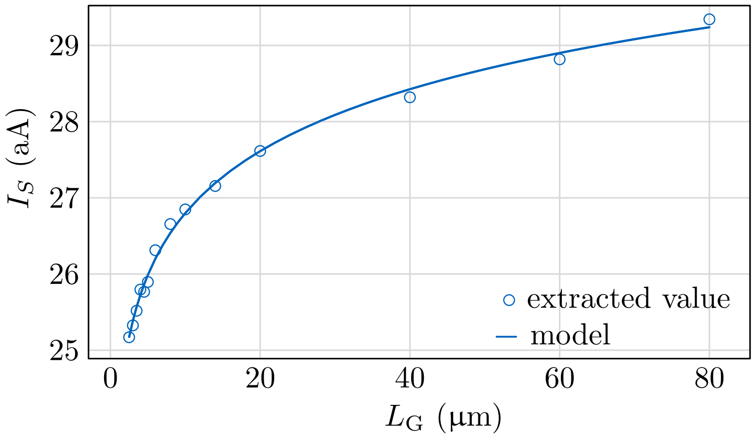


Figure 2.8. Vertical parasitic BJT: I_S vs L_G.

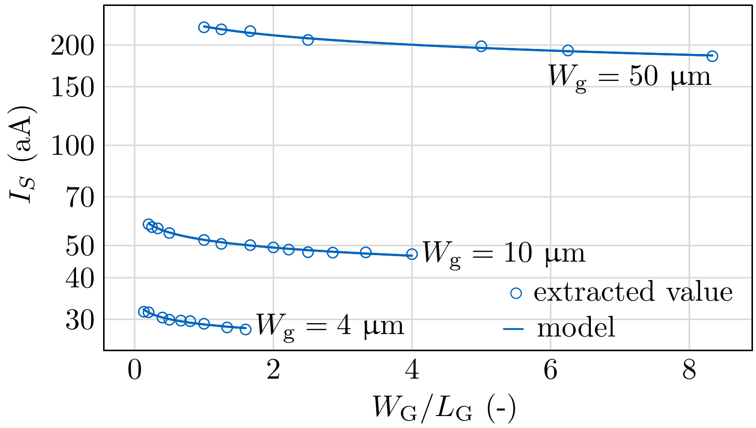


Figure 2.9. Vertical parasitic BJT: I_S vs $W_{\mathrm{G}}/L_{\mathrm{G}}$.

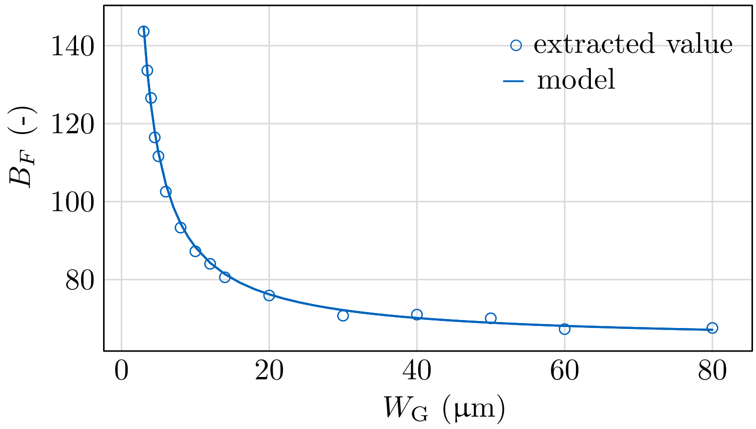


Figure 2.10. Vertical parasitic BJT: B_F vs W_{G}.

The model parameter B_F (ideal forward maximum beta) is not dependent on the gate length L_{G} and is a constant for a whole range of L_{G}. On the other hand there exists a strong nonlinear dependency of the parameter B_F on the gate width W_{G} (gate width is included in the component parameters a_d and p_d). This dependency is shown in Fig. 2.10 and is expressed as

$$B_F = \frac{j_{sat}a_d + j_{sp}p_d + j_{sc}}{j_{ba}a_d + j_{bp}p_d + j_{bc}} \tag{3}$$

where j_{sat} is a scaling saturation current parameter, j_{ba}, j_{bp}, and j_{bc} are the extracted scaling parameters. The saturation current parameter j_{sat} in the B_F numerator in (3) assures the correlation between parameters B_F and I_S [19]: $B_F \sim I_S/(I_{\mathrm{B}}@V_{\mathrm{BE}} = 0\ \mathrm{V})$.

The model parameter I_{KF} (forward beta high current roll-off) is independent on the gate length L_{G} and linearly dependent on the gate width W_{G}

$$I_{KF} = j_{ka}a_d + j_{kp}p_d + j_{kc} \tag{4}$$

where j_{ka}, j_{kp}, and j_{kc} are the extracted scaling parameters.

The model parameters R_E (emitter resistance), R_C (collector resistance) and R_B (base resistance) are inversely proportional to the gate width W_{G} and are not dependent on the gate length L_{G}

$$R_E = \frac{1}{g_{ea}a_d + g_{ep}p_d + g_{ec}} \tag{5}$$

$$R_C = \frac{1}{g_{ca}a_d + g_{cp}p_d + g_{cc}} \tag{6}$$

$$R_B = \frac{1}{g_{ba}a_d + g_{bp}p_d + g_{bc}} \tag{7}$$

where g_{ea}, g_{ep}, g_{ec}, g_{ca}, g_{cp}, g_{cc}, g_{ba}, g_{bp}, and g_{bc} are the extracted scaling parameters.

The parasitic capacitance is modeled by the vertical BJTs. Therefore, the capacitance parameters of the lateral BJT (C_{JE}, C_{JC}) and source/drain junction diode parameters of MOSFET [12] (C_{JS}, C_{JD}, C_{JSWS}, C_{JSWD}, C_{JSWGS}, C_{JSWGD}, J_{SS}, J_{SD}, J_{SWS}, J_{SWD}, J_{SWGS}, J_{SWGD}) are suppressed (set to zero or very low value, e.g. 10^{-30}). The dependency of the model parameters C_{JE} and C_{JC} of the vertical BJTs on the gate width is linear

$$C_{JE} = c_{jea}a_d + c_{jep}p_d + c_{jec} \tag{8}$$

$$C_{JC} = c_{jca}a_b + c_{jcp}p_b + c_{jcc} \tag{9}$$

where c_{jea}, c_{jep}, c_{jec}, c_{jca}, c_{jcp}, and c_{jcc} are the extracted scaling parameters and a_b, p_b is the area and perimeter of the bulk.

The Early voltage effect was not observed due to the deep nwell that means the big base width, so the model parameter VAF was set to the large number.

Scaling parameter	Unit	Value
j_{sa}	Am^{-2}	3×10^{-19}
j_{sb}	Am^{-2}	9×10^{-19}
j_{sp}	Am^{-1}	1.2×10^{-19}
j_{sc}	A	1.6×10^{-17}
j_{sat}	Am^{-2}	2.1×10^{-18}
j_{ba}	Am^{-2}	2.2×10^{-20}
j_{bp}	Am^{-1}	5.2×10^{-22}
j_{bc}	A	4×10^{-21}
j_{ka}	Am^{-2}	1×10^{-6}
j_{kp}	Am^{-1}	2.9×10^{-7}
j_{kc}	A	5×10^{-5}
g_{ea}	$\Omega^{-1}\mathrm{m}^{-2}$	2×10^{-4}
g_{ep}	$\Omega^{-1}\mathrm{m}^{-1}$	5×10^{-5}
g_{ec}	Ω^{-1}	1×10^{-2}
g_{ca}	$\Omega^{-1}\mathrm{m}^{-2}$	2×10^{-1}
g_{cp}	$\Omega^{-1}\mathrm{m}^{-1}$	8×10^{-3}
g_{cc}	Ω^{-1}	5×10^{-2}
g_{ba}	$\Omega^{-1}\mathrm{m}^{-2}$	1×10^{-4}
g_{bp}	$\Omega^{-1}\mathrm{m}^{-1}$	3.7×10^{-6}
g_{bc}	Ω^{-1}	2.1×10^{-5}
c_{jea}	Fm^{-2}	2.45×10^{-16}
c_{jep}	Fm^{-1}	3.09×10^{-16}
c_{jec}	F	2.9×10^{-16}
c_{jca}	Fm^{-2}	2.95×10^{-17}
c_{jcp}	Fm^{-1}	6.02×10^{-16}
c_{jcc}	F	2.1×10^{-17}

Table 2.1. Extracted parameters of the parasitic vertical BJTs

Both parasitic vertical BJTs were measured and also their parameters were extracted based on the standard methodology described in [18]. Extracted parameters (computed by the Levenberg-Marquardt algorithm [20]) are summarized in Tab. 2.1.

2.2.3 Lateral parasitic BJT

The model parameters of the lateral parasitic BJT reflect the dependency on gate dimensions and also the impact of the current redistribution between vertical and lateral parasitic BJTs. The values of the model parameters are replaced by equations with scaling parameters.

The model parameter I_S (transport saturation current) is defined as

$$I_S = \frac{i_{slw} W_{\mathrm{G}}}{(L_{\mathrm{G}}/L_0)^{\left(\alpha_{sla} + \frac{L_{\mathrm{G}}}{W_{\mathrm{G}}} \alpha_{slb}\right)}} + i_{slc} \tag{10}$$

where i_{slw}, α_{sla}, α_{slb}, and i_{slc} are the extracted scaling parameters. The parameter i_{slw} expresses the almost linear dependency of the transport saturation current I_S on the gate width W_{G} that is shown in Fig. 2.11. Increasing the gate width W_{G} of MOSFET causes the increasing of the effective emitter size of the lateral BJT and this leads to increasing of the saturation current I_S.

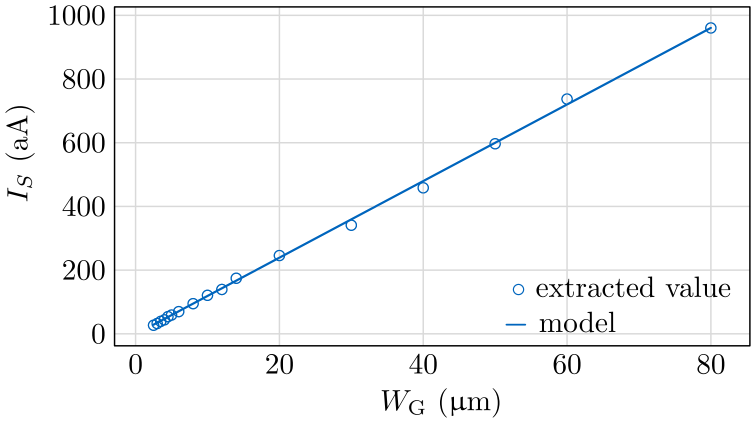


Figure 2.11. Lateral parasitic BJT: I_S vs W_{G}.

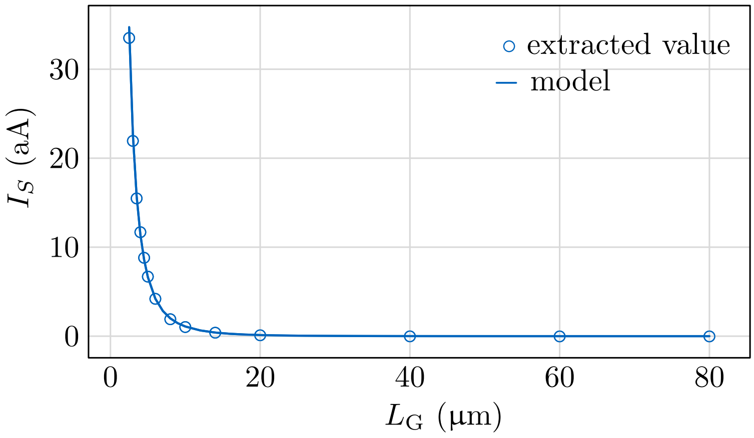


Figure 2.12. Lateral parasitic BJT: I_S vs L_{G}

The strong nonlinear dependency on the gate length L_G is depicted in Fig. 2.12 and is determined by the parameters α_{sla} and α_{slb}. Increasing the gate length L_G of MOSFET means increasing the distance between emitter and collector (base width) that causes decreasing of the saturation current I_S. The dependency of I_S on $W_\mathrm{G}/L_\mathrm{G}$ is shown in Fig. 2.13.

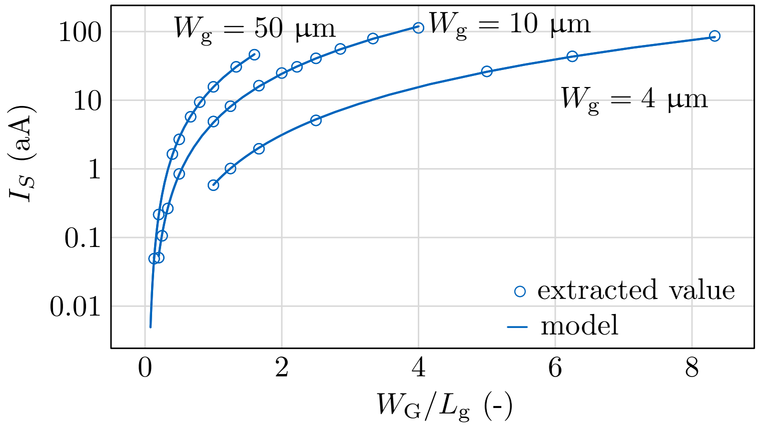


Figure 2.13. Lateral parasitic BJT: I_S vs $W_\mathrm{G}/L_\mathrm{G}$.

The dependency of the current redistribution between vertical and lateral parasitic BJTs on the gate length is demonstrated in TCAD simulation graphs for two selected gate lengths. The hole current density of MOSFET with the gate length 2.5 µm is depicted in Fig. 2.14 that shows the leakage current flowing from the drain to the source (lateral BJT) and also to the substrate (vertical BJT). However, MOSFET with the gate length 10.5 µm, depicted in Fig. 2.15, shows the leakage current flowing predominantly to the substrate. The current density in Figs. 2.14 and 2.15 is modeled at nominal temperature 300.15 K, and is exponentially temperature dependent as is demonstrated in Figs. 2.17 and 2.18. The difference between the current densities at 300.15 K and 423.15 K is about six orders, so the leakage at the higher temperatures, where devices often operate, becomes significant for practical designs and should not be neglected.

The model parameter I_{KF} is independent on the gate length L_G and is linearly dependent on the gate width W_G

$$I_{KF} = j_{klp} W_\mathrm{G} + j_{klc} \tag{11}$$

where j_{klp} and j_{klc} are the extracted scaling parameters.

The model parameters R_E, R_C, and R_B are inversely proportional to the gate width W_G and are not dependent on the gate length L_G

$$R_E = \frac{1}{g_{elp} W_\mathrm{G} + g_{elc}} \tag{12}$$

$$R_C = \frac{1}{g_{clp} W_\mathrm{G} + g_{clc}} \tag{13}$$

$$R_B = \frac{1}{g_{blp} W_\mathrm{G} + g_{blc}} \tag{14}$$

where g_{elp}, g_{elc}, g_{clp}, g_{clc}, g_{blp}, and g_{blc} are the extracted scaling parameters.

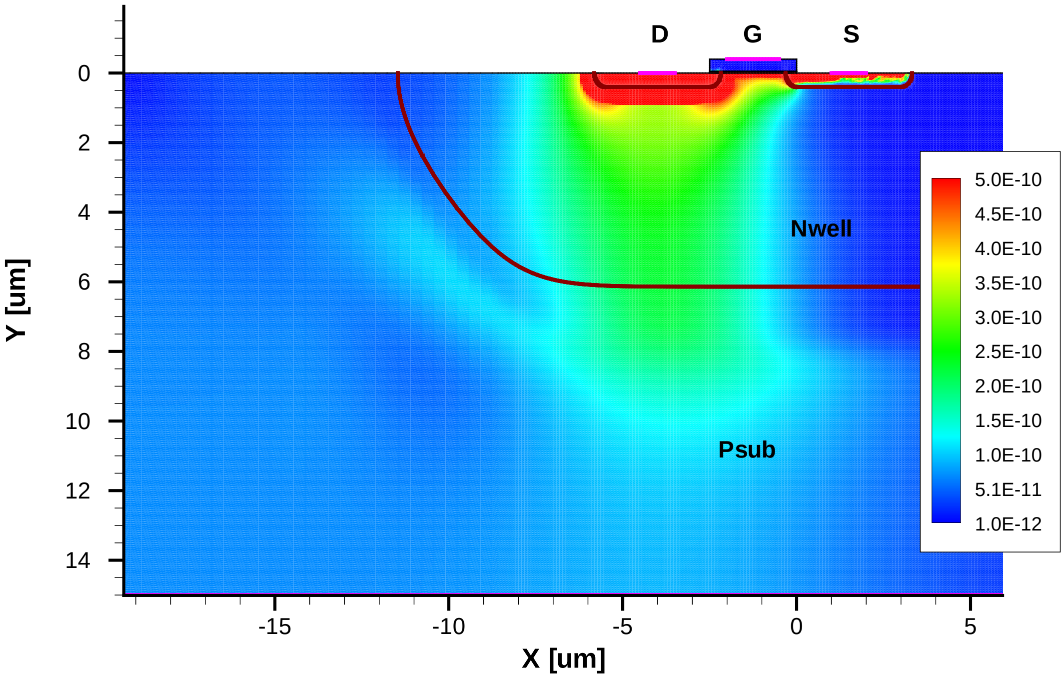


Figure 2.14. TCAD simulation of the leakage current redistribution in MOSFET with $L_G = 2.5$ µm at nominal temperature 300.15 K. Graph represents the hole current density in $\mathrm{Am^{-2}}$.

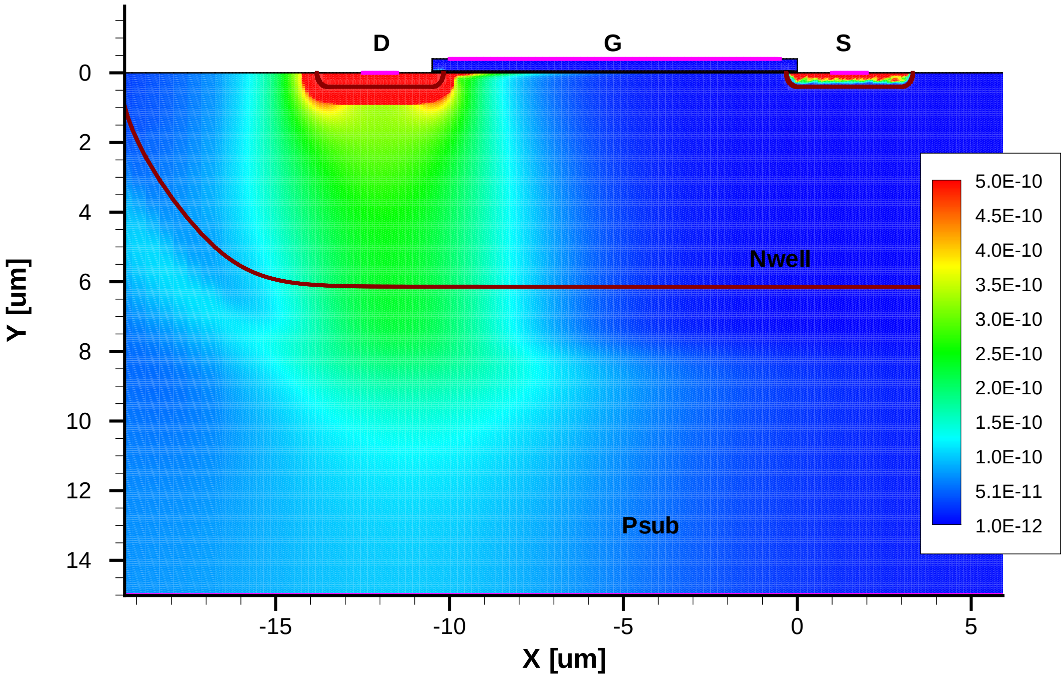


Figure 2.15. TCAD simulation of the leakage current redistribution in MOSFET with $L_G = 10.5$ µm at nominal temperature 300.15 K. Graph represents the hole current density in $\mathrm{Am^{-2}}$.

The Early voltage dependency on the gate length L_{G}, that is actually the base width of parasitic lateral transistor, was negligible in comparison with very high dependency of saturation current I_S on the gate length. This is the reason why the Early voltage parameter was fixed to the constant value $V_{AF} = 50$ V.

The model parameter B_F (ideal forward maximum beta) is dependent neither on the gate length L_{G} nor the gate width W_{G} and is a constant for a whole range of L_{G} and W_{G} (see Fig. 2.16).

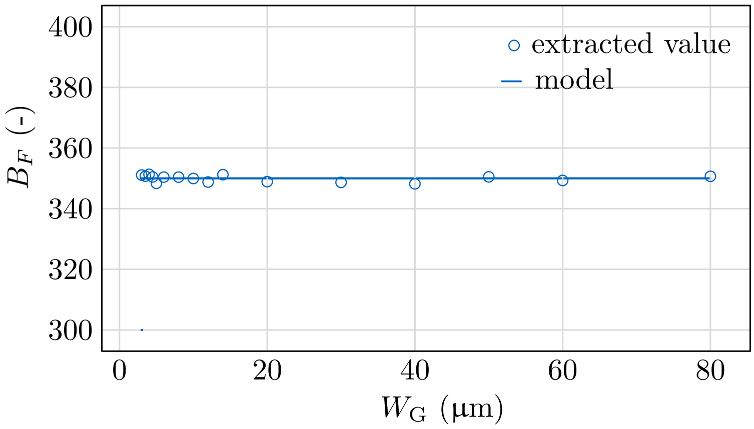


Figure 2.16. Lateral parasitic BJT: B_F vs W_{G}.

The parasitic lateral BJT was measured and also its parameters were extracted based on standard methodology described in [18]. Extracted parameters are summarised in Tab. 2.2.

Scaling parameter	Unit	Value
i_{slw}	Am^{-1}	9.54×10^{-17}
α_{sla}	–	2.25
α_{slb}	–	0.127
i_{slc}	A	3×10^{-23}
j_{klp}	Am^{-1}	5×10^{-7}
j_{klc}	A	7.5×10^{-8}
g_{elp}	$\Omega^{-1}\mathrm{m}^{-1}$	1×10^{-4}
g_{elc}	Ω^{-1}	1.5×10^{-5}
g_{clp}	$\Omega^{-1}\mathrm{m}^{-1}$	1×10^{-4}
g_{clc}	Ω^{-1}	1.5×10^{-5}
g_{blp}	$\Omega^{-1}\mathrm{m}^{-1}$	1×10^{-4}
g_{blc}	Ω^{-1}	1.5×10^{-5}

Table 2.2. Extracted parameters of the parasitic lateral BJT

The comparison of the $I_{\mathrm{D}}V_{\mathrm{G}}$ characteristics between the standard BSIM4 model and MOSFET with parasitic BJTs is shown in Fig. 2.17 and 2.18. The leakage current in the standard BSIM4 model flows from the drain only to the bulk. To the contrary the model with parasitic BJTs takes into account injection from the drain to the substrate and also to the source (see source current in Fig. 2.17 and 2.18).

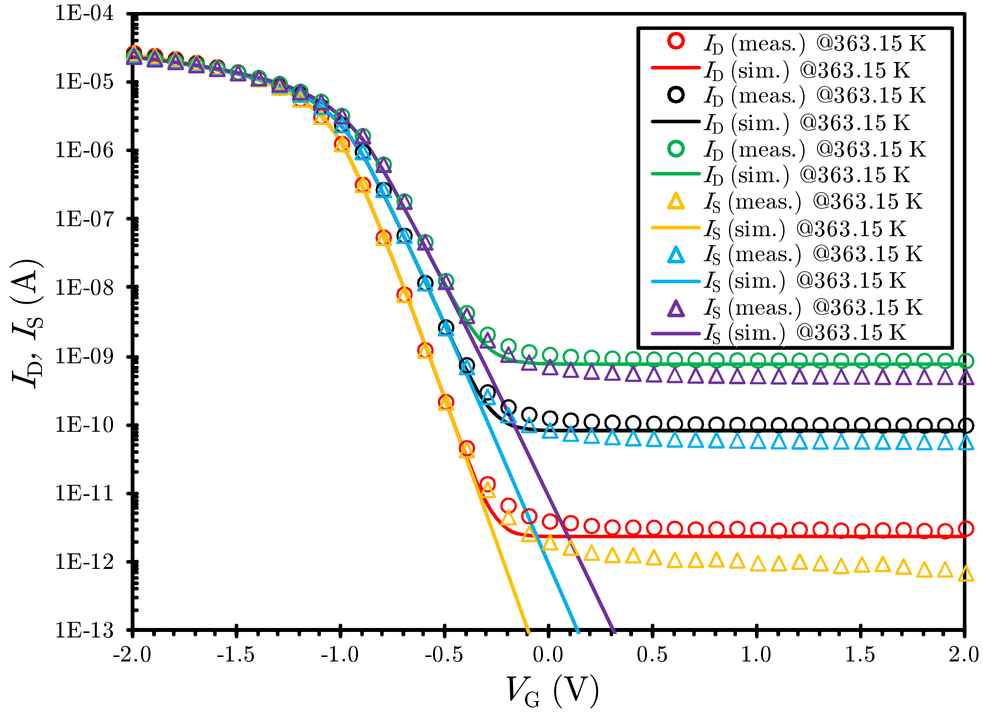


Figure 2.17. I_DV_G characteristics of MOSFET with $L_G = 2.5$ µm and $W_G = 50$ µm without parasitic BJTs (standard BSIM4).

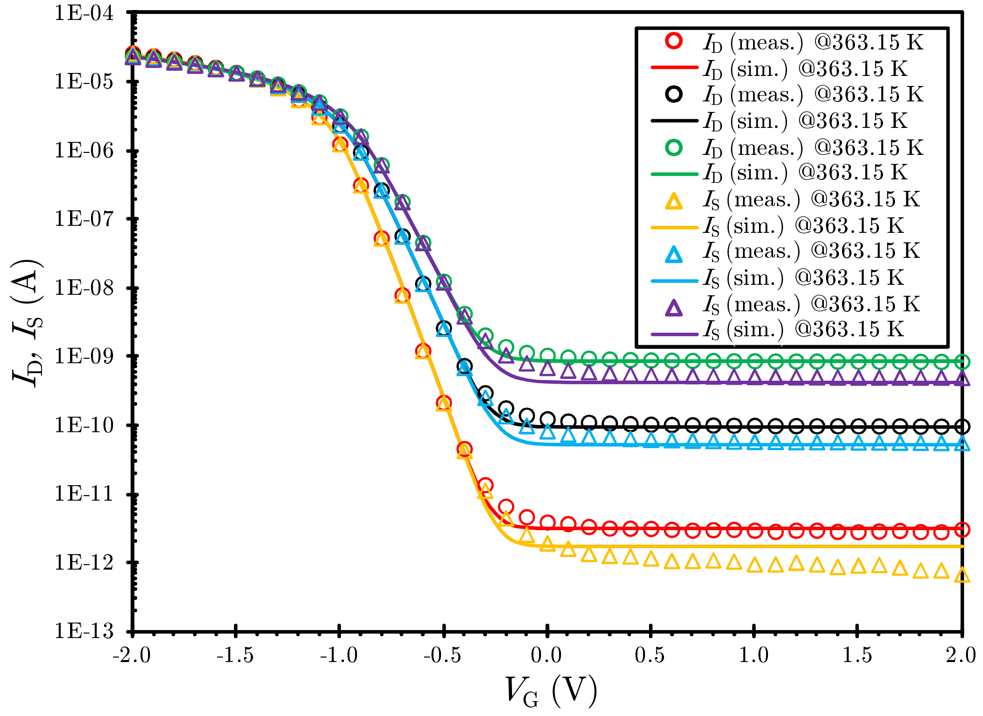


Figure 2.18. I_DV_G characteristics of MOSFET with $L_G = 2.5$ µm and $W_G = 50$ µm with parasitic BJTs.

The similar modeling approach, but without implemented scalability, is used in [21], where MOSFET and two substrate BJTs are parasitic devices and the main device is lateral BJT.

2.3 N-channel LDMOS

2.3.1 Crossection and modeling

The second selected testcase is the N-channel LDMOS scaled with the gate width only. A crossection of this device is depicted in Fig. 2.19. The drain is formed from nwell layer (contacted by N^+), the source from N^+ layer and the bulk from P layer. This configuration forms a different parasitic components than MOSFET in previous chapters. The substrate vertical parasitic BJT has a major influence on the leakage current. An emitter is formed from the bulk, a base from the drain and a collector from the substrate. This parasitic BJT is scaled with the gate width and the accuracy of the leakage current is significantly increased by adding this BJT to the standard BSIM model as is denoted in Fig. 2.20.

The LDMOS transistor is predominantly used in forward bias regime where the source is connected with the bulk. Hence the potential influence of the lateral parasitic BJT (nwell as an emitter, the bulk as a base and the source as a collector) is negligible.

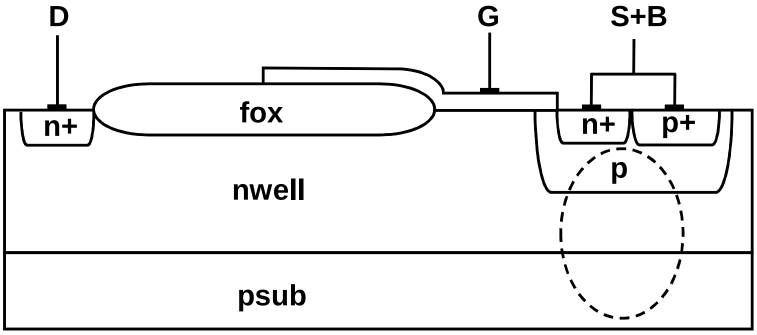


Figure 2.19. Crossection of N-channel LDMOS with indication of parasitic BJT.

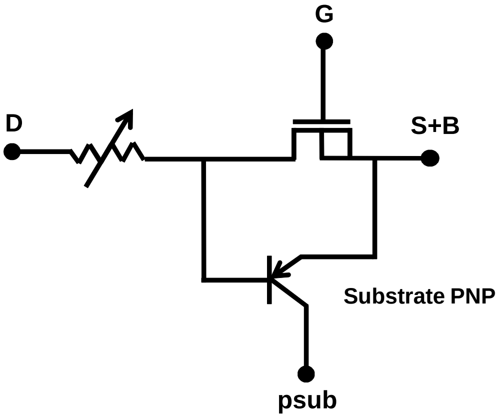


Figure 2.20. Updated LDMOS model with parasitic BJT.

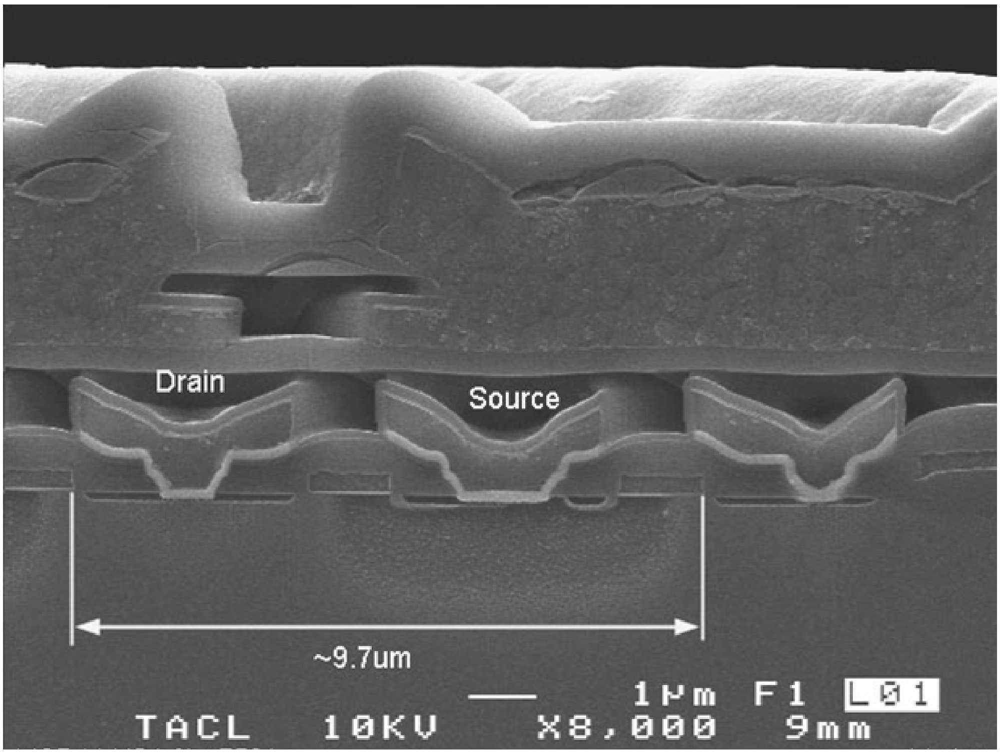


Figure 2.21. Photo of the LDMOS construction analysis - drain, source and gate are shown in detail.

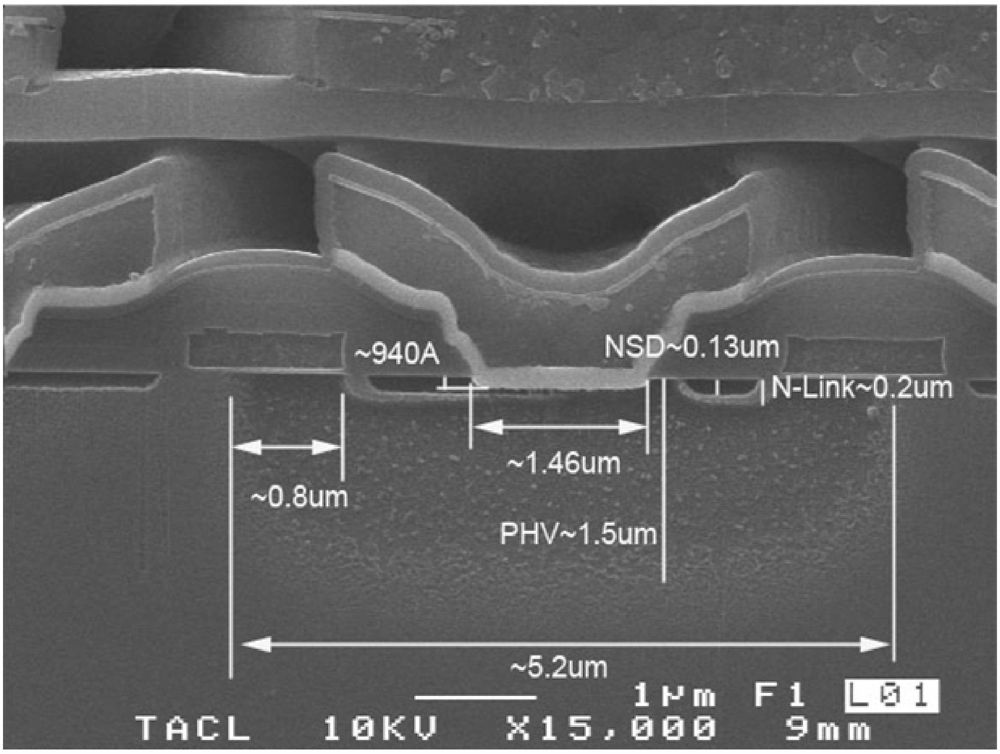


Figure 2.22. Photo of the LDMOS construction analysis - lateral diffusion of the bulk (PHV) defining gate length is shown in more detail.

2.3.2 Substrate vertical parasitic BJTs

Because the emitter of the parasitic BJT is formed from the bulk, the emitter area and perimeter depends only on the gate width

$$\begin{aligned} a_b &= W_\mathrm{G} L_\mathrm{B} \\ p_b &= 2(W_\mathrm{G} + L_\mathrm{B}) \end{aligned} \tag{15}$$

where W_G is the gate width of LDMOS, a_b and p_b are area and perimeter of the bulk (emitter) and L_B is the lengths of the bulk.

The model parameters of the parasitic BJTs reflect the dependency on gate width. The values of the model parameters are replaced by equations with scaling parameters.

The model parameter I_S is defined as

$$I_S = j_{sa} a_b + j_{sp} p_b + j_{sc} \tag{16}$$

where j_{sa}, j_{sp}, and j_{sc} are the extracted scaling parameters. This equation implies that the parameter I_S is linearly dependent on gate width W_G which is shown in Fig. 2.23.

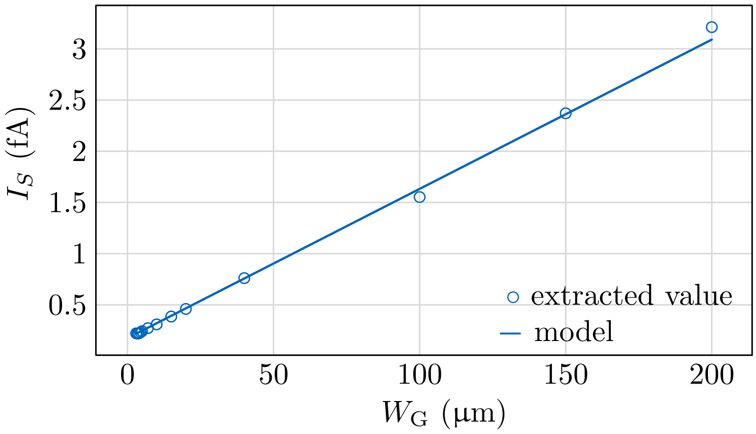


Figure 2.23. Vertical parasitic BJT: I_S vs W_G.

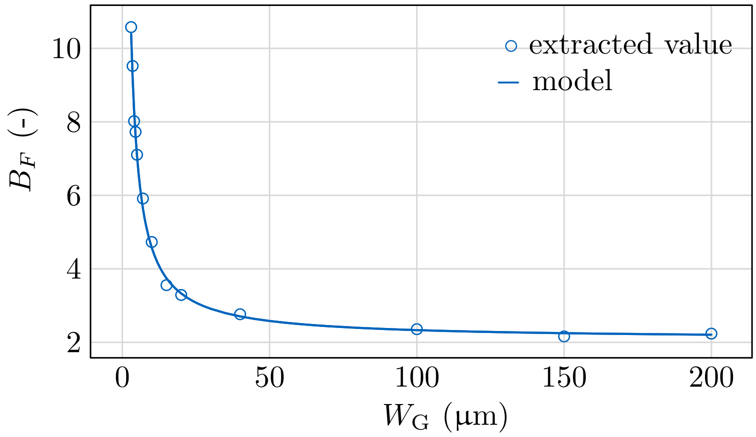


Figure 2.24. Vertical parasitic BJT: B_F vs W_G.

The model parameter B_F is nonlinear dependent on the gate width W_G and is expressed as

$$B_F = \frac{j_{sa}a_b + j_{sp}p_b + j_{sc}}{j_{ba}a_d + j_{bp}p_d + j_{bc}} \tag{17}$$

where j_{ba}, j_{bp}, and j_{bc} are the extracted scaling parameters. This dependency is shown in Fig. 2.24.

The model parameter I_{KF} (forward beta high current roll-off) is independent on the gate length L_G and linearly dependent on the gate width W_G

$$I_{KF} = j_{ka}a_b + j_{kp}p_b + j_{kc} \tag{18}$$

where j_{ka}, j_{kp}, and j_{kc} are the extracted scaling parameters.

The model parameters R_E (emitter resistance), R_C (collector resistance) and R_B (base resistance) are inversely proportional to the gate width W_G and are not dependent on the gate length L_G

$$R_E = \frac{1}{g_{ea}a_b + g_{ep}p_b + g_{ec}} \tag{19}$$

$$R_C = \frac{1}{g_{ca}a_b + g_{cp}p_b + g_{cc}} \tag{20}$$

$$R_B = \frac{1}{g_{ba}a_b + g_{bp}p_b + g_{bc}} \tag{21}$$

where g_{ea}, g_{ep}, g_{ec}, g_{ca}, g_{cp}, g_{cc}, g_{ba}, g_{bp}, and g_{bc} are the extracted scaling parameters.

The parasitic capacitance is modeled by the vertical BJTs. Therefore, the capacitance parameters of the lateral BJT (C_{JE}, C_{JC}) and source/drain junction diode parameters of MOSFET [12] (C_{JS}, C_{JD}, C_{JSWS}, C_{JSWD}, C_{JSWGS}, C_{JSWGD}, J_{SS}, J_{SD}, J_{SWS}, J_{SWD}, J_{SWGS}, J_{SWGD}) are suppressed (set to zero or very low value, e.g. 10^{-30}). The dependency of the model parameters C_{JE} and C_{JC} of the vertical BJTs on the gate width is linear

$$C_{JE} = c_{jea}a_b + c_{jep}p_b + c_{jec} \tag{22}$$

$$C_{JC} = c_{jca}a_d + c_{jcp}p_d + c_{jcc} \tag{23}$$

where c_{jea}, c_{jep}, c_{jec}, c_{jca}, c_{jcp}, and c_{jcc} are the extracted scaling parameters and a_d, p_d is the area and perimeter of the drain (nwell).

The parasitic vertical BJTs was measured and also its parameters were extracted based on the standard methodology described in [18]. Extracted parameters are summarized in Tab. 2.3.

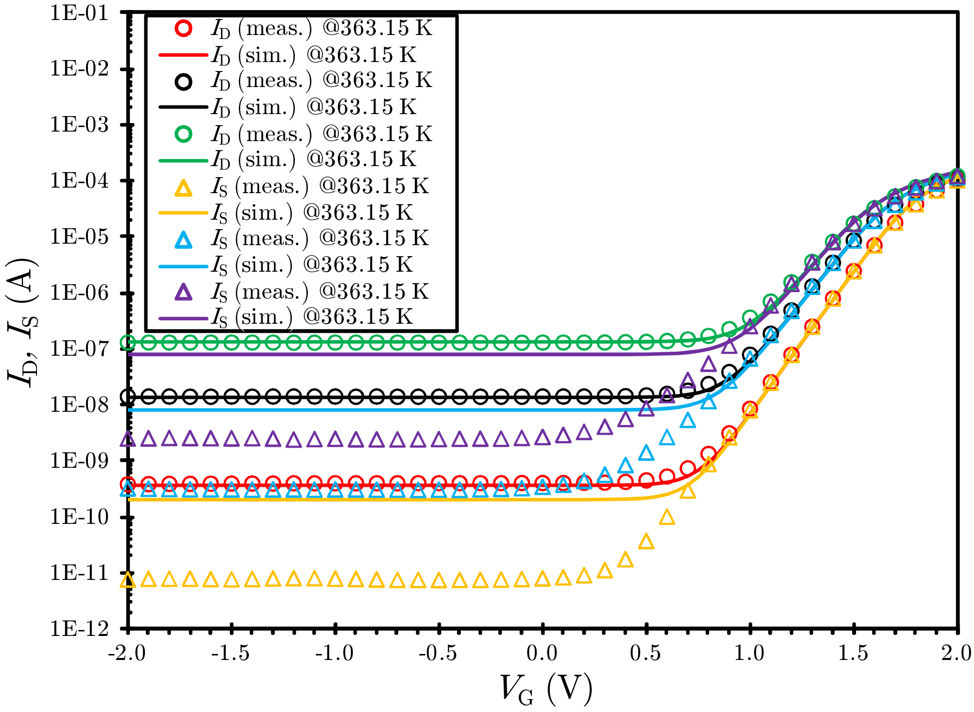


Figure 2.25. $I_D V_G$ characteristics of LDMOS with $W_G = 150$ μm without parasitic BJT.

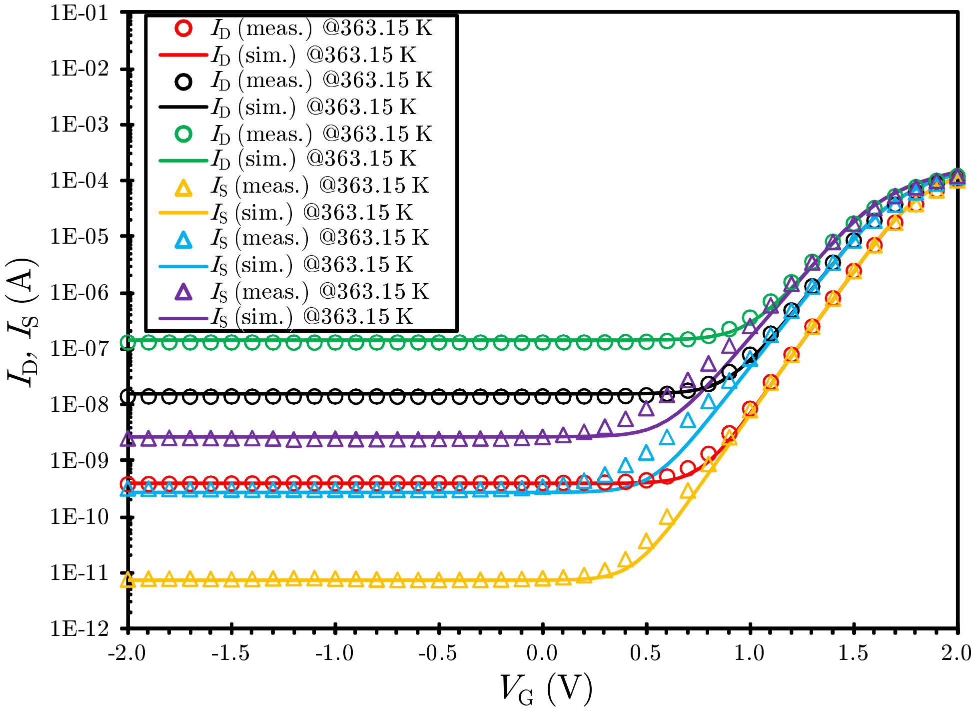


Figure 2.26. $I_D V_G$ characteristics of LDMOS with $W_G = 150$ μm with added parasitic BJT.

Scaling parameter	Unit	Value
j_{sa}	Am^{-2}	3.6×10^{-18}
j_{sp}	Am^{-1}	9×10^{-20}
j_{sc}	A	1.5×10^{-16}
j_{ba}	Am^{-2}	7×10^{-18}
j_{bp}	Am^{-1}	2×10^{-20}
j_{bc}	A	5×10^{-21}
j_{ka}	Am^{-2}	3.85×10^{-6}
j_{kp}	Am^{-1}	2.22×10^{-19}
j_{kc}	A	7.75×10^{-5}
g_{ea}	$\Omega^{-1}\mathrm{m}^{-2}$	6.6×10^{-5}
g_{ep}	$\Omega^{-1}\mathrm{m}^{-1}$	2×10^{-6}
g_{ec}	Ω^{-1}	5×10^{-5}
g_{ca}	$\Omega^{-1}\mathrm{m}^{-2}$	2×10^{-1}
g_{cp}	$\Omega^{-1}\mathrm{m}^{-1}$	8×10^{-3}
g_{cc}	Ω^{-1}	5×10^{-2}
g_{ba}	$\Omega^{-1}\mathrm{m}^{-2}$	1×10^{-4}
g_{bp}	$\Omega^{-1}\mathrm{m}^{-1}$	3.7×10^{-6}
g_{bc}	Ω^{-1}	2.1×10^{-5}
c_{jea}	Fm^{-2}	1.44×10^{-16}
c_{jep}	Fm^{-1}	1.3×10^{-15}
c_{jec}	F	2×10^{-16}
c_{jca}	Fm^{-2}	2.95×10^{-17}
c_{jcp}	Fm^{-1}	6.02×10^{-16}
c_{jcc}	F	2.1×10^{-17}

Table 2.3. Extracted parameters of the parasitic vertical BJT

The comparison of the $I_\mathrm{D}V_\mathrm{G}$ characteristics between standard LDMOS model and LDMOS with parasitic BJT is shown in Figs. 2.25 and 2.26. The source/bulk leakage current fitting of the LDMOS is improved by adding parasitic BJT. The gate leakage current (tunneling) modeling has been already presented in many publications, e.g. [22–25], but phenomena described in this chapter were mostly neglected.

2.4 Chapter Summary

In this chapter the accurate gate dimension dependent drain and source leakage modeling was presented (the structure of a proposed macro models, implemented scalability, developed scaling equations, and physical explanation of this scaling). Finally, the comparison of measured data vs. simulation is presented in order to confirm the model validity. This model improvement solves not only leakage current scaling, but it also accounts for additional parasitic bipolar effects, such as current injection to the substrate.

Chapter 3
HV Start-up MOSFET Description

This chapter describes the structure and applications of the high voltage power start-up MOSFET with integrated nonlinear spiral high voltage polysilicon divider. This start-up MOSFET transistor is used to minimizing the power consumption (structure and application patented by ON Semiconductor [26–27]). It is designed to provide initial current directly from the high voltage source. This MOSFET transistor charges up the regulator voltage on an external capacitor to about 14 V. The main goal is to minimize power consumption of the circuit that is directly connected to the rectified DC high voltage source. This high voltage can be up to 400 V for a 230 V AC supply and 700 V for switcher applications using power factor correction.

3.1 Structure Description

The HV start-up MOSFET is fabricated in an analog 1 μm CMOS technology. The simplified structure of this MOSFET is depicted in Fig. 3.1. The source and drain are formed from a low-doped Nwell1 and are contacted by N+ diffusion. The drain drift area is doped by Nwell2 that is deeper and more doped than Nwell1. Furthermore, the drain drift area contains a floating P doped resurf diffusion (ptop) fabricated before field oxide. The final doping concentration of the ptop is the same as of Nwell2 (but with different type of dopant) after all process steps. The concentration profiles are shown in Fig. 3.2 where is acceptor concentration (Fig. 3.2a), donor concentration (Fig. 3.2b) and total doping concentration (Fig. 3.2c). For abbreviations explanation see Appendix A.

The MOSFET bulk is created from Pwell not isolated from the P-substrate and it is covered by polysilicon gate. This drain-gate-source structure is rotary symmetrical around vertical axis in the center of the drain. It means that the drain is created in the shape of a circle and the gate and the source in the shape of an annulus.

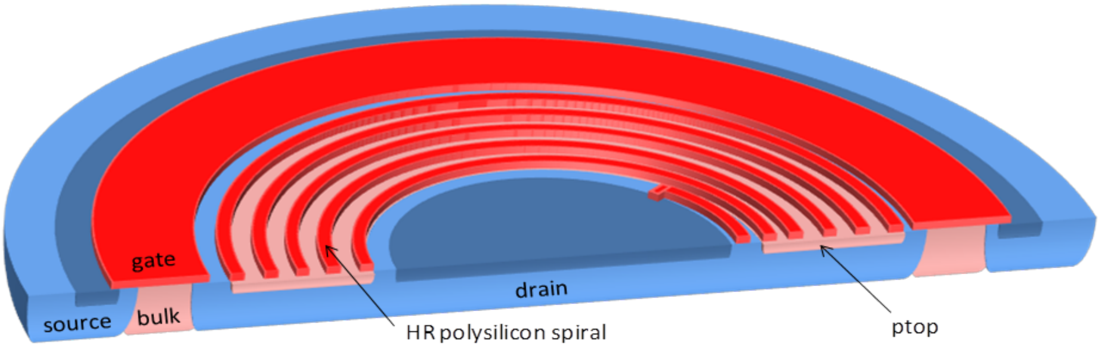
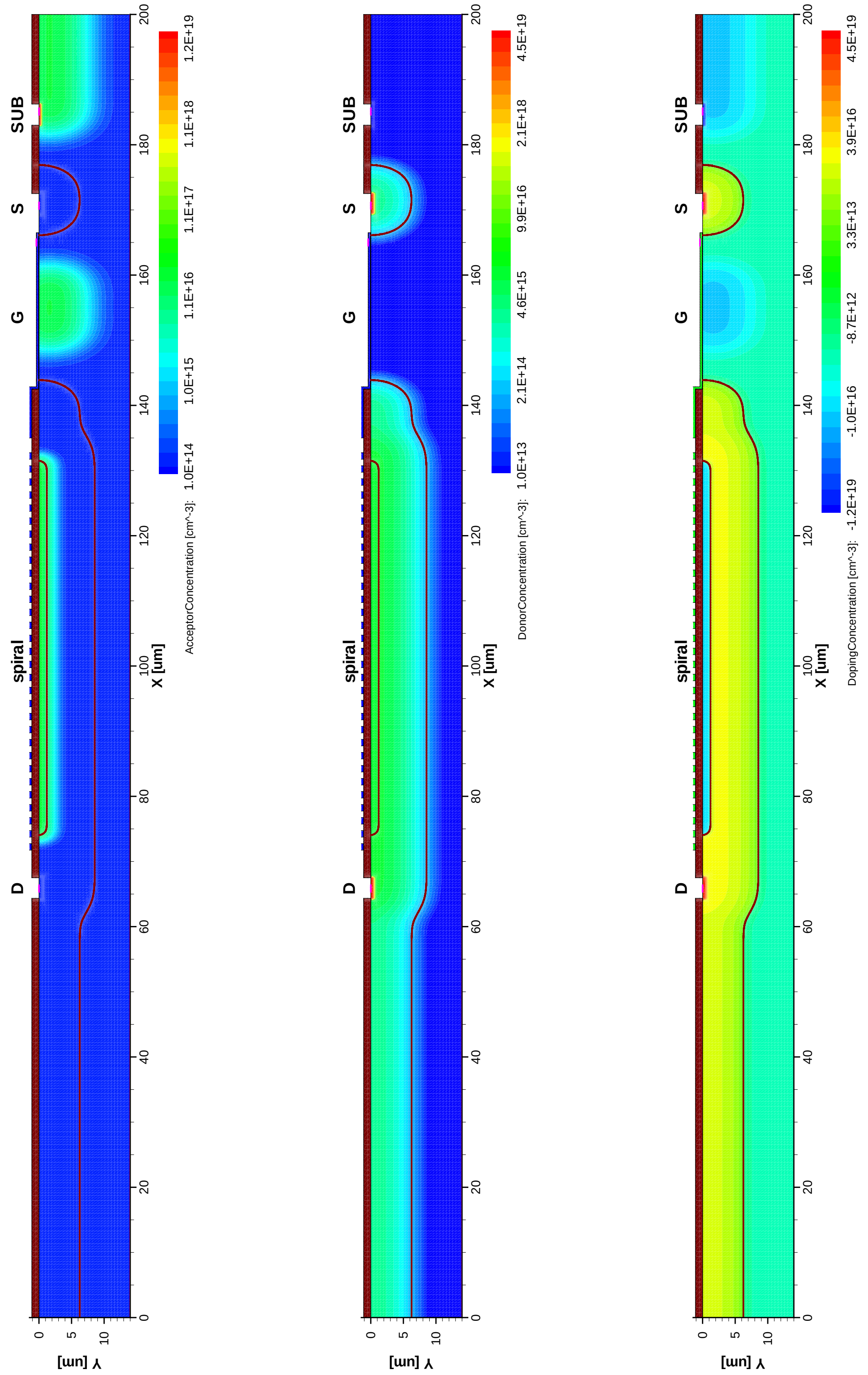


Figure 3.1. The simplified 3D structure of HV start-up MOSFET transistor.

The drain is located in the center of the device and contains a rounded bonding pad. A drain bonding wire is connected directly to this bonding pad and this is only one



a) b) c)

Figure 3.2. Concentration profiles: a) acceptor concentration, b) donor concentration and c) total doping concentration. Each figure has different contour range. The axial symmetry is in $X = 0$.

possible way how the drain can be connected. The oxide breakdown is much lower (about 100 V) than the maximum allowed drain voltage. The drain can be biased up to 700 V and this makes integrated direct sensing of the high drain voltage impossible. Hence, the high resistance polysilicon spiral voltage divider is used for the sensing of high drain voltage.

The spiral is connected to the drain and continues spirally toward the gate. How the polysilicon spiral divider is connected to other device components is depicted in the schematic symbol of HV MOSFET in the Fig. 3.3 (terminals d, tap1, tap2).

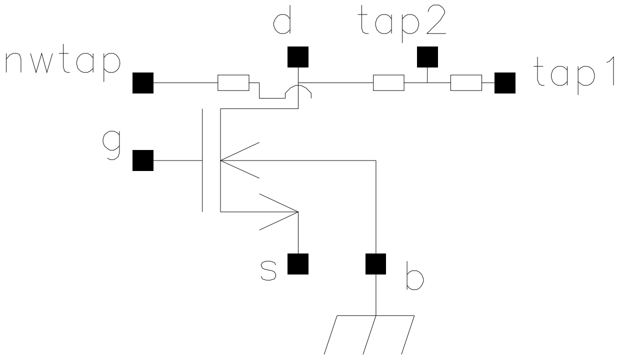


Figure 3.3. Schematic symbol of HV start-up MOSFET.

The spiral divider is designed to have the electric field distribution as much similar as possible as the drain drift area under it. This ensures the voltage between divider and silicon does not exceed oxide breakdown voltage. The polysilicon spiral divider has a big impact on a distribution of the electric field in the low doped drain drift area. And on the contrary, the strong electric field in the low doped drain drift area causes a lot of parasitic effects that have a big influence on DC and RF device characteristics. These effects can be observed later in modeling chapters were the results of TCAD simulations are shown.

These attributes make the modeling of this start-up MOSFET complicated, especially the divider ratio voltage and frequency dependency. The divider is usually modeled by the simple RC network, but there exist the operation areas where such simple model is not sufficient.

The layout of HV start-up MOSFET device as is seen by design engineers in layout editors (Cadence Virtuoso Layout Editor or Mentor Pyxis Layout) is depicted in Fig. 3.4.

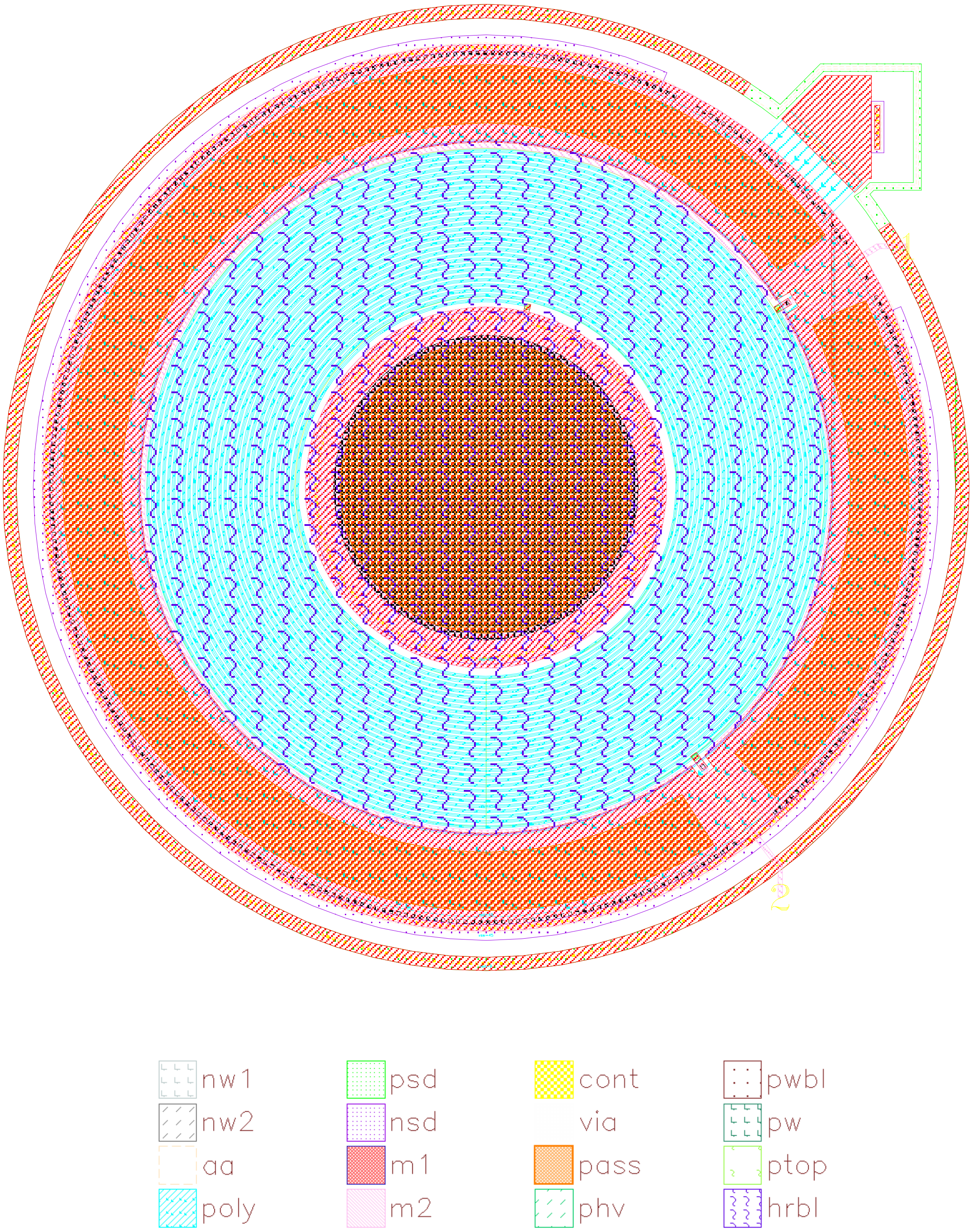


Figure 3.4. Layout of HV start-up MOSFET.

3.2 HV MOSFET Applications

The AC/DC convertor [28] has been selected as an example of a typical application of HV start-up MOSFET with the polysilicon spiral divider. The simplified AC/DC convertor circuit is depicted in Fig. 3.5. The HV start-up MOSFET subblock is modeled by the circuit in Fig. 4.7 and by the equations introduced in this thesis.

The voltage reference V_{ref1} determines the voltage (in Comparator A) to which the external capacitor C_{vcc} is charged up and basically determines the voltage at which the HV start-up MOSFET is switched off. This solution decreases the power consumption in comparison with older solution where the external capacitor C_{vcc} was permanently charged through an external resistor. The solution with HV spiral divider enables to switch off the charging in case the external capacitor C_{vcc} is charged up enough. The voltage reference V_{ref2} determines when the whole AC/DC convertor is switched on based on the direct sensing of high voltage by the spiral divider described in this thesis. The high input voltage is divided by the spiral divider and compared in Comparator B with the voltage reference V_{ref2}. It means that the AC/DC convertor is turned off if the input high voltage is lower than defined value (depends on product specification, e.g. 112 V). For more applications see [29] for design of a 65 W adapter, [30] for 32 W, 32 V universal input AC-DC printer adapter, and [31] for designing converters with the NCP101X family.

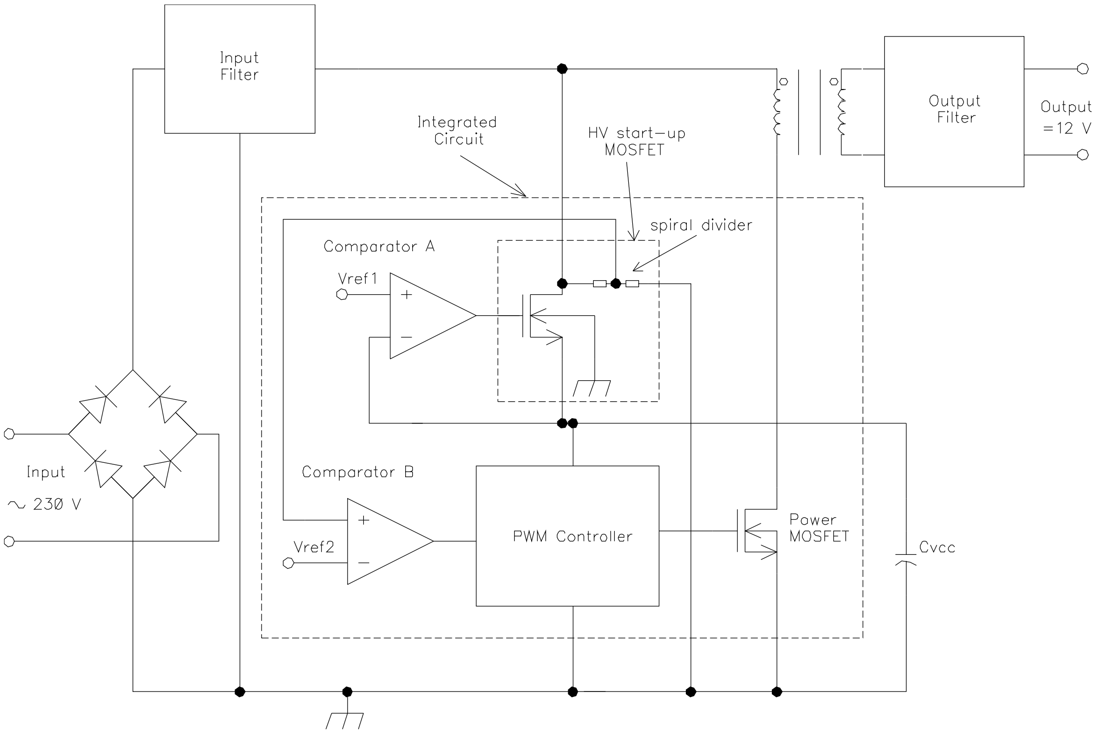


Figure 3.5. The simplified circuit of AC/DC convertor. The HV start-up MOSFET subblock is modeled by the circuit in Fig. 4.7.

The circuits that use HV start-up MOSFET with spiral divider allow designing applications with many features such as:

- The Dynamic Self-Supply
- No need of auxiliary winding [31]
- Low Standby-Power

- High Voltage Sensing
- Brown-out Protection [29]
- Line Overvoltage Protection [29].

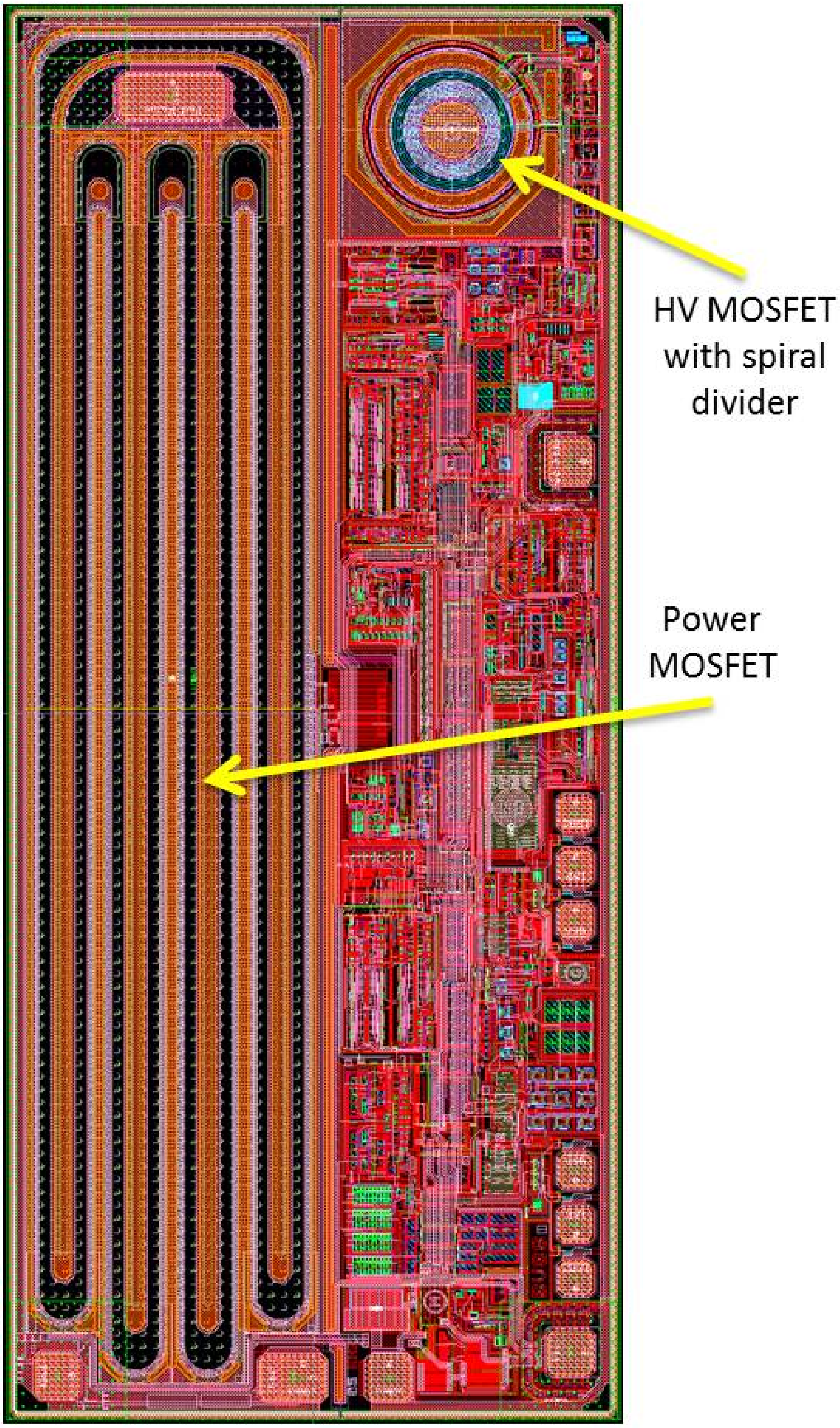


Figure 3.6. Layout of AC/DC convertor.

Chapter 4
Spiral Divider Modeling

This chapter deals with the proposed and implemented DC and AC model of the nonlinear spiral high voltage polysilicon divider which is one of the fundamental results (new scientific findings) of this thesis. For the purpose of the equivalent lumped element circuit creation the polysilicon spiral is divided into several separate spiral elements. This division is shown in Fig. 4.1(a) where each spiral element has a different color. For better lucidity only the first four turns are depicted in this figure. The equivalent 3D circuit in Fig. 4.1(b) is obtained if these spiral elements are uncoiled to parallel plains. The 3D equivalent circuit in Fig. 4.1(b) can be redrawn for better lucidity to the 2D equivalent circuit, which is depicted in Fig. 4.2.

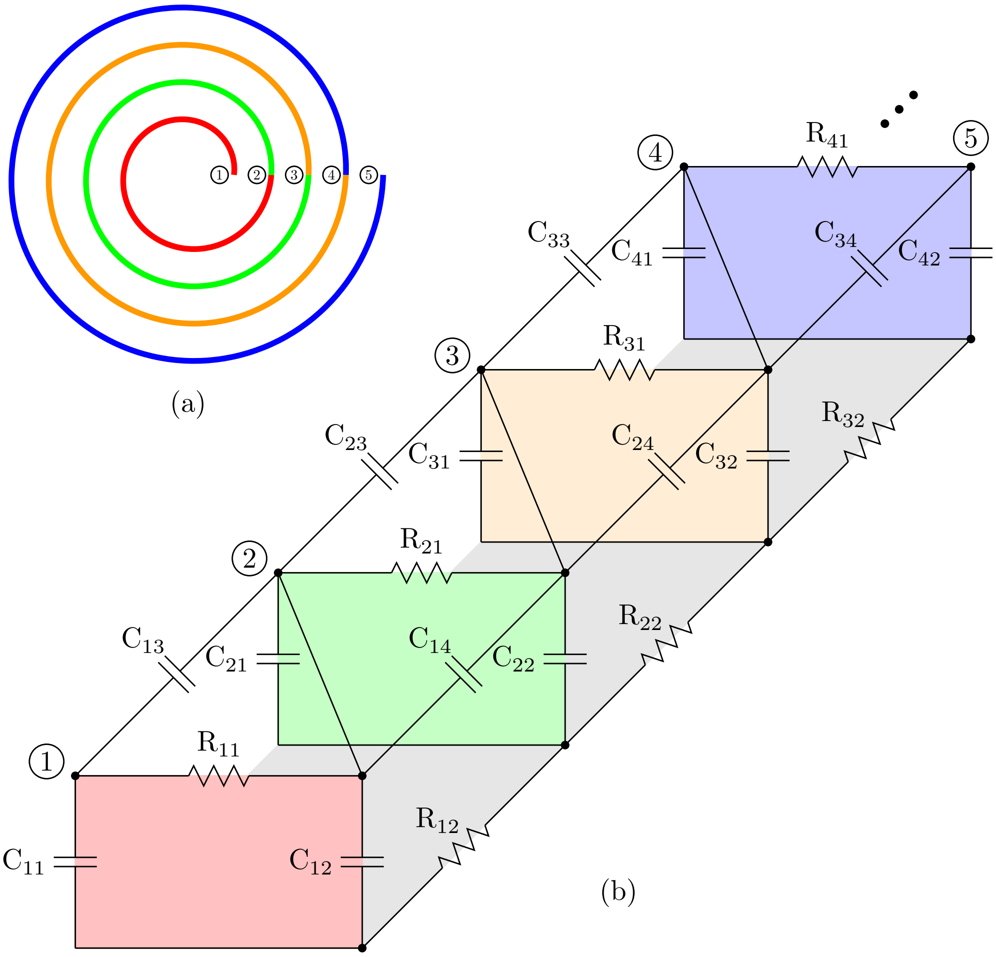


Figure 4.1. Equivalent lumped 3D circuit of first four spiral poly subsegments and ptop: (a) colored spiral subsegment, (b) equivalent circuit. Colors from (a) match (b).

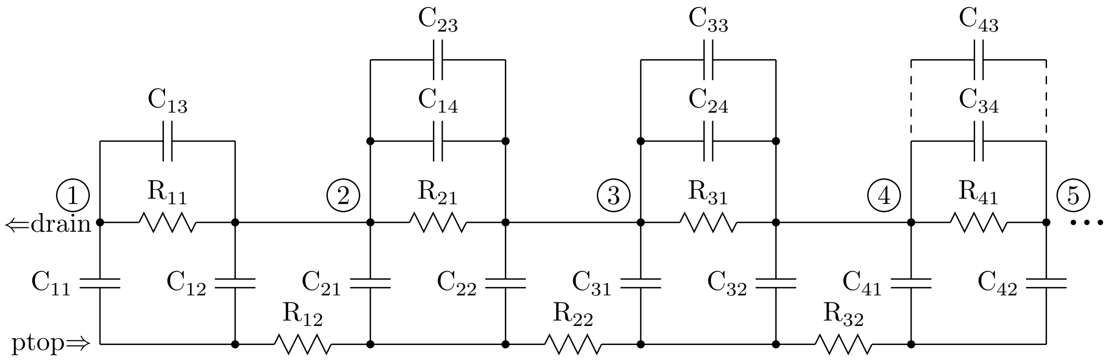


Figure 4.2. Equivalent lumped 2D circuit of first four spiral poly subsegments and ptop.

4.1 Spiral Element Length

In this section the length L of a spiral is determined. The spiral divider of the HV MOSFET transistor is a special case of the Archimedes spiral. The radius r of the spiral is increased in one turn by a radius increment Δr. The basic equation defined in polar coordinates for the radius is

$$r = r_0 + \varphi\frac{\Delta r}{2\pi} \tag{24}$$

where r_0 is an initial radius of the spiral and φ is an actual angle circumscribed by the spiral. The parameters of the spiral are depicted in Figure 4.3.

The curve length can be calculated in the following way. If $f(\varphi)$ is the function of the curve in polar coordinates then the length L of the curve is defined as

$$L = \int_{\psi}^{\phi} \sqrt{[f(\varphi)]^2 + \left(\frac{\mathrm{d}f(\varphi)}{\mathrm{d}\varphi}\right)^2}\,\mathrm{d}\varphi \tag{25}$$

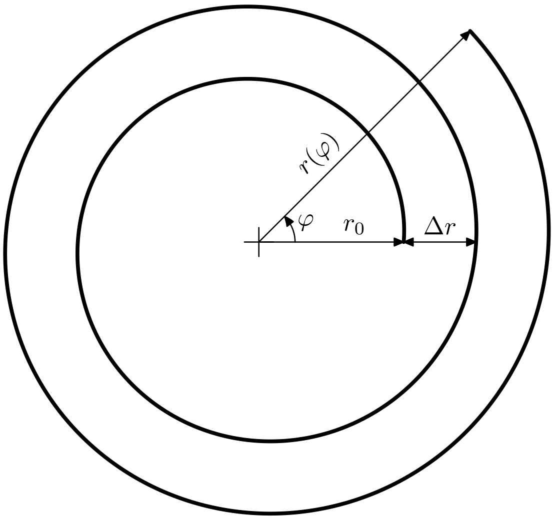


Figure 4.3. Schematic drawing of the spiral parameters.

For the spiral defined in polar coordinates by (24) the spiral length L is obtained by substituting the equation (24) into (25):

$$L = \int_{\psi}^{\phi} \sqrt{\left(r_0 + \varphi\frac{\Delta r}{2\pi}\right)^2 + \left(\frac{\Delta r}{2\pi}\right)^2} \mathrm{d}\varphi \tag{26}$$

where ϕ is an angle circumscribed by a whole spiral. The beginning of the spiral is given by initial radius r_0 and therefore it is assumed the starting angle $\psi = 0$. The solution of the integral yields the following expression

$$\begin{aligned} L = & \frac{\Delta r}{4\pi} \ln\left(\frac{r_0 + \phi\frac{\Delta r}{2\pi} + \sqrt{\left(r_0 + \phi\frac{\Delta r}{2\pi}\right)^2 + \frac{\Delta r^2}{4\pi^2}}}{r_0 + \sqrt{r_0^2 + \frac{\Delta r^2}{4\pi^2}}}\right) + \\ & + \left(\frac{r_0\pi}{\Delta r} + \frac{\phi}{2}\right)\sqrt{\left(r_0 + \phi\frac{\Delta r}{2\pi}\right)^2 + \frac{\Delta r^2}{4\pi^2}} - \frac{r_0\pi}{\Delta r}\sqrt{r_0^2 + \frac{\Delta r^2}{4\pi^2}} \end{aligned} \tag{27}$$

The logarithmic term in (27) can be neglected. The difference caused by neglecting this logarithm therm is below 0.05 % for initial radiuses bigger than 10 µm. The equation for the length L of the spiral after neglecting logarithmic term reduces to

$$L = \left(\frac{r_0\pi}{\Delta r} + \frac{\phi}{2}\right)\sqrt{\left(r_0 + \phi\frac{\Delta r}{2\pi}\right)^2 + \frac{\Delta r^2}{4\pi^2}} - \frac{r_0\pi}{\Delta r}\sqrt{r_0^2 + \frac{\Delta r^2}{4\pi^2}} \tag{28}$$

When $\Delta r << r_0$ then the equation (28) can be simplified to

$$L = r_0\phi + \frac{\Delta r}{4\pi}\phi^2 \tag{29}$$

and the length of the spiral segment between angles φ_1 and φ_2 can be calculated based on (29) as

$$L_{\varphi_1,\varphi_2} = r_0(\varphi_2 - \varphi_1) + \frac{\Delta r}{4\pi}(\varphi_2^2 - \varphi_1^2) \tag{30}$$

The calculated and process parameters of the spiral are summarized in Table 4.1 and calculated parameters of each spiral segment are summarized in Table 4.2.

Parameter	Value	Unit	Note
r_0	72.47	µm	initial radius of the spiral
Δr	2	µm	radius increment
L_{tot}	19208	µm	whole spirale length
L_2	192.69	µm	sense spiral segment length
R_{SHpoly}	5000	Ω/sq	HR polysilicon sheet resistance
R_{tot}	96.041	MΩ	whole spirale resistance
R_2	963.5	kΩ	sense spiral segment resistance
t_{poly}	350	nm	polysilicon thickness
t_{FOX}	1.1	µm	field oxide thickness
W_{poly}	1	µm	polysilicon width

Table 4.1. Calculated and process parameters of the spiral (for $V_D \to 0$).

Spiral segment order	φ_1 [rad]	φ_2 [rad]	Length [µm]	Calc. resistance (@$V_D \to 0$) [MΩ]
1	0π	2π	461.63	2.308
2	2π	4π	474.19	2.371
3	4π	6π	486.76	2.434
4	6π	8π	499.32	2.497
5	8π	10π	511.89	2.559
6	10π	12π	524.46	2.622
7	12π	14π	537.02	2.685
8	14π	16π	549.59	2.748
9	16π	18π	562.16	2.811
10	18π	20π	574.72	2.874
11	20π	22π	587.29	2.936
12	22π	24π	599.86	2.999
13	24π	26π	612.42	3.062
14	26π	28π	624.99	3.125
15	28π	30π	637.55	3.188
16	30π	32π	650.12	3.251
17	32π	34π	662.69	3.313
18	34π	36π	675.25	3.376
19	36π	38π	687.82	3.439
20	38π	40π	700.39	3.502
21	40π	42π	712.95	3.565
22	42π	44π	725.52	3.628
23	44π	46π	738.09	3.690
24	46π	48π	750.65	3.753
25	48π	50π	763.22	3.816
26	50π	52π	775.78	3.879
27	52π	54π	788.35	3.942
28	54π	56π	800.92	4.005
29	56π	58π	813.48	4.067
30	58π	186.227	526.35	2.632
31	186.227	187.687	192.69	0.963

Table 4.2. Calculated parameters of the spiral segments

The resistances for $V_D \to 0$ are calculated as

$$R_2 = R_{\text{SHpoly}} \frac{L_2}{W_{\text{poly}}} \tag{31}$$

$$R_{\text{tot}} = R_{\text{SHpoly}} \frac{L_{\text{tot}}}{W_{\text{poly}}} \tag{32}$$

and lengths L_{tot} and L_2 are calculated by (29). Symbols are explained in Table 4.1.

4.2 Divider Ratio Modeling

A simpler way of the divider ratio modeling has been published in [32] but without ratio scalability, temperature and statistical modeling. This two important model abilities has been developed and implemented into the enhanced model that has been published in [33] and is introduced in this chapter.

The divider ratio is dependent on the drain and source voltage V_D and V_S. The voltage dependency caused by depletion effects in the ptop and nwell layers is modeled by Verilog-A code using nonlinear functions. The increasing of the drain voltage causes the depletion of the ptop and nwell and when the ptop is fully depleted under the spiral polysilicon divider then it causes a change of the ratio voltage dependency slope as is depicted in Fig. 4.4.

The geometrical ratio is expressed as

$$ratio_{\mathrm{geom}} = \frac{L_1 + L_2}{L_2} \tag{33}$$

where L_1 and L_2 are long and sensing part of the spiral. Based on (29) the geometrical ratio is finally calculated as

$$ratio_{\mathrm{geom}} = \frac{4\pi r_0(\varphi_{\mathrm{tap1}} - \varphi_D) + \Delta r(\varphi_{\mathrm{tap1}}^2 - \varphi_D^2)}{4\pi r_0(\varphi_{\mathrm{tap1}} - \varphi_{\mathrm{tap2}}) + \Delta r(\varphi_{\mathrm{tap1}}^2 - \varphi_{\mathrm{tap2}}^2)} \tag{34}$$

where φ_D, φ_{tap1} and φ_{tap2} are drain, tap1 and tap2 angles on the spiral.

The electrical ratio is expressed as

$$ratio_{\mathrm{el}} = \frac{V_D}{V_{\mathrm{tap2}}} \tag{35}$$

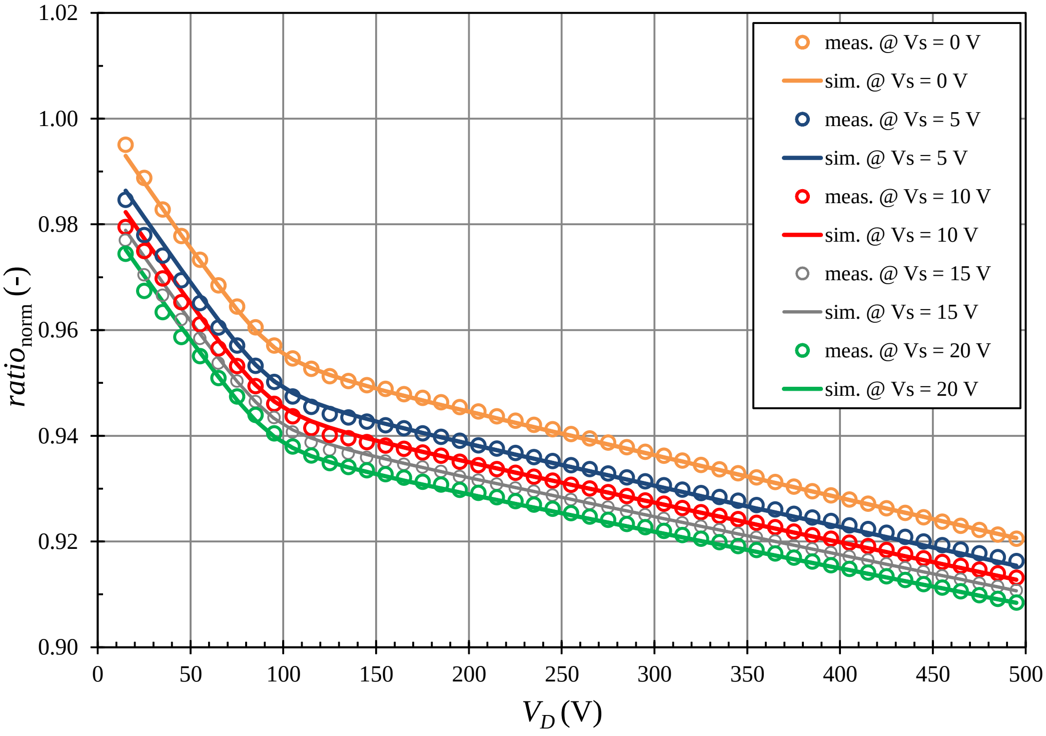


Figure 4.4. Drain and source voltage dependency of normalized ratio.

where V_D and V_{tap2} are voltages on pins drain and tap2.

The normalized ratio is defined as

$$ratio_{\text{norm}} = \frac{ratio_{\text{el}}}{ratio_{\text{geom}}} \tag{36}$$

that is modeled as

$$ratio_{\text{norm}} = 1 + \beta_{\text{D1}} + \text{VSS}_1 \left(1 + \frac{1}{2}\tanh\frac{V_S}{\text{VSS}_2}\right) V_S + \beta_{\text{D2}}\left(1 + \text{VSS}_3 \cdot V_S\right) V_D \tag{37}$$

where β_{D1} and β_{D2} are voltage dependency coefficients (see equations (38), (39) and (40)), VSS_1, VSS_2 and VSS_3 are source voltage dependency model parameters and V_S is source voltage. The parameter VSS_1 determines a linear dependency of $ratio_{\text{norm}}$ on V_S, while the parameter VSS_2 a nonlinear dependency. The parameter VSS_3 influences the slope of the curve (for $V_D > V_P$) depending on V_S.

The voltage dependency coefficient β_{D1} is expressed as

$$\beta_{D1} = \begin{cases} \text{VDD}_1 \cdot V_D & \text{for } V_D \le V_P \\ \text{VDD}_2 & \text{for } V_D > V_P \end{cases} \tag{38}$$

where VDD_1 and VDD_2 are drain voltage dependency model parameters and V_P is the ptop pinch-off voltage. The parameter VDD_1 represents the slope of the curve (for $V_D \le V_P$) depending on V_D and the parameter VDD_2 determines a linear absolute shift of $ratio_{\text{norm}}$ for $V_D > V_P$.

To ensure smoothness (to avoid convergency issue) (38) can be modeled as

$$\beta_{D1} = \frac{1}{2}\left(\text{VDD}_1 \cdot V_D + \text{VDD}_2 + \sqrt{\left(\text{VDD}_1 \cdot V_D - \text{VDD}_2\right)^2 + \text{k}_\text{D}}\right) \tag{39}$$

where k_D is smoothness parameter that determines smooth transition between two cases in (38).

The voltage dependency coefficient β_{D2} is temperature dependent and can be expressed as

$$\beta_{D2} = \text{VDD}_3\Big[1 + \alpha_D\left(T - T_{\text{nom}}\right)\Big] \tag{40}$$

where T is temperature, model parameter VDD_3 represents the slope of the curve (for $V_D > V_P$) depending on V_D at nominal temperature T_{nom} and α_D is temperature coefficient. The extracted ratio model parameters are summarized in Table 4.3.

Parameter	Value	Unit
VDD_1	-4.30×10^{-4}	V^{-1}
VDD_2	-3.95×10^{-2}	-
VDD_3	-8.30×10^{-5}	V^{-1}
VSS_1	-1.8×10^{-3}	V^{-1}
VSS_2	-10	V
VSS_3	-8.5×10^{-3}	V^{-1}
k_D	-4.3×10^{-4}	-
α_D	1.1×10^{-4}	K^{-1}
$ratio_{\text{mult}}$	0.916	-
$ratio_{\Delta}$	1.6	-

Table 4.3. Extracted ratio model parameters.

The final equation for $ratio_{\text{norm}}$ is

$$\begin{aligned} ratio_{\text{norm}} = 1 + \text{VSS}_1 \left(1 + \frac{1}{2}\tanh\frac{V_S}{\text{VSS}_2}\right) V_S + \\ + \frac{1}{2}\left(\text{VDD}_1 \cdot V_D + \text{VDD}_2 + \sqrt{(\text{VDD}_1 \cdot V_D - \text{VDD}_2)^2 + \text{k}_\text{D}}\right) + \\ + \text{VDD}_3 \Big[1 + \alpha_D \left(T - T_{\text{nom}}\right)\Big] \left(1 + \text{VSS}_3 \cdot V_S\right) V_D \end{aligned} \tag{41}$$

The model is scalable by an editable model argument $ratio_{\text{geom}}$ that is refined to

$$ratio'_{\text{geom}} = \left(ratio_{\text{mult}}\, ratio_{\text{geom}} - ratio_{\Delta}\right)\delta_{\text{ratio}} \tag{42}$$

where $ratio_{\text{mult}}$ and $ratio_{\Delta}$ are model fitting parameters for ratio scalability and δ_{ratio} is relative statistical mismatch model parameter.

4.3 Divider Dynamical Modeling

The AC response is modeled by a distributed RC network. The measurement setup for divider AC measurement is depicted in Fig. 4.5. The GSG (Ground-Signal-Ground) structure used for AC measurement is shown in Fig. 4.6. The magnitude and phase of the normalized ratio are depicted in Figs. 4.8 and 4.9.

4.3.1 Spiral segments resistance

The high resistance polysilicon spiral segments are modeled by the Verilog-A code. Each resistor segment has a length L_n equal to a length of one turn and is modeled as

$$R_{\text{segn}} = R_{\text{tot}} \frac{L_{\text{segn}}}{L_{\text{tot}}} \tag{43}$$

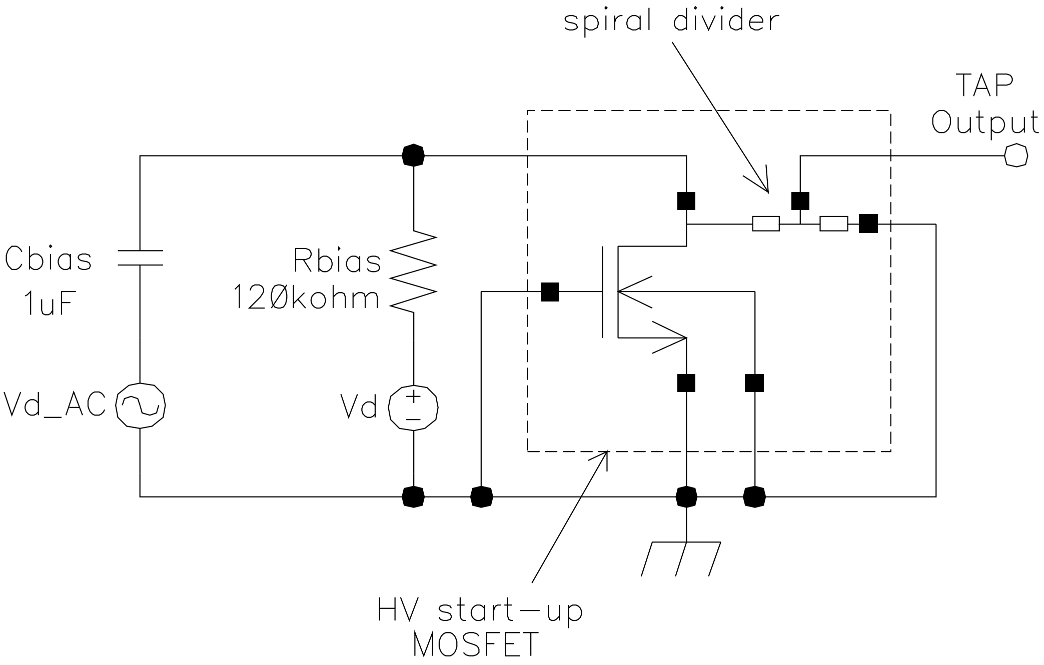


Figure 4.5. Measurement setup for divider AC measurement.

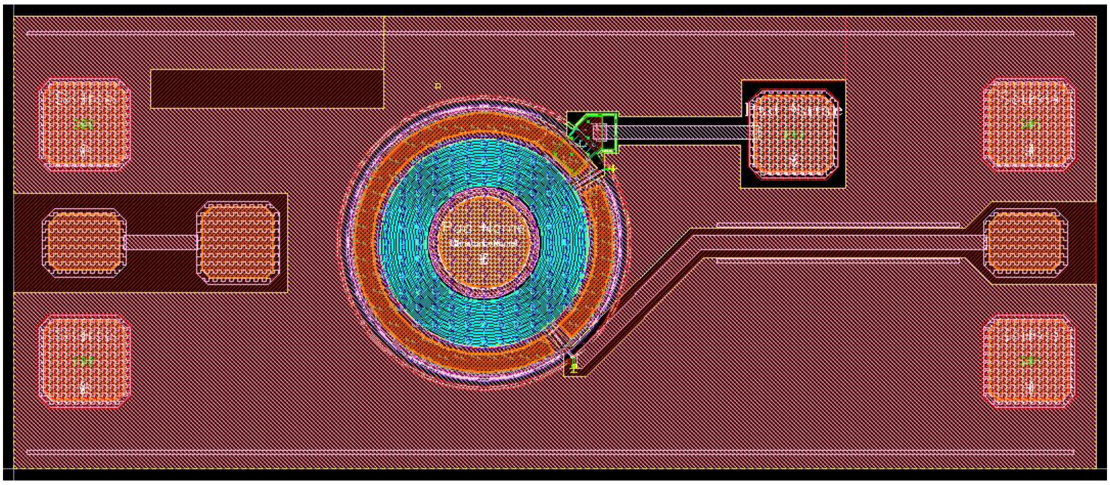


Figure 4.6. Layout of HV MOSFET for divider AC measurement.

where n is the spiral segment order and L_{tot} is a total spiral divider length. R_{tot} is total spiral divider resistance calculated as

$$R_{\text{tot}} = \frac{R_{\text{SHpoly}}\, L_{\text{tot}} \left[1 + \alpha_{\text{p1}} \left(T - T_{\text{nom}}\right) + \alpha_{\text{p2}} \left(T - T_{\text{nom}}\right)^2\right]}{W_{\text{poly}} + \delta_W} \tag{44}$$

where R_{SHpoly} is polysilicon spiral sheet resistance, W is spiral segment width, δ_W is absolute statistical process model parameter, α_{p1} and α_{p2} are temperature coefficients dependent on R_{SHpoly}

$$\begin{aligned} \alpha_{\text{p1}} =& \alpha_{\text{rsh1}} R_{\text{SHpoly}} + \alpha_{\text{rp1}} \\ \alpha_{\text{p2}} =& \alpha_{\text{rsh2}} R_{\text{SHpoly}} + \alpha_{\text{rp2}} \end{aligned} \tag{45}$$

where α_{rsh1}, α_{rsh2}, α_{rp1}, and α_{rp2} are polysilicon temperature coefficients. These coefficients was extracted from three experimental process split wafers (implant dose 85 %, 100 % and 115 %) and extracted values are summarized in Table 4.4

Parameter	Value	Unit
α_{rsh1}	-4.8×10^{-7}	$\Omega^{-1}\text{K}^{-1}\text{sq}$
α_{rsh2}	1.9×10^{-9}	$\Omega^{-1}\text{K}^{-2}\text{sq}$
α_{rp1}	-1.6×10^{-3}	K^{-1}
α_{rp2}	6.0×10^{-6}	K^{-2}

Table 4.4. Extracted resistance temperature model parameters.

The resistance of the sense segment is

$$R_{sense} = \frac{R_{\text{tot}}}{ratio_{\text{norm}}\, ratio'_{\text{geom}}} \tag{46}$$

The full macromodel circuit of HV start-up MOSFET is shown in Fig. 4.7.

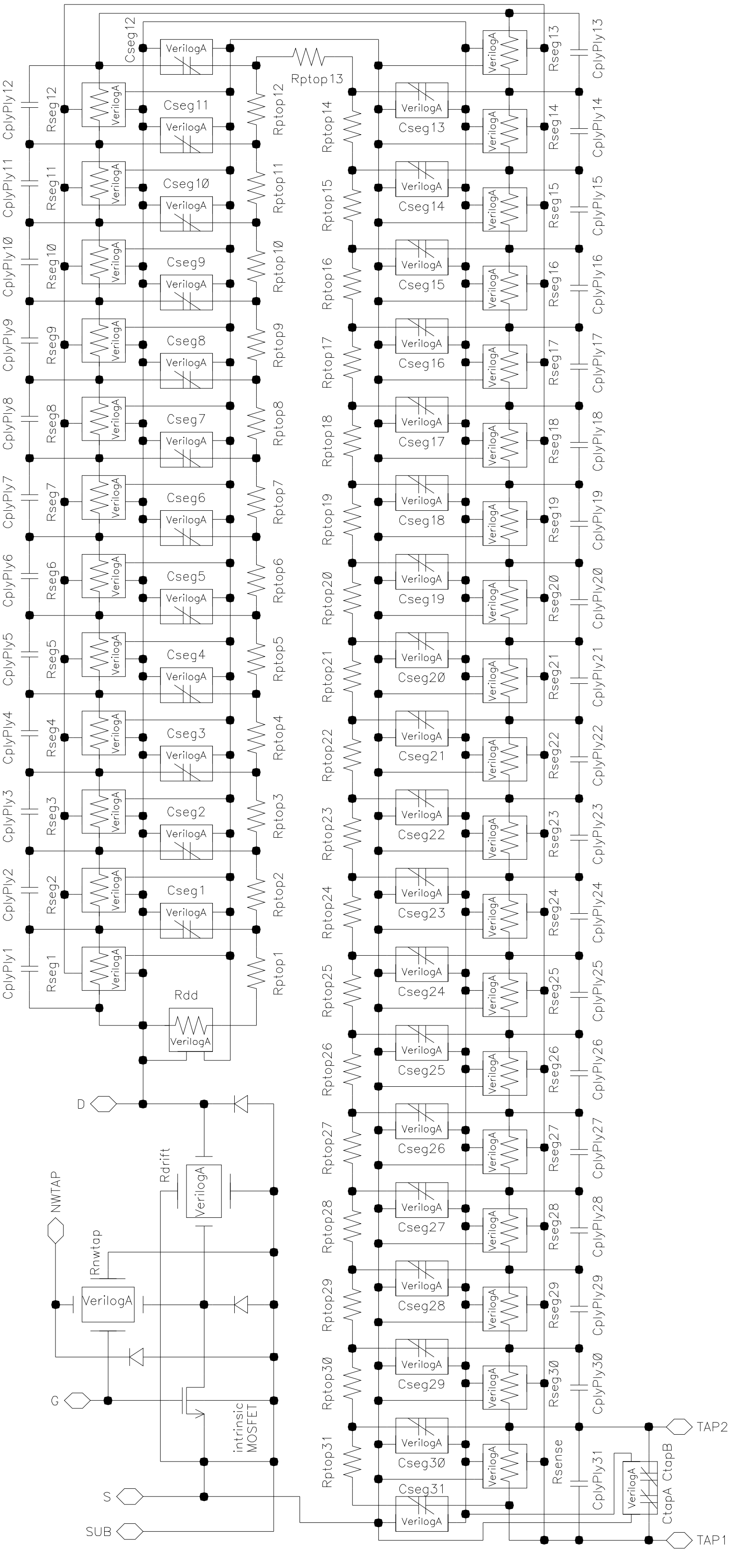


Figure 4.7. The full macromodel circuit of HV MOSFET with polysilicon spiral divider.

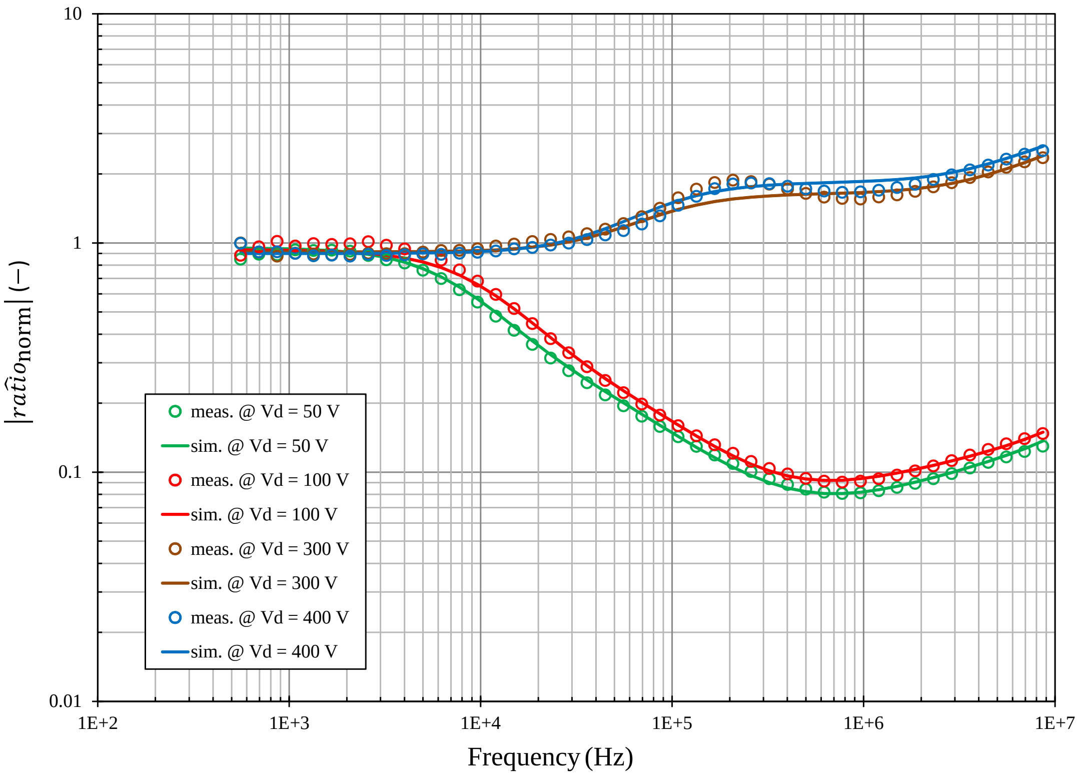


Figure 4.8. Magnitude of normalized complex divider ratio.

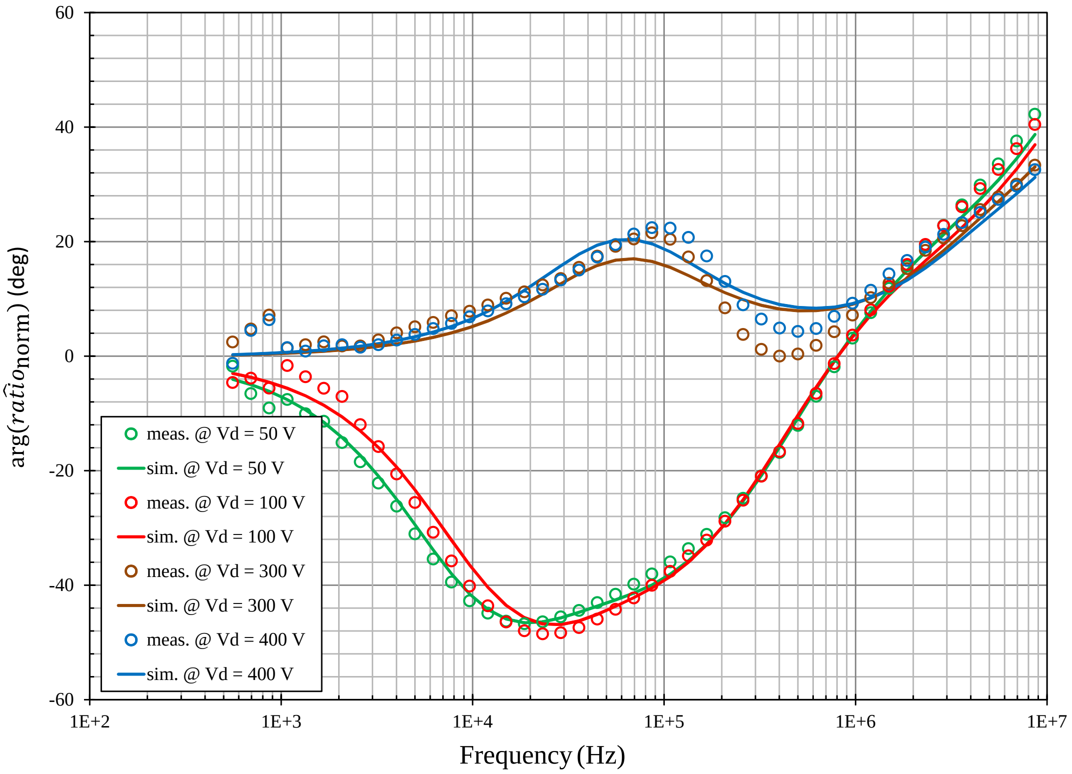


Figure 4.9. Phase of normalized complex divider ratio.

4.3.2 Spiral to silicon capacitance

The capacitances are modeled by the Verilog-A code and are voltage dependent similarly as resistances. The voltage dependency is caused by depleting effects of very low doped drift drain area due to the high electric field. Each capacitor segment is modeled as

$$C_{\text{seg}n} = C_{\text{PPpfld}} \left(W_{\text{poly}} + \delta_W \right) L_{\text{seg}n} \, \beta_{\text{cor}n} \tag{47}$$

where C_{PPpfld} is polysilicon (field oxide) capacitance per unit area, W is spiral segment width, and $\beta_{\text{cor}n}$ is voltage dependency correction coefficient calculated for each spiral segment n as

$$\beta_{\text{cor}n} = c_{\text{sp}n} + \frac{\Delta_{\text{csp}n}}{2} \left(1 + \tanh \frac{V_D - V_{\text{P}n}}{c_{\text{sl}n}} \right) \tag{48}$$

where $c_{\text{sp}n}$, $\Delta_{\text{csp}n}$, $V_{\text{P}n}$, and $c_{\text{sl}n}$ are voltage dependent capacitance model fitting parameters. The parameter $c_{\text{sp}n}$ determines the value of coefficient $\beta_{\text{cor}n}$ for $V_D \leq V_{\text{P}n}$, while the parameter $\Delta_{\text{csp}n}$ determines the shift of coefficient $\beta_{\text{cor}n}$ for $V_D > V_{\text{P}n}$. The function hyperbolic tangent ensures the smooth transition with the slope determined by parameter $c_{\text{sl}n}$. Each of these parameters is calculated for each spiral segment and is used as an argument for Verilog-A spiral capacitance instance. The calculated parameters are summarized in Table 4.5.

The electrostatic potential distribution simulated in TCAD is depicted in Figs. 4.11 and 4.12. The cuts in polysilicon and in silicon under the surface based on TCAD simulation is shown in Fig. 4.13. The approximated distribution of the voltage between polysilicon and silicon is depicted in Fig. 4.14.

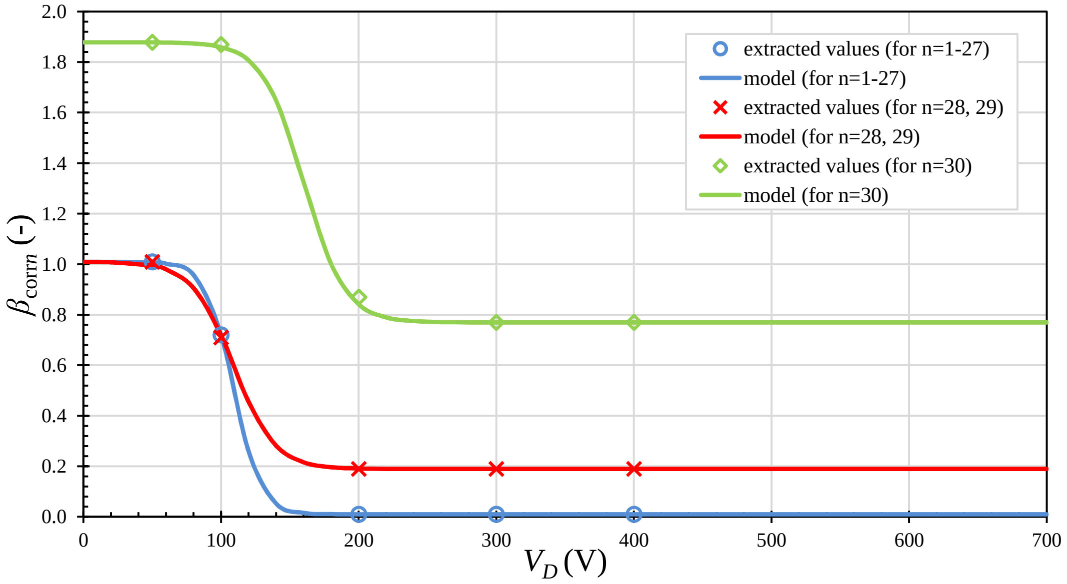
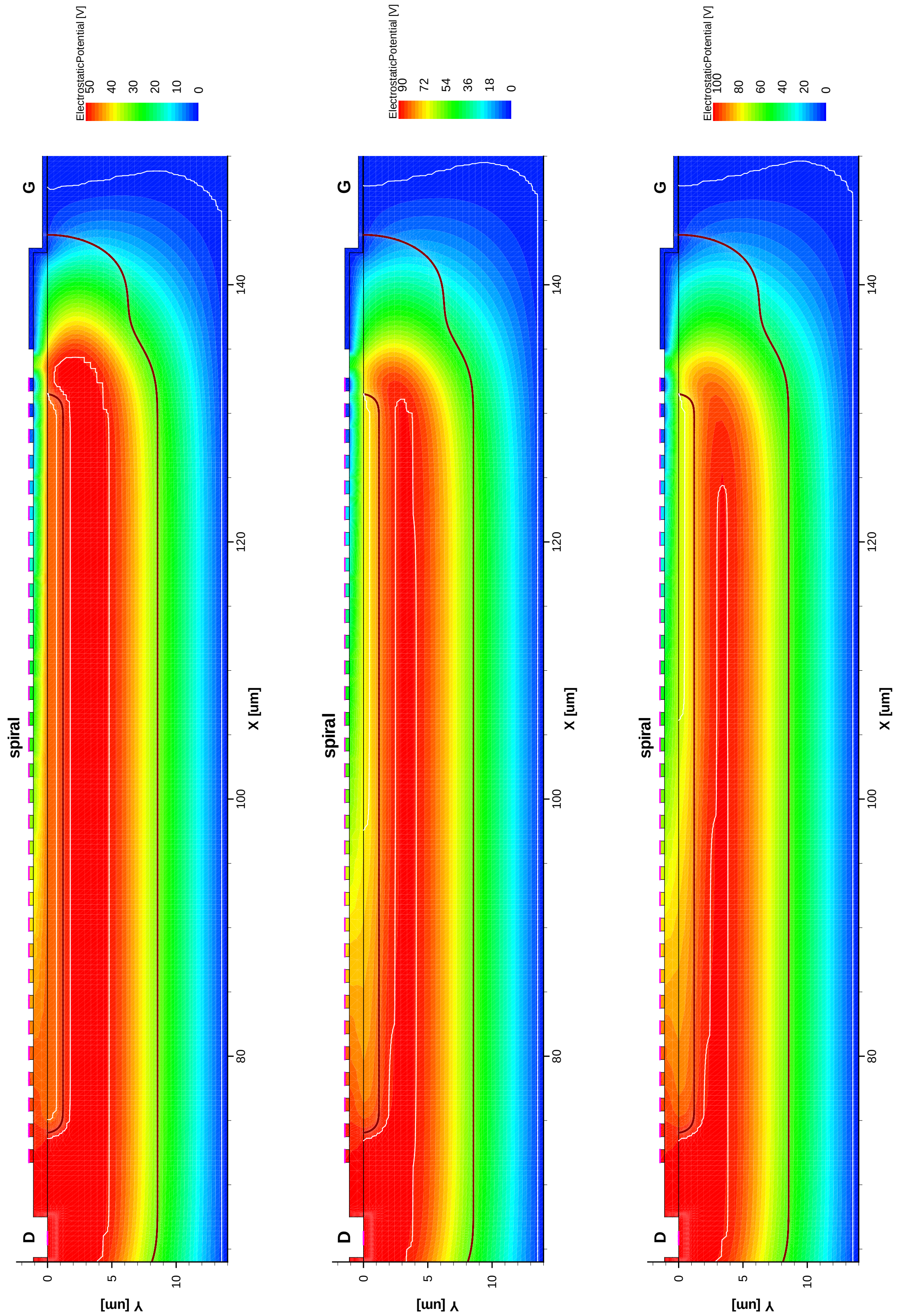


Figure 4.10. Voltage dependency correction coefficient $\beta_{\text{cor}n}$.

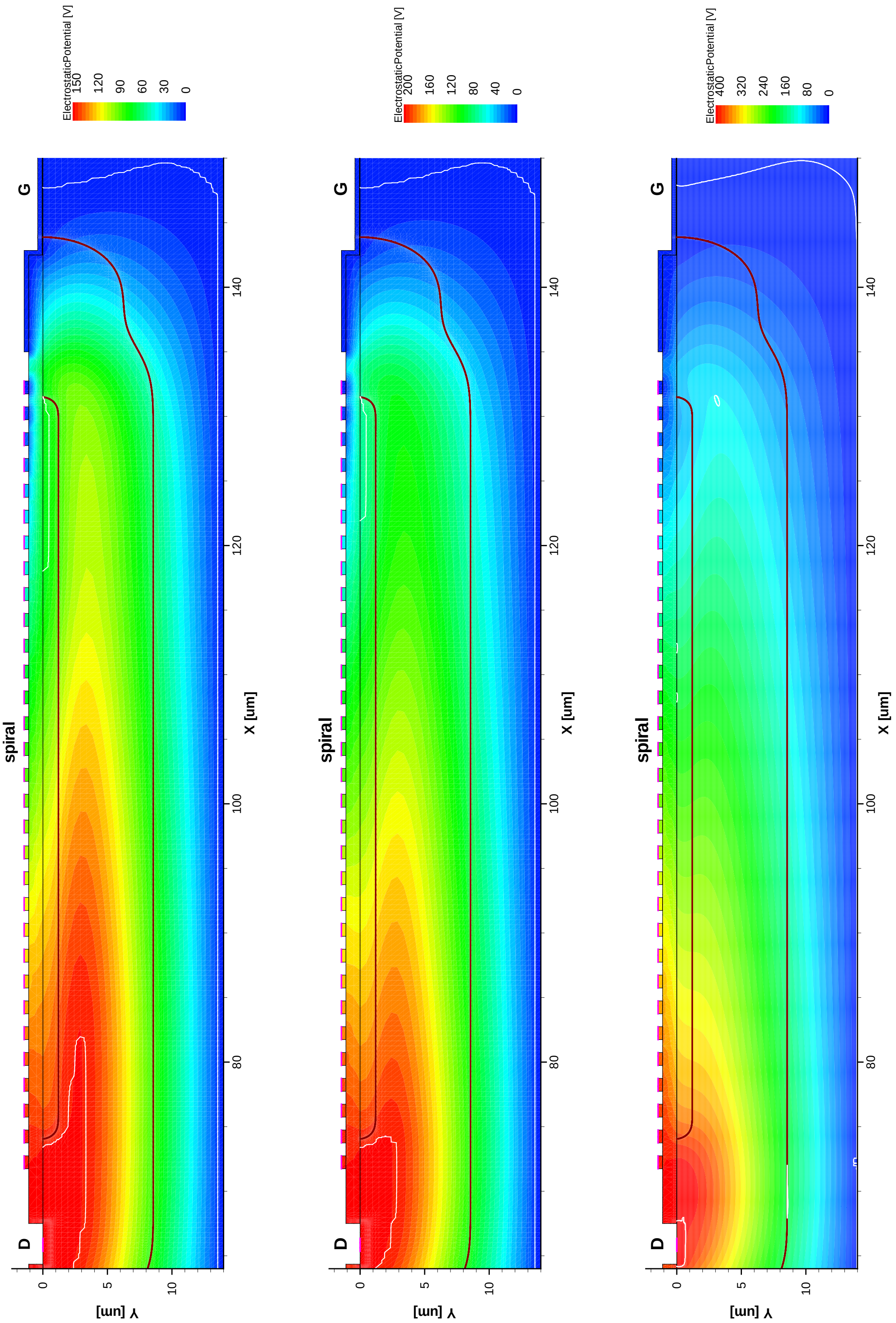
index n	$c_{\text{sp}n}$ [-]	$\Delta_{\text{csp}n}$ [-]	$V_{\text{P}n}$ [V]	$c_{\text{sl}n}$ [V^{-1}]
1-27	1	-0.9998	109	20
28-29	1	-0.82	109	30
30	1.869	-1.109	160	30
31 (sense)	10	0	160	30

Table 4.5. Extracted spiral capacitance model parameters.



a) b) c)

Figure 4.11. TCAD simulation of electrostatic potential (zoomed to interested area) for a) $V_D = 50$ V, b) $V_D = 90$ V and c) $V_D = 100$ V. Each figure has different contour range. The depletion region is indicated by white line.



a) b) c)

Figure 4.12. TCAD simulation of electrostatic potential (zoomed to interested area) for a) V_D = 150 V, b) V_D = 200 V and c) V_D = 400 V. Each figure has different contour range. The depletion region is indicated by white line.

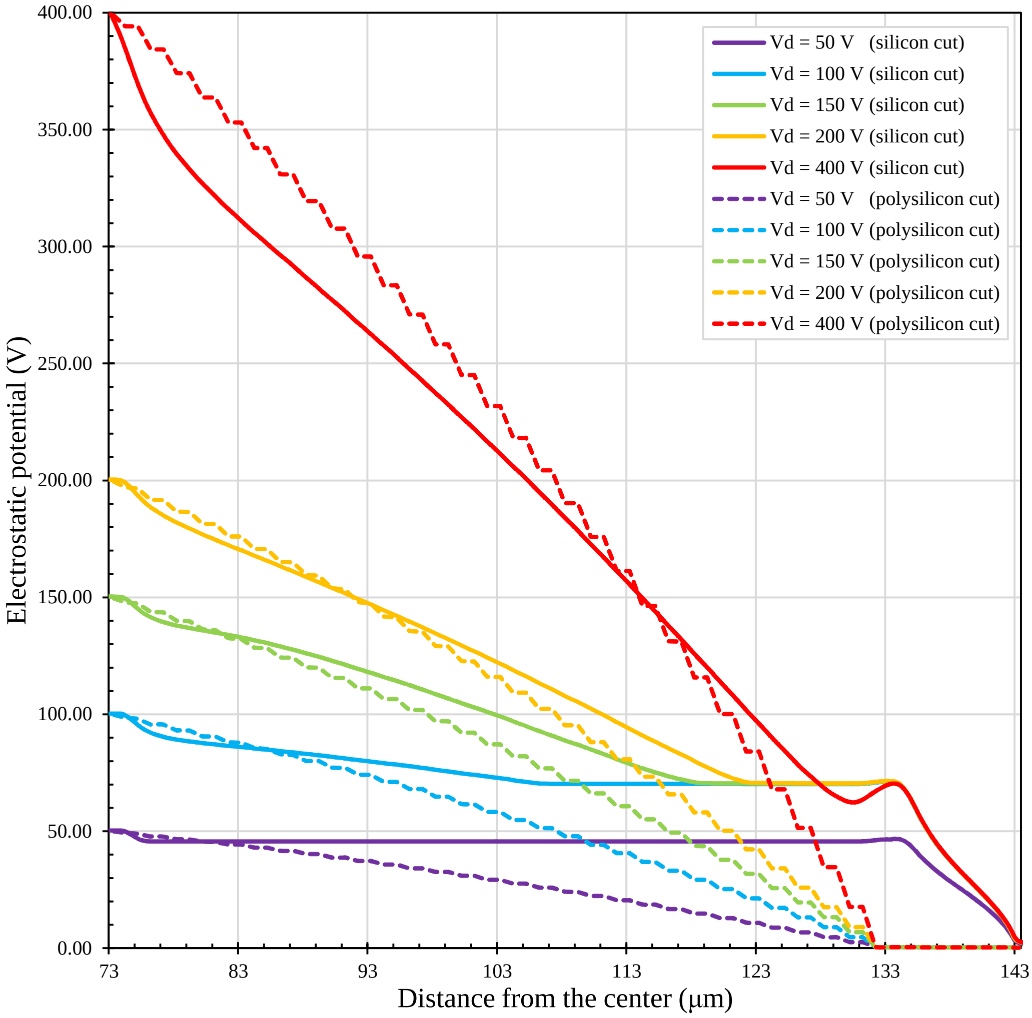


Figure 4.13. Electrostatic potential distribution in polysilicon and in silicon under the surface. Discrete levels are caused by 1 µm polysilicon width.

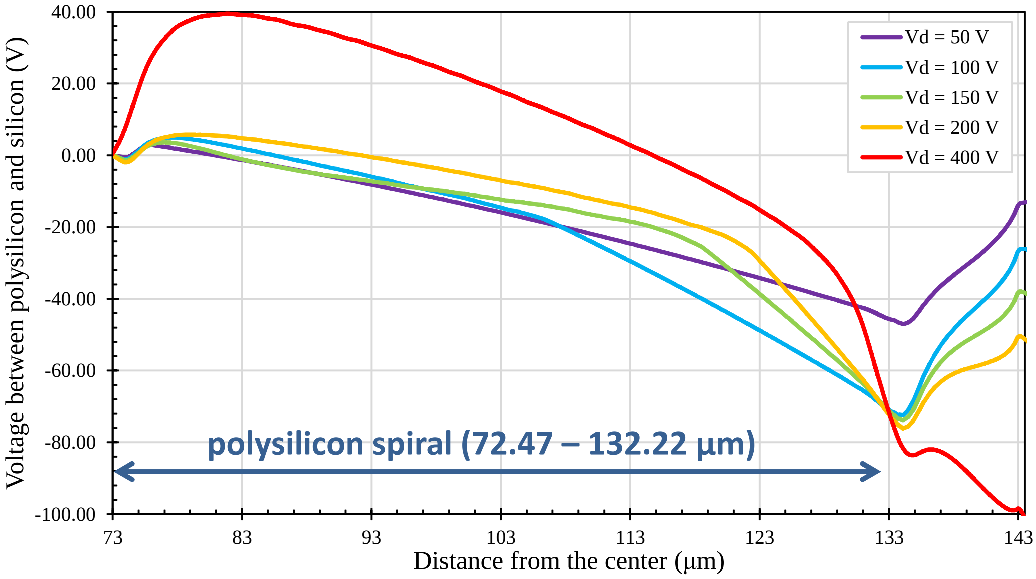


Figure 4.14. Voltage between polysilicon and silicon (approximated).

4.3.3 Additional capacitance between taps

The additional capacitance between pins tap1 and tap2 is modeled as two capacitors in series. The equation is similar to (48) but parameters has different units:

$$C_{\mathrm{tapA}} = C_{\mathrm{CtapA}} + \frac{\Delta_{\mathrm{ctapA}}}{2}\left(1 + \tanh \frac{V_D - V_{\mathrm{PtapA}}}{c_{\mathrm{sltapA}}}\right) \tag{49}$$

$$C_{\mathrm{tapB}} = C_{\mathrm{CtapB}} + \frac{\Delta_{\mathrm{ctapB}}}{2}\left(1 + \tanh \frac{V_D - V_{\mathrm{PtapB}}}{c_{\mathrm{sltapB}}}\right) \tag{50}$$

where C_{CtapA}, C_{CtapB}, Δ_{ctapA}, Δ_{ctapB}, V_{PtapA}, V_{PtapB}, c_{sltapA}, c_{sltapB} are voltage dependent capacitance model fitting parameters. The parameters C_{CtapA}, C_{CtapB} determines the value of capacitance for $V_D \le V_{\mathrm{PtapA}}$, $V_D \le V_{\mathrm{PtapB}}$, respectively. The parameters Δ_{ctapA}, Δ_{ctapB} determines the shift of capacitance value for $V_D > V_{\mathrm{PtapA}}$, $V_D > V_{\mathrm{PtapB}}$, respectively. The function hyperbolic tangent ensures the smooth transition with the slope determined by parameters c_{sltapA} and c_{sltapB}. The calculated parameters are summarized in Table 4.6.

Parameter	Value	Unit
C_{CtapA}	2.63×10^{-15}	F
C_{CtapB}	1×10^{-20}	F
Δ_{ctapA}	1.0×10^{-9}	F
Δ_{ctapB}	3.8×10^{-12}	F
V_{PtapA}	230	V
V_{PtapB}	150	V
c_{sltapA}	25.93	V^{-1}
c_{sltapB}	200	V^{-1}

Table 4.6. Extracted tap capacitance model parameters.

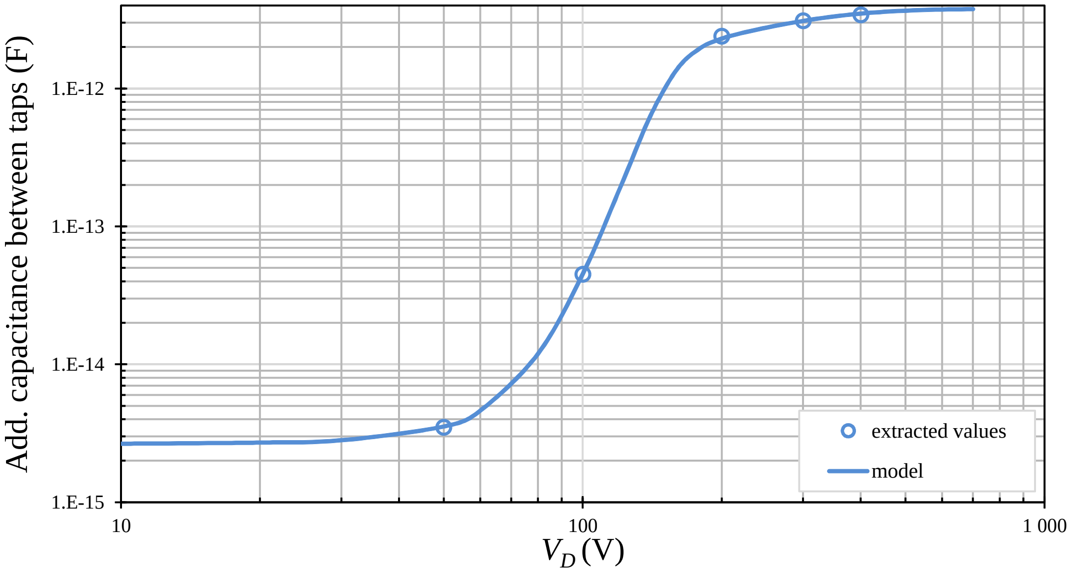


Figure 4.15. Additional capacitance between pins tap1 and tap2. Both axes are in logarithmic scale.

4.3.4 Turn-to-turn polysilicon capacitance

The turn-to-turn polysilicon-polysilicon capacitance is modeled as a capacitor connected between spiral segments. The capacitance of two parallel plates is defined as

$$C = \epsilon_r \, \epsilon_0 \frac{wl}{d} \tag{51}$$

where w, l are the capacitor width and length, d is a distance between capacitor plates, ϵ_r is a relative permittivity of the field oxide (3.9) and ϵ_0 is the permittivity of vacuum (8.854×10^{-12} F/m). The capacitors width w is given by the thickness t_{poly} of the polysilicon and the length l corresponds to the length of the spiral turn $L_{\text{seg}n}$. The distance d between the capacitor plates is defined by the gap between the spiral elements which is defined by the radius increment Δr of the spiral in one turn decreased by the width of the polysilicon spiral W_{poly}. This yields to the following expression

$$C_{\text{PolyToPoly}n} = \epsilon_r \epsilon_0 \, \frac{t_{\text{poly}} \, \beta_{fit}}{\Delta r - (W_{\text{poly}} + \delta_W)} L_{\text{seg}n} \tag{52}$$

where β_{fit} is the model fitting correction coefficient.

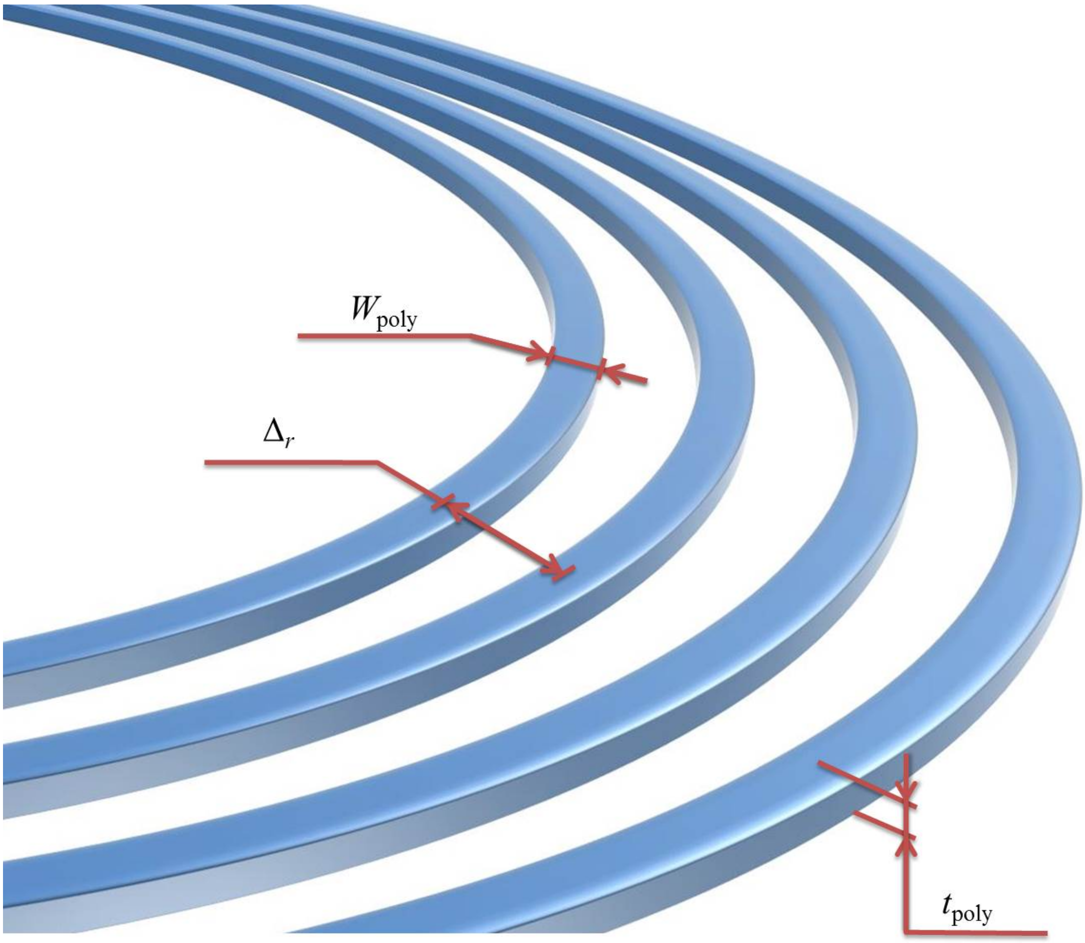


Figure 4.16. Turn-to-turn polysilicon capacitance parameters.

4.3.5 Ptop resistance

The ptop resistance between two spiral elements is modeled as a resistor with an annulus shape (for simplification). The resistivity of a rectangular resistor is defined as

$$R_{\mathrm{ptop}n} = R_{\mathrm{SHptop}} \frac{L_{\mathrm{ptop}n}}{W_{\mathrm{ptop}n}} \tag{53}$$

where $W_{\mathrm{ptop}n}$ and $L_{\mathrm{ptop}n}$ are the width and length of the resistor, n is the spiral segment order, and R_{SHptop} is a ptop sheet resistance. For the purpose of the annulus resistance calculation, which has inner radius r_1 and outer radius r_2 (see Fig. 4.17), the annulus is divided into the elements of the length dr and the width $2\pi r$. This elements are connected in series. The resistance of one element is

$$\mathrm{d}R_{\mathrm{ptop}n} = R_{\mathrm{SHptop}} \frac{\mathrm{d}r}{2\pi r} \tag{54}$$

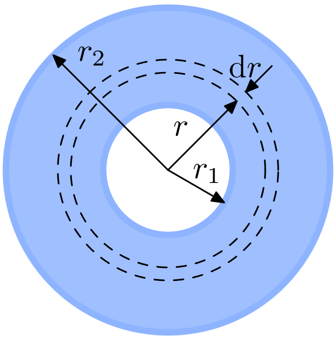


Figure 4.17. Calculation of annulus resistance.

Therefore, based on such an approximation, the total resistance of the annulus ptop resistor can be calculated as

$$R_{\mathrm{ptop}n} = \int_{r_1}^{r_2} R_{\mathrm{SHptop}} \frac{\mathrm{d}r}{2\pi r} \tag{55}$$

and solving this integral yields to

$$R_{\mathrm{ptop}n} = \frac{R_{\mathrm{SHptop}}}{2\pi} \ln \frac{r_2}{r_1} \tag{56}$$

The additional resistor is placed between ptop and pin drain. This resistor is voltage dependent and is calculated as

$$R_{\mathrm{dd}} = R_{\mathrm{ddLow}} + \frac{\Delta_{\mathrm{Rdd}}}{2} \left(1 + \tanh \frac{V_D - V_{\mathrm{Pdd}}}{r_{\mathrm{sl}}} \right) \tag{57}$$

where R_{ddLow}, Δ_{Rdd}, V_{Pdd}, and r_{sl} are voltage dependent resistance model fitting parameters. The parameter R_{ddLow} determines the value of R_{dd} for $V_D \leq V_{\mathrm{Pdd}}$, while the parameter Δ_{Rdd} determines the shift of resistance R_{dd} for $V_D > V_{\mathrm{Pdd}}$. The function hyperbolic tangent ensures the smooth transition with the slope determined by parameter r_{sl}. The calculated parameters are summarized in Table 4.7 and voltage dependency of resistor R_{dd} is depicted in Fig. 4.18

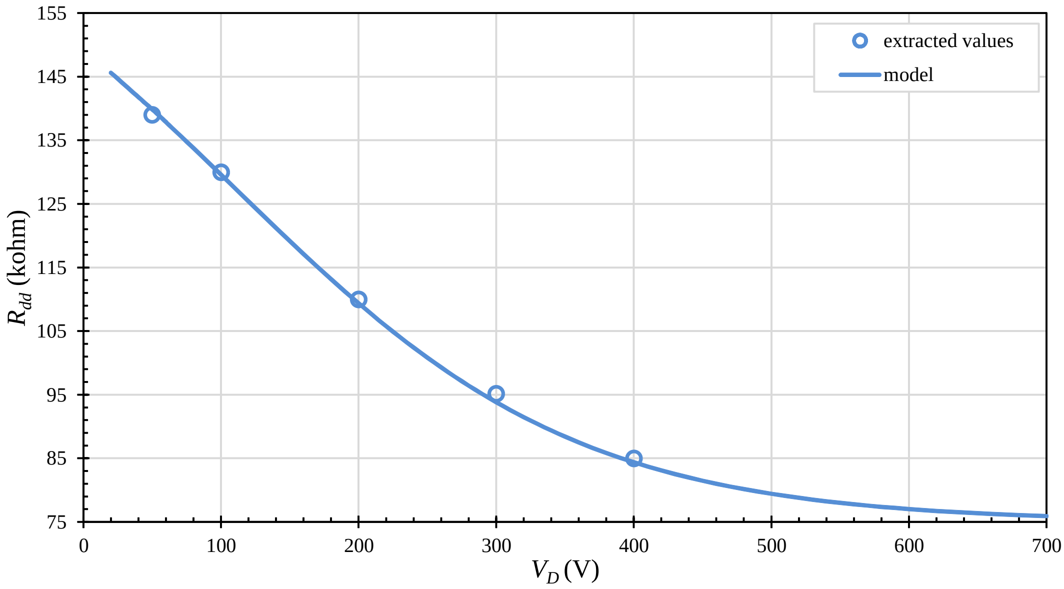


Figure 4.18. Voltage dependent resistor R_{dd}.

Parameter	Value	Unit
R_{ddLow}	180	kΩ
Δ_{Rdd}	−105	kΩ
V_{Pdd}	110	V
r_{sl}	250	V^{-1}

Table 4.7. Extracted R_{dd} resistance model parameters.

4.4 Chapter Summary

In this chapter the proposed and implemented DC and AC model of the nonlinear spiral high voltage polysilicon divider was described (the structure of a proposed macro models, implemented voltage, frequency and temperature dependency, developed equations, and physical explanation). The comparison of measured data vs. simulation is presented in order to confirm the model validity.

Chapter 5
Divider Statistical Modeling

Another fundamental thesis aim was to develop a model that is responsive to the statistical process variation. This developed model and also mismatch modeling are described in this thesis. The HV start-up MOSFET described in Chapters 3 and 4 was placed on process control monitoring test chip where this device is measured on each fabricated wafer in a standard production. Data from this test chip are used for statistical process control and also for statistical modeling.

5.1 Mismatch Variation Modeling

The mismatch modeling [34], [35] is implemented only to the divider ratio. The parameter δ_{ratio} is relative statistical mismatch model parameter and is defined as

$$\delta_{\text{ratio}} = 1 + \sigma_{\text{ratio}} \cdot \text{VAR}_{\text{MATCH\_RATIO}} \tag{58}$$

where σ_{ratio} is relative standard deviation of the divider ratio and $\text{VAR}_{\text{MATCH\_RATIO}}$ is random variable of mean 0 and standard deviation 1 that represents the normalized Gaussian distribution for modeling the stochastic variations. The histogram of measured and simulated voltage V_{tap2} and box plot are depicted in Figs. 5.1 and 5.2 (one lot typically contains from 20 to 30 wafers and one wafer typically contains 5 test chips). The number of measured devices was 3825. The standard deviation σ_{ratio} is equal to the standard deviation of measured electrical parameter V_{tap2} at $V_D = 100\,\text{V}$, $V_S = V_G = V_{\text{tap1}} = 0\,\text{V}$.

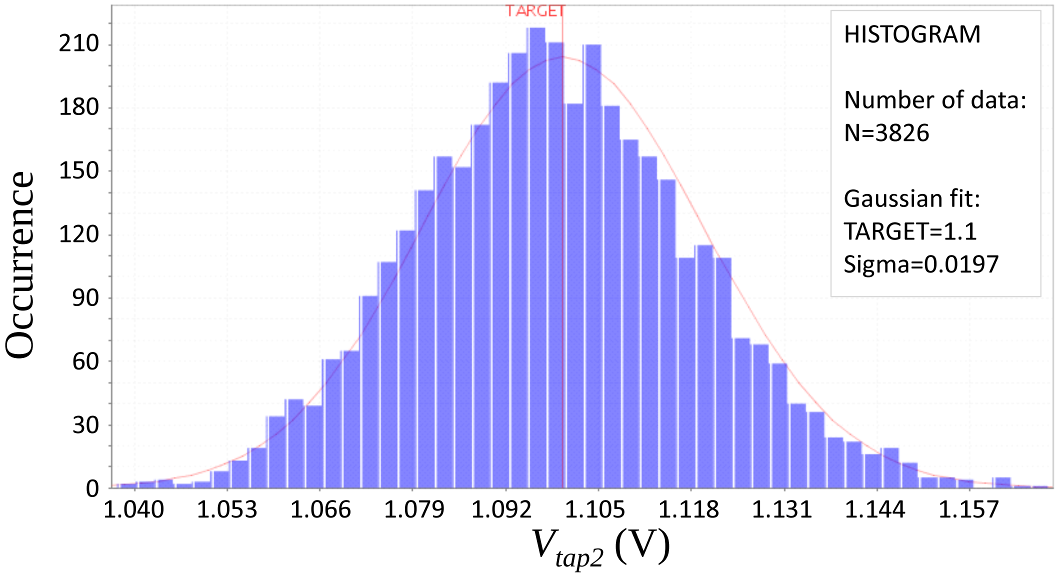


Figure 5.1. The histogram of measured and simulated electrical parameter V_{tap2}. The red curve represents modeled Gaussian distribution.

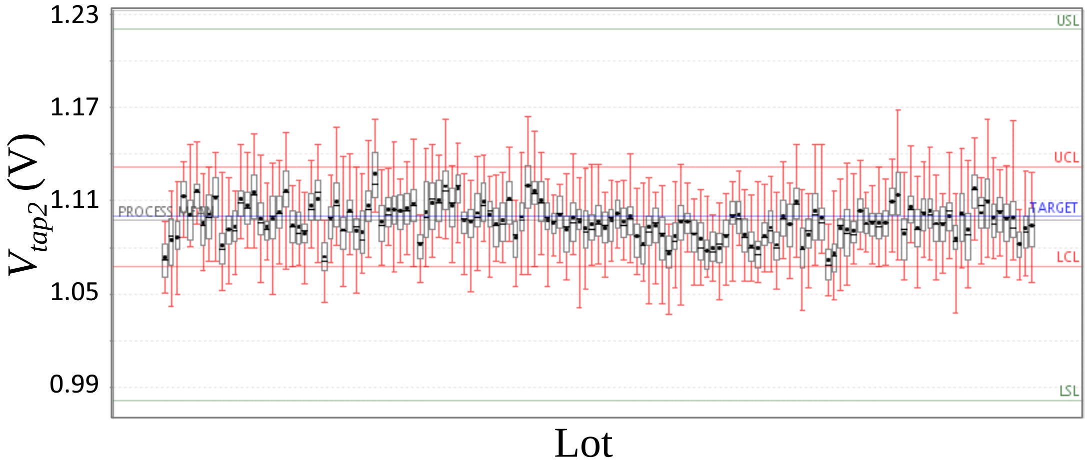


Figure 5.2. The boxplot of measured electrical parameter V_{tap2}. The green lines define upper and lower specification limit (USL and LSL) while the red lines define upper and lower control limit (UCL and LCL).

5.2 Process Variation Modeling

The influence of process parameters variation on the device parameters is implemented through master variables by using mapping equations:

$$R_{\text{SHpoly}} = R_{\text{SHpoly\_nominal}} + \sigma_{\text{RSHpoly}} \cdot \text{VAR}_{\text{RSHpoly}} \tag{59}$$

$$\delta_W = \delta_{\text{W\_nominal}} + \sigma_{\text{DW}} \cdot \text{VAR}_{\text{DW}} \tag{60}$$

$$C_{\text{PPpfld}} = C_{\text{PPpfld\_nominal}} + \sigma_{\text{PPpfld}} \cdot \text{VAR}_{\text{PPpfld}} \tag{61}$$

where $R_{\text{SHpoly\_nominal}}$, $\delta_{\text{W\_nominal}}$, and $C_{\text{PPpfld\_nominal}}$ are nominal values, σ_{RSHpoly}, σ_{DW} and σ_{PPpfld} are the standard deviations, and $\text{VAR}_{\text{RSHpoly}}$, VAR_{DW} and $\text{VAR}_{\text{PPpfld}}$ are master random variables of mean 0 and standard deviation 1 that represents the normalized Gaussian distribution for modeling the stochastic variations.

As an example, the histograms of measured and simulated electrical process parameter DW and RS_RHP are depicted in Fig. 5.4 and Fig. 5.6 respectively, and the box plots in Fig. 5.5 and Fig. 5.7 respectively. The number of measured devices was 29257. The standard deviations of device parameters σ_{RSHpoly}, σ_{DW} and σ_{PPpfld} can be calculated from the standard deviations of these measured electrical process parameters by using forward and backward propagation of variances [36].

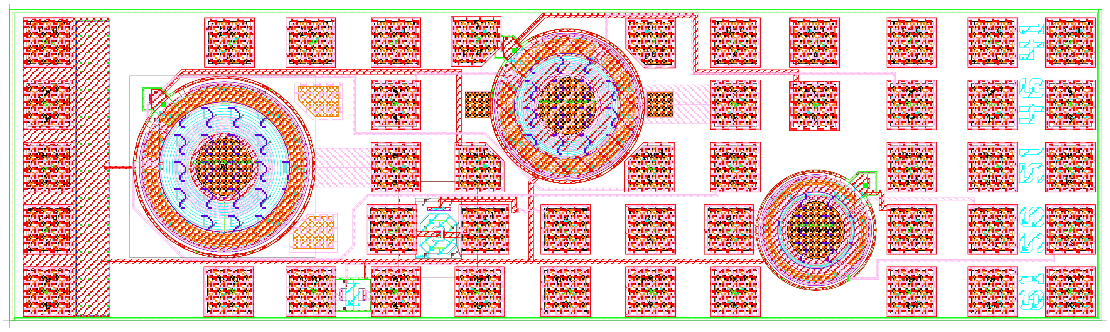


Figure 5.3. Layout of HV MOSFET (in black square) placed on the SGPCM test chip.

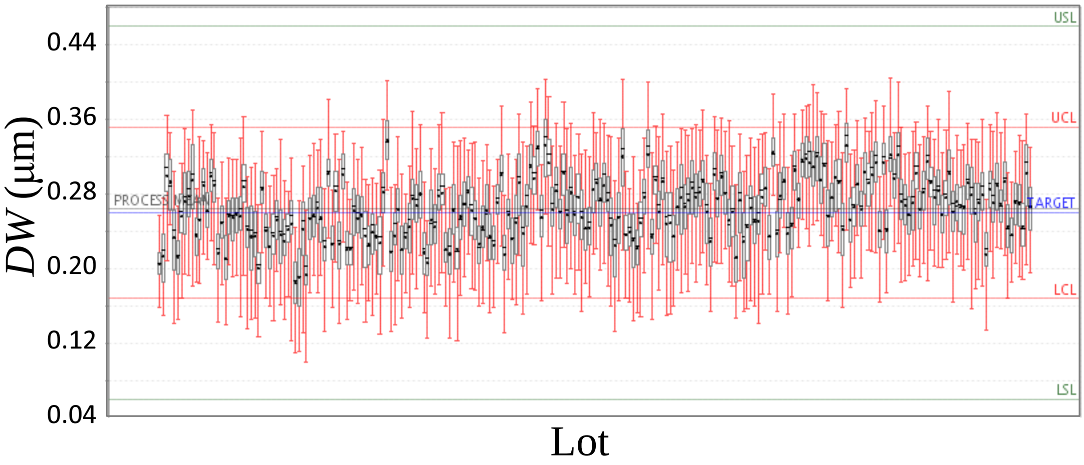


Figure 5.5. The boxplot of measured electrical process parameter DW. The green lines define upper and lower specification limit (USL and LSL) while the red lines define upper and lower control limit (UCL and LCL).

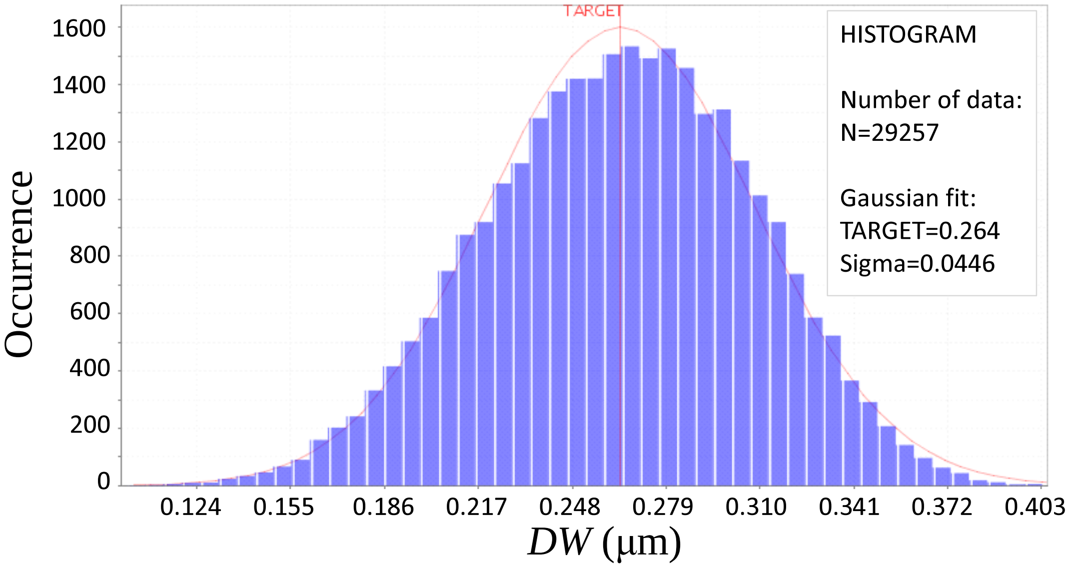


Figure 5.4. The histogram of measured and simulated electrical process parameter DW. The red curve represents modeled Gaussian distribution.

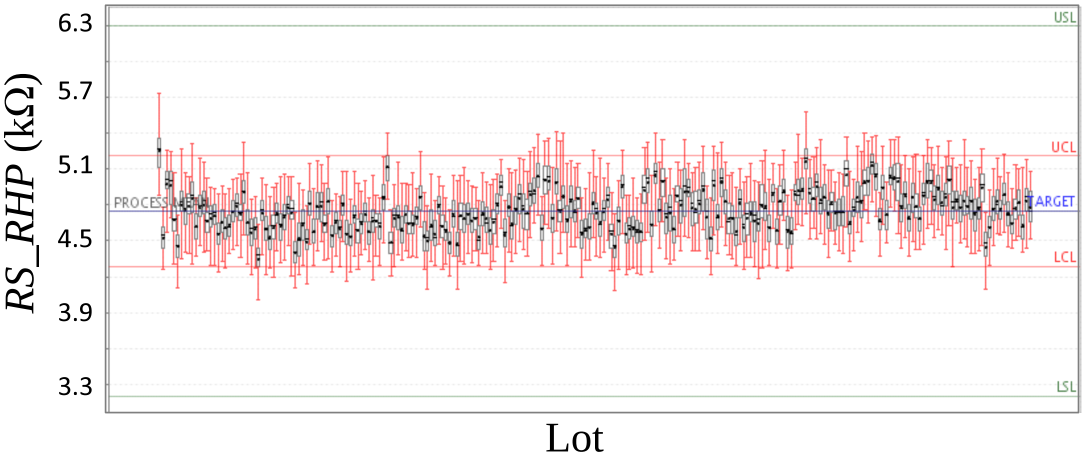


Figure 5.7. The boxplot of measured electrical process parameter RS_RHP. The green lines define upper and lower specification limit (USL and LSL) while the red lines define upper and lower control limit (UCL and LCL).

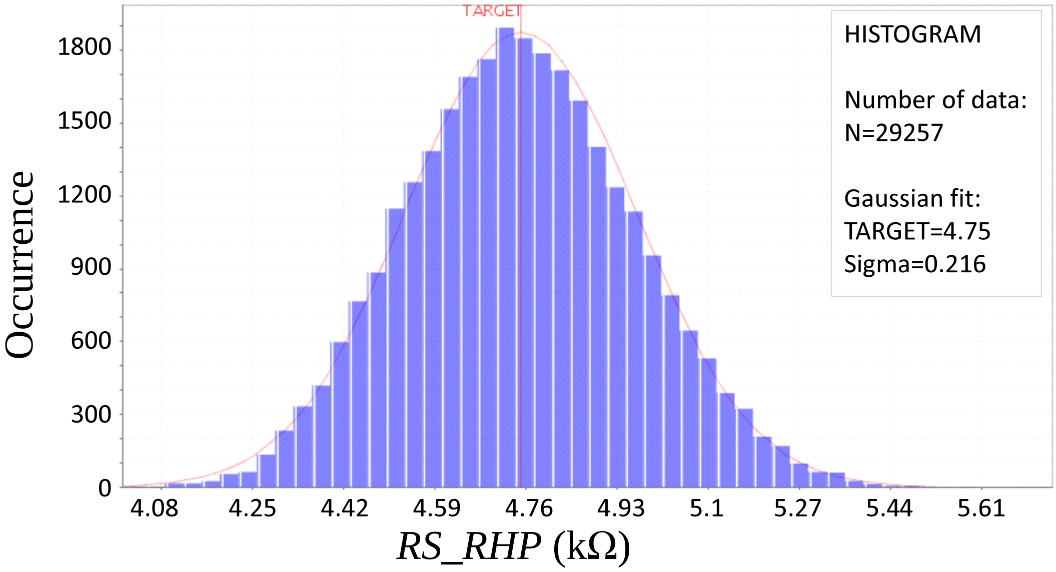


Figure 5.6. The histogram of measured and simulated electrical process parameter RS_RHP. The red curve represents modeled Gaussian distribution.

Chapter 6
Conclusion

The first fundamental thesis aim was proposing new models of the MOSFET and LDMOS drain and source leakage that are dependent on the gate dimensions, and implementing them into the commercial simulators. The second fundamental thesis aim was extracting, developing and implementing new model of the nonlinear high voltage spiral polysilicon divider in HV start-up MOSFET. Last but not least thesis aim was evaluating statistical data and making new HV divider model responsive to the statistical process variation.

The gate dependent source and drain leakage modeling has been proposed by adding several parasitic BJTs that are modeled by standard Gummel-Poon models without additional optimization of $I_{\mathrm{D}}V_{\mathrm{G}}$ characteristics. These BJTs were added without the necessity of adding new circuit node. The verification realized on several real designs did not show any significant impact on the simulation speed. The typical increase of the simulation time was in the order of several percent.

The splitting of the scaling equations to the area, perimeter and constant segments makes the higher geometry accuracy than the using a conventional area factor scaling. The parasitic BJTs are not active when MOSFET operates in the standard regime in ON state and take part only in drain and source leakage in OFF state or in non-standard operation where drain-bulk or source-bulk junction is in forward regime. All the equations used in Chapter 2 were semiempirically derived from measured data.

The proposed solution is applicable not only to the BSIM models mentioned in this thesis, but to all compact models, where the drain-bulk and source-bulk junctions are modeled by diode equations (e.g. PSP [37–39], HiSIM [40–42], HiSIM HV [43–44]). The necessary precondition is the suppression of appropriate MOSFET model parameters, namely the drain-bulk and source-bulk parasitic diode parameters.

The proposed models from Chapter 2 were published in a paper in the impacted journal Solid-State Electronics [45]. The methods for electrical characterization of MOS-based devices were also published in a paper in the impacted journal Solid-State Electronics [20]. Using artificial neural network was tested and published in a paper [46] but finally physical based models described in this thesis were selected.

The enhanced accurate DC and RF model of nonlinear spiral polysilicon voltage divider in high voltage start-up MOSFET transistor has been created and is presented in this thesis. The modeling results are compared with measured data and the maximal relative model error of divider ratio is less then 1.1 %. The intrinsic MOSFET is modeled by the standard BSIM3v3 model described in [12–13, 15, 47].

The created model is very accurate in the large operation area (V_D up to 400 V, frequencies up to 10 MHz, at temperatures from −40 to 150 °C). The big advantage of this model are smooth derivatives of simulated characteristics which is generally important in computer-aided design (the smooth derivatives are necessary for numerical methods). Very often the hyperbolic function tanh was used to ensure the smooth transition between two parameters values. This hyperbolic function also enables to define the slope of the transition as a model parameter. The simulation speed is acceptable and any convergency issue was not observed during the verification realized on several real designs.

A special attention is paid to the ability of the created model to cover the influence of a variation of process parameters on the device characteristics. The statistical process variation model is created based on measurement about 30000 devices and mismatch model is based on measurement about 3000 devices. It has to be pointed out that Monte Carlo simulations represent the most powerful tool to verify the robustness of a designed circuit over natural process and mismatch variations.

First, a simpler way of the proposed divider ratio modeling was published in a paper in the [32] but without ratio scalability, temperature and statistical modeling. This three important model abilities were developed and implemented into the enhanced model that was published in a paper in the impacted journal Radioengineering [33].

All the created models (leakage modeling and HV divider) were implemented into the commercial simulators (Eldo, Spectre, HSpice) and can be used in circuits from various areas of electrical engineering, such as analog, digital, signal processing or RF circuits.

References

[1] Kim, N.S., T. Austin, D. Baauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan. Leakage current: Moore's law meets static power. *Computer*. Dec, 2003, Vol. 36, No. 12, pp. 68-75. ISSN 0018-9162.
Available from DOI 10.1109/MC.2003.1250885.

[2] Elgharbawy, W.M., and M.A. Bayoumi. Leakage sources and possible solutions in nanometer CMOS technologies. *IEEE Circuits and Systems Magazine*. Fourth, 2005, Vol. 5, No. 4, pp. 6-17. ISSN 1531-636X.
Available from DOI 10.1109/MCAS.2005.1550165.

[3] Bailey, B.. Power 104: Reducing power consumption. *EE Times*. 2012.
`http://www.eetimes.com/author.asp?section_id=36&doc_id=1286045`.

[4] Santos, Rodolfo P., Gabriela S. Clemente, A. Silva-Filho, C. Araujo, A. Sarmento, M. Lima, and E. Barros. An Optimization Mechanism Intended for Static Power Reduction Using Dual-Vth Technique. *Journal of Electrical and Computer Engineering*. 2012, Vol. 2012, pp. 1-12. ISSN 2090-0147.
Available from DOI 10.1155/2012/561580.

[5] Kim, Kyung Ki, and Yong-Bin Kim. A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. April, 2009, Vol. 17, No. 4, pp. 517-528. ISSN 1063-8210.
Available from DOI 10.1109/TVLSI.2008.2007958.

[6] Rowe, A., K. Lakshmanan, Haifeng Zhu, and R. Rajkumar. Rate-Harmonized Scheduling and Its Applicability to Energy Management. *IEEE Transactions on Industrial Informatics*. Aug, 2010, Vol. 6, No. 3, pp. 265-275. ISSN 1551-3203.
Available from DOI 10.1109/TII.2010.2052106.

[7] Unni, Bhavyasree, Nazia Parveen, Ankit Kumar, and B.S. Bindhumadhava. An intelligent energy optimization approach for MPI based applications in HPC systems. *CSI Transactions on ICT*. Springer-Verlag, 2013, Vol. 1, No. 2, pp. 175-181. ISSN 2277-9078.
Available from DOI 10.1007/s40012-013-0012-6.

[8] Chen, Yi-Jung, Chia-Lin Yang, Jaw-Wei Chi, and Jian-Jia Chen. TACLC: Timing-Aware Cache Leakage Control for Hard Real-Time Systems. *IEEE Transactions on Computers*. June, 2011, Vol. 60, No. 6, pp. 767-782. ISSN 0018-9340.
Available from DOI 10.1109/TC.2011.44.

[9] Xu, C.Q., C.J. Xue, and E.H.-M. Sha. Energy-Efficient Joint Scheduling and Application-Specific Interconnection Design. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*. Oct, 2011, Vol. 19, No. 10, pp. 1813-1822. ISSN 1063-8210.
Available from DOI 10.1109/TVLSI.2010.2062544.

[10] Banimelhem, O., and R. Bani Hani. Neural network based optimization of CMOS transistor sizing for leakage power minimization. In: *2012 International Conference*

on Innovations in Information Technology (IIT). 2012. pp. 167-172. ISBN 978-1-4673-1100-7.
Available from DOI 10.1109/INNOVATIONS.2012.6207724.

[11] Wilson, R., and D. Lammers. Grove Calls Leakage Chip Designers' Top Problem. *EE Times.* 2002.
`www.eetimes.com/story/OEG20021213S0040`.

[12] Liu, W. *MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4*. Wiley-IEEE Press, 2001. ISBN 978-0-471-39697-0.

[13] Ytterdal, T., Y. Cheng, and T.A. Fjeldly. *Device modeling for analog and RF CMOS circuit design*. Wiley, 2003. ISBN 9780471498698.

[14] Gildenblat, G.. *Compact Modeling: Principles, Techniques and Applications*. Springer, 2010. ISBN 9789048186136.

[15] Massobrio, G., and P. Antognetti. *Semiconductor device modeling With SPICE*. New York: McGraw-Hill, 1993. ISBN 9780070024694.

[16] Takakubo, K., T. Eto, and H. Takakubo. Analysis and Modeling of Leakage Current for Four-Terminal MOSFET in Off-State and Low Leakage Switches. *IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences.* 2009, Vol. 92, pp. 421-429. ISSN 0916-8508.
Available from DOI 10.1587/transfun.E92.A.421.

[17] Vladimirescu, A.. *The SPICE book*. New York: John Wiley & Sons, 1994. ISBN 9780471609261.

[18] Sischka, F.. *Gummel Poon Bipolar model.*

[19] McAndrew, C.C., J. Bates, R.T. Ida, and P. Drennan. Efficient statistical BJT modeling, why beta is more than Ic/Ib. In: *Proc of the Bipolar/BiCMOS Circuits and Technology Meeting.* 1997. pp. 28-31. ISSN 1088-9299.
Available from DOI 10.1109/BIPOL.1997.647349.

[20] Dobeš, J., J. Míchal, V. Paňko, and L Pospíšil. Reliable procedure for electrical characterization of MOS-based devices. *Solid-State Electronics.* 2010, Vol. 54, No. 10, pp. 1173-1184. ISSN 0038-1101.
Available from DOI 10.1016/j.sse.2010.05.034.

[21] MacSweeney, D., K.G. McCarthy, A. Mathewson, and B. Mason. A SPICE compatible subcircuit model for lateral bipolar transistors in a CMOS process. *IEEE Transactions on Electron Devices*. sep, 1998, Vol. 45, No. 9, pp. 1978-1984. ISSN 0018-9383.
Available from DOI 10.1109/16.711364.

[22] Cao, K.M., W.-C. Lee, W. Liu, X. Jin, P. Su, S.K.H. Fung, J.X. An, B. Yu, and C. Hu. BSIM4 gate leakage model including source-drain partition. In: *International Electron Devices Meeting, Technical Digest.* 2000. pp. 815-818. ISBN 0-7803-6438-4.
Available from DOI 10.1109/IEDM.2000.904442.

[23] Gehring, A., and S. Selberherr. Gate leakage models for device simulation. In: *Proc 7th International Conference on Solid-State and Integrated Circuits Technology.* 2004. pp. 971-976. ISBN 0-7803-8511-X.
Available from DOI 10.1109/ICSICT.2004.1436668.

[24] Hu, Jayson, Xuemei Xi, Ali Niknejad, and Chenming Hu. On gate leakage current partition for MOSFET compact model. *Solid-State Electronics.* 2006, Vol. 50,

No. 11-12, pp. 1740-1743. ISSN 0038-1101.
Available from DOI 10.1016/j.sse.2006.09.016.

[25] Rao, R.M., J.L. Burns, A. Devgan, and R.B. Brown. Efficient techniques for gate leakage estimation. In: *Proc of the 2003 International Symposium on Low Power Electronics and Design.* 2003. pp. 100-103. ISBN 1-58113-682-X.
Available from DOI 10.1109/LPE.2003.1231843.

[26] Hall, J, M. T. Quddus, R. Burton, K. Oikawa, and G. Chang. *High voltage sensor device and method therefor*. US Patent, 7955943.

[27] Hall, J., and M. T. Quddus. *Method of sensing a high voltage*. US Patent, 8349625.

[28] ON Semiconductor. *Fixed Frequency Current Mode Controller for Flyback Converters*. Data Sheet NCP1237/D.

[29] ON Semiconductor. *Design of a 65 W Adapter Utilizing the NCP1237 PWM Controller*. Application note AND8461/D.

[30] ON Semiconductor. *32 W, 32 V Universal Input AC-DC Printer Adapter using the NCP1237*. Application note AND8454/D.

[31] ON Semiconductor. *Designing Converters with the NCP101X Family*. Application note AND8134/D.

[32] Panko, V., S. Banas, K. Ptacek, R. Burton, and J. Dobes. An accurate DC and RF modeling of nonlinear spiral polysilicon voltage divider in high voltage MOSFET transistor. In: *Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on.* 2012. pp. 538-540. ISBN 978-1-4673-2474-8.
Available from DOI 10.1109/ICSICT.2012.6467635.

[33] Panko, V., S. Banas, R. Burton, K. Ptacek, J. Divin, and J. Dobes. Enhanced Model of Nonlinear Spiral High Voltage Divider. *Radioengineering.* 2015, In print. ISSN 1210-2512.

[34] Papathanasiou, K. A.. A designer's approach to device mismatch: Theory, modeling, simulation techniques, applications and examples. *Analog Integrated Circuits and Signal Processing*. Kluwer Academic Publishers, 2006, Vol. 48, No. 2, pp. 95-106. ISSN 0925-1030.
Available from DOI 10.1007/s10470-006-5367-2.

[35] Drennan, P.G., and C.C. McAndrew. Understanding MOSFET mismatch for analog design. *IEEE Journal of Solid-State Circuits.* 2003, Vol. 38, No. 3, pp. 450-456. ISSN 0018-9200.
Available from DOI 10.1109/JSSC.2002.808305.

[36] McAndrew, C.C.. Statistical Modeling Using Backward Propagation of Variance (BPV). In: *Compact Modeling*. Springer Netherlands, 2010. pp. 491-520. ISBN 978-90-481-8613-6.
Available from DOI 10.1007/978-90-481-8614-3_16.

[37] Gildenblat, G., Xin Li, Weimin Wu, Hailing Wang, A. Jha, R. van Langevelde, G.D.J. Smit, A.J. Scholten, and D.B.M. Klaassen. PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation. *Electron Devices, IEEE Transactions on*. Sept, 2006, Vol. 53, No. 9, pp. 1979-1993. ISSN 0018-9383.
Available from DOI 10.1109/TED.2005.881006.

[38] Gildenblat, G., W. Wu, X. Li, Z. Zhu, G.D.J. Smit, A.J. Scholten, and D.B.M. Klaassen. Surface-potential-based MOSFET models with introduction to PSP

(invited). In: *Wireless and Microwave Technology Conference, 2009. WAMICON '09. IEEE 10th Annual.* 2009. pp. 1-2. ISBN 978-1-4244-4564-6.
Available from DOI 10.1109/WAMICON.2009.5207226.

[39] Li, X., W. Wu, A. Jha, G. Gildenblat, R. van Langevelde, G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen, C.C. McAndrew, J. Watts, M. Olsen, G. Coram, S. Chaudhry, and J. Victory. Benchmarking the PSP Compact Model for MOS Transistors. In: *Microelectronic Test Structures, 2007. ICMTS '07. IEEE International Conference on.* 2007. pp. 259-264. ISBN 1-4244-0781-8.
Available from DOI 10.1109/ICMTS.2007.374495.

[40] Suetake, M., K. Suematsu, H. Nagakura, M. Miura-Mattausch, H.J. Mattausch, S. Kumashiro, T. Yamaguchi, S. Odanaka, and N. Nakayama. HiSIM: a drift-diffusion-based advanced MOSFET model for circuit simulation with easy parameter extraction. In: *Simulation of Semiconductor Processes and Devices, 2000. SISPAD 2000. 2000 International Conference on.* 2000. pp. 261-264. ISBN 0-7803-6279-9.
Available from DOI 10.1109/SISPAD.2000.871258.

[41] Miura-Mattausch, M., H.J. Mattausch, and T. Ezaki. *The Physics and Modeling of MOSFETS: Surface-potential Model HiSIM*. World Scientific, 2008. International series on advances in solid state electronics and technology. ISBN 9789812568649.

[42] Mattausch, H.J., M. Miura-Mattausch, N. Sadachika, M. Miyake, and D. Navarro. The HiSIM compact model family for integrated devices containing a surface-potential MOSFET core. In: *Mixed Design of Integrated Circuits and Systems, 2008. MIXDES 2008. 15th International Conference on.* 2008. pp. 39-50. ISBN 978-83-922632-7-2.

[43] Mattausch, H.J., M. Miyake, T. Iizuka, H. Kikuchihara, and M. Miura-Mattausch. The Second-Generation of HiSIM HV Compact Models for High-Voltage MOSFETs. *Electron Devices, IEEE Transactions on*. Feb, 2013, Vol. 60, No. 2, pp. 653-661. ISSN 0018-9383.
Available from DOI 10.1109/TED.2012.2225836.

[44] Mattausch, H.J., T. Umeda, H. Kikuchihara, and M. Miura-Mattausch. The HiSIM compact models of high-voltage/power semiconductor devices for circuit simulation. In: *Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on.* 2014. pp. 1-4. ISBN 978-1-4799-3296-2.
Available from DOI 10.1109/ICSICT.2014.7021424.

[45] Paňko, V., Banáš, S, D. Prejda, and J. Dobeš. MOSFET gate dimension dependent drain and source leakage modeling by standard SPICE models. *Solid-State Electronics.* 2013, Vol. 81, No. 0, pp. 144 - 150. ISSN 0038-1101.
Available from DOI http://dx.doi.org/10.1016/j.sse.2013.01.001.

[46] Dobeš, J., L. Pospíšil, and V. Paňko. Selecting an optimal structure of artificial neural networks for characterizing RF semiconductor devices. In: *2010 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS).* 2010. pp. 1206-1209. ISSN 1548-3746.
Available from DOI 10.1109/MWSCAS.2010.5548882.

[47] Liou, J.J., A. Ortiz-Conde, and F. García-Sánchez. *Analysis and design of MOSFETs: modeling, simulation, and parameter extraction*. Kluwer Academic Publishers, 1998. ISBN 9780412146015.

List of Candidate's Works

List of Candidate's Works Relating to the Doctoral Thesis

Papers in Impacted Journals

[A1] V. Paňko, S. Banáš, R. Burton, K. Ptáček, J. Divín, J. Dobeš. Enhanced Model of Nonlinear Spiral High Voltage Divider, *Radioengineering*. Finally accepted. In print. ISSN 1210-2512. (Contribution 40 %, WoS IF=0.796)

[A2] V. Paňko, S. Banáš, D. Prejda, J. Dobeš. MOSFET gate dimension dependent drain and source leakage modeling by standard SPICE models. *Solid-State Electronics*. 2013, vol. 81, no. 3, art. no. 27, p. 144-150. ISSN 0038-1101. (Contribution 35 %, WoS IF=1.514)

[A3] J. Dobeš, J. Míchal, V. Paňko, L. Pospíšil. Reliable procedure for electrical characterization of MOS-based devices. *Solid-State Electronics*. 2010, vol. 54, no. 10, p. 1173-1184. ISSN 0038-1101. (Contribution 25 %, WoS IF=1.44)

Papers Excerpted in Web of Science

[B1] J. Dobeš, V. Paňko, S. Banáš, D. Černý. An Improved Model of High-Voltage Power LDMOSFET and Its Usage in Multi-Objective Optimization of Radio-Frequency Amplifiers. In *Proceedings of the 14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*. Piscataway: IEEE, 2013, p. 1-5. ISSN 1093-5142. ISBN 978-1-4673-4916-1. (contribution 15 %)

[B2] V. Paňko, S. Banáš, K. Ptáček, R. Burton, J. Dobeš. An Accurate DC and RF Modeling of Nonlinear Spiral Polysilicon Voltage Divider in High Voltage MOSFET Transistor. In *Proceedings of the 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology*. Piscataway: IEEE, 2012, p. 1-3. ISBN 978-1-4673-2472-4. (contribution 35 %)

[B3] J. Dobeš, L. Pospíšil, V. Paňko. Selecting an Optimal Structure of Artificial Neural Networks for Characterizing RF Semiconductor Devices. In *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems*. Piscataway: IEEE, 2010, p. 1206-1209. ISSN 1548-3746. ISBN 978-1-4244-7773-9.

[B4] J. Dobeš. V. Paňko, L. Pospíšil. An Accurate Gate-Delay Model for High Speed Digital and Analog Circuits. In *Proceedings of the 2008 IEEE Dallas Circuits And Systems Workshop*. Piscataway: IEEE, 2008, p. 37-40. ISBN 978-1-4244-2955-4. (contribution 10 %)

Papers in Reviewed Journals

[C1] S. Banáš, V. Paňko, V. Stejskal, J. Slezák, J. Dobeš. Universal behavioral model for accurate modeling of high voltage devices. *WIT Transactions on Information and Communication Technologies*. 2014, vol. 60, p. 545-551. ISSN 1743-3517.

Other Publications

[D1] J. Dobeš, V. Paňko, D. Černý, J. Divín. A Flexible Algorithm for Solving Systems of Circuit Differential-Algebraic Equations With Integrated Fortran 95 Compiler for Modeling. In *Proceedings of the IEEE AFRICON 2013*. Piscataway: IEEE, 2013, p. 1-5. ISSN 2153-0025. ISBN 978-1-4673-5943-6.

[D2] J. Dobeš, J. Míchal, V. Paňko. Multiobjective Optimization of Nonlinear Circuits. In *Proceedings of the 2012 International Conference on Scientific Computing*. Las Vegas: CSREA Press, 2012, p. 20-26. ISBN 1-60132-207-0.

[D3] J. Dobeš, V. Paňko, L. Pospíšil. Reliable Procedure for Electrical Characterization of MOS-Based Devices. In *Proceedings of the 2009 International Semiconductor Device Research Symposium*. Piscataway: IEEE, 2009, p. 1-2. ISBN 978-1-4244-6031-1.

List of Other Candidate's Works

Other Publications

[E1] J. Dobeš, J. Míchal, F. Vejražka, J. Popp, V. Paňko. Multi objective Optimization of Input Low Noise Amplifier for Common GPS/Galileo/GLONASS/Compass Satellite Navigation System Receiver. In *Proceedings of the 11th International SoC Design Conference*. New York: IEEE, 2014, art. no. HI-4, p. 88-89. ISSN 2163-9612. ISBN 978-1-4799-5126-0.

[E2] V. Paňko, J. Slezák, J. Dobeš, L. Vojkůvka. Lateral PNP Transistor Modeling with SPICE Models. In *Proceedings of the MOS-AK/ESSDERC/ESSCIRC Workshop*. Edinburgh: MOS-AK, 2008.

[E3] V. Paňko. Optimizing the SPICE Models for Lateral PNP Bipolar Junction Transistor. In *Sborník příspěvků konference IEEE Workshop Zvůle 2008*. Valtinov, Aug. 2008, p. 186-189. ISBN 978-80-214-3709-8.

Response and Reviews

Citations

Paper [A3]

J. Dobeš, J. Míchal, V. Paňko, L. Pospíšil. Reliable procedure for electrical characterization of MOS-based devices. *Solid-State Electronics*. 2010, vol. 54, no. 10, p. 1173-1184. ISSN 0038-1101.

was cited in:

[G1] S. Tebby. *Optimal Vehicle Structural Design for Weight Reduction using Iterative Finite Element Analysis*. 2012. PhD Thesis. University of Ontario Institute of Technology.

Paper [B3]

J. Dobeš, L. Pospíšil, V. Paňko. Selecting an Optimal Structure of Artificial Neural Networks for Characterizing RF Semiconductor Devices. In *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems*. Piscataway: IEEE, 2010, p. 1206-1209. ISSN 1548-3746. ISBN 978-1-4244-7773-9.

was cited in:

[G2] Z. Yang. User-Online Load Movement Forecasting for Social Network Site Based on BP Artificial Neural Network. *Journal of Computers*, 2013, vol. 8, no. 12, p. 3176-3183. ISSN 1796-203X.

[G3] HomaShahmohamadi, M. Gholami, Y. Ganjdanesh. Applying neural network for RF and electrical semiconductor to get an optimal structure. *Technical Journal of Engineering and Applied Sciences*, 2013, vol.2, p. 150-158. ISSN 2051-0853.

[G4] Zong-chang Yang. Establishing Structure for Artificial Neural Networks Based-on Fractal. *Journal of Theoretical and Applied Information Technology*, 2013, vol. 49, no. 1. ISSN 1992-8645

Appendix A

Abbreviations and Symbols

ϵ_r [-]	relative permittivity of oxide
ϵ_0 [F/m]	permittivity of vacuum (8.854×10^{-12} F/m)
aa	active area
cont	contact
D	drain
DAM	ON Semiconductor internal measurement and data management system
FOX	field oxide
G	gate
GOX	gate oxide
HR	high resistance
hrbl	high resistance blocking layer
HV	high voltage
IC-CAP	Integrated Circuit Characterization and Analysis Program, Keysight Technologies
m1	first metal
m2	second metal
nsd	N+ diffusion (mainly forming source and drain)
nw	Nwell
nwell	N- diffusion
nw1	Nwell1
nw2	Nwell2
OECD	Organisation for Economic Co-operation and Development
pass	passivation
PCM	Process control monitoring
phv	P diffusion
poly	polysilicon
psd	P+ diffusion (mainly forming source and drain)
ptop	P doped resurf diffusion
pw	pwell (P- diffusion)
pwell	P- diffusion
S	source
SUB	substrate

Appendix B
Used Equipments and Software

Equipments Used for Measurement

DC/CV Measurement Equipment - auto prober:

- Electroglas EG4090A Automatic Prober
- Thermo chuck (-40C to 150C)
- Temptronic 315A temperature controller
- HP4072 Test System
- LCR meter HP 4284A
- Multimeter HP 3458A (DVM)
- 4x Middle-power SMU, 1x High-power SMU
- switch matrix

DC/CV Measurement Equipment - manual prober:

- Manual prober Karl Suss PM8
- Thermo chuck (-40C to 200C)
- Temptronic 315A temperature controller
- HP 4156B Semiconductor Parameter Analyzer
- HP4284 LCR meter
- HP4142 Modular DC Source up to 1000V

AC Measurement Equipment - manual prober:

- Cascade Microtech Summit 9000 Manual Probe Station
- Thermo chuck (-40C to 150C)
- Temptronic 315A temperature controller
- HP 8753E Vector Network Analyzer

Used Software

- Cadence Virtuoso Layout
- Cadence Schematic Editor
- IC-CAP
- Eldo
- Spectre

Appendix C

Candidate’s Short Curriculum Vitae

PERSONAL INFORMATION

Name	Václav
Surname	Paňko
Address	Lužánky 330, 75366 Hustopeče nad Bečvou, Czech Republic
Email	vaclav.panko@onsemi.com

EDUCATION

2008–Present	**PhD Student in Radioelectronics** Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radio Engineering
2006–2008	**Master’s degree in Radioelectronics** Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radio Engineering *Thesis: Optimizing the SPICE Model for Lateral PNP Bipolar Junction Transistor*
2002–2006	**Bachelor’s degree in Electronics and Communications** Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radio Engineering *Thesis: The EKV Model Parameters Extraction of the MOS Transistor*

EXPERIENCE

2007–Present	**Senior Modeling & Characterization Engineer** ON Semiconductor, SCG Czech Design Center, s.r.o. Rožnov pod Radhoštěm, CZ
2002–2007	**Design/CAD Technician** ON Semiconductor, SCG Czech Design Center, s.r.o. Rožnov pod Radhoštěm, CZ
2001	**Shift Process Engineer** ON Semiconductor, Tesla Sezam, a.s. Rožnov pod Radhoštěm, CZ
2000	**Service Technician** ON Semiconductor, Tesla Sezam, a.s. Rožnov pod Radhoštěm, CZ

INTERSHIP

1998	**International Student Intership** Kapyla Vocational Institut, City of Helsinki, Finland

LANGUAGES

English	Fluent
Russian	Elementary

CERTIFICATIONS

2014	ELDO Simulation (Mentor Graphics GmbH)
2013	IC Design with Pyxis (Mentor Graphics GmbH)
2011	Advanced Analog CMOS IC Design (Swiss Federal Institute of Technology) *in Lausanne, Switzerland*
2010	Analog Modeling and Simulation with Spice (Cadence Design Systems GmbH)
2010	Ample (Mentor Graphics GmbH) *in Munich, Germany*
2007	IC-CAP (Agilent Technologies) *in Paris, France*
2006	IC Station Custom Training (Mentor Graphics GmbH)
2004	Skill Language Programming (Cadence Design Systems GmbH)
2004	Virtuoso XL Layout Editor (Cadence Design Systems GmbH)

SKILLS

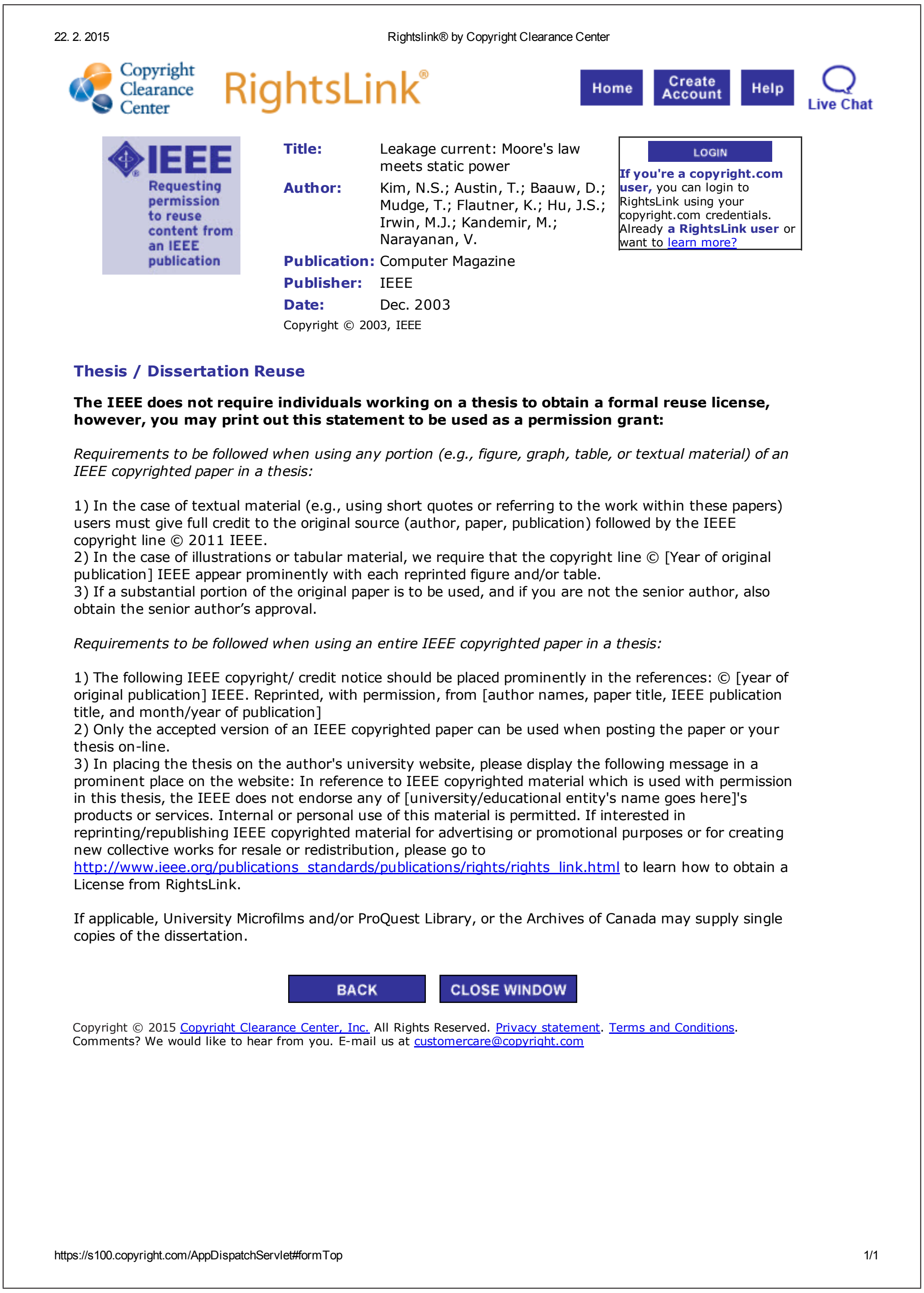
Prog. Languages	Perl, C, C++, PHP, HTML, SQL, Ample, Skill, TeX, LaTeX
Sim. Languages	Spice, Hspice, Eldo, Spectre, ADMS, Verilog-A
Design Tools	Cadence, Mentor, Calibre
Other Tools	TCAD (Synopsys), Matlab, MathCAD, ICCAP

GROUPS AND ASSOCIATIONS

Membership	IEEE Electron Devices Society IEEE Circuits and Systems Society IEEE Communications Society IEEE Microwave Theory and Techniques Society IEEE Computational Intelligence Society

Appendix D

Permission Grant



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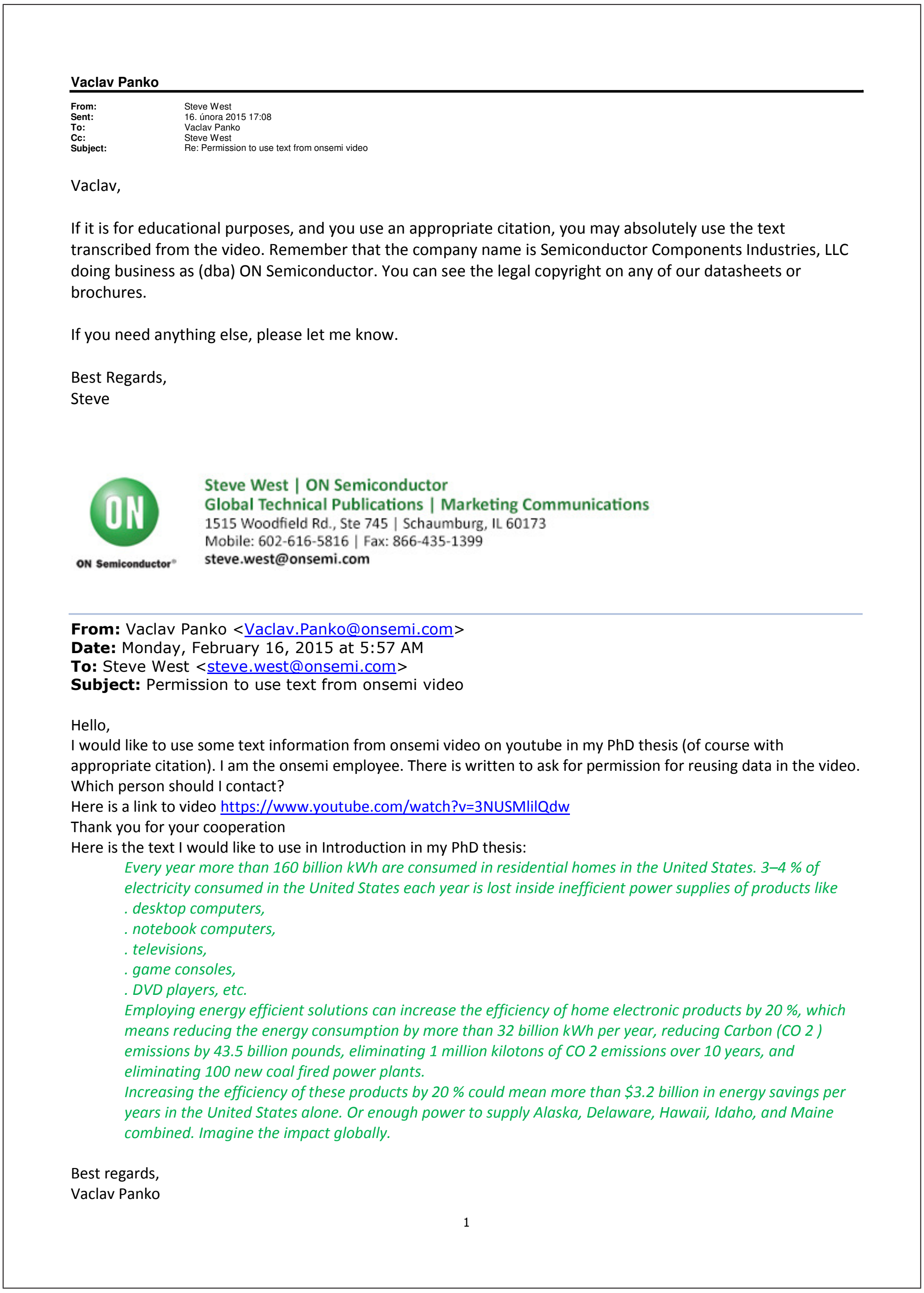

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Cc: Steve West
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> *. desktop computers,*
> *. notebook computers,*
> *. televisions,*
> *. game consoles,*
> *. DVD players, etc.*
> *Employing energy efficient solutions can increase the efficiency of home electronic products by 20 %, which means reducing the energy consumption by more than 32 billion kWh per year, reducing Carbon (CO 2) emissions by 43.5 billion pounds, eliminating 1 million kilotons of CO 2 emissions over 10 years, and eliminating 100 new coal fired power plants.*
> *Increasing the efficiency of these products by 20 % could mean more than $3.2 billion in energy savings per years in the United States alone. Or enough power to supply Alaska, Delaware, Hawaii, Idaho, and Maine combined. Imagine the impact globally.*

Best regards,
Vaclav Panko