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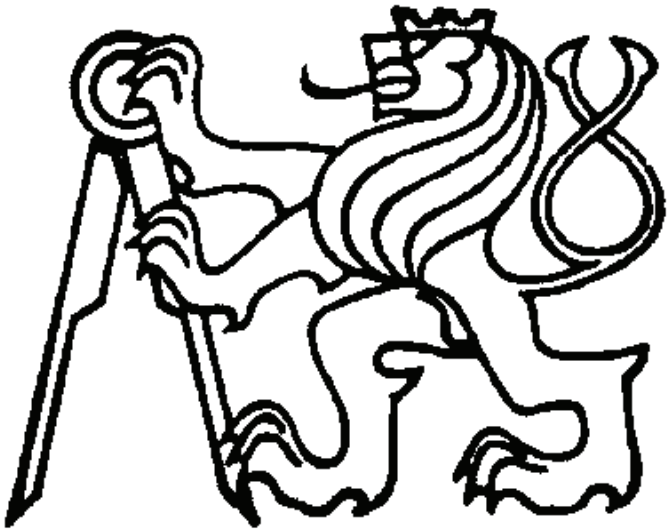

DOCTORAL THESIS STATEMENT

Czech Technical University in Prague
Faculty of Electrical Engineering
Department of Electric Drives and Traction

Pavel Kobrle

CONTROL STRATEGY OF FIVE-LEVEL FLYING CAPACITOR INVERTER

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1 CURRENT SITUATION OF THE STUDIED PROBLEM

1.1 Introduction

Despite the progress, the parameters of the devices are still not high enough for the use in "classical" three-phase inverters with six power semiconductor devices for the MV or HV applications (Thielemans *et al.*, 2009), e.g. for variable speed drives (the electric traction, winding engines, pumps for long-distance transport of gas and liquid mediums etc.) (Stemmler, 1993; Hammond, 1997) and for compensatory and filtration applications (Fujita *et al.*, 1995). With the growth of non-linear loads such as cycloconverters, rectifiers, arc furnaces and asymmetrical loads, the active power filters are also widely used due to the clearing of high disturbances in the power supply system (Yoshioka *et al.*, 1996; Bollen, 1999; Martins *et al.*, 2011). Classical semiconductor inverters switch on high frequency between the positive and the negative pole and have high conduction losses, relatively. Both, the voltage step between two poles and the higher switching frequency exert influence over the quality of an output voltage waveform. If the required output voltage is higher than the rate value of power electronic devices available on market then some method of voltage reduction per one device must be used. Lower voltage stress can be achieved by connecting them in series – this method has been widely used for more than 35 years, e.g. in the first light high voltage direct current (HVDC) transmission link between Hellsjön and Grängesberg in 1997 (Eriksson *et al.*, 1998). Input DC voltage of both inverters is ±10 kV, i.e. 20 kV between levels. Output RMS line-to-line voltage of inverter is 10 kV. The distance between stations is 10 km. In each arm there are 22 in series connected IGBTs. The IGBTs were selected according to small deviation of parameters. This selection allows complying a uniform voltage distribution between the transistors. The advantage of this method is simple control strategy; as disadvantages we should mention the above mentioned selection of transistors and the high voltage changes caused by switching of one arm. That is why this method is not practically used. In addition, to connect IGBTs in series is possible only with auxiliary circuits (Baek *et al.*, 2001).

Other, modern solution is to feed the electric drives from multilevel converters (MCs), mostly from multilevel inverters (MIs) that provide the possibility to eliminate series connected semiconductor devices in the MV and HV applications which is considered the main problem.

Using them in these applications resolves not only the problem of voltage equable distribution across semiconductor switches, but it also makes possible to:

- eliminate the need of bulky and expensive step-down transformers,
- reduce the connection cables cross-sections,
- improve the harmonic content of output voltage and phase current consequently thanks to output quantity waveforms; as a result better electromagnetic compatibility is obtained,

- reduce the costs of output filters thanks to lower d*v*/d*t* stress of semiconductor switches (the dielectric stress of motor winding insulation which occurs due to reflections inside the cables is reduced),
- operate in applications where semiconductor switches are not able to operate at high switching frequencies.

Of course, the MCs also have several drawbacks. The large number of semiconductor devices ranks among the most obvious drawbacks. With the increasing number of voltage levels, the number of semiconductor devices rises. Besides, more voltage levels require more passive elements; each semiconductor switch needs its own driver, it is necessary to have an independent galvanic isolated zero potential for each driver etc. The MC turns into a larger and more complex system, especially when it comes to spatial demands, construction, measurement and control.

Some disadvantages and limitations depend on the particular topology of the MC. As Thai (2003) mentions, diode-clamped multilevel topology brings the problem of a DC link voltage unbalance, and consequently of unequal stress across semiconductor devices, H-bridge multilevel topology depends on separated DC sources, and flying (clamping) capacitors topology is limited by the heat capacity of the flying capacitors etc. Even the M^2C topology needs many separate, isolated DC-supplies or battery parts (Marquardt, 2010).

Although MCs can operate with lower switching frequency, there are several applications, e.g. MV or HV active filters or power line conditioners, for which the switching frequency is the limiting parameter.

1.2 Multilevel Converters

The essence of the MC is to divide the output phase voltage range (bordered by two levels – upper and lower one) into several inner levels with an equal voltage distance from each other. The magnitude of this distance determines the permitted voltage stress of the semiconductor devices that are used. If this distance gets wider, the voltage stress increases across the first device and decreases across the second one. When this deviation becomes excessively large, the device can be endangered and the core of the MC gets lost. That is why ensuring correct and constant voltage levels is one of the most important control tasks. It is usually called a voltage balancing.

The first and the simplest MCs were not based on the semiconductor technique, but on a magnetic coupling. The waveform of the output multilevel voltage was obtained by adding several rectangle voltages that were produced by classical inverters under square-wave control. Their rectangle phase shifted output voltages supplied the coupling transformers and the voltages summed on the secondary sides of these transformers were added into a staircase multilevel waveform.

The first MC based on semiconductors was described and constructed by Baker and Bannister (1975). It was a cascaded topology, which is a serial connection of one-phase converters. Today, these converters are known as cascaded H-bridge converters.

The cascaded H-bridge converters are nowadays widely used because of their very good harmonic spectrum and because of their relatively easy control. We can find them in applications such as automotive all-electric drives, automotive hybrid drives (Tolbert *et al.*, 2002), power line conditioners (Peng *et al.*, 1997; Tolbert *et al.*, 2000), static var generation (Peng *et al.*, 1996; Peng and Lai, 1997) and compensation (Joos *et al.*, 1997) and converters for renewable energy sources (Tolbert and Peng, 2000).

For illustrative purposes, the contemporary power and voltage values of produced converters are presented. Siemens manufactures this type of inverter (Perfect Harmony) to power 30 MVA at 13.8 kV with IGBTs, ABB in five-level performance to power 24 MVA at 6.9 kV with IGCTs (Beuermann *et al.*, 2006).

Five years after the description and realization of the first cascaded H-bridge MC, Baker (1980) proposed a new topology – a neutral-point-clamped multilevel inverter, namely a three-level and a five-level connection. However, just one year later Nabae, Takahashi and Akagi (1981) published an article concerning the implementation of pulse-width modulation for this topology and they introduced their first results of the three-level performance. This topology was the first one that made it possible to produce an output voltage from only one DC source.

In industrial applications appear three-, four-, five-, six- and seven-level converters. Like the H-bridge MCs, the diode-clamped converters are also used as static var compensators (Hochgraf *et al.*, 1994; Menzies and Zhuang, 1995). This topology is also quite popular in motor drive applications (Tolbert *et al.*, 1998; Tolbert *et al.*, 2002), however only in a three-level performance because diode-clamped converters of more than three levels cannot be stabilized without any auxiliary power circuits (Sivkov, 2011). Lai and Peng (1996) designed a diode-clamped inverter as an interface between HV DC and AC transmission line, Schneider Electric uses this topology for its medium power UPS systems (Rizet, 2010). This topology in a three-level performance was also the base of the first unified power-flow controller in the world (Renz *et al.*, 1998).

To illustrate this, today's power relations are obvious from the following: Siemens manufactures this type of converter to power 28 MVA at 4.16 kV with IGBTs, ABB to power 27 MVA at voltage 3.3 kV with IGCTs, Converteam to 42 MVA at 6.6 kV with PP-IGBTs (Beuermann *et al.*, 2006).

During the 1980s the development of the MCs did not move much forward. Only after ten years, at the turn of the decade, finally appeared articles about new applications, e.g. nuclear fusion, and new control methods. The next turning point came at the beginning of the 1990s when Meynard and Foch (1992) presented the flying capacitor converter – as a multilevel chopper and a multilevel inverter (FCMI).

The advantage of this topology is that it has redundant switching states for inner voltage levels. Therefore, the flying capacitors can be balanced with the control strategy only. However, the control is complicated for high number of levels. The three-, four- and five-level flying capacitor inverters (FCIs) operates mostly for motor drive applications, on the other

hand the six- and seven-level FCIs operates in applications with reactive power compensation (Huang and Corzine, 2006).

Nowadays, the four-level flying capacitor inverters of power 8 MVA at 4.2 kV with IGBTs are produced by Converteam (Bernet and Sommer, 2010), at 6 kV with IGCTs and at 10 kV with IGBTs by ČKD Elektrotechnika, a.s.

The last crucial topology appeared just after the turn of the millennium when Lesnicar and Marquardt (2003) presented the modular multilevel converter (M^2C). It looks a little bit like the first H-bridge topology, but the difference is in the use of half bridges instead of full bridges.

M^2C is strictly modular and it does not need any additional external components or circuits for a four-quadrant operation of the converter. What is worth noticing is that there is no capacitor in the DC link. This fact rapidly decreases the possibility of a short circuit in the DC link. With respect to the reliability and safety it is very beneficial to replace the damaged submodule during the converter operation without switching it off.

Except for the above mentioned advantages, Marquardt (2010) adds the following: there is no need of passive filters on the AC side, there are very low switching losses, the efficiency is high and there is fully dynamic control of both the AC and the DC side. As drawbacks he mentions insufficient maximum temperatures of capacitors with high energy density and bulky capacitors that hamper integration.

Today this converter topology is still in the centre of interest because it is suitable for solar power generation, HVDC transmission, and especially for grid connection of off-shore wind plants (Gambach and Schuster, 2010), power supply of large cities and electric supplies for railway grids (Nee, 2010). Converters of the M^2C topology are employed in the project Skagerrak 4 of the Norwegian and Danish state-owned energy enterprises Statnett and Energinet.dk. This ca 240 km long HVDC Light transmission between Danmark and Norway will be of 700 MW power rating; the voltage levels on both AC sides are on 400 kV, on the DC side 500 kV (Statnett, 2013).

1.3 Modulation Techniques for Flying Capacitor Multilevel Inverters

The modulation techniques for the MIs evolved from the modulation techniques of classical two-level inverters (Hussein, 2009). The most widely utilized modulation is the pulse width modulation (PWM) for controlling of voltage source inverters (Holmes and Lipo, 2003). Another popular modulation technique is the hysteresis modulation for control of the current output of voltage source inverters (Shukla, 2011). PWM is the technique which changes the switch-on/switch-off ratio (duty cycle) of the inverter switches at a high switching frequency in order to achieve the desired average low frequency voltage or current output. The classification of PWM techniques is not unified; even in the field of two-level inverters. The authors sometimes contradict each other. Anyway, it can be generally said that the PWM techniques for multilevel inverters can be divided into three main groups - programmed PWM, carrier-based PWM and space vector PWM - that are described in the Thesis together with the voltage balancing algorithm across the flying capacitors.

2 AIMS OF THE DOCTORAL THESIS

The aims of this Thesis are:

- to summarize the pieces of knowledge about FCMIs and their control strategies,
- to analyze and to evaluate the potential switching processes for a five-level FCI,
- to create a functional simulation model of a three-phase five-level FCI,
- to design and construct a compact laboratory model of a three-phase five-level FCI,
- to verify the conclusions drawn from the previous analysis,
- the evaluation of the possibility to use a multilevel inverter as an active filter.

3 WORKING METHODS

Analysis of the Switching Process of the Five-level FCI

In the introduction of the Thesis was stated that the switching process of a MI is patterned on a switching process of a classical two-level inverter as it is supposed in literature including substantial publications such as (e.g. Corzine and Kou, 2003; Huang and Corzine, 2006; McGrath and Holmes, 2007; Escalante *et al.*, 2002; Meynard *et al.*, 1997; Lai and Peng, 1996). However, theoretically another possibility of switching for MI can be implemented, as was for the first time published in (Kobrle and Pavelka, 2010) for the case of a four-level FCI.

3.1 1C-transitions of Five-level Flying Capacitor Inverter

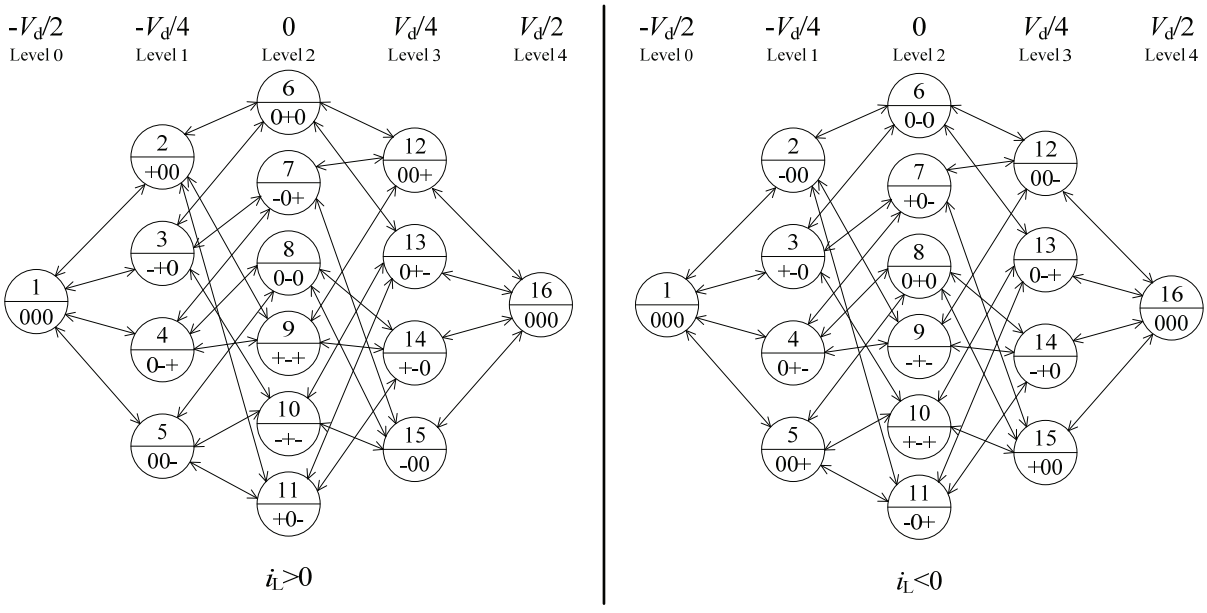

Fig. 1 State diagrams of a five-level FCI for 1C-transitions

There is described in details and explained in the Thesis how the three-level FCI switches and what is the complementary switching. Then, it is shown that the principle of the complementary switching is the same also in case of more-level FCI. A switching process of MIs patterned on a switching process of classical two-level inverters mentioned above

means that only one complementary switching pair switches in one phase leg by turning over. However, a five-level FCI enables turning over of up to four complementary switching pairs at the same time. It will be kept following marking: under 1C-transition is understood the transition when one commutation occurs (one complementary switching pair turns over); under 2C-transition is understood the transition when two commutations occur (two complementary switching pairs turn over); under 3C-transition is understood the transition when three commutations occur (three complementary switching pairs turn over); under 4C-transition is understood the transition when four commutations occur (all four complementary switching pairs turn over). The similar analysis of switching as for two-level inverter will be performed for all three possibilities of the five-level FCI further.

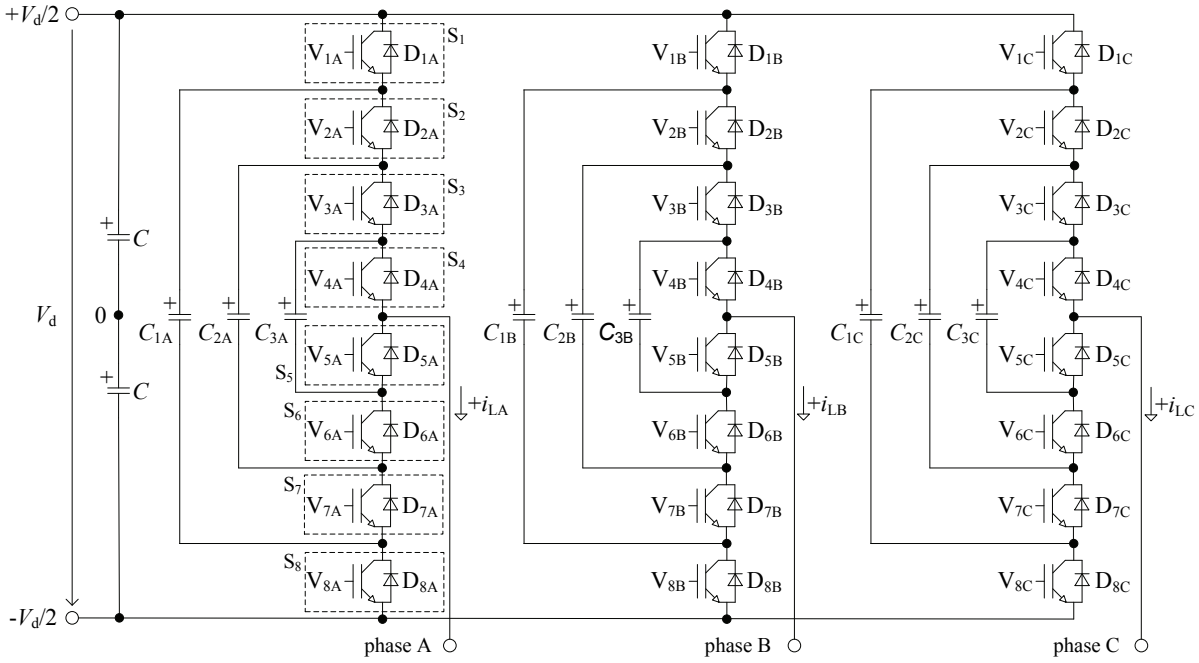

Fig. 2 Basic scheme of a three-phase five-level flying capacitor multilevel inverter

All possible 1C-transitions of a five-level FCI (Fig. 2) are depicted in the state diagrams presented in Fig. 1. There are 64 of them for each direction of the load current i_L. Let us select a sample of transitions for one phase and with the help of it explain the principle of the 1C-transition. The sample transition we chose is from the switching state 6 to 2 and back, for a positive load current. The transitions are shown in Fig. 3. The power devices S_{1A}, S_{2A}, S_{5A} and S_{6A} from Fig. 2 are turned on in the state 6. The load current flows through V_{1A}, V_{2A}, D_{6A} and D_{5A} and the output terminal A is connected to the voltage 0. At the time t_1 the switch S_{2A} turns off, the load current begins to commutate to the diode D_{7A} and the output terminal A is on potential $-V_d/4$. Thanks to this commutation the inverter is transferred directly from the switching state 6 to 2. If the load current does not decrease due to high inductance during the blank time, it no more depends on the time t_2 when the switch S_7 turns on. For a reverse transition, the switching state 2 is the initial state. At the time t_3 the switching cell S_{7A} turns off but the current keep flowing through the diode D_{7A}, so the switching state stays 2. After turning the S_{2A} on at t_4 the current commutates from D_{7A} to V_{2A} and on the output terminal the voltage 0 appears – the inverter is in the switching state 6 again.

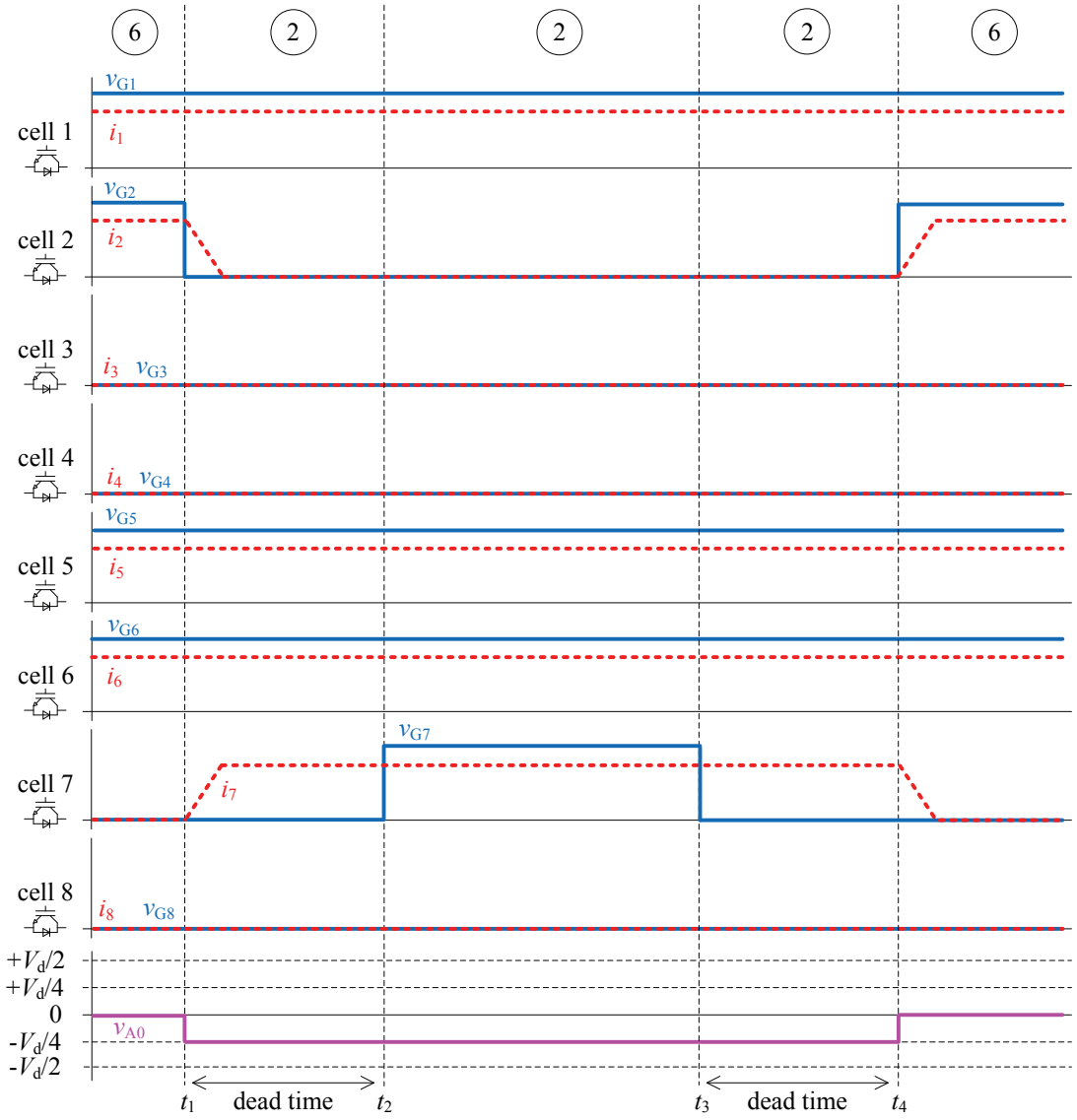

Fig. 3 1C-transitions

3.2 2C-transitions of Five-level Flying Capacitor Inverter

All possible 2C-transitions of a five-level FCI (Fig. 2) are shown in the state diagrams presented in Fig. 5. There are 48 of them for each direction of the load current i_L. As an example, the 2C-transitions from the switching state 6 to 7 and back for a positive load current are selected. The transitions are depicted in Fig. 4. The power devices S_{1A}, S_{2A}, S_{5A} and S_{6A} are turned on in the state 6. The load current flows through V_{1A}, V_{2A}, D_{6A} and D_{5A} and the output terminal A is connected to the potential 0. At the time t_1 switches S_{1A} and S_{6A} turn off, the dead time begins and the load current commutates to the diode D_{8A}. This closed circuit corresponds to the switching state 3, so the output terminal A is on potential $-V_d/4$. After the dead time at time t_2 the switching cells S_{3A} and S_{8A} turn on, the load current commutates from the diode D_{6A} to the valve V_{3A} and the output terminal is connected back to the potential 0. The back transition begins with turning the switching cells S_{3A} and S_{8A} off. At the beginning of the dead time at t_3, the load current commutates from V_{3A} to D_{6A}. The state that just passed corresponds to the switching state 3, the voltage $-V_d/4$ appears on the

output terminal A. At the end of the dead time t_4 the load current commutates from the D_{8A} to V_{1A} thanks to turning the S_{1A} and S_{8A} on and this ensures the switching state 6 which means there is a 0 potential on the output terminal.

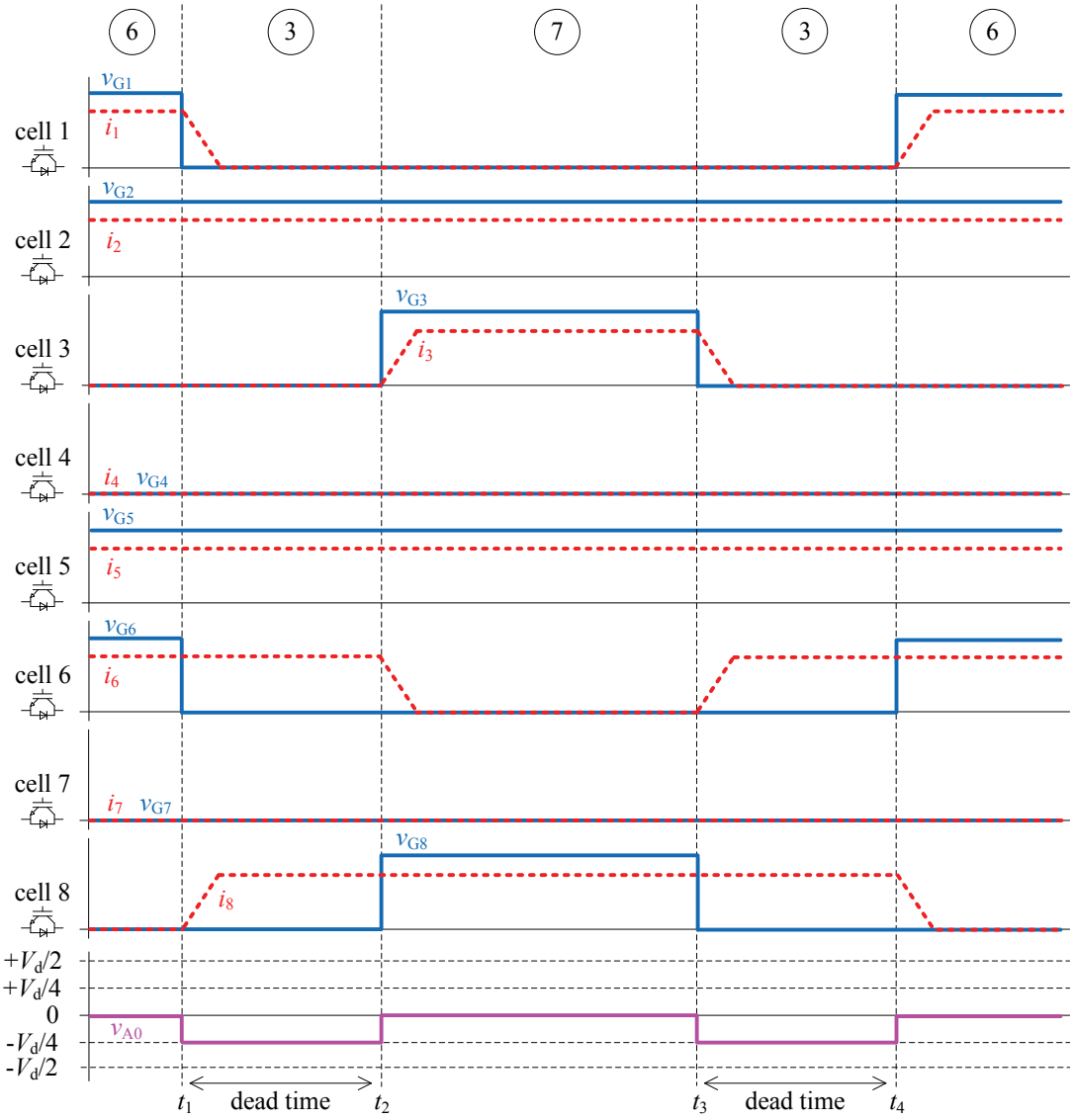

Fig. 4 2C-transitions

The crucial difference between 1C- and 2C-transitions lies in the dead time. Since the voltage stays constant in the case of the 1C-transitions, it alternates between two neighbouring voltage levels in the case of the 2C-transitions. A request for a switching within one voltage level means the increase of switching frequency, practically because of the possibility to switch in each modulation cycle. However, it does not contradict the core of MIs.

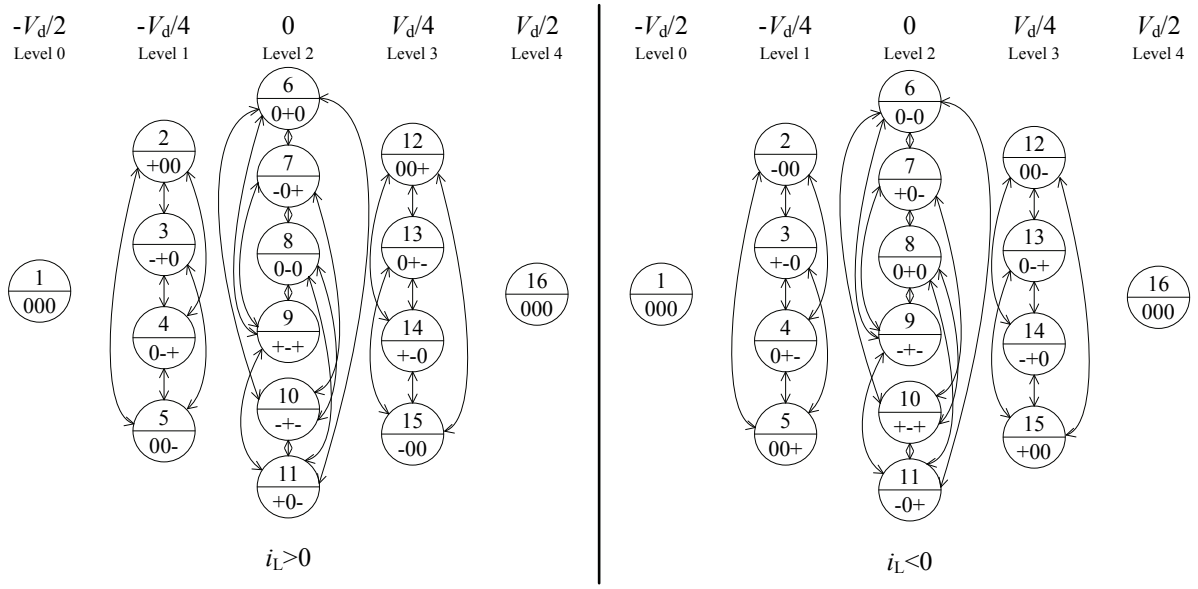

Fig. 5 State diagrams of a five-level FCI for 2C-transitions

3.3 3C-transitions of Five-level Flying Capacitor Inverter

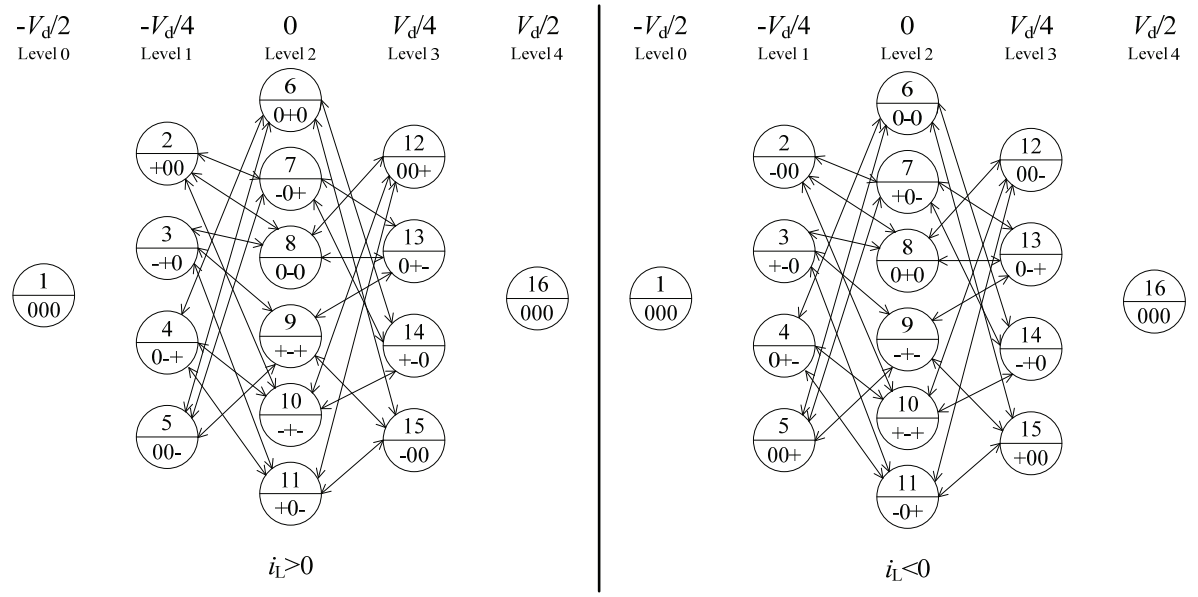

Fig. 6 State diagrams of a five-level FCI for 3C-transitions

All possible 3C-transitions of a five-level FCI (Fig. 2) are shown in the state diagrams presented in Fig. 6. There are 48 of them for each direction of the load current i_L. As an example, the 3C-transitions from the switching state 7 to 2 and back for a positive load current are selected. The transitions are depicted in Fig. 7. the power devices S_{2A}, S_{3A}, S_{5A} and S_{8A} are turned on in the state 7. The load current flows through V_{2A}, V_{3A}, D_{5A} and D_{8A} and the output terminal A is connected to the voltage 0. At the time t_1 the switches S_{2A}, S_{3A} and S_{8A} turn off, the dead time begins and the load current commutates from V_{2A} to D_{7A} and from V_{3A} to D_{6A} - D_{8A} keeps conducting. This closed circuit corresponds to the switching state 1, so the output terminal A is on potential $-V_d/2$. After the dead time at the time t_2 the switching cells S_{1A}, S_{6A} and S_{7A} turn on, the load current commutates from the diode D_{8A} to the valve

V_{1A} and the output terminal is connected to the potential -V_d/4, because the inverter is in the switching state 2. The transition back to state 7 begins with turning the switching cells S_{1A}, S_{6A} and S_{7A} off. At the beginning of the dead time at t_3, the load current commutates from V_{1A} to D_{8A}, the diodes D_{6A} and D_{7A} keep conducting. The state that just passed corresponds to the switching state 1, the voltage –V_d/2 appears on the output terminal A. At the end of the dead time at t_4 the load current commutates from D_{7A} to V_{2A} and from D_{6A} to V_{3A} thanks to turning the S_{2A} and S_{3A} on and that ensures the switching state 7 which means there is a potential 0 on the output terminal.

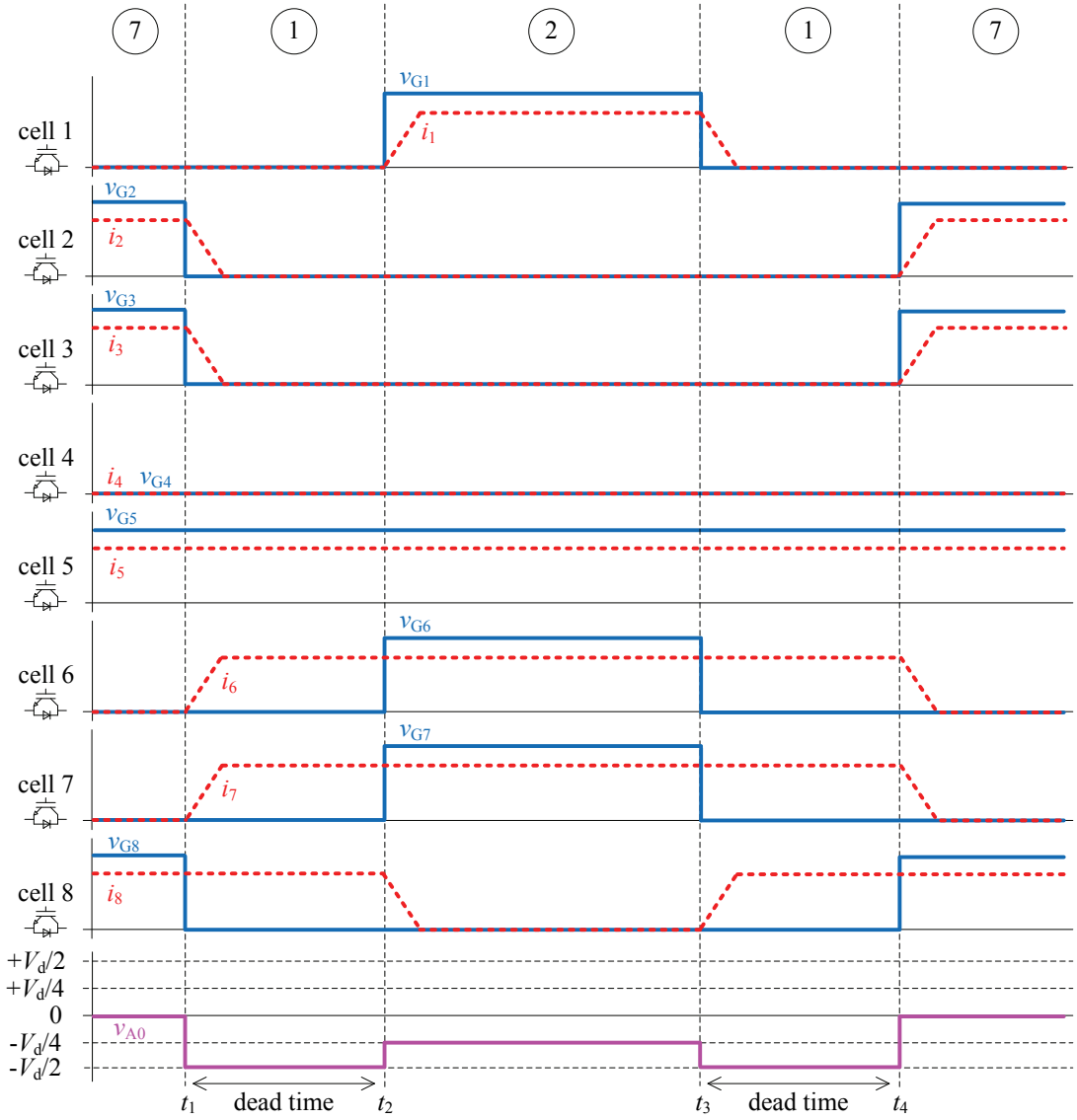

Fig. 7 3C-transitions

The above mentioned description and the Fig. 7 clearly show that between two required neighbouring states another switching state appears. The 3C-transition involves a step over two voltage levels. The reason for this is the dead time. During the dead time, the one pole of the load is connected either to a positive or to a negative polarity of the DC link. A step over two voltage levels is not acceptable because the voltage stress across the semiconductor

devices would in such a case be too big and the main purpose of the multilevel topology was vain. That is why the 3C-transitions are not permitted in proper operation of the FCMI.

4 RESULTS

4.1 Experimental Results of Switching with 1C-transitions

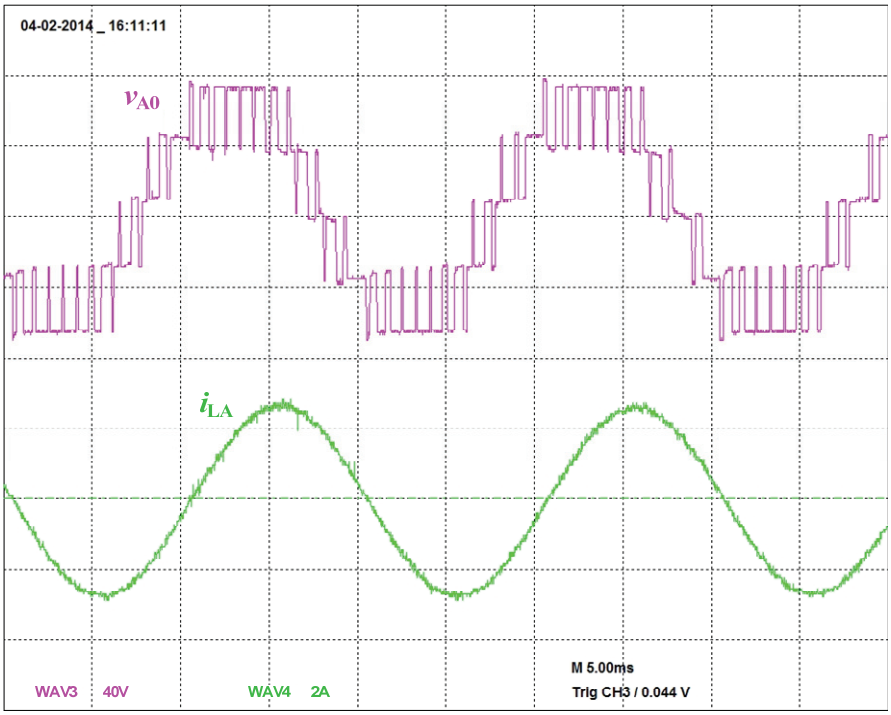

Fig. 8 Waveforms of v_{A0} and i_{LA} in the case of 1C-transitions; f = 50 Hz, M = 0.95, RL load

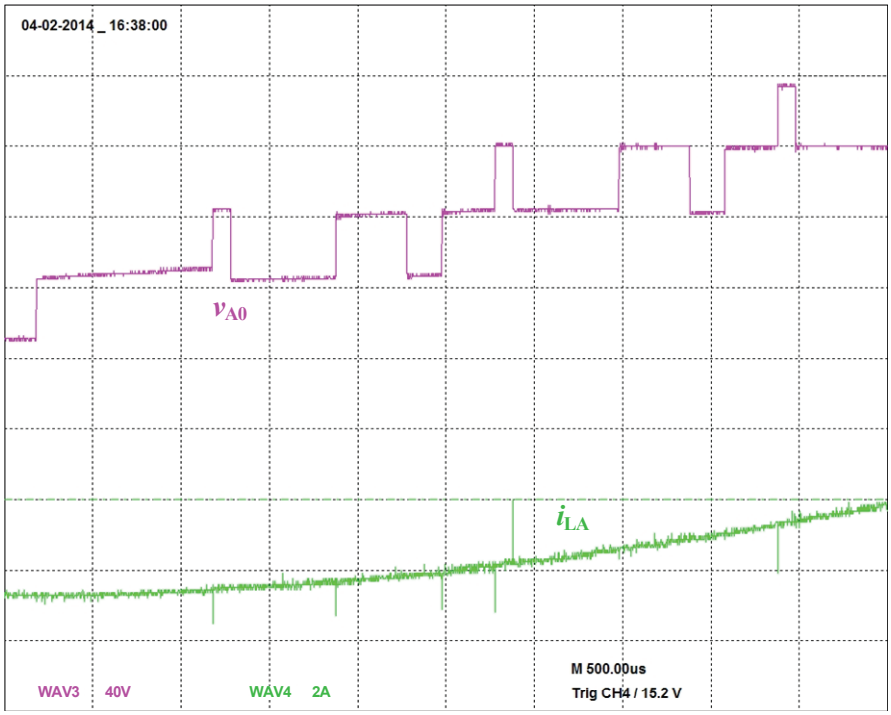

Fig. 9 A detail of waveforms in the case of 1C-transitions; f = 50 Hz, M = 0.95, RL load

The waveforms of the resistive-inductive (RL) load are depicted in Fig. 8. The important message of the above mentioned analysis is that the expected transitions are only in the voltage waveform. There are neither any spikes reaching to the neighbouring voltage level nor over one level. Fig. 9 shows it in more detail.

4.2 Experimental Results of Switching with 2C-transitions

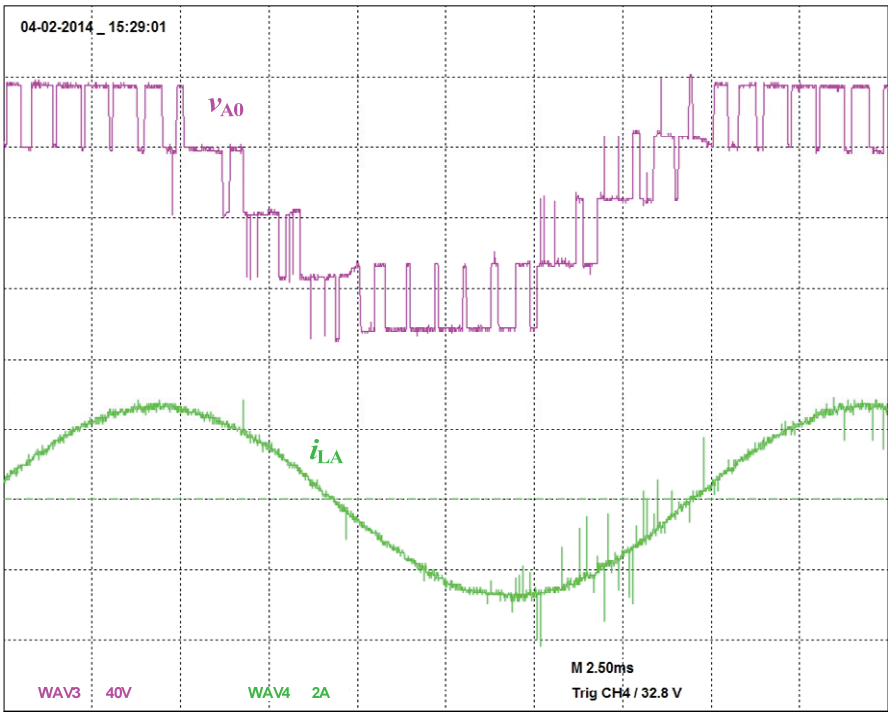

Fig. 10 Waveforms of v_{A0} and i_{LA} in the case of 2C-transitions; f = 50 Hz, M = 0.95, RL load

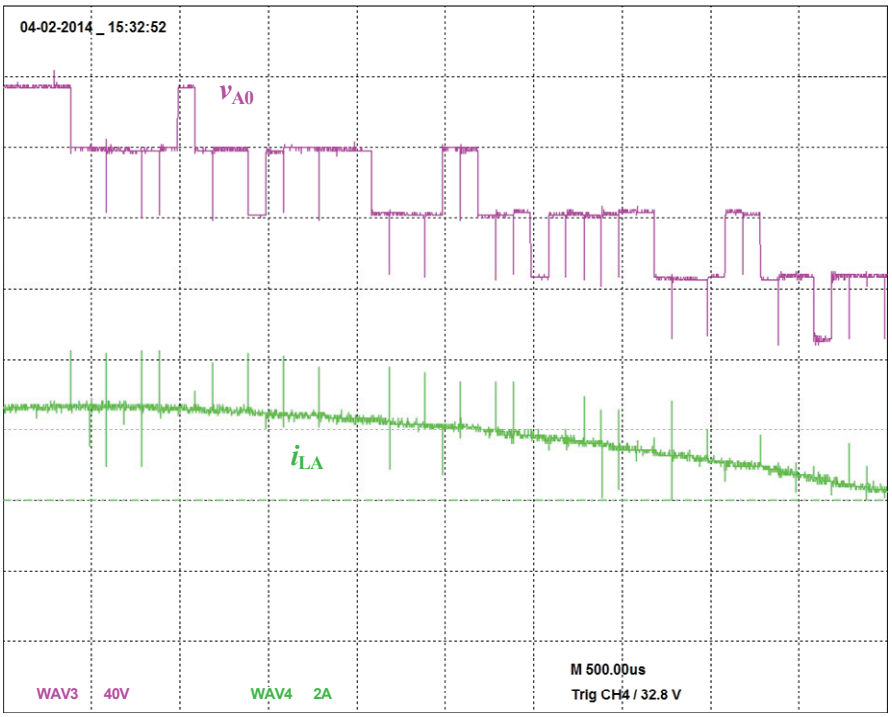

Fig. 11 A detail of waveforms in the case of 2C-transitions; f = 50 Hz, M = 0.95, RL load

Oscillograms with the five-level voltage and a corresponding current for the switching process with 2C-transitions are depicted in Fig. 10. That the transitions in question are the 2C-transitions is obvious thanks to the short spikes in the voltage waveform whose height does not exceed two neighbouring levels. They are as wide as the dead time (if rising and falling times are neglected). A detail of the 2C-transitions is depicted in Fig. 11. It is quite obvious that the switching appears every 100 μs. This correlates with the duration of one step the dSpace works with. Hence, the switching frequency increases. That corresponds with the conclusions concerning the 2C-trasitions drawn from the analysis in chapter 3.2.

4.3 Experimental Results of Switching with 3C-transitions

Oscillograms with five-level voltage and a corresponding current for the switching process with 3C-transitions are depicted in Fig. 12. That the transitions in question are the 3C-transitions is obvious thanks to the short spikes in the voltage waveform that are as high as the extent of three neighbouring levels. A detail of the 3C-transitions is shown in Fig. 13. The “forbidden” transitions reaching over two levels can be distinctly seen. Although these spikes correspond with the period of a dead time, they are unacceptable for a MI operation. The experiment results also confirm the conclusions about the 3C-transitions drawn from the analysis in chapter 3.3.

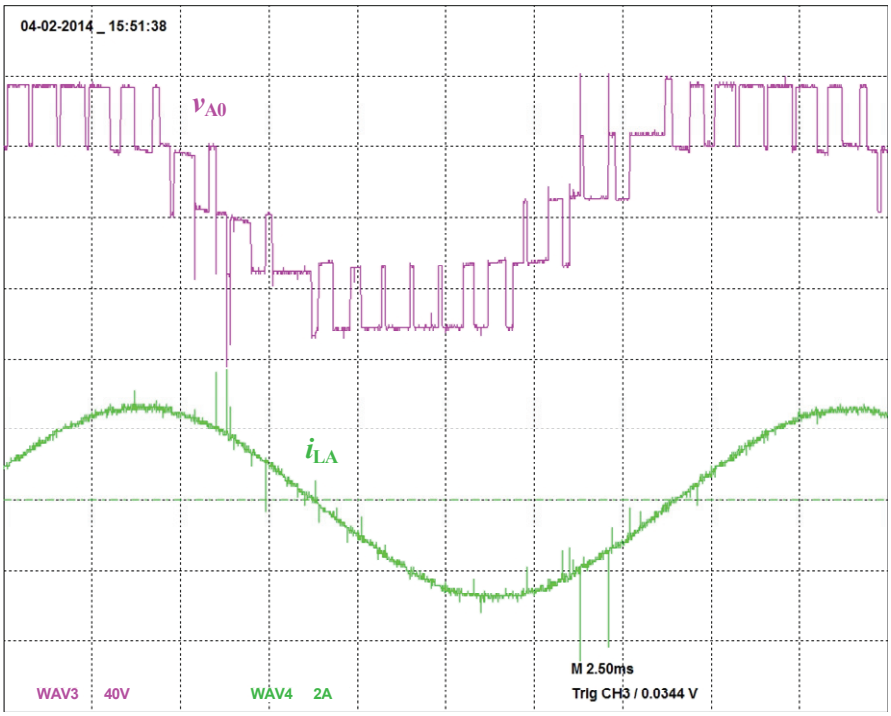

Fig. 12 Waveforms of v_{A0} and i_{LA} in the case of 3C-transitions; f = 50 Hz, M = 0.95, RL load

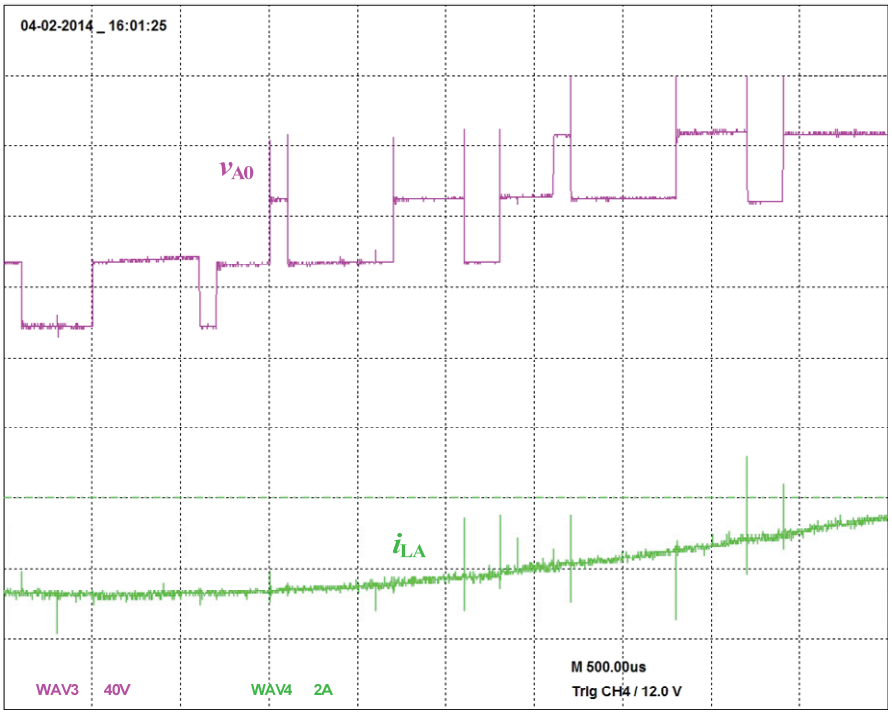

Fig. 13 A detail of waveforms in the case of 3C-transitions; f = 50 Hz, M = 0.95, RL load

5 CONCLUSION

5.1 Overview of Results and Contributions

As can be seen from the Table of contents of this Thesis, it yielded both theoretical and practical results.

The pieces of knowledge about flying capacitor multilevel inverters and their control strategies have been presented. The three-, four- and five-level FCIs are described and the five-level FCI has been treated in more detail. It is also shown why, in reality, the FCIs are not used with more than seven levels. The popular modulation strategies are summarized with the emphasis on carrier-based PWM. The topic of flying capacitor voltage balancing without any auxiliary power circuit is explained as well as its control algorithm for the five-level FCI.

Next, the analysis of switching processes is performed, accompanied by particular examples. It is shown why switching over of one complementary switching device pair (1C-transitions) is preferably used. From the analysis follows – apart from other things – that the switching over of two complementary switching pairs (2C-transitions) is also possible, however, it leads to an increase of the switching frequency because the modulator instructs to switch over at each operational step. The performed analysis also considers the switching over of three complementary switching pairs (3C-transitions). In this case, it is shown that this manner of switching cannot be permitted because of the voltage jumps over two levels in

the dead time which is an unacceptable transition considering the very core of multilevel inverters.

Furthermore, the dynamic model of the three-phase five-level FCI was created. Both the power part and its control part have been realized in Matlab-Simulink. The control algorithm has been designed with regard to its subsequent implementation into the real-time control system dSpace. Both the balancing algorithm and the performed analysis have been verified thanks to this model which was confirmed by the simulation results that have also been presented. The results show that, according to our expectations, the switching process with the 2C-transitions improves the voltage balancing of the flying capacitors. On the other hand, the switching process with 3C-transitions has no apparent effect on voltage balancing.

Because of the balancing algorithm and the performed analysis a real verification of the compact laboratory model of the three-phase five-level FCI has been realized. Also the compact unit of the DC link for the FCI has been realized because the flying capacitors must not be clamped by auxiliary resistors. The measured voltage and current oscillograms prove that the laboratory model operates correctly.

All three switching processes have been implemented into the laboratory model of the FCI. The obtained results fully confirm the conclusions following from the performed analysis and simulations.

One theoretical chapter is devoted to the evaluation of the possible use of a multilevel inverter as an active filter. Specific requirements for medium voltage inverters operated as active filters are discussed – topology, semiconductor devices, switching frequency and supply voltage in the DC link. It is explained that for MV active filters the multilevel topology with IGBTs is appropriate. Besides, it is shown that (and in what way) the DC link voltage should be determined with respect to the order of the filtered harmonics and on the power factor. The basic possible control methods are briefly discussed. Also, the simulation model of the five-level FCMI, which is controlled by the hysteresis current control, has been created.

5.2 Suggestions for Follow-up Development

One possible way, how to improve the voltage stabilization process, seems to be the on-line changing of flying capacitor nominal voltages according to the actual voltage in the DC link.

For further development, the flying capacitor pre-charging process should stay in focus. The attempt to eliminate the pre-charging resistor and the electric contactor could secure cheaper production because the DC electric contactors for MV applications are (even nowadays) quite expensive and their space requirements are not negligible.

As far as the multilevel active filter is concerned, the control strategy that keeps the voltage in the DC link constant has not been dealt with in this Thesis. However, for the prospective use of the FCMI in practice, it will be necessary to take it into consideration.

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10 SUMMARY

This Thesis deals with the control strategy of five-level flying capacitor inverters (FCI). At the beginning, the subject of multilevel inverters is generally discussed. The crucial topologies and their schemes are introduced, their principal functions are described and their use is mentioned.

After the initial state-of-art overview, the flying capacitor multilevel inverter (and particularly the five-level FCI) and its different performances are described in detail. Furthermore, the most important modulation techniques, as well as the voltage balancing of flying capacitors are explained. The core of this Thesis is the analysis of possible switching modes and the verification of their applicability. Afterwards, a simulation model of a three-phase five-level FCI is introduced and the simulation results are presented.

The third chapter discusses the possibility of using the flying capacitor multilevel inverter as an active filter. Several specific requirements are taken into consideration and subsequently analyzed, the simulation model is presented together with the simulation results.

Finally, a laboratory model of the three-phase five-level flying capacitor inverter is introduced and described. At the end, the experimental results are introduced and it is shown that they confirm the correctness of the propounded switching analysis.

11 RÉSUMÉ

Předložená disertační práce se zabývá řídicí strategií pětiúrovňového střídače s plovoucími kondenzátory. Na začátku práce je shrnuta problematika víceúrovňových měničů obecně. Jsou v ní popsány klíčové topologie a jejich schémata, je vysvětlen princip jejich funkce a ke každému typu jsou uvedeny aplikace, v nichž se střídače používají.

Po úvodní přehledové části následuje detailní popis víceúrovňového měniče s plovoucími kondenzátory ve tří-, čtyř- a pětiúrovňovém provedení, přičemž v dalších částech se práce zabývá už jen pětiúrovňovou variantou střídače. Dále jsou uvedeny a vysvětleny jak důležité techniky modulací pro víceúrovňové střídače, tak i algoritmus pro udržování požadovaného napětí na plovoucích kondenzátorech. Poté je provedena analýza možných způsobů přepínání součástek, která je spolu s jejím ověřením jádrem disertační práce. Následuje popis simulační modelu třífázového pětiúrovňového střídače s plovoucími kondenzátory i prezentace výsledků simulací, týkajících se provedené analýzy.

Jedna kapitola práce je věnována úvaze o možnosti použít víceúrovňový střídač s plovoucími kondenzátory jako aktivní filtr. Jsou v ní uvedeny specifické požadavky na střídač pro takovou aplikaci a je v ní představen i simulační model aktivního filtru se zmíněným střídačem. Rovněž jsou předloženy výsledky simulace.

Dále je v práci představen a popsán reálný laboratorní model třífázového pětiúrovňového střídače s plovoucími kondenzátory. Nakonec jsou uvedeny naměřené výsledky, na nichž je ukázáno, že provedená analýza možných způsobů přepínání součástek je správná.